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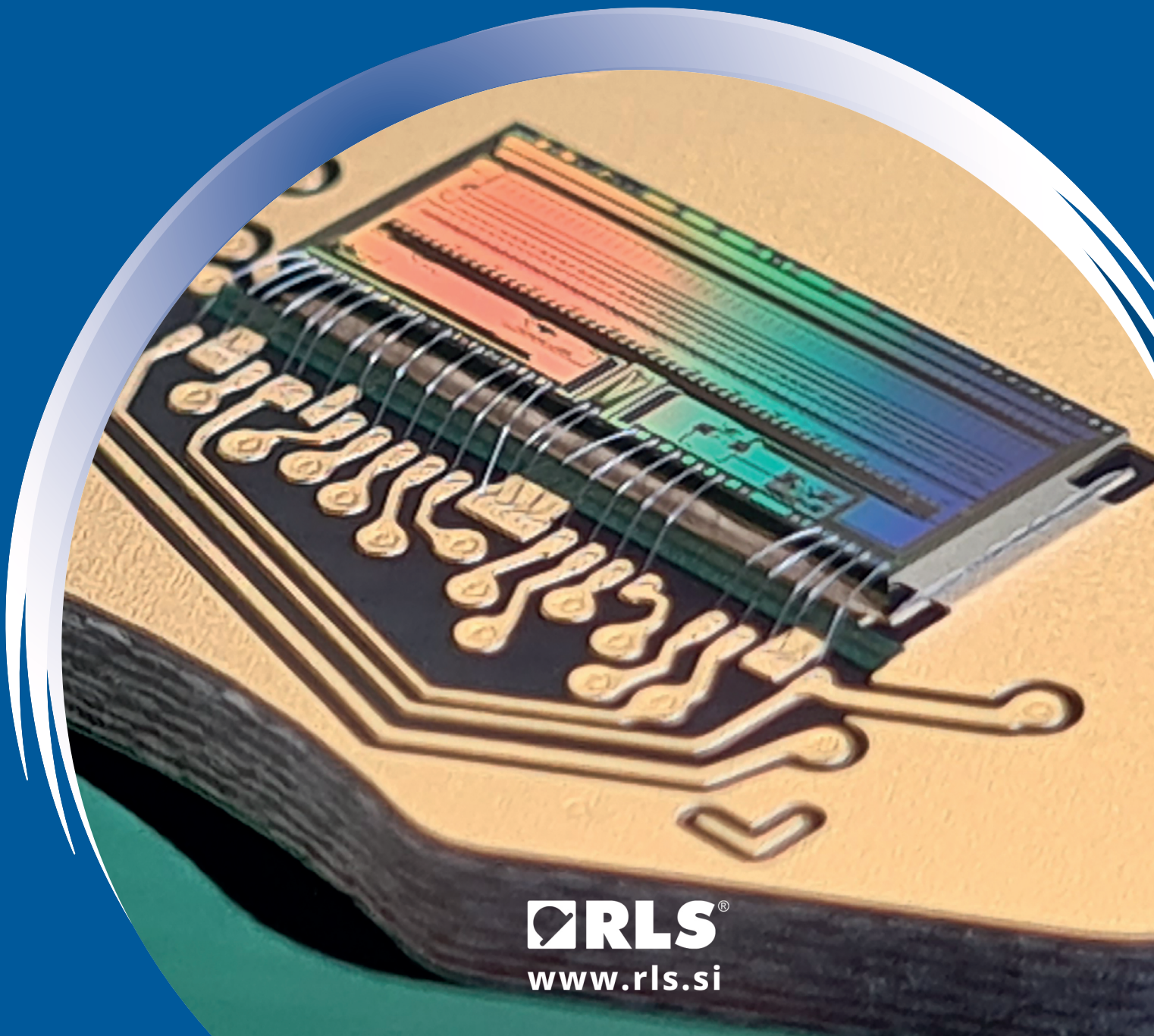

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Hardware Implementation of Residue Multipliers based Signed RNS Processor for Cryptosystems

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Abstract: The Residue Number System (RNS) characterize large integer numbers into smaller residues using moduli sets to enhance the performance of digital cryptosystems. A parallel Signed Residue Multiplication (SRM) algorithm, VLSI parallel array architecture for balanced (2^n-1, 2^n, 2^n+1) and unbalanced (2^k-1, 2^k, 2^k+1) word-length moduli are proposed which in turn are capable of handling signed input numbers. Balanced 2^n-1 SRM is used as a reference to design an unbalanced 2^k-1 and 2^k+1. The synthesized results show that the proposed 2^n-1 SRM architecture achieves 17% of the area, 26% of speed, and 24% of Power Delay Product (PDP) improvement compared to the Modified Booth Encoded (MBE) architectures discussed in the review of the literature. The proposed 2^n+1 SRM architecture achieves 23% of the area, 20% of speed, and 22% of PDP improvement compared to recent counterparts. There is a significant improvement in the results due to the fully parallel coarsely grained approach adopted for the design, which is hardly attempted for signed numbers using array architectures. Finally, the proposed SRM modules are used to design {2^n-1, 2^n, 2^n+1} special moduli set based RNS processor, and the real-time verification is performed on Zynq (XC7Z020CLG484-1) Field Programmable Gate Array (FPGA).

Keywords: signed modulo multiplication; Very Large Scale Integration (VLSI); FPGA; computer arithmetic; RNS

Strojna implementacija množilnikov ostankov na osnovi predznačenega RNS procesorja za sisteme kriptiranja

Izvleček: Številski sistem ostankov velike celoštevilske cifre v manjše ostanke na osnovi setov modulov za povečanje učinkovitosti sistemov kriptiranja. Predlagan je algoritem vzporednega množenja predznačenih ostankov (SRM) v VLSI paralelni arhitekturi za uravnotežen (2^n-1, 2^n, 2^n+1) in neuravnotežen (2^k-1, 2^k, 2^k+1) modul dolžine besede. Uravnotežen SRM je uporabljen kot referenca za načrtovanje neuravnoteženega algoritma. Rezultati kažejo, da predlagana arhitektura zajema 17% prostora, 26% hitrosti in 22% izboljšanost PDP glede na trenutne arhitekture. Izboljšava je dosežena na osnovi paralelnega načrtovanja. Verifikacija v realnem času je izvedena na Zynq FPGA.

Ključne besede: predznačeno množenjem odulov; VLSI; FPGA; računalniška arithmetika; RNS

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1 Introduction

In cloud computing and the Internet of Things (IoT), data security is one of the major concerns for service providers. Therefore a dedicated hardware cryptography support is needed for modern electronic devices [1],[2],[3][4][5]. In recent years, Elliptic Curve Cryptography (ECC) [6] has received scientific interest as it ensures more security through hard underlying mathematical problems. It leads to an increase in the length of the key, and as a result, performing faster arithmetic operations on larger integers have become the bottleneck problem. RNS based arithmetic operation [7,8] is a solution through which residue multiplication has become the heart of computation architecture. The natu-

ral defense offered by RNS against attacks is another reason for the selection of residue arithmetic as the prime candidate in cryptosystems [9,10].

Similarly to the above operation, modular exponentiation [11] is a time-critical operation that is widely used in cryptographic algorithms like RSA. The modular exponentiation operation is performed in the form of residue multiplication. Therefore, the employment of efficient high-speed residue multiplication is vital in public-key encryption and decryption.

Typical hardware implementation of the RNS based application is dependent on the chosen moduli set. The selection of RNS Moduli [12] and the width of the residue decide the efficiency and performance of the cryptosystems. A $\{2^n-1,2^n,2^n+1\}$ special moduli set representation is a pairwise relatively co-prime standard RNS. These moduli set has a unique advantage in which two or more numbers do not have the same representation. Special moduli set shows better representational efficiency [12] compared to that of other moduli set and also maintains a good balance between the different moduli in a given moduli-set. Based on the number of bits used to represent the input, moduli and residue output are classified into balanced and unbalanced word-length moduli multiplication [13] [14].

Modified Booth Encoded (MBE) modulo multiplication scheme is relatively faster and can handle both signed, and unsigned numbers, the researcher's attention turned towards it, and many modifications of the same are reported in recent years [15,16,17,18,19,20]. The residue multipliers based on diminished-1 input representation in array and bit pair recoding booth algorithm are seen in [16,17,21]. Based on the conducted survey, it is evident that there is no work based on a signed array modulo multiplication scheme reported in the literature. The reasons for the above could be based on the complexity in handling the Partial Product (PP) and poor speed performance. This is one of the reasons that have highly motivated us to attempt a proposal on an array-based high-speed area-efficient parallel SRM module for RNS. In this work, the high-speed performance is achieved by a new multiplication methodology incorporating parallelism in PP generation and addition process.

Six significant contributions for this work include (i) an SRM algorithm for 2^n-1, 2^n+1 and 2^n balanced word-length moduli (ii) an SRM for 2^k-1, 2^k+1 and 2^k unbalanced word – length moduli (iii) Mathematical modeling of SRM algorithm for each moduli (iv) VLSI characterization of proposed SRM algorithm in terms of high-speed area-efficient Carry Save Adder (CSA) architecture and very high-speed Han Carlson parallel prefix-based SRM array architecture (v) Functional verification of the proposed modules in FPGA and synthesis in ASIC (vi) Design of RNS Processor to demonstrate the effectiveness of the proposed algorithm.

The paper is structured as follows: In Section 2, the related works connected to residue multipliers with various moduli sets performance are analyzed. In Section 3, characteristic equation, algorithm, and VLSI architecture are presented for both balanced (2^n-1, 2^n, 2^n+1) and unbalanced (2^k-1, 2^k, 2^k+1) word-length moduli. The design of the RNS processor is given in section 4. In section 5, Synthesis results, performance analysis, and RNS processor implementation are presented. The conclusion for the proposed work is drawn in section 6.

2 Review of Existing Work

An MBE based 2^n-1 multiplication module to reduce the number of PPs is presented in [22]. The results show a significant improvement in area and delay. However, they fail to address power consumption. A radix-8 booth encoded RNS 2^n-1 multiplier [14] using unbalanced word length of moduli supporting sizeable dynamic range with adaptable delay to achieve less area and power consumption is presented. The same authors have designed a radix-8 2^n-1 & 2^n+1 multiplier with a balanced word length of moduli in [18] using various modulo properties. The author claims that less area and power are achieved by using CSA in [14] and parallel prefix adders in [18] for efficient addition operations with a slight increase in delay for lower bit width. Improved booth selector and encoder architecture consist of MUX, and the EXOR gate for the 2^n-1 MBE multiplication algorithm is presented in [23]. The architecture improves the speed performance and efficiency, but the introduction of MUX in selector architecture leads to a slight increase in area requirement, and also power consumption is not discussed.

A compact ordinary array structure [15] based 2^n+1 multiplication scheme by grouping the PPs and modify the correction bit are presented. The PP is reduced by the CSA tree, and the final carry propagation addition is carried out by prefix structure in order to achieve better area and delay performance in which the power consumption is not discussed. By introducing a new PP formation scheme, a binary-weighted representation based modulo 2^n+1 multiplier is presented in [19] and is extended to implement a multiply-add unit. The authors have achieved less area and power consumption with similar delay performance compared to [15]. A radix-4 MBE architecture with a diminished-1 input representation and dadda tree reduction scheme, which

can handle zero operands with better speed and area, is discussed in [16]. A compressor structure is introduced in [24] for PP reduction. This work achieves less power, delay, and consumes less area compared to [15].

A hybrid input representation approach with a radix-4 booth encoding scheme utilizing one binary-weighted operand and diminished-1 input representation for the other operand is explained in [17]. The architecture supports both odd and even value of n. The authors have achieved a compact area with an enhanced speed compared to the existing multipliers. The radix-8 booth encoded 2^n+1 multiplier for balanced word length moduli is designed in [18] using hard multiple generators, bias, and adders. The authors claim that the area and power reduction is accomplished compared to radix-4 and array type multiplier. However, there is an increase in operation time. In [20], the authors have improved the hard multiple generator method with a minimum number of bias terms compared to [18]. Two novel methods to increase the performance and to improve the efficiency of the radix-8 modulo 2^n+1 multiplier are explained in [20]. The first method significantly reduces the amount of bias, and the second one is new hard multiple generators based on a parallel-prefix structure computes carry only for odd positions. These schemes result in a lightweight parallel-prefix adder for the computation of triple the number with significant area-saving and improved fan-out. It achieves less area and power compared to the radix-8 booth multiplier [18]. There is an increase in HMG delay compared to [18] and almost maintains the same delay performance for multiplier operation compared to [18].

The problem in MBE based architecture is that it requires an efficient booth selector and encoder compared to the array-based architectures. The former scheme reduces the number of PPs and improves speed performance. However, it invites additional hardware costs during implementation. Our proposed work is an entirely different approach compared to [18], [20] designed to address the above issues. In the proposed approach, split array type architecture is considered for implementing the 2^n+1 operation, which occupies less area compared to the MBE scheme. Array architecture is a non-encoded architecture compared to the booth, so it does not require hard multiples for processing the PPs. The problem of an increased number of PPs in an array is addressed in the proposed scheme by splitting array structure into four segments, and full parallelism is maintained in PP additions also. The parallelism in the architecture ensures improved speed by maintaining the area advantage of the general array structure. The handling of signed numbers in array architecture is another reason for which the array scheme is less explored for data processing applications. The representation of signed numbers is addressed in the proposed architecture using appropriate constants.

3 Proposed Work

3.1 Proposed balanced word-length SRM

In balanced word-length modulo multiplication, the number of bits required representing the input, moduli, and output bits are summarized in Table 1. The type mentioned above of multiplication called balanced residue multiplication as it maintains a balanced bit-width between input, output, and moduli representation, as given in Table 1. In literature, the design problem of 2^n-1 and 2^n+1 residue multiplication is achieved through MBE schemes, whereas the possibilities of addressing this problem using array architecture are hardly considered, especially for signed numbers. The hierarchical approach for signed array multiplication presented in [25]. The motivation behind this work is the regularity in VLSI implementation and the reduced area budget offered by the array architectures compared to MBE architecture. The delay problem usually found in array architecture compared to the MBE scheme is addressed here using hierarchy based processing of the input bits and parallel addition structure. For comparative analysis, the adder structure is realized using CSA and Han Carlson parallel prefix [26] based schemes. The mathematical background, algorithm, and architecture of proposed residue 2^n-1, 2^n+1, and 2^n multiplications are presented in the following subsections.

Table 1: Balanced word-length moduli representation

Moduli	2^n-1	2^n	2^n+1
Number of input bits A & B	n		
Moduli representation bits	n	n	n+1
Number of output bits - P	n	n	n+1

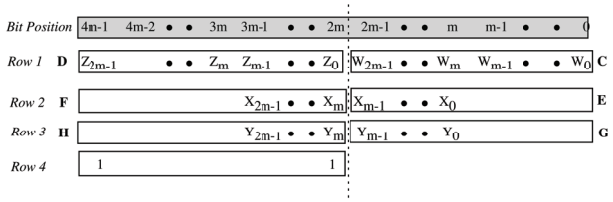

Figure 1: Intermediate PPs arrangement (nxn) [25]

3.1.1 Proposed 2^n-1 SRM

The 2^n-1 modulo multiplication module is one of the essential operations in the RNS independent arithmetic channel. The mathematical background, algorithm,

and the proposed architectures for the signed 2^n-1 residue multiplier are given below.

Mathematical modeling

Consider the 2's complement signed number representation of two binary numbers A and B as given in Eq. (1) & (2)

$$A = -a_{n-1}2^{n-1} + \sum_{i=0}^{n=-2} a_i 2^i \quad (1)$$

$$B = -b_{n-1}2^{n-1} + \sum_{i=0}^{n=-2} b_i 2^i \quad (2)$$

The 2^n-1 residue product representation is given in Eq. (3)

$$P = |A \times B|_{2^n-1} = \left| \left(-a_{n-1}2^{n-1} + \sum_{i=0}^{n-2} a_i 2^i \right) \times \left(-b_{n-1}2^{n-1} + \sum_{i=0}^{n-2} b_i 2^i \right) \right|_{2^n-1} \quad (3)$$

Step 1. Partitioning of Input bits and Generation of intermediate PPs W, X, Y, Z using hierarchical partitioning multiplier [25]

Step 2. PP arrangement:

The generated PPs are arranged [25], and a constant is added, as shown in Fig. 1 where m=n/2.

Step 3. Rearrangement of Intermediate PPs:

Fig. 2 shows the rearrangement of PPs, and the addition process flow carried out for the 2^n-1 residue multiplication, and the corresponding mathematical operations are given in Eq. (4) – (6). The notations and operators used in this mathematical modeling are summarized in Table 2 and Table 3 respectively.

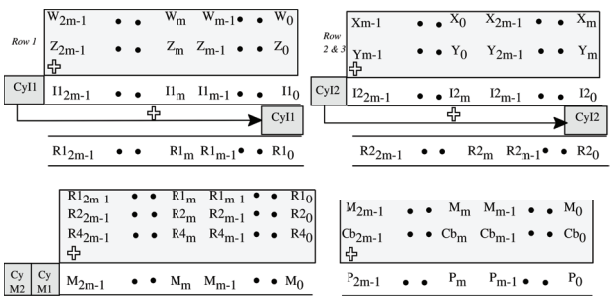

Figure 2: PP Rearrangement and addition process 2^n-1 (nxn)

Table 2: Notations used in mathematical modeling

Notations	Description
A_H, A_L, B_H, and B_L	Higher and Lower bits of A & B inputs.
C_b	Compensation Bits
$M_{i+1} \| M_i$	Overflow bits of M_{i-1} addition process
Cy_{I1}	One bit Carry of I_1 addition process that has to be IEAC (Inverted End around Carry)
Cy_{I2}	One bit Carry of I_2 addition process that has to be IEAC
Cy_{I3}	One bit Carry of I_3 addition process that has to be IEAC
R_{1c}	Carry Bit of R_1 (or) Overflow bit of R_1
R_{2c}	Carry Bit of R_2 (or) Overflow bit of R_2
R_{3c}	Carry Bit of R_3 (or) Overflow bit of R_3
Cy_{Mi}	n/2 Overflow carry bits of Mi addition process. If No overflow occurred n/2 bit zeros is considered
Cy_{Qi}	One bit Carry of Qi addition process that has to be IEAC

Table 3: Operators used in mathematical modeling

Decimal Format: a=12; b=8; n=4 Binary Format: a=1100; b=1000; n=0100			
Operator	**Description/ Functionality**	**Example**	**Result**
$\cdot$	AND	$(a_i \cdot b_i)$	$(1000)_2$
$\|$	OR	$(a_i \| b_i)$	$(1100)_2$
$\overline{a}$	NOT	$\overline{a}$	$(0011)_2$
$\overline{\cdot}$	NAND	$\overline{(a_i \cdot b_i)}$	$(0111)_2$
$\oplus$	EXOR	$(a_i \oplus b_i)$	$(0111)_2$
$\overline{\oplus}$	EXNOR	$\overline{(a_i \oplus b_i)}$	$(1000)_2$
+	Addition	$(a_i + b_i)$	$(20)_{10}$
$\|\|$	Modulus	$\|a \times b\|_{2^n-1}$	$(6)_{10}$
Σ	Summation	$\sum_{i=0}^{3} a_i$	$(12)_{10}$
$\Sigma\,\Sigma$	Double Summation	$\sum_{j=0}^{3}\sum_{i=0}^{3} (a_i \cdot b_i) 2^{i+j}$	$(96)_{10}$
-	Subtraction	$(a - b)$	$(4)_{10}$

a b	Multiplication	a b	$(96)_{10}$
X	Multiplication	$(a \times b)$	$(96)_{10}$
/	Division	$\left(n/2+1\right)$	$(3)_{10}$
$\left\|(\times)^{-1}\right\|_{2^n+1}$	Multiplicative Inverse	$\left\|(a\times b)^{-1}\right\|_{2^n+1}$	$(14)_{10}$
$\|\|$	Concatenation	$(a \,\|\|\, b)$	$(11001000)_2$

$$M_{i-1}=\sum_{i=1}^{n}\left(W_{i-1}+Z_{1i-1}\right)2^{i-1}+\sum_{i=\frac{n}{2}+1}^{n}\left(X_{1i-1}+Y_{1i-1}\right)2^{i-1}$$
$$+\sum_{i=1}^{\frac{n}{2}}\left(X_{1i-1}+Y_{1i-1}\right)2^{i-1}+2^{0}+2^{n-1} \quad (4)$$

The final product is

$$P_{i-1}=\left|A\times B\right|_{2^n-1}=\sum_{i=1}^{n}\left(M_{i-1}+C_{bi-1}\right)2^{i-1} \quad (5)$$

The compensation bits are expressed as

$$C_{bi-1}=\left(\sum_{i=1}^{n}(Sub)2^{i-1}\right)+\left(\sum_{i=1}^{2}\left(Add_{i-1}\right)2^{i-1}\right) \quad (6)$$

Where

$$Ad_0=M_{i+1}\bullet\overline{M_i}\;;\; Ad_1=M_{i+1}\bullet M_i;\; Sub=\overline{M_{i+1}}\bullet\overline{M_i}$$

Algorithm

The proposed 2^n-1 SRM algorithm is given below

1. Input: A & B (A, B → n-bit signed numbers), where *n = 4,8,16,32,etc..*
2. Output $P \leftarrow \left|A\times B\right|_{2^n-1}$, where *P ← n bit*
3. Intermediate PPs Generation →*W,X,Y,Z*
4. Rearrange the Intermediate PPs into 4 rows as in Fig. 1.
5. Split the arrangement in Fig. 1 into two equal halves
   LSP (Least Significant Plane) ← *Bit_Pos(0 to (n-1))*
   MSP (Most Significant Plane) ← *Bit_Pos(n to (2n-1))*
6. Fold the MSP towards LSP side as given in Fig. 2.
7. M ← *Sum (LSP, Folded MSP, EAC)*
8. P ← *Sum (M,C_b)*

Architecture

The architecture of proposed 2^n-1 residue multiplication is shown in Fig. 3. The architecture consists of three stages, namely the partitioning stage, intermediate PPs generation stage, and adder stage. The four parallel modules in the intermediate PP generation stage M-I, M-II, M-III, M-IV indicates the hardware required for computing W, X, Y, Z given in [25]. The four independent parallel addition process observed in the architecture is the main reason for achieving high performance in the proposed array architecture. The compensation bits are gets added in the final stage to obtain modulo results. CSA and Han-Carlson parallel prefix adder structure is incorporated in Fig. 3 in order to analyze the performance. The results of the proposed work are further discussed in Section 5.

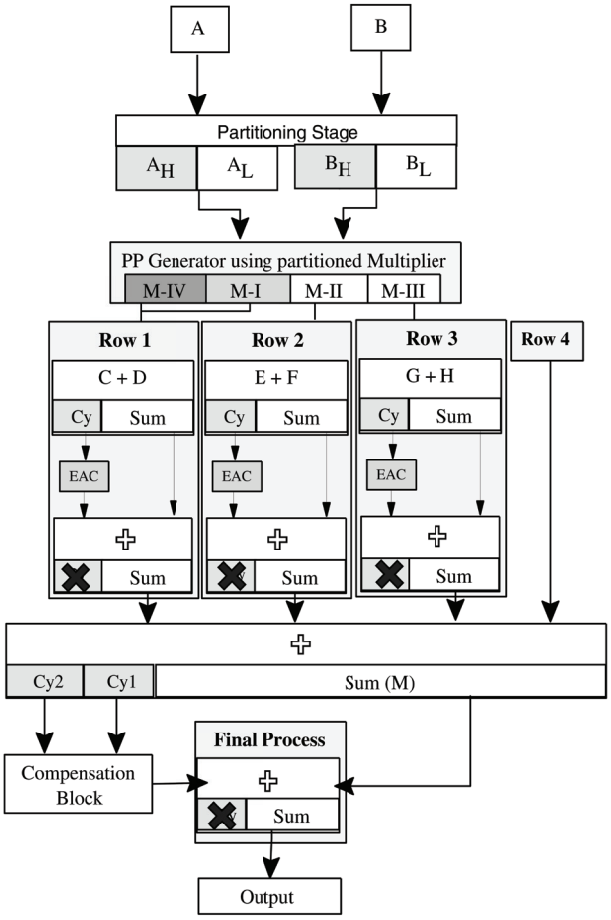

Figure 3: Architecture of 2^n-1 SRM

3.1.2. Proposed 2^n+1 SRM

The 2^n+1 residue multiplication problem is considered as a demanding operation in RNS Processor due to the increase in moduli output range compared to 2^n and 2^n-1 multiplications, as represented in Table 1. In the proposed scheme, the increased moduli output range is regulated using the diminished-1 approach for both multiplier and multiplicand. The primary advantage of using the proposed scheme is that this architecture can handle exceptional cases like 'all-zeros' input and

'all-ones' input, which consecutively produce the correct results. This architecture handles the bit positions higher than n-1 by complementing and mapping them to the LSBs. The mathematical background, algorithm, and the proposed architectures for signed 2^n+1 residue multipliers are given in the below subsections.

Mathematical modeling

The diminished-1 representation of binary inputs A and B are modified as A' & B', which is given in Eq. (7) – (8)

$$A' = \left(-a_{n-1}2^{n-1} + \sum_{i=0}^{n-2} a_i 2^i\right) - 1 \tag{7}$$

$$B' = \left(-b_{n-1}2^{n-1} + \sum_{i=0}^{n-2} b_i 2^i\right) - 1 \tag{8}$$

The residue product P is given by the following Eq.(9)

$$P = \left|A \times B\right|_{2^n+1} = \left|\left(A' \times B'\right) + A' + B' + C_b\right|_{2^n+1} \tag{9}$$

The methodology and arrangements of PP are the same as step 1 and step 2 of signed 2^n-1, but the inputs are A' and B'. The final product is obtained by rearranging the PPs of Fig. 1 in such a way to obtain the result of 2^n+1 residue multiplication. Fig. 4 shows the rearrangement of PPs, the position of PPs, and the addition process flow carried out for the 2^n+1 multiplication, and the same is represented in Eq. (10) – (20). The mathematical operations performed between Row 1 to Row 4 are given below

Row 1:

$$I_{1(i-1)} = \left(\sum_{i=1}^{n}\left(W_{i-1} + \overline{Z_{1i-1}}\right)2^{i-1} + 1\right) \tag{10}$$

$$R_{1(i-1)} = \sum_{i=1}^{n}\left(I_{1(i-1)}\right)2^{i-1} + \left(\overline{Cy_{I1}}\right)2^0 \tag{11}$$

Row 2:

$$I_{2(i-1)} = \sum_{i=\frac{n}{2}+1}^{n}\left(X_{1\left(i-(m+1)\right)}\right)2^{i-1} + \left(\sum_{i=1}^{\frac{n}{2}}\left(\overline{X_{1(m+i-1)}}\right)2^{i-1}\right) + \sum_{i=\frac{n}{2}+1}^{n}(1)2^{i-1} + \left(\sum_{i=1}^{\frac{n}{2}}(0)2^{i-1}\right) + 1 \tag{12}$$

$$R_{2(i-1)} = \sum_{i=1}^{n}\left(I_{2(i-1)}\right)2^{i-1} + \left(\overline{Cy_{I2}}\right)2^0 \tag{13}$$

Row 3:

$$I_{3(i-1)} = \sum_{i=\frac{n}{2}+1}^{n}\left(Y_{1\left(i-(m+1)\right)}\right)2^{i-1} + \left(\sum_{i=1}^{\frac{n}{2}}\left(\overline{Y_{1(m+i-1)}}\right)2^{i-1}\right) + \sum_{i=\frac{n}{2}+1}^{n}(1)2^{i-1} + \left(\sum_{i=1}^{\frac{n}{2}}(0)2^{i-1}\right) + 1 \tag{14}$$

$$R_{3(i-1)} = \sum_{i=1}^{n}\left(I_{3(i-1)}\right)2^{i-1} + \left(\overline{Cy_{I3}}\right)2^0 \tag{15}$$

Row 4:

$$R_{4(i-1)} = (0)2^{n-1} + \sum_{i=1}^{n-1}(1)2^{i-1} \tag{16}$$

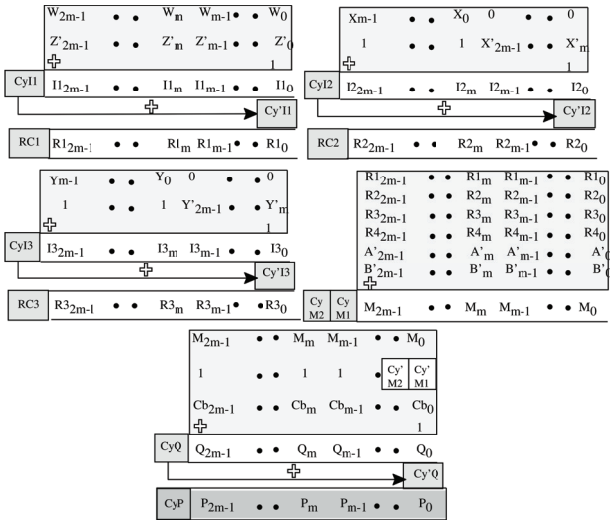

Figure 4: PP Rearrangement and addition process 2^n+1 (nxn)

Finally, all four rows get added as per the following equations.

$$M_{(i-1)} = \sum_{i=1}^{n}\left(R_{1(i-1)} + R_{2(i-1)} + R_{3(i-1)} + R_{4(i-1)} + A_{i-1} + B_{i-1}\right)2^{i-1} \tag{17}$$

$$Q_{i-1} = \left(\sum_{i=1}^{n}\left(M_{i-1} + C_{bi-1}\right)2^{i-1}\right) + \sum_{i=1}^{2}\left(\overline{Cy_{Mi-1}}\right) + \sum_{i=1}^{2}\left(\overline{Cy_{Mi-1}}\right)2^{i-1} + \left(\sum_{i=3}^{n}(1)2^{i-1}\right) + 1 \tag{18}$$

Where C_b is given in Eq. (19)

$$C_{bi-1} = \left(\sum_{i=3}^{n}(1)2^{i-1}\right) + \left(\sum_{i=1}^{2}\left(Ad_{i-1} + \overline{Sub_{i-1}}\right)2^{i-1}\right) + 1$$

$$Ad_0 = A'[n-1] \oplus B'[n-1]$$

$$Ad_1 = A'[n-1] \mid B'[n-1]$$

$$Sub_0 = \left(R_{1c} \oplus R_{2c} \oplus R_{3c}\right)$$

$$Sub_1 = \left(R_{1c} \cdot R_{2c}\right) \mid \left(R_{2c} \cdot R_{3c}\right) \mid \left(R_{3C} \cdot R_{1c}\right) \tag{19}$$

The 2^n+1 multiplication is given in Eq. (20)

$$P_{[n:0]}=\left|A\times B\right|_{2^n+1}=\sum_{i=1}^{n}\left(Q_{(i-1)}\right)2^{i-1}+\overline{Cy_{Qi}} \quad (20)$$

Algorithm
The proposed 2^n+1 SRM algorithm is given below

1. Input: A & B (A, B→ n-bit signed numbers), where *n=4,8,16,32,etc..*
2. Output $P \leftarrow \left|A\times B\right|_{2^n+1}$, where *P ← n+1 bit*
3. A′ ← *Diminished-1 (A);* B′ ← *Diminished-1 (B);*
3. Intermediate PPs Generation →*W,X,Y,Z*
4. Rearrange the Intermediate PPs into 4 rows as shown in Fig. 1.
5. Split the arrangement in Fig. 1 into
   LSP ← *Bit_Pos(0 to (n-1))*
   MSP ← *Bit_Pos (n to (2n-1))*
6. Fold the MSP towards LSP as given in Fig. 4.
7. R_1←*Sum (LSP, 2's Comp. (MSP), IEAC);*
8. R_2←*Sum (LSP, 2's Comp. (MSP), IEAC);*
9. R_3←*Sum (LSP, 2's Comp. (MSP), IEAC);*
10. R_4←*Sum (LSP, 2's Comp. (MSP), IEAC);*
11. M ← *Sum ((Rx,) A′, B′)*, where *x =1,2,3,4*
12. P ← *Sum (M, 2's Complement (Cy_M),C_b, IEAC)*

Architecture
The overall architecture arrangement of 2^n+1 is similar to that of 2^n-1 except for the fact that it has some additional modules to perform 2's complement operation and Inverted End Around Carry (IEAC), as shown in Fig. 5. However, the compensation generation scheme is complicated compared to 2^n-1 architecture.

3.1.3 Signed 2^n residue multiplier

Mathematical modeling
The operation required to obtain Module I (W) follows the same pattern as in 2^n-1. The X & Y are given in Eq. (21) and (22). Z is not required for computing 2^n because it has a higher weight position compared to 2^n value.

$$X=\left(\overline{a_{n-1}\cdot b_0}\right)2^{m-1}+\sum_{i=m}^{n-2}\left(a_i\cdot b_0\right)2^{i-m}+\sum_{j=1}^{m-1}\sum_{i=m}^{n-1-j}\left(a_i\cdot b_j\right)2^{i+j-m} \quad (21)$$

$$Y=\left(\overline{b_{n-1}\cdot a_0}\right)2^{m-1}+\sum_{i=m}^{n-2}\left(b_i\cdot a_0\right)2^{i-m}+\sum_{j=1}^{m-1}\sum_{i=m}^{n-1-j}\left(b_i\cdot a_j\right)2^{i+j-m} \quad (22)$$

The final 2^n product is given in Eq. (23)

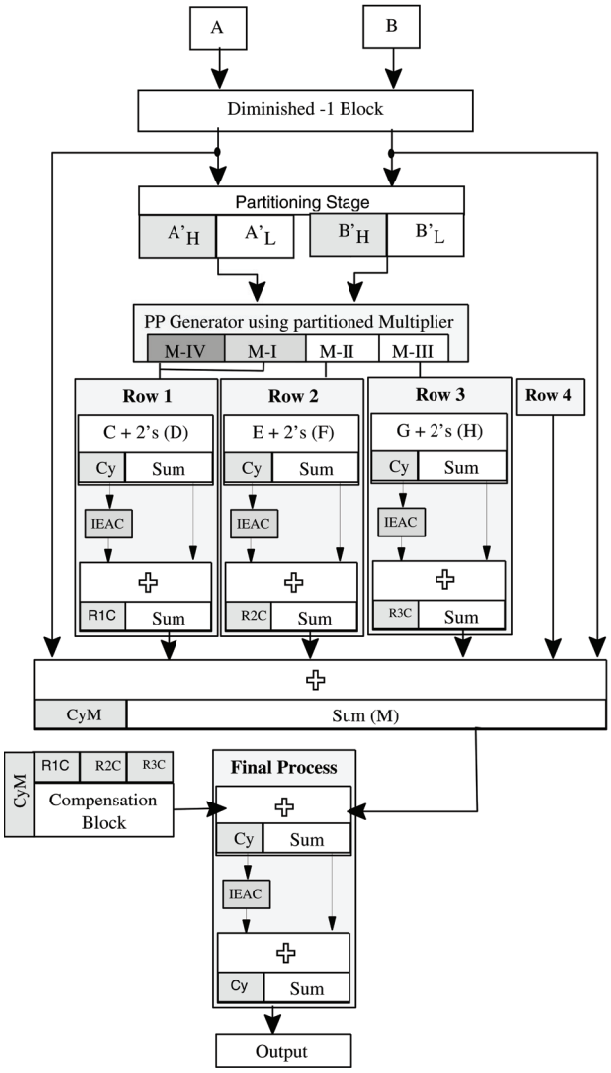

Figure 5: Architecture of 2^n+1 SRM

$$P=\left|A\times B\right|_{2^n}=\sum_{i=0}^{2m-1}W_i 2^i+\sum_{k=m}^{2m-1}\left(X_{k-m}+Y_{k-m}\right)2^k \quad (23)$$

3.2 Proposed unbalanced word-length SRM

The unbalanced word-length moduli multiplier typically used in applications different bit-width proportion between input, moduli, and output is required. In unbalanced word-length residue multiplication, the number of bits required to represent the input, moduli, and output bit-width, which are summarized in Table 4. The strategy followed to design 2^k-1module is derived from the 2^n-1 balanced module. However, the 2^k+1 is not derived from the 2^n+1 balanced module because it may lead to comparatively complex architecture with more delay penalty. Instead, 2^n-1 balanced design is converted to an unbalanced 2^k+1 by modifying the final result of 2^n-1 multiplication.

Table 4: Unbalanced word-length moduli representation

Moduli	2^k-1	2^k	2^k+1
Number of input bits A & B	n		
Moduli representation bits	k	k	k+1
Number of output bits -P	k	k	k+1

3.2.1. Proposed 2^k-1 and 2^k+1 SRM

Mathematical modeling

Let us consider the n bit output of balanced 2^n-1 multiplication given in Eq. (5). It is split into two halves P_L and P_H, as shown in Fig. 6 to obtain the result k=n/2 & k=n/4 bits, and the corresponding equations are given in (24) – (25).

For k=n/2

$$\left.\begin{aligned} P_L &= P\left[\frac{n}{2}\text{-}1:0\right] \\ P_H &= P\left[n\text{-}1:\frac{n}{2}\right] \end{aligned}\right\} 2^n\text{-}1(\text{Output})$$

$$\left.\begin{aligned} UP_{i-1} &= \sum_{i=1}^{\frac{n}{2}}\left(P_{i-1}+P_{\frac{n}{2}+i-1}\right)2^{i-1} \\ P2_{i-1} &= \sum_{i=1}^{\frac{n}{2}}\left(UP_{i-1}\right)2^{i-1}+C_{out}2^0 \end{aligned}\right\} 2^k\text{-}1 \qquad (24)$$

$$\left.\begin{aligned} UP_{i-1} &= \sum_{i=1}^{\frac{n}{2}}\left(P_{i-1}+\overline{P_{\frac{n}{2}+i-1}}\right)2^{i-1}+2^0 \\ P2_{[k:0]} &= \sum_{i=1}^{\frac{n}{2}}\left(UP_{i-1}\right)2^{i-1}+\overline{C_{out}2^0} \end{aligned}\right\} 2^k+1$$

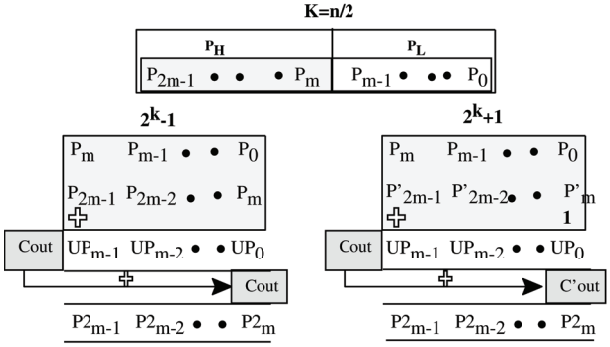

Figure 6: Unbalanced PP Rearrangements and addition process

For k=n/4

k=n/4 design is derived from k=n/2. The output of k=n/2 acts as an input for the k=n/4 design.

$$\left.\begin{aligned} P2_L &= P2\left[\frac{n}{2}\text{-}1:0\right] \\ P2_H &= P2\left[n\text{-}1:\frac{n}{2}\right] \end{aligned}\right\} 2^n\text{-}1(\text{output})$$

$$\left.\begin{aligned} NP_{i-1} &= \sum_{i=1}^{\frac{n}{2}}\left(P2_{i-1}+P2_{\frac{n}{2}+i-1}\right)2^{i-1} \\ P4_{i-1} &= \sum_{i=1}^{\frac{n}{2}}\left(NP_{i-1}\right)2^{i-1}+C_{out}2^0 \end{aligned}\right\} 2^k\text{-}1 \qquad (25)$$

$$\left.\begin{aligned} UP_{i-1} &= \sum_{i=1}^{\frac{n}{2}}\left(P2_{i-1}+\overline{P2_{\frac{n}{2}+i-1}}\right)2^{i-1}+2^0 \\ P4_{[k:0]} &= \sum_{i=1}^{\frac{n}{2}}\left(UP_{i-1}\right)2^{i-1}+\overline{C_{out}2^0} \end{aligned}\right\} 2^k+1$$

Algorithm

The proposed SRM algorithm for the unbalanced 2^k-1 and 2^k+1 is given below

1. Input: A & B (A, B → n bit signed numbers), where *n=4,8,16,32,etc..*
2. Output $P \leftarrow |A\times B|$, where *P ← k bit for- 2^k-1 and k+1 bit for 2^k+1*
3. Consider Eq.(5) - $P \leftarrow |A\times B|_{2^n-1}$,
4. Split the Eq. (5) into two equal halves
   P_H ← *Bit_Pos(0 to (n/2)-1)*
   P_L ← *Bit_Pos((n/2) to n-1)*
5. Fold the P_H towards P_L side as mentioned in Fig. 6.

If (2^k-1) Operation

6. P_2 = Sum(P_L, P_H, EAC) → k=n/2
7. P_4 = Sum(P_{2L}, P_{2H}, EAC) → k=n/4
8. P_8 = Sum(P_{4L}, P_{4H}, EAC) → k=n/8

If (2^k+1) Operation

6. P_2 = Sum(P_L, 2's (P_H), EAC) → k=n/2
7. P_4 = Sum(P_{2L}, 2's (P_{2H}), EAC) → k=n/4
8. P_8 = Sum(P_{4L}, 2's (P_{4H}), EAC) → k=n/8

Architecture

The unbalanced SRM architecture for 2^k-1 and 2^k+1 is depicted in Fig. 7. The architecture is derived from proposed 2^n-1 SRM.

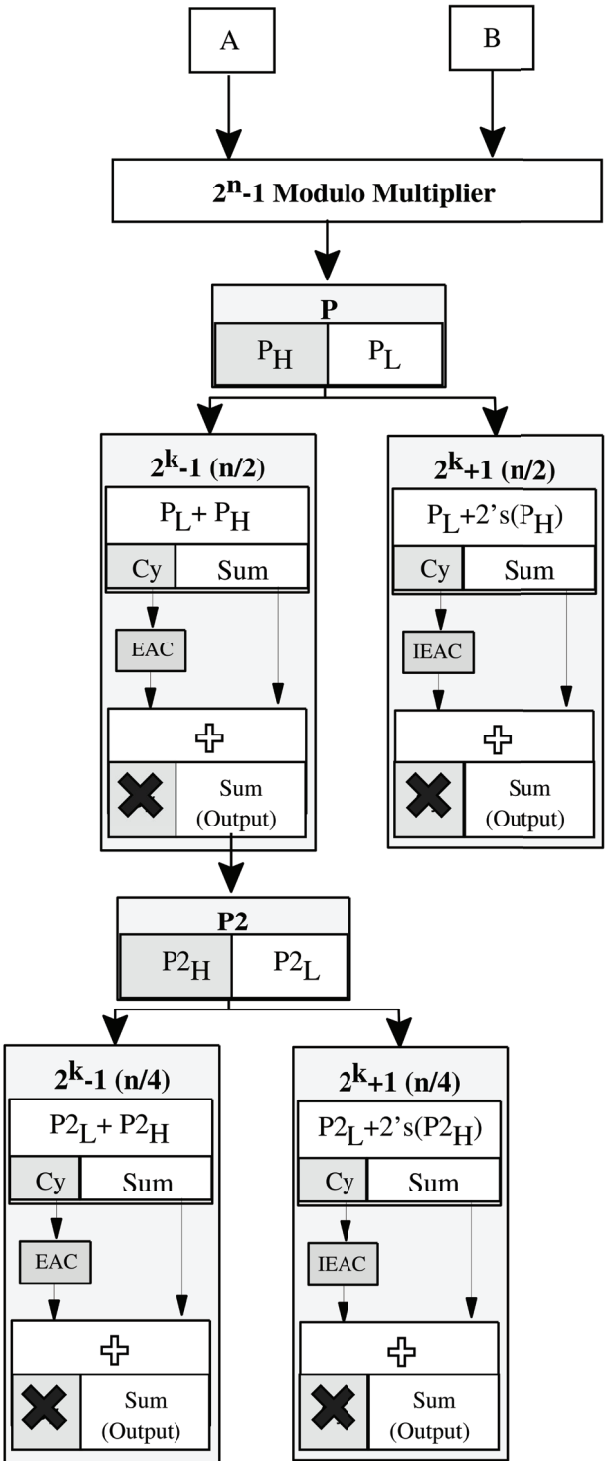

Figure 7: Architecture of 2^k-1 & 2^k+1 SRM

3.2.2. 2^k SRM

The residue multiplication $P = |A \times B|_{2^k}$ is derived from a 2^n balanced residue multiplier equation. The characteristic equations of 2^k unbalanced residue multiplication are given in Eq. (26)

$$P=|A\times B|_{2^k}=\begin{cases} RP_{i-1}=\sum_{i=1}^{\frac{n}{2}}(P_{i-1})2^{i-1} \rightarrow k=\dfrac{n}{2} \\ P4_{i-1}=\sum_{i=1}^{\frac{n}{4}}(P_{i-1})2^{i-1} \rightarrow k=\dfrac{n}{4} \\ P8_{i-1}=\sum_{i=1}^{\frac{n}{8}}(P_{i-1})2^{i-1} \rightarrow k=\dfrac{n}{8} \end{cases} \quad (26)$$

4 RNS processor

4.1 Architecture

In general, the cryptographic algorithm requires many rounds of arithmetic operations in order to create the ciphertext. Instead of doing such lengthy arithmetic operations in binary representation, residue values can be used to save the area and time budget. The proposed balanced and unbalanced word-length residue multipliers are used for implementing special moduli set based RNS computing platforms, as given in Fig. 8. The RNS processing system consists of three blocks, namely Forward Converter (FC), Independent Modulo Arithmetic Processing Unit (IMAPU), and Reverse Converter (RC) [13], [27]. The proposed SRM architectures are used to design arithmetic channels and RC. The FC and RC blocks convert the binary number to residue number and vice versa. The IMAPU block consists of application-based arithmetic operations or any other desired operations in modulo representation. The RC operation can be performed using the Chinese Remainder Theorem (CRT) [28] or Mixed Radix Conversion (MRC) [29]. In this paper, the MRC technique [13,27] is considered for the conversion in the RC block. The characteristic equations of MRC given in Eq. (27) – (29) shows that the operation can be done by modulo subtractions, multiplicative inverses, and residue multiplication. Here the multiplicative inverse is computed using the Extended Euclidean algorithm (EECD) [30]. From [13,27] the decoded number is expressed in the following form for MRC technique

$$X=Z_N m_{N-1} m_{N-2} \cdots\cdots m_1 + \cdots\cdots + Z_3 m_2 m_1 + Z_2 m_1 + Z_1 \quad (27)$$

where $0<Z_i<m_i$

The mixed-radix digits are derived as,

$$\begin{aligned} Z_1 &= x_1 \\ Z_2 &= \left| |m_1^{-1}|_{m_2} \times (x_2 - Z_1) \right|_{m_2} \\ Z_3 &= \left| \left| (m_2 m_1)^{-1} \right|_{m_3} \times (x_3 - Z_2 m_1 + Z_1) \right|_{m_3} \end{aligned} \quad (28)$$

The finalized equation is derived for the value of N bit as,

$$Z_N = \left|\left(m_1 m_2 m_3 \cdots\cdots m_{N-1}\right)^{-1}\right|_{m_N} \times \left|\left(x_N - \left(x_{N-1} m_{N-2} \cdots\cdots Z_2 m_1 + z_1\right)\right)\right|_{m_N} \quad (29)$$

Where m_1,m_2,m_3 are moduli sets, and x_1, x_2, x_3 are residue output of IMAPU.

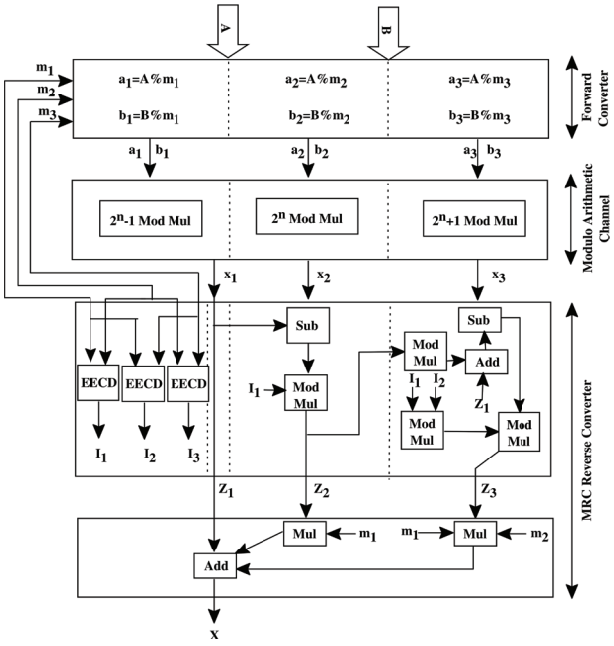

Figure 8: Hardware realization of signed RNS processor

The effectiveness of the proposed multiplier is tested by designing decoupled modulo arithmetic channels and memoryless MRC reverse converter, as shown in Fig. 8. An example calculation depicting the dataflow in the architecture is given in Table 5.

Table 5: RNS processor computation

A=600	B=600	m_1=255	m_2=256	m_3=257
Forward Conversion				
$a_1=\|600\|_{255}=90$	$a_2=\|600\|_{256}=88$			$a_3=\|600\|_{257}=86$
$b_1=\|600\|_{255}=90$	$b_2=\|600\|_{256}=88$			$b_3=\|600\|_{257}=86$
IMAPU				
$x_1=\|90x90\|_{255}= 195$	$x_2=\|88x88\|_{256}=64$			$x_3=\|86x86\|_{257}= 200$
MRC based Reverse Conversion				
$Z_1 = 195$	$Z_2 = \|\|255\|^{-1}_{256}x(64-195)\|_{256}$ $= \|255x-131\|_{256}$ $= 131$			
$Z_3 = \|(\|\|255\|^{-1}x\|256\|^{-1}\|_{257})x(200-(131x255)+195)\|_{257}$ $= \|32768x(200-33600)\|_{257}$ $= 5$	X=(5x255x256)+ ((131x255)+195) =326400+33405+195 X=360000			
X=3,60,000				

4.2 Range analysis

The permissible number ranges for balanced and unbalanced word-length residue multipliers are shown in Table 6. The bit-width required to represent triple moduli set {2^n-1, 2^n, 2^n+1} balanced system is 3n+1bits whereas the maximum number of bits required for unbalanced moduli {2^k+1,2^k, 2^k-1} system is 3k+1.

5 Results and Discussions

5.1 FPGA synthesis

The architecture level functional verification of the proposed design is coded using Verilog HDL and simulated in the Xilinx ISIM tool. The results corresponding to hardware architectures are synthesized in Xilinx Synthesis Technology (XST) for balanced and unbalanced type residue multipliers. The results of the proposed architecture with CSA (Proposed-I) and prefix-based adders (Proposed-II) are presented in Table 7 and Table 8, respectively.

Table 7: FPGA synthesis results of balanced word-length SRM

Multiplier	n	Xilinx Zynq FPGA Board (XC7Z020CLG484-1)			
		Proposed - I		Proposed - II	
		LUT (No's)	Delay (ns)	LUT (No's)	Delay (ns)
2^n	8	37	11.5	37	11.4
	16	186	26.2	203	21.7
	32	928	70.3	1026	45.1
2^n-1	8	112	18.6	144	17.7
	16	530	51.3	697	28.7
	32	2134	155.7	2848	53.0
2^n+1	8	235	29.4	270	27.4
	16	688	85.8	861	44.1
	32	2215	196.7	3705	79.8

Table 6: Range analysis of triple moduli set RNS processor

	Balanced Word-Length Moduli			Unbalanced Word-Length Moduli		
Moduli	2^n-1	2^n	2^n+1	2^k-1	2^k	2^k+1
Number of Input Bits – A & B	n					
Number of Output Bits -P	n	n	n+1	k	k	k+1
Permissible Number Range						
Input Range (Signed Integers)	$\left[-\frac{2^n}{2} \leftrightarrow \frac{2^n}{2}-1\right]$					
Input Range (Unsigned Integers)	[0 ↔ 2n-1]					
Output Range -P	[0 ↔ 2^n-2]	[0 ↔ 2^n-1]	[0 ↔ 2^n]	[0 ↔ 2^k-2]	[0 ↔ 2^k-1]	0 ↔ 2^k]
Dynamic Range of the Moduli	R= {2^{3n}-2^n }			R= {2^{3k}-2^k }		
Permissible Range (Signed Integers)	$R=\left\{-\frac{\left[\left(2^{3n}-2^n\right)\right]}{2} \leftrightarrow \frac{\left[\left(2^{3n}-2^n\right)\right]}{2}-1\right\} \rightarrow \mathrm{Even}(n)$ $R=\left\{-\frac{\left[\left(2^{3n}-2^n\right)-1\right]}{2} \leftrightarrow \frac{\left[\left(2^{3n}-2^n\right)-1\right]}{2}\right\} \rightarrow \mathrm{Odd}(n)$			$R=\left\{-\frac{\left[\left(2^{3k}-2^k\right)\right]}{2} \leftrightarrow \frac{\left[\left(2^{3k}-2^k\right)\right]}{2}-1\right\} \rightarrow \mathrm{Even}(k)$ $R=\left\{-\frac{\left[\left(2^{3k}-2^k\right)-1\right]}{2} \leftrightarrow \frac{\left[\left(2^{3k}-2^k\right)-1\right]}{2}\right\} \rightarrow \mathrm{Odd}(k)$		
Permissible Range (Unsigned Integers)	$R=\left\{0 \leftrightarrow \left(2^{3n}-2^n\right)-1\right\}$			$R=\left\{0 \leftrightarrow \left(2^{3k}-2^k\right)-1\right\}$		

Table 8: FPGA synthesis results of unbalanced word-length SRM

Mul.	n	Zynq FPGA Board (XC7Z020CLG484-1)					
		k=n/2		k=n/4		k=n/8	
		LUT (No's)	Delay (ns)	LUTs (No's)	Delay (ns)	LUT (No's)	Delay (ns)
Proposed -I							
2^k	8	6	8	-	-	-	-
	16	41	15	5	7.9	-	-
	32	250	43	41	13.2	5	7.9
2^k-1	8	120	20	-	-	-	-
	16	645	67	654	68.8	-	-
	32	2577	162	2597	166.5	2605	168
2^k+1	8	121	19	-	-	-	-
	16	649	70	654	78.1	-	-
	32	2587	173	1580	176.0	2599	179
Proposed -II							
2^k	8	5	8	-	-	-	-
	16	44	13	5	7.8	-	-
	32	255	25	44	15.0	5	7.8
2^k-1	8	156	18	-	-	-	-
	16	735	52	753	55.0	-	-
	32	2967	157	3018	61.9	3049	164
2^k+1	8	163	21	-	-	-	-
	16	960	54	980	36.0	-	-
	32	2996	160	3056	162.5	3081	165

**LUT – Look Up Table & LE- Logic Element*

Table 9: ASIC synthesis results of balanced word-length SRM

Mul.	n	Technology											
		180 nm				90 nm				45 nm			
		Area (μm^2)	Power (μW)	Delay (ns)	PDP (pJ)	Area (μm^2)	Power (μW)	Delay (ns)	PDP (pJ)	Area (μm^2)	Power (μW)	Delay (ns)	PDP (pJ)
2^n													
Proposed - I	8	2164	217	1.3	0.3	682	30	0.8	0.02	369	20	0.5	0.0
	16	10438	1677	7.4	12	2967	308	4.2	1.3	1604	200	3.6	0.7
	32	39171	6095	26.8	163	12273	1218	15.2	18.5	6557	739	13	9.4
Proposed - II	8	2044	228	1.2	0.3	652	51	0.8	0.0	357	32	0.8	0.0
	16	11302	1809	6.7	12	3167	407	4.7	1.9	1712	232	4.1	1.0
	32	45784	6316	23.5	148	15787	1264	16.7	21	8435	769	14	10.7
2^n-1													
[22]	8	8668	849	6.8	6	2733	169	4.2	1	1477	108	4.0	0.43
	16	34382	4328	29.1	126	9770	797	16.4	13	5281	513	14.3	7
	32	125346	19176	86.5	1658	39270	3835	48.9	188	20981	2323	41.2	96
[14]	8	8148	781	6.2	5	2569	156	3.8	1	1389	101	3.7	0.37
	16	32663	3983	26.5	105	9282	732	15.0	11	5017	473	13.0	6
	32	119079	17259	78.7	1357	37306	3452	44.5	154	19932	2089	37.5	78
[23]	8	8235	798	6.4	5	2597	158	3.9	1	1404	103	3.8	0.38
	16	32663	4069	27.0	110	9282	748	15.3	11	5017	483	13.3	6
	32	117825	18025	80.4	1449	36913	3607	45.5	164	19722	2185	38.3	84
Proposed - I	8	6518	789	5.1	4	2055	163	3.2	1	1111	124	3.1	0.38
	16	26447	4058	22.2	90	7516	824	12.5	10	4063	537	10.9	6
	32	97926	18282	67.0	1225	30679	3689	37.9	140	16392	2211	31.9	71
Proposed - II	8	6708	809	4.7	4	2081	169	2.8	0	1141	127	2.8	0.35
	16	28937	4147	20.1	83	8120	845	11.3	10	4389	548	9.7	5
	32	114459	18447	58.8	1084	35859	3722	33.7	125	19159	2234	27.5	61
2^n+1													
[21]	8	17659	1058	13.8	15	5588	209	8.6	2	3020	135	8	1
	16	63121	5999	56.5	339	18179	1104	31.6	35	9827	713	27.8	20
	32	254585	30713	170	5221	79827	6145	96	590	41349	3719	81	301
[15]	8	15365	1049	13.6	14	4874	207	8.3	2	2634	135	8	1
	16	59211	5894	54.9	324	16899	1085	31	34	9135	699	27	19
	32	237894	28951	168	4864	73352	5792	95	550	39659	3508	80	281
[16]	8	13961	944	11.1	10	4402	188	6.8	1	2380	122	6.6	1
	16	53425	5216	51.6	269	15182	961	29.1	28	8207	618	25.4	16
	32	210141	25176	159.6	4018	65835	5036	90.3	455	35175	3049	76	232
[17]	8	13251	870	12.2	11	4142	173	7.5	1	2239	112	7.2	1
	16	52376	4658	46.7	218	14871	859	26.4	23	8039	554	23	13
	32	224280	22582	141.1	3186	68951	4518	79.8	361	37280	2736	67.2	184
[18]	8	12565	954	13.3	13	3962	190	8.2	2	2142	122	7.9	1
	16	48617	5306	57	302	13816	977	34	33	7468	629	29	18
	32	187025	26057	155	4039	58593	5211	81	422	31305	3155	78	246
[19]	8	15058	975	14	14	4776	194	9	2	2582	125	8.5	1
	16	52698	5130	55.1	283	15040	945	32	30	8130	610	28	17
	32	166526	23163	154	3567	51347	4633	80	371	27762	2805	74	208
[20]	8	8796	916	12.4	11	2773	182	8.3	2	1499	118	7.4	1
	16	38893	4882	44.6	218	11053	899	26.6	24	5974	581	22.5	13
	32	158971	21889	134.7	2948	49804	4379	64.7	283	26610	2650	60.5	160
Proposed - I	8	8356	908	11.7	11	2635	186	7.9	1	1424	143	7.1	1
	16	33059	4787	41.4	198	9395	972	24.5	24	5078	637	20.2	13
	32	122408	21797	120.2	2620	38349	4439	57.6	256	20489	2670	55.6	148
Proposed - II	8	8831	929	11	10	2825	192	7.2	1	1495	148	6.5	1
	16	36171	4841	37	179	10279	1004	22	22	5556	653	18.1	12
	32	143074	22127	102	2257	44857	4472	50.7	227	23982	2683	49.8	134

5.2 ASIC synthesis

5.2.1 Performance analysis

From Table 9, the area comparison of 2^n-1 SRM shows that the proposed architecture I & II requires less area compared to other multipliers [14][22][23]. The synthesis results show that the proposed design I occupy 17% - 22%, and design II occupies a 10% lesser area than existing modulo MBE. Delay analysis indicates that the proposed-I has a 17% - 24% speed improvement, and Proposed-II excels in speed by 26% - 30%. Power analysis shows that the total power required for the design is almost the same compared to recent works.

In 2^n+1 SRM architectures, the proposed designs outperforms the other multipliers in area efficiency and speed improvement [15,16,17,18,19,20,21]. Proposed architecture I save area in the range of 23% - 44%, whereas the proposed architecture II reduces the area in the range of 10% - 32% compared to existing MBE architectures. The speed improvement of proposed-I and II lies between the ranges of 10% - 35% and 20% – 39%, respectively. The power profiles of the proposed

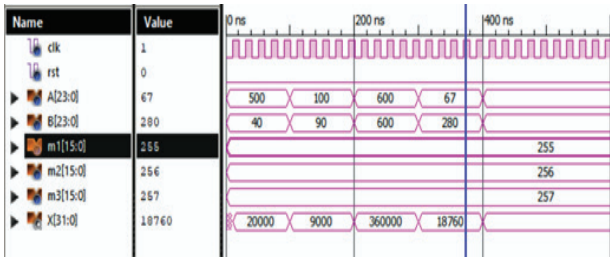

Figure 9: Simulation result of RNS processor

multipliers are almost the same as that of recent works. Since the proposed unbalanced residue multipliers are derived from proposed balanced residue multipliers, they follow the same trend in the area, delay, and power metrics, which are presented in Table 10.

The core problem addressed in this work is the improvement of speed performance of residue signed array multiplier, which generally consumes less area than its booth type counterparts. To achieve this objective, an enormous parallel operation from start to end is envisioned, designed, and implemented. It is inferred

Table 10: ASIC results (90 nm) of unbalanced word-length SRM

Mul.	n	k=n/2				k=n/4				k=n/8			
		Area (μm^2)	Power (μW)	Delay (ns)	PDP (pJ)	Area (μm^2)	Power (μW)	Delay (ns)	PDP (pJ)	Area (μm^2)	Power (μW)	Delay (ns)	PDP (pJ)
2^k													
Proposed - I	8	173	11.4	0.7	0.01	-	-	-	-	-	-	-	-
	16	640	32	2.5	0.08	124.2	5.4	1.6	0.01	-	-	-	-
	32	3224	241	8.0	1.93	739.2	26.4	5.8	0.15	142	13	1.5	0.02
Proposed - II	8	110	3.8	0.7	0.00	-	-	-	-	-	-	-	-
	16	637	45	2.7	0.12	110.7	10.7	1.5	0.02	-	-	-	-
	32	3564	254	8.5	2.16	732.6	36	4.5	0.16	129	20	2.6	0.05
2^k-1													
Proposed - I	8	2172	181	3.6	1	-	-	-	-	-	-	-	-
	16	7757	905	14.1	13	8146	934	15.2	14.2	-	-	-	-
	32	31413	3953	42.15	167	32984	4085	45.2	184.7	33314	4142	47	195
Proposed - II	8	2196	186	3.3	1	-	-	-	-	-	-	-	-
	16	8405	950	12.8	12	8659	986	13.9	13.7	-	-	-	-
	32	36643	3993	36.8	147	37742	4145	39.5	164	38122	4188	41	173
2^k+1													
Proposed - I	8	2212	203	3.7	0.7	-	-	-	-	-	-	-	-
	16	7846	964	14.3	14	8084	996	15.3	15	-	-	-	-
	32	31634	4043	42.6	172	32584	4184	45.5	190	32911	4241	48	204
Proposed - II	8	2240	209	3.6	0.7	-	-	-	-	-	-	-	-
	16	8575	1021	13.4	14	8821	1053	14.4	15	-	-	-	-
	32	36924	4142	38.2	158	38402	4264	40.1	171	39937	4323	45	192

Table 11: FPGA and ASIC synthesis Results of RNS Processor

Parameter	FPGA Synthesis		Parameter	ASIC Synthesis					
				180 nm		90 nm		45 nm	
	Proposed - I	Proposed - II		Proposed - I	Proposed - II	Proposed - I	Proposed - II	Proposed - I	Proposed - II
Number of LUTs	23490	26508	Area (μm^2)	230237	241028	73676	77129	41259	43192
			Power (mW)	36	41	15	18	10	12
Delay (ns)	936	875	Delay (ns)	870	700	440	325	170	145

from the analysis that proposed designs have significant improvement in speed and area performance.

5.2.2 Hardware Implementation of RNS Processor

RNS processing examples discussed in Section 4 and the architecture is shown in Fig. 8 is simulated, and ISIM simulated results are shown in Fig. 9. The synthesis of the RNS Processor is done for both FPGA and ASIC platforms. The results for the same are presented in Table 11. The synthesized netlist of the RNS processor is implemented by targeting to the Xilinx Zynq board (XC7Z020CLG484-1).

6 Conclusion

A new array signed residue multiplication scheme for balanced (2^n-1, 2^n+1, 2^n) and unbalanced (2^k-1, 2^k+1, 2^k) word-length moduli are proposed in this paper. The proposed architecture with enormous parallelism is realized by incorporating CSA and Han-Carlson prefix adder structures into it. The existing and proposed multipliers are synthesized in both ASIC and FPGA technologies. From the synthesis results, the proposed-I 2^n-1 residue multiplication scheme saves 17% area. However, the scheme with prefix structure achieves 26% speed and 24% PDP improvement compared to state of the art MBE 2^n-1 residue multipliers. Similarly, a balanced 2^n+1 proposed-I saves 23% area requirement. Speed and PDP improvement of proposed-II is 20% and 22 %, respectively, compared to the state of the art 2^n+1 residue multipliers. The unbalanced multipliers derived from the balanced multiplier follows the same trend. Finally, the proposed residue arithmetic modules are used in arithmetic channel creation, reverse converter design of {2^n-1, 2^n, 2^n+1} triple moduli set RNS Processor and the same is implemented as hardware using Zynq (XC7Z020CLG484-1) device for real-time verification. The results indicate that the proposed designs can be efficiently utilized to improve the speed and area performances of RNS based cryptographic applications like RSA and ECC. The results also show that the proposed-I SRM architecture implemented using CSA may be used for area constrained RNS applications, and the Proposed-II SRM architecture using prefix can be used for high-speed applications.

7 Conflict of Interest

We have no conflict of interest to declare.

8 References

1. Sousa, L., Antao, S., Martins, P., " Combining Residue Arithmetic to Design Efficient Cryptographic Circuits and Systems," IEEE Circuits Syst. Mag., vol.16, no.4, pp.6-32, 2016. https://doi.org/10.1109/MCAS.2016.2614714
2. Celesti, A., Fazio, M., Villari, M., Puliafito, A., "Adding long-term availability, obfuscation, and encryption to multi-cloud storage systems," J. Netw. Comput. Appl., vol.59, pp. 208–218, 2016. https://doi.org/10.1016/j.jnca.2014.09.021
3. Chang, C.H., Molahosseini, A.S., Zarandi, A.A.E., Tay, T.F., "Residue number systems: A new paradigm to datapath optimization for low-power and high-performance digital signal processing applications," IEEE Circuits Syst. Mag., vol.15, no.5,pp.26–44,2015. https://doi.org/10.1109/MCAS.2015.2484118
4. Molahosseini, A.S., Zarandi, A.A.E., Martins, P., Sousa, L., "A multifunctional unit for designing efficient RNS-based datapaths," IEEE Access, vol.5, pp. 25972–25986,2017. https://doi.org/10.1109/ACCESS.2017.2766841

5. Patronik, P., Piestrak, S.J., "Hardware/Software Approach to Designing Low-Power RNS-Enhanced Arithmetic Units," IEEE Trans. Circuits Syst. I Regul. Pap., vol.64, no.5 , pp.1031–1039 , 2017. https://doi.org/10.1109/TCSI.2017.2669108
6. He, D., Chen, Y. & Chen, J., "An Id-Based Three-Party Authenticated Key Exchange Protocol Using Elliptic Curve Cryptography for Mobile-Commerce Environments," Arabian Journal for Science and Engineering (2013) 38: 2055. https://doi.org/10.1007/s13369-013-0575-4
7. Esmaeildoust, M., Schinianakis, D., Javashi, H., Stouraitis, T., Navi, K., "Efficient RNS implementation of elliptic curve point multiplication over GF(p)," IEEE Trans. Very Large Scale Integr. Syst. vol.21, no.8, pp.1545–1549, 2013. https://doi.org/10.1109/TVLSI.2012.2210916
8. Ding, J., Li, S., "A Modular Multiplier Implemented with Truncated Multiplication," IEEE Trans. Circuits Syst. II Express Briefs. vol.65, no.11, pp.1713–1717,2018. https://doi.org/10.1109/TCSII.2017.2771239
9. Antao, S., Sousa, L., "The CRNS framework and its application to programmable and reconfigurable cryptography," ACM Trans. Archit. Code Optim. , vol.9,no.4,pp.1–25,2013. https://doi.org/10.1145/2400682.2400692
10. Sung-Ming Y., Kim S., Lim S., Moon S., "RSA Speedup with Residue Number System Immune against Hardware Fault Cryptanalysis," In: Kim K. Information Security and Cryptology — ICISC 2001 Lecture Notes in Computer Science, vol 2288. Springer, Berlin, Heidelberg, 2002.
11. Fathy, K.A., Bahig, H.M. & Ragab A.A., "A Fast Parallel Modular Exponentiation Algorithm," Arabian Journal for Science and Engineering vol. 43, 903, 2018. https://doi.org/10.1007/s13369-017- 2797-3
12. Wei Wang, Swamy, M.N.S., Ahmad, M.O., "Moduli selection in RNS for efficient VLSI implementation," In: Proceedings of the 2003 International Symposium on Circuits and Systems, 2003. ISCAS '03. pp. 512-515, IEEE 2003.
13. Omondi, A., Premkumar, B., Residue number systems, Published by Imperial College Press and Distributed By World Scientific Publishing Co. , 2014.
14. Muralidharan, R., Chang, C.H., "Radix-8 booth encoded modulo 2^n-1 multipliers with adaptive delay for high dynamic range residue number system," IEEE Trans. Circuits Syst. I Regul. Pap. vol.58,no.5,pp.982–993,2011. https://doi.org/10.1109/TCSI.2010.2092133
15. Vergos, H.T., Efstathiou, C., "Design of efficient modulo 2^n+1 multipliers," IET Comput. Digit. Tech. vol.1,pp.49-57,2007. https://doi.org/10.1049/iet-cdt:20060026
16. Chen, J.W., Yao, R.H. "Efficient modulo 2^n+1 multipliers for diminished-1 representation," IET Circuits, Devices Syst., vol.4, pp.291-300,2010. https://doi.org/10.1049/iet-cds.2009.0284
17. Chen, J.W., Yao, R.H., Wu, W.J., "Efficient modulo 2^n+1 multipliers," IEEE Trans. Very Large Scale Integr. Syst., vol.19,no.12, pp.2149–2157, 2011. https://doi.org/10.1109/TVLSI.2010.2080330
18. Muralidharan, R., Chang, C.H., "Area-power efficient modulo 2^n-1 and modulo 2^n+1 Multipliers for {2^n-1, 2^n, 2^n+1} Based RNS," IEEE Trans. Circuits Syst. I Regul. Pap., vol.59, no.10,pp.2263–2274 , 2012. https://doi.org/10.1109/TCSI.2012.2185334
19. Efstathiou, C., Moshopoulos, N., Axelos, N., Pekmestzi, K., "Efficient modulo 2^n+1 multiply and multiply-add units based on modified Booth encoding," Integr. VLSI J., vol.47, pp.140–147 ,2014. https://doi.org/10.1016/j.vlsi.2013.04.001
20. Mirhosseini, S.M., Molahosseini, A.S., Hosseinzadeh, M., Sousa, L., Martins, P., "A Reduced-Bias Approach with a Lightweight Hard-Multiple Generator to Design a Radix-8 Modulo 2^n + 1 Multiplier," IEEE Trans. Circuits Syst. II Express Briefs, vol.64, no.7, pp.817–821, 2017. https://doi.org/10.1109/TCSII.2016.2601285
21. Efstathiou, C., Vergos, H.T., Dimitrakopoulos, G., Nikolos, D., "Efficient diminished-1 modulo 2^n+1 multipliers," IEEE Trans. Comput., vol.54, pp.491–496,2005. https://doi.org/10.1109/TC.2005.63
22. Efstathiou, C., Vergos, H.T., Nikolos, D., "Modified booth modulo 2^n - 1 multipliers," IEEE Trans. Comput., vol.53, 370–374,2004. https://doi.org/10.1109/TC.2004.1261842
23. Li, L., Hu, J., Chen, Y., "Modified booth encoding modulo (2^n-1) multipliers," IEICE Electron. Express, vol.9, no.5, pp.352–358, 2012. https://doi.org/10.1587/elex.9.352
24. Alaie, M.A., Timarchi, S., "Efficient modulo 2^n+1 multiplier," Int. J. Comput. Aided Eng. Technol. , vol.8, no.3, pp. 260-276, 2016. https://doi.org/10.1504/ijcaet.2016.077604
25. S Elango , P Sampath, "Implementation of High Performance Hierarchy Based Parallel Signed Multiplier for Cryptosystems, J Circuit Syst. Comp., vol. 29, no. 13, pp. 2050214-1-2050214-25, 2020. https://doi.org/10.1142/S021812662050214X
26. Gupta, T., Sharma, J.B., "Han–Carlson adder based high-speed Vedic multiplier for complex multipli-

cation," Microsyst. Technol., vol.24, pp. 3901–3906, 2018.
https://doi.org/10.1007/s00542-018-3872-8
27. Ananda Mohan, P. V., Residue number systems: Theory and applications, Springer International Publishing, Cham, 2016.
28. Noorimehr, M.R., Hosseinzadeh, M. & Farshidi, R. 'High Speed Residue to Binary Converter for the New Four-Moduli Set $\{2^{2n}, 2^n+1, 2^{n/2}+1, 2^{n/2}-1\}$ Arabian Journal for Science and Engineering, vol.39, 2887,2014.
https://doi.org/10.1007/s13369-014-0963-4
29. Sousa, L., Antão, S.: MRC-based RNS reverse converters for the four-moduli sets $\{2^n-1, 2^n, 2^n+1, 2^{2n+1}-1\}$,"IEEE Trans. Circuits Syst. II Express Briefs,vol.59,no.4,pp.244–248,2012.
https://doi.org/10.1109/TCSII.2012.2188456
30. Sedjelmaci, S.M., "A parallel extended GCD algorithm," J. Discret. Algorithms, vol.6, pp.526 – 538,2008.
https://doi.org/10.1016/j.jda.2006.12.009

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Real-time, Cuff-less and Non-invasive Blood Pressure Monitoring

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Abstract: In in this study ultrasonic method was applied for the measurement of blood pressure (BP). First, a novel method is proposed to measure mean arterial pressure (MAP), diastolic blood pressure (DBP) and systolic blood pressure (SBP) using ultrasonic sensors. The proposed algorithm is implemented by measuring the diameter of the artery and the speed of blood flow based on Doppler physical phenomena so that the BP can be calculated. The results of the proposed algorithm for MAP, SBP, and DBP hypertension analyses were evaluated with the results of Association for the Advancement of Medical Instrumentation (AAMI standard) for all three cases and their mean error rate for the worst case was -0.233mmHg and the standard deviation for 422 samples taken from individuals in the worst case was 4.53 mmHg that meets the standard requirements. Also, according to the British Hypertension Society (BHS) standard, the proposed algorithm for the estimation of BP for all three cases of MAP, DBP, and SBP has Grade A, indicating its higher accuracy in measuring and using the most effective variables in the diagnosis of hypertension in the human body. The proposed algorithm in BP estimation is non-invasive, cuff-less which needs no calibration, and is only based on using the ultrasonic sensor.

Keywords: cuff-less; continues monitoring;blood pressure

Neinvazivno merjenje krvnega tlaka v realnem času brez uporabe manšete

Izvleček: V članku je predstavljena metoda meritve krvnega tlaka z ultrazvočnimi senzorji. Najprej je predstavljena nova metoda merjenja povprečnega (MAP), diastoličnega (DBP) in sistoličnega tlaka(SBP) z uporabo ultrazvočnih senzorjev. Predlagan algoritem temelji na meritvi preseka žile in hitrosti pretoka krvi na osnovi dopplerjevega pojava. Razultati meritev so preverjeni z rezultati meritev po AAMI standardu. Povprečna napaka vseh treh veličin na najslabšem primeru je bila -0.233 mmHg s standardno napako 5.53 mmHg. Glede na britansko združenje BHS se metoda uvršča v razred A meritev krvnega tlaka. Metoda je ne invazivna brez uporabe manšete

Ključne besede: brez manšete; nepretrgane meritve ;krvni tlak

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1 Introduction

Cardiovascular disease (CVD) is one of the main causes of death in the world. According to the European Heart Institute reports, 4.1 million people die from the disease each year [1]. Long-term hypertension is one of the most important risk factors for coronary artery disease, stroke, heart failure, atrial fibrillation, peripheral vascular disease, vision loss, chronic kidney disease and dementia [15-17]. The prevalence of hypertension in 2014 was 1.3 billion worldwide, and it is projected to reach 1.56 billion by 2030 [2, 3].

Blood pressure (BP) is one of the most important parameters of the human body where by its measurement, very useful information can be provided for the physician. Repeated measurements of BP can lead to early diagnosis of the disease, which can be controlled and treated owing to the early diagnosis [4]. By definition, BP is the pressure exerted by blood on the walls of a blood vessel. Its value depends on the functional factors of the cardiovascular system, such as the strength of the cardiac extrusion, the flexibility, and the thickness of the vessel wall [5]. This pressure applied to the vessel wall differs in the two modes of cardiac function and resting phase, which are termed the systolic pressure-maximum pressure (SBP) and the diastolic pressure-minimum pressure (DBP) respectively [6].

According to the National Heart, Lung and Blood Institute (NHLBI), standard systolic and diastolic BP values are 120 and 80 mmHg, respectively. So, BP can be considered in a range which varies proportional to each heartbeat [7]. Another important factor in BP measurement is obtaining the mean blood pressure (MAP) that can be calculated using equation (1).

$$MAP = (2DBP + SBP)/3 \quad (1)$$

In health centers, BP is generally measured with a cuff, which is the most common method for its estimation [8]. Although the measurement of BP using cuff-based methods is meticulously acceptable and reliable, this method is completely dependent on the ability of the one who performs the measurement. Furthermore, cuff-based methods cannot be directly and continuously used because they require several minutes of interruption between each measurement [18]. Hence, the challenges of measurement using the cuff are: BP measurement during movement, the harmfulness of this type of pressure measurement for the patient's cardiovascular system, the inability of the device in continuous measurement, The cuff weight itself, patients' dissatisfaction with the use of cuffs under specific conditions, such as exercise testing and Ambulatory Blood Pressure Monitoring (ABPM) (ABPM) [5, 9, 10]. In the last two decades, there have been extensive studies over non-invasive BP measurement without applying cuff that has led to good results. Amongst these technologies are wearable sensors used by typical people daily, such as smart watches, which provide useful information about vital signs of the body. Many sensors that are used to gather vital body information such as body temperature, heart rate, the amount of oxygen for blood saturation and blood sugar, etc. can be made of flexible and portable materials so that they are easy to use [24 to 29]. This article aims at presenting a novel method for measuring BP in a non-invasive way without using cuff. In order to measure BP without using cuff ,some other methods have been proposed ,in which most of the mathematical relationships and estimation of BP are obtained from one of the measured elements of the body by either using sensors or by imaging the desired vessel as well as extracting their features using image processing techniques [72].

One of the most commonly used non-invasive BP measurements is Pulse Transit Time (PTT) [11]. The pulse transit time is when the heartbeat reaches the desired sensor mounted on the body. In many cases, researchers use electrocardiographic (ECG) signals and sensors (PPGs) to measure BP using this method. PTT measurements can be implemented by one ECG sensor and one PPG sensor or two PPG sensors [12]. The proper reception of the ECG signal requires at least three electrodes at three different points of the body. Patient movement, poor electrode contact with the skin surface and electrode wires for prolonged reception can cause signal noise, which is a limiting factor for measuring BP based on this method [9, 13]. The high cost of using these different devices and sensors, the difficulties associated with installing sensors in different parts of the body and their interconnection with the central control system is a great concern in using this method to measure BP. As has been frequently reported, using PTT due to the dynamic nature of human muscles and hydrostatic changes cannot be a reliable method for measuring BP [20]. A simple and efficient way to directly measure BP using PPG sensors has been reported. In which they used a kind of regression modeling between the amplitude of the signals obtained from PPG sensors to estimate BP [21]. The results of this method were promising for estimating systolic BP, but in the estimation of diastolic pressure did not have a good performance and had significant errors. Furthermore, since regression has no memory, it cannot model the delay between the received PPG signal and the instantaneous BP which in turn, it can create some errors in the measurement [22]. Although this method is perfectly suited for modeling the portable systems, it has complex computations. In addition, the BP and the results of PPG sensors are not constant due to dynamic human muscle changes and hydrostatic vascular changes, so the application of this method may be limited to certain conditions. Particularly, if somebody would like to estimate BP using PPG, considering the fact that this method is based on measuring the amount of oxygen in the blood and when there are disorders such as hypoxia (hypoxia), this method cannot be practically used [23]. In [31] a new method has been reported for extracting BP characteristics from the amplitude and frequency of the signal received from the body based on PTT and Fourier Series Transform (FFT). In all the studies based on the extraction of amplitude and frequency information, after the formation of the characteristic vector and system training steps, using different machine learning algorithms such as regression algorithms, neural network [33] and fuzzy logic [10] The BP estimation is possible. These methods, in which the features are extracted in the form of a signal, are called the parameter-based approach. This method has a lot of complexities and errors, so it is desirable to use more accurate methods to obtain BP. All the above-mentioned methods estimate BP somehow by measuring one of the characteristics of the body's blood transfusion system and generalizing it to different conditions.

It must be mentioned that the Bernoulli method can also be of interest for BP measurement. However, if we want to employ such a method, we need to measure the primary pressure. Therefore, it is not applicable for our purpose.

According to the points mentioned above, in all these methods the amount of BP is measured indirectly by measuring one of the effects of increasing or decreasing BP in different parts of the body. On the contrary to what has been said earlier, the method presented in this paper, for the first time, directly examines the effect of blood changes on the blood vessels to measure BP very accurately. In the proposed method, the ultrasonic sensor is used to measure the transmitted and received waves, and after receiving the information from the ultrasonic sensor, using the Doppler physical phenomenon the vessel diameter and blood velocity are obtained, and then using the presented equations the amount of BP is calculated. Due to the flexibility and elasticity of the blood vessels, as the blood passes through them, the diameter of the vessels and then the volume of blood passing through the artery varies fully depending on the BP [14]. If the blood volume changes are accurately measured, they will have a waveform similar to Figure 1 and their frequency will be the same as the heart's operating frequency [30]. The above signal can be divided into two parts. The upper part of the signal is related to the heart or systole, while the lower part is attributed to the diastole.

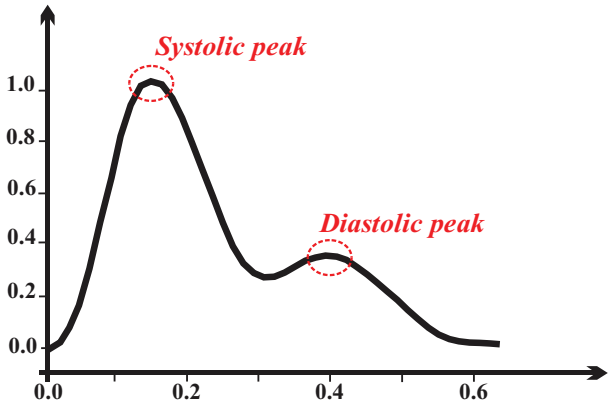

Figure 1: The volume of blood vessels in one cardiac cycle

2 Hypothesis and objectives

The main idea behind the paper was to introduce a continuous-time, cuff-less method for the measurement of the BP. According to the provided expressions in this study, the main parameters such as error, blood density and the diameter of the artery are supposed to have constant values.

3 Materials and methods

How to describe and measure the elastic behavior of the arteries is of a great importance, since from the aspect of basic physiology in the clinical domain, the risk of cardiovascular disease has been more prevailing. In 1960, Patterson is. [34]

$$E_P = \Delta P / (\Delta D / D) \tag{2}$$

In Patterson equation (E_p), P and D represent the pressure and the diameter respectively. The reverse of equation 2 was introduced in 1975 as the "arterial compliance" [2].

$$C = (\Delta D / D) / \Delta P \tag{3}$$

Since then, however, various authors have used the term "distensibility" for such cases which led to a greater association between mechanics and medical science. Accordingly, the authors recommend that this difference in terms all referring to the inverse of the elastic modulus be disregarded Instead, they had better use some terms which are well-defined and appropriately used in various disciplines and replace "elastic modulus" and "compressibility" with "compliance" and "distensibility"[36-38].

In classical physics, the "elasticity" is measured by increasing the force, the amount of deformation of the isotropic sample, and finally, using these values the stress-strain curve is obtained. The amount of deformation of a specimen will depend on the elastic modulus and its geometry (length and cross-section). In engineering designs, the information about the behavioral properties of materials is required, regardless of their geometry. Thus, to eliminate the effect of geometry, the existing data is converted to other parameters. For this purpose, the amount of tensile or applied compressive force and the deformation values are converted to stress and strain respectively. The relationship between stress and strain is linear until the material reaches the Yield strength. E_p represents the slope of this part of

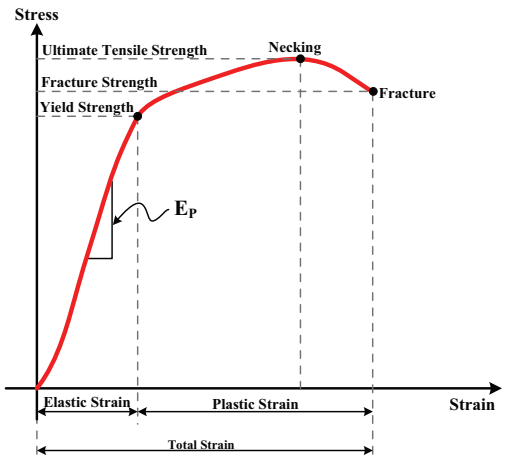

Figure 2: Stress-strain diagram

the curve which is identified by Young's modulus or the modulus of elasticity that can be used to calculate E_p of material by Hook's law as shown in Figure 2.

ΔV_{volume} the change in volume V_{volume} from the isotropic material that is created in response to the pressure change ΔP, the value of $V_{volume} \times \Delta P/\Delta V_{volume}$ is known as the "volume elasticity coefficient" and is usually denoted by the letter K.

In [39-40], in expression was driven for the forward going velocity of the pressure pulse, ΔP, in an infinitely long, thin-walled elastic tube filled with an essentially incompressible fluid and with the elasticity of the tube wall was considered to be isotropic. This has been known as the characteristic pulse wave velocity as shown in the equation below if we consider blood as the expected fluid and the artery equivalent to a very long tube with thin walls;

$$PWVc = \sqrt{K/\rho} \tag{4}$$

In this equation, ρ is the density of blood and K is the elastic modulus of luminal volume change, per unit length of the artery (artery containing refined blood), which is calculated from equation 5.[78]

$$K = V_{Volume} \times \Delta P/\Delta V_{Volume} \tag{5}$$

It may be noted that since $V_{Volume} = 4/3\,\pi R^3$ where R is the luminal radius and, and $dV_{volume} = 4\pi R^2 \times dR$ if we consider ΔV_{volume} to be small enough $dV_{volume}/V_{volume} = \Delta V_{volume}/V_{volume} = 3\times\Delta R/R = 3\times\Delta D/D$ then equation 2 can be written as following.

$$K = \frac{\Delta P}{3\times\Delta D/D} = \frac{\Delta P}{\Delta V_{volume}/V_{volume}} \tag{6}$$

Using Young-Laplace Equation Theory of Young-Laplace Equation and for thin-walled tubes, it can be concluded that the stress of the T-ring on the arterial wall with thickness t and radius R depends on the luminal pressure P and is obtained using the following equation [40].

$$T = P \times R/t \tag{7}$$

If we rewrite this equation based on the pressure, then the Barlow's Formula will be obtained.

$$P = T \times t/R \tag{8}$$

If the pressure P changes with a little value change as ΔP, then the stress will change with the little change value of ΔT using the following equation.

$$\Delta T = \Delta P \times R/t \tag{9}$$

Therefore, E_{inc} can be defined for static incremental Young's modulus for arterial wall type:

$$E_{inc} \equiv stress/strain = \left[\Delta P \times R/t\right] \Big/ \left[\Delta R/R\right] \tag{10}$$

$$E_{inc} = \Delta P \times D^2/2t \times \Delta D = \frac{K \times D}{2 \times t} \tag{11}$$

Since then the relation of pulse wave velocity can be written as follows:

$$PWV = \sqrt{E_{inc} \times t/3 \times R \times \rho} \tag{12}$$

Relation 12 refers to the Moens-Korteweg equation [41-42]. This equation assumes that the arterial wall is isotropic and experiences isometrics changes with the pulse pressure.

A detailed study of the structure of the arterial wall reveals that the three main components of arterial wall elasticity are: collagen, elastin, and smooth muscle, which cause different K values.[43-46] Thus, the value of K for each artery will vary with the pressure and the amount of stress applied [47-49]. As a result, a constant K value cannot be used in the analyses and accordingly in the estimation of BP because the K value is directly related to the individual, the material of vessels and many other factors that are unique to each individual.

Therefore, it is proposed to describe the tensile behavior of the arterial walls, namely the elastic modulus for the volume change per unit length of the lumen and its inverse, that is, the amount of compression.

4 The proposed method

According to the explanations given in the previous sections, and knowing the pulse velocity equation, we can rewrite equation 12 as equation 13.[79-80]

$$V_{Velosity} = \sqrt{\frac{tE}{\rho d}} \tag{13}$$

In this equation , $V_{velocity}$ is the velocity of blood passing through the vessel and t is the thickness of the artery, E

is the Young's module, d is the diameter of the vessel, ρ is the density of blood, and in this regard ,the value of E can be substituted by 14, where E0 is the value of the Young's module at the pressure of zero and it is always about 33.7 to 63.7mmhg and also the coefficient α of the arteries that is always in the range 0.016 to 0.018 mmhg-1.[74-75]

$$E = E_0 e^{\alpha p} \tag{14}$$

Substituting the relation 15 [76-77] into relation 14, will have:

$$V_{Velosity} = \sqrt{\frac{t.E_0.e^{\alpha p}}{\rho.d}} \tag{15}$$

Then, after several steps of simplification and obtaining the parameter p from the relation 15, we will have:

$$P = \frac{1}{\alpha}\ln\left(\frac{\rho d V_{Velocity}^{\ 2}}{tE_0}\right) \tag{16}$$

The relation 16 is presented as the final relation for measuring the BP in which ρ is the density of blood with a value of 1080 kg/m^3 and t is the approximate thickness of the vessels which is 0.46mm.

If we obtain the values of $V_{Velosity}$ for the velocity of blood flow through the artery and also the value of d for the diameter of the arterial vessels, we will be able to find the BP. The description given is shown as below:

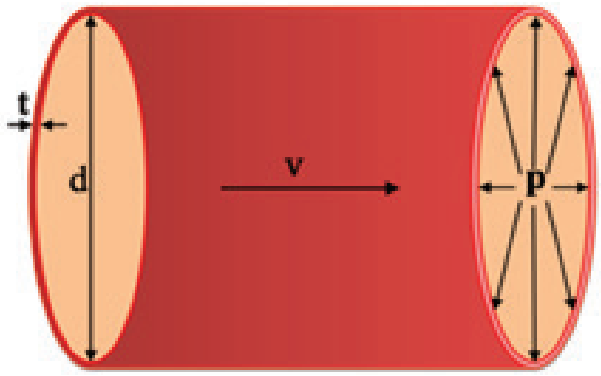

Figure 3: Artery and its related parameters

Therefore, in order to obtain BP, we need to find the diameter of the artery and the velocity of blood flow, but since the method presented in this article is a non-invasive method; both of these quantities should be measured non-invasively.

The best way to measure the blood velocity is using ultrasound and Doppler methods because ultrasonic waves are one of the least dangerous methods for measuring all kinds of vital quantities and the simplest imaging methods in the medical world. The procedure is carried out by sending a wave having a particular frequency to the tissue or the target part of the body and depends on the quantity being measured either by discrete Doppler method or by continuous Doppler method, the measurements are implemented. According to clinical trials, the best frequency to measure blood flow through the artery is 4.63MHz, and the frequency of ultrasonic waves transmitted to measure vessel diameter is 5MHz because of having the highest rate of reflection by blood and arteries walls [73]. In relation 16, the parameters ρ and t are different for different individuals as the blood density and thickness of the vessel will change as the age goes up. Thus, to prove the validity of the presented relationship and also to show that the presented relationship has the least error, these two factors are identified as the causes of error in the measurement results and then the error caused by the effect of these two parameters on the measured pressure value was obtained. If we determine the amount of changes in blood density with Δρ and the changes in artery thickness with Δt, then we will have:

$$P = \frac{1}{\alpha}\ln\left(\frac{\rho dV^2}{tE_0}\right) = \frac{1}{\alpha}\ln\left(\frac{(\rho+\Delta\rho)dV^2}{(t+\Delta t)E_0}\right)$$

$$P = \frac{1}{\alpha}\ln\left(\frac{\rho\left(1+\frac{\Delta\rho}{\rho}\right)dV^2}{t\left(1+\frac{\Delta t}{t}\right)E_0}\right) = \frac{1}{\alpha}\ln\frac{\rho dV^2}{tE_0}\times\frac{1+\frac{\Delta\rho}{\rho}}{1+\frac{\Delta t}{t}} \tag{17}$$

$$P = \frac{1}{\alpha}\left[\ln\frac{\rho dV^2}{tE_0} + \ln\frac{1+\frac{\Delta\rho}{\rho}}{1+\frac{\Delta t}{t}}\right]$$

The second term in the above equation is equal to the error arisen from the density and the thickness so we will have:

$$error = \ln\left(\frac{1+\frac{\Delta\rho}{\rho}}{1+\frac{\Delta t}{t}}\right) = \ln\frac{1+\frac{\Delta\rho}{\rho}+\frac{\Delta t}{t}-\frac{\Delta t}{t}}{1+\frac{\Delta t}{t}} = \ln\left(1+\frac{\frac{\Delta\rho}{\rho}-\frac{\Delta t}{t}}{1+\frac{\Delta\rho}{\rho}}\right) \tag{18}$$

Concerning the Taylor expansion of the logarithmic function, we can write:

$$\ln(1+u) = u - \frac{u^2}{2} + \frac{u^3}{3} - \dots$$

$$error = \frac{\frac{\Delta\rho}{\rho}-\frac{\Delta t}{t}}{1+\frac{\Delta\rho}{\rho}} - \frac{\left(\frac{\frac{\Delta\rho}{\rho}-\frac{\Delta t}{t}}{1+\frac{\Delta t}{t}}\right)^2}{2} + \frac{\left(\frac{\frac{\Delta\rho}{\rho}-\frac{\Delta t}{t}}{1+\frac{\Delta t}{t}}\right)^3}{3} - \dots \tag{19}$$

If Δρ/ρ and Δt/t have the same signs, then the numerators of the fractions are reduced and the error value is reduced. If Δρ/ρ and Δt/t have opposite signs, then we will have the highest amount of error: There are two states for having opposite signs, in the first case when Δρ/ρ is positive and Δt/t is negative, there will be:

$$error = \frac{\frac{\Delta\rho}{\rho} + \frac{\Delta t}{t}}{1 - \frac{\Delta t}{t}} \tag{20}$$

The numerator of the fraction will be positive and the denominator of the fraction will be less than one, and as the subsequent statements are subtracted, the error will be reduced.

In the second case, if Δρ/ρ is negative and Δt/t is positive, we will have:

$$error = \frac{-\frac{\Delta\rho}{\rho} - \frac{\Delta t}{t}}{1 + \frac{\Delta t}{t}} \tag{21}$$

The numerator will be negative and the denominator of the fraction will greater than one, so we will have the highest rate of error.

If Δρ/ρ and Δt/t is considered to be equal, then we will have:

$$error = \frac{2\frac{\Delta t}{t}}{1 - \frac{\Delta t}{t}}$$

$$\frac{x}{1+x} = \left(x - x^2 + x^3 + \ldots\right) = x\left(1 - x + x^2 + \ldots\right) \tag{22}$$

$$error = \frac{-2\frac{\Delta t}{t}}{1 + \frac{\Delta t}{t}} = -2\left[\left(\frac{\Delta t}{t}\right) - \left(\frac{\Delta t}{t}\right)^2 + \left(\frac{\Delta t}{t}\right)^3 + \ldots\right] \cong error = 2\frac{\Delta t}{t}$$

5 The measurement of the blood flow velocity in the artery using Doppler theorem

The Doppler phenomenon was originally proposed for frequency variations of the sound source in classical physics. According to this effect, whenever the receiver of the audio source is moving relative to an audio transmitter, the receiver receives a frequency other than that sent one by the audio source. Taking into account the relativity theorem, there is no difference in the movement of the sound transmitter relative to the sound receiver or the sound receiver toward the sound transmitter. In this case, the received wavelength will be different from the transmitted one. In the Doppler theorem in the above relations, is C the velocity of sound moving in the desired environment, λ is the wavelength, and F is the ultrasonic wave frequency. Now if the generator source moves at the speed of V:

$$f = c/\lambda$$

$$\lambda' = \frac{c \pm v}{f} = \frac{c \pm v}{c/\lambda} = \frac{\lambda\left(c \pm v\right)}{c}$$

$$\lambda' = \frac{c}{f'} = \frac{c \pm v}{f} \tag{23}$$

$$f' = \frac{c}{\left(c \pm v\right)} f$$

$$f' = \frac{v}{\left(v \pm v_s\right)} f$$

In equation 23, F is the frequency of the sent signal towards the moving fluid, V is the velocity of the movement of the waves in the desired environment, VS is the velocity of passing fluid and is the received frequency belonging to the reflected signal from the moving fluid, which can be readily obtained by knowing the velocity of movement in the body and the frequency of the signals being transmitted and received. This is related to the condition that the transmitter and receiver are beside each other without having any angles relative to each other But in construction of two sensor side by side, one has the role of transmitter and the other one the role of the receiver, there will always be an angle with the blood flowing through the artery, and having this angle would give a better and more accurate measurement. Using the following equation, we also include this angle in our analyses to give a more accurate measurement so the relation about the Doppler theorem for measuring blood flow velocity can be rewritten as follows: [69-71]

$$V = \frac{c}{2\cos\theta}\left(\frac{F_2 - F_1}{F_1}\right) \tag{24}$$

In equation 24, V is the velocity of the passing blood, F1 the frequency of the transmitted signal and F2 is the frequency of the received signal, and the difference between these two frequencies is known as Doppler shift. Also, in the equation above, θ is the angle between the ultrasonic signal transmitted and the blood flowing through the artery which will be adjusted once the device is constructed and it will be fixed, and C is the rate of movement of ultrasonic waves in body tissues.

The operation of the above system is shown in Figure 3, where the signal is transmitted from the transmitter sensor to the target vessel and it is reflected in the artery after moving through the blood. Then, the receiver sensor receives the reflected signal, and the Doppler shift can be obtained by detecting the frequency of the received signal. The accuracy of the system is very high because the only vessel near the elbow through which blood passes is the arterial vessel. It should be noted that there are other vessels at the location of measurement, but due to their small diameter or sub-arteries, they will have a smaller Doppler shift compared to the main vessel, and accordingly, to solve this problem, the receiver takes into account the highest difference of the received frequency. So, this problem is resolved automatically and what we have in the output is the velocity of the blood passing through the target artery.

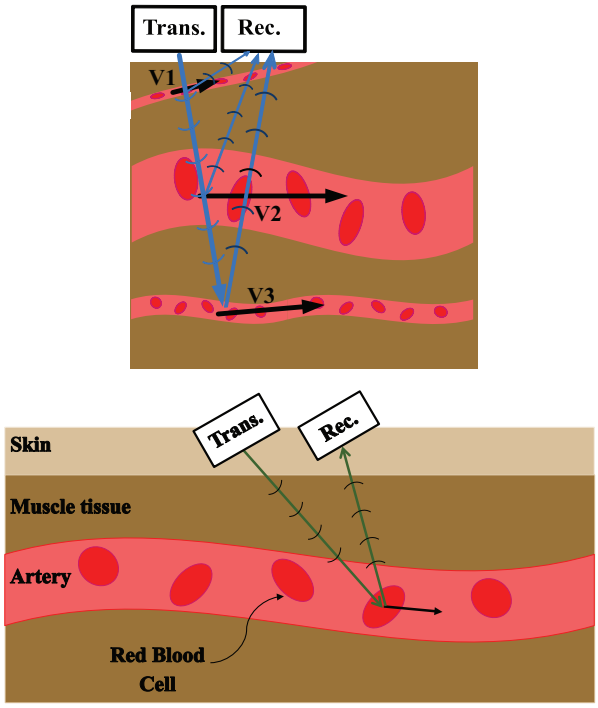

Figure 4: How to apply Doppler theorem to measure the blood velocity in an artery

How to select the desired vessel from the vessels at the site of measurement is based on the selection of the highest frequency difference. Since there are no other vessels near the target vessel, even if the sensor is not positioned in the proper location, it will still be possible to detect the passage of blood correctly because the vessel has the highest rate of passing through it, and the adjacent arteries are much slower than the main artery and have a very little impact on the transmitted frequency. Then, by performing a maximization step, it practically filters out the effect of the other veins and the resulting change in the received frequency is due to the main artery and our target vessel, as shown in Figure 4. The method of measuring blood velocity will be as in the block diagram of Figure 5, in which the block diagram sends a number of ultrasonic sensors acting as a transmitter and transmits a sound having the frequency of 4.63MHz to the target artery. This frequency is generated by the generator signal block. Another ultrasonic sensor that plays the role of the receiver receives the frequency-shifted signal from the blood flow and sends it to the divider block after passing through an amplifier step. At the output of this block, we also have the frequency resulting from the division of the transmitted and the received signals. The output of the subtractor output is sent to the processor where along with the other required components, the desired process is performed and the blood flow rate is extracted.

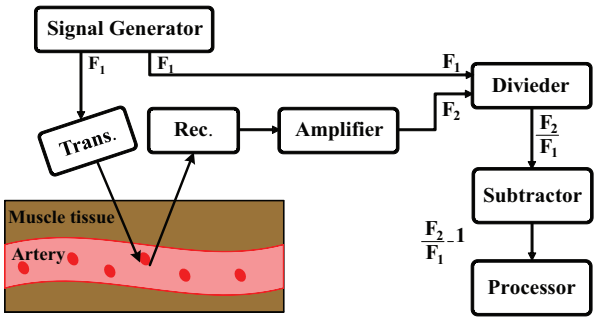

Figure 5: Block diagram of detection of the blood velocity

6 The measurement of vessel diameter using Doppler theorem

As mentioned before, applying the ultrasonic system and the Doppler theorem can be done in two ways of continuous Doppler discrete Doppler. The Doppler transmits the ultrasonic waves continuously and the other sensor receives the reflected signal, and by synthesizing the received signal and extracting its frequency, the desired measurement can be made. This method based upon Doppler theorem is very useful for velocity measurement, and in the medical world, and especially in sonographic devices, this technique is used to find the rate of blood flowing through different parts of the body, as well as to detect vascular congestion and even blood flow in the fetus.

An ultrasonic signal is sent to the desired location to measure the diameter of the artery, and with respect to the reflections made from different interior and exterior walls and so on the depth as well as the distance from the desired part to the sensor and body surface as well as the thickness can be measured and even it is feasible to

obtain a three-dimensional shape of the desired body by considering the differences between the reflections made from different parts. We used this technique in this article to measure the vessel diameter. The procedure is done in this way that using the signal with specific frequency after being transmitted by the transmitter sensor and the reflections made from the vessel walls; the diameter of the vessel can be detected. According to clinical trials, the vessel wall with the frequency of 5 MHz has the highest response and the highest reflection as well. In this case, the time difference between the signals with the highest amplitude (the arteries with thicker wall diameters have more reflection at the desired frequency and reflect the transmitted signal more) will be equal to the sweep time of the signal from the vessel walls and then through which the diameter of the vessel can be calculated. The schematic function of the measurement of the vessel diameter system is shown in Figure 6 and the block diagram of the vessel diameter detection system is shown in Figure 7. Since, however, the material the arterial wall is made of differs from that of the vein, and the frequency chosen to be transmitted toward the artery to measure artery diameter is proportional to the structure and material of the arteries, and most of the reflection is made from the arterial wall, not the vein, so, the selection of the arterial vessels will be done with a high accuracy.

According to Figure 7, the system functions in this way that the signal is transmitted by the transmitter sensor at a frequency of 5 MHz and after colliding with the outer wall of the vessel, some portion of the signal is reflected and the rest continues its way and colliding with the other wall of the vessel, it will be reflected. By having the time difference between the first reflected signal and the second reflected signal and the wave velocity in the body tissues using equation 25, we can obtain the desired artery diameter. Here, d is the diameter of the desired artery, C is the velocity of ultrasonic movement in the body and Δt is the time difference between the two signals reflected from the two vessel walls. The signals reflected through the vessel wall pass through an amplifier block and go into the Level Detector block. In this block, by detecting amplified signal edges, a counter is applied and starts counting at a specified frequency that can be obtained by measuring the amounts counted to obtain the diameter of the vessel.

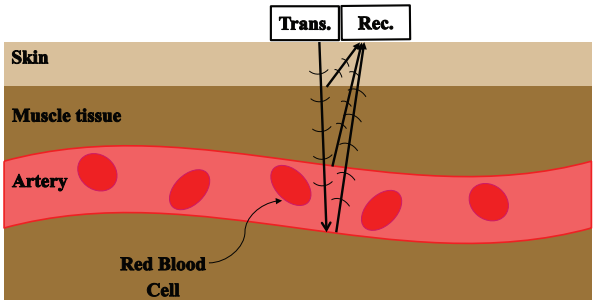

Figure 6: The mechanism of the measurement of artery diameter

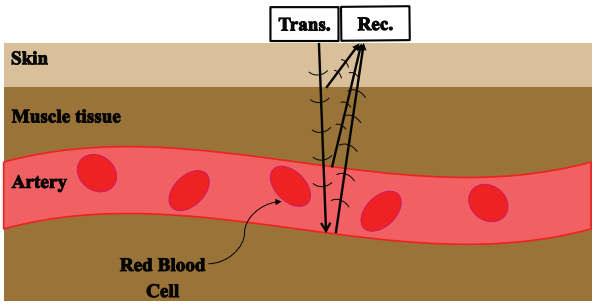

Figure 7: The block Diagram of the Measurement of artery Diameter

$$d = \frac{C.\Delta t}{2} \tag{25}$$

7 The implementation of the total system of blood pressure measurement

The block diagram of the total system for measuring the BP will be in figure 8. In this figure, the solid lines are related to the control path and the continuous lines are belonging to the data path. According to the descriptions above, using the ultrasonic sensors of the receiver the desired signal after being received is amplified and loaded into the Frequency detector and Time Detector

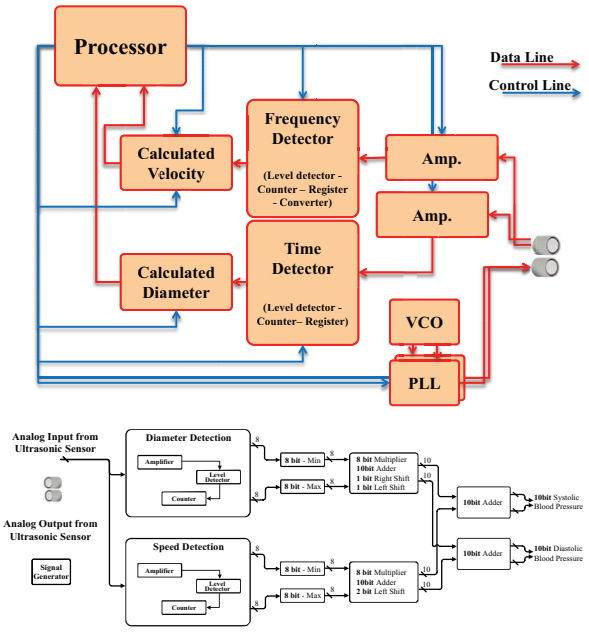

Figure 8: The block Diagram of the total BP measurement system

block and then, from these blocks the velocity and the diameter of the blood artery are extracted. Finally, in the Processor block, the necessary processes are performed according to equation 17 and the BP is obtained.

To demonstrate the correct performance of the proposed equations, we used MATLAB software; we considered the blood velocities in the range of 30-50 cm/s and the vessel diameter 1.6-3.4mm to be variables, assuming that the other parameters in the equation 18 were constant. Also, we considered the value of α as a constant coefficient of the vessel to be 0.017mmHg-1, E0 Young's modulus at zero pressure to have the constant value of 4.5kPa, ρ representing the blood density of1080 kg⁄m^3 and the approximate thickness of the vessels to be 0.46mm. [73] After simulating the above relationship, the ranges of high and low BP changes were obtained as 135mmHg and 73mmHg, respectively. The effect of instantaneous changes in the artery diameter and blood flow velocity that are inversely correlated is clearly shown in Figure 9.

In order to verify the correct operation of the proposed method and its equations, clinical testing was performed at Urmia Shams Cardiology Center (Iran). The test was performed simultaneously on one person in two ways; one using a Finapres BP monitor NOVA (Finapres Medical Systems, Enschede, Netherlands) and the other one using an ultrasonic sensor.

The NOVA device is able to measure the BP at the moment, so it records the person's BP momentarily and simultaneously we can simultaneously obtain the vessel diameter using the ultrasonic sensor and blood

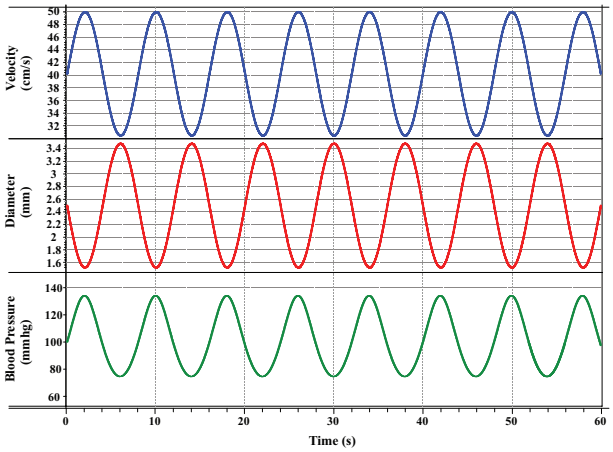

Figure 9: The simulation of BP due to changes in the velocity and diameter of the artery

velocity and later, applying the proposed method we obtained the person's BP. We compared the results of the systolic and diastolic BP measurements and MAP for 60 seconds with the NOVA device and the proposed method, and the curves presented in Figure 10 show the results of these measurements.

The test was performed on the person in two different ways, one when the person was holding his or her breath and the other one when the person was breathing normally. In the curves in Figure 10, the dashed lines (blue) are the results obtained from the NOVA and the solid lines (red) are the results of the instantaneous measurement of BP by the proposed method. By examining the results of the two methods, one can clearly show the accuracy of the measurement using the presented system.

Table 1: The comparison of mean and standard deviation values measured by Sphygmomanometer desktop device using the proposed method

		MEAN(mmHg)	SD(mmHg)	Min (mmHg)	Max(mmHg)
Measure with RDMS device	DBP	65.16	10.31	51.3	112
	SBP	110.47	10.50	90.6	146
	MAP	80.3	10.18	65.1	122.2
Measure by proposed method	DBP	65.04	10.91	47.82	114.40
	SBP	110.24	11.28	90.63	148.49
	MAP	80.11	10.47	63.31	124.50

Table 2: The comparison of the results of the proposed method with the AAMI standard.

		MEAN(mmHg)	SD (mmHg)	Subject
Proposed Method Results	DBP	0.118	4.218	211
	MAP	0.015	3.235	211
	SBP	-0.233	4.538	211
AAMI[58]	BP	≤ 5	≤ 8	85 ≤

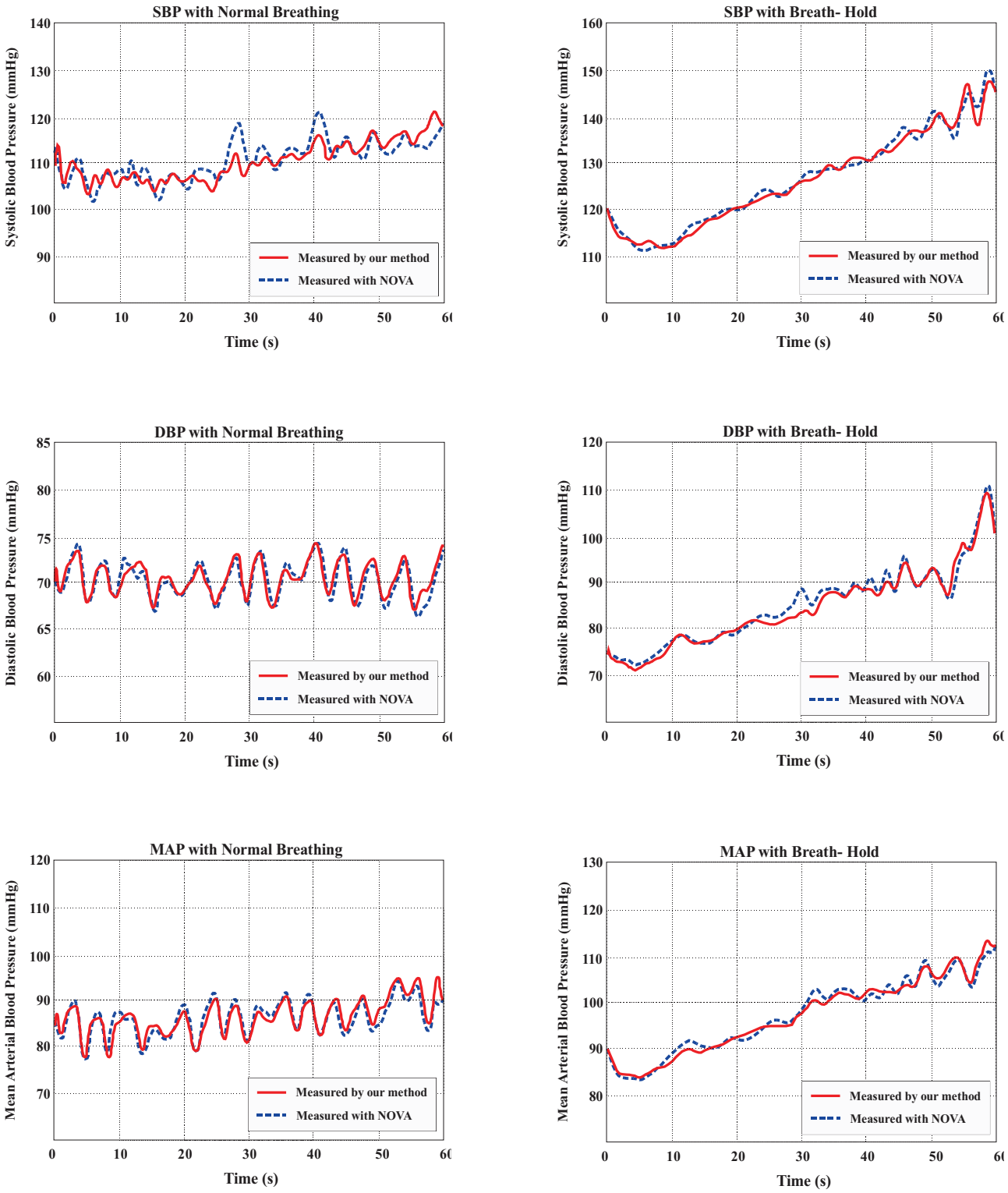

Figure 10: The results of a person's BP test in two different ways

8 Database

The number of patients selected for measuring the BP was measured was 211, from whom 122 were males and 89 were females. For each individual, Sampling was taken twice. Hence the number of samples was 422. This test was performed at various medical and clinical centers, and for all individuals, both systolic and diastolic BPs were measured using the Riester Dip-

Table 3: The comparison of the results of this paper with the BHS standard.

		Cumulative Error Percentage		
		≤ 5 mmHg	≤ 10 mmHg	≤ 15 mmHg
BHS Standard [59]	Grade A	60%	85%	95%
	Grade B	50%	75%	90%
	Grade C	40%	65%	85%
Proposed Method Results	SBP	164(78.09%)	197(93.8%)	207(98.6%)
	DBP	162(77.2%)	202(96.2%)	209(99.5%)
	MAP	191(90.6%)	209(99.5%)	210(100. %)

lomat Mercury Sphygmomanometer (RDMS) desktop monitor and the proposed method. The results of this review are presented in Table 1. The histogram diagram of this test with the desktop device is also shown in Figure 11. To demonstrate the correct performance of the proposed method, these results are compared with two of the most important and accepted standards in this field.

The validity of the proposed method was evaluated in the Association for the Advancement of Medical Instrumentation (AAMI) standard, based on ME (Mean Error) and SD (Standard Deviation). According to this standard, if the proposed method is experimented on at least 255 separate samples, the results will be reliable. This standard also allows a maximum of 3 samples per person, so at least 85 people must take the test. According to this standard, the validity of a method is confirmed when the measured ME is less than 5 mmHg and the SD is less than 8 mmHg. By comparing the values obtained from the measurements using the proposed method and the standard requirements of AAMI, it is revealed that all cases are acceptable and the values of SD and ME are lower than the expected values and the number of people tested is higher than the number of people required by the standard. In addition, the accuracy of the proposed method was also evaluated by the British Hypertension Society (BHS) standard. In this standard three different grades are reported based on the cumulative error percentage. From the samples at least 85 should be examined, which is similar to the AAMI standard. The acceptable error values according to the BHS standard [59] along with a comparison of the results obtained from the method presented under this standard are presented in Table 3. By comparing the results of BHS standard and proposed method in all grades the results have much better conditions than the standard requirements and they are true for all three SBP, DBP, and MAP cases. Therefore, the proposed method meets the requirements of both BHS and AAMI standards. Figure 12 presents the rates of the errors created between the measurements using the RDMS model mercury Sphygmomanometer desktop and the proposed barometer. The graph shows that the error rates in the various measurements of SBP, DBP, and MAP have the highest correlation with the actual pressure value.

It should be noted that the database used in this work contains SBP and DBP pressure data measured by RDMS and Aixplorersonographic probe manufactured by Supersonic Imagine to measure blood velocity and diameter of patients in different wards of Shams hospitals in Urmia city. But the research data in [65] and [67] were collected from healthy people. The results of the proposed method will undoubtedly be improved if healthy people's data are added to the database. Better convergence results can be obtained provided that the number of samples in a database increases. According to the AAMI standard, one person's data can be used up to three times in the database, but in this study we used the data belonging to 211 persons and each person was sampled twice and with increasing it to three times the accuracy of the result can be amended unlike other studies, as in [12] and [66], that used fewer people with more sampling. In many studies, calibration has been used to improve results, but our proposed method does not require any calibration. Table 4 shows a comparison between the proposed method and the other methods. Figure 13 illustrates the measurement of vessel diameter and blood velocity using an ultrasound probe and these results were analyzed using MATLAB software. At the same time, we measured BP using a Sphygmomanometer desktop device. Both methods had similar results for systolic and diastolic BP.

9 Acknowledgments

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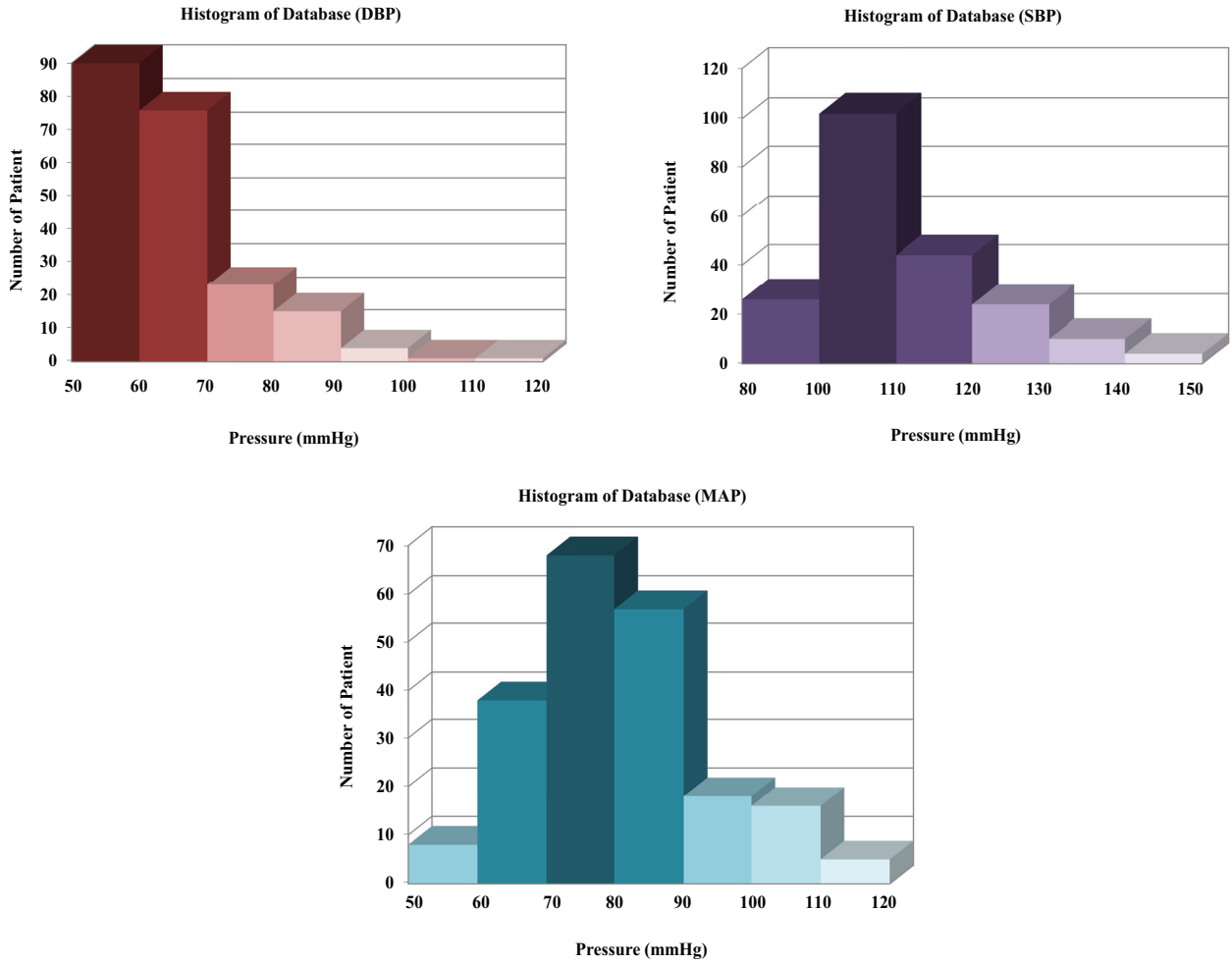

Figure 11: The Histogram diagram for the database presented in this article

Table 4: The comparison between the proposed method and the other methods.

Work	Subject	Record	DBP			SBP			MAP		
			ME	SD	RMSE*	ME	SD	RMSE*	ME	SD	RMSE*
[63]	32	7678	3.67	5.69	-	4.77	7.68	-	3.85	5.87	-
[61]	-	3000	0.03	4.72	-	0.16	6.85	-	-	-	-
[62]	69	69	0.01	4.66	-	0.06	7.08	-	-	-	-
[64]	113	113	7E-15	9.45	-	-1.9E-16	13.81	-	9.3E-7	10.44	-
[14]	-	910	-	-	5.8	-	-	10.9	-	-	-
[65]	10	-	-	-	-	3.8	4.2	-	-	-	-
[12]	19	7000	-	-	-	-	-	-	-	-	-
[33]	-	250	1.92	2.47	-	2.32	2.91	-	-	-	-
[60]	-	15000	-	-	-	-	-	-	-	-	-
[66]	32	7000	-	-	-	-	-	-	-	-	-
[67]	65	78	4.6	4.3	-	5.1	4.3	-	-	-	-
[68]	572	53708	-3.65	8.69	-	-2.98	19.35	-	-3.38	10.35	-
This	211	422	0.118	4.218	4.20	-0.233	4.538	4.53	0.015	3.235	3.22

* Root Mean Square Error.

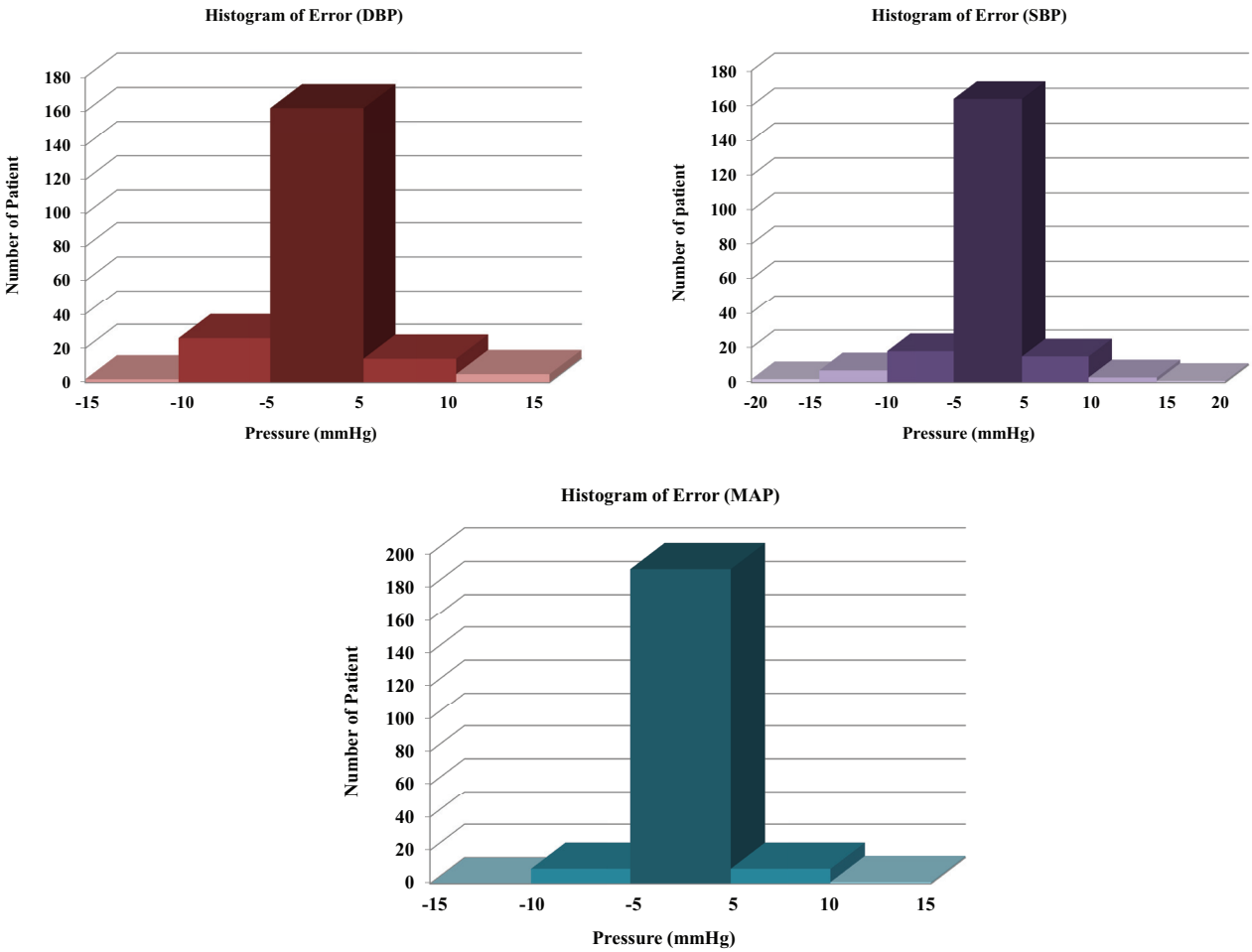

Figure 12: The histogram of the measured error based on the proposed method compared to the RDMS desktop device

10 Conclusions

In this paper, a new method based on the use of ultrasonic signals for BP measurement is presented, which is a non-invasive and continuous method and does not require calibration. In this study, the problems of previous methods such as different PTT-based measurements with PPG and ECG sensors or BP estimation methods that only estimate BP by measuring one quantity of vessels have been resolved. The proposed method was measured by calculating the diameter of the artery and the velocity of the blood passing through using ultrasonic waves, and then we obtained the BP using the presented equations. Finally, the comparative results show that the proposed algorithm is better than previous methods for accurate measurement of BP considering the results obtained for all three parameters of DBP, SBP, and MAP. This method fully meets the requirements for AAMI and BHS standards, which are valid in this field.

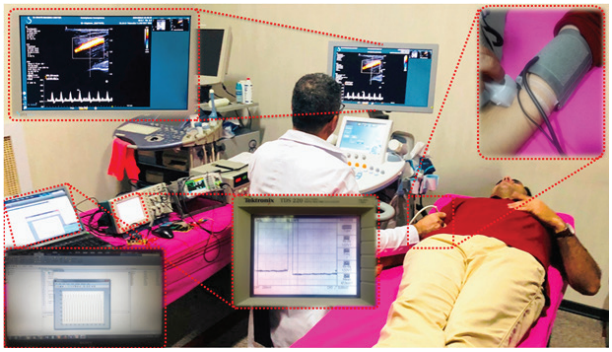

Figure 13: Measurement of vessel diameter and blood velocity instantaneously using Aixplorer ultrasound, the proposed method, and RDMS

11 Conflict of Interest

The authors declare that there is no conflict of interest for this paper. Also, there are no funding supports for this manuscript.

12 References

1. M. Nichols, N. Townsend, P. Scarborough, M. Rayner, Cardiovascular disease inEurope: epidemiological update, Eur. Heart J. 34 (2013) 3028–3034. https://doi.org/10.1093/eurheartj/ehu299
2. W. H. Organization, et al., World Health Statistic 2015, World HealthOrganization, 2015.
3. V. Perkovic, R. Huxley, Y. Wu, D. Prabhakaran, S. MacMahon, The burden ofblood pressure-related disease: a neglected priority for global health,Hypertension 50 (2007) 991–997. https://doi.org/10.1161/HYPERTENSIONAHA.107.095497
4. X.-R. Ding, N. Zhao, G.-Z. Yang, R.I. Pettigrew, B. Lo, F. Miao, et al., Continuousblood pressure measurement from invasive to unobtrusive: celebration of200th birth anniversary of Carl Ludwig, IEEE J. Biomed. Health Inform. 20(2016) 1455–1465. https://doi.org/10.1109/JBHI.2016.2620995)
5. L. Peter, N. Noury, M. Cerny, A review of methods for non-invasive andcontinuous blood pressure monitoring: pulse transit time method ispromising? IRBM 35 (2014) 271–282. https://doi.org/10.1016/j.irbm.2014.07.002
6. P.A. Iaizzo, Handbook of Cardiac Anatomy, Physiology, and Devices, SpringerScience & Business Media, 2009.
7. N.H. Lung, B. Institute, Diseases and Conditions Index: Hypotension, 2008.
8. D. Buxi, J.-M. Redouté, M.R. Yuce, A survey on signals and systems inambulatory blood pressure monitoring using pulse transit time, Physiol.Meas. 36 (2015), p. R1.
9. Y. Zheng, C.C. Poon, B.P. Yan, J.Y. Lau, Pulse arrival time based cuff-less and24-H wearable blood pressure monitoring and its diagnostic value inhypertension, J. Med. Syst. 40 (2016) 195. https://doi.org/10.1007/s1091
10. S. Mottaghi, M. Moradi, L. Roohisefat, Cuffless blood pressure estimationduring exercise stress test, Int. J. Biosci. Biochem. Bioinform. 2 (2012)394.
11. L. Geddes, M. Voelz, C. Babbs, J. Bourland, W. Tacker, Pulse transit time as anindicator of arterial blood pressure, Psychophysiology 18 (1981) 71–74. https://doi.org/10.1111/j.1469-8986.1981.tb01545.x
12. Y. Zhang, Z. Feng, A SVM method for continuous blood pressure estimationfrom a PPG Signal, in: Proceedings of the 9th International Conference onMachine Learning and Computing, 2017, pp. 128–132. https://doi.org/10.1145/3055635.3056634
13. C. Sideris, H. Kalantarian, E. Nemati, M. Sarrafzadeh, Building continuousarterial blood pressure prediction models using recurrent networks, in: 2016IEEE International Conference on Smart Computing (SMARTCOMP), 2016, pp.1–5. https://doi.org/10.1109/SMARTCOMP.2016.7501681
14. M. Liu, P. Lai-Man, H. Fu, Cuffless blood pressure estimation based onphotoplethysmography signal and its second derivative, Int. J. Comput.Theory Eng. 9 (2017) 202. https://doi.org/10.7763/IJCTE.2017.V9.1138
15. Mendis, Shanthi; Puska, Pekka; Norrving, Bo (2011). Global atlas on cardiovascular disease prevention and control (PDF) (1st ed.). Geneva: World Health Organization in collaboration with the World Heart Federation and the World Stroke Organization. p. 38. ISBN 9789241564373. Archived(PDF) from the original on 17 August 2014.
16. Jump up to:a b Hernandorena, I; Duron, E; Vidal, JS; Hanon, O (July 2017). "Treatment options and considerations for hypertensive patients to prevent dementia". Expert Opinion on Pharmacotherapy (Review). 18 (10): 989–1000. https://doi.org/10.1080/14656566.2017.1333599. PMID 28532183.
17. Lau, DH; Nattel, S; Kalman, JM; Sanders, P (August 2017). "Modifiable Risk Factors and Atrial Fibrillation". Circulation (Review). 136 (6): 583–96. https://doi.org/10.1161/CIRCULATIONAHA.116.023163. PMID 28784826.
18. Parati G, Ochoa JE, Lombardi C, Salvi P, Bilo G, "Assessment and interpretation of blood pressure variability in a clinical setting," Blood press, vol. 22, no. 6, pp. 345-354, 2013. https://doi.org/10.3109/08037051.2013.782944
19. Campbell NR, Chockalingam A, Fodor JG, McKay DW, "Accurate, reproducible measurement of blood pressure," CMAJ(Canadian Medical Association Journal), vol. 143, no. 1, pp. 19-24, 1990.
20. R. A. Payne, C. N. Symeonides, D. J. Webb, and S. R. J. Maxwell, "Pulse transit time measured from the ECG: an unreliable marker of beat-to-beat blood pressure," J. Appl. Physiol., vol. 100, no. 1, pp. 136-141, 2006. https://doi.org/10.1152/japplphysiol.00657.2005
21. E.C. Chua, S.J. Redmond, G. McDarby and C. Heneghan, "Towards using photoplethysmogram amplitude to measure blood pressure during sleep," Annals of Biomedical Engineering, vol. 38, no. 3, pp. 945-954, 2010. https://doi.org/10.1007/s10439-009-9882-z
22. X. Xing and M. Sun, "Optical blood pressure estimation with photoplethysmography and FFT-based neural networks," BIOMEDICAL OPTICS EXPRESS, vol. 7, no. 8, pp. 3007-3020, 2016. https://doi.org/10.1364/BOE.7.003007
23. Longmore, Sally K., Gough Y. Lui, Ganesh Naik, Paul P. Breen, Bin Jalaludin, and Gaetano D. Gargiulo. "A comparison of reflective photoplethysmography for detection of heart rate, blood oxy-

gen saturation, and respiration rate at various anatomical locations." Sensors 19, no. 8 (2019): https://doi.org/10.3390/s19081874
24. W. Tao, T. Liu, R. Zheng and H. Feng, "Gait analysis using wearable sensors". Sensors (Basel), vol. 4, pp. 2255–83, 2012. https://doi.org/10.3390/s120202255
25. O. Olguin, P. Gloor, & A. Pentland, "Wearable Sensors for Pervasive Healthcare Management." Principles and applications," Proceedings of the IEEE, vol. 66, pp. 1–4, 2009. https://doi.org/10.4108/ICST.PERVASIVEHEALTH2009.6033
26. G. Appelboom, E. Camacho, M. E. Abraham, S. S. Bruce, E. L. P. Dumont, B. E. Zacharia, R. D'Amico, J. Slomian, J. Y. Redinster, O. Bruyère and E. S. Collony "Smart wearable body sensors for patient self-assessment and monitoring." Arch. Public Health, 72, p. 28, 2014. https://doi.org/10.1186/2049-3258-72-28
27. N. Luo, J. Ding, N. Zhao, B. H. K. Leung & C. C. Y. Poon, "Mobile health: Design of flexible and stretchable electrophysiological sensors for wearable healthcare systems." 11th International Conference on Wearable and Implantable Body Sensor Networks, BSN 2014, pp. 87–91. https://doi.org/10.1109/BSN.2014.25
28. S. Yao, & Y. Zhu, "Wearable multifunctional sensors using printed stretchable conductors made of silver nanowires." Nanoscale, vol. 6, p. 2345, 2014. https://doi.org/10.1039/C3NR05496A
29. D. Vilela, A. Romeo & S. Sánchez, "Flexible sensors for biomedical technology." Lab Chip (2016). https://doi.org/10.1039/C5LC90136G
30. Z. Zhang, Z. Pi, B. Liu, TROIKA: a general framework for heart rate monitoringusing wrist-type photoplethysmographic signals during intensive physicalexercise, IEEE Trans. Biomed. Eng. 62 (2015) 522–531. https://doi.org/10.1109/TBME.2014.2359372
31. S.C. Millasseau, F.G. Guigui, R.P. Kelly, K. Prasad, J.R. Cockcroft, J.M. Ritter,et al., Noninvasive assessment of the digital volume pulse: comparison withthe peripheral pressure pulse, Hypertension 36 (2000) 952–956.
32. M. Kachuee, M.M. Kiani, H. Mohammadzade, M. Shabany, Cuffless bloodpressure estimation algorithms for continuous health-care monitoring, IEEETrans. Biomed. Eng. 64 (2017) 859–869. https://doi.org/10.1109/TBME.2016.2580904
33. P. Li, M. Liu, X. Zhang, X. Hu, B. Pang, Z. Yao, et al., Novel wavelet neuralnetwork algorithm for continuous and noninvasive dynamic estimation ofblood pressure from photoplethysmography, Sci. China Inf. Sci. 59 (2016), p.042405. https://doi.org/10.1007/s11432-015-5400-0
34. Peterson LH, Jensen RE, Parnell J. Mechanical properties of arteries in vivo. Circ Res. 1960;8:622–639. https://doi.org/10.1161/01.RES.8.3.622
35. Gosling RG. Extraction of physiological information from spectra analysed Doppler-shifted continuous wave ultrasound signals. Peter Peregrinus UK IEE Med Electron Monographs. 1976;21:73–125.
36. O'Rourke MF, Staessen JA, Vlachopoulos C, Duprez D, Plante GE. Clinical applications of arterial stiffness: definitions and reference values. Am J Hypertens. 2002; 15:426–444. https://doi.org/10.1016/S0895-7061(01)02319-6
37. Handbook of Chemistry and Physics. 76th ed. Boca Raton, Fla: Chemical Rubber Co; 1995–1996; section 6:137.
38. Chambers Dictionary. London: Chambers Harrap Ltd; 1993:353.
39. Frank O. Die Theorie de Pulswellen. Ztschr Biol. 1926;85:91–130.
40. Bergel DH. The static elastic properties of the arterial wall. J Physiol. 1961;156:445–469. https://doi.org/10.1113/jphysiol.1961.sp006686
41. Moens AI. Die Pulskurve. Leiden, Netherlands. 1878.
42. Korteweg DJ. Uber die Fortpflanzungsgeschwindigkeit des Schalles in Elastiischen Rohren. Ann Phys Chem (NS). 1878:5:52–537. https://doi.org/10.1002/andp.18782411206
43. Clark JM, Glagov S. Transmural organization of the arterial media: the lamellar unit revisited. Arteriosclerosis. 1985;5:19–34. https://doi.org/10.1161/01.ATV.5.1.19
44. Roach MR, Burton AC. The reason for the shape of the distensibility curves of arteries. Can J Biochem Physiol. 1957;35:681–690. https://doi.org/10.1139/o57-080
45. Bank AJ, Wang H, Holte JE, Mullen K, Shammas R, Kubo SH. Contribution of collagen, elastin, and smooth muscle to in vivo human brachial artery wall stress and elastic modulus. Circulation. 1996;94:3263–3270. https://doi.org/10.1161/01.CIR.94.12.3263
46. Farrar DJ, Green HD, Bond MG, Wagner WD, Gobbee RA. Aortic pulse wave velocity, elasticity, and composition in a nonhuman primate model of atherosclerosis. Circ Res. 1978;43:52–62. https://doi.org/10.1161/01.RES.43.1.52
47. Berry CL, Greenwald SE. Effects of hypertension on the static mechanical properties and chemical composition of the rat aorta. Cardiovasc Res. 1976;10:437–451. https://doi.org/10.1093/cvr/10.4.437
48. Bergel DH. Arterial Viscoelasticity in Pulsatile Blood Flow. Attinger EO, ed. London: McGraw-Hill; 1964:279–290.

49. O'Rourke MF, Taylor MG. Input impedance of the systemic circulation. Circ Res. 1967;20:365–380. https://doi.org/10.1161/01.RES.20.4.365
50. Hayashi K, Sato M, Hauda H, Moritake K. Biomechanical study of the constitutive laws of vascular walls. Exp Mech. 1974;14:440–444. https://doi.org/10.1007/BF02324024
51. Hayashi K, Hauda H, Nagasawa S, Okuwura A, Moritake K. Stiffness and elastic behaviour of human intracranial and extracranial arteries. J Biomech. 1980;13:175–184. https://doi.org/10.1016/0021-9290(80)90191-8
52. Kawasaki T, Sasayama S, Yagi S, Asakawa T, Hirai T. Non-invasive assessment of age-related changes in stiffness of major branches of thehuman arteries. Cardiovasc Res. 1987;21:678–687. https://doi.org/10.1093/cvr/21.9.678
53. Lehman ED, Gosling RG, Parker JR, de Silva T, Taylor MG. A blood pressure independent index of aortic distensibility. Br J Radiol. 1993;66: 126–131. https://doi.org/10.1259/0007-1285-66-782-126
54. Lehmann ED, Hopkins KD, Parker JR, Turay RC, Rymer J, Fogelman I, Gosling RG. Aortic distensibility in post-menopausal women receiving Tibolone. Br J Radiol. 1994;67:701–705. https://doi.org/10.1259/0007-1285-67-799-701
55. Lehmann ED, Hopkins KD, Jones RL, Rudd AG, Gosling RG. Aortic distensibility in patients with cerebrovascular disease. Clin Sci (Lond). 1995;89:247–253.
56. Van Bortel LM, Balkestein EJ, van der Heijden-Spek JJ, Vanmolkot FH, Staessen JA, Kragten JA, Vredeveld JW, Safar ME, Struijker BoudierHA, Hoeks AP. Non-invasive assessment of local arterial pulse pressure: comparison of applanation tonometry and echo-tracking. J Hypertens. 2001;19:1037–1044.
57. Laogun AA, Gosling RG. In vivo arterial compliance in man. Clin Phys Physiol Meas. 1982;3:201–212.
58. A. f. t. A. o. M. Instrumentation, American National Standard. Manual,Electronic or Automated Sphygmomanometers, ANSI/AAMI SP10-2002/A1,2003.
59. E. O'brien, B. Waeber, G. Parati, J. Staessen, M.G. Myers, Blood pressuremeasuring devices: recommendations of the European Society ofHypertension, BMJ: Br. Med. J. 322 (2001) 531. https://doi.org/10.1136/bmj.322.7285.531
60. Y. Kurylyak, F. Lamonaca, D. Grimaldi, A neural network-based method forcontinuous blood pressure estimation from a PPG signal, in: 2013 IEEEInternational Instrumentation and Measurement Technology Conference(I2MTC), 2013, pp. 280–283. https://doi.org/10.1109/I2MTC.2013.6555424
61. A. Gaurav, M. Maheedhar, V.N. Tiwari, R. Narayanan, Cuff-less PPG basedcontinuous blood pressure monitoring—A smartphone based approach, in:IEEE 38th Annual International Conference of the Engineering in Medicineand Biology Society (EMBC), 2016, pp. 607–610. https://doi.org/10.1109/EMBC.2016.7590775
62. X. Xing, M. Sun, Optical blood pressure estimation withphotoplethysmography and FFT-based neural networks, Biomed. Opt. Express7 (2016) 3007–3020. https://doi.org/10.1364/BOE.7.003007
63. K. Duan, Z. Qian, M. Atef, G. Wang, A feature exploration methodology forlearning based cuffless blood pressure measurement usingphotoplethysmography, in: IEEE 38th Annual International Conference of theEngineering in Medicine and Biology Society (EMBC), 2016, 2016, pp.6385–6388. https://doi.org/10.1109/EMBC.2016.7592189
64. H. Jiang, F. Miao, M. Gao, X. Hong, Q. He, H. Ma, et al., A novel indicator forcuff-less blood pressure estimation based on photoplethysmography, in:International Conference on Health Information Science, 2016, pp. 119–128. https://doi.org/10.1007/978-3-319-48335-1_13
65. R. Gircys, A. Liutkevicius, A. Vrubliauskas, E. Kazanavicius, Blood pressureestimation accoording to photoplethysmographic signal steepness, Inf. Technol. Control. 44 (2015) 443–450. https://doi.org/https://doi.org/10.5755/j01.itc.44.4.12562
66. A.D. Choudhury, R. Banerjee, A. Sinha, S. Kundu, Estimating blood pressureusing Windkessel model on photoplethysmogram, in: 2014 36th AnnualInternational Conference of the IEEE Engineering in Medicine and BiologySociety (EMBC), 2014, pp. 4567–4570. https://doi.org/10.1109/EMBC.2014.6944640
67. S.C. Gao, P. Wittek, L. Zhao, W.J. Jiang, Data-driven estimation of bloodpressure using photoplethysmographic signals, in: 2016 IEEE 38th Annual-International Conference of the Engineering in Medicine and Biology Society(EMBC), 2016, pp. 766–769. https://doi.org/10.1109/EMBC.2016.7590814
68. J.C. Ruiz-Rodríguez, A. Ruiz-Sanmartín, V. Ribas, J. Caballero, A. García-Roche,J. Riera, et al., Innovative continuous non-invasive cuffless blood pressuremonitoring based on photoplethysmography technology, Intensive Care Med.39 (2013) 1618–1625. https://doi.org/10.1007/s00134-013-2964-2
69. Spicer D.W. and Boyes W. Consumer guide to ultrasonic and correlation flowmeter. Copperhill and Pointer Inc. USA P.9. 2004.)
70. C.Carlander. installation Effect and Self Diagnostics for Ultrasonic Flow Measurement, Doctoral Thesis 2001:11. Department of computer and

electrical engineering, Lulea University of Technology, 2004. ISSN 1402-1544.
71. James W. Bowen, Fundamentals of Ultrasonic Flow Meters, Instromet, Incorporated.
72. Developing a Method of Measuring Blood Pressure Using a Video Recording Julia Jansson julia.jansson@gmail.com under the direction of Prof. Hamed Hamid Muhammed Department of Techology and Health Royal Institute of Technology Research Academy for Young.
73. Seo, Joohyun, Sabino J. Pietrangelo, Hae-Seung Lee, and Charles G. Sodini. "Noninvasive arterial blood pressure waveform monitoring using two-element ultrasound system." IEEE transactions on ultrasonics, ferroelectrics, and frequency control 62, no. 4 (2015): 776-784. https://doi.org/10.1109/TUFFC.2014.006904
74. Kowalewski, Tomasz A. "Blood Flow-Modelling and Diagnostics: Advanced Course and Workshop-BF 2005, Warsaw, June 20-23, 2005." Lecture Notes-ABIOMED (2005).
75. Athanasiou, Kyriacos A., and Roman M. Natoli. "Introduction to continuum biomechanics." Synthesis lectures on biomedical engineering 3, no. 1 (2008): 1-206. https://doi.org/10.2200/S00121ED1V01Y200805BME019
76. McNaught, Alan D. Compendium of chemical terminology. Vol. 1669. Oxford: Blackwell Science, 1997.
77. Truesdell, Clifford, and Leonhard Euler. The Rational Mechanics of Flexible Or Elastic Bodies, 1638-1788: Introduction to LeonhardiEuleri Opera Omnia Vol X Et XI SerieiSecundae. Vol. 11.OrellFüssli, 1960.
78. Manning, Warren J., and Dudley J. Pennell. Cardiovascular Magnetic Resonance: A Com-panion to Braunwald's Heart Disease E-Book. Elsevier Health Sciences, 2018.
79. Wiedeman, Mary Purcell. An introduction to microcirculation. Vol. 2. Elsevier, 2012.
80. Button, Vera. Principles of Measurement and transduction of biomedical variables. Academic Press, 2015.

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CMOS series-shunt single-pole double-throw transmit/ receive switch and low noise amplifier design for internet of things based radio frequency identification devices

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Abstract: The incompatibility between current radio frequency identification (RFID) standards has led to the need for universal and wireless fidelity (Wi-Fi) compatible RFID for internet of things (IoT) applications. Such a universal RFID requires a single pole double throw (SPDT) switch and a low noise amplifier (LNA) to direct and amplify the received raw signal by the antenna. The SPDT suffers from low isolation, high insertion loss and low power handling capacity whereas the LNA suffers from smaller gain, bulky die area, lesser quality (Q) factor, limited tuning flexibility etc. because of passive inductor usage in current generation of devices. In this research, complementary metal oxide semiconductor (CMOS) based inductorless SPDT and LNA designs are proposed. The SPDT adopts a series-shunt topology along with parallel resonant circuits and resistive body floating in order to achieve improved insertion loss and isolation performance whereas the LNA design is implemented with the gyrator concept in which the frequency selective tank circuit is formed with an active inductor accompanied by the buffer circuits. The post-layout simulation results, utilizing 90 nm CMOS process of cadence virtuoso, exhibit that our SPDT design accomplishes 0.83 dB insertion loss, a 45.3 dB isolation, and a 11.3 dBm power-handling capacity whereas the LNA achieves a peak gain of 33 dB, bandwidth of 30 MHz and NF of 6.6 dB at 2.45 GHz center frequency. Both the SPDT and LNA have very compact layout which are 0.003 mm^2 and 127.7 μm^2, respectively. Such SPDT and LNA design will boost the widespread adaptation of Wi-Fi-compatible IoT RFID technology.

Keywords: active inductor; Complementary Metal Oxide Semiconductor (CMOS); internet of things (IoT); low noise amplifier (LNA); Radio frequency identification (RFID); single pole double throw (SPDT) switch

Enopolno menjalno oddajno/sprejemno CMOS uporovno stikalo in nizkošumen ojačevalnik za internet stvari identifikacijske elemente na radijski frekvenci

Izvleček: Nekompatibilnost trenutnih RFID standardov je pripeljala do uporabe Wi-Fi kompatibilnega RFID za internet stvari. Takšen univerzalen RFID zahteva uporabo enopolnega menjalnega stikala (SPDT) in nizkošumnega ojačevalnika (LNA) za usmerjanje in ojačenje sprejetega surovega signala. STPD ima nizko izolativnost, visoke vrinjene izgube in nizko zmogljivost prenosa moči, LNA pa majhno ojačenje, velikost , nižji faktor kvalitete in omejeno zmogljivost nastavljanja. V tem delu sta predlagana SPDT in LNA na osnovi CMOS brez uporabe tuljave. Topologija SPDT uporablja seriske upore v povezavi z vzporednim resonančnim vezje, in plavajočim uporovnim jedrom. LNA uporablja žiratorski koncept, pri katerem je frekvenčno nastavljivo vezje izvedeno z aktivno tuljavo in spremljajočim vezjem. Rezultati kažejo, da SPDT izkazuje 0.83 dB vrinjenih izgub, 45.3 dB izolativnost, in 11.3 dBm energijsko kapaciteto, LNA pa izkazuje ojačenje 33 dB, pasovno širino 30 MHz in NF 6.6 dB pri 2.45 GHz. Oba sta izvedena v kompaktnem dizajnu in omogočata povečano uporabo Wi-Fi kompatibilne RFID tehnologije v internetu stvari.

Ključne besede: aktivna tuljava; CMOS; internet stvari; RFID; enopolno menjalno stikalo

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1 Introduction

The widespread usage of smartphones and smart sensors today has transformed the network into a connected web of smart devices and intelligent services which introduces the concept of IoT. RFID is currently a very reliable wireless communication standard that stores and remotely retrieves the information. RFID has a great potential to be used as IoT devices for many useful applications. The technology comprises of mainly transponders and readers. The transponders store information about its identification along with some additional information which is, generally, transferred to the reader on request. In RFID communication, a reader receives data from transponders wirelessly in High Frequency to microwave frequency band which is decided by the nature of the application. Among all concurrent identification technologies, RFID exhibits many advantages. As a consequence, RFID technology is being deployed for many commercial and home applications since few decades and is anticipated to be available for more advanced applications in near future. The continuous downscaling of CMOS technology made it easy for the radio frequency integrated circuits (RFIC) designers to fabricate fully integrated, low-power and compact RFID [1-2].

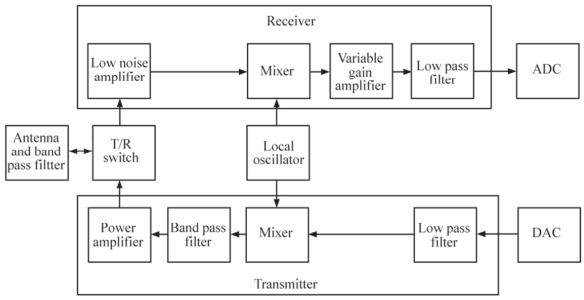

Figure 1: The IoT RFID front end blocks.

In the current generation of RFID communication, the reader is the most exclusive module. Regardless of the versatile opportunities, RFID is yet to overcome the obstruction of reader specific solutions and higher cost for widespread IoT application. In order to abolish the vendor specific unwanted operational cost, a state-of-the-art RFID communication system, by adopting IEEE 802.11b protocol, has been advised in which the wireless network interface cards can be a replacement of the typical RFID reader using future IPV6 concept [2-3]. Therefore, it is expected that a universal RFID communication will be available at very cheap price for widespread IoT application. Fig. 1 illustrates the standard constituents of a transceiver front-end for IoT RFID consisting of a transmitter frontend, a receiver frontend and a common SPDT antenna switch along with a local oscillator for proper information exchange. A power amplifier (PA), band pass and low pass filters, and an up-conversion mixer constitute the transmitter front-end. On the other hand, an LNA, a down conversion mixer, a variable gain amplifier (VGA) and a low pass filter (LPF) build up the receiver frontend. All the modules must be properly matched for the best possible data transmission and reception.

It is obvious that SPDT antenna switch and LNA are the significant modules of every RFID transceiver as it deals with varying low power raw analog signal. An SPDT switch makes it possible for a transceiver to share a common antenna for both transmission and reception process. This design of this switch is quite complicated as it need to handle both high and low power signal. The researchers have tried different combinations of circuit design strategies in order to optimize the CMOS SPDT structure and performance such as: optimized transistor, MOS biasing, stacking transistors, impedance transformation, adjusting substrate impedance [4-10]. However, the trade-off among different performance indicators including isolation, insertion loss, linearity, power handling capacity are application specific and have scope to improve the trade-off for IoT based RFID.

For typical LNA architecture, the frequency selective tank (LC) circuit forms the heart of the LNA. Inductors are always essential components of analogue front-end of typical RF devices for widespread exciting applications [11-16]. Usually, amplifiers and filters, operated in RF regime, utilize on-chip inductors. But inductors in silicon substrates suffer from the parasitic losses which in turn bring down the RF device performance. Additionally, the concerns like die size, lower Q factor, limited tuning flexibility etc. make RFIC designers think alternative to the onchip inductor [17].

In order to conquer the shortcomings, MOS based active inductors are introduced. These active inductors have the privilege of proper tuning in order to compensate the process-voltage-temperature (PVT) variation effects. Moreover, they can offer higher inductance value and better quality factor at only 10% of the die compared to its on-chip equivalent [17]. Consequently, even rapid advancements in integrated circuit technologies cannot keep the passive inductors in the preferred list of RFIC designers.

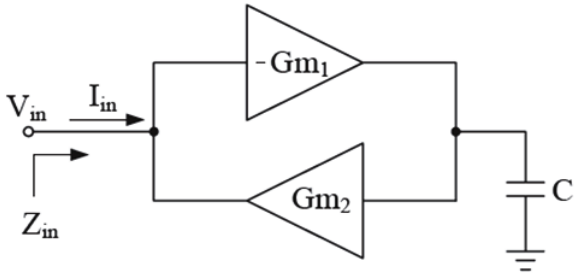

Figure 2: The concept of a typical gyrator.

The concept of the active inductor is a consequence of the gyrator-capacitor model [18-19] as shown in Fig. 2. The gyrator is a two-port circuitry which is composed of a pair of transconductors interconnected in negative feedback in order to reproduce the inductor transfer function. The transconductors designed with NMOSs results in the simple active inductor circuit [19]. Nevertheless, such a composition usually brings some unwanted issues including small inductance, low Q factor, and limited tuning flexibility. In order to compensate these issues, several design ideas have been incorporated as illustrated in the literature [20-27]. Thus, in this proposal, a fully integrated inductorless SPDT and low noise amplifier have been designed and validated by post-layout simulation in 90 nm CMOS technology for 2.4 GHz ISM band IoT based RFID.

2 Design Strategy

2.1 SPDT Design

There are four basic SPDT design topologies which are Series, Series-Shunt, Differential and Asymmetric. Among these, the series-shunt topology is considered the best based on good trade-off between performance and size [5]. Therefore, the proposed series-shunt SPDT, as shown in Fig. 3, consists of transistors (M1, M2) responsible for switching and transistors (M3 and M4) responsible for directing the unwanted leakage signal to the ground. The conduction of these transistors are controlled by the control signals (Vc, Vc´). While the transmitter is active, M1 conducts the signal from the (TX) port to the antenna (ANT) port and M4 drains any leakage approaching the receiver (RX) port to ground in spite of impedance imposed by the combination of non-conducting transistor M2 and active inductor. This improves the isolation of the SPDT with negligibly degraded insertion loss. In addition, the problem of low power handling capacity of the SPDT has been taken care of by utilizing the resistive body floated CMOS structure.

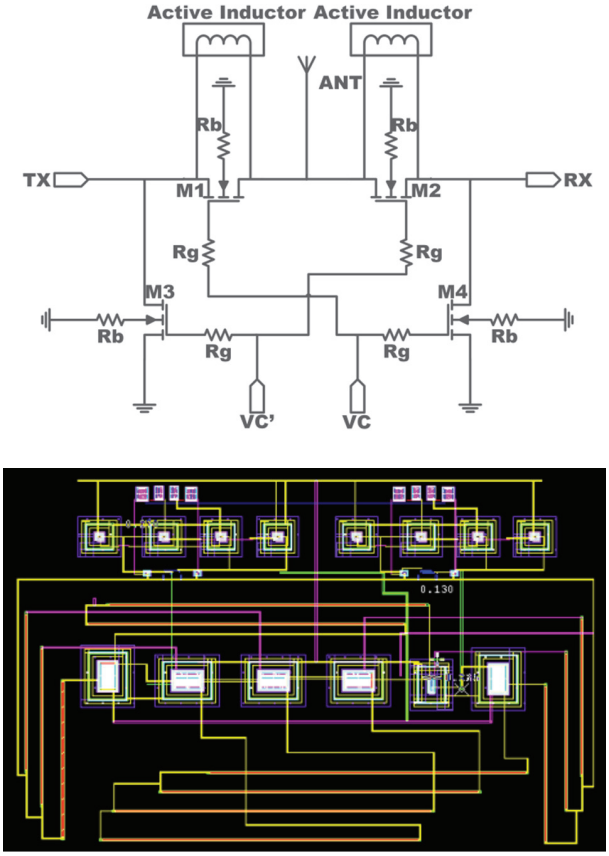

Figure 3: The design concept of SPDT: M1, M2 (100/0.13), M3, M4 (40/0.0.13), Rb, Rg = 10 KΩ. The dimension of the SPDT die is only 0.003 mm^2.

At lower frequency bands, Isolation offered by a typical SPDT is acceptable because of the high impedance of the non-conducting transistors which begins to low down as the signal frequency increases as a result of the leakage through the stray capacitances of the non-conducting transistor. But a selective inductance across this stray capacitance can impose a very high impendence by forming resonant circuit for certain frequency band. This design makes the SPDT offer frequency selective high isolation performance. With the aim of forming such a frequency selective circuit for SPDT, an on-chip inductor was proposed by Feng et al. (2010) [28]. As the lower Q value and larger chip size are the major concerns of on-chip inductors, an optimized active inductor, shown in Fig. 4 [27], has been employed in this SPDT design so that the optimal performance trade-off can be achieved.

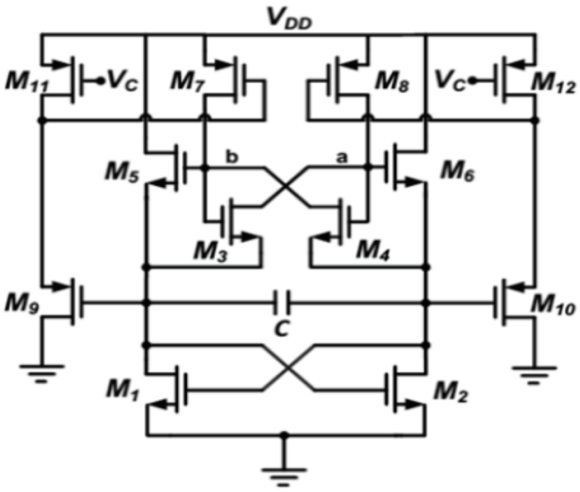

Figure 4: Active inductor for parallel resonant circuit: M1-M6 (0.35/0.13), M7, M8 (20/0.13), M9-M12 (0.35/0.13).

2.2 LNA Design

The proposed schematic of the LNA comprises of three major parts which are: input and output buffer and an active inductor based frequency selective tank circuit. Here, the active inductor utilizes the feature of very low admittance at the resonant-frequency to be used as a frequency selective circuit. Fig. 5 illustrates the schematic of the active inductor circuit used for the proposed LNA. In this active inductor, M_1 and M_2 act as a non-inverting transconductor (g_{M1}) with the input voltage at V_1 and output current at V_3. M_3 is an inverting transconductor ($-g_{M2}$) with the input voltage at V_3 and output current at V_1. Hence, $-g_{M2}$ and g_{M1} form the gyrator which in turn form an inductor at node 1 along with the parasitic capacitor C1 at node 3. This active inductor circuit can be represented as an equivalent RLC circuit as well.

The values of the equivalent inductance, resistance and capacitance are evaluated by:

$$L_{eq} = \frac{C_3}{g_{m1}g_{m2}g_{m3}} \approx \frac{C_3}{0.5g_{m1}g_{m3}} \tag{1}$$

$$r_{loss} = \frac{g_3}{0.5g_{m1}g_{m3}} \tag{2}$$

$$C_p = C_1 \tag{3}$$

$$R_p = \frac{1}{g_1} \tag{4}$$

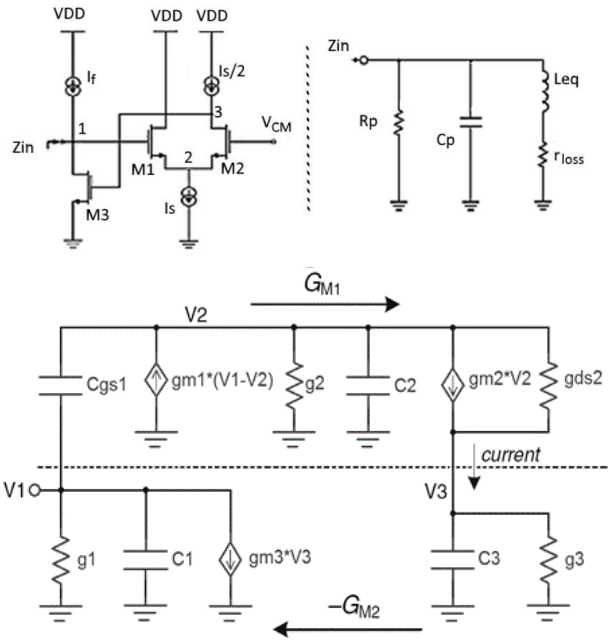

Figure 5: The active inductor and its equivalent circuit proposed for LNA.

The value of the resonant frequency is, therefore:

$$\omega = \sqrt{\frac{0.5g_{m1}g_{m3}}{C_1C_3}} = \frac{1}{\sqrt{L_{eq}C_1}} \tag{5}$$

In the case of passive inductor, the prime noise contribution comes from the internal damping resistance. But in the case of CMOS based emulated active inductor, the main impact is because of the thermal noise modelling in CMOS channel. For the noise analysis of the active inductor, let us consider that it is terminated with a resistance, Rp, the value of which is greater than (1/gm1) and also neglecting the flicker noise of the transistors used, the spot noise figure for Gm cell can be approximately expressed as:

$$NF = 1 + \frac{\gamma}{g_{m2}R_S} + \gamma g_{m1}R_S + \frac{(1+g_{m2}R_S)^2}{g_{m2}{}^2R_SR_P} \tag{6}$$

Where R_S is the source impedance and γ is some constant that depends on the thermal noise behaviour of a given fabrication process. The second term of the NF represents the noise added by M2 and a high ensuring matching conditions can make this term negligible. The third part characterizes the noise hosted by M1 and its transconductance need to be kept small to contribute a lower total

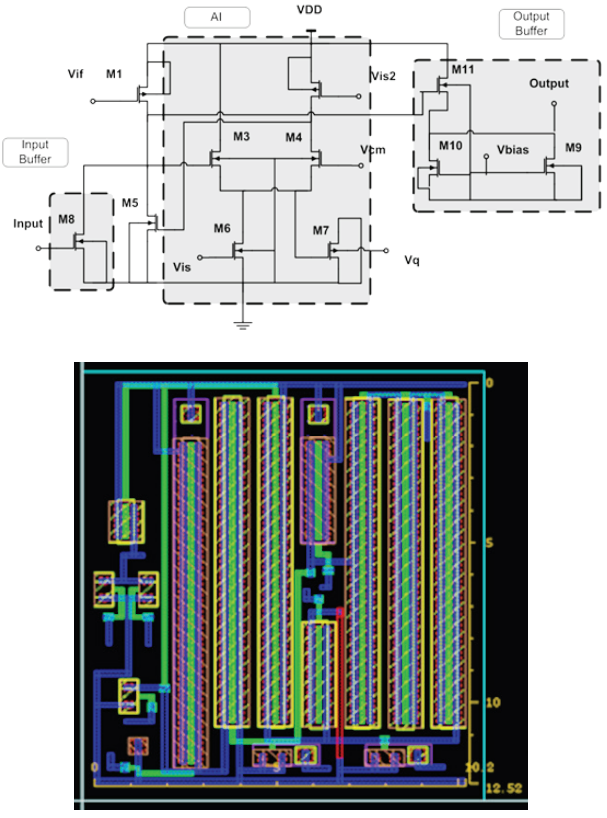

Figure 6: LNA schematic and layout design: M1, M3, M4 (10/0.13), M2 (30/0.13), M5, M6 (3/0.13), M7 - M10 (0.12/0.36), M11 (1/0.36), V_{IF}, $V_{is/2}$, V_{is} = 0.85 V, V_q = 0.7 V, V_{cm} = 0.7 V, VDD = 1.5 V. The die area of the LNA layout is only 127.704 μm².

noise. The fourth term characterizes the noise added by the load. For a high gm2 value, this term becomes nearly identical to R_S/R_P. Hence, increasing the load R_P has the effect of reduced noise contributed by the load.

The architecture of the inductorless nano-CMOS LNA including its biasing and tuning arrangements is shown in Fig. 6. The signal, extracted from the antenna, is fed to the input buffer and is extracted from the output buffer. The active inductor provides all the amplifications and noise minimization at 2.4 GHz band. In this LNA, the voltage biasing V_{IP}, $V_{is/2}$, V_{is}, V_q, V_{cm} contribute to the tuning of centre frequency, noise figure and frequency response. From the small signal equivalent circuit of the LNA, it is obvious that the maximization of the transconductances of M2, M3 and M4 improves the noise performance. But this corresponds to the increase in the parasitic capacitances which lower down the bandwidth and gain. Moreover, the transconductances of M5 and M6 have very small effect on performance as those serve as current followers. So, in order to set the best possible tradeoff, these transconductances have been tuned by trial and error basis.

3 Results and Discussions

The inductorless SPDT and LNA are designed and simulated by 90 nm CMOS process in Analog Design Environment (ADE) of cadence virtuoso. In this study, the performance of the SPDT and LNA is assessed by the post-layout simulation results at standard temperature of 300° K.

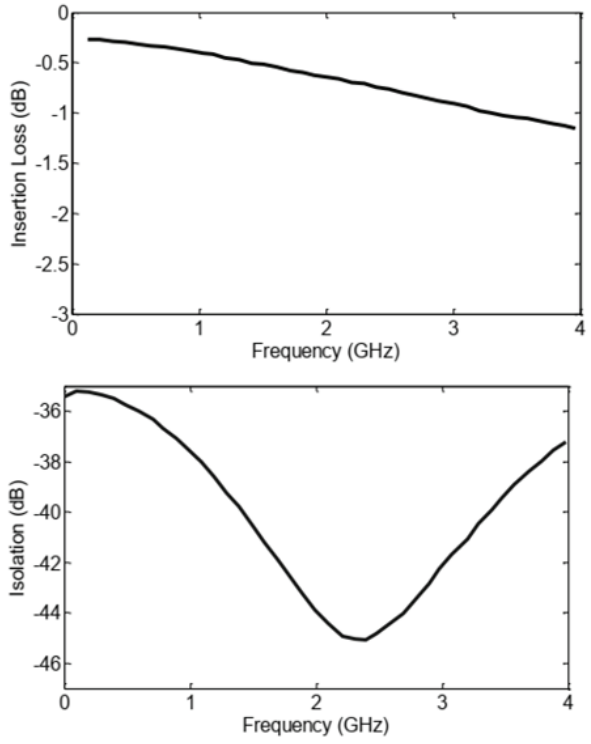

Figure 7: The insertion loss and the isolation of the SPDT.

3.1 SPDT Performance Analysis

Fig. 7 shows the insertion loss and the isolation of the SPDT as a function of the input signal frequency. At higher frequencies, the insertion loss is increased because of the effect of parasitic junction capacitances of the MOSs. The isolation of the switch is a maximum at the 2.4GHz set by the parallel resonant circuit, As the operating frequency shifts in both ways, the leakage causes the degradation of the isolation. The insertion loss and isolation of the SPDT at resonance are 0.83dB and 45.3dB respectively,

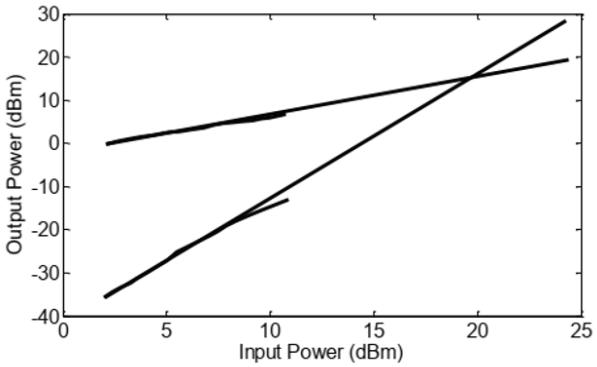

Figure 8: The P1dB and the IP3 of the SPDT.

Fig. 8 shows the power handling capacity and linearity of the SPDT. The P1dB point of this spdt is 11.3 dBm whereas the ip3 point is 19.60 dBm. Above this input power, the MOS body diodes experience break down which allow leakage of the signal to the ground. In the Monte-Carlo analysis for 50 samples, as illustrated in Fig. 9, the insertion loss was found between 0.88 dB and 0.82 dB, while the isolation was between 44.0 dB and 45.5 dB. The performance parameters of the SPDT were less dispersive and steady.

The performance parameters of this SPDT has been listed in Table 1 for comparing to the other recently reported switches. The diode connected transistor pair and suppressing the channel forming signal helped Chen and Lin (2014) to elevate IIP3 and input P1dB of the SPDT to 22.4dBm P1dB and 33 dBm IIP3, respectively [6]. But the isolation and die area were still not satisfactory. Proper impedance matching implementation by Tan et al. (2012) to design a high-power differential switch resulted in lower isolation compared to other designs [7]. Liu et al (2012) with his asymmetrical transistor based design succeeded to achieve lower IL and high P1dB but the core layout area was quite big

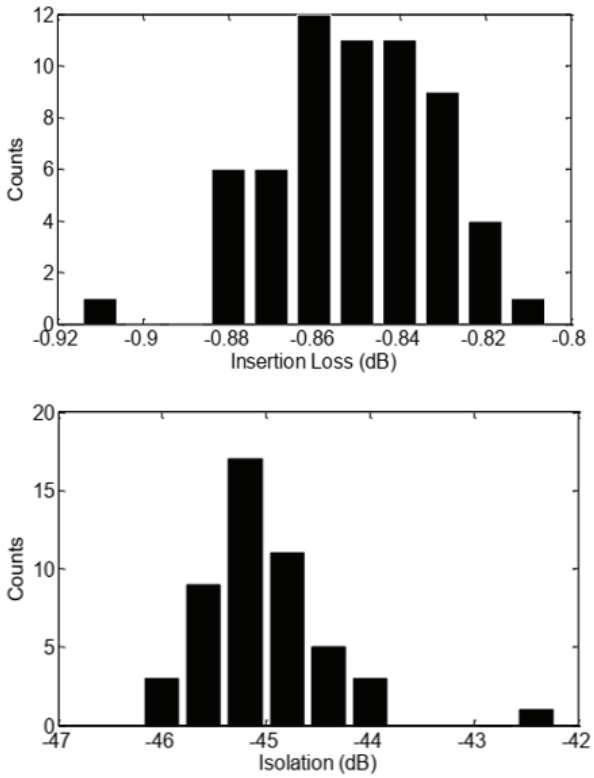

Figure 9: The Monte-Carlo analysis of insertion loss and isolation of the SPDT.

[8]. Body floated transistors with proper impedance matching resulted in 40 dB isolation switch design by Nga et al. (2016) but at the cost of bulky chip and higher IL [9]. The asymmetric SPDT utilizing ac-floating and dc-bias, designed by Chen and Gan (2017), achieved moderate P1dB but other parameters including chip area were quite undesired [10]. However, compared to these design, our SPDT realized the highest isolation and lowest die area due to the implementation of frequency dependent impedance imposed by parallel resonant circuit at 2.4 GHz band. All other parameters are reasonable and meets the 2.4 GHz prerequisites implying that our design demonstrates a good performance tradeoff for 2.4 GHz IoT applications.

Table 1: Summary of the SPDT performance comparison

Reference	CMOS Technology	IL (dB)	ISO (dB)	P1dB (dBm)	Chip Size (mm^2)
[8] (2012)	0.18 µm	0.62	33	29.2	0.125
[7] (2012)	32 nm	1.3	32	34	-
[6] (2014)	0.18 µm	0.72	24.5	22.4	0.037
[9] (2016)	65 nm	0.96	40	-	0.143
[10] (2017)	0.18 µm	1.16	20.8	20.5	0.26
This work	90 nm	0.83	45.3	11.3	0.03

3.2 LNA Performance Analysis

From the AC analysis, as shown in Fig. 10, it is observed that the proposed LNA circuit has a high gain of 33 dB with 30 MHz pass-band at the center resonant frequency of 2.45 GHz. Besides, the noise analysis of the LNA exhibits a noise figure of only 6.6 dB at its center frequency. The peak reverse isolation of the LNA is -33.1 dB at 2.4 GHz as shown in Fig. 11. The total power dissipation for this amplification operation, including the biasing and buffer circuits, equals the only 1.08 mW from a 1.5 V power supply which is very competitive compared to other contemporary researches. Moreover, the power handling capacity and third order linearity have been evaluated as given in Fig. 12 which are also very competitive. For statistical analysis, Monte-Carlo analysis has been conducted and it shows a stable performance of this LNA where the gain varied between 32.8 dB to 33.3 dB and NF varied between 6.4 dB to 6.8 dB for 50 samples as evident from Fig. 13.

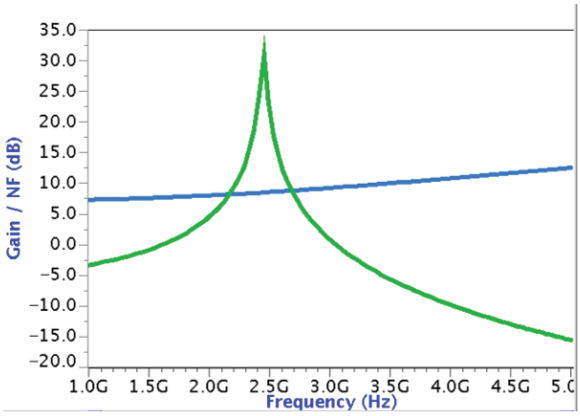

Figure 10: The AC and NF analysis of the LNA.

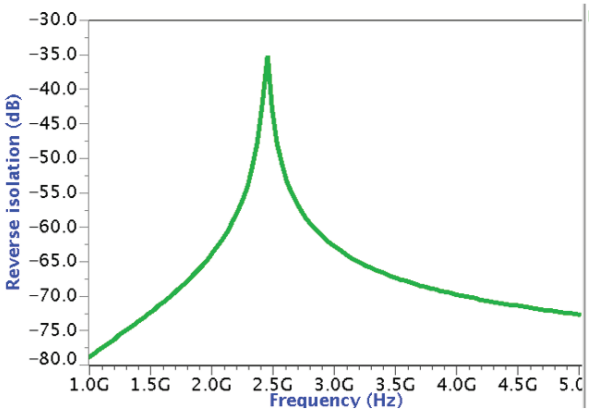

Figure 11: The reverse isolation analysis of the proposed LNA circuit.

Table 2 illustrates the performance comparison of the low noise amplifier with other recent researches. It is clear

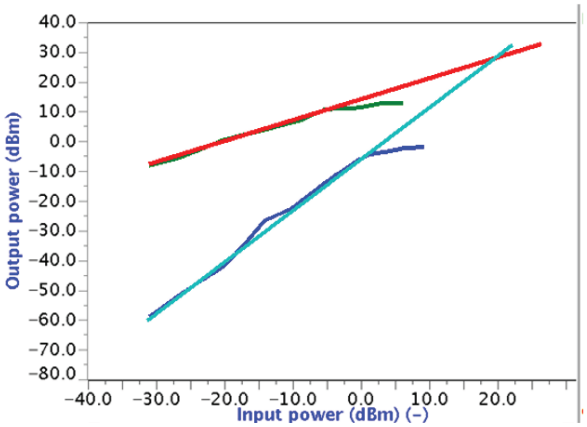

Figure 12: The linearity analysis of the proposed LNA circuit.

from the comparison that the inductorless LNA has the smallest die area which is only 127.704 μm^2. This is mainly due to the adaptation of small size transistors as well as avoidance of bulky passive constituents like capacitors, resistors etc. Moreover, the highest gain of 33 dB will facilitate the receiver frontend to amplify the weak intercepted signal by the antenna because of proper selection of transconductances. However, this work suffers from relatively higher noise figure of 6.6 dB at 2.4 Ghz frequency due to the simple common gate topology used for the amplification and also for using smaller sized transistors. Other parameters, including power dissipation and bandwidth, are also very competitive and support the requirements of 2.4 GHz RFID receiver specifications. Such a fully integrated inductorless LNA will be a handy block for low power compact readerless RFID for IoT applications operated at 2.4 GHz ISM band.

4 Conclusions

The widespread utilization of IoT, nowadays, urges the researchers to fabricate low power and portable de-

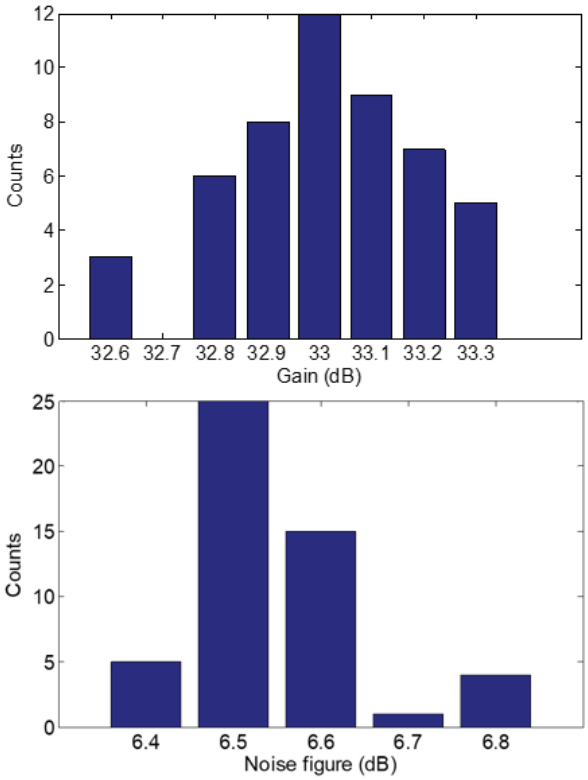

Figure 13: The Monte-Carlo analysis of gain and noise figure of the LNA circuit.

vices. The overall performance of the IoT devices depends on its frontend performance; specially on SPDT and LNA. In this research, the proposed inductorless nano-CMOS SPDT and LNA for 2.4 GHz RFID for IoT application were designed and assessed through the post-layout simulation by using Cadence. The results confirm that the design presented experiences a better performance tradeoff along with smaller power consumption and very compact die area compared to other concurrent researches after meeting all the requirements for 2.4 GHz RF communication. Such high-performance SPDT and LNA will certainly improve the

Table 2: Summary of the LNA performance comparison

Specifications	[22] (2016)	[20] (2017)	[24] (2017)	[21] (2018)	[25] (2019)	This work
Technology	130 nm CMOS	180 nm CMOS	180 nm CMOS	130 nm CMOS	65 nm CMOS	90 nm CMOS
fc (GHz)	2.45	2.5	3-5	2.4	0.5–7	2.45
Gain (dB)	12.3	16.9	12.7	20.7	16.8	33
Power dissipation (mW)	0.4	9.5	8.4	24.9	11.3	1.08
Supply voltage(V)	1.0	1.8	1.8	1.2	1.2	1.5
BW (MHz)	0.1-2.2 GHz	0.1-1.45 GHz	3.43 GHz	550	6.5 GHz	30
NF (dB)	4.9-6	2.5	3.2	2.1	2.87-3.77	6.6
Active Die area (mm^2)	0.0052	0.075	-	0.84	0.044	0.000127

performance of Wi-Fi compatible low power compact RFID as IoT devices.

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6 Conflict of Interest

The authors declare no conflict of interest. Besides, the funding sponsors had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, and in the decision to publish the results.

7 References

1. T. I. Badal et al., "Nano CMOS charge pump for readerless RFID PLL," Journal of Microelectronics, Electronic Components and Materials, 2019, Vol. 49, No. 2, pp. 53-60. https://doi.org/10.33180/InfMIDEM2019.201.
2. M. A. S. Bhuiyan et al., "A compact transmit/receive switch for 2.4 GHz reader-less active RFID tag transceiver," Journal of Central South University, 2015, Vol. 22, No. 2, pp. 546-51. https://doi.org/0.1007/s11771-015-2554-2.
3. M. A. S. Bhuiyan et al., "Design of a band-pass filter in 0, 18 µm CMOS for 2, 4 GHz reader-less RFID transponder," Technical Gazzatte 2017, Vol. 24, No.1, pp. 31-34. https://doi.org/10.17559/TV-20140330063721.
4. M. A. S. Bhuiyan et al., "Design trends in fully integrated 2.4 GHz CMOS SPDT switches," Current Nanoscience, 2014, Vol. 10, No. 3, pp. 334-343. https://doi.org/10.2174/15734137113096660106
5. P. Schmiedeke at al., "A fully integrated high IP1dB CMOS SPDT switch using stacked transistors for 2.4 GHz TDD transceiver applications," Sådhanå, 2018, vol. 43, article no. 94, pp. 1 - 7. https://doi.org/10.1007/s12046-018-0913-z
6. C. C. Chen, and G. C. Lin, "A CMOS T/R switch using a MOSFET diode pair for linearity improvement," 2014 Asia-Pacific Microwave Conference, 2014, pp. 735–737. URL: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7067768&isnumber=7067568
7. Y. Tan et al., "A 2.4- GHz WLAN transceiver with fully-integrated highly-linear 1.8-V 28.4-dBm PA, 34-dBm T/R switch, 240-MS/s DAC, 320-MS/s ADC, and DPLL in 32-nm SoC CMOS," Proceedings of the 2012 Symposium on VLSI Circuits (VLSIC 2012), 2012, pp. 76–77. https://doi.org/10.1109/VLSIC.2012.6243797.
8. S.L. Liu, M.H. Wu and A. Chin, "Design of a CMOS T/R switch with high power capability: using asymmetric transistors," IEEE Microwave Wireless Component Letter, 2012, Vol. 22, No. 12, pp. 645-647. https://doi.org/10.1109/LMWC.2012.2227465
9. T. T. K. Nga, D.S. Lee and K.Y. Lee, "A low insertion–loss, high–isolation switch based on single pole double throw for 2.4GHz BLE applications," IEIE Transactions on Smart Processing and Computing, 2016, Vol. 5, No. 3, pp.164-168. https://doi.org/10.5573/IEIESPC.2016.5.3.164.
10. L. Chen, and Y.B. Gan, "An asymmetrical bulk CMOS switch for 2.4 GHz application," Progress in Electromagnetic Research Letter, 2017, Vol. 66, pp. 99–104. https://doi.org/10.2528/PIERL17010905.
11. A. B. Hammadi et al., "An enhanced design of multi-band RF band pass filter based on tunable high-Q active inductor for nano-satellite applications," Journal of Circuits, Systems, and Computers, 2017, Vol. 26, No. 4, pp. 1-20. https://doi.org/10.1142/S0218126617500554.
12. Y. C. Hsiao, C. Meng and S. T. Yang, "2.4-GHz Q-enhanced lumped ring filter with two transmission zeros using 0.18-µm SiGe BiCMOS process," IEEE Microwave Wireless Component Letter, 2017, Vol. 27, No. 3, pp.305-307. https://doi.org/10.1109/LMWC.2017.2662000.
13. V. Kumar, R. Mehra and A. Islam, "A 2.5GHz low power, high-Q, reliable design of active bandpass filter," IEEE Transaction on Device and Material Reliabilty, 2017, Vol. 17, No. 1, pp. 229-244. https://doi.org/10.1109/TDMR.2017.2652142.
14. S. Lee, J. Park and S. Hong, "A Ka-band phase-compensated variable-gain CMOS low-noise amplifier," IEEE Microwave and Wireless Component Letter, 2019, Vol. 29, No. 2, pp. 131-33. https://doi.org/10.1109/LMWC.2018.2887335.
15. M. A. S. Bhuiyan et al., " Design Architectures of the CMOS Power Amplifier for 2.4 GHz ISM Band Applications: An Overview," Electronics, 2019, Vol. 8, No. 5, pp. 477. https://doi.org/10.3390/electronics8050477.
16. S. Wang and R. H. Chan, "2.4GHz CMOS bandpass filter using active transmission line," Electronic Letters, 2016, Vol. 52, No. 5, pp. 371-372. https://doi.org/10.1049/el.2015.3392.

17. M. A. S. Bhuiyan et al., "Advances in active inductor based CMOS band-pass filter," Micro and Nanosystems, 2018, Vol. 10, No. 1, pp.03-10. https://doi.org/10.2174/1876402910666180524121649.
18. D. Sachan, M. Goswami and P. K. Misra, "A high-Q floating active inductor using 130 nm BiCMOS technology and its application in IF band pass filter," Analog Integrated Circuits and Signal Processing, 2018, Vol. 96, No. 3, pp. 385–393. https://doi.org/10.1007/s10470-018-1196-3.
19. H.G. Momen, M. Yazgi, R. Kopru and A.N. Saatlo, "Design of a new low loss fully CMOS tunable floating active inductor," Analog Integrated Circuits and Signal Processing, 2016, Vol. 89, pp. 727–737. https://doi.org/10.1007/s10470-016-0784-3.
20. L. Ma, Z. G. Wang, J. Xu and N. M. Amin, "A high linearity wideband common-gate LNA with differential active inductor," IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, Vol. 64, No. 4, pp.402 - 406. https://doi.org/10.1109/TCSII.2016.2572201.
21. M. Muhamad, N. Soin and H. Ramiah, "Design of 2.4Ghz CMOS floating active inductor LNA using 130nm technology." IOP Conference Series: Materials Science and Engineering 2018, Vol. 341, pp. 1-7. https://doi.org/10.1088/1757-899X/341/1/012008.
22. M. Parvizi, K. Allidina and M. N. Gamal, "An ultra-low-power wideband inductorless CMOS LNA with tunable active shunt-feedback," IEEE Transactions on Microwave Theory and Techniques, 2016, Vol. 64, No. 6, pp. 1843 - 1853. https://doi.org/10.1109/TMTT.2016.2562003.
23. D. P. Patel and S. Oza, "CMOS active inductor: a technical review," International Journal of Applied Engineering Research, 2018, Vol. 13, No. 11, pp. 9680–9685. URL: https://www.ripublication.com/ijaer18/ijaerv13n11_131.pdf
24. J. Shima and J. Jeong, "A band-selective low-noise amplifier using an improved tunable active inductor for 3–5 GHz UWB receivers," Microelectronics Journal, 2017, Vol. 65, pp. 78 - 83. https://doi.org/10.1016/j.mejo.2017.03.018.
25. H. Yu et al., "A 0.044-mm2 0.5-to-7-GHz resistor-plussource-follower-feedback noise-cancelling LNA achieving a flat NF of 3.3±0.45 dB," IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, Vol. 66, No. 1, pp. 71 - 75. https://doi.org/10.1109/TCSII.2018.2833553.
26. Y. Zhang, F. Huang, L. Yang, X. Tang and Z. Chen, "A 2–5 GHz wideband inductorless low noise amplifier for LTE and intermediate-frequency-band 5G applications," IEICE Transactions on Fundamentals of Electronics, Communications and Computer Science, 2019, Vol. 102A, No. 1, pp. 209 - 10. https://doi.org/10.1587/transfun.E102.A.209
27. M. Ebrahimzadeh, F. Rezaei and S. Rezaei, "A new active inductor and its application to wide tuning range LC oscillator," International Journal of Soft Computing and Engineering, 2011, Vol. 1, No. 5, pp. 111-114. URL: http://www.ijsce.org/wp-content/uploads/papers/v1i5/E0162081511.pdf
28. Y. X. Feng, L. Kang, Y. Hao and X. Y. Bin, "A high isolation and low insertion loss T/R switch design," 10th IEEE International Conference on Solid-State and Integrated Circuit Technology, 2010, pp. 749-751. https://doi.org/10.1109/ICSICT.2010.5667403

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CMOS High-Performance 5-2 and 6-2 Compressors for High-Speed Parallel Multipliers

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Abstract: In this article, the design procedure for high-speed 5-2 and 6-2 compressors, along with their analysis, has been discussed. With the help of the combinational logic consisting of the 4-2 compressor and 3-2 counter blocks, a high-performance structure for 6-2 compressor has been achieved, which shows significant speed improvement over previous architectures. The optimization has been carried out by reducing the carry rippling issue between the adjacent compressor structures. Also, the help of some modifications, the proposed 6-2 compressor will turn into a 5-2 compressor where the latency of the critical path has considerably been reduced, illustrating the superiority of designed circuits. The corresponding latencies of the proposed 5-2 and 6-2 structures are equal to 3.5 and 4 XOR logic gates, respectively, demonstrating speed boosting of 15% and 20% compared to the best-reported architectures. In addition, the power consumption and the transistor count of proposed circuits are have remained at a moderate level. Therefore, by considering the Power-Delay Product (PDP), our work will be a good choice for high-speed parallel multiplier design. Post-layout simulation results based on TSMC 90nm standard CMOS process and 0.9V power supply have been presented to confirm the correct functionality of the implemented compressors. These results have also been used as a fair comparison infrastructure between the proposed works and redesignated architectures of the previously reported schemes.

Keywords: 6-2 compressor; 5-2 compressor; multiplier; CMOS; high-speed

Visoko učinkovit CMOS 5-2 in 6-2 kodirnik za vzporedne množilnike velikih hitrosti

Izvleček: V članku je predstavljen postopek načrtovanja in analiza hitrega 5-2 in 6-2 kodirnika. S pomočjo kombinatorne logike 4-2 kodirnika in 3-2 števca je bil izveden visoko učinkovit 6-2 kodirnik. Z dodatnimi poenostavitvami je bil načrtan 5-2 kodirnik pri katerem so bile močno zmanjšane latence kritičnih poti. Latence predlaganih 5-2 in 6-2 kodirnikov so enake 3.5 oziroma 4 XOR logičnim vratom, pri čemer je bila hitrost izboljšana za 15% oziroma 20%. Pri upoštevanju porabe se je izkazalo, da je predlagan kodirnik dober za hitre paralelne množilnike. Simulacije v standardnem CMOS okolju so potrdile rezultate raziskav. Rezultati pa so uporabljeni tudi za verno primerjavo nove arhitekture s prejšnjimi.

Ključne besede: 6-2 kodirniki; 5-2 kodirnik; množilnik; CMOS; visoka hitrost

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1 Introduction

In 1981 a new architecture was introduced by Weinberger, which was based on the cascaded carry-save adders [1]. Getting popular as 4-2 compressor, the structure was composed of two Full Adders (FAs). One of the outputs of such structure (denoted as C_{out}) is horizontally sent to the next sitting compressor block with a higher binary bit position value [2]. Figure 1 illustrates the explained structure in which X1 – X4 constitute the main input bits while the fifth input comes from the previous compressor with a lower binary bit value [3].

Along with the development of VLSI circuits, which provided the possibility for hardware-level realization of the parallel multipliers [4], the applications of such systems were greatly increased in Digital Signal Processors (DSPs) and microprocessors. A thorough literature review depicts that the parallel multiplier lies in the critical path for delay measurement of its former system [5]. Also, the most significant part of the propagation latency in a parallel multiplier belongs to the Partial Product Reduction Tree (PPRT) consisting of the compressors [6]. As a consequence, delay reduction for PPRT in state-of-the-art schemes is one of the main concerns for the circuit designers.

One of the effective solutions for this purpose that impressively applies to the large input bit multiplications is the utilization of high compression rate compressors such as 5-2, 6-2, and 7-2 blocks [7].

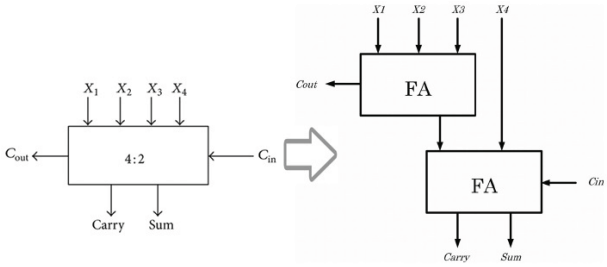


Figure 1: General architecture of the 4-2 compressor consisting of two cascaded FAs.

Following the general concept of the 4-2 compressor, the cascading of three FAs will result in the conventional architecture of 5-2 compressor [7]. At least a latency of 5 XOR logic gates (in gate-level) is expected for this realization where with the help of some optimizations reported in [8], the delay has been reduced to 4 XOR gates. Although there are many structures reported in the literature [8, 9, 10, 11, 12, 13, 14], none of them have been able to reach latencies less than 4 XOR gates. This partially comes down to the lack of deep consideration and investigation of the original truth table for the 5-2 compressor block.

The structure of a 6-2 compressor consists of three horizontal paths which transfer their corresponding bits to the adjacent block. Although several works have been introduced over recent years for hardware implementation of this structure [10, 15, 16, 17, 18, 19], none of them could achieve latencies less than 5 XOR logic gates.

A comprehensive study over n-2 compressor design depicts that there are some neutral states in the conventional truth table. These states can be helpful in the simplification of the Karnaugh Map (KM) for the corresponding compressor. The main objective is to obtain better speed performance while the power consumption would not be degraded. This concept is the basis of the idea in this article to design a high-performance 6-2 compressor. Furthermore, after successfully applying the mentioned idea to the 6-2 structure and by using some simplifications, a novel 5-2 compressor will be presented later in this paper. This scheme also outperforms previous works when the Power-Delay Product (PDP) is concerned.

One important issue that needs to be considered in the design of the proposed structures is the reduction of carry rippling problem between the adjacent compressor blocks. For instance, in the horizontally cascaded architectures of Figure 2, the conventional design principles will lead to the rippling of input signals to three compressor blocks. The same concept also holds for 6-2 compressor. However, in this paper, careful design considerations have utilized to reduce the carry rippling problem by one level. The effect of such decrement is the key factor for speed enhancement.

The organization of the paper is as follows. Section 2 explains the analysis and design of the proposed high-performance 6-2 compressor. In section 3, the novel 5-2 compressor architecture has been discussed. Post-Layout simulation results, along with the comparison tables, have been presented in section 4. Finally, section 5 contains the conclusions.

2 The 6-2 compressor

The conventional structure of a 6-2 compressor comprises two FAs along with one 4-2 compressor, as shown in Figure 3. Based on the defined architecture, a 6-2 compressor is composed of nine inputs and five outputs. The following expression describes the relationship between the input and output bits [10]:

$$\begin{aligned} I_1 + I_2 + I_3 + I_4 + I_5 + I_6 + C_{in1} + C_{in2} + C_{in3} \\ = Sum + 2 \times \left(Carry + C_{out1} + C_{out2} + C_{out3} \right) \end{aligned} \quad (1)$$

As Eq. (1) shows, all of the input bits along with output have the same weighting while the other four outputs will assume the next higher binary bit value. By considering the proposed architectures for 4-2 compressor reported in [2] and [3], which exhibit 2 XOR logic gate-level delay from inputs to the outputs, the latency of less than 5 XOR logic gates is expected for implementation of the 6-2 compressor in Figure 3.

The design introduced in [10], directly uses the conventional structure for hardware realization of a 6-2 compressor. Because the 4-2 compressor of [7] was employed, the latency of the circuit was equal to 5 XOR gates. If the compressor of [3] is going to be used in that structure, again, a slight amount of gate-level reduction can be achieved for the critical path delay.

In [15] and [19], gate-level simplification has been utilized for the design of 6-2 compressor. However, the critical path delay which belongs to output is still 5 XOR gates. The architectures used in [17] and [18] have modified the conventional structure by using two 4-2 compressors and one adder. But they were not able to reduce the latency, and due to the higher transistor count, neither active area nor power consumption has been improved.

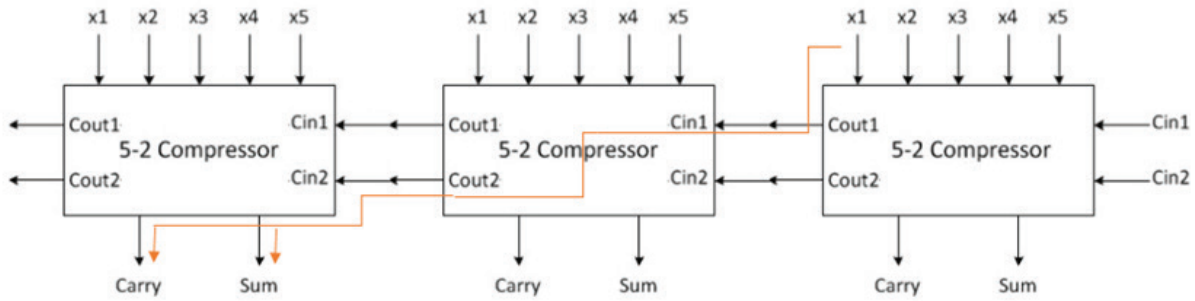


Figure 2: The carry rippling problem between three cascaded 5-2 compressor blocks.

By considering the aforementioned implementations and their drawbacks, in this paper, a new architecture has been proposed for the 6-2 compressor. In this realization, the gate-level delay has been reduced considerably.

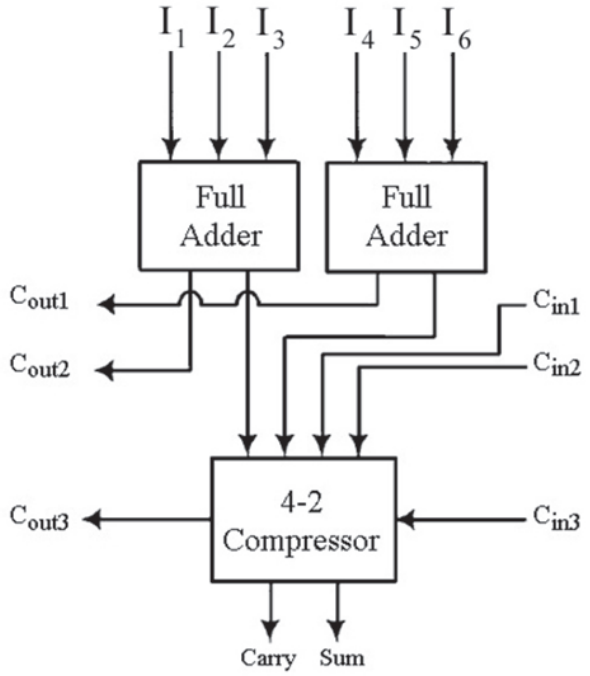


Figure 3: Conventional structure of 6-2 compressor.

The proposed circuit is shown in Figure 4, in which the pins labeled I_1, I_2, I_3, I_4, I_5, and I_6, along with C_{in1}, C_{in2}, and C_{in3}, constitute the input bits. Also, C_{out1}, C_{out2}, and C_{out3}, along with *Carry*6 - 2 and *Sum*6 - 2 form the output bits. The operating principle of the proposed structure can be seen as a 4-2 compressor that is fed by I_1, I_2, I_3, I_4, and I_5 inputs. These inputs are then utilized to generate C_{out1} and C_{out2} outputs of the 6-2 compressor. If at least two of five inputs have high-level logic value, then one of C_{out1} and C_{out2} outputs will rise to high-level voltage. If at least four input bits have the logic value of one, then both of the outputs will get the high logic value as well. By considering the conventional architecture of the 4-2 compressor described in [7], the Boolean expressions pertaining to the functions of C_{out1} and C_{out2} will be as follows:

$$C_{out1} = (I_1 \oplus I_2 \oplus I_3 \oplus I_4).I_5 + \overline{(I_1 \oplus I_2 \oplus I_3 \oplus I_4).I_4} \quad (2)$$

$$C_{out2} = (I_1 \oplus I_2).I_3 + \overline{(I_1 \oplus I_2).I_1} \quad (3)$$

The odd number of ones at the input pins will result in the corresponding sum output signal (denoted as *Sum*4 - 2) to get the high logic value.

For the comparison of three horizontal inputs (represented as C_{in1}, C_{in2}, and I_6), an FA has been utilized where the corresponding carry output of this stage will establish the C_{out3} output of the proposed 6-2 compressor. In order to increase the speed performance, the three gates model of FA from [12] has been employed to implement such block. This output abides by the following relation:

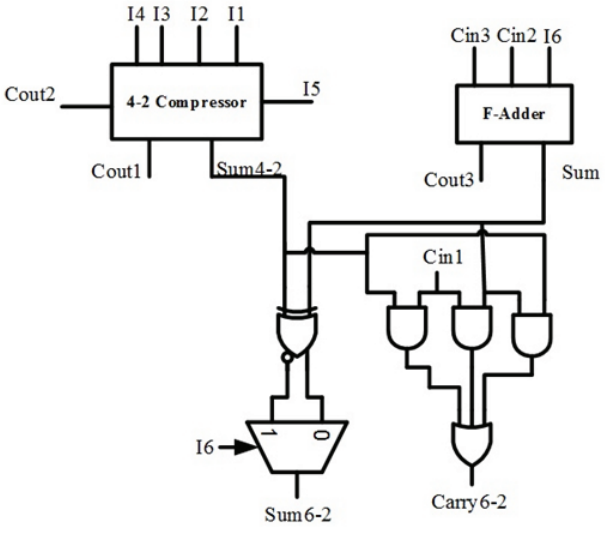


Figure 4: Proposed 6-2 compressor.

$$C_{out3} = \left(C_{in2} + C_{in3}\right).I_6 + C_{in2}.C_{in3} \tag{4}$$

The combination of two sum outputs coming from 4-2 compressor and the FA block will construct the Sum output of the 6-2 compressor, which is noted as *Sum*6 - 2. Finally, for *Carry* output will have:

$$\begin{aligned} Carry = &\left(\left(I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5\right) + \left(C_{in2} \oplus C_{in3} \oplus I_6\right)\right).C_{in1} \\ &+ \left(\left(I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5\right).\left(I_6 \oplus C_{in2} \oplus C_{in3}\right)\right) \end{aligned} \tag{5}$$

The calculated Boolean expressions clearly demonstrate that the carry rippling issue has been reduced by one, which is a notable advantage of the proposed 6-2 compressor.

To calculate the gate-level latency, we refer to the calculations provided in [7]. As shown in Figure 5(a) and discussed in [7], the latency of two output XOR/XNOR gate is considered Δ. As a consequence, the propagation delay of the single output XOR gate in Figure 5(b) will be equal to 0.75 Δ, considering the fact that the Transmission Gate (TG) transistors are channel-ready transistors. For a channel-ready transistor, the corresponding latency is half of a transistor where the bias signal of the gate didn't put the transistor in ON state.

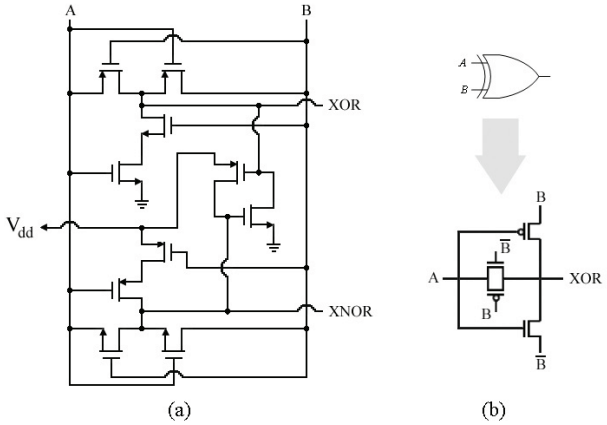


Figure 5: The XOR gates used in the compressor circuits (a) Two output XOR-XNOR gate proposed in [7] (b) Single output XOR gate introduced in [2].

The same hypothesis also holds for the Multiplexer (MUX) gate of Figure 6, which is composed of two paralleled TGs. In the normal mode, the normalized latency of this gate will be equal to 0.5 Δ, while for the channel-ready case, the corresponding delay will be reduced to 0.25 Δ.

Furthermore, the three input OR gate can be treated almost the same as two output XOR-XNOR gate concerning the propagation latency. Also, a single pass transistor-like device will have a delay value of 0.25 Δ of the unit gate [2]. The NAND/NOR gates will also be treated the same as the MUX circuit, which is operating in the normal mode.

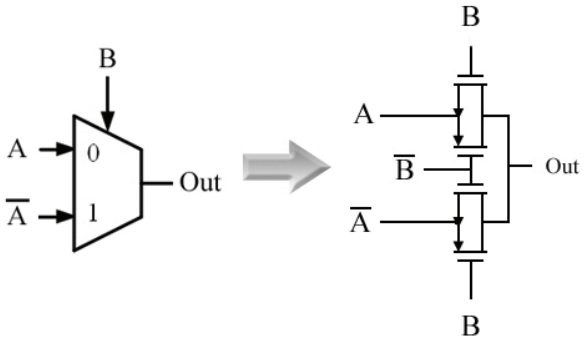


Figure 6: Utilized MUX gate and its circuitry.

Therefore, according to the circuit structure in Figure 4, the critical path of the proposed 6-2 compressor will belong to *Carry* output. The start point for this path is at C_{out2} output coming from the adjacent compressor, which then enters the FA block inside the proposed present 6-2 compressor. Such a gate-level delay (T_d) will abide by:

$$T_d = t_{Cout2} + t_{FA} + t_{AND} + t_{3OR} \tag{6}$$

in which t_{Cout2} defines the corresponding delay for the generation of C_{out2} from the previous level compressor block. Moreover, t_{FA} illustrates the time interval for the generation of output in Figure 4. The terms t_{AND} and t_{3OR} represent the latencies for AND, and three input OR gates, respectively. By considering the optimizations pertaining to the conversion of AND to NOR and OR to NAND, t_{AND} and t_{3OR} can be replaced by t_{NOR} and t_{3NAND} to reduce the gate-level latency.

Because the 4-2 compressor block reported in [3] has been utilized to achieve higher speed performance, t_{Count2} will be equal to Δ. On the other hand, in an FA block, two single output XOR gates are needed to produce *Sum*. Therefore, t_{FA} will be equal to 1.5 Δ. Substitution of the obtained values in Eq. (6), will result in:

$$T_d = \Delta + 1.5\Delta + 0.5\Delta + \Delta = 4\Delta \tag{7}$$

As Eq. (7) expresses, the gate-level delay of the proposed compressor is almost equal to 4 XOR logic gates, which is a substantial improvement for the delay performance of the proposed 6-2 compressor compared with the previously reported works.

3 The 5-2 compressor

By applying some modifications, the designed 6-2 compressor can be used as a high-speed 5-2 compressor. In order to achieve this configuration, *Sum*. Therefore, t_{FA} will be equal to 1.5 Δ. output should be connected to the ground. The proposed architecture has been illustrated in Figure 7.

Because one of the inputs to the FA cell has been eliminated, therefore, this block can be replaced with a Half Adder (HA), which is denoted in Figure 7 as H-Adder. Equations (8), (9), (10), and (11) present the corresponding expressions for the four output signals of this system:

$$Sum = I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5 \oplus C_{in1} \oplus C_{in2} \quad (8)$$

$$Carry = (I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5).(C_{in1} \oplus C_{in2}) + C_{in1}.C_{in2} \quad (9)$$

$$C_{out1} = (I_1 \oplus I_2 \oplus I_3 \oplus I_4).I_5 + \overline{(I_1 \oplus I_2 \oplus I_3 \oplus I_4).I_4} \quad (10)$$

$$C_{out2} = (I_1 \oplus I_2).I_3 + \overline{(I_1 \oplus I_2).I_1} \quad (11)$$

With the help of the same definitions for propagation latency, it can easily be concluded that the delay of the critical path for the proposed 5-2 compressor will belong to the *Carry* signal. By starting from the C_{out1} node of the adjacent compressor, the path will end in the HA block. This can be expressed in terms of gate-level delay (T_d), by means of the following expression:

$$T_d = t_{Cout1} + t_{HA} + t_{AND} + t'_{MUX} \quad (12)$$

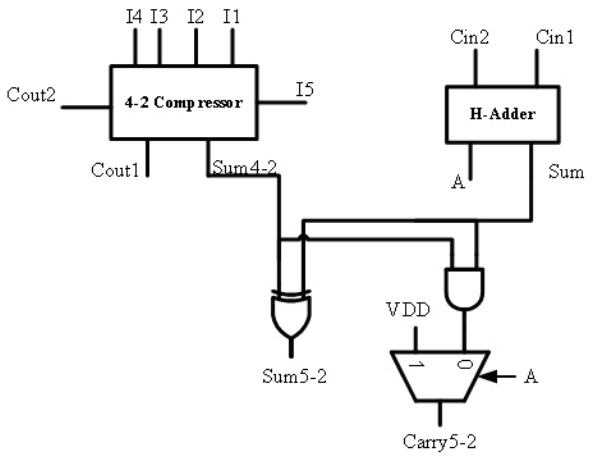


Figure 7: Proposed 5-2 compressor.

In this equation, t_{Count1} represents the delay associated with the generation of C_{out1} from the previous compressor block, which is equal to the summation of two different terms.

Again, by considering the 4-2 compressor architecture of [3], the first term will belong to a two output XOR-XNOR gate. The second term will pertain to the latency of two cascaded MUX gates with channel-ready transistors. As a consequence, t_{Cout1} will be equal to 1.5Δ.

For a HA block, the propagation latency denoted by t_{HA} will be equal to that of a single output XOR gate (0.75Δ). But for the AND gate, the combination of a NAND and inverter gate is needed, which makes the corresponding delay of this gate (t_{AND}) be equal to Δ. Finally, t'_{MUX} represents the propagation latency of a channel-ready MUX, which is equal to 0.25Δ. The sum of these latencies will result in the following value:

$$T_d = 1.5\Delta + 0.75\Delta + \Delta + 0.25\Delta = 3.25\Delta \quad (13)$$

As Eq. (13) expresses, the gate-level delay of the designed compressor is almost 3.5 XOR logic gates, which is a notable improvement for the speed performance of this block.

4 Simulation results

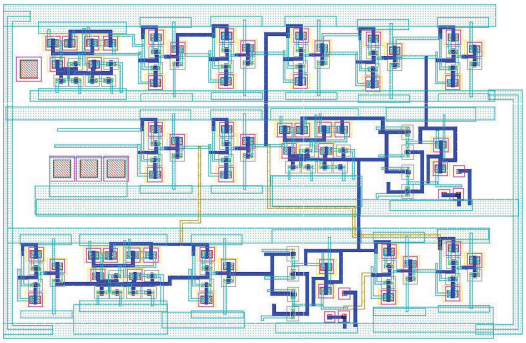
In order to perform a thorough analysis and comparison for the simulation results of the works, which are discussed in this paper, at the first step, the layouts of the designed circuits have been drawn, and their parasitics have been extracted. After that, some of the recently reported structures in the literature for 6-2 and 5-2 compressors with remarkable results and improvements have been selected and redesigned here using the similar gates employed for this work.

Figure 8 illustrates the layout schemes for the proposed architectures. In Figure 8(a), the layout of the 6-2 compressor has been shown, which occupies an active area of 55×35mm^2. For the implemented 5-2 compressor, as demonstrated in Figure 8(b), an active area of 35×30mm^2 is needed.

In order to resemble the practical situation in the simulation setup, each of the inputs is driven by a buffer circuit. Every output has been passed through a buffer block as well to be able to drive the next stage without loading effect on the compressor circuit. In addition, the compressor blocks are used in a parallel fashion to cover the critical path, as shown in Figure 9.

It must be mentioned that the configuration of Figure 9 is used for the case in which the propagation delay between two adjacent compressor structures finishes in the second compressor block. If the propagation delay is rippled for three horizontally cascaded compressors, then three compressors must be considered in the simulation environment. This fact has been presumed for the architectures reported in [9], [10], [12], [13], [14], [18] and [19] (similar as Figure 2).

(a)



(b)

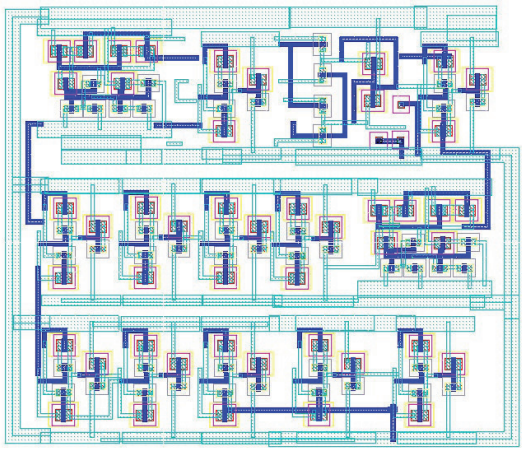


Figure 8: Layouts of the proposed architectures (a) 6-2 compressor (b) 5-2 compressor.

Meanwhile, in the simulation environment, the propagation delay has been measured from the point that the earliest input transition reaches 50% of V_{dd}, to the point where the latest output signal rises to 50% of the V_{dd} voltage. [7]. The worst-case, which demonstrates the longest latency from inputs to the outputs (considering the signal propagation between the adjacent blocks), shows the delay of the critical path.

4.1 The 6-2 compressor

Post-layout simulations using HSPICE for TSMC standard 90nm CMOS technology along with 0.9V power supply have been carried out to measure the delay, and power consumption of the proposed 6-2 compressor and the works reported in [10], [18] and [19] which are

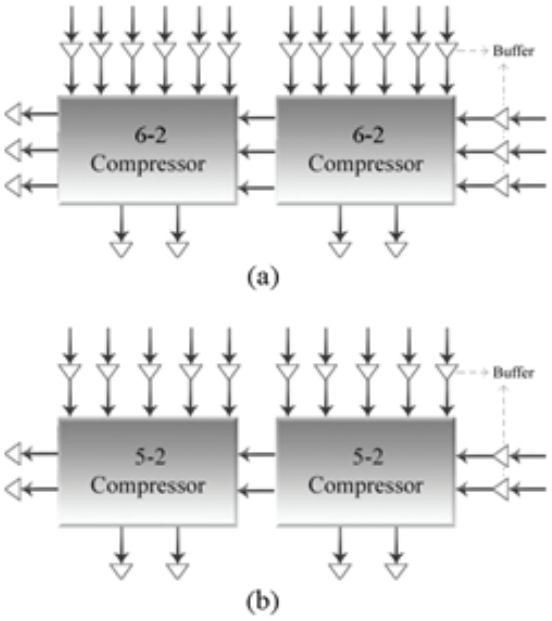


Figure 9: Simulation setup for (a) 6-2 compressor (b) 5-2 compressor considering the propagation delay for two stages.

redesigned and optimized here to make a fair comparison.

Figure 10 illustrates the results for the correct functionality of the proposed architecture along with delay measurements. The results demonstrate the delay of 314ps for the critical path of the proposed circuit.

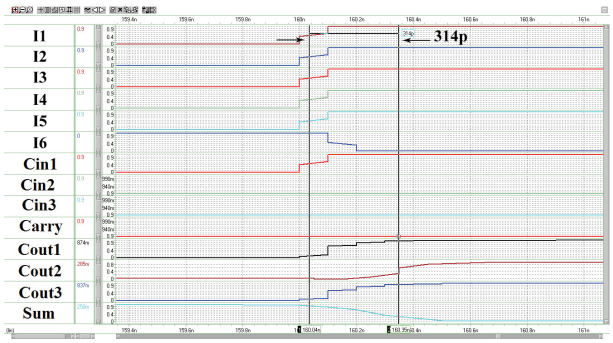


Figure 10: Simulation results for correct functionality and delay measurement of the proposed 6-2 compressor.

The result of the comparison for the power-delay measurement of the designed structure and the selected works is shown in Figure 11. The results indicate that the lowest PDP value belongs to the proposed architecture. The design reported in [19], which has a delay value of about 481ps will need 53% more time to produce the output compared to the designed scheme.

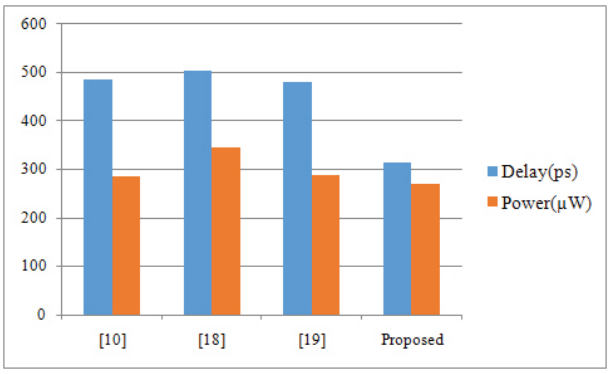


Figure 11: Power-Delay comparison of the proposed work and redesigned 6-2 compressors based on the TSMC 90nm CMOS process.

Also, the measurement results for the power dissipation at the operating frequency of 100MHz demonstrate that the proposed compressor circuit has the lowest value of power consumption, while the design reported in [10] which shows the lowest power consumption among the competitors, consumes 6% more power compared to the proposed circuit.

Table 1 illustrates the comparison between the redesigned 6-2 configurations based on their circuitry and simulation results obtained by the author.

Table 1: Comparison of Proposed 6-2 Compressor and Other Structures.

Work	Proposed	[10]	[18]	[19]
Technology (nm)	90	90	90	90
Transistor Count	125	140	152	142
Gate Level Delay (XOR)	4 gates	5 gates	6 gates	5 gates
Power (µW) @100MHz	269	285	345	289
Delay(ps)	314	487	505	481
PDP (pJ)	0.084	0.139	0.174	0.139

4.2 The 5-2 compressor

As described for 6-2 compressor, post-layout simulations using HSPICE for TSMC standard 90nm CMOS technology along with 0.9V power supply have been carried out to measure the delay and power consumption of the proposed 5-2 compressor and redesigned architectures reported in [8], [9], [10], [12], [13], and [14].

Figure 12 illustrates the results for the correct functionality of the proposed structure along with the delay measurement, which depicts the value of 183ps for the delay of the critical path.

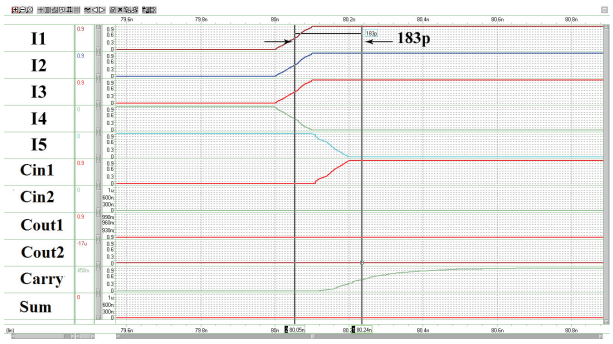


Figure 12: Simulation results for correct functionality and delay measurement of the proposed 5-2 compressor.

The result of the comparison for the power-delay measurement of the proposed design and the redesigned works is shown in Figure 13. The results indicate that the lowest delay value belongs to the designed scheme. Also, the measurement result and comparison for power dissipation at the operating frequency of 100MHz demonstrates that the power consumption of the proposed design is about 97µW, which is not the lowest among the presented works. The designs reported in [13] and [14] have the lowest power consumption. However, the lowest PDP belongs to the proposed scheme.

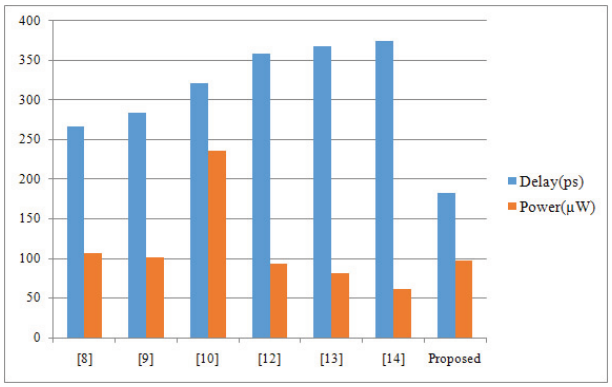


Figure 13: Power-Delay comparison of the proposed work and redesigned 5-2 compressors based on the TSMC 90nm CMOS process.

Finally, Table 2 summarizes the comparison between the redesigned 5-2 structures based on their circuitry and simulation results obtained by the author.

5 Conclusions

In this article, a novel 6-2 compressor was introduced, which outperforms the previous designs from the viewpoint of the propagation delay for the critical path. The proposed architecture is based on the combinational

Table 2: Comparison of Proposed 5-2 Compressor and Other Structures.

Work	Proposed	[8]	[9]	[10]	[12]	[13]	[14]
Technology (nm)	90	90	90	90	90	90	90
Transistor Count	97	112	112	135	90	82	58
Gate Level Delay (XOR)	3.5 gates	4 gates	5 gates	5.5 gates	6 gates	6 gates	6 gates
Power (µW) @100MHz	97	107	101	236	94	81	61
Delay(ps)	183	247	284	321	359	368	375
PDP (pJ)	0.0177	0.0286	0.0287	0.0757	0.0337	0.0298	0.0229

circuit consisting of a 4-2 compressor and FA, which has resulted in a 20% speed improvement in comparison with the other works reported in this criterion. The design approach for the proposed compressor was able to reduce the number of transistors used in the circuit. This is another advantage of the presented circuit, which will occupy a small area on the chip while the carry rippling problem has been reduced by one level.

With some extra modifications, the proposed 6-2 compressor can be used as a 5-2 compressor. In this case, the latency of the critical path has also been reduced significantly. The gate-level delay of the proposed 5-2 and 6-2 compressors is equal to 3.5 and 4 XOR logic gates, respectively, which demonstrate a 15% speed enhancement for the proposed 5-2 architecture compared with the best-reported works. The aforementioned advantages illustrate the capability of the implemented circuits for utilization in high compression multiplication systems.

Simulation results of the proposed circuits using HSPICE for TSMC 90nm standard CMOS technology and 0.9V power supply represent the delay value of 314ps and 183ps for the proposed 6-2 and 5-2 compressors, respectively. The power dissipation is also 269µW and 97µW for these structures at the operating frequency of 100MHz.

6 Conflict of Interest

The author declares no conflict of interest.

The author declares that there is no funding support for this work.

7 References

1. A. Weinberger, "4:2 Carry-Save Adder Module," *IBM Technical Disclosure Bull.*, vol. 23, 1981.
2. A. Fathi, S. Azizian, Kh. Hadidi, A. Khoei, and A. Chegeni, "CMOS Implementation of a Fast 4-2 Compressor for Parallel Accumulations," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1476–1479, 2012, https://doi.org/10.1109/ISCAS.2012.6271526.
3. A. Fathi, S. Azizian, Kh. Hadidi, and A. Khoei, "A Novel and Very Fast 4-2 Compressor for High Speed Arithmetic Operations," *IEICE transactions on electronics*, vol. 95, no. 4, pp. 710–712, 2012, https://doi.org/10.1587/transele.E95.C.710.
4. P. Aliparast, Z. D. Koozehkanani, and F. Nazari, "An Ultra High Speed Digital 4-2 Compressor in 65-nm CMOS," *International Journal of Computer Theory and Engineering*, vol. 5, no. 4, pp. 593–597, 2013, https://doi.org/10.7763/IJCTE.2013.V5.756.
5. A. Fathi, S. Azizian, Kh. Hadidi, and A. Khoei, "Ultra High Speed Modified Booth Encoding Architecture for High Speed Parallel Accumulations," *IEICE transactions on electronics*, vol. 95, no. 4, pp. 706–709, 2012, https://doi.org/10.1587/transele.E95.C.706.
6. H.-L. Lin, R.C. Chang, and M.-T. Chan, "Design of a Novel Radix-4 Booth Multiplier," *The 2004 IEEE Asia-Pacific Conference on Circuits and Systems*, vol. 2, pp. 837–840, 2004, https://doi.org/10.1109/APCCAS.2004.1413009.
7. C.-H. Chang, J. Gu, and M. Zhang, "Ultra Low-Voltage Low-Power CMOS 4-2 and 5-2 Compressors for Fast Arithmetic Circuits," *IEEE Transactions on Circuits and Systems I*, vol. 51, no. 10, pp. 1985–1997, 2004, https://doi.org/10.1109/TCSI.2004.835683.
8. O. Kwon, K. Nowka, and E.E. Swartzlander, "A 16-bit x 16-bit MAC Design Using Fast 5-2 Compressors," *Proceedings of IEEE International Conference on Application-Specific Systems, Architectures, and Processors*, pp. 235–243, 2000, https://doi.org/10.1109/ASAP.2000.862394.
9. K. Prasad, and K.K. Parhi, "Low-power 4-2 and 5-2 compressors," *IEEE Thirty-Fifth Asilomar Conference on Signals, Systems and Computers*, 2001, https://doi.org/10.1109/ACSSC.2001.986892.
10. W. Ma, and Sh. Li, "A new high compression compressor for large multiplier," *9th International Conference on Solid-State and Integrated-Circuit Technology (ICSICT)*, 2008, https://doi.org/10.1109/ICSICT.2008.4734925.

11. M. Tohidi, M. Mousazadeh, S. Akbari, Kh. Hadidi, and A. Khoei, "CMOS implementation of a new high speed, glitch-free 5-2 compressor for fast arithmetic operations," *Proceedings of the 20th International Conference Mixed Design of Integrated Circuits and Systems (MIXDES)*, 2013.
12. S. Veeramachaneni, K. M. Krishna, L. Avinash, S. R. Puppala, and M.B. Srinivas, "Novel Architectures for High-Speed and Low-Power 3-2, 4-2 and 5-2 Compressors," *20th Int. Conf. VLSI Design*, pp. 324-329, 2007, https://doi.org/10.1109/VLSID.2007.116.
13. A. Najafi, S. Timarchi, and A. Najafi, "High-speed Energy-efficient 5:2 Compressor," *37th Int. Convention on Information and Communication Technology, Electronics and Microelectronics*, 2014, https://doi.org/10.1109/MIPRO.2014.6859537.
14. D. Balobas, and N. Konofaos, "Low-power high-performance CMOS 5-2 compressor with 58 transistors," *Electronics Letters*, vol. 54, no. 5, pp. 278-280, 2018, https://doi.org/10.1049/el.2017.3339.
15. W. Shi, M. Cai, and T. Zhong, "A Partial Parallel folding Multiplier Design for 1024 bit Modular Multiplication," *8th International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, 2006, https://doi.org/10.1109/ICSICT.2006.306593.
16. M. Kalemati, M.Z. Moghadam, and K. Navi, "Depth-Optimized Reversible 4:2 and 6:2 Compressors," *Int. J. Emerg. Sci.*, vol. 3, no. 4, pp. 359-369, 2013.
17. G. Paim, M. Fonseca, E. Costa, and S. Almeida, "Power efficient 2-D rounded cosine transform with adder compressors for image compression," *IEEE International Conference on Electronics, Circuits, and Systems (ICECS)*, 2015, https://doi.org/10.1109/ICECS.2015.7440320.
18. G. Paim, and E. Costa, "Using adder compressors for power-efficient 2-D approximate Discrete Tchebichef Transform," *14th IEEE International New Circuits and Systems Conference*, 2016, https://doi.org/10.1109/NEWCAS.2016.7604835.
19. W. Shi, and C.-S. Choy, "A 0.4V 320Mb/s 28.7μW 1024-bit configurable multiplier for subthreshold SOC encryption," *29th IEEE International System-on-Chip Conference (SOCC)*, 2016, https://doi.org/10.1109/SOCC.2016.7905451.

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Single VDGA-Based Dual-Mode Multifunction Biquadratic Filter and Quadrature Sinusoidal Oscillator

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Abstract: This article relates to the realization of voltage-mode and/or current-mode multifunction biquadratic filter and quadrature oscillator circuits each using one voltage differencing gain amplifier (VDGA), two resistors and two grounded capacitors. The proposed dual-mode filter having one output and three inputs can provide the three standard biquadratic transfer functions with both voltage and current output filter responses simultaneously. It also has the independent tuning of the angular resonance frequency and the quality factor. With a slight modification of the proposed filter, a new dual-mode quadrature sinusoidal oscillator can be obtained. The proposed quadrature oscillator provides orthogonal resistive/electronic control of both oscillation condition and oscillation frequency. Non-ideal and parasitic conditions are also examined and their effects on the circuit performance are discussed. To confirm the theory, several computer simulation results with PSPICE program are given.

Keywords: Voltage Differencing Gain Amplifier (VDGA); biquadratic filter; quadrature oscillator; dual-mode operation; voltage-mode circuit; current-mode circuit

Enojen multifunkcijski bi-kvadratičen filter na osnovi VDGA in sinusni kvadrantni oscilator

Izvleček: Članek opisuje multifunkcijski bi-kvadratičen filter v napetostnem in/ali tokovnem načinu ter kvadrantni oscilator. Oba sta zasnovana na osnovi VDGA ojačevalnik, dveh uporov in dveh ozemljenih kondenzatorjev. Predlagan filter ima en izhod in tri vhode, kar omogoča uporabo treh standardnih bikvadratičnih funkcij sočasno na napetostnem in tokovnem izhodu. Omogoča tudi neodvisno nastavljanje kotne resonančne frekvence in faktorja kvalitete. Z majhnimi spremembami lahko dobimo sinusni oscilator. Raziskani so tudi neidealni in parazitni pogoji in njihov vpliv na učinkovitost vezja. Teorija je bila preverjena v PSPICE simulacijskem okolju.

Ključne besede: (VDGA); bikvadratičen filter; kvadrantni oscillator; napetostni način; tokovni način

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1 Introduction

Multifunction filters, which can simultaneously realize low-pass (LP), band-pass (BP) and high-pass (HP) filter responses with the same configuration, are fundamental circuit elements widely used in the design of several electronic systems, such as phase-locked loop frequency modulators, crossover networks, stereo demodulators, etc.[1]-[2]. For decades, multifunction biquadratic filters have been designed by using numerous modern electronic active elements, such as second-generation current conveyor (CCII) [1], [5]-[9], differential voltage current conveyor (DVCC) [2]-[3], [10]-[11], differential difference current conveyor (DDCC) [4], differential voltage current conveyor transconductance amplifier (DVCCTA) [12], universal voltage conveyor (UVC) [13], unity gain cells [14]-[15], current-controlled current conveyor (CCCII) [16], voltage differencing gain amplifier (VDGA) [19], voltage differencing transconductance amplifier (VDTA)

[20-23]. Considering the number of input and output terminals, the previously designed configurations in literature can be classified as single-input multi-output (SIMO) [1], [3-7], [11-15], [18], [19], [22-23], multi-input single-output (MISO) [8], [10], [21] and multi-input multi-output (MIMO) [9], [16-17] filter topologies. If the type of signal processing is considered, these filters can further be classified as voltage-mode [3-7], [10-13], [16], [20], current-mode [1-2], [8-9], [14], [17-18], [21], and dual-mode [15], [19], [22-23] filter topologies. However, this finding focuses on the design of the dual-mode SIMO multifunction biquad filter with both voltage and current output responses using only a single active element. The topology in the literature [15] needs to employ four voltage followers, four dual-output current followers, seven resistors, and two grounded capacitors. In [19], the single -input three-output dual-mode multifunction filter was developed by using two VDGAs and three capacitors. However, this configuration does not have the feature of independent control of its natural angular frequency (ω_o) and quality factor (Q). Separate studies in [22-23] introduced SIMO dual-mode biquad filters combining a single VDTA, one grounded resistor, and three capacitors. Both the circuits still require a floating capacitor and also perform only a biquadratic filter.

In the design of electronic communication and control systems, sinusoidal quadrature oscillators (QOs) which can provide two periodic waveforms with a phase difference of 90° are necessarily needed. Application tasks of QO are, for example, in quadrature mixers for mixing the analog signal outputs, in phase sensitive detection systems for generating reference signals, and in measurement systems for testing electronic device and circuit characteristics. Up to now, several variable frequency quadrature oscillator circuits have been built employing various types of active elements, such as operational amplifier [24], CCII [25-26], DDCC [27], four terminal floating nullor (FTFN) [28-30], current feedback operational amplifier (CFOA) [31-33], current differencing buffered amplifier (CDBA) [34-35], current differencing transconductance amplifier (CDTA) [36-38], VDTA [39], and voltage differencing buffered amplifier (VDBA) [40]. Note that the above mentioned QO circuits are useful in either voltage [24-27], [31-32], [34-35], [39-40] or current-mode [28-30], [33], [36-38] applications. Some QO configurations were developed in [41-49], where the voltage and current quadrature outputs are generated simultaneously. Several dual-mode QOs make use of one or more active elements [42-44], [47], [49]. Although another set of compact QO realizations using a single active element were proposed in [46], [48], they do not permit non-interactive control of the condition of oscillation (CO) and the frequency of oscillation (ω_{osc}). Besides, the possible realization of the dual-mode multifunction biquad filter is not available with any of the previously mentioned QO realizations.

This contribution led us to the design of the dual-mode multifunction biquad filter and sinusoidal quadrature oscillator which can provide both voltage and current output signals simultaneously. Each of the proposed configurations includes only a single voltage differencing gain amplifier (VDGA) [50], two resistors, and two grounded capacitors. The proposed dual-mode multifunction biquad configuration can orthogonally control of ω_o and Q. With a slight modification of the proposed biquad, a compact dual-mode QO circuit with non-interactive adjustment of CO and ω_{osc} is also obtained. Non-ideal characteristics parasitic element effects on the behavior of the proposed circuits are considered. The working of the circuits is evaluated by simulation results.

2 VDGA Description

The VDGA device is a versatile six-terminal active building block, which is recently introduced in [50]. As a consequence, a variety of VDGA-based analog circuit applications have been developed in technical literature, such as active filters [50]-[51], quadrature sinusoidal oscillators [52]-[53], and capacitance multiplier circuit [54]. Its schematic symbol is shown in Fig.1, where p and n are high-impedance voltage input ports, z+, z- and x are high-impedance current output ports, and w is low-impedance voltage output port. The ideal property of the VDGA device can be characterized as in the following matrix equation:

$$\begin{bmatrix} i_{z+} \\ i_{z-} \\ i_x \\ v_w \end{bmatrix} = \begin{bmatrix} g_{mA} & -g_{mA} & 0 & 0 \\ -g_{mA} & g_{mA} & 0 & 0 \\ 0 & 0 & g_{mB} & 0 \\ 0 & 0 & \beta & 0 \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_{z+} \\ v_x \end{bmatrix}, \quad (1)$$

where g_{mA} and g_{mB} are the transconductance gains, and β is the transfer voltage gain of the VDGA.

Fig.2 shows a CMOS implementation of the VDGA used in this work, and it is derived from the one in [50]. According to [55], it can be realized from Fig.2 that each transconductance g_{mk} ($k = A, B, C$) of the VDGA can be determined by:

$$g_{mk} \cong \left(\frac{g_{1k} g_{2k}}{g_{1k} + g_{2k}} \right) + \left(\frac{g_{3k} g_{4k}}{g_{3k} + g_{4k}} \right), \quad (2)$$

where

$$g_{ik} = \sqrt{K I_{Bk}}, \quad (3)$$

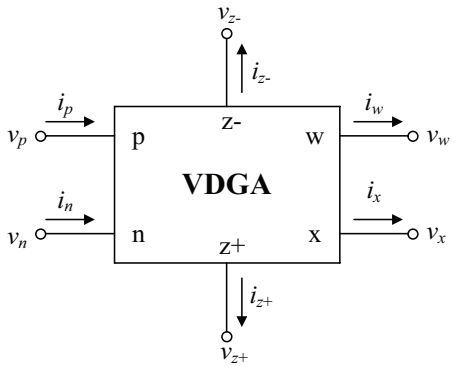

Figure 1: VDGA schematic representation.

for $i = 1, 2, 3, 4$ and the parameter K is the transconductance of the transistor M_{ik}. From equations (2) and (3), the value of g_{mk} can be scaled electronically, since each transconductance g_{ik} is proportional to the square root of the bias current I_{Bk}. Furthermore, a pair of transconductors M_{1B}-M_{9B} and M_{1C}-M_{9C} performs a current-controlled voltage amplifier with the voltage transfer gain $b = v_w/v_{z+} = g_{mB}/g_{mC}$.

3 Proposed dual-mode multifunction biquadratic filter

The proposed dual-mode multifunction biquadratic filter topology is shown in Fig.3. It essentially comprises a single VDGA, two grounded capacitors and two resistors (one of them is grounded). A straightforward analysis with $i_{in} = 0$ provides the three voltage transfer functions as follows:

$$\frac{V_{o1}(s)}{V_{in}(s)} = g_{mA}R_1\left[\frac{\frac{s}{R_1C_1}}{D(s)}\right], \tag{4}$$

$$\frac{V_{o2}(s)}{V_{in}(s)} = \left[\frac{\frac{g_{mA}g_{mB}}{C_1C_2}}{D(s)}\right], \tag{5}$$

and

$$\frac{V_{o3}(s)}{V_{in}(s)} = -\left(g_{mA}R_2\right)\left[\frac{s^2}{D(s)}\right], \tag{6}$$

where

$$D(s) = s^2 + \left(\frac{s}{R_1C_1}\right) + \left(\frac{g_{mA}g_{mB}}{C_1C_2}\right). \tag{7}$$

Therefore, the proposed circuit of Fig.3 provides a non-inverting BP, a non-inverting LP and an inverting HP filter voltage response at the output voltages v_{o1}, v_{o2}, and v_{o3}, respectively. Equations (4)-(7) suggest that the characteristics ω_o and Q of the filter are obtained as :

$$\omega_o = 2\pi f_o = \sqrt{\frac{g_{mA}g_{mB}}{C_1C_2}}, \tag{8}$$

and

$$Q = R_1\sqrt{\frac{g_{mA}g_{mB}C_1}{C_2}}. \tag{9}$$

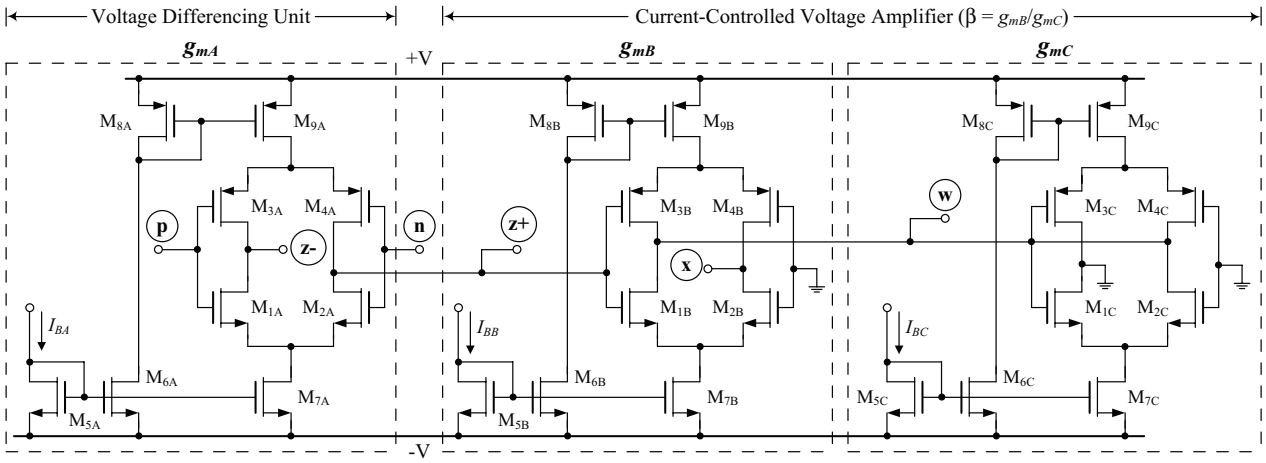

Figure 2: Internal circuit configuration of the CMOS VDGA.

It is important to note that the parameter ω_o is now tunable electronically by adjusting g_{mA} and/or g_{mB}, while the value of the *Q*-factor is adjustable through the value of R_1 without affecting ω_o. In other words, the parameters ω_o and *Q*-factor of the filter are orthogonally controllable.

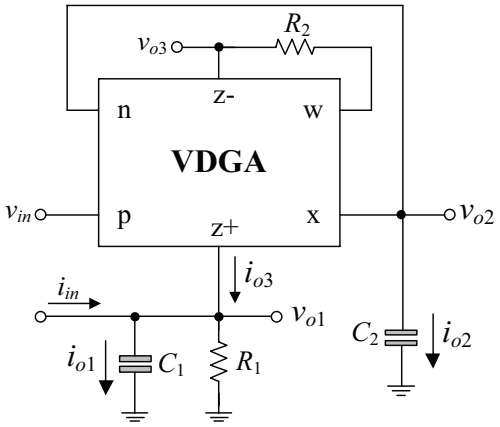

Figure 3: Proposed dual-mode multifunction biquadratic filter.

Considering again the proposed dual-mode frequency filter given in Fig.3, its routine algebraic analysis with $v_{in} = 0$ also reveals the three following current transfer functions:

$$\frac{I_{o1}(s)}{I_{in}(s)} = \left[\frac{s^2}{D(s)}\right], \tag{10}$$

$$\frac{I_{o2}(s)}{I_{in}(s)} = \left(g_{mB}R_1\right)\left[\frac{\frac{s}{R_1C_1}}{D(s)}\right], \tag{11}$$

and

$$\frac{I_{o3}(s)}{I_{in}(s)} = -\left[\frac{\frac{g_{mA}g_{mB}}{C_1C_2}}{D(s)}\right], \quad (\tag{12}$$

where the denominator *D*(*s*) is the same as in equation (7). It is clear from equations (10)-(12) that, by the same structure, current-mode HP, BP, and inverting LP responses are simultaneously obtained at i_{o1}, i_{o2}, and i_{o3}, respectively. For this version, the ω_o and the *Q*-factor are the same as those given in equations (8) and (9).

4 Proposed dual-mode quadrature sinusoidal oscillator

From Fig.3, it is further noted that the dual-mode quadrature sinusoidal oscillator is obtainable by setting i_{in} = 0, and connecting the p-terminal to the w-terminal of the VDGA. The resulting QO circuit is depicted in Fig.4, and its characteristic equation is found as:

$$s^2 + \frac{s}{C_1}\left(\frac{1}{R_1} - g_{mA}\beta\right) + \left(\frac{g_{mA}g_{mB}}{C_1C_2}\right) = 0\,. \tag{13}$$

From the above equation, the CO and ω_{osc} of the realized QO are respectively given by:

$$\frac{1}{R_1} = g_{mA}\beta\,, \tag{14}$$

and

$$\omega_{osc} = 2\pi f_{osc} = \sqrt{\frac{g_{mA}g_{mB}}{C_1C_2}}\,. \tag{15}$$

It is clear from equations (14) and (15) that the CO of the oscillator can be varied independently of ω_{osc} by R_1. This QO provides two voltage outputs and two current outputs, which relate as follows:

$$V_{o1} = \left(\frac{\omega_{osc}C_2}{g_{mB}}\right)e^{j90^\circ}V_{o2}\,, \tag{16}$$

and

$$I_{o1} = \left(\frac{\omega_{osc}C_1}{g_{mB}}\right)e^{j90^\circ}I_{o2}\,. \tag{17}$$

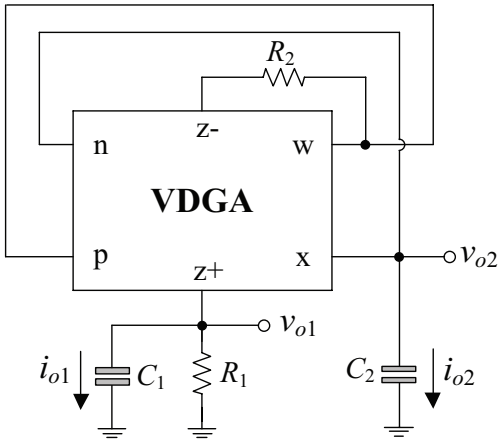

Figure 4: Proposed dual-mode quadrature sinusoidal oscillator.

Equations (16) and (17) show that the two voltage and current outputs are each other shifted in phase by 90°, thereby exhibiting quadrature property to the proposed QO circuit. Moreover, the proposed oscillator also offers versatility by simultaneously providing both quadrature voltage as well as current outputs.

5 Effect of VDGA Non-idealities

5.1 Effect of transfer errors

Taking into consideration the VDGA non-idealities, the characteristic of the practical VDGA can be written as:

$$\begin{bmatrix} i_{z+} \\ i_{z-} \\ i_x \\ v_w \end{bmatrix} = \begin{bmatrix} \alpha_A g_{mA} & -\alpha_A g_{mA} & 0 & 0 \\ -\alpha_A g_{mA} & \alpha_A g_{mA} & 0 & 0 \\ 0 & 0 & \alpha_B g_{mB} & 0 \\ 0 & 0 & \delta\beta & 0 \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_{z+} \\ v_x \end{bmatrix}. \quad (18)$$

In above expression, α_k ($\alpha_k = 1 - \varepsilon_\alpha$) is the transconductance inaccuracy parameter and δ ($\delta = 1 - \varepsilon_\delta$) is the non-ideal voltage transfer gain of the VDGA. These unwanted parameters alter from unity by the transfer errors ε_α ($|\varepsilon_\alpha| << 1$) and ε_δ ($|\varepsilon_\delta| << 1$), respectively.

The proposed dual-mode multifunction biquadratic filter of Fig.3 is re-analyzed using the non-ideal performance relation (18) of VDGA, and the non-ideal ω_o and Q become as follows:

$$\omega_o = 2\pi f_o = \sqrt{\frac{\alpha_A \alpha_B g_{mA} g_{mB}}{C_1 C_2}}, \quad (19)$$

and

$$Q = R_1 \sqrt{\frac{\alpha_A \alpha_B g_{mA} g_{mB} C_1}{C_2}}. \quad (20)$$

Equations (19) and (20) indicate that the transfer errors directly affect the parameters ω_o and Q of the filter. However, since α_A and α_B are typically close to unity, these small deviations can be compensated by slightly re-adjusting the values of g_{mA} and g_{mB} via the bias currents I_{BA} and I_{BB}, respectively.

Similarly, in the non-ideal case, the characteristic equation of the proposed dual-mode QO circuit in Fig.4 can be found as:

$$s^2 + \frac{s}{C_1}\left(\frac{1}{R_1} - \alpha_A \delta g_{mA} \beta\right) + \left(\frac{\alpha_A \alpha_B g_{mA} g_{mB}}{C_1 C_2}\right) = 0, \quad (21)$$

where the parameters CO and ω_{osc} of the oscillator for this case are modified as:

$$\frac{1}{R_1} = \alpha_A \delta g_{mA} \beta, \quad (22)$$

and

$$\omega_{osc} = \sqrt{\frac{\alpha_A \alpha_B g_{mA} g_{mB}}{C_1 C_2}}. \quad (23)$$

The CO and ω_{osc} of the oscillator are deviated from the ideal case by the non-ideal transfer gains. In the same manner, because the voltage transfer gain β is proportional to g_{mB}/g_{mC}, the transconductance g_{mC} is adjustable to minimize the influence of α_A and δ on the CO. Also, note from (23) that the slight ω_{osc} deviation can be overcome by re-tuning g_{mA} and g_{mB}.

5.2 Effect of parasitic elements

In practice, a parasitic problem should be taken into count to determine the effects of the VDGA parasitic impedances on the proposed circuits. Fig.5 displays a sophisticated equivalent model behavior that represents the practical VDGA. In Fig.5, the dashed line encircles the practical VDGA, while the continuous line denotes the ideal VDGA with various parasitic elements at its terminals. As can be seen, there are parasitic parallel resistances and capacitances from terminals p, n, z+ and z- to ground [(R_p//C_p), (R_n//C_n), (R_{z+}//C_{z+}) and R_{z-}//C_{z-})], and a parasitic serial resistance (R_w) at the terminal w. Therefore, by applying the practical model of the VDGA to the proposed dual-mode multifunction filter in Fig.3 and assuming the condition $R_2 >> R_w$, the modified ω_o and Q can be expressed as:

$$\omega_o = \sqrt{\frac{g_{mA} g_{mB} + \left(\frac{1}{R_1' R_x'}\right)}{C_1' C_2'}}, \quad (24)$$

and

$$Q = \left[\frac{R_1' R_x'}{R_1' C_1' + R_x' C_2'}\right] \sqrt{\left[g_{mA} g_{mB} + \left(\frac{1}{R_1' R_x'}\right)\right] C_1' C_2'}. \quad (25)$$

where $R_1' = R_1//R_{z+}$, $R_x' = R_x//R_n$, $C_1' = C_1 + C_{z+}$ and $C_2' = C_2 + C_x + C_n$.

In a similar way, accounting for the VDGA parasitic elements given in Fig.5, the CO and ω_{osc} of the proposed dual-mode sinusoidal QO in Fig.4 can be derived as:

$$\left(\frac{1}{R_1'} + \frac{C_1'}{R_x' C_2'}\right) = \beta g_{mA}, \quad (26)$$

and

$$\omega_{osc} = \sqrt{\frac{g_{mA}g_{mB} + \left(\frac{1}{R_1' R_x'}\right)}{C_1' C_2'}}. \quad (27)$$

From inspection of equations (24)-(27), it is possible to reduce the VDGA parasitic influences on the proposed circuits by taking the following conditions in the design: $R_1 << R_{z+}$, $R_x << R_n$, $C_1 >> C_{z+}$ and $C_2 >> (C_x + C_n)$.

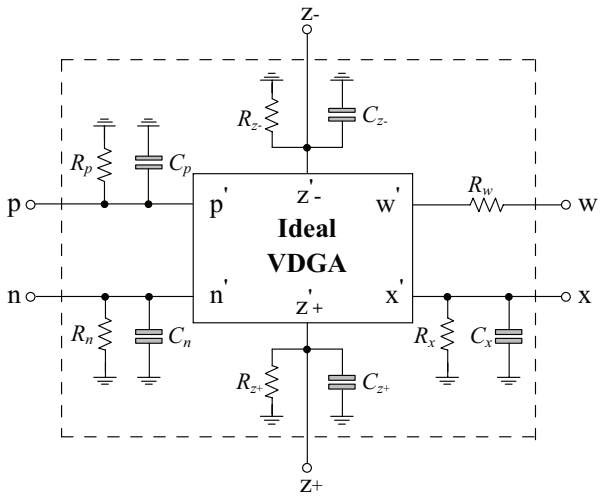

Figure 5: Practical VDGA model

6 Simulation results and discussions

The correct operation of the proposed dual-mode multifunction filter and QO topologies in Fig. 3 and 4 is assessed through PSPICE simulation results. For this purpose, the transistor models of the TSMC 0.25-μm CMOS process parameters have been used. The CMOS VDGA in Fig.2 is simulated under DC supply voltages of ±1V. The values of transistor aspect ratios (W/L) are provided in Table 1.

Table 1: Values of transistor aspect ratios (W/L) of the VDGA circuit in Fig.2.

Transistor	W (μm)	L (μm)
M_{1k} - M_{2k}	15	0.25
M_{3k} - M_{4k}	23	0.25
M_{5k} - M_{7k}	4.5	0.25
M_{8k} - M_{9k}	6	0.25

6.1 Simulation results of the proposed dual-mode multifunction biquadratic filter

For the proposed dual-mode multifunction biquadratic filter in Fig.3, the active and passive components are taken as: $g_{mk} \cong 1$ mA/V ($I_{Bk} = 100$ μA), $R_1 = R_2 = 1$ kΩ and $C_1 = C_2 = 100$ pF which result in $f_o \cong 1.59$ MHz and $Q \cong 1$. The simulated and ideal frequency responses for the voltage and current gains are represented in Fig.6. In Fig.7, the input and output waveforms for the proposed BP filters at 1.59-MHz sinusoidal input signals are also shown. Total harmonic distortions (THDs) are less than 4% and 1.6% for the voltage-mode and current-mode BP filters, respectively. In addition to the simulation result, this filter has the total power consumption of about 1.49 mW. Next, the large-signal behavior of the proposed filter is also evaluated by applying a sinusoidal input signal of 1.59 MHz. The BP output responses are found to demonstrate the THD variations of input signal amplitude as shown in Fig.8.

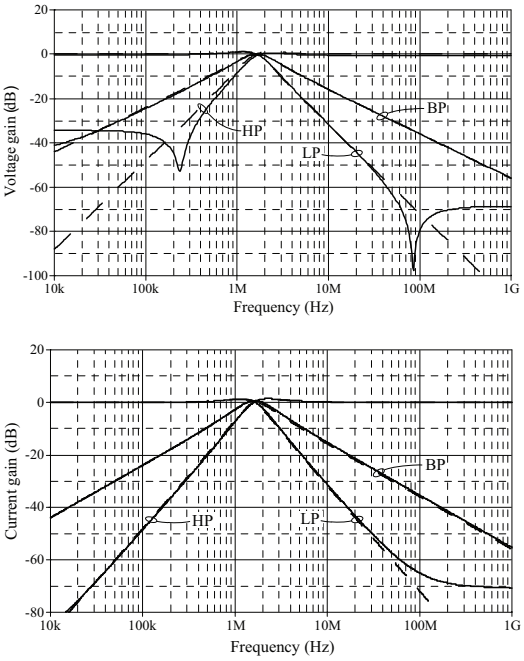

Figure 6: Simulated and ideal frequency responses of the proposed dual-mode multifunction filter in Fig.3 (solid line: simulated response, dashed line: ideal response). (a) voltage-mode (b) current-mode.

To test the adjustability of *Q*-factor without changing the f_o-value, the following circuit components are selected as: $g_{mk} = 1$ mA/V, $C_1 = C_2 = 100$ pF, with four different values of R_1 namely 0.5 kΩ, 1 kΩ, 2 kΩ, and 10 kΩ. The four BP voltage responses are illustrated in Fig.9, which accordingly shows the orthogonal variability of *Q*-factor. Furthermore, by keeping the product of $g_{m1}R_1$ constant, and tuning the value of g_{m1}/R_1 only, an independent tunability of f_o can be obtained as shown in

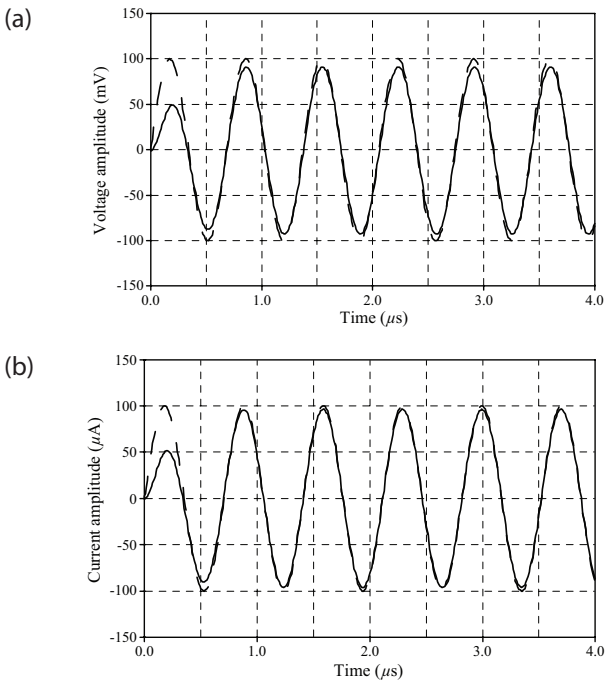

Figure 7: Input (dashed line) and output (solid line) waveforms of the BP filter for 1.59-MHz sinusoidal input signal. (a) voltage-mode (solid line: v_{o1}, dashed line: v_{in}), (b) current-mode (solid line: i_{o2}, dashed line: i_{in})

Fig.10. The component values for simulating the realized BP filter with different f_o and their resulting characteristics are given in Table 2.

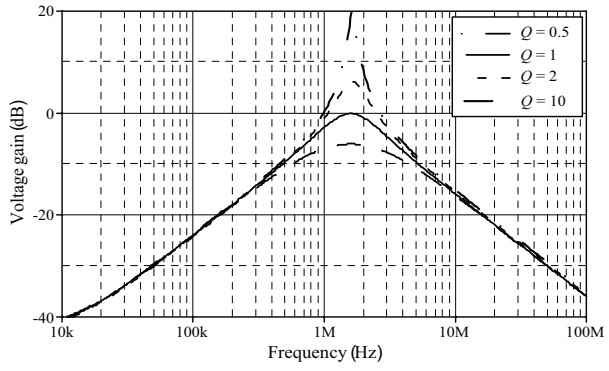

Figure 9: Gain-frequency characteristics with Q = 0.5, 1, 2, and 10 of the proposed voltage-mode BP filter in Fig.3.

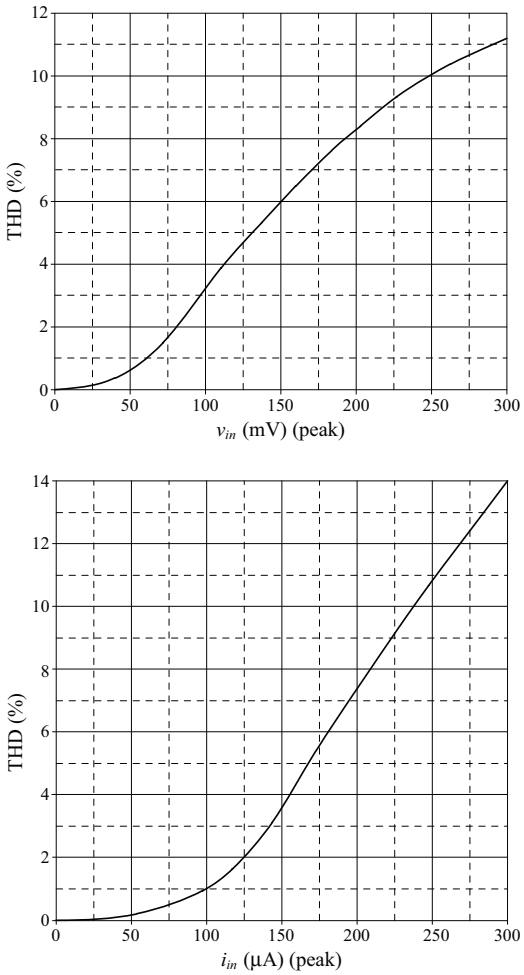

Figure 8: THD variations of the BP response versus input signal amplitude at 1.59 MHz. (a) voltage-mode (b) current-mode.

To evaluate the mismatch and process variation effects, Monte Carlo (MC) analysis has been performed for 100 iterations. MC simulation results showing deviations in filter responses for 5% changes in all passive elements (R_1, R_2, C_1, and C_2) and transconductances (g_{mk}) are illustrated in Fig.11(a) and 11(b), respectively. Temperature variation impacts on the filter responses are also studied for observed range 0°C to 100°C. The simulation results of the gain-frequency characteristics with a variation in operating temperature are drawn in Fig.12. From the graph, the value of f_o varies from 1.69 MHz at

Table 2: Component values for implementing the proposed BP filter in Fig.3 with independent adjustability of f_o.

g_{mk} (mA/V)	I_{Bk} (µA)	R_1 (kΩ)	$g_{mk}R_1$	g_{mk}/R_1	f_o (MHz)		Q
					Simulated	Theory	
0.63	40	1.6	1	0.40E-06	1.01	0.98	1
1.00	100	1.0	1	1.00E-06	1.59	1.54	1
1.35	180	0.74	1	1.82E-06	2.15	2.05	1

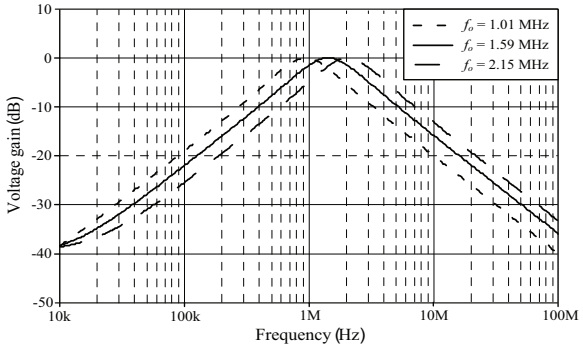

Figure 10: Gain-frequency characteristics with independent adjustability of f_o of the proposed voltage-mode BP filter in Fig.3.

0°C to 1.35 MHz at 100°C with a maximum deviation of 17%. It may also be observed that the f_o-value shifts to the lower frequencies with an increase in temperature. This is due to the fact that the transconductance decreases with increases in temperature due to decrease in mobility. This shifting in f_o can easily be compensated through bias current variation, or the PTAT (Proportional to Absolute Temperature) current reference can be used as bias current sources to compensate for the temperature behavior of the proposed circuits.

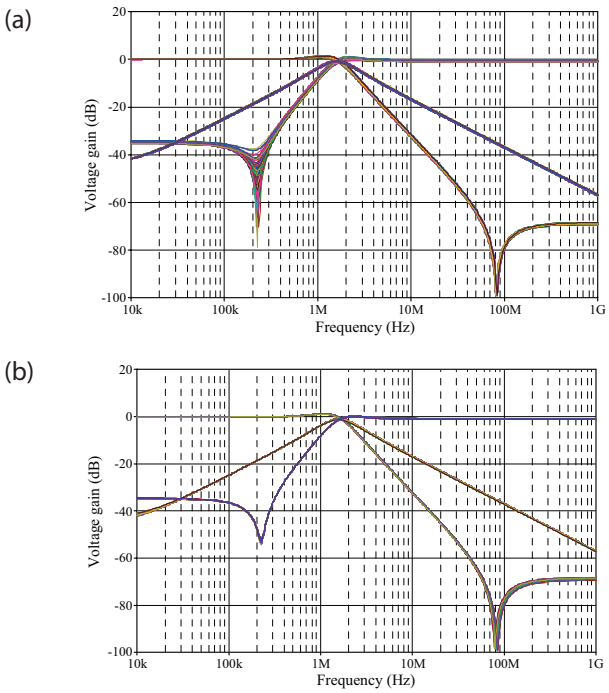

Figure 11: Monte Carlo analyses with 100 iterations, showing variations in LP, BP and HP filter responses, due to 5% changes in (a) all resistors and capacitors (b) all transconductances.

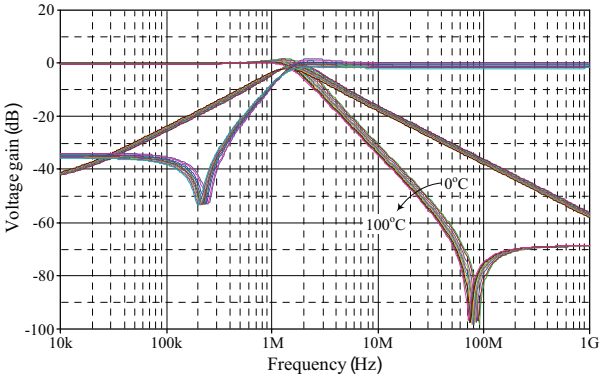

Figure 12: Gain-frequency characteristics with a variation in temperature from 0°C to 100°C.

6.2 Simulation results of the proposed dual-mode quadrature sinusoidal oscillator

With the same above designed values, the proposed dual-mode QO circuit of Fig.4 has been simulated for a frequency of oscillation of f_{osc} = 1.59 MHz. Simulation results of the voltage and current quadrature output responses are shown in Fig.13 and 14, respectively. Fig.13(a) indicates the two quadrature voltage outputs difference in phase by 88°, while Fig.14(a) shows 91° phase-shifted quadrature current outputs. The observed THD for both voltage and current outputs are around 3.76% and 3.73%, respectively. The Lissajous patterns for the two voltage and two current outputs are further depicted through Fig.15(a) and 15(b), respectively. It is observed that the resultants produce circles around the origin with no tilt in axis illustrating the quadrature property of the proposed oscillator circuit.

7 Conclusions

The paper proposes compact circuit configurations for realizing dual-mode (i.e. both voltage-mode and current- mode) multifunction biquadratic filter and quadrature sinusoidal oscillator. Each of the proposed circuit configurations requires a single VDGA, two grounded capacitors, and two resistors (one of them is grounded). The proposed filter can realize simultaneously the three standard biquadratic filtering functions, i.e. LP, BP, and HP ones, with both voltage and current output responses. It has also capable of independent control of ω_o and Q-factor. Another notable advantage of the proposed circuit is that it can also be used as a sinusoidal quadrature oscillator to provide two quadrature voltage outputs and two quadrature current outputs simultaneously. The oscillation condition and the oscillation frequency of the proposed dual-mode QO are orthogonally controllable by separate bias currents.

The effect of non-idealities influences of the VDGA on the circuit functionality has been studied, and simulation results using PSPICE with TSMC 0.25-μm CMOS technology have also been included to validate the functionality of the proposed circuits in both frequency filter and oscillator mode.

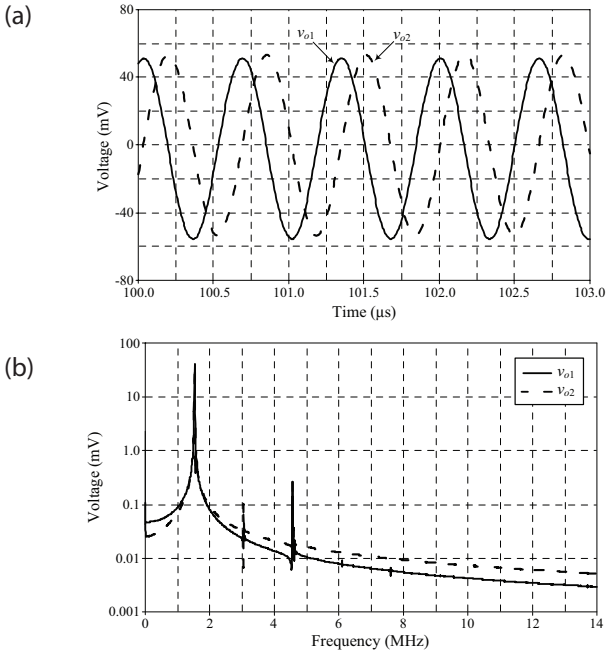

Figure 13: Simulated voltage output responses. (a) time-domain responses (b) frequency spectrum.

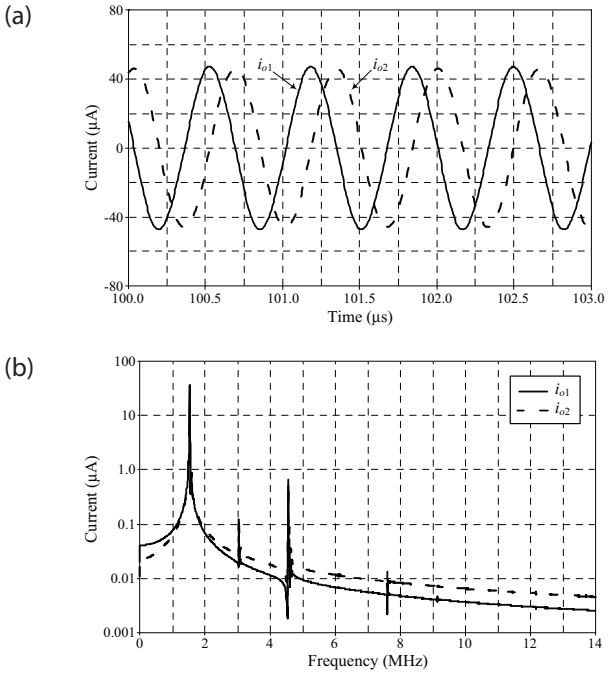

Figure 14: Simulated current output responses. (a) time-domain responses (b) frequency spectrum.

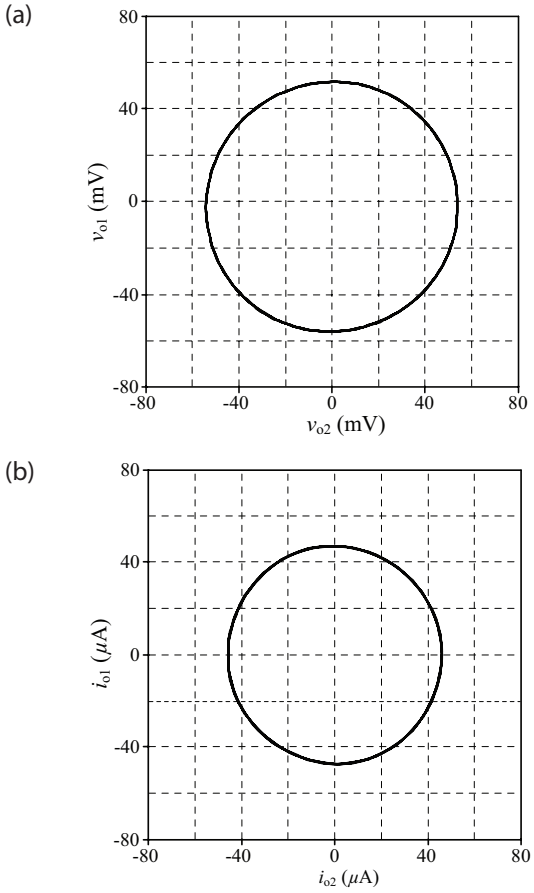

Figure 15: Lissajous patterns illustrating the quadrature property. (a) voltage-mode (b) current-mode.

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9 Conflict of Interest

The authors confirm that this article content has no conflict of interest.

10 References

1. O. Cicekoglu, N. Tarim, H. Kuntman, "Wide dynamic range high output impedance current-mode multifunction filters with dual-output current conveyors", *Int. J. Electron. Commun. (AEU)*, vol.56, no.1, pp.55-60, 2002, https://doi.org/10.1078/1434-8411-54100073.

2. M. A. Ibrahim, S. Minaei, H. Kuntman, "A 22.5 MHz current-mode KHN biquad using differential voltage current conveyor and grounded passive element", *Int. J. Electron. Commun. (AEU)*, vol.59, pp.311-318, 2005, https://dx.doi.org/10.1016/j.aeue.2004.11.027.
3. J. W. Horng, "Voltage-mode multifunction biquadratic filter employing single DVCC", *Int. J. Electron.*, vol.99, no.2, pp.153-162, 2012, https://doi.org/10.1080/00207217.2011.623268 .
4. J. W. Horng, W. Y. Chiu, and H. Y. Wei, "Voltage-mode highpass, bandpass and lowpass filters using two DDCCs", *Int. J. Electron..*, vol.91, no.8, pp.461-464, 2004, https://doi.org/10.1080/00207210412331294603
5. J. W. Horng, J. R. Lay, C. W. Chang, M. H. Lee, "High input impedance voltage-mode multifunction filters using plus-type CCIIs", *Electron. Lett.*, vol. 33, no. 6, pp. 472-473, 1997, https://doi.org/10.1049/el:19970297.
6. C. M. Chang, M. J. Lee, "Voltage-mode multifunction filter with single input and three outputs using two compound current conveyors", *IEEE Trans. Circuits Syst.-I: Fundamental Theory and Applications*, vol. 46, no. 11, pp. 1364-1365, 1999, https://doi.org/10.1109/81.802827.
7. F. Yucel, E. Yuce, "A new CCII based voltage-mode multifunctional filter with reduced number of active and passive elements", *J. Circuits Syst. Comp.*, vol.24, no. 4, 1550047 (11 pages), 2015, https://doi.org/10.1142/s0218126615500474.
8. S. Ozcan, O. Cicekoglu, and H. Kuntman, "Multi-input single-output filter with reduced number of passive elements employing single current conveyor", *Comp. Electri. Eng.*, vol.29, pp.45-53, 2003, https://doi.org/10.1016/s0045-7906(01)00024-6 .
9. H. Y. Wang, C. T. Lee, "Versatile insensitive current-mode universal biquad implementation using current conveyors", *IEEE Trans. Circuits Syst.-II: Analog and Digital Signal Processing*, vol.48, no.4, pp.409-413, 2001, https://doi.org/10.1109/82.933806.
10. S. Maheshwari, "High performance voltage-mode multifunction filter with minimum component count", *WSEAS Trans. Electron.*, vol.5, pp.244-249, 2008.
11. E. Yuce, "Voltage-mode multifunction filters employing a single DVCC and grounded capacitors", *IEEE Trans. Instrum. Meas.*, vol. 58, no. 7, pp.2216-2221, 2009, https://doi.org/10.1109/tim.2009.2013671.
12. W. Tangsrirat, and O. Channumsin, "High-input impedance voltage-mode multifunction filter using a single DDCCTA and grounded passive elements", *Radioengineering*, vol.20, no.4, pp.905-910, 2011.
13. M. Minarcik, and K. Vrba, "Single-input six-output voltage-mode filter using universal voltage conveyors", *IEICE Trans. Fundamentals.*, vol.E91-A, no.8, pp.2035-2037, 2008, https://doi.org/10.1093/ietfec/e91-a.8.2035.
14. H. Alpaslan, and E. Yuce, "Current-mode biquadratic universal filter design with two terminal unity gain cells", *Radioengineering*, vol.21, no.1, pp.304-311, 2012.
15. S. S. Gupta, and R. Senani, "New voltage-mode/current- mode universal biquad filter using unity-gain cells", *Int. J. Electron.*, vol.93, no.11, pp.769-775, 2006, https://doi.org/10.1080/00207210600711622.
16. H. P. Chen, and P. L. Chu, "Versatile universal electronically tunable current-mode filter using CC-CIIs", *IEICE Electronics Express*, vol.6, no.2, pp.122-128, 2009, https://doi.org/10.1587/elex.6.122.
17. E. Yuce, A. Kircay, and S. Tokat, "Universal resistorless current-mode filters employing CCCIIs", *Int. J. Circ. Theor. Appl.*, vol.36, no.5-6, pp.739-755, 2008, https://doi.org/10.1002/cta.455.
18. W. Chunhua, A. U. Keskin, L. Yang, Z. Qiujing, and D. Sichun, "Minimum configuration insensitive multifunctional current-mode biquad using current conveyors and all-grounded passive components", *Radioengineering*, vol.19, no.1, pp.178-184, 2010.
19. O. Channumsin, and W. Tangsrirat, "Dual-mode multifunction filter using VDGAs", *Proc. 15th Int. Conf. Electri./Electron. Comput. Telecommun. Inform. Tech. (ECTI-CON 2018),* Chiang Rai, Thailand, July 18-21, pp. 90-93, 2018.
20. J. Satansup, T. Pukkalanun, and W. Tangsrirat, "Electronically tunable single-input five-output voltage-mode universal filter using VDTAs and grounded passive elements," *Circuits Syst. Signal Process*, vol. 32, no. 3, pp. 945–957, 2013, https://doi.org/10.1007/s00034-012-9492-0.
21. J. Satansup and W. Tangsrirat, "Compact VDTA-based current-mode electronically tunable universal filters using grounded capacitors,"*Microelectron. J.*, vol. 45, no. 6, pp. 613–618, 2014, https://doi.org/10.1016/j.mejo.2014.04.008.
22. N. Singhal, R. Pandey, and N. Pandey, "Dual mode biquadratic filter using single VDTA," *Int. J. Electri. Electron. Eng.*, vol. 6, pp.134–139, 2014.
23. R. Pandey, N. Pandey, and N. Singhal, "Single VDTA based dual mode single input multioutput biquad filter", *J. Engineering*, vol. 2016, Article ID 1674343, 10 pages, 2016, http://dx.doi.org/10.1155/2016/1674343.

24. J. W. Horng, "Quadrature oscillators using operational amplifiers", *Active and Passive Electron. Comp.*, vol. 2011, Article ID 320367, 4 pages, 2011, https://doi.org/10.1155/2011/320367.
25 N. Minhaj, "Current conveyor-based voltage-mode two-phase and four-phase quadrature", *Int. J. Electron.*, vol.94, no.7, pp.663-669, 2007, https://doi.org/10.1080/00207210701405870.
26. J. W. Horong, C. L. hou, C. M. Chang, W. Y. Chung, H. W. Tang, and Y. H. Wen, "Quadrature oscillators using CCIIs", *Int. J. Electron.*, vol.92, no.1, pp.21-31, 2005, https://doi.org/10.1080/00207210412331332899
27. M. Kumngern, and K. Dejhan, "DDCC-based quadrature oscillator with grounded capacitors and resistors", *Active and Passive Electron. Comp.*, vol.2009, Article ID 987304, 4 pages, 2009, https://doi.org/10.1155/2009/987304.
28. S.I. Liu, and Y.H. Liao, "Current mode quadrature sinusoidal oscillator using single FTFN", *Int. J. Electron.*, vol.81, no.2, pp.171-175, 1996, https://doi.org/10.1080/002072196136832.
29. D. R. Bhaskar, R. Senani, "New FTFN-based grounded-capacitor SRCO with explicit current-mode output and reduced number of resistors", *Int. J. Electron. Commun. (AEU)*, vol.59, no.1, pp.48-51, 2005, https://doi.org/10.1016/j.aeue.2004.11.029.
30. U. Cam, A. Toker, O. Cicekoglu, H. Kuntman, "Current-mode high output impedance sinusoidal oscillator configuration employing single FTFN", *Analog Integr. Circ. Sig. Process.*, vol.24, no.3, pp.231-238, 2000, https://doi.org/10.1023/A:1008365726144.
31. A. M. Soliman, "Current feedback operational amplifier based oscillators", *Analog Integr. Circ. Sig. Process.*, vol.23, no.1, pp.45-55, 2000, https://doi.org/10.1023/A:1008391606459.
32. W. Tangsrirat, W. Surakampontorn, "Single-resistance-controlled quadrature oscillator and universal biquad filter using CFOAs", *Int. J. Electron. Commun. (AEU)*, vol.63, no.12, pp.1080-1086, 2009, https://doi.org/10.1016/j.aeue.2008.08.006.
33. A. Lahiri, W. Jaikla, M. Siripruchyanun, "First CFOA-based explicit-current-output quadrature sinusoidal oscillators using grounded capacitors", *Int. J. Electron.*, vol.100, no.2, pp.259-273, 2013, https://doi.org/10.1080/00207217.2012.692632.
34. A.U. Keskin, "Voltage-mode high-Q band-pass filters and oscillators employing single CDBA and minimum number of components", *Int. J. Electron.*, vol.92, no.8, pp.479-487, 2005, https://doi.org/10.1080/00207210500168626.
35. W. Tangsrirat, D. Prasertsom, T. Piyatat, W. Surakampontorn, "Single-resistance-controlled quadrature oscillator using current differencing buffered amplifiers", *Int. J. Electron.*, vol.95, no.11, pp. 1119-1126, 2008, https://doi.org/10.1080/00207210802387676.
36. W. Tangsrirat, W. Tanjaroen, "Current-mode quadrature oscillator with independent control of oscillation frequency and condition using CDTAs", *Indian J. Pure & Appl. Phys.*, vol.48, no.5, pp.363-366, 2010.
37. J. Jin, C. Wang, "Single CDTA-based current-mode quadrature oscillator", *Int. J. Electron. Commun. (AEU)*, vol.66, no.11, pp.933-936, 2012, https://doi.org/10.1016/j.aeue.2012.03.018.
38. J. Jin, C. Wang, "CDTA-based electronically tunable current-mode quadrature oscillator", *Int. J. Electron.*, vol.101, no.8, pp. 1086-1095, 2014, https://doi.org/10.1080/00207217.2013.805394.
39. K. Banerjee, D. Singh, S. K. Paul, "Single VDTA based resistorless quadrature oscillator", *Analog Integr. Circ. Sig. Process.*, vol.100, no.2, pp.495-500, 2019, https://doi.org/10.1007/s10470-019-01480-4.
40. A. Yesil, F. Kacar, and K. Gurkan, "Design and experimental evaluation of quadrature oscillator employing single FB-VDBA", *J. Electri. Eng.*, vol.67, no.2, pp.136-142, 2016, https://doi.org/10.1515/jee-2016-0019.
41. J. W. Horng, C. L. Hou, C. M. Chang, H. P. Chou, C. T. Lin, and Y. H. Wen, "Quadrature oscillators with grounded capacitors and resistors using FDCCIIs", *ETRI J.*, vol. 28 no.4, pp.486-494, 2006, https://doi.org/10.4218/etrij.06.0105.0181.
42. S. Maheshwari, I. A. Khan, "Novel single resistor controlled quadrature oscillator using two CDBAs", *J. Active Passive Devices*, vol.2, pp.137-142, 2007.
43. A. Lahiri, "Novel voltage/current-mode quadrature oscillator using current differencing transconductance amplifier", *Analog Integr. Circ. Sig. Process.*, vol.61, no.2, pp.199-203, 2009, https://doi.org/10.1007/s10470-009-9291-0.
44. S. Maheshwari, "Quadrature oscillator using grounded components with current and voltage outputs", *IET Circuits Devices Syst.*, vol.3, no.4, pp.153-160, 2009, https://doi.org/10.1049/iet-cds.2009.0072.
45. A. Lahiri, "Explicit-current-output quadrature oscillator using second-generation current conveyor transconductance amplifier", *Radioengineering*, vol.18, no.4, pp.522-526, 2009.
46. W. Tangsrirat, "Dual-mode sinusoidal quadrature oscillator with single CCTA and grounded capacitors", *Informacije MIDEM*, vol.46, no.3, pp.130-135, 2016.
47. M. Srivastaya, D. Prasad, "VDCC based dual-mode sinusoidal quadrature oscillator with outputs at appropriate impedance", *Theoretical and Applied Electrical Eng.*, vol.14, no.2, pp.168-177, 2016, https://doi.org/10.15598/aeee.v14i2.1611.

48. W. Tangsrirat, "Compact quadrature oscillator with voltage and current outputs using only single VDTA and grounded capacitors", *Indian J. Pure & Appl. Phys.*, vol.55, no.4, pp.254-260, 2017.
49. A. Yesil, F. Kacar, "Current and voltage mode quadrature oscillator based on voltage differencing buffered amplifier", *Electrica*, vol.18, no.1, pp.6-12, 2018, https://doi.org/10.5152/iujeee.2018.1802.
50. J. Satansup**,** W. Tangsrirat, "CMOS realization of voltage differencing gain amplifier (VDGA) and its application to biquad filter", *Indian J. Eng. Mater. Sci.*, vol.20, no.6, pp.457-464, 2013.
51. Z. G. Cam Taskiran, H. Sedef and F. Anday, "Voltage differencing gain amplifier-based Nth-order low-pass voltage-mode filter", *J. Circuit. Syst. Comp.*, vol.27, no.6, 2018, https://doi.org/10.1142/S0218126618500895.
52. O. Channumsin and W. Tangsrirat, "Compact electronically tunable quadrature oscillator using single voltage differencing gain amplifier (VDGA) and all grounded passive elements", *Turk. J. Elec. Eng. & Comp. Sci.*, vol.25, pp.2686-2695, 2017, https://doi.org/10.3906/elk-1607-1.
53. O. Channumsin, W. Tangsrirat, "Voltage differencing gain amplifier-based sinusoidal quadrature oscillator using only two grounded capacitors", *Recent Advances in Electrical & Electronic Engineering*, vol.12, no.5 , pp.439-444, 2019, https://doi.org/10.2174/2352096512666181219121941
54. W. Tangsrirat, O. Channumsin, and J. Pimpol, "Electronically adjustable capacitance multiplier circuit with a single voltage differencing gain amplifier (VDGA)", *Informacije MIDEM*, vol.49, no.4, pp.211-217, 2019, https://doi.org/10.33180/infmidem2019.403.
55. A. F. Arbel, L. Goldminz, "Output stage for current-mode feedback amplifiers, theory and applications", *Analog Integr. Circ. Sig. Process.*, vol.2, no.3, pp.243–255, 1992, https://doi.org/10.1007/bf00276637.

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DTMOS Based High Bandwidth Four-Quadrant Analog Multiplier

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Abstract: Analog multiplication circuits are very important blocks widely used in analog signal processing applications. In analog multiplication circuits, low power consumption is expected with wide bandwidth, low nonlinearity and high input range according to the supply voltage. In this work, folded Gilbert cell structure was resized using dynamic threshold MOS (DTMOS) transistors. The proposed circuit is laid out with 491.4 μm2 chip area. Post layout simulations show that the proposed circuit has high bandwidth (1.2 GHz), low supply voltage (0.2 V), and low power consumption (44.6 μW). In addition, the proposed circuit is examined for temperature variation, total harmonic distortion, intermodulation products and Monte Carlo analysis of the dimensioning of the circuit. The post layout results show that the proposed circuit has promising performance against its counterparts in the literature.

Keywords: Four-quadrant; analog multiplier; DTMOS.

Štiri-kvadranten širokopasovni množilnik na osnovi DTMOS

Izvleček: Analogna množilna vezja imajo zelo pomemben del pri analognem procesiranju signalov. Od njih se pričakuje nizka poraba, velika pasovna širina, nizka nelinearnost, in visoko vhodno območje glede na napajalno napetost. V tem delu je bila uporabljena povečana Gilbertova struktura z uporabo tranzistorjev z dinamičnim pragom (DTMOS). Vezje je narejeno na površini 491.4 μm2. Simulacije so pokazale, da je pasovna širina vezja 1.2 GHz, napajalna napetost 0.2 V in poraba 44.6 μW. Dodatno je bil raziskan vpliv temperature, skupna harmonična distorzija, intermodulacija in Monte Carlo analiza.

Ključne besede: štiri kvadranten; analogni množilnik; DTMOS.

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1 Introduction

Analog multipliers that are commonly used in analog signal processing applications such as analog and frequency modulation, phase locked-loop, phase shifting and detection, frequency converter, automatic control, artificial neural networks, Neuro-fuzzy systems. The analog multipliers are electronic circuits with two input ports and one output port. Output signal of the multiplier is defined by the transfer function $z = K \times x \times y$, where x and y are two continuous input signals and K is a constant value appropriately dimensioned. Analog multipliers are classified according to the polarization of their inputs. The classifications are as follows: i) One quadrant [1] whose inputs are non-polarized, ii) Two quadrant [2], [3] whose one of the inputs are polarized, iii) Polarized both inputs are called four quadrant [4–7]. In addition, the multipliers are divided into two types: current mode [8], [9] and voltage mode [4–7].

The first bipolar analog multiplier known as the Gilbert cell was published in 1968 by Barrie Gilbert [10]. Since analog multipliers based on CMOS technology have been classified (i) according to the form of the input signal; current or voltage mode (ii) with regard to the operating region of the transistors; weak inversion [8], [11], [12] strong inversion [13], [14], saturation region [15] and linear region [16], [17]. Although the input signal range and bandwidth of analog multipliers operating in the weak inversion region are quite narrow, they are frequently used in low power consumption applications. Analog multipliers operating in the saturation region have wide bandwidth, dynamic input range and high speed. In multipliers operating in the strong inversion region, the error caused by the body effect causes mismatch in the threshold voltage.

In recent years, the increasing popularity of portable devices such as smartphones and tablet computers has brought restrictions on battery capacity, weight and size. It has created serious restrictions on power consumption and led to the emergence of low-power and high-performance circuitry techniques. Thus, several methods have been suggested to concentrate the power consumption of the analog multipliers. Some of these techniques are as follows: weak-inversion [8], [11], [12], [18], subthreshold MOSFETs [19–23], bulk driven [11], [12], DTMOS [24][25], and floating gate MOSs [5], [26], [27]. It is seen that transistor multipliers working in weak inversion region have poor dynamic range, limited voltage swing and low bandwidth. In the study of Soltany and Razai [12], although the power consumption was reduced by bulk-input, it was seen that the speed and output voltage range were also very low. Even though, analog multipliers designed with transistors operating in the subthreshold region [19–23] show low power consumption, but the dynamic range and operating speed of the multiplier are low. In the study, using DTMOS transistor [24], low power consumption and full-scale input voltage were provided, but -3dB bandwidth was obtained as 1.11 MHz. In articles [26] and [27] a low power consumption analog multiplication circuit was implemented using FGMOS, but their bandwidth was specified as 10 MHz and 200 MHz, respectively. In the study of Keles and Kuntman [5], FGMOS technique has been achieved with high bandwidth such as 1.5 GHz, but there is no information about power consumption here.

In this article, a low power, wide bandwidth four-quadrant analog multiplier by using DTMOS based folded Gilbert cell is proposed. The simulation results are given using Cadence Environment using 0.18 µm TSMC CMOS technology under a supply voltage of 0.2 V.

Gilbert cell is one of the first studies of analog multiplication circuits proposed by Barrie Gilbert in 1968 [10]. Gilbert cell is popular in bipolar integrated circuits (IC) due to its wide dynamic range and bandwidth. In this study, the analog multiplier was realized with the folded Gilbert cell by using DTMOS technology and the bandwidth is obtained pretty much wider.

Due to undesirable behavior in nonlinearity, the range of the input signal is limited to half or generally much less of the supply voltage. In this study, full-scale supply voltage can be used for an input signal range [26]. In order to demonstrate its technological strength, Monte Carlo analyses were performed in AC form with 10% mismatch of process parameters (t_{ox} and V_{TH}) and transistor widths.

The rest of the paper is arranged as follows: Information on the DTMOS structure and the proposed multiplication circuit structure as well as equations are given in Section 2. AC/DC characteristics, intermodulation products, temperature sensitivity, total harmonic distortion and Monte Carlo analysis are given in Section 3. Finally, Section 4 concludes the paper.

2 DTMOS based four-quadrant analog multiplier

Today, the increase in the use of portable devices has brought limits on battery capacity, weight and size. These restrictions have contributed to an increase in studies on low power and high performance circuit techniques.

The need to reduce power consumption has led to a reduction in the supply voltage of the circuits. Excessive lowering of the supply voltage causes standby power and speed problems of the memory elements. MOSFET with dynamic threshold voltage was proposed by Assaderaghi et al. in 1994 to meet low voltage performance requirements [28]. The topology and symbol of the DTMOS obtained by connecting the body and gate of a MOSFET are given in Figure 1.

The threshold voltage of DTMOS is as follows:

$$V_{th} = V_{t0} + \gamma\left(\sqrt{|2\phi_F| + V_{SB}} - \sqrt{2\phi_F}\right) \quad (1)$$

V_{th} is threshold voltage, V_{t0} is the zero body bias threshold voltage. γ is the body effect coefficient and it depends on the gate oxide capacitance, silicon permittivity and substrate doping ϕ_F. is the Fermi potential. V_{SB} is the source to body voltage. The threshold voltage

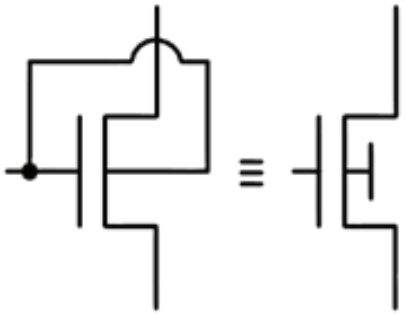

Figure 1: Topology and symbol of DTMOS.

equation is written for a long channel NMOS transistor where drain-induced barrier lowering (DIBL) effect is neglected. The proposed DTMOS has a high threshold voltage at zero bias and low threshold voltage when the gate-source voltage is equal to supply voltage($V_{gs} = V_{dd}$)[29].

By reduction of threshold voltage, inversion charge (Q_N) is increased; so, larger inversion charge leads to a higher current drive in DTMOS in comparison to the regular MOSFETs

MOS transistor's drain current is given by below Eq. (2).

$$I_D = I_S\left(\frac{W}{L}\right)exp\left(q\frac{V_{GS}-V_{TH}}{nkT}\right)\left[1-exp\left(-q\frac{V_{DS}}{kT}\right)\right] \quad (2)$$

According to the equation the transistor will saturate in weak inversion when $V_{DS} \geq 3kT/q$ [17]. Under some limitations, bulk-DTMOS technique can be applied to cheap standard CMOS fabrication process without additional processing steps. The transconductance g_m is described by

$$g_m = q\frac{I_D}{nkT} \quad (3)$$

DTMOS reduces the junction width and consequently the depletion region charge density, which contributes to a decrease in the threshold voltage. In case of reverse bias, the depletion region width increases, and the increase in the body charges causes the threshold voltage to increase. DTMOS-based circuits in case of forward biasing, the threshold voltage will be low. When the transistor is turned off, the V_{TH} becomes high, resulting the leakage current will also be low. Thus, the threshold voltage is changed dynamically with respect to the gate input, whereas operating state of the circuit is also changed.

The DTMOS based four-quadrant analog multiplier circuit by using the folded Gilbert cell is presented in Figure 2. M3-M4 forms one differential pair, while M5-M6 transistors form another differential pair. The drain of M3-M5 and M4-M6 transistors are cross connected. The input signal V_X is applied to the cross connected differential pairs, while the input signal V_Y is applied to another differential pair consisting of M1 and M2. The bias currents (I_{SS1}, I_{SS2}, I_{SS3}) are the tail currents and $I_{SS1} = I_{SS2} = I_{SS3}$. The output current expression of the circuit is:

$$I_{OUT} = k_n V_X\left[\sqrt{\frac{k_p}{k_n}\left(\sqrt{\frac{I_{SS}}{k_p}-\frac{V_Y^2}{2}}+\frac{V_Y}{\sqrt{2}}\right)^2-V_X^2}-\sqrt{\frac{k_p}{k_n}\left(\sqrt{\frac{I_{SS}}{k_p}-\frac{V_Y^2}{2}}-\frac{V_Y}{\sqrt{2}}\right)^2-V_X^2}\right] \quad (4)$$

Where k_n and k_p are the transconductance of the n-channel and p-channel transistors, respectively. $k_n = (\mu_n C_{OX}/2)(W/L)$, μ_n, is the electron mobility, C_{OX} is the gate oxide capacitance of the NMOS transistor. W and L are the width and length of the NMOS transistors, respectively.

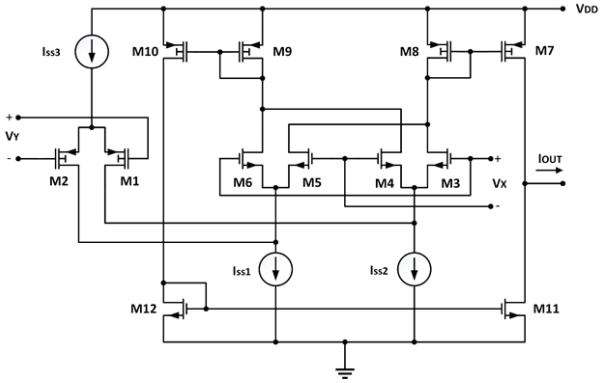

Figure 2: DTMOS based four-quadrant analog multiplier by using folded Gilbert cell

3 Simulation Results

Simulation results are presented in this section to evaluate the performance of DTMOS based folded Gilbert cell four-quadrant analog multiplier. The design verified by the Cadence Environment using 0.18 µm TSMC CMOS technology model parameters under 0.2 V supply voltage and $I_{SS1} = I_{SS2} = I_{SS3} = 100$ µA. Dimensions of the transistors are given in Table 1. Layout of the proposed DTMOS based Analog Multiplier is given in Figure 3.

Table 1: Aspect ratio of the analog multiplier

Transistor	W(µm)	L(µm)
M1, M2, M8, M9	20	0.26
M7, M10	10	0.26
M3-M6, M11, M12	1.3	0.26

The DC transfer characteristic of DTMOS based analog multiplier is given in Figures 4 and 5. For the proposed multiplier topology, the transfer curve I_{OUT} versus V_X and I_{OUT} versus V_Y are shown in Figure 4 and Figure 5 respectively. In Figure 4, V_Y is swept from −200 mV to 200 mV while V_X is varied from −200 mV to 200 mV in step size of 100 mV. In Figure 5, V_X is swept from −200 mV to 200 mV while V_Y is varied from −200 mV to 200 mV in step size of 100 mV. Figures 4 and Figure 5 show that the proposed multiplier can be easily used as four quadrant multiplier.

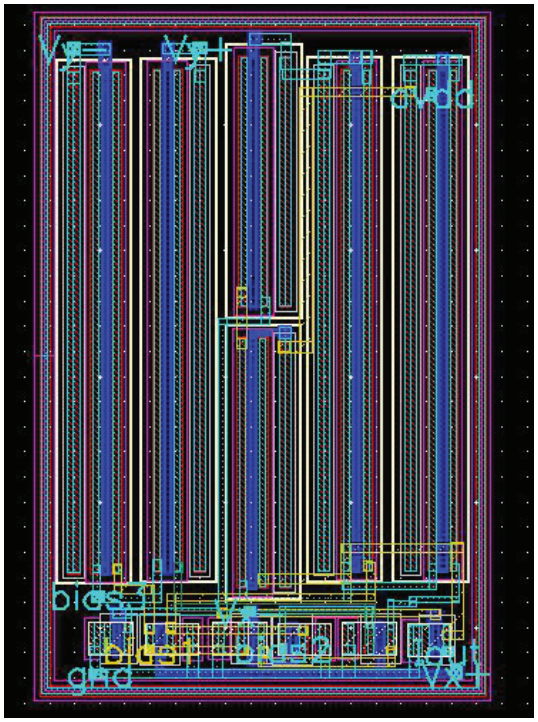

Figure 3: The layout of the proposed analog multiplier (Chip area of the proposed structure is 491.4 µm^2.)

In order to evaluate the AC transfer characteristics of DTMOS based analog multiplier, the input voltage V_X 100 mV DC is kept constant while the other input voltage V_Y 100 mVp-p AC is applied. The frequency response characteristics of the analog multiplier are shown in Figure 6. -3 dB bandwidth of the proposed structure is 1.4 GHz and 1.2 GHz for the schematic and post layout simulations respectively.

To evaluate the performance of the DTMOS-based analog multiplier as an amplitude modulator, two sinusoidal signals with 200 mV amplitude at 10 kHz and 300 kHz frequencies were applied to the inputs, respectively. The multiplier can be used as a modulator is shown in Figures 7 and 8.

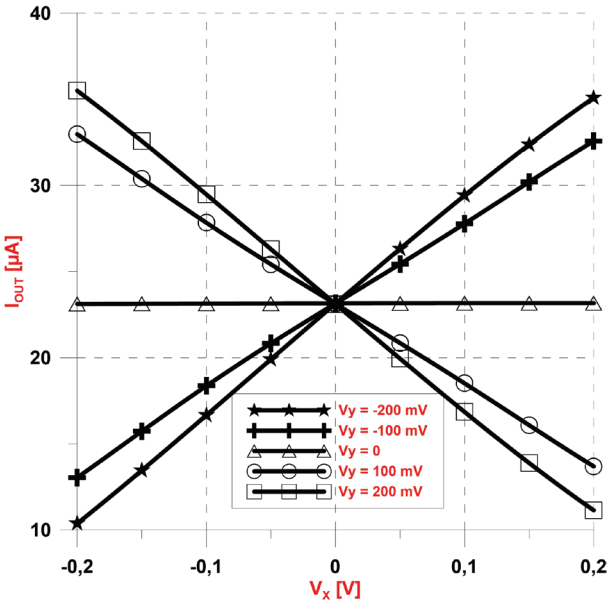

Figure 4: DC characteristics of the proposed multiplier versus V_X with V_Y as a parameter.

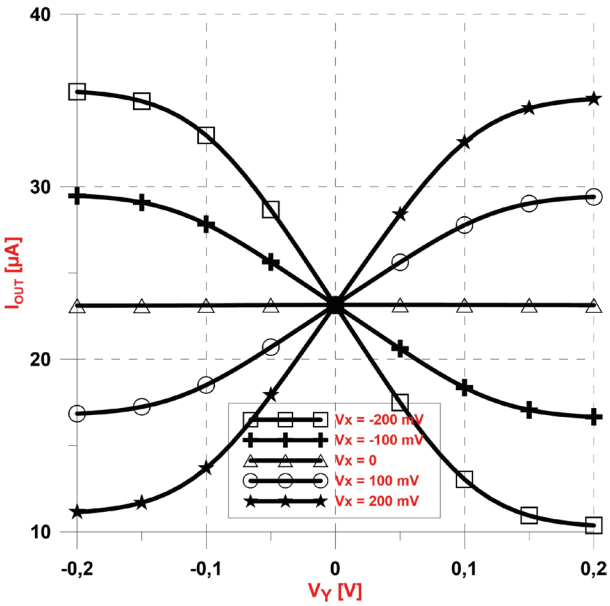

Figure 5: DC characteristics of the proposed multiplier versus V_Y with V_X as a parameter.

Intermodulation distortion for analog multipliers is a performance criterion just like total harmonic distortion. Ideally, the total harmonic distortion at the output of a multiplier is zero and no intermodulation products are presented. Intermodulation products arise as a result of the non-linearity of analog multipliers. Table 2

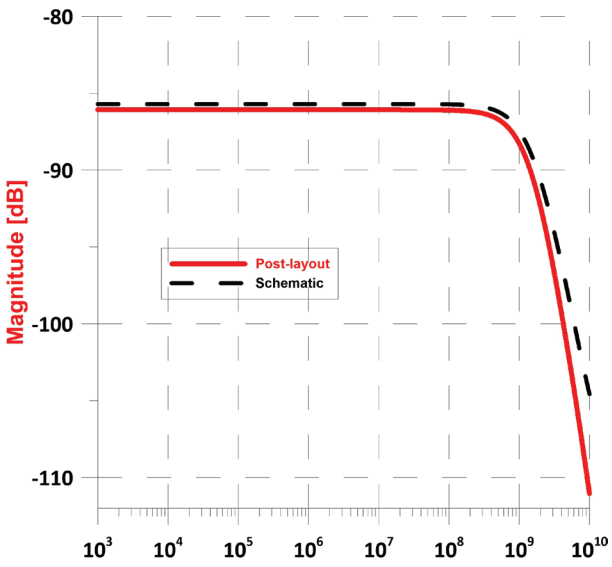

Figure 6: AC characteristics of the proposed multiplier for post layout and schematic simulations

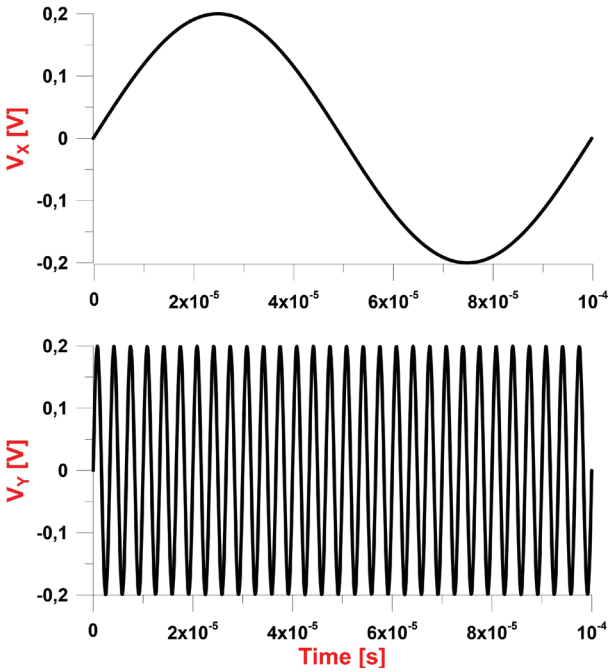

Figure 7: V_X (10 kHz) and V_Y (300 kHz) input signals applied to the proposed multiplier.

shows the 2nd, 3rd, 4th and 5th degree intermodulation products of the signal at the output of the proposed multiplier. Two sinusoidal signals were applied to the inputs of the analog multiplier at frequencies f_1 = 10 kHz and f_2 = 300 kHz. Furthermore, the frequency spectrum of the output of the proposed multiplier is given in Figure 9.

To evaluate the total harmonic distortion (THD) of the output signal of the proposed multipliers, a constant

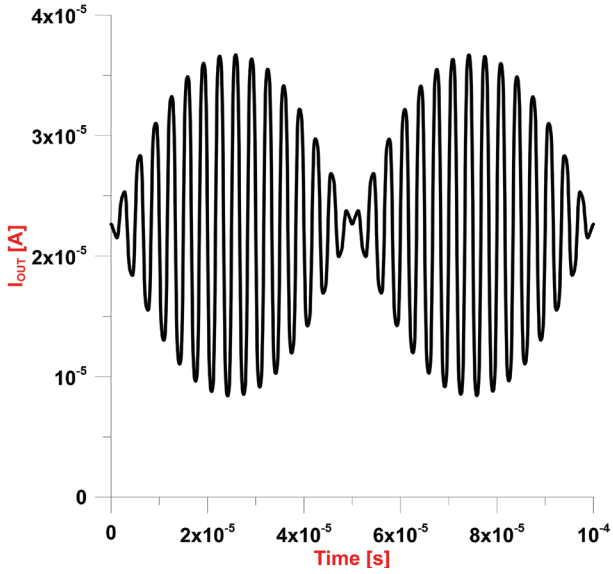

Figure 8: Output of the proposed multiplier as an amplitude modulator

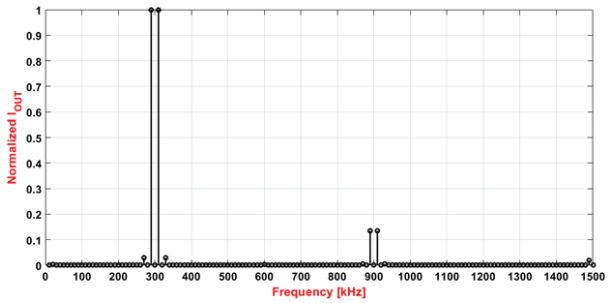

Figure 9: Frequency spectrum of the proposed multiplier as an amplitude modulator

DC voltage of 200 mV was applied to the V_Y input, while a sinusoidal signal with a frequency of 1 kHz, 10 MHz and 100 MHz were applied to the V_X input. The THD of the output voltage of the proposed multiplier is given in Figure 10 as a function of the input signal. THD [%] is composed of 9 harmonics and it is considered that the maximum THD is below 3% for the total scope of the input signal.

In order to evaluate the performance of the proposed multiplier as a frequency doubler, a sinusoidal signal of 100 mV amplitude and 10 kHz frequency was applied to both inputs of the multiplier. The accuracy of the frequency doubler function for the proposed multiplier is indicated in Figure 11.

The variation of AC and DC characteristics of the proposed multiplier with temperature is investigated. The temperature changes from 0 to 100 ° C, while the change in AC characteristic is shown in Figure 12. The DC characteristic change in the same temperature

Table 2: Intermodulation products of the proposed multiplier.

Order	Harmonics [kHz]	Fourier Components	Normalized Fourier Components (dB)	Intermodulation Products [kHz]	Fourier Components	Normalized Fourier Components (dB)
2	20	2.90×10^{-8}	-24.55	290	8.26×10^{-6}	0
	600	2.02×10^{-8}	-26.12	310	8.26×10^{-6}	0
3	30	9.50×10^{-11}	-49.39	320	3.10×10^{-9}	-34.25
	900	1.80×10^{-9}	-36.62	590	7.70×10^{-11}	-50.30
				610	1.12×10^{-10}	-48.69
4	40	1.68×10^{-9}	-36.92	330	2.48×10^{-7}	-15.22
				580	9.48×10^{-9}	-29.40
				620	9.45×10^{-9}	-29.42
	1200	6.04×10^{-9}	-31.36	890	1.11×10^{-6}	-8.70
				910	1.11×10^{-6}	-8.70
5	50	8.59×10^{-11}	-49.83	340	1.06×10^{-9}	-38.92
				630	1.10×10^{-10}	-48.74
				880	7.19×10^{-10}	-40.60
	1500	6.70×10^{-11}	-50.91	920	7.94×10^{-10}	-40.17
				1190	1.51×10^{-11}	-57.38
				1210	5.62×10^{-11}	-51.67

change is presented in Figure 13. V_Y is swept from –200 mV to 200 mV while V_X is varied from –200 mV to 200 mV in step size of 100 mV.

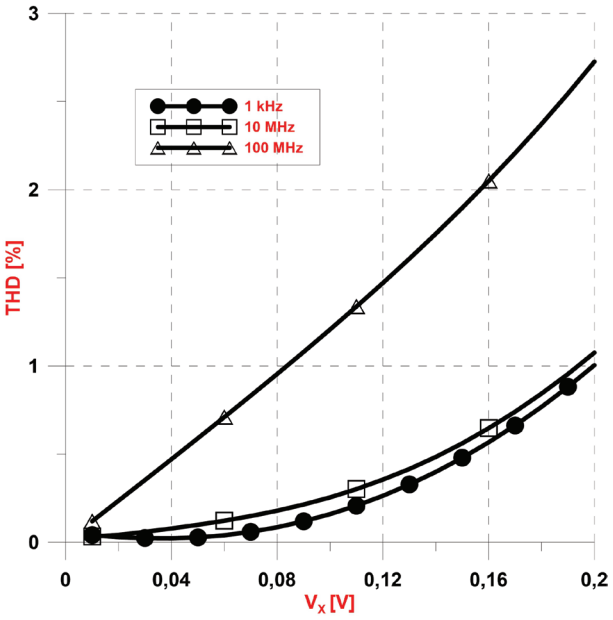

Figure 10: Relation between THD and V_X (peak) voltage with respect to 1 kHz, 10 MHz and 100 MHz frequencies.

The statistical distribution of the width (W) of the proposed multiplier circuit for 10% mismatch is given in Figure 13 for 200 runs. The histogram showing the statistical distribution in Figure 14 according to the 10% mismatch change in transistor width is given in Monte

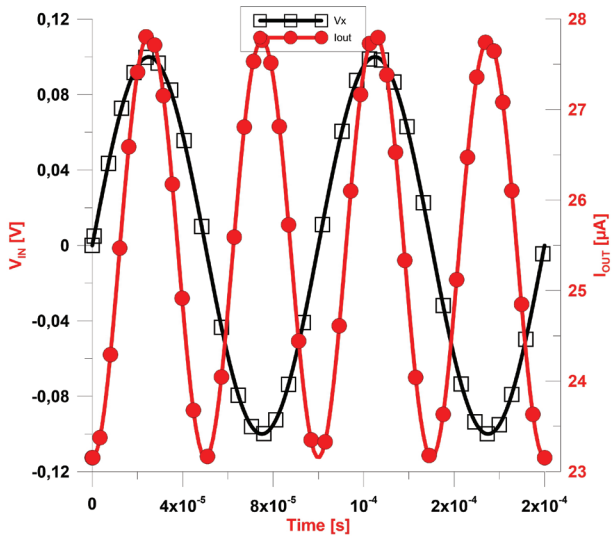

Figure 11: Output of the proposed multiplier as a frequency doubler.

Carlo analyses. According to the histogram, maximum bandwidth reaches up to 1.309 GHz whereas minimum bandwidth is 1.105 GHz. Also, average value is given as 1.230 GHz according to the post layout simulations. In addition to the 10% mismatch in width (W), the analysis made by adding 10% mismatch change in t_{ox} and V_{TH} process parameters is presented in Figure 15. In the histogram showing the statistical distribution here, the maximum bandwidth is 1.360 GHz and the minimum bandwidth is 1.114 GHz respectively. The average bandwidth is 1.23 GHz. All simulations have been done with post layout simulations.

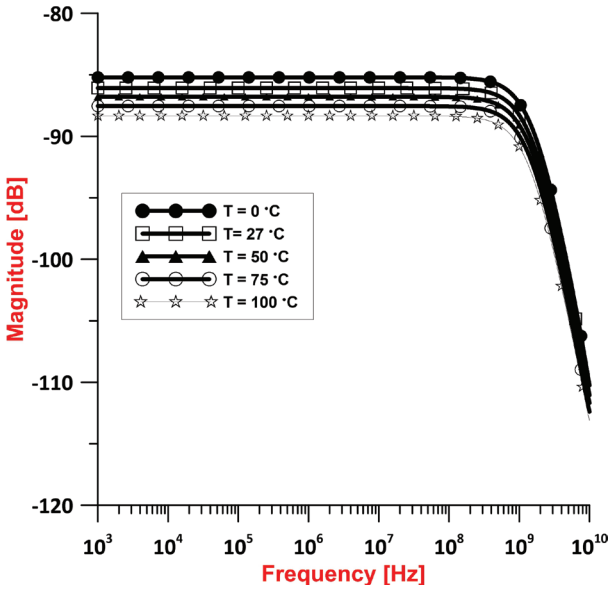

Figure 12: Post layout AC characteristic of the proposed multiplier when the temperature varies from 0 to 100 ° C.

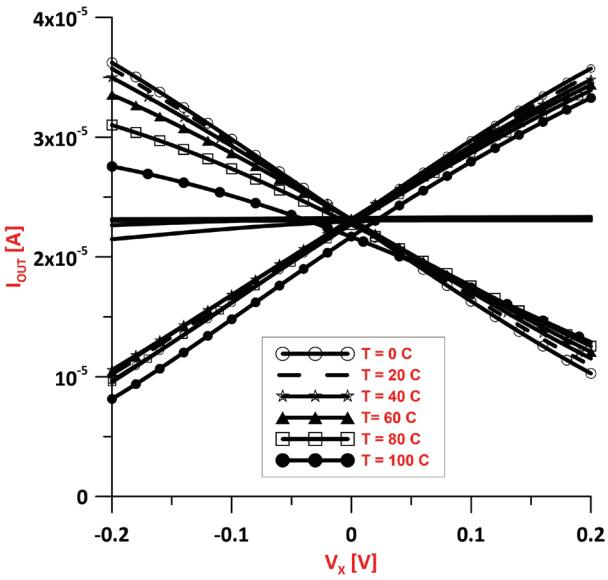

Figure 13: Post layout DC characteristic of the proposed multiplier when the temperature varies from 0 to 100 ° C.

Figure of Merit (FoM) is defined in order to compare the analog multiplier circuits in the literature with the proposed multiplier. Definition of FOM is:

$$\mathrm{FoM} = \frac{\mathrm{Bandwidth\,(MHz)}}{\mathrm{THD} \times \mathrm{Supply\_Voltage\,(V)} \times \mathrm{Power\_Consumption\,(\mu W)}} \quad (5)$$

where bandwidth is in (MHz), THD in (%), supply voltage in (V), and power consumption is evaluated in (μW). The FoM value of the proposed multiplier outperforms the other multipliers in the literature. Table 3 shows the comparison of the multiplier according to FoM value and various performance criteria with the existing multipliers in the literature. The circuits with higher FOM values are superior to the others. According to this, the FoM value of the circuit we recommend is 162.08, while the FoM value of the nearest circuit [30] is nearly four times less.

Table 3: Comparison table of the proposed multiplication circuit with previous studies

Ref	Year	Tech.	Power Supply	Bandwidth	THD (Frequency, Voltage)	Power Consumption	Input Range	FoM
[4]	2014	0.25 μm	±1.25 V	NA	1.62% (1 MHz, 125 mV)	4.02 μW	125 mV	-
[5]	2011	0.35 μm	2 V	1.5 GHz	2.67% (1 MHz, 1 V)	NA	±1 V	-
[6]	2018	0.25 μm	±0.75 V	NA	3% (1 MHz, 200 mV)	777 μW	±200 mV	0.002*
[7]	2005	0.5 μm	±1.5 V	25.34 MHz	4.667% (1 MHz, 1 V)	1.6 mW	±1 V	0.0011
[31]	2000	0.35 μm	±1.5 V	1.3 GHz	0.9% (1 MHz, 1V)	2.6 mW	±1 V	0.1851
[32]	2006	0.35 μm	±2.5 V	30 MHz	0.62% (NA)	1.2 mW	±400 mV	0.0080
[11]	2013	0.18 μm	0.5 V	221 kHz	5.8 % (1 kHz, 50 mV)	714 nW	±80 mV	0.1067
[33]	2010	0.35 μm	1.5 V	268 kHz	4.2 % (10 kHz, NA)	6.7 μW	±120 mV	0.0063
[34]	2015	0.18 μm	1.8 V	1.45 GHz	0.37 % (1 MHz, 0.5 V)	84 μW	500 mV	25.9187
[26]	2012	0.13 μm	0.5 V	10 MHz	1.4 % (NA, 0.5 V)	1.56 μW	±600 mV	9.157
[30]	2010	0.18 μm	1.2 V	2 GHz	1.5 % (NA)	25 μW	±200 mV	44.4444
[24]	2019	0.18 μm	±0.2 V	1.11 MHz	3.7 % (1 kHz, 100 mV)	18.4 nW	±200 mV	40.760
[35]	2009	0.25 μm	±0.5 V	250 MHz	NA	NA	NA	-
[23]	2019	0.5 μm	3.3 V	50 MHz	lower 1 % (1 kHz, 0.2 V)	660 μW	±200 mV	0.022
Proposed#	2020	0.18 μm	0.2 V	1.2 GHz	0.83 % (10 MHz, 100 mV)	44.6 μW	200 mV	162.08

*Bandwidth is defaulted to 10 MHz.
Data are post layout simulation results

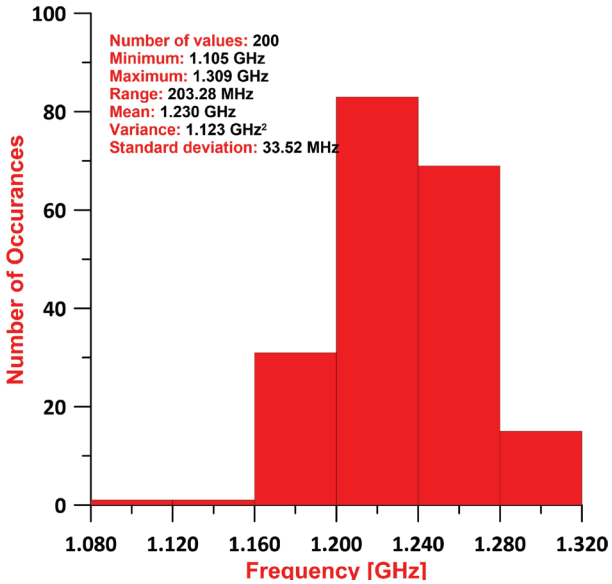

Figure 14: The bandwidth distribution of analog multiplier depending on MOSFET widths (W)

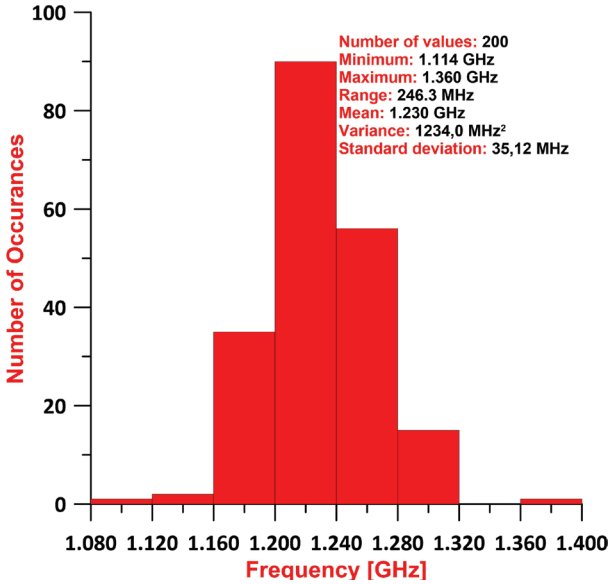

Figure 15: The bandwidth distribution of analog multiplier depending on process parameters (t_{ox} and V_{TH}) and MOSFET widths (W)

4 Conclusion

In this study, a four-quadrant analog multiplier in with voltage input and current output is presented. The circuit is designed using dynamic threshold MOS and folded Gilbert cell structure. The circuit has advantageous parameters such as wide bandwidth, low supply voltage, low power consumption and low THD. Also, the proposed structure is tested in various applications to evaluate circuit performance. Intermodulation products are given to show the efficiency as a modulator. Compared with the studies in the literature, it stands out with its wide bandwidth and low power consumption.

5 Acknowledgement

All simulations have done with Cadence Design Environment in 0.18µm TSMC CMOS technology. In this respect, we are thankful to Istanbul Technical University VLSI Laboratories for the Cadence Design Environment support.

6 References

1. S. Menekay, R. C. Tarcan, and H. Kuntman, "Novel high-precision current-mode multiplier/divider," *Analog Integr. Circuits Signal Process.*, vol. 60, no. 3, pp. 237–248, 2009. https://doi.org/10.1007/s10470-009-9289-7
2. J. M. Algueta Miguel, C. a. De La Cruz Blas, and A. J. Lopez-Martin, "Fully Differential Current-Mode CMOS Triode Translinear Multiplier," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 58, no. 1, pp. 21–25, Jan. 2011. https://doi.org/10.1109/TCSII.2010.2092821
3. I. M. Filanovsky and H. Baltes, "CMOS two-quadrant multiplier using transistor triode regime," *IEEE J. Solid-State Circuits*, vol. 27, no. 5, pp. 831–833, May 1992. https://doi.org/10.1109/4.133175
4. E. Yuce and F. Yucel, "A new cascadable CMOS voltage squarer circuit and its application: Four-quadrant analog multiplier," *Indian J. Eng. Mater. Sci.*, vol. 21, no. 4, pp. 351–357, 2014.
5. S. Keleş and H. H. Kuntman, "Four quadrant FG-MOS analog multiplier," *Turkish J. Electr. Eng. Comput. Sci.*, vol. 19, no. 2, pp. 291–301, 2011. https://doi.org/10.3906/elk-1001-377
6. F. Yucel and E. Yuce, "Analog Squarers Using only Seven MOS Transistors and a Four Quadrant Analog Multiplier Application," *J. Circuits, Syst. Comput.*, vol. 27, no. 5, pp. 1–9, 2018. https://doi.org/10.1142/S0218126618500718
7. M. A. Hashiesh, S. A. Mahmoud, and A. M. Soliman, "New four-quadrant CMOS current-mode and voltage-mode multipliers," *Analog Integr. Circuits Signal Process.*, vol. 45, no. 3, pp. 295–307, 2005. https://doi.org/10.1007/s10470-005-4957-8
8. A. Alikhani and A. Ahmadi, "A novel current-mode four-quadrant CMOS analog multiplier/divider," *AEU - Int. J. Electron. Commun.*, vol. 66, no. 7, pp. 581–586, 2012. https://doi.org/10.1016/j.aeue.2011.11.012
9. I. Aloui, N. Hassen, and K. Besbes, "A CMOS current mode four quadrant analog multiplier free from

mobility reduction," *AEU - Int. J. Electron. Commun.*, vol. 82, pp. 119–126, Dec. 2017. https://doi.org/10.1016/j.aeue.2017.08.006
10. B. Gilbert, "A precise four-quadrant multiplier with subnanosecond response," *IEEE J. Solid-State Circuits*, vol. 3, no. 4, pp. 365–373, Dec. 1968. https://doi.org/10.1109/JSSC.1968.1049925
11. A. Panigrahi and P. K. Paul, "A novel bulk-input low voltage and low power four quadrant analog multiplier in weak inversion," *Analog Integr. Circuits Signal Process.*, vol. 75, no. 2, pp. 237–243, 2013. https://doi.org/10.1007/s10470-012-9951-3
12. S. Soltany and A. Rezai, "A novel low power and low voltage bulk-input four-quadrant analog multiplier in voltage mode," *Int. J. Multimed. Ubiquitous Eng.*, vol. 11, no. 1, pp. 159–168, 2016. https://doi.org/10.14257/ijmue.2016.11.1.16
13. S. Menekay, R. C. Tarcan, and H. Kuntman, "Novel high-precision current-mode circuits based on the MOS-translinear principle," *AEU - Int. J. Electron. Commun.*, vol. 63, no. 11, pp. 992–997, 2009. https://doi.org/10.1016/j.aeue.2008.08.010
14. M. A. Al-Absi and I. A. As-Sabban, "A New Highly Accurate CMOS Current-Mode Four-Quadrant Multiplier," *Arab. J. Sci. Eng.*, vol. 40, no. 2, pp. 551–558, 2015. https://doi.org/10.1007/s13369-014-1551-3
15. A. N. Saatlo and I. S. Özoğuz, "Design of a high-linear, high-precision analog multiplier, free from body effect," *Turkish J. Electr. Eng. Comput. Sci.*, vol. 24, no. 3, pp. 820–832, 2016. https://doi.org/10.3906/elk-1307-159
16. C. Abel, S. Sakurai, F. Larsen, and M. Ismail, "Christopher Abel, Satoshi Sakurai, Frode Larsen, and Mohammed Ismail Department of Electrical Engineering The Ohio State University 2015 Neil Avenue, Columbus, OH 43210," *Electr. Eng.*, no. 3, pp. 273–276, 2015. https://doi.org/10.1109/ISCAS.1994.409358
17. E. Ibaragi, A. Hyogo, and K. Sekine, "A CMOS analog multiplier free from mobility reduction and body effect," *Analog Integr. Circuits Signal Process.*, vol. 25, no. 3, pp. 281–290, 2000. https://doi.org/10.1023/A:1008377914605
18. C.-C. Chang and S.-I. Liu, "Weak inversion four-quadrant multiplier and two-quadrant divider," *Electron. Lett.*, vol. 34, no. 22, p. 2079, 1998. https://doi.org/10.1049/el:19981496
19. A. G. Andreou and K. A. Boahen, "Translinear circuits in subthreshold MOS," *Analog Integr. Circuits Signal Process.*, vol. 9, no. 2, pp. 141–166, Mar. 1996. https://doi.org/10.1007/BF00166411
20. D. Coué and G. Wilson, "A four-quadrant subthreshold mode multiplier for analog neural-network applications," *IEEE Trans. Neural Networks*, vol. 7, no. 5, pp. 1212–1219, 1996. https://doi.org/10.1109/72.536315
21. M. Gravati, M. Valle, G. Ferri, N. Guerrini, and L. Reyes, "A novel current-mode very low power analog cmos four quadrant multiplier," *Proc. 31st Eur. Solid-State Circuits Conf. 2005. ESSCIRC 2005.*, no. 1, pp. 495–498, 2005. https://doi.org/10.1109/esscir.2005.1541668
22. P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, 3th ed. New York, USA: Oxford University Press, 2012.
23. G. Zamora-Mejia, A. Diaz-Armendariz, H. Santiago-Ramirez, J. M. Rocha-Perez, C. A. Gracios-Marin, and A. Diaz-Sanchez, "Gate and Bulk-Driven Four-Quadrant CMOS Analog Multiplier," *Circuits, Syst. Signal Process.*, vol. 38, no. 4, pp. 1547–1560, 2019. https://doi.org/10.1007/s00034-018-0945-y
24. Y. Babacan, "Ultra-low voltage and low-power voltage-mode DTMOS-based four-quadrant analog multiplier," *Analog Integr. Circuits Signal Process.*, vol. 99, no. 1, pp. 39–45, 2019. https://doi.org/10.1007/s10470-018-1322-2
25. E. Ozer, "A DTMOS based Four-Quadrant Analog Multiplier," *Electrica*, vol. 20, no. 2, pp. 207–217, Jun. 2020. https://doi.org/10.5152/electrica.2020.20019
26. J. De La Cruz-Alejo, A. S. Medina-Vazquez, and L. N. Oliva-Moreno, "FGMOS four-quadrant analog multiplier," *CCE 2012 - 2012 9th Int. Conf. Electr. Eng. Comput. Sci. Autom. Control*, 2012. https://doi.org/10.1109/ICEEE.2012.6421200
27. M. Gupta, R. Srivastava, and U. Singh, "Low Voltage Floating Gate MOS Transistor Based Differential Voltage Squarer," *ISRN Electron.*, vol. 2014, pp. 1–6, 2014. https://doi.org/10.1155/2014/357184
28. F. Assaderaghi, S. Parke, D. Sinitsky, J. Bokor, P. K. Ko, and Chenming Hu, "A dynamic threshold voltage MOSFET (DTMOS) for very low voltage operation," *IEEE Electron Device Lett.*, vol. 15, no. 12, pp. 510–512, Dec. 1994. https://doi.org/10.1109/55.338420
29. M. E. Başak and F. Kaçar, "Ultra-low voltage VDBA design by using PMOS DTMOS transistors," *IU-JEEE*, vol. 17, no. 2, pp. 3463–3469, 2017. https://doi.org/10.1109/55.338420
30. A. Ebrahimi, H. M. Naimi, and M. Gholami, "Compact, low-voltage, low-power and high-bandwidth CMOS four-quadrant analog multiplier," *2010 11th Int. Work. Symb. Numer. Methods, Model. Appl. to Circuit Des. SM2ACD 2010*, no. 6, pp. 1–5, 2010. https://doi.org/10.1109/SM2ACD.2010.5672341
31. S. C. Li, "A Symmetric Complementary Structure for RF CMOS Analog Squarer and Four-Quadrant

Analog Multiplier," *Analog Integr Circ Sig Process*, vol. 23, pp. 103–115, 2000. https://doi.org/10.1023/A:100838980

32. B. Boonchu and W. Surakampontorn, "CMOS voltage-mode analog multiplier," in *2006 IEEE International Symposium on Circuits and Systems*, 2006, vol. 1, no. 5, p. 4. https://doi.org/10.1109/ISCAS.2006.1693003
33. W. Liu and S. I. Liu, "Design of a CMOS low-power and low-voltage four-quadrant analog multiplier," *Analog Integr. Circuits Signal Process.*, vol. 63, no. 2, pp. 307–312, 2010. https://doi.org/10.1007/s10470-009-9382-y
34. A. Amiri and A. N. Saatlo, "Voltage mode implementation of highly accurate analog multiplier circuit," *ICEE 2015 - Proc. 23rd Iran. Conf. Electr. Eng.*, vol. 10, pp. 1059–1062, 2015. https://doi.org/10.1109/IranianCEE.2015.7146368
35. V. Niranjan and M. Gupta, "Low voltage four-quadrant analog multiplier using dynamic threshold MOS transistors," *Microelectron. Int.*, vol. 26, no. 1, pp. 47–52, Jan. 2009. https://doi.org/10.1108/13565360910923179

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In memoriam zaslužnemu profesorju dr. Jožetu Furlanu

(Žalna seja, UL FE, 1.7.2020)

Prof. dr. Jože Furlan
Zaslužni professor Univerze v Ljubljani
(1934-2020)

Spoštovana družina profesorja Jožeta Furlana, spoštovani prijatelji in sodelavci profesorja Jožeta Furlana, spoštovani bivši študenti, diplomanti in doktoranti profesorja Jožeta Furlana, spoštovane dame in gospodje!

V imenu Katedre za elektroniko želiva predstaviti zaslužnega profesorja Univerze v Ljubljani, rednega profesorja dr. Jožeta Furlana, univ. dipl. inž. el. In njegovo življenjsko pot.

Prof. Jože Furlan je preko šest desetletij oblikoval, zaznamoval in bogatil slovensko elektroniko kot univerzitetni učitelj Fakultete za elektrotehniko Univerze v Ljubljani. Prof. Furlan se je trajno zapisal v zgodovino slovenske elektronike kot pionir na področju polprevodniških elementov, tranzistorskih in integriranih vezij ter fotovoltaike.

Jože Furlan je bil rojen leta 1934 v Limbušu pri Mariboru. Že v otroških letih se je navdušil nad elektrotehniko. Kot gimnazijski dijak je pridno obiskoval radioamaterske tečaje in sestavljal radijske sprejemnike ter na ta način prišel v prvi stik z elektroniko, ki se ji je nato zapisal za vse življenje.

Med leti 1952 in 1957 je študiral elektrotehniko na Oddelku za elektrotehniko Tehniške visoke šole v Ljubljani. Med študijem je sodeloval kot demonstrator pri predmetu *Elektronika in elektronske cevi* ter vodil vaje za študente elektrotehnike in fizike. Hkrati je bil v višjih letnikih honorarno zaposlen na Fizikalnem inštitutu Medicinske visoke šole v Ljubljani, kjer je načrtoval in sodeloval pri gradnji elektronskih naprav. Zelo zgodaj se je zavedal pomena mednarodne vpetosti in znanja tujih jezikov. Tako se je kot študent usposabljal na 4-mesečni praksi v Nemčiji pri podjetju Electronic GmbH v Münchnu, po končani diplomi leta 1958 pa v Veliki Britaniji in sicer 2 meseca pri podjetju Edward's High Vacuum v Crawleyu.

Še istega leta se je zaposlil kot asistent pri prof. dr. Dušanu Lasiču na Oddelku za šibki tok Fakultete za elektrotehniko in strojništvo Univerze v Ljubljani. Prvo raziskovalno in pedagoško področje prof. Furlana so bile tedaj, v predtranzistorskem obdobju, še vedno zelo aktualne vakuumske elektronke. Pri tem delu je preučeval električna polja in gibanje elektronov v večelektrodnih elektronkah ter raziskoval šum v osnovnih elektronskih elementih. Še posebej je znan njegov merilnik šumov fotopomnoževalk.

Leta 1960 je bil z ameriško tehnično pomočjo na polletnem akademskem in raziskovalnem izpopolnjevanju v laboratoriju tedaj enega od vodilnih strokovnjakov na področju prihajajočih tranzistorjev, pri prof. Johnu Linvillu na Univerzi Stanford, kjer je pridobival vrhunska znanja s področja polprevodniških elementov. Tako se je že na začetku šestdesetih let kot eden prvih slovenskih elektronikov preusmeril od elektronk k tranzistorjem in od tod naprej na področje mikroelektronike. Od jeseni 1960 je bil honorarni predavatelj za predmet *Elektronika* na Oddelku za fiziko in od jeseni 1963 tudi za predmet *Osnove elektronike* na Oddelku za metalurgijo Fakultete za naravoslovje in tehnologijo. Na III. stopnjo študija *Elektronska optika* na Fakulteti za elektrotehniko se je vpisal leta 1961 in ga uspešno zaključil z magistrskim delom v letu 1966 in z doktoratom iz elektrotehniških znanosti 1968. Sredi šestdesetih let je napisal znano knjigo *Elektronika*, v kateri je obravnaval nova tranzistorska vezja in jih primerjal z vezji na osnovi elektronk. Od leta 1966 je bil zaposlen kot redni docent za predmete *Elektronika* in *Napajalne naprave*, dve

leti kasneje je prevzel še podiplomska predmeta *Fizika šumov* in *Mikroelektronika*.

V letih 1969-1970 je bil na izpopolnjevanju v enem od vodilnih razvojno-raziskovalnih laboratorijev na področju mikroelektronike, pri podjetju Hewlett-Packard v Silicijevi dolini, kjer je raziskoval tranzistorska integrirana vezja. Tu je pridobival najnovejša načrtovalska in tehnološka znanja na področju integriranih vezij. V tem obdobju je za Hewlett-Packard razvil tudi dve zahtevni integrirani vezji za števni merilnik frekvence HP 5345A. Kot je zapisala strokovna komisija ob njegovi izvolitvi v izrednega profesorja leta 1972: "…, kjer je izvedel nekatere nove tipe integriranih tranzistorskih vezij pa tudi dva osnovna tipa in nekaj izvedenk ekstremno hitrih integriranih vezij za impulzne signale na 500 MHz. Pripomniti velja, da najhitrejša komercialno dosegljiva vezja dosegajo komaj mejo 300 MHz.".

Po povratku v Ljubljano je prof. Furlan napisal prvi knjigi pri nas s področja mikroelektronskih tehnologij in elektronike integriranih vezij. Nato je do sredine sedemdesetih let intenzivno deloval pri raziskovalnem in pedagoškem delu v Laboratoriju za mikroelektroniko na Fakulteti za elektrotehniko UL, pri čemer so bile za uspešno delo izredno koristne njegove bogate izkušnje, pridobljene v Ameriki.

Profesor Furlan pa ni bil samo izredno prodoren na raziskovalnem in strokovnem področju. Vseskozi je bil tudi skrben pedagog in odličen predavatelj ter vsestransko aktiven, angažiran in predan.

Leta 1977, ob izvolitvi v rednega profesorja, je strokovna komisija zapisala: "Kandidat je svojo družbeno aktivnost izpričal z delom v mnogih delovnih telesi: predstojnik oddelka, predstojnik katedre, predsednik sindikalnega odbora, 5 let poslanec Kulturno prosvetnega zbora Skupščine SRS, član sveta VDO FE, član drugih odborov in komisij. S posebno zavzetostjo je vodil delo Sistematizacijske komisije kot njen predsednik."

Profesor Furlan je aktivno sodeloval tudi izven univerze, predvsem v stroki. Bil je med pobudniki in od samega začetka sodeloval pri snovanju jugoslovanske sekcije Mednarodne elektrotehniške organizacije IEEE. Od njene ustanovitve leta 1972 je deloval najprej kot tajnik, nato pa kot predsednik jugoslovanske sekcije IEEE. Mnogo let je bila Jugoslovanska sekcija IEEE edina iz skupine vzhodnoevropskih držav, kar je – v tistih precej hermetičnih časih – med drugim omogočilo nemoten dostop do vrhunskih IEEE publikacij ter do raznih drugih članskih ugodnosti.

V drugi polovici 70-tih let se je raziskovalno delo prof. Furlana usmerilo v študij osnovnih pojavov, lastnosti in aplikacij polprevodniških elementov ter tedaj še razmeroma novih sončnih celic iz monokristalnega in amorfnega silicija. Ustanovil in mnogo let je uspešno vodil Laboratorij za nelienarne elemente, ki se je kasneje preimenoval v Laboratorij za elektronske elemente. Iz slednjega sta zaradi povečanega obsega raziskovalnega dela kasneje izšla dva uspešna laboratorija na UL FE, laboratorij LMSE (Laboratorij za mikrosenzorske strukture in elektroniko) in LPVO (Laboratorij za fotovoltaiko in optoelektroniko).

Svoje bogate izkušnje je prof. Furlan prispeval v mnogih uspešnih raziskovalnih projektih, tako v povezavi z domačimi in mednarodnimi raziskovalnimi institucijami kot v sodelovanju z industrijo. S podjetji je bilo najtesnejše in najplodnejše sodelovanje z Iskro Tovarno polprevodnikov v Trbovljah.

Vsa leta aktivnega delovanja na Fakulteti za elektrotehniko je prof. Furlan tudi zelo zavzeto predaval mnoge predmete in napisal večje število izvrstnih knjižnih del in učbenikov s področja elektronike, polprevodniških in drugih elektronskih elementov ter integriranih vezij. Tako univerzitetnih kot srednješolskih učbenikov. Na Fakulteti za elektrotehniko je predaval vrsto dodiplomskih in podiplomskih predmetov, od osnov elektronike do mikroelektronike, polprevodniških elementov in pasivnih elementov, optoelektronike, sončnih celic, teorije polprevodnikov ter teorije šumov. Predaval je tudi predmete dodiplomskega in podiplomskega študija na Fakulteti za naravoslovje in tehnologijo, UL in tudi izvajal predavanja za izredne študente v centrih Ljubljana, Kranj in Novo mesto.

Prof. Furlan je vsa leta zelo prizadevno, kot izjemno pozoren mentor, vodil tudi raziskovalno delo študentov in mladih raziskovalcev podiplomskega in doktorskega študija. Njegovi študentje in diplomanti so postali vodilni razvojniki, direktorji, znanstveni svetniki in celo redni profesorji. Rezultati opravljenih raziskav prof. Furlana, v sodelovanju z mlajšimi sodelavci in podiplomskimi študenti, so bili objavljeni v mnogih skupnih publikacijah, ki so izšle v številnih znanstvenih revijah in na specializiranih konferencah doma in v tujini, o čemer priča tudi njegova izredno bogata bibliografija. Prof. Furlan je imel tudi vrsto vabljenih predavanj na uglednih univerzah v Evropi in v ZDA.

Na Fakulteti za elektrotehniko je med drugim vrsto let vodil Oddelek za elektroniko in bil dolga leta predstojnik Katedre za elektroniko. Bil je tudi prodekan za pedagoško delo in predsednik komisije za podiplomski študij.

Prof. Furlan je bil tudi izumitelj. Prijavil je več izumov in patentov. S področja polprevodniških struktur in integriranih vezij je npr. prijavil novo vezje polnega seštevalnika, integrirano MOS izvedbo elektronskega časovnega izbiralnika in novo strukturo modificirane CHIL celice. S področja fotovoltaike je najbolj znan ameriški patent o paralelni tandemski sončni celici iz amorfnega silicija.

Za svoje bogato pionirsko, znanstveno-raziskovalno in pedagoško delovanje na področju polprevodnikov, mikroelektronike in fotovoltaike je prof. Furlan prejel številna priznanja in nagrade. Med prvimi učitelji na FE UL je prejel Vidmarjevo nagrado za odlično pedagoško delo.

Za raziskave optoelektronskih lastnosti monokristalnega in amorfnega silicija je s sodelavci leta 1989 prejel nagrado Sklada Borisa Kidriča.

Za pomembne dosežke v IEEE organizaciji je prejel IEEE Third Millenium Medal.

Leta 1990 je za posebne zasluge in uspehe pri delu prejel Red dela z zlatim vencem.

Leta 2000 mu je Univerza v Ljubljani podelila naziv zaslužnega profesorja Univerze v Ljubljani.

Slika: Podelitev nagrade Sklada Borisa Kidriča 1989

Prof. Furlan je kljub formalni upokojitvi konec leta 1999 ostal zelo aktiven in nadaljeval z iskanjem odgovorov na nova, nerešena vprašanja na področju polprevodniških elementov in fotovoltaike. V sodelovanju z mlajšimi raziskovalci je z navdušujočo energijo, zavzetostjo in pronicljivostjo razčlenjeval in pojasnjeval nove pojave na omenjenih področjih, kar je vodilo do novih spoznanj ter do znanstvenih objav v mednarodnih publikacijah tudi 15 let po upokojitvi.

Celotna fakulteta, še posebej pa Katedra za elektroniko je z globoko pretresenostjo prejela žalostno vest, da je srce pionirja slovenske elektronike in vsem nam predragega zaslužnega profesorja Jožeta Furlana zastalo.

V imenu Katedre za elektroniko izrekava globoko sožalje gospe Dragici Furlan in otrokom Ariani, Alenki, Tamari, Andreju, doktorici Tjaši Furlan in vnukom ter vsem žalujočim.

Prof. dr. Jože Furlan je pustil neizbrisljive sledi in z velikim spoštovanjem ga bomo ohranili v trajno lepem spominu. Slava mu!

Prof. dr. Slavko Amon
Prof. dr. Marko Topič

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