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NAČRTOVANJE PREIZKUSLJIVOSTI MEŠANIH ANALOGNO-DIGITALNIH INTEGRIRANIH VEZIJ

Uroš Kač

Institut Jožef Stefan, Ljubljana, Slovenija

Ključne besede: načrtovanje preizkusljivosti, mešana analogno-digitalna vezja, vgrajen samodejni preizkus, oscilacijska metoda

Izvleček: V članku je obravnavana problematika načrtovanja preizkusljivosti mešanih analogno-digitalnih integriranih vezij. Predstavljeni so osnovni principi načrtovanja preizkusljivosti, ki jih je možno vgraditi v računalniška načrtovalska orodja preko takoimenovanih nadzornikov pravil načrtovanja (ang. design rule checker). Omenjene so metode, ki temeljijo na meritvah parametrov integriranega vezja, kot na primer meritev mirovnega napajalnega toka. Sledi opis tehnik, ki zagotavljajo dostop do globoko vgnezdenih podsklopov. Obravnavani sta tudi problematika generiranja in vrednotenja analognih signalov v vezju ter zasnova vgrajenega samodejnega preizkusa. Zadnji del prispevka povzema osnovne značilnosti oscilacijske preizkusne metode.

Design for test of mixed-signal integrated circuits

Key words: design for test, mixed-signal integrated circuits, built-in self-test, oscillation based test

Abstract: The proliferation of consumer electronics increasingly determines the course of development of semiconductor technology. In this context analog and mixed-signal integrated circuits and systems are regaining importance as electronic devices heavily rely on analog signal processing techniques. The semiconductor industry follows market demands by developing increasingly complex application specific integrated circuits and systems. This introduces new challenges in the process of circuit design and results in numerous difficulties in assuring adequate product quality. The latter is becoming a severe problem as the established analog test procedures already represent one of the bottlenecks in the development of complex mixed-signal systems. Consequently, research of new techniques supporting a structured approach to the design of testable analog integrated circuits is increasing steadily. Due to the diversity of analog and mixed-signal designs various solutions are being explored. The main trends are described in the paper.

The problem of circuit testing is tightly related to the circuit design process. The implementation of test structures can be simplified and the quality of the test procedure can be increased by applying design rules and procedures or design for testability (DfT) techniques. Numerous DfT techniques for mixed-signal integrated circuits have been proposed in recent years. Although the basic concepts of various techniques can differ substantially, we can roughly classify them into design of support structures for implementation of external analog measurement methods and the design of structures for the implementation of analog built-in self-test (BIST). The second group of DfT techniques is expected to play a crucial role in future complex integrated circuits and systems as it eliminates some limitations related to the use of conventional automated test equipment and increases product reliability throughout its life cycle.

The oscillation based test method (OBT) described in the last part of the paper belongs to the second group of DfT techniques. The method is based on the assumption that the tested circuit can be reconfigured into an oscillator. Faulty circuits can then be identified by simply measuring the oscillation frequency and comparing it to a reference value obtained from a fault-free (i.e., "golden") circuit under the same operating conditions. The method assumes that the oscillation frequency is sensitive to those component parameters which determine the relevant characteristics of the tested circuit. The main issue in oscillation based circuit testing is the design of testability structures and circuit reconfiguration schemes, which provide for an efficient test implementation. In the paper, general principle of OBT is described and some more details are given on its application in analog filter testing.

1 Uvod

Z naraščanjem kompleksnosti ter vse težjim dostopom do globoko vgnezdenih analognih podsklopov postaja preizkušanje integriranih vezij vse večji problem, zato jih je potrebno načrtovati tako, da jih bo možno učinkovito preizkušati. V industriji in akademskih ustanovah narašča število raziskav, katerih cilj je razvoj ustreznih tehnik in postopkov strukturiranega načrtovanja preizkusljivih analognih vezij. Pristope v grobem razdelimo na realizacijo struktur za izboljšanje vodljivosti (angl. controllability) in spremljivosti (angl. observability) notranjih vozlišč analognih podsklopov ter na načrtovanje struktur, ki omogočajo izvedbo vgrajenega samodejnega preizkusa v integriranem vezju. Zaradi obsežnosti področja ne gre iskati splošne rešitve za vsa analogna vezja, temveč je bolj smiselno iskati učinkovite tehnike preizkušanja za posamezne razrede analognih vezij.

V tem prispevku uvodoma povzemamo osnovne principe načrtovanja preizkusljivosti (angl. Design for Testability, ali okrajšano DfT), v nadaljevanju pa opisujemo izbrane pristope preizkušanja mešanih analogno-digitalnih vezij, ki so dosegli ustrezno pozornost v strokovni javnosti in se uveljavili v praksi. Zadnji del prispevka je namenjen oscilacijski preizkusni metodi, pri kateri smo tudi sami prispevali teoretske rezultate in jo uspešno uporabili v praksi.

2 Tehnološki izziv

Pomanjkanje strukturiranih DfT tehnik načrtovanja analognih podsklopov postaja ena poglavitnih ovir nadaljnjemu razvoju mešanih integriranih sistemov. Ker jih proizvajalci praviloma preverjajo s funkcionalnim preizkušanjem, je optimizacija postopkov težavna in zahteva izkušene inženirje z odličnim poznavanjem problematike. Hkrati je zelo težko

oceniti kvaliteto postopka, saj se funkcionalni preizkusi ne nanašajo neposredno na strukturne napake. Raziskovalci iz industrije in akademskih ustanov so si zato enotni, da je potrebno razviti ustrezne DfT tehnike, ki bi omogočile strukturiran pristop k problemu preizkušanja analognih podsklopov že od začetnih faz načrtovanja proizvoda, /1/, /2/, /3/, /4/. Nadalje bi razvoj učinkovitih analognih BIST struktur omogočil uporabo popolnoma digitalnih avtomatskih preizkuševalnih naprav (ang. *Automatic Test Equipment* - ATE), kar bi bistveno poenostavilo in pocenilo postopke proizvodnega preizkušanja. Iz napovedi Združenja industrije polprevodnikov /5/, lahko razberemo predvidene trende razvoja mešanih analogno-digitalnih DfT tehnik ter njihovo uporabo v bodočih kompleksnih SoC vezjih.

V skladu z naraščajočimi potrebami industrije se je v preteklih nekaj letih občutno povečalo število raziskav na tem področju. V znanstveni in strokovni literaturi lahko tako zasledimo številne prispevke, ki obravnavajo različne analogne oziroma mešane DfT tehnike. Predlagani pristopi se medsebojno precej razlikujejo, kar izhaja predvsem iz lastnosti ciljne aplikacije, vendar pa je njihov skupni cilj izboljšanje preizkusljivosti kompleksnih mešanih integriranih vezij. Slika 1 skuša povzeti nekatere najbolj pogoste DfT tehnike in primere njihove uporabe.

3 Načrtovanje preizkusljivosti mešanih analogno-digitalnih vezij

3.1 Splošna DfT pravila

Večina splošnih DfT pravil izhaja iz uveljavljenih tehnik načrtovanja analognih vezij oziroma iz predhodno pridobljenih načrtovalskih izkušenj. Osnovna pravila so:

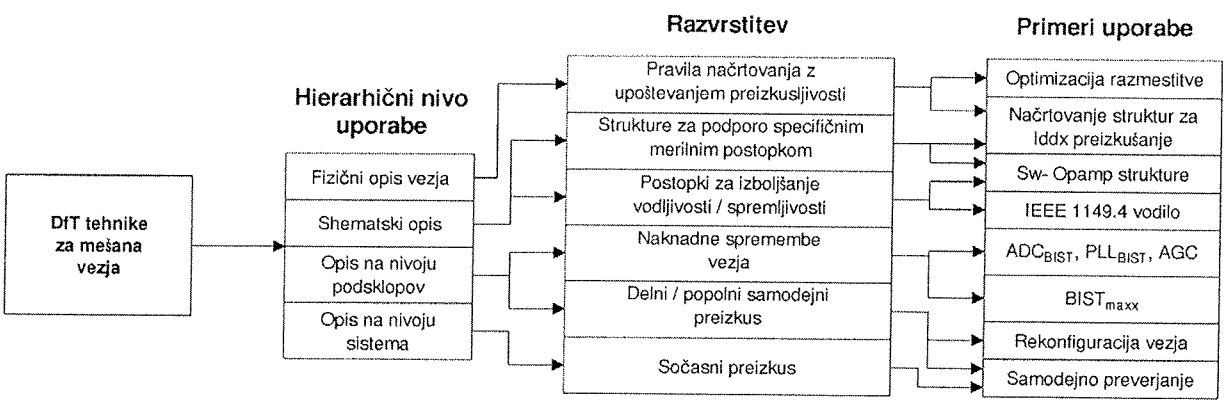
- vezja delimo na podsklope (makro celice),
- zagotovimo vodljivost vhodov podsklopov,
- zagotovimo spremljivost izhodov podsklopov,
- omogočimo izključitev povratnih zank v analognih podsklopih,
- vgradimo digitalne spominske celice v stičišča analognih in digitalnih podsklopov,
- uporabimo standarden digitalni preizkusni vmesnik za izbiro načina delovanja vezja (normalno obratovanje ali preizkušanje).

Tovrstna pravila je možno vgraditi v računalniška načrtovalska orodja, kjer lahko njihovo upoštevanje spremljamo preko t.i. "nadzornikov pravil načrtovanja" (ang. *design rule checker*). Poleg splošnih DfT pravil lahko v to skupino uvrstimo tudi ukrepe, kot je upoštevanje pravil oziroma omejitev pri fizičnem razvrščanju elementov vezja. S tem lahko zmanjšamo verjetnost pojava določenih napak in tako izboljšamo preizkusljivost vezja /6/.

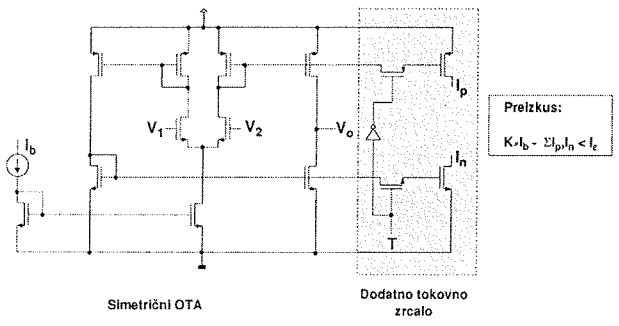
3.2 Podpora zunanjim merilnim metodam

Drugo skupino DfT tehnik predstavljajo strukture za podporo postopkom preizkušanja, ki temeljijo na zunanjih meritvah parametrov integriranega vezja. Meritev mirovnega napajalnega toka (I_{DDQ} preizkušanje) je uveljavljena tehnika proizvodnega preizkušanja digitalnih vezij /7/. Njegova uporaba v mešanih integriranih vezjih zahteva upoštevanje ustreznih strategij delitve vezja na podsklope ter možnost ločene izključitve analognih jeder. To zagotavlja minimalen vpliv le-teh na mirovni tok vezja med preizkušanjem digitalnih podsklopov.

Po drugi strani je možno meritve toka uporabiti tudi za preizkušanje analognih podsklopov vezja. Ker so nekatere analogne strukture, kot so tokovna zrcala ali generatorji prečnega (ang. *bias*) toka ali napetosti, posebej občutljive na naključno spreminjanje parametrov proizvodnega procesa, lahko pride tudi pri pravilno delujočih vezjih do občutnih odstopanj v velikosti električnih tokov v vezju. Posledica je maskiranje napak v vezju, čemur se lahko izognemo s ponovitvami meritev napajalnega toka ob vhodnih signalih nasprotne polaritete. Možna rešitev je tudi realizacija dodatnih struktur v nekaterih tipičnih analognih podsklopih. Avtorji v /8/in /9/tako predlagajo izvedbo dodatnih tokovnih zrcal v transkonduktančnih operacijskih ojačevalnikih (OTA), slika 2, s katerimi omogočimo meritev mirovnega toka analognega vezja z zunanjimi merilnimi instrumenti ali z vgrajenimi tokovnimi senzorji.



Slika 1: DfT tehnike za mešana analogno-digitalna integrirana vezja

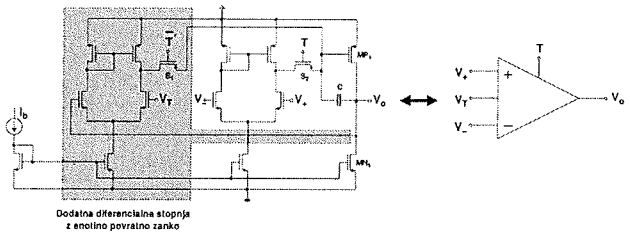


Slika 2: Dodatna tokovna zrcalna struktura v simetričnem OTA

3.3 Dostop do globoko vgnezdenih podsklopov

V to skupino DfT tehnik uvrščamo načrtovalske ukrepe za izboljšanje vodljivosti in spremljivosti analognih podsklopov. V pretežno digitalnih mešanih integriranih vezjih za dostop do analognih podsklopov pogosto uporabljamo obstoječe A/D in D/A pretvornike. Takšen pristop omogoča popolnoma digitalno povezavo med preizkuševalno napravo in preizkušanim vezjem /10/, kar bistveno poenostavi celoten postopek preizkušanja. Kadar obstoječe zmogljivosti ne zadoščajo, je potrebno realizirati namenske A/D ali D/A pretvornike izključno za potrebe preizkušanja, to pa lahko pomeni občutno povečanje polprevodniške površine. Možna je tudi realizacija posebnih kontaktnih ploskev na polprevodniku, ki merilni napravi omogočajo dostop do izbranih vozlišč integriranega vezja. Uporaba te tehnike je težavna in zahteva uporabo dragih preizkuševalnih vmesnikov, vendar pa je včasih edina možna rešitev. V tem primeru skušamo kontakte realizirati na najmanj občutljivih vozliščih vezja, kot so izhodi ojačevalnikov ter druga nizko impedančna vozlišča.

V literaturi so bili predstavljeni tudi različni pristopi, ki temeljijo na rekonfiguraciji posameznih analognih podsklopov. Ena izmed tehnik temelji na t.i. sw-opamp strukturah /11/. Pri teh gre dejansko za operacijske ojačevalnike, ki lahko delujejo v normalnem načinu, ali pa kot ojačevalniki z enotnim ojačanjem in dodatnim vhodom. Prednost pristopa je v majhnem vplivu preizkusne infrastrukture na prenosno funkcijo analognega vezja. Kot je razvidno iz slike 3 so stikala, s katerimi lahko analogni podsklop izoliramo od okolice ter zagotovimo dostop do njegovega vhoda oz. izhoda, nameščena med diferencialno vhodno in močnostno izhodno stopnjo ojačevalnika. Zaradi majhnih amplitud signala lahko uporabimo MOS tranzistorje majhnih dimenzij, s čemer se zmanjša vpliv parazitnih kapacitivnosti na karakteristiko ojačevalnika. Avtorji so v /12/predlagali zamenjavo vseh operacijskih ojačevalnikov v večstopenjskem analognem vezju s sw-opamp strukturami. Če vse stopnje, razen trenutno preizkušane, obratujejo v načinu enotinega ojačevalnika, se vzpostavi posredna povezava med primarnim vhodom/izhodom vezja in vhodom/izhodom preizkušane stopnje. Na različnih primerih so tudi pokazali, da je vpliv preizkusne infrastrukture na prenosno funkcijo vezja minimalen.



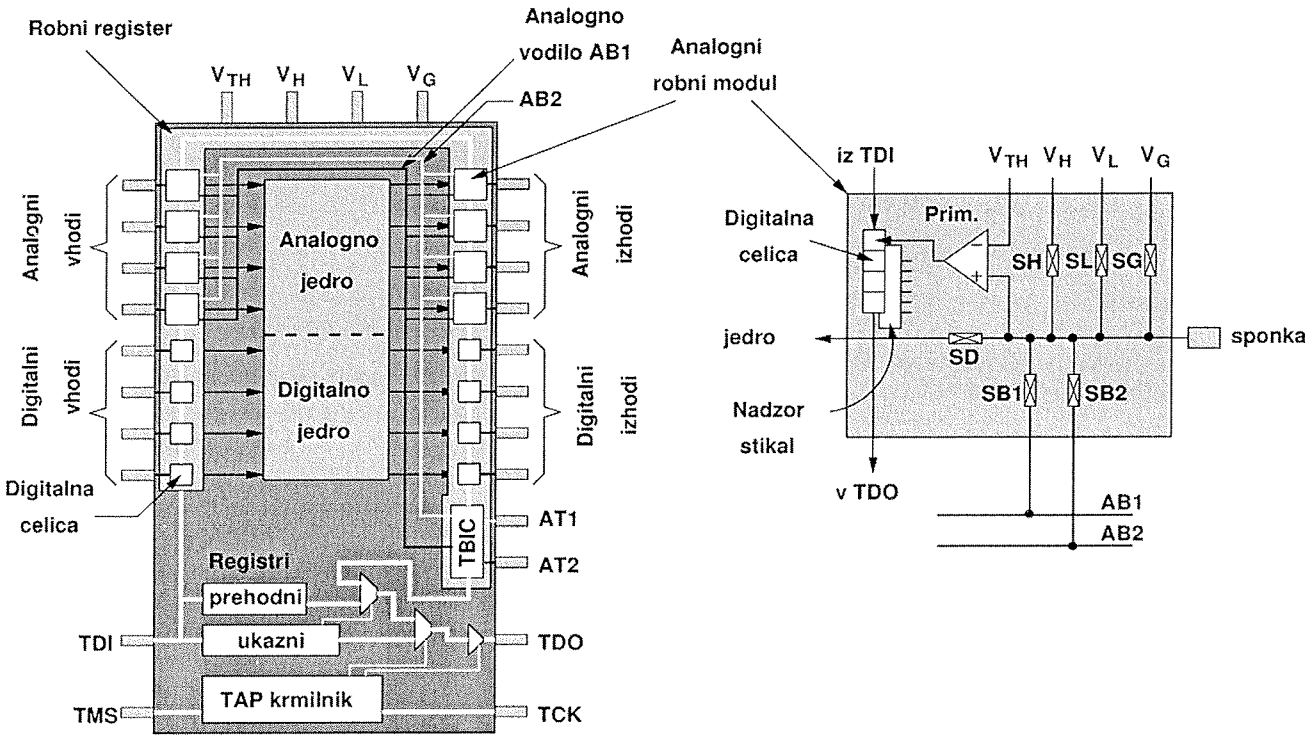
Slika 3: operacijski ojačevalnik z možnostjo rekonfiguracije (sw-opamp)

Podobno rešitev, ki temelji na rekonfiguraciji posameznih stopenj analognega filtra v navadne ojačevalne stopnje, predlagajo tudi avtorji v /13/. Ker je v tem primeru rekonfiguracija izvedena s stikali v osnovni poti signala, je lahko vpliv nelinearnih upornosti in parazitnih kapacitivnosti stikal na prenosno funkcijo sistema precejšen. Takšna rešitev zato zahteva podrobno analizo in upoštevanje vpliva stikal že med postopkom načrtovanja osnovnega analognega vezja.

Med pogosteje uporabljane tehnike sodi realizacija namenskih preizkusnih analognih vodil. Načrtovalci z realizacijo le-teh omogočijo vodljivost in spremljivost analognih vozlišč na nivoju integriranega ali tiskanega vezja oziroma na nivoju sistema. Čeprav je osnovni princip uporabe preprost, pa je dejanska izvedba precej zahtevna. Pri načrtovanju tovrstnih struktur zato uporabljajo različne tehnike, kot so diferencialna vodila, vgrajeni gonilniki signalov (prilagoditev na impedanco oz. kapacitivno obremenitev vodila), ločevanje vodil za različne analogne podsklope (NF, RF) ter ozemljene oklopne plasti nad in pod vodili, ki lahko pripomorejo k zmanjšanju motenj v merilnem postopku. Pri načrtovanju pa je pomembna tudi uporaba standardnega preizkusnega vmesnika, ki lahko precej olajša pripravo potrebnega merilnega okolja in prenosljivost obstoječih preizkusnih programov na nove aplikacije.

3.4 Standard IEEE 1149.4

Konec leta 1999 je bil dokončno potrjen industrijski standard IEEE 1149.4 za mešano preizkusno vodilo (ang. *Mixed-Signal Test Bus*, /14/), ki se navezuje na že obstoječi in v praksi uveljavljeni standard za načrtovanje digitalnih vezij z robno preizkusno linijo (IEEE 1149.1 - *Test Access Port and Boundary-Scan Architecture*). Standard določa lastnosti analognega preizkusnega vodila in predpisuje osnovno preizkusno infrastrukturo sistema (slika 4). Bistvena značilnost standarda so t.i. analogne robne celice (ang. *Analog Boundary Module* - ABM), ki so nameščene med funkcionalne priključke analognega jedra in vhodne/izhodne sponke vezja ter omogočajo povezavo analognih vozlišč z zunanjimi merilnimi instrumenti brez uporabe občutljivih merilnih sond. Standard poleg analogne infrastrukture predpisuje tudi obvezno krmilno logiko in osnovne načina delovanja analognih robnih celic. Poleg tega dopušča tudi različne razširitve infrastrukture, npr. z vgradnjo struktur za izvedbo analognega samodejnega preizkusa.



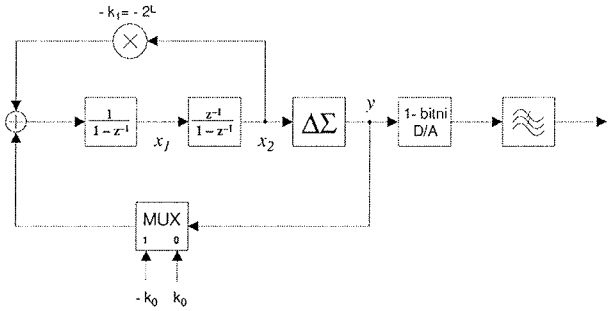
Slika 4: arhitektura IEEE 1149.4 mešanega preizkusnega vodila

Upoštevanje standarda omogoča bolj strukturiran pristop k načrtovanju preizkusljivih mešanih analogno-digitalnih vezij, vendar pa ima predlagana infrastruktura tudi nekatere slabosti. Med temi sta relativno omejeno frekvenčno in impedančno merilno območje, ki sta določeni predvsem z načinom izvedbe vgrajenega analognega vodila in pripadajočih analognih stikal v robnih celicah. Izbira najustreznejše tehnike je zato prepuščena načrtovalcu, ki mora pri tem upoštevati vpliv dejavnikov, kot so končne upornosti in parazitne kapacitivnosti MOS stikal, ali pa enosmerna odstopanja (*offset*) ojačevalnikov, tako na natančnost meritev kot na osnovne parametre analognega vezja.

3.5 Generiranje in vrednotenje analognih signalov v vezju

Generiranje in vrednotenje analognih signalov z zunanjo merilno opremo vnaša nekatere omejitve v postopek preizkušanja vezij. Te so posledica omejenega frekvenčnega ali amplitudnega območja signalov, ki jih lahko prenašamo med merilnimi napravami ter integriranim vezjem (oziroma vhodi in izhodi vgnezdenih analognih podsklopov), občutljivosti prenosnih poti signalov na motnje ipd. Možno rešitev tega problema predstavlja generiranje oziroma vrednotenje analognih signalov v samem integriranem vezju. V tem primeru poteka prenos preizkusnih podatkov in merilnih rezultatov med vezjem in zunanjo preizkuševalno napravo v digitalni obliki. Ceno za možnost uporabe preprostejših digitalnih preizkuševalnih naprav plačamo z dodatno površino polprevodnika, ki je potrebna za realizacijo ustreznih analognih preizkuševalnih struktur v samem integriranem vezju.

Izbira generatorja signala je odvisna od vrste preizkusa, ki ga želimo opraviti. Medtem, ko za preizkus določenih tipov vezij, kot so npr. analogno/digitalni (A/D) pretvorniki zadošča en sam vhodni signal, pa pri vezjih, kot so analogni filtri, običajno uporabljamo postopek preizkušanja z večfrekvenčnimi vhodnimi signali. Haurie in Roberts sta v /15/predstavila izvedbo sinusnega oscilatorja, ki temelji na LDI (ang. *Lossless Discrete Integrator*) rezonatorju in ΔΣ modulatorju (slika 5). Oscilator je možno skoraj v celoti realizirati z relativno preprostimi digitalnimi elementi, kot so registri, seštevalniki, multiplekserji in pomikalni registri, medtem ko je uporaba analognih struktur omejena na 1-bitni digitalno/analogni (D/A) pretvornik (zadrževalnik ničtega reda) in preprost nizkoprepustni filter. Predlagano strukturo odlikuje visoko razmerje signal/šum (ang. *Signal to Noise Ratio* - SNR) kot tudi možnost generiranja večtonskih signalov.



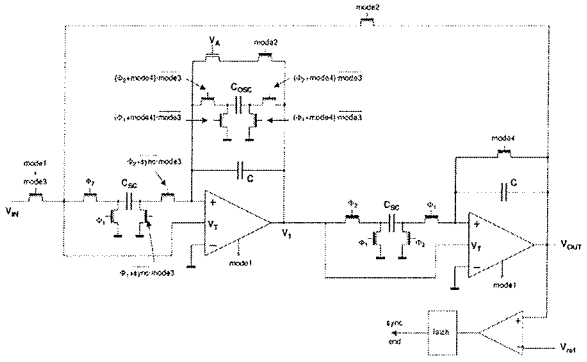
Slika 5: Generator sinusnega signala na osnovi DS modulatorja

Preizkus A/D pretvornikov običajno obsega določitev integralne (INL) in diferencialne nelinearnosti (DNL) ter napake

ojačanja in enosmernega odstopnaja pretvornika. Te parametre lahko določimo z analizo v frekvenčnem ali v časovnem prostoru kar vpliva tudi na izbiro oblike vhodnega signala. Pri meritvah v časovnem prostoru želimo na vhodu pretvornika uporabiti počasen, linearno naraščajoči signal. Primer realizacije generatorja tovrstega signala je predstavljen v /16/. Pri histogramskem (frekvenčnem) preizkusu /17/beležimo število ponovitev posameznih digitalnih kod na izhodu pretvornika ob periodičnem vhodnem signalu z znano amplitudno distribucijo, npr. sinusnemu ali trikotnemu signalu /18/.

Vrednotenje odziva analognega vezja otežuje vsebovana nenatančnost analognih signalov. Zaradi tega moramo pri analizi odziva vezja na dani vhodni signal upoštevati vplive šuma in odstopanj v generatorju signala kot tudi dopustnih odstopanj parametrov preizkušanega vezja. Včasih lahko pri vrednotenju odziva preizkušanih podsklopov izkoristimo obstoječe D/A pretvornike in DSP jedra v integriranem vezju /19/, /20/. Kadar to ni možno, je potrebno realizirati namenske preizkusne zmogljivosti, pri čemer pa skušamo čim bolj omejiti potrebno površino polprevodnika /21/. Realizacija A/D pretvornika visoke časovne in amplitudne resolucije je običajno v nasprotju z zahtevo po majhni površini: na eni strani poznamo hitre a velike *flash* A/D pretvornike, na drugi pa počasne pretvornike na osnovi sukcesivne aproksimacije, ki sicer zasedejo manjšo površino polprevodnika. Pod določenimi pogoji pa je možno realizirati pretvornike, pri katerih resolucija ni obratno sorazmerna hitrosti pretvorbe. Avtorji v /22/in /23/tako izkoriščajo periodičen odziv analognega vezja, ki tudi počasnim sukcesivnim A/D pretvornikom omogoča doseganje časovne resolucije, ki je primerljiva tistim pri veliko višjih frekvencah vzorčenja. Poleg klasičnih A/D pretvornikov lahko za analizo preizkušanega vezja uporabimo tudi druge strukture. Eno izmed možnosti predstavljajo t.i. analogni nadzorniki (ang. *analogue checker*). S pomočjo le-teh preverjamo določene parametre vezja glede na znan vhodni signal. Nadzorniki iz odziva vezja izločijo vrednost iskanega parametra in jo primerjajo z dvema referenčnima vrednostima (P_{MIN} , P_{MAX}), ki ustrezata zgornji in spodnji meji dopustnega odstopanja parametra od željene vrednosti, rezultat pa je preprost digitalni signal, ki javi prisotnost napake (go/no-go preizkus). Analogni nadzorniki običajno sestojijo iz vezja za izločanje iskanega parametra in pripadajočega primerjalnika, vendar pa se dejanska izvedba nadzornika razlikuje glede na vrsto obravnavanega analognega vezja, /24/, /25/, /26/.

Ker je v praksi nemogoče ločeno primerjati vsako vzorčeno vrednost izhodnega signala z željeno vrednostjo, uporabljamo postopke komprimiranja analognih signalov. Želena lastnost struktur za komprimiranje analognih signalov je, da za dva različna vhodna signala ustvarijo dve različni signaturi, hkrati pa za dopustna odstopanja vhodnega preizkusnega signala tudi signatura ostaja v mejah pričakovanega območja. čeprav je mogoče signaturo določiti s klasično A/D pretvorbo izhodnega signala in uporabo digitalnih tehnik komprimiranja z večvhodnimi signaturnimi registri (ang. *Multiple Input Signature Register* - MISR), so se nekatere druge strukture, /27/, /28/, izkazale za učinkovitejše glede na potrebno površino polprevodnika. V /29/so avtorji predstavili izvedbo generatorja analogne signature, v SC (ang. *Switched-Capacitor*) tehnologiji, ki lahko hkrati služi tudi kot generator preizkusnih signalov (slika 6). Potrebno površino polprevodnika lahko dodatno zmanjša souporaba funkcionalnih elementov vezja v preizkusni shemi.



Slika 6: ABILBO - vgrajen observator analognih blokov

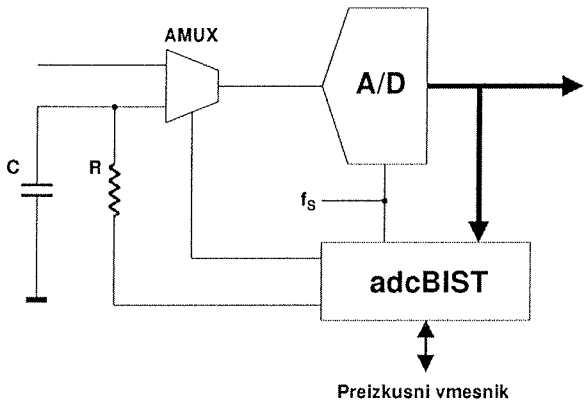
3.6 Vgrajen samodejni preizkus

Z vgradnjo ustreznih zmogljivosti v integrirano vezje lahko omogočimo popolnoma avtonomno izvajanje preizkusnega postopka, ki ne zahteva nobene dodatne podpore s strani zunanje merilne opreme, z izjemo proženja začetka in spremljanja končnega rezultata preizkusa. Prednost takšnega pristopa je v zmanjšanju kompleksnosti (in cene) zunanje preizkuševalne naprave in možnosti sočasne izvršitve več ločenih vgrajenih preizkusov ter posledično skrajšanju časa celotnega preizkusa. Slabost je vsekakor povečanje polprevodniške površine vezja zaradi dodatne preizkusne infrastrukture ter omejena možnost obdelave analognih signalov. Pristopi k izvedbi vgrajenega samodejnega preizkusa analognih podsklopov se razlikujejo predvsem glede na njihov vpliv na funkcionalne elemente vezja ter glede na tehniko generiranja preizkusnih signalov in vrednotenja odziva preizkušanega analognega vezja. Razlikujemo lahko tudi med bolj ali manj strukturiranimi pristopi k načrtovanju BIST struktur. Prvi so bolj splošne narave in pripomorejo k skrajšanju načrtovalskega časa, običajno na račun večje potrebne površine polprevodnika. Nestrukturirani pristopi so prilagojeni specifičnim analognim vezjem in lahko ob manjši dodatni površini polprevodnika občutno izboljšajo preizkusljivost vezja. Prilagoditev struktur specifičnemu vezju po drugi strani zahteva daljši čas načrtovanja.

Največ pozornosti je bilo do sedaj posvečene izvedbi BIST struktur za A/D in D/A pretvornike, /31/, /32/, /33/, saj gre za pogosto uporabljane mešane analogno-digitalne podsklope s širokim naborom parametrov (ojačanje, INL, DNL, enosmerno odstopanje), ki po drugi strani zahtevajo obsežen in drag postopek preizkušanja. Primer strukturiranega pristopa k preizkušanju vezij, ki vsebujejo tako A/D kot D/A pretvornike je t.i. hibridni BIST (HBIST), ki ga je v /30/predlagal Ohletz. Samodejni preizkus se izvede z vz-

postavitvijo povezave med izhodom D/A in vhodom A/D pretvornika, medtem ko vhode D/A pretvornika vzbujajo vzorci iz vgrajenega LFSR (ang. *Linear Feedback Shift Register*) generatorja psevdo-naključnih vrednosti. Sočasno se v digitalni domeni izvaja analiza signature na izhodih A/D pretvornika.

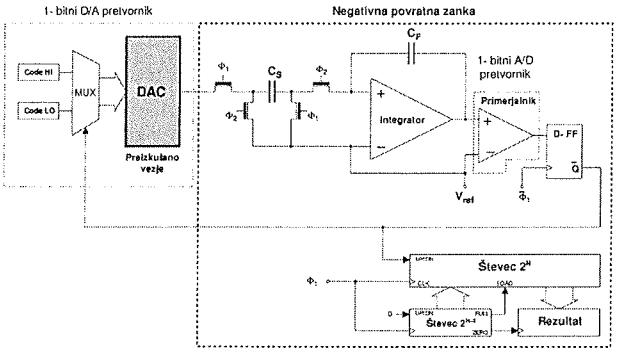
Med analognimi BIST pristopi velja posebej omeniti komercialne rešitve podjetij LogicVision ter Fluence Technology. Avtorja Sunter in Nagi iz podjetja LogicVision sta razvila adcBIST tehniko namenjeno preizkušanju A/D pretvornikov /34/, ki zahteva uporabo nekaterih dodatnih elementov: analognega multiplekserja na vhodu pretvornika, R-C vezja za glajenje vhodnega signala ter digitalnega bloka za generiranje preizkusnih vrednosti in procesiranje rezultatov pretvorbe. Elemente vključujemo v načrtovano vezje na nivoju blokov, zato pristop ne zahteva posegov v strukturo A/D pretvornika (slika 7). Digitalno vezje skrbi za generiranje vhodnega preizkusnega signala in za izračun koeficentov polinoma tretjega reda. Slednji so določeni na podlagi najmanjše vsote kvadratov tako, da zagotavljajo prileganje polinoma dani sekvenci izhodnih vrednosti pretvornika. Koeficienti vsebujejo vso potrebno informacijo za določitev enosmernega odstopanja, ojačanja ter harmoničnega popačenja drugega in tretjega reda. Izračun parametrov se izvede digitalno in lahko poteka v ali izven integriranega vezja. Prednost pristopa je njegova odpornost na šum, variacije v proizvodnem procesu in nelinearnosti na vhodu pretvornika, med slabosti pa sodi predvsem ne-izračunavanje dinamične in integralne nelinearnosti pretvornika. Poleg adcBIST ponujajo pri LogicVision tudi rešitev za preizkušanje digitalnih in analognih PLL struktur pod imenom pllBIST /35/.



Slika 7: Shematski prikaz adcBIST pristopa

Podjetje Fluence Technology trži skupino analognih BIST rešitev pod skupnim imenom BISTmaxx. Skupina proizvodov obsega strukture za preizkušanje A/D (ADCBIST) in D/A (DACBIST) pretvornikov ter PLL struktur (VCOBIST). Medtem ko ADCBIST temelji na vgradnji namenskih zmogljivosti, ki omogočajo izvedbo klasičnega histogramskega preizkusa, pa DACBIST uporablja t.i. oscilacijsko tehniko za določitev pomembnih parametrov preizkušanega vezja. Oscilacijska tehnika temelji na možnosti pretvorbe preizkušanega vezja v oscilator, /36/, /37/, in na predpostavki, da napake v vezju vplivajo na frekvenco oscilacij. Naravna frekvenca transformiranega vezja je tako odvisna od dodanih zunanjih komponent ter od večine parametrov, ki določajo frekvenčno karakteristiko oziroma časovni odziv vezja. DACBIST predvideva transformacijo D/A pretvornika poljubne resolucije v eno-bitni D/A pretvornik ter priključitev negativne regulacijske povratne zanke na preizkušano vezje. Frekvenco oscilacij določimo s preprostim vezjem, ki obsega eno-bitni A/D pretvornik (primerjalnik) in digitalni števec, preizkusna infrastruktura pa vključuje še integrator analognega signala in ustrezno krmilno logiko (slika 8). Nekaj dodatnih besed namenjamo oscilacijski metodi in njeni uporabi pri preizkušanju analognih filtrov v naslednjem poglavju.

Pri uporabi tehnik vgrajenega samodejnega preizkušanja analognih vezij lahko na koncu ugotovimo, da se s selitvijo preizkusnih zmogljivosti v samo integrirano vezje ustrezno povečuje tudi potrebna površina polprevodnika, kljub temu pa je za določene aplikacije to ena izmed ugodnejših rešitev, predvsem zaradi povečanja učinkovitosti preizkusnega postopka, skrajšanja časa preizkušanja vezja in pogosto tudi možnosti izvajanja preizkusov med obratovanjem sistema. Hkrati tudi trenutni trendi razvoja čedalje bolj nakazujejo potrebo po uporabi tovrstnih tehnik pri načrtovanju zanesljivih a cenovno ugodnih mešanih integriranih vezij in sistemov.



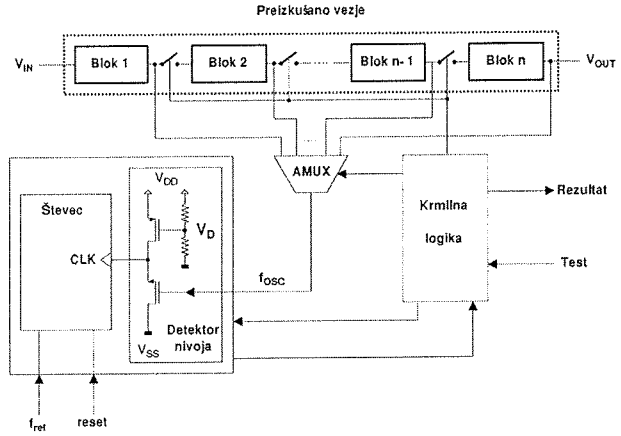
Slika 8: Primer izvedbe DACBIST strukture

3.7 Oscilacijska metoda

Oscilacijsko metodo /36/, /37/, /38/je možno uporabiti za preizkušanje različnih razredov analognih vezij. Pri tej metodi vzpostavimo pogoje, da vezje, ki ga želimo preizkusiti, zaoscilira. Izmerimo frekvenco oscilacij in jo primerjamo s frekvenco izmerjeno pod enakimi merilnimi pogoji na referenčnem vezju, za katerega vemo, da je brez napak. Ob predpostavki, da se morebitne napake v vezju odražajo v frekvenci oscilacij, tako lahko odkrivamo vezja z napakami. Splošni pristop k uporabi oscilacijske preizkusne metode je podan na sliki 9. Preizkušano vezje običajno delimo na manjše podsklope, znotraj katerih izvedemo ustrezne ukrepe za vzpostavitev nestabilnega stanja in posledično oscilacij na izhodu podsklopa.

Oscilacijska metoda je posebej privlačna za realizacijo vgrajenih samodejnih preizkusov saj običajno zahteva relativno

omejene posege v strukturo preizkušanega vezja, hkrati pa se izognemo potrebi po realizaciji namenskih struktur za generiranje preizkusnih signalov. Za vrednotenje odziva vezja pa zadošča že zelo preprosta struktura, ki jo lahko realiziramo z detektorjem nivoja analognega signala in digitalnim števcem.



Slika 9: Splošni pristop k uporabi oscilacijske metode

Preizkušanje analognih filtrov pogosto temelji na dinamičnih meritvah frekvenčnega odziva vezja na vhodni signal spremenljive frekvence. Učinkovitost takšnega postopka je v veliki meri odvisna od izbire ustrezne oblike vzbujanja ter načina vrednotenja odziva. V primeru načrtovanja vgrajenega samodejnega preizkusa zahteva realizacijo ustreznih namenskih struktur, ki lahko občutno povečajo potrebno površino polprevodnika, poleg tega večina aplikacij zahteva uporabo generatorjev analognih signalov visoke stabilnosti in možnost generiranja večfrekvenčnih signalov.

V zadnjih letih je bilo objavljenih več prispevkov, ki obravnavajo uporabo oscilacijske metode pri preizkušanju aktivnih analognih filtrov /38/. Predstavljene so bile nekatere rešitve za izbrane razrede aktivnih R-C filtrov, ki temeljijo na pretvorbi preizkušanega vezja v oscilatorsko strukturo s pomočjo vgrajenih stikal in dodatnih pasivnih elementov /39/, ali pa z uporabo zunanjega vezja, /40/. Poleg tega naletimo tudi na nekatere rešitve, ki obravnavajo specifična aktivna R-C vezja, /41/, /42/, in dokazujejo praktično uporabnost postopka v proizvodnem preizkušanju integriranih analognih filtrov.

Uporaba oscilacijske metode je še posebej smiselna v primeru preizkušanja SC vezij, saj le ta že v osnovi vključujejo analogna stikala, torej je vezje pogosto možno transformirati brez večjih posegov v strukturo samega vezja oziroma že z zagotovitvijo ustreznih (digitalnih) krmilnih signalov. Huertas et al. so v /43/in /44/predstavili preizkusni postopek za specifično SC filtrsko vezje, ki temelji na uporabi oscilacijske metode. Oscilacijska struktura je zasnovana z uporabo dodatnega zunanjega vezja, ki v preizkusnem načinu zagotavlja obratovanje preizkušanega pasovnoprepustnega SC filtra v mejno stabilnem območju. Na podlagi analize pokritosti napak so tudi ugotovili, da lahko kakovost preizkusa izboljšajo z dodatnim preverjanjem amplitude izhodnega signala. V /45/je predlagana rekonfiguracijska shema oscilacijskega preizkusa pasovnoprepustne SC stopnje, ki se nanaša na univerzalno Fleischer-Laker-jevo stopnjo drugega reda. Delo predstavlja posplošen pristop k načrtovanju struktur za izvedbo oscilacijskega preizkusa v tipičnih topologijah SC filtrskih stopenj.

4 Zaključek

Reševanje problema preizkušanja je tesno povezano s postopkom načrtovanja vezja. Z upoštevanjem pravil, postopkov in tehnik načrtovanja, ki jih skupno označujemo kot načrtovanje preizkusljivosti, lahko bistveno olajšamo izvedbo in povečamo učinkovitost preizkusnega postopka. Na področju načrtovanja preizkusljivosti v mešanih analogno-digitalnih integriranih vezjih so bile v preteklih letih predstavljene številne rešitve, vendar pa so se le redke uveljavile v praksi. Posamezne tehnike se po svoji zasnovi precej razlikujejo, vendar jih lahko v grobem razdelimo na načrtovanje struktur za podporo zunanjim merilnim metodam in na načrtovanje struktur za izvedbo vgrajenega samodejnega preizkusa vezja. Cilj našega prispevka je bil predstaviti glavne sodobne že uveljavljene preizkusne metode, hkrati pa pokazati tudi na nekatere zanimive ideje in izhodišča za razvoj novih učinkovitih rešitev.

5 Literatura

/1/ G.W. Roberts, "Metrics, Techniques and Recent Developments in Mixed-Signal Testing", Proc. IEEE/ACM Int'l Conference on Computer Aided Design, San Jose, CA, USA, 1996, pp. 514-521

/2/ G.W. Roberts, "Improving the Testability of Mixed-Signal Integrated Circuits", Proc. IEEE Custom Integrated Circuits Conference, Santa Clara, CA, USA, 1997, pp. 214-221

/3/ R. Spina, and S. Upadhyaya, "Test Time Versus Design-for-Test Resources in Mixed-Signal Systems", Proc. IEEE International Mixed-Signal Testing Workshop (IMSTW'96), Quebec City, Canada, 1996, pp. 173-180

/4/ A. Lechner, M. Burbridge, A. Richardson, B. Hermes, "3DB Challenge for DfT, DfM, DOT & BIST Integration into Analogue and Mixed Signal ICs", Proc. IEEE Latin-American Test Workshop, Cancun, Mexico, 2001, pp. 194-199

/5/ Semiconductor Industry Association, International Technology Roadmap for Semiconductors, Edition 2003

/6/ J.A. Prieto, A. Rueda, I. Grout, E. Peralias, J.L. Huertas, A.M. Richardson, "An Approach to Realistic Fault Prediction and Layout Design for Testability in Analogue Circuits", Proc. Design, Automation and Test in Europe Conference (DATE'98), Paris, France, 1998, pp. 905-912

/7/ J.M. Soden, "IDDQ Testing: A Review", Journal of Electronic Testing: Theory and Applications, No. 3, 1992, pp. 291-303

/8/ I. Baturone, J.L. Huertas, S.Sanchez Solano, and A.M. Richardson, "Supply Current Monitoring for Testing CMOS Analog Circuits", XI Congreso de Diseño de Circuitos Integrados y Sistemas, Barcelona, Spain, 1996, pp. 231-236

/9/ I. Baturone, S. Sanchez Solano, A.M. Richardson, and J.L. Huertas, "Current-Mode Techniques for Self-Testing Analogue Circuits", Proc. IEEE International Workshop on IDDQ Testing, Washington D.C., USA, 1997

/10/ J.S. Matos, A.C. Leao, J.C. Ferreira, "Control and observation of analog nodes in mixed-signal boards", Proc. IEEE Int'l Test Conference (ITC'93), Baltimore, USA, 1993, pp. 323-331

/11/ A.H. Bratt, A.M.D. Richardson, R.J.A. Harvey, and A.P. Dorey, "A design-for-test structure for optimising analogue and mixed signal IC test", Proc. European Design & Test Conference (ED&TW'95), Paris, France, 1995, pp. 24-32.

/12/ D. Vasquez, A. Rueda, J.L. Huertas, "A DfT methodology for active analogue filters", Proc. IEEE Mixed Signal Test Workshop (IMSTW'95), Grenoble, France, 1995

/13/ M. Renovell, F. Azais, Y. Bertrand, "A Design-for-Test Technique for Multi-Stage Analog Circuits", Proc. Asian Test Simposium (ATS'95), Bangalore, India, 1995, pp.113-118

/14/ IEEE Standard for a Mixed-Signal Test Bus, IEEE 1149.4-1999

//5/ X. Haurie, G.W. Roberts, "Arbitraty-Precision Signal Generation for Mixed-Signal Built-In-Self-Test", IEEE Tran. Circuits and Systems II: Analog and Digital Signal Processing, Vol. 45, No. 11, 1998, pp. 1425-1431

/16/ B. Provost, E. Sanchez-Sinencio, "Adaptive Analog Timer for On-Chip Testing", Proc. Int'l Workshop on Design of Mixed-Mode Integrated Circuits and Applications, Puerto-Vallarta, Mexico, 1999, pp. 29-32

/17/ F. Azais, S. Bernard, Y. Bertrand, M. Renovell, "Implementation of a Linear Histogram BIST for ADCs", Proc. Design Automation and Test in Europe Conference (DATE'01), Munich, Germany, 2001, pp. 590-595

/18/ S. Bertrand, F. Azais, Y. Bertrand, M. Renovell, "A High Accuracy Triangle-Wave Signal Generator for On-Chip ADC Testing", Proc. European Test Workshop (ETW'02), Corfu, Greece, 2002, pp. 365-370

/19/ M.F. Toner, G.W. Roberts, "A BIST Scheme for a SNR, Gain Tracking and Frequency Response Test of a Sigma-Delta ADC", IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, Vol. 42, No. 1, 1995, pp. 1-15

/20/ E.K.F. Lee, "Reconfigurable Data Converter as a Building Block for Mixed-Signal Test", Proc. European Design & Test Conference (ED&TW'97), Paris, France, 1997

/21/ M. Renovell, F. Azais, S. Bernard, Y. Bertrand, "Hardware Resource Minimization for Histogram-based ADC BIST", Proc. VLSI Testing Symposium (VTS'00), Montreal, Canada, 2000, pp. 247-252

/22/ K. Lofstrom, "Early Capture for Boundary Scan Timing Measurements", Proc. of the IEEE International Test Conference (ITC'96), Washington D.C., USA, 1996, pp. 417-422

/23/ A. Hajjar, G.W. Roberts, "A High Speed and Area Efficient On-Chip Analog Waveform Extractor", Proc. of the IEEE International Test Conference (ITC'98), Washington D.C., USA, 1998, pp. 688-697

/24/ R. Hajrani, B. Vinnakota, "Analog Circuit Observer Blocks", IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Processing, Vol. 44, No. 2, 1997, pp. 154-163

/25/ D. De Venuto, M.J. Ohletz, B. Ricco, "On-Chip Signal Level Evaluation for Mixed-Signal ICs using Digital Window Comparators", Proc. IEEE European Test Workshop (ETW'01), Stockholm, Sweden, 2001, pp. 175-179

/26/ C.C. Hsu, W.S. Feng, "OTA-C Based BIST Structure for Analog Circuits", IEICE Trans. Fundamentals, Vol. E83-A, No.4 April 2000, pp. 771-773

/27/ M. Renovell, F. Azais, Y. Bertrand, "On-Chip Analog Output Response Compaction", Proc. European Design & Test Conference (ED&TC'97), Paris, France, 1997

/28/ S. Saine, J. Raczkowycz, P. Mather, "An analogue test response compaction technique using delta-sigma modulation", Microelectronics Journal, Vol. 32, No.4, April 2001, pp. 339-350

/29/ M. Lubaszewski, S. Mir, L. Pulz, "ABILBO: Analog BuILt-in Block Observer", Proc. Int'l Conference on Computer-Aided Design (ICCAD'96), San Jose, CA, USA, 1996, pp. 600-603

/30/ M.J. Ohletz, "Hybrid built-in self-test (HBIST) for mixed analog/digital integrated circuits", Proc. European Test Conference (ETC'91), 1991, pp. 307-316

/31/ M.F. Toner, G.W. Roberts, "A BIST SCheme for a SNR, Gain Tracking, and Frequency Response Test of a Sigma-Delta ADC", IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Processing, Vol. 42, No. 1, 1995, pp. 1-15

/32/ J. Raczkowycz, S. Allott, "Embedded ADC characterization techniques using a BIST structure, an ADC model and histogram data", Microelectronics Journal, Vol. 27, No. 6, 1996, pp. 539-549

/33/ E. Teraoka, T. Kengaku, I. Yasui, K. Ishikawa, T. Matsuo, H. Wakada, N. Sakashita, Y. Shimazu, T. Tokuda, "A Built-In Self-Test for ADC and DAC in a Single-Chip Speech CODEC", IEICE Trans. Fundamentals, Vol. E80-A, No. 2, 1997, pp. 339-345

/34/ S. Sunter, N. Nagi, "A Simplified Polynomial-Fitting Algorithm for DAC and ADC BIST", Proc. IEEE Int'l Test Conference (ITC'97), Washington D.C., USA, 1997, pp. 389-395

/35/ LogicVision, PLL BIST Datasheet, http://www.logicvision.com/

/36/ K. Arabi, B. Kaminska, "Efficient and Accurate Testing of Analog-to-Digital Converters Using Oscillation-Tets Method", Proc. European Design & Test Conference (ED&TC'97), Paris, France, 1997, pp. 348-352

/37/ K. Arabi, B. Kaminska, "Oscillation Built-In Self-Test (OBIST) Scheme for Functional and Structural Testing of Analog and Mixed-Signal Integrated Circuits", Proc IEEE Int'l Test Conference (ITC'97), Washington D.C., USA, 1997, pp. 786-796

/38/ K. Arabi, B. Kaminska, "Testing Analog and Mixed-Signal Integrated Circuits Using Oscillation-Test Method", IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems, Vol. 16, No. 7, 1997, pp. 745-752

/39/ M. Santo-Zarnik, F. Novak, S. Maček, "Design of oscillation-based test structures for active RC filters", IEE Proc. Circuits, Devices and Systems, Vol. 147, No. 5, 2000, pp. 297-302

/40/ M. Santo-Zarnik, F. Novak, S. Maček, "Efficient Go No-Go Test of Active RC Filters", Int'l Journal of Circuit Theory and Applications, No. 26, 1998, pp. 523-529

/41/ M.W.T. Wong, "On Issues of Oscillation Test Methodology", IEEE Trans. Instrumentation and Measurement, Vol. 49. No. 2, 2000, pp. 240-245

/42/ K.Y. Ko, N.S. Gorla, M.W.T. Wong, Y.S. Lee, "Improving fault diagnostic resolution of an oscillation-based test methodology scheme for the treshold detector circuit", Int'l Journal of Electronics, Vol. 88, No. 2, 2001, pp. 175-187

/43/ G. Huertas, D. Vazquez, E. Peralias, A. Rueda, J.L. Huertas, "Testing Mixed-Signal Cores: Practical Oscillation-Based Test in an Analog Macrocell", Proc. Asian Test Symposium (ATS'00), Taipei, Taiwan, 2000, pp. 31-38

/44/ G. Huertas, D. Vazquez, A. Rueda, J.L. Huertas, "Oscillation-Based Test Experiments in Filters: a DTMF Example", IEEE Int'l Mixed Signal Testing Workshop, Whistler, Canada, 1999, pp. 249-253

/45/ U. Kač, F. Novak, "all-pass SC biquad reconfiguration scheme for oscillation based analog BIST", Proc. IEEE European Test Symposium 2004, Ajaccio, France, pp. 133-138.

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OPTIMIZATION OF INTEGRATED CIRCUITS BY MEANS OF SIMULATED ANNEALING

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Key words: parametric optimization, simulated annealing, design of integrated circuits.

Abstract: The purpose of this paper is to test the efficiency of the modified orthogonal simulated annealing algorithm. The method is compared with the COMPLEX method on a set of mathematical functions. The method is then used on three real-world cases of integrated circuits and compared with a modified COMPLEX method that uses intelligent initial points selection.

Optimizacija integriranih vezij z algoritmom simuliranega ohlajanja

Kjučne besede: parametrična optimizacija, simulirano ohlajanje, načrtovanje integriranih vezij.

Izvleček: Namen prispevka je preizkusiti učinkovitost modificiranega ortogonalnega simuliranega ohlajanja. Primerjamo ga z metodo COMPLEX na skupini matematičnih funkcij. Metoda je nato uporabljena na treh realnih primerih integriranih vezij in primerjana z modificirano metodo COMPLEX, ki uporablja pametno izbiranje začetnih točk.

1 Introduction

Optimization problems arise in virtually every field of engineering, science, and business. The parametric optimization problems are usually presented in the following form:

$$\begin{aligned} &\min_{\underline{x}\in R^n} f(\underline{x}) \\ &f: R^n \rightarrow R \\ &\underline{x} \in [\underline{L}, \underline{U}] \end{aligned} \tag{1}$$

where f is the so-called cost function (CF) and $\underline{x}$ is a vector of parameter values. $\underline{L}$ and $\underline{U}$ are vectors of lower and upper parameter bounds, respectively. Unfortunately analytical solutions to (1) can only be obtained for some very simple and small problems. Most practical problems are complex and often include simulations and measurements, which are very expensive and time consuming. The complexity of the optimization problem depends on the dimensionality (i.e. the number of optimization parameters) and on the shape of the CF. The size of the solution space increases exponentially with the problem dimensionality, so locating good solutions becomes increasingly more difficult. But the real challenge arises from the CF itself. In most real-world applications the CF is nonlinear and has many local minima. Often the value of the CF is a result of numerical simulations or measurements that introduce noise to the CF. Noise makes the fast deterministic gradient based methods useless and derivative free direct methods become more attractive. Direct methods are usually divided in two major groups. Deterministic methods always produce the same final solution when they start with the same initial guess. One method from this group is the simplex method which is well known and popular due to its simplicity and speed. But the simplex method is a local downhill search method and its solution greatly depends on the initial guess. Stochastic methods, on the other hand, introduce randomness to the search process and are capable of escaping from the local minima in order to find better solutions. Simulated annealing is a stochastic method. In this paper we describe a recent version of simulated annealing referred to as Orthogonal Simulated Annealing (OSA) /1/ and compare it with a modified simplex method also known as COnstrained siMPLEX (COMPLEX) /2/. The comparison is done on a set of mathematical test functions. OSA and modified COMPLEX methods are then used on three real-world integrated circuit (IC) design problems. The purpose of comparison is to establish the feasibility of circuit optimization with OSA.

The paper is organized as follows. In section 2 a brief description of the basic simulated annealing algorithm is given and in section 3 the OSA algorithm is described in detail. Section 4 compares the algorithm with the COMPLEX method on a set of mathematical test functions. In section 5 OSA is compared with a modifed COMPLEX methods on three cases of IC design. Section 6 gives the conclusions.

2 Simulated annealing algorithm

Downhill methods can easally get trapped in local minima. To escape from a local minimum uphill moves must be allowed from time to time to give the algorithm a chance to move to unexplored parts of the solution space. Simulated

annealing /3/ was developed for this purpose. It always accepts downhill moves but occasionally uphill moves are also accepted. The basic features of the algorithm come from the analogy with the movement of atoms in metal. When metal is heated up to a very high temperature, atoms can move freely even to a state with higher energy. When the material is cooled down slowly, atoms are more likely to move to low energy states. If the annealing is slow enough, the resulting metal has an uniform structure with very few defects and minimal free energy. The simulated annealing method mimics this process by introducing an artifical parameter to the search process often referred to as the temperature (T) which controlls the acceptance probability for the uphill moves. At the beginning of the search it is set to a high value and most transitions to higher CF values are accepted. As the search progresses, the temperature is slowly decreased so that the uphill moves become less frequent. If the annealing is done in a sufficiently slow manner, the final solutions reached by the algorithm are near the global minimum of the CF. The CF is an analogy of the free energy of the atoms in a metal. The basic steps of the simulated annealing algorithm are:

1. initialize - set algorithm parameters, inital point
2. generate new point - generation mechanism
3. acceptance criterion - transition
4. continue with 2 until end of temperature stage
5. annealing - cooling schedule (decrease temperature)
6. continue with 2 until stopping condition is met

These steps must be chosen carefully in order to ensure the probabilistic convergence to the global optimum. The obtained algorithms, however, are not very efficient in practice because the required cooling schedules are too slow or the generation mechanisms are too inefficient to get any useful result in a reasonable amount of time. That is why most practical versions of the algorithm use modified generation mechanisms and cooling schedules. This way the convergence proofs (i.e. /5/) no longer apply but good solutions can still be obtained in a reasonable amount of time.

3 Orthogonal simulated annealing algorithm (OSA)

Recently a new version of the simulated annealing algorithm was developed /1/, taking advantage of a carefully designed set of experiments at every iteration that helps to choose a good point for the next iteration. Since the results reported in /1/ were encouraging, this method was chosen for implementation and testing. All steps of the algorithm are described in this section.

3.1. Initialization

In the initialization step basic algorithm parameters are set. For this purpose several points (in our case 100) are randomly chosen and evaluated. The best of these points is set as the starting point for the algorithm. The initial value of the temperature parameter T is set to the standard deviation of CF values at these points. Our method differs slightly from the original one /1/. Instead of using the same parameter (temperature) for the acceptance criterion and the generation meachanism we use a separate parameter for generation of random moves. The allowed intervals /$\underline{L}$, $\underline{U}$/ for different optimization variables can vary considerably so the generation mechanism must use a separate parameter for each variable. For this reason we introduce another vector parameter referred to as the range ($\underline{R}$). The initial values of the components of $\underline{R}$ are set to allowed interval widths of optimization variables. Another parameter that needs to be set is the number of moves at each temperature stage N_t. In theory it must be large enough for the algorithm to reach thermal equlibrium in every temperature stage. In our case N_t is set to 10.

3.2. Generation mechanism

The algorithm uses orthogonal experimental design (OED) to choose good candidates for the next iteration. A carefully designed set of experiments allows for an efficient factor analysis. The main idea is to evaluate a small number of points in order to estimate factor effects on the given CF. The selection of these points is done with the help of orthogonal arrays. In this context orthogonal means statistically independent so that the estimation of the effect of one factor does not affect the estimation of the effects of others. An example of such an experimental design for three factors and three levels per factor is given in table 1, which contains the generated orthogonal array and figure 1, which shows the distribution of the corresponding experimental points.

Table 1: Orthogonal array for 3 factors and 3 levels per factor.

experiment number	factor 1 level	factor 2 level	factor 3 level
1	1	1	1
2	1	2	2
3	1	3	3
4	2	1	2
5	2	2	3
6	2	3	1
7	3	1	3
8	3	2	1
9	3	3	2

There is a total of $Q^{N_f} = 3^3 = 27$ combinations of factor levels for this example, where Q is the number of levels per factor and N_f is the number of factors. In our case only nine experimental points have to be evaluated and the use of the orthogonal array assures that these points are evenly spread around the search space. The algorithm for generation of orthogonal arrays can be found in /4/.

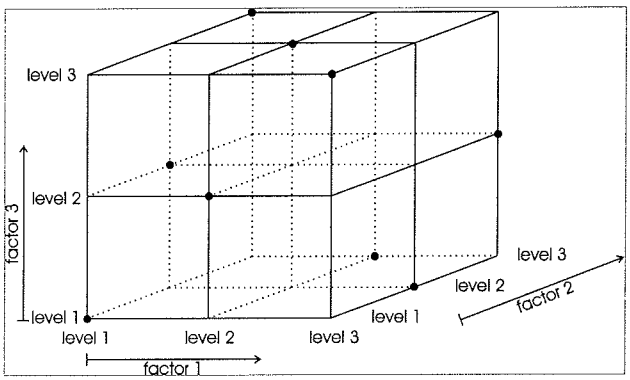

Fig. 1: Distribution of experimental points when the orthogonal array from Table 1 is used.

The use of orthogonal arrays also has drawbacks. The method works very well when there are no interactions between different factors. Unfortunately this is usually not the case. Furthermore optimization problems often include many optimization variables so the number of required experiments for an efficient factor analysis is large. Therefore the N_v variables are randomly grouped into N_f factors. The two most extreme cases are when $N_f = N_v$ and $N_f = 1$. In the former case there are many factors but because of the interaction effects between factors, the estimation of factor effects is less accurate. In the latter case there is only one factor and the estimated effect is accurate, but the optimization requires more iterations. A compromise is needed. The formula for determining the number of factors for a given problem is:

$$N_f = \left(3^{\lfloor \log_3(2 \cdot N_v + 1) \rfloor} - 1\right)/2 \tag{2}$$

At the beginning of every iteration the variables are randomly divided into N_f groups and every group is considered as one factor. Then a random perturbation vector is generated according to a specified probability distribution (in our case the Cauchy distribution). For every optimization parameter x_i the probability distribution of perturbation dx_i is:

$$p(dx_i) = \frac{R_i}{\pi\left(R_i^2 + dx_i^2\right)}, \quad i = 1,2,...N_v \tag{3}$$

where R_1 is the range parameter of the i-th variable in the current temperature stage. To generate a random variable from this distribution the inversion method is used:

$$dx_i = R_i \cdot \tan\left(\pi \cdot (U - 1/2)\right), \quad i = 1,2,...N_v \tag{4}$$

where U is an uniformly distributed random number from the interval /0,1/. After generating the perturbation vector $\underline{dx}$, the three levels for every optimization variable are determined as:

$$\begin{aligned} x_i^0 &= x_i^c \\ x_i^1 &= x_i^c + dx_i, \quad i = 1,2,...N_v \\ x_i^2 &= x_i^c - dx_i \end{aligned} \tag{5}$$

where x_i^c is the current value of the i-th variable. If x_i^1 or x_i^2 violates box-constraints /L_i, U_i/, its value is chosen randomly from this interval. Since variables are grouped into factors, setting one factor to some level means setting all the variables x_i from that factor to the corresponding level (x_i^0, x_i^1 or x_i^2). This way the orthogonal array is converted into experimental points, which are then evaluated. The main effects of all factor levels are obtained by the following formula:

$$S_{j,k} = \sum_t y_t \cdot F_t \tag{6}$$

where $S_{j,k}$ denotes the effect of the k-th level of the j-th factor and y_t is the value of the CF from the t-th experiment. F_t has only two possible values. It is 1 if in the t-th experiment the j-th factor has k-th level. Otherwise F_t is 0. The new candidate solution can now be generated. For every factor (j) the level (k) with the minimum $S_{j,k}$ is chosen. The CF of the new candidate solution is then evaluated. The best of all the experimental points and the candidate solution is then submitted to the acceptance criterion as a potential solution for the next iteration. This process is repeated N_t times in every temperature stage.

3.3. Acceptance criterion

Most versions of the simulated annealing algorithm use the same transition acceptance criterion which is known as the Metropolis criterion. Downhill transitions are allways accepted. Uphill transitions are accepted with the probability:

$$P = e^{\left(-\frac{y'-y}{T}\right)} \tag{7}$$

where y' and y are the CF values at the new and the current point, respectively, and T is the value of the temperature parameter. At high temperatures almost all transitions are accepted but when the temperature is close to zero most of the uphill moves are rejected and the algorithm acts as a downhill method.

3.4. Annealing

The next step of the algorithm is the cooling schedule. Several schedules have been developed but the best known and also very popular is the original schedule of Kirkpatrick /3/. The temperature decreases exponentially:

$$T(k) = T(k-1) \cdot \alpha, \quad \alpha \in [0,1] \tag{8}$$

where k is the temperature stage index. Large values of α mean slow convergence but more reliable search for the

global optimum whereas smaller values mean fast convergence with the increased risk of getting trapped in a local minimum. The empirically chosen value for α was 0.99. At the end of every temperature stage the number of moves N_t in a temperature stage is also decreased by α:

$$N_t(k) = N_t(k-1)\cdot\alpha \tag{9}$$

The probaility distribution for random moves must also be adapted. The range parameter $\underline{R}$ is reduced at the end of every temperature stage:

$$R_t(k) = R_t(k-1)\cdot\alpha, \quad i = 1,2,...N_v \tag{10}$$

3.5. Stopping criterion

Several stopping criteria can be used. In our case the algorithm stops when the temperature reaches user specified minimal value T_{min} (in our case 10^{-6}) or when the number of CF evaluations exceeds the maximum allowed number of evaluations.

4 Optimization of mathematical test functions

Orthogonal simulated annealing was compared with the COMPLEX method /2/ on a set of mathematical functions. The set includes unimodal functions, functions with a small number of local minima (considered as moderatelly difficult problems) and difficult problems with many local minima, noise, nonlinearity and strong interactions between variables. All of the tested functions can be found in /4/. The optimization was repeated 50 times for every function with randomly chosen initial points. Both methods had the same limited number of CF evaluations (50000 and 70000 for problems with N_v = 30 and N_v = 100, respectively). The optimization results are given in table 2.

The results show that the OSA method is promising when compared to COMPLEX. The COMPLEX method exhibits very fast convergence but gets stuck in a local minimum in almost every tested case. It outperforms the OSA method in some cases of unimodal functions and functions with strong noise. The latter is not unexpected since the method maintains a population of points between iterations. Simulated annealing, on the other hand, starts every iteration from a single point. On multimodal functions OSA outperformed the COMPLEX method in terms of global search capabilities. Due to the modified generation mechanism and cooling schedule the algorithm was not able to locate the global minimum in all optimization runs, but the solutions that were found were still fairly good when compared to the global minimum.

5 Optimization of integrated circuits

Since the OSA performance on mathematical functions was very promising, the next step was to test it on real-world

	N_v	COMPLEX	OSA	global minimum
f_1	30	-9596.2 -3012.3	-12569.5 -12569.5	-12569.5
f_2	30	6.9709 224.67	$3.5527\cdot10^{-14}$ 1.9899	0
f_3	30	$1.6714\cdot10^{-2}$ 3.93447	$1.5234\cdot10^{-7}$ $2.7337\cdot10^{-7}$	0
f_4	30	$2.2362\cdot10^{-5}$ 3.04840	$1.7375\cdot10^{-13}$ $1.6971\cdot10^{-1}$	0
f_5	30	$2.1584\cdot10^{-5}$ 1.59433	$1.6672\cdot10^{-16}$ $2.0732\cdot10^{-1}$	0
f_6	30	$1.9551\cdot10^{-5}$ 6.99148	$3.1601\cdot10^{-15}$ $1.0987\cdot10^{-2}$	0
f_7	100	-61.124 -29.261	-98.861 -97.860	-99.2784
f_8	100	-70.408 -63.311	-78.332 -78.331	-78.33236
f_{10}	100	113.13 196.95	283.59 795.04	0
f_{11}	30	$2.5981\cdot10^{-8}$ $5.3587\cdot10^{-5}$	$5.4955\cdot10^{-14}$ $8.2124\cdot10^{-13}$	0
f_{12}	30	$4.1618\cdot10^{-3}$ $2.0489\cdot10^{-2}$	$2.4360\cdot10^{-2}$ $1.5660\cdot10^{-1}$	0
f_{13}	30	$1.9705\cdot10^{-1}$ 3.6034	$1.8169\cdot10^{-7}$ $8.2303\cdot10^{-7}$	0
f_{14}	30	$8.9943\cdot10^{-2}$ 39.777	102.83 1928.0	0
f_{15}	30	1.8026 9.4910	$1.2809\cdot10^{-5}$ $8.4080\cdot10^{-1}$	0

Table 2. Table shows the best and the worst solution found in 50 optimization runs. The functions used are defined in [4].

electronic circuit design problems and compare its performance with the COMPLEX method. For this purpose SPICE OPUS circuit simulator was used /6/. In SPICE OPUS a modified COMPLEX method is already integrated as one of the available optimization methods. Since the original method has very fast convergence, restart with intelligent initial points selection is conducted every time the basic method reaches its stopping criterion /7/. This process is repeated untill the given limit of CF evaluations is reached. The final result is the best solution of all the runs. The OSA method had to be implemented in C langunage and added as one of the available optimization methods in SPICE OPUS.

Three cases of electronic circuit design were considered. The first circuit was a simple delay element, the second an operational amplifier, and the third a rather complex amplifier circuit. Circuit topologies for all three cases are given in figures 2, 3, and 4. The key properties of all three optimization problems are given in table 3.

Optimization parameters were resistances, capacitances and transistor channel lengths, widths, and multiplier factors. For every circuit several design goals were set. A single CF is constructed as a combination of all the design goals /8/. Optimization is conducted across several cor-

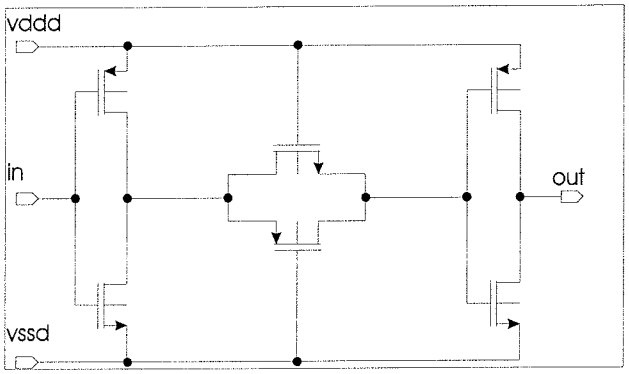

Fig. 2: Topology of the first circuit.

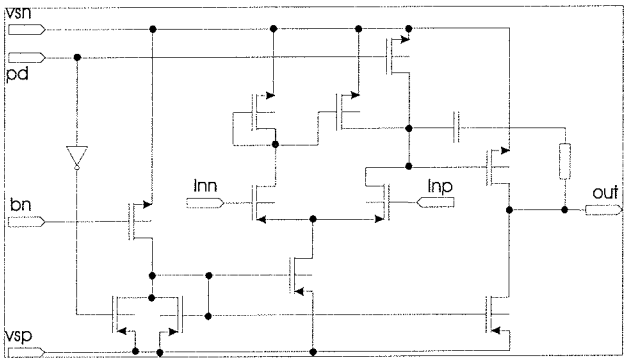

Fig 3: Topology of the second circuit.

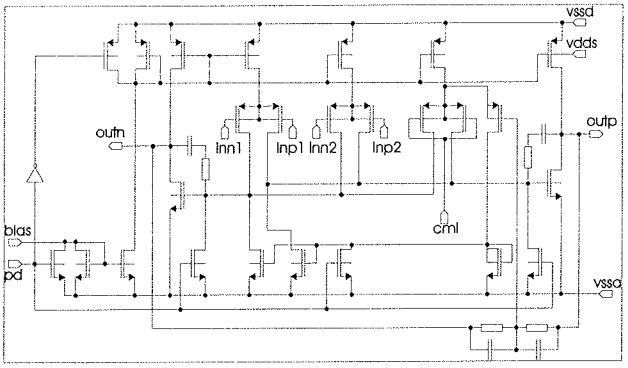

Fig. 4: Topology of the third circuit.

Table 3: Summary of the optimization cases: number of optimization parameters, number of design goals, and number of corner points.

case	N_v	design goals	corner points
1	12	7	1
2	15	14	14
3	17	32	17

ner points to account for different envirenmental conditions (supply voltage, temperature, process parameter variations, ...). Since every CF evaluation requires a separate circuit simulation for each corner point, a large number of simulations is expected resulting in very long run times. Therefore every circuit was optimized only once. The results of the optimization are given in table 4.

Table 4: Optimization results: number of function evaluations (FE) to find a solution of the given quality, and final solutions. For modified COMPLEX method the number of the run in which a solution was found, is also given in brackets.

case		mdified COMPLEX	OSA
1	FE until cost < $100 \cdot 10^3$	253 (1)	1011
	FE until cost < $20 \cdot 10^3$	660 (1)	12758
	best cost	$6.39 \cdot 10^3$	$11.3 \cdot 10^3$
	FE until best cost	21409 (28)	14703
	final FE	> 100 000	16122
2	FE until cost < 50	124 (1)	58
	FE until cost < 10	2483 (2)	33595
	best cost	8.07	7.37
	FE until best cost	96912 (69)	47605
	final FE	> 100 000	47768
3	FE until cost < 10	3672 (3)	32014
	FE until cost < 1	26688 (21)	34248
	best cost	0.282	0.088
	FE until best cost	41131 (32)	43877
	final FE	> 45 000	44164

Since the modified COMPLEX method uses restarts and can explore several local solutions within the given number of CF evaluations, the number of the run in which a solution was found is given in brackets. The number of CF evaluations after which the COMPLEX method was manually stopped, is also given. The OSA method stopped automatically when the temperature reached its final value. Both tested methods were compared in terms of the solution quality and the number of CF evaluations (FE).

The first case is the most simple of the three cases considered. It only has a few design goals and does not include corner points. It also has the least optimization variables. All this makes the solution space smaller and the CF less complex. For this case the modified COMPLEX method performed considerably better than OSA. It did however require more CF evaluations and several restarts to reach a good solution. In the second case multiple corner points and more design goals were considered. OSA outperformed the modified COMPLEX method in terms of solution quality and number of required CF evaluations. The third case has the largest number of optimization variables, design goals, and corner points. In this case OSA was also more successfull than the modified COMPLEX method. These results show that for simpler cases the modified COMPLEX method clearly is a better choice. But when it comes to complex circuits, many design goals, and, above all, a large number of corner points, it does not perform as good as OSA. Not even restarts helped the COMPLEX method to find a better solutions than the one OSA found in a single run.

6 Conclusions

A recently developed optimization method called Orthogonal Simulated Annealing (OSA) is described and compared against a version of the simplex algorithm (COMPLEX method). Both methods are first tested on a set of mathematical test functions. The results showed that OSA performs better when the CF has many local minima. On the other hand, the COMPLEX method is a good choice when finding a local minimum quickly is more important than finding a global minimum. OSA and modified COMPLEX method were then tested on three IC design cases. The results showed that on the simpler case the modified COMPLEX method using restarts outperformed the OSA method. As the problem complexity increased, the ability of the OSA to explore the search space more thoroughly resulted in better performance (compared to the modified COMPLEX method). But in order to obtain a good solution in a reasonable amount of time, probabilistic global convergence of the algorithm had to be sacrificed (modified generation mechanism and cooling schedule). Therefore there is no guarantee as to when and if the global minimum will actually be found. Nevertheless OSA is well suited to IC optimization and design, particularly for problems with many variables and corner points.

7 Acknowledgment

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8 References

/1/ Li-Sun Shu, Shinn-Ying Ho, *A Novel Orthogonal Simulated Annealing Algorithm for Optimization of Electromagnetic Problems,* IEEE transactions on magnetics, Vol. 40, No. 4, pp. 1790-1795, July 2004.

/2/ M.J. Box, *A new method of constrained optimization and a comparison with other* methods, Computer Journal, Vol. 8, pp. 42-52, 1965.

/3/ S. Kirkpatrick, C.D. Gelatt, M.P. Vecchi, *Optimization by simulated annealing,* Science, Vol. 220, pp. 1277-1292,1983.

/4/ Yiu-Wing Leung, *An orthogonal Genetic Algorithm with Quantization for Global Numerical Optimizaion,* IEEE transactions on evolutionary computation, Vol. 5, No. 1, pp. 41-53, 2001.

/5/ R.L. Yang, *Convergence of simulated annealing algorithm for continuous global optimization*, Journal of optimization theory and applications, Vol. 104, No. 3, pp. 691-716, 2000.

/6/ SPICE OPUS circuit simulator homepage:
URL: http://www.fe.uni-lj.si/spice/ ,
Faculty of Electrical Engineering, Electronic Design Automation Laboratory:
URL: http://www.fe.uni-lj.si/edalab/\hspace{1mm}.

/7/ Puhan J, Bűrmen A, Tuma T. *Analogue integrated circuit sizing with several optimization runs using heuristics for setting initial points*, Canadian journal of electrical and computer engineering, Vol. 28 (3-4): pp. 105-111 JUL-OCT 2003.

/8/ Bűrmen A, Strle D, Bratkovič F, Puhan J, Fajfar I, Tuma T. *Automated robust design and optimization of integrated circuits by means of penalty functions*, AEU- International journal of electronics and communications, Vol. 57 (1), pp. 47-56, 2003.

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A METHODOLOGY FOR OPTIMUM DELAY, SKEW, AND POWER PERFORMANCES IN AN FPGA CLOCK NETWORK

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Key words: FPGA clock network, High performance, IC design, Low power design, CMOS

Abstract: A methodology for FPGA clock network optimisation is presented. The algorithms for optimisation of clock skew, delay, and power considering slew rate constraint for an FPGA fixed-clock network are implemented and verified on SX 32 FPGA chip. Measurements indicated a 60% reduction in clock slew rate and a 22% improvement in power dissipation when compared to the results of the initial, un-optimised chip.

Metodologija za doseganje optimalne zakasnitve, porazdelitve signala in porabe moči urinega omrežja vezij FPGA

Kjučne besede: CMOS, FPGA, urina vezja, načrtovanje integriranih vezij, načrtovanje vezij z majhno porabo, CMOS

Izvleček: V prispevku predstavljamo metodologijo za doseganje optimalnega delovanja urinega omrežja znotraj vezij FPGA. Algoritmi za optimizacijo zakasnitve, popačenja signala in porabe moči so bili uvedeni in preverjeni na vezju SX 32 FPGA. Meritve pokažejo 60% zmanjšanje v popačenju signala in 22% zmanjšanje porabe moči v primerjavi z rezultati pred optimizacijo.

1 Introduction

Modern high performance VLSI systems are designed to work at a specific maximum clock frequency depending on their applications and the process technology used. One of the constraints in achieving maximum clock frequency is clock rise time (*slew rate*). The longest rise time in the clocking network limits the clock frequency (clock period) /1/.

A clock network is responsible for distributing clock signal from an input pad to the clock input of each block in an IC (sink). The clock net should be able to maintain the clock signal integrity. The distribution of clock signal on the chip must be done while minimizing the clock delay, clock skew, and slew rate /3/. *Clock delay* is defined as the maximum delay from the clock source to the input of any logic block. *Maximum clock skew* is defined as the difference between the longest clock delay and the shortest clock delay in the system.

To achieve minimum slew rate while maintaining clock signal integrity, minimum number of buffers are added into the clock tree. This technique also helps to reduce clock delay and clock skew. Proper buffer placement and buffer sizing minimizes the slew rate. Capacitive load of the driven gates/logic blocks (gate load) and parasitic loads of signal line (wiring load) are among the factors that affect clock slew rate, delay and power dissipation. Since power consumed by the clock network contributes a major portion of the total chip's power consumption /4/, reducing the clock net power consumption will have tremendous effect in system's overall power consumption.

Research works in the buffered clock network mainly focused on the minimization of clock delay and clock skew. As far as this work is concerned, previous works have not addressed the problem of clock delay, skew, and power optimisation with slew rate constraint. Work in /1/ emphasized on generating a clock network and optimising clock delay and skew without considering power performance while work in /3/ focused on inserting minimum number of buffers in clock trees with skew and slew rate constraints. The latter assumes that the clock tree will be buffered by a single type CMOS buffer. No doubt, this strategy helps to reduce clock skew and skew sensitivity to process variation. It, however, requires a balanced tree network, which is not applicable to FPGAs. The simultaneous change of buffer size and wire width to optimise performance and power in /5/ assumes that buffer locations are already given; i.e. clock tree is already buffered. This technique is useful in minimizing delay and power but it does not consider any slew rate constraint. Although the work done in /6/ can significantly reduce the clock delay and clock skew, it does not consider the effect buffer insertion has on slew rates and power dissipation. Additional capacitive loading imposed by adding buffers into the clock tree will increase the slew rates and power dissipation, which is not desirable, especially for high-speed mobile applications.

Based on these observations, this paper proposes an optimisation methodology for optimum clock delay, skew, and power performances for a given slew rate constraint.

For this work, several constraints are considered and a few assumptions are made:

- Buffers can be inserted at tree nodes only due to the FPGA physical layout constraint.

- The maximum clock slew rate is 0.5 ns, and the maximum allowable clock delay is 2.5 ns for CMOS 0.35-um technology.
- The clock tree will be buffered by buffer of different sizes due to loading considerations.

The outline for the remainder of this paper is as follows. Problem formulation is discussed in Section 2. In Section 3, the algorithm that solves the initial buffer insertion problem is presented. Algorithm for delay and slew rate optimisation by changing buffer position is discussed in Section 4. Section 5 discusses the buffer sizing strategy for simultaneous clock delay, skew, slew rate, and power optimisation. Section 6 explains the wire width sizing technique for delay reduction. Section 7 contains the simulation results and comparisons. Conclusions are presented in Section 8.

2.1 Definitions

The definitions of the terms that will be used in the later sections are as follows:

- *Unbuffered Clock Tree* (UBT): a clock tree T(V,E) consisting of wires (edges) E and nodes V with no buffers between the source and sink nodes (initial clock tree).
- *Buffered Clock Tree* (BFT): a clock tree T(V,E) after buffer insertion.
- *Wire* (E): an internal signal line connecting logic block's input to its output.
- *Node (V)*: a point that connects two logic blocks together

An FPGA is made up of z number of logic blocks (**x** rows x **y** columns, where **x** x **y** = **z**, input-output (I/O) blocks, and programmable interconnects (see Fig. 1). Logic blocks can be either logic modules or flip-flops (see Fig. 2 (a) and (b), respectively). The circuit models for this work are as shown in Fig. 3 and Fig. 4. Each clock tree branch (vertical column) consists of logic blocks and a driver to drive the clock signal to all the logic blocks in the column (see Fig. 4). Logic blocks are modelled as a series RC-circuit while the vertical wires are modelled as a π-RC circuit (see Fig. 3). The resistance R for the two models (series π-RC and RC) is given by the following formula:

$$R = \left(\frac{L}{W}\right)\rho \qquad (1)$$

where L = length of Logic Module

W= width of vertical track for the path of clock signal inside the logic block

r = sheet resistance of signal path

The capacitance in the RC-circuit that models the logic block for CMOS 0.35-um technology is 21.2 fF (calculated based on the 3D modelling technique described in /7/).

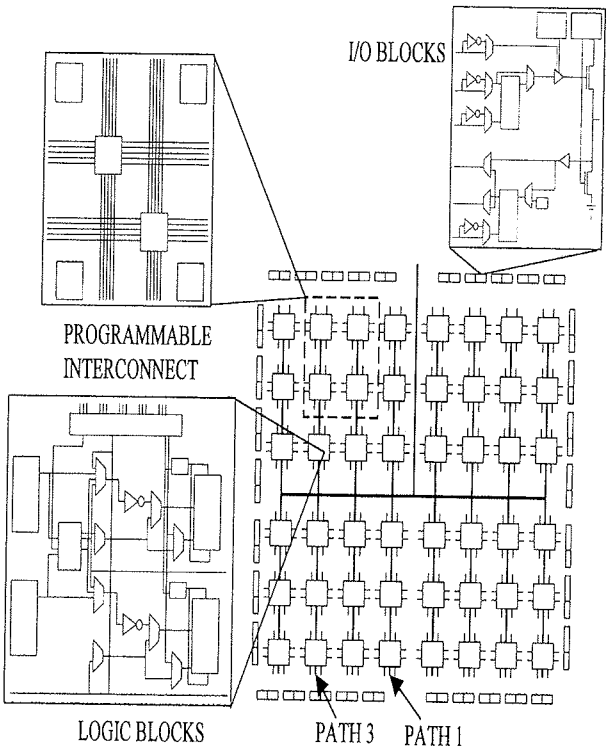

Fig. 1. FPGA Building Blocks

Horizontal wires are modelled as a PI-RC circuit (see Fig. 3). Wire resistance is calculated as follows:

$$R = \frac{L_h}{W_h}\rho + R_{\text{int}\,erconnect} \qquad (2)$$

where L_h = horizontal length of logic module

W_h = horizontal width of logic module

r = sheet resistance of signal line

$R_{interconnect}$= resistance of interconnect

The capacitance is found to be 23 fF (based on the method described in /7/).

Figure 5 shows the sketch of the proposed technique for simultaneous optimisation of clock delay, skew, and power with slew rate constraint. The overall algorithm is shown in TABLE 1.

i. Initial Buffer Insertion:

Inserts different number of buffers in each source-to-sink for a UBT depending on the slew rates of that path.

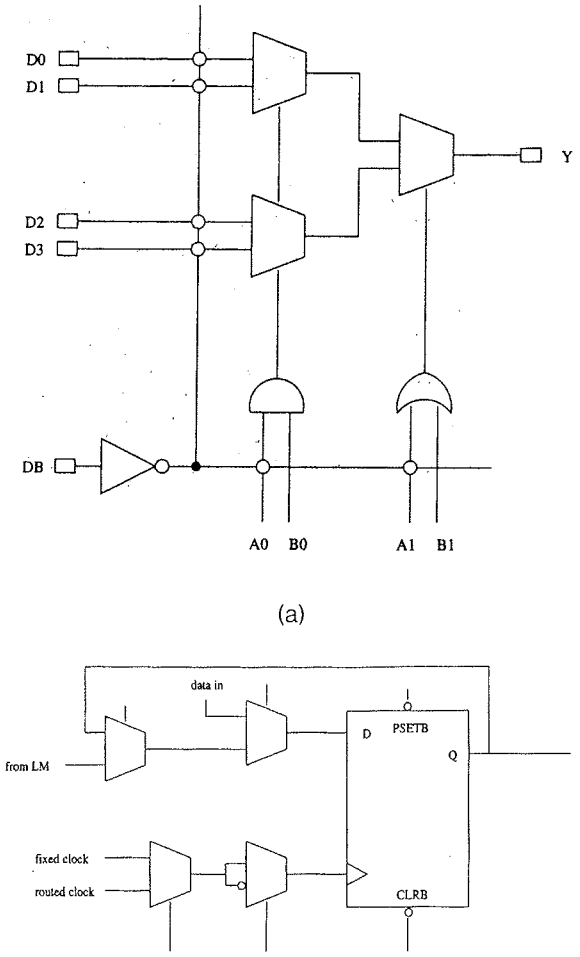

Fig. 2. FPGA Logic Blocks: (a) Logic Module; (b) Flip-flop

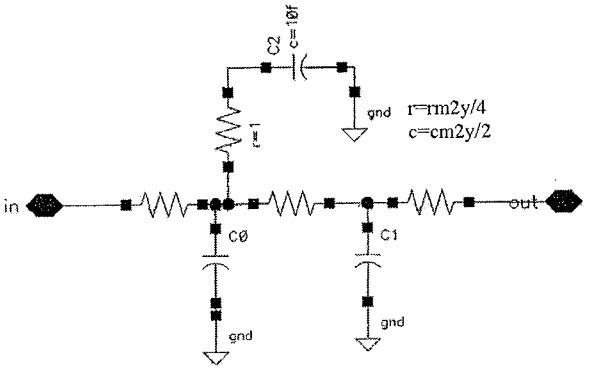

Fig. 3. RC Model for Logic blocks and wire

ii. Delay & Power Optimisation (Slew Rate Constraint) - modified /6/

Buffer locations are optimised to minimize clock delay. Buffer sizes in the BFT are changed accordingly to minimize slew rate, should there be a need to do so.

iii. Delay & Skew Optimisation by Buffer Sizing - proposed by /5/ and /6/, modified to consider slew rate constraint

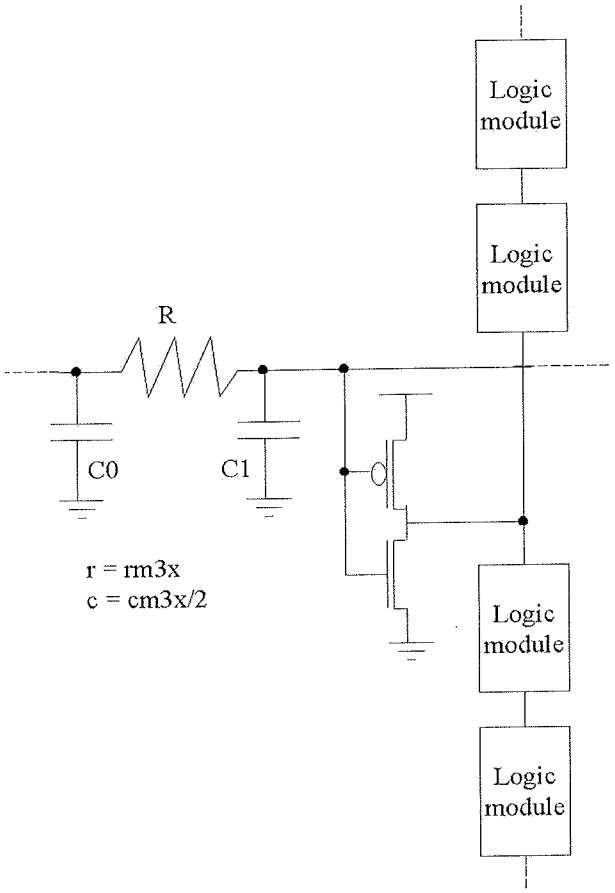

Fig. 4. Column model

Path by path, buffer sizes are changed to change the delay of each path/column.

iv. Wire sizing approach to optimise power, skew, and delay

Wire widths are changed to see the effect on clock delay, skew, and optimisation.

Table 1 - Overall optimization algorithm

```
Get slew rates and delay of every path
Do Initial Buffer Insertion

while flag = TRUE
  Do Delay and Power Optimization
  (Buffer Positions)

  if slew rates < t_max
    Do Delay & Skew Optimization (Buffer Sizing)
    flag = FALSE
  else
    flag = TRUE
    Do Slew Rate Minimization (change size of B_k-1)
  end
end
Do Skew & Power Optimization (Wire Sizing)
```

In this section, Initial Buffer Insertion problem is discussed.

Initial Buffer Insertion Problem: Given a UBT and a maximum clock delay, clock skew, and slew rates, determine the number of buffers to be inserted in each path (source to sink) such that slew rate is less than t_{max} of 0.5 ns. That is, number of buffers in each path = f(slew rate)

To solve the initial buffer insertion problem, given a slew rate constraint, the paths are first sorted in ascending order according to the maximum path clock delay, i.e. t_{delay_P1} (t_{path_min}) < t_{delay_P2} < ... < t_{delay_P20} < t_{delay_P21} (t_{path_max}). Next, the size of column driver is reduced by a factor of two.

We then measure the maximum slew rate of every path, starting with the shortest delay path, i.e. path 1. If the slew rate is less than t_{max}, no buffer is inserted in that path.

However, if the slew rate is greater than t_{max}, one buffer is inserted right in the middle of the clock path. The maximum slew rate for the path is then measured. If it is still greater than t_{max} or if the rise time improvement is less than 15%, we remove the buffer and start increasing the size of column driver until the goal is achieved.

If there is at least 15% improvement in path slew rate but it is still greater than t_{max},, another buffer is inserted. This time the two buffers are placed such that they divide the clock path in three equal-length sections. The buffer insertion step is repeated until the slew rates for all paths are less than t_{max}. In general, if we have k buffers in a path, they should be arranged such that they divide the path in k+1 equal sections.

For instance, consider three paths in the FPGA chip shown in Fig. 1. Initially, the slew rates for paths 1, 3, and 21 are 482 ps, 583 ps, and 940 ps, respectively. After the size of column driver has been reduced by a factor of two and one buffer has been inserted in path one, the slew rate is reduced by only 5%. Therefore, we remove the buffer in path 1 and start increasing the size of column driver (see Fig. 4). The final result for path 1 is that the slew rate is less than 0.5 ns. Path 3 needs one buffer while path 21 (the longest path, not shown in Fig. 1) needs two buffers.

We, then, continue the optimisation process with the simultaneous optimisation of clock delay, slew rate, and power by changing buffer positions.

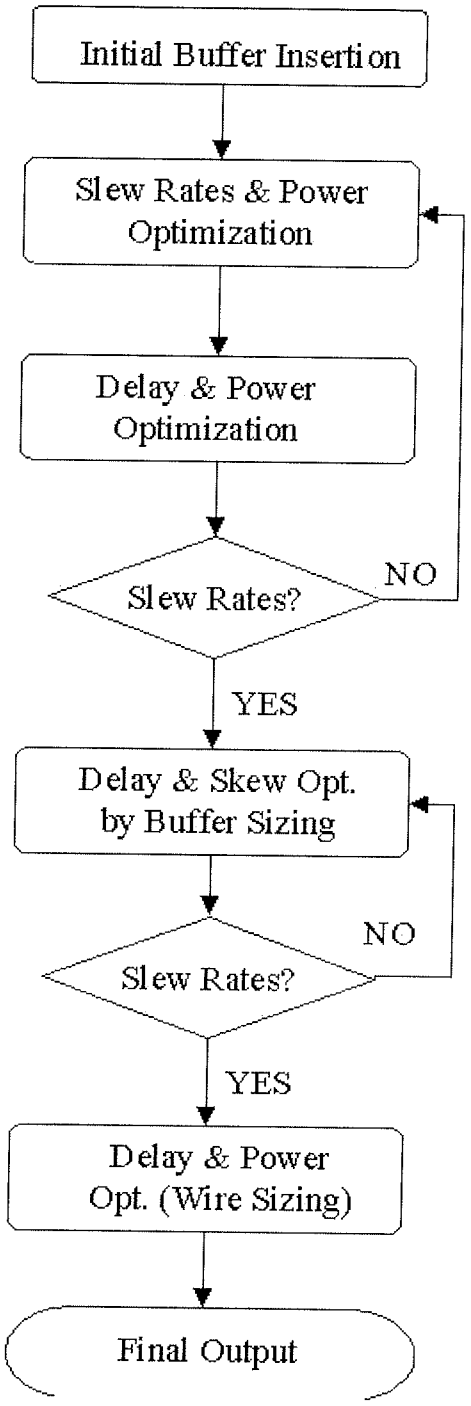

Fig. 5. Optimisation Approach

The algorithm selects a buffer from source to sink (depth-first) and move its position to reduce the clock delay. If the delay is reduced, the buffer is moved to the new location, otherwise it stays at its original position. After all buffer positions have been optimised, we check the slew rate. A buffer is selected from sink to source (bottom-up). If the slew rate at input of buffer B_k is greater than 0.5 ns, we increase the size of buffer B_{k-1} until the slew rate is less than t_{max}.

TABLE III displays the Buffer Positioning Algorithm for simultaneous optimisation of clock delay and power with slew rate constraint. The original algorithm developed by /6/ was modified to consider the slew rate constraint.

Table 5 displays the algorithm used for optimising clock delay and skew. This original technique was developed by /6/, and then was modified to take into account the slew rate constraint.

Step 1: The algorithm arranges the path according to its delay in ascending order; t_{delay_P1} (t_{path_min}) < t_{delay_P2} < ... < t_{delay_P20} < t_{delay_P21} (t_{path_max}).

Step 2: Starting with t_{path_min}, it selects a buffer from source to sink (depth-first).

Step 3: The buffer size is changed by Δs. If the delay is reduced, we then check the slew rate. We stick with the new size should the slew rate be less than t_{max},. Otherwise, the buffer size is not changed.

Step 4: If delay is reduced and slew rate is less than t_{max}, repeat step 3 until there is no further improvement.

Wire width sizing strategy for delay, skew and power optimisation is as described below:

Step 1: Given a maximum wire width due to chip area constraint, vertical and horizontal wire widths are increased.

Step 2: If clock delay, and skew are reduced, then change the widths.

Step 3: Otherwise, reduce wire widths. If delay and skew is decreased, keep reducing the wire widths. Else stop.

The results of the algorithms developed were verified on an FPGA chip where the clock tree is neither balanced nor of equal length. All the logic blocks in the FPGA chip have fan-out of one for worst-case capacitive loading imposed on the clock tree.

Table 4 presents the results of clock delay, skew, slew rates, and power before and after the clock tree is optimised. Chip area savings of 765 μm^2 is achieved with the new optimised clock tree. Power dissipation is improved by 22%. For all paths, the slew rates are reduced to within the scope of 500 ps (t_{max}). These values range from 366 ps to 463 ps.

Table 2 - Delay & Power optimization algorithm

Input: Buffered Clock Tree (BFT) with n
paths and k_i level of buffers in path i.
n = no. of paths
Δx: buffer moving step (single-node step)

Output: Optimized clock path (position-wise)

Procedure: PathDelayMinimization (Path i, k_I, Δx, n)

```
for path = 1 to n
  // optimize delay (move buffer position)
  for buffer level i = 1 to k (depth-first approach)
    move buffer i, B_i up Δx
    check path clock delay

    if delay is reduced
       stay at new location
            keep moving up Δx until no further
       improvement
    else
       go back to old location
       move buffer i, B_i down Δx
       check path clock delay
       if delay is reduced
          stay at new location
                    keep moving down Δx
          until no improvement
       else
          back to old location
       end
    end

end


  // minimize slew rate
  for buffer j = k to 1 (bottom-up)
    if slew rate at input of B_j > 500 ps
       increase size of B_j-1
    end
  end
end
```

Table 3 - Delay and skew minimization with slew rate constraint

```
Input: BFT with optimized buffer position
       Δs: buffer size increase
       n = no. of paths

Output: Optimized buffer sizes for delay, skew,
slew rate and power.

Procedure: BufferSizing (Path i, k_i, Δs, n)

for path = 1 to n (i.e. τ_path_min to τ_path_max)
  for buffer level i = 1 to k

    // increase buffer size
    while increase_buffer_size = TRUE
      increase size of buffer i, B_i by Δs

      if delay is reduced
        if slew rate < t_max
        buffer size = new size
        increase_buffer_size = TRUE
      else
        buffer size = old size
        increase_buffer_size = FALSE
      end
    end

    // reduce buffer size
    while reduce_buffer_size = TRUE
      reduce size of buffer i, B_i by Δs

      if delay is reduced
        if slew rate < t_max
        buffer size = new size
        reduce_buffer_size = TRUE
      else
        buffer size = old size
        reduce_buffer_size = FALSE
      end
    end

  end                    // end of 2nd for loop

// need additional buffers?
  if delay > 2.5 ns (t_max)
    add another buffer in the path
    go to PathDelayMinimization
  end

  end            // end of main for loop
```

In this paper, a methodology for optimisation of clock delay, clock skew and power with slew rate constraint is presented. This method is effective especially when dealing with trade-offs among delay, skew, power, and slew rate for an FPGA chip.

The results presented in this paper have shown convincingly that the method developed yields sharper rise and fall edges and reduces power dissipation with practically no penalty in the clock delay.

/1/ I-Min Liu, T.L. Chou, A. Aziz, and D.F. Wong, "Zero-Skew Clock Tree Construction by Simultaneous Routing, Wire Sizing and Buffer Insertion", **Proc. 2000 Int'l Symposium on Physical design, pp. 33-38, 2000.**

/2/ M.Afghani and C.Svensson, "Performance of synchronous and asynchronous schemes for VLSI systems", *IEEE Trans. Comput.*, vol. 41, no. 7, pp. 858-872, 1992.

/3/ G.E. Tellez, "Minimal Buffer Insertion in Clock Trees with Skew and Slew Rate Constraints", *IEEE Transactions on CAD of IC and Systems*, vol. 16, pp. 333 - 342, April 1997.

/4/ J.W. Chung, D.Y. Kao, C.K. Cheng, and T.T. Lin, "Optimization of Power Dissipation and Skew Sensitivity in Clock Buffer Synthesis", *ISLPED 95*, pp. 179 - 184, 1995.

/5/ J.Cong, C.K.Koh, and K.S.Leung, "Simultaneous Buffer and Wire Sizing for Performance and Power Optimization", *ISPLED 96*, pp. 271 - 276, 1996.

/6/ X. Zheng, D. Zhou, and Wei Li, "Buffer Insertion for Clock Delay and Skew Minimization", *ISPD 99*, pp. 36 - 41, April 1999.

/7/ T.Stohr, et al, "Analysis, Reduction and Avoidance of Crosstalk on VLSI Chips", *ISPD 98*, pp. 211 - 218, 1998.

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Table 4 - Comparison of clock delay, skew, slew rate, power dissipation, and buffer area between the unoptimised design and the optimized design

	Initial Clock Tree		Optimised Clock Tree		% Improvement
	Shortest Path (1)	Longest Path (21)	Shortest Path (1)	Longest Path (21)	Overall (Path 21)
Rise Time (ps)	481.1	939.5	463.5	362.8	61.4
Fall Time (ps)	493.0	842.9	456.3	385.7	54.2
Clock Delay (ns)	1.43	2.35	1.38	2.26	3.8
Maximum Clock Skew (ns)		0.92		0.88	4.3
Power (mW)		112.7		87.4	22.4
Area occupied by Buffers & Column Drivers (μm^2)		5145		4380	14.9

AN AI BASED SELF-MODERATED SMART-HOME

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Key words: Smart-Home, VHDL, Multiagent, FPGA, Prediction.

Abstract: Smart-home conception has emerged in recent years and played a very important part in the formation of future houses. Making our current homes more adaptable and self-directed is the main focus of smart home research. Achieving these goals won't be possible without giving our today's home enough intelligence to make rational decisions to operate itself which usually we as inhabitants of the home make these decisions in our everyday life to manage our home and achieve comfort that we desire. In this paper we present prototype of a system that overcomes this problem by giving the home enough intelligence to adapt to its inhabitants life style without the need for the inhabitants to exercise authority. The system makes use of multi-agent and prediction techniques to provide intelligent smart-home appliances automation. The final prototype will be downloaded into FPGA chip.

Pametni dom na osnovi umetne inteligence

Ključne besede: Inteligentni dom, VHDL, večagentni sistemi , FPGA, napoved

Izvleček: Koncept inteligentnega doma se je pojavil v zadnjih letih in je odigral pomembno vlogo pri načrtovanju bodočih hiš. Glavni cilj raziskav na področju inteligentnega doma je ustvariti bolj prilagodljiv in samo-upravljiv dom. Takega cilja ne bo mogoče doseči brez, da bi domu dali določeno mero inteligence, s pomočjo katere se bo lahko odločal in se upravljal, kar je do sedaj bila izključno domena stanovalcev. V prispevku predstavimo prototip sistema, ki domu omogoča dovolj inteligence, da se prilagodi življenskemu slogu stanovalcev brez potrebe po njihovem avtoritativnem posredovanju. Sistem uporablja večagentne tehnike in tehnike napovedi za avtomatizacijo delovanja naprav znotraj inteligentnega doma. Končni prototip bo izveden kot vezje FPGA.

1. Introduction

Smart-home is a structure that is equipped with technology that makes it possible for the home inhabitant to operate the house using special techniques. These techniques might include programming an array of home appliances or by using remote control schemes. Recently many high profiled researches discrete such as IBM, MIT and Microsoft started to setup smart-homes to be used as test beds by researchers /1/.

The Artificial Intelligence (AI) designation; is the ability of a computer to perform rational tasks, such as reasoning and learning that human intelligence is capable of doing /2/. The aim of AI is to utilize the abilities of the human brain into computer powered devices. One of these devices is the smart-home appliance that can automatically adjust itself to the desire of the home inhabitants.

The physical picture of a home being rational is very plausible. A home that is capable of making coherent decisions could possibly offer a level of self-sufficiency that is not available in the current home environment. By automating the home many residents prefer that home tasks such as security and power consumption can be carried out by the smart-home systems automatically with out their need for exercising authority. The essence of smart-home study lies in the creation of smart environment saturated with computing and communication capability, yet gracefully enhanced integrated with the human users The complexity of a Smart Home solution lies in the variety of different protocols and media involved, and the requirements of the various services provided such as automation, security and power management etc.

During the past years many home appliances automation projects has emerged /3, 4, 5/. Although previous systems achieve the required home mechanization needs but on the other hand most of previous systems were software based and expensive to be implemented and commercialized and that's probably the main reason why previous systems were not used by the general public. In this paper we present a portable, low cost and fast hardware prototype of a multi-agent system that is designed to provide home automation without the need to be programmed.

In the next section we will look into the detail of the techniques used in our system and at the end we will illustrate the expected performance of the system and furthermore future work will be discussed.

2. Research methodology

The system main goals are to achieve high operational speed and efficiency and at the same time making it cost effective and portable. Due to the mentioned goals the system is implemented on hardware rather than software.

The system makes use of multi-agent techniques; each agent will be responsible to control a section of the home

and automate the devices appliances usage according to the life style of the inhabitants. The agents are homogeneous and non-communicative; the only communication that the agents can perform is to share the overall environment state of the whole smart-home so as to make better predictions and device automations.

To correspond with the outside world the system makes use of X10 protocol to send and receive messages from and to the home appliances. The system has two modules; one of the modules is used to generate X10 packet and the other is responsible to receive and translate an X10 packet. Based on the information contained in the packet, the unit generates a message to each agent environment state maintainer. When the device state maintainer receives the message it updates the local view of the agent devices state.

The system is event driven. The events are themselves time driven and are controlled by a system clock. The time frame of the events is adjustable by the home occupants. Each time an event trigger is generated the agents will issue a device command based on their learned knowledge that were gathered by monitoring the users everyday device interactions.

The agent consists of three main units; prediction unit, decision unit and communication unit. The prediction unit is designed by using Active-Lezi algorithm /6/, the unit is responsible for predicting the future environment state based on the current environment state. On the other hand the decision unit is modeled using techniques of Reinforcement learning, the algorithm used for modeling the unit is Q-Learning.

The use of prediction unit with the decision unit makes better system performance since it is sometimes undesirable to directly predict and operate a particular home appliance. That's why we need the reinforcement learning techniques to be used so that the agent learns from previous experience and not letting the prediction unit perform unnecessary action. Finally the communication unit is responsible to handle the communication between the agents as illustrated in Fig.1

Before putting the system into operation the system needs to be trained. The training is done by collecting devices usage patterns of the home inhabitants, after data gathering phase the data is fed to the system. The system performance is improved by using more accurate training data. For detailed system superficial overview refer to Fig.2.

3. Decision unit

The decision unit of the system is responsible for performing rational decision. The unit is modeled according to Q-Learning algorithm. Q-learning is a reinforcement learning technique where action value function is used to assign values to actions that the system performs at a given state.

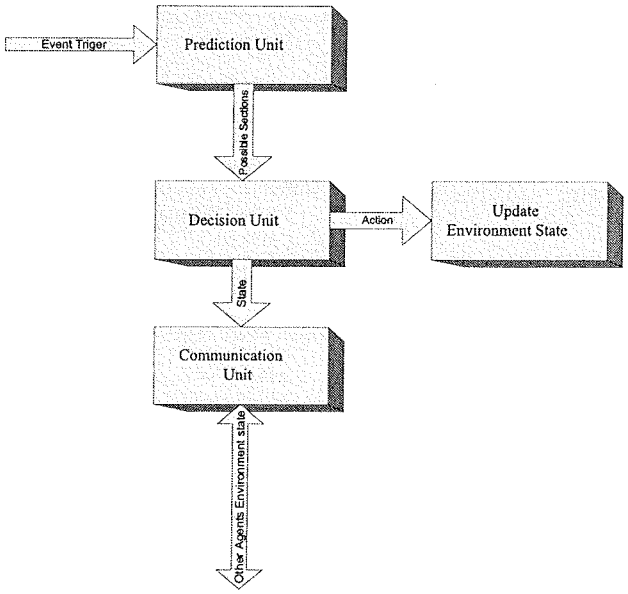

Fig. 1 The agent illustration diagram

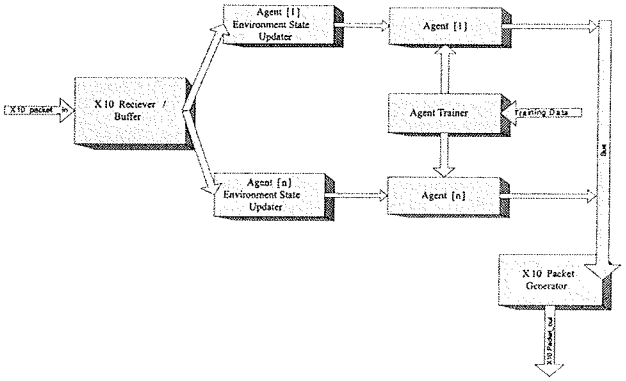

Fig. 2 Superficial illustration diagram of the system

Given the environment devices states as [S], and the device actions that can be taken on a given environment state as [A], we can form the Q value array of reinforcement learning as shown in equation 1.

$$Q = S \times A \tag{1}$$

According to Q-Learning algorithm the Q value array is used to store the rewards the agent has received by performing a particular action at a given environment state. Each time the agent makes a correct decision; the agent is given a positive reward or a negative reward. The reward is calculated based on the user feedback to the agents performed action, which can be sensed by the system through monitoring the devices state constantly.

The Q value function will be calculated as shown in equation 2.

$$Q^*(x,a) = (1-\alpha)Q^*(x,a) + \alpha(r + \gamma V^*(y)) \tag{2}$$

where Q* is the Q-learning value function, *x* is the environment states, a is the action that can be taken, α is the

learning rate, γ is the value of future reinforcement and V* is the future Q-learning value function.

4. Prediction unit

The prediction unit is very important unit; due to the reason that it can minimize the error rate by predicting the future environment state, thus allowing the decision unit to take actions based on the predicted future state. The unit is modeled using an online predictor Active-Lezi.

Active-LeZi algorithm is an enhancement of both LZ78 and LeZi-Update algorithms /6/. It incorporates a sliding window approach to address the drawbacks of both LZ78 and LeZi-Update. This approach also demonstrates various other desirable characteristics given below.

- The core model of Active-Lezi algorithm is Growing-Order-Markov model based on LZ78 algorithm, therefore Active-Lezi accomplish optimal predictability.
- Active-Lezi stores more information, which implies that as the input sequence (the experience) grows, the algorithm performs better. This is a desirable characteristic of any learning algorithm.

After simulating Active-Lezi algorithm by using input data pattern with high noise. We can see that the result gained from the simulation is very desirable since the algorithm achieves prediction of 100%. The simulation result is shown in Fig.3.

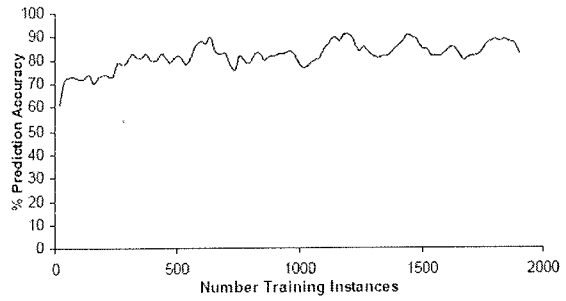

Fig. 3 Graph showing the prediction accuracy of Active-lezi

5. Results and discussion

The purpose of the research is to implement a home appliances automation system by using multi-agent techniques. The system will be later hardware synthesized. At the moment our system is still under development, so the testing of the system that we have so far performed has been done using software simulation.

During our testing phase we have implemented a synthetic data generator to generate training data to train the system. The synthetic data generator is used to produce devices usage pattern that accurately symbolize an actual home occupant devices usage routine. The data simply include the time, place and action of the event that is hypothetically performed by a particular home resident as shown in Table 1. After the data is generated it is converted into an accurate X10 protocol packets and then is fed to the system using the system training unit.

Table 1 Sample Synthetic Data Used To Train The Multi-Agent System

Date and Time	Action	Device	Location
2006-03-03 / 09:21	On	Lamp1	Living Room
2006-03-03 / 10:26	Off	Fan1	Bedroom
2006-03-03 / 10:29	On	Tv1	Living Room
2006-03-03 / 18:21	Off	Lamp1	Living Room
2006-03-03 / 20:22	Off	Tv2	Bedroom

The system has been simulated and tested using our synthetic data generator. Since the system is hardware based we have used Model-Sim VHDL simulation software to simulate the design. Based on our simulation results we realize that the system can perform accurately and the error rate is reduced by using more training data as shown in Fig.4.

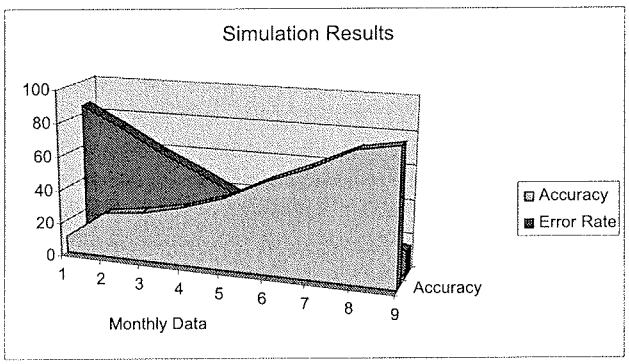

Fig. 4 Graph Illustrate The Simulation Results

Since the system is modeled using the techniques of reinforcement learning, there are few some important point need to be mentioned. In order to accommodate the home inhabitant preferences and learn accurately form the interaction of inhabitant devices, we decided to give a small reward value to every accurate action that the decision-making unit performs and a larger value to a particular action that the user performs. These make the system to adapt the inhabitant preferences faster and more accurate.

Since the actions are increased according to the number of home appliances, thus more the appliances installed in the home, the more complicated the decision making process becomes. The simulation results shows that the system without prediction unit has a dramatically fall in the performance. This proves that the prediction unit is highly important to minimize the number of actions to be performed on the predicted next environment state.

6. Conclusion

The purpose of this research is to implement a revolutionary home automation system that automates the home devices appliances usage based on the inhabitant's life style. The methodology used in this system is based on techniques of AI in particular multi-agent techniques. This system will be realized on hardware to overcome problems faced by other systems such as cost and portability. Moreover making use of muti-agnet techniques will make the system performs faster than previous home automation systems due to the fact that parallelism of multi-agent can help deal with limitations imposed by time-bounded reasoning requirements.

References

/1/ M. Coen, 'Design principles for Intelligent Environments', AAAI Spring Symposium, Stanford, 23rd - 25th March 1998, pp. 36-43.

/2/ Edwin O. Heierman, III Diane J. Cook, "Improving Home Automation by Discovering Regularly Occurring Device Usage Patterns", Data Mining, 2003. ICDM 2003. Third IEEE International Conference on, 19-22 Nov. 2003, pp. 537- 540.

/3/ R. Hamabe, M. Murata, and L. Namekawa, 'Home Bus System (HBS) Interface LSI and its Standard Protocol Example,' IEEE Trans. Consumer Electronics. vol. 36, no. 4. November 1990, pp. 949-953.

/4/ Kashiwamura. H. Koga, and Y. Murakami, "Telecommunications Aspects of Intelligent Building." IEEE Comm. Mag., vol. 29, no. 4, April 1991, pp. 28-40.

/5/ C. K. Lim et al., "Development of A Test Bed for High- Speed Power Line Communications," Int'l. Conf. Power Sys. Tech., 2000, vol. 1, Perth, WA., 4th -7th December 2000, pp. 451-56.

/6/ Karthik Gopalratnam, Diane J. Cook, "Active LeZi: An Incremental Parsing Algorithm for Sequential Prediction", FLAIRS Conference. St. Augustine, Florida, 12th - 14th May 2003, pp. 38-42.

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PRECISE CHARACTERIZATION OF SOFT-MAGNETIC MATERIALS AT HIGH SATURATION

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Key words: ring core, soft-magnetic material, measuring system, DSP, low-distortion, form factor, B-H curve

Abstract: The presented paper deals with a computerized measuring system for evaluating magnetic properties of soft-magnetic ring cores (in compliance with the IEC60404-2 standard). A measuring set-up with a feedback power amplifier is introduced. Its basic operation is explained and an upgraded version is presented. Its main feature is a superior control loop based on a repetitive action control method which assures an accurate and stable secondary induced sinusoidal voltage waveform without voltage zero-crossing distortion caused by a large magnetizing current. Two variants of the repetitive method are presented which provide more realistic measurements of magnetic field strength *H* at the specified amplitude of the secondary induced voltage. Measurements done without and with the repetitive action corrector are presented and discussed. Reasons for choosing one variant are given and results that confirm the improvement over a conventional approach without the repetitive controller are shown.

Merjenje lastnosti mehkomagnetnih materialov pri visoki stopnji magnetnega nasičenja

Ključne besede: toroidno jedro, mehkomagnetni material, merilni sistem, DSP, nizko popačenje, faktor oblike, B-H krivulja

Izvleček: V članku je predstavljen mikrokrmilniško nadzorovan merilni sistem za merjenje parametrov mehkomagnetnih jeder z zaključeno magnetno potjo (po predpisih, ki jih določa standard IEC60404-2). Opisano je osnovno merilno vezje, ki temelji na linearnem močnostnem ojačevalniku z negativno povratno zanko. Razloženi so temelji njegovega delovanja. Predlagana je nadgradnja merilnega sistema z nadrejeno regulacijsko zanko z regulatorjem, ki temelji na repetitivni korekcijski metodi. Slednji je posebno primeren za zagotavljanje stabilne sinusne oblike sekundarne inducirane napetosti brez popačenja pri prehodu skozi ničlo, ki ga povzroča velik magnetilni tok. Predstavljeni sta dve različici repetitivne korekcijske metode, ki omogočata realnejše posredno merjenje magnetne poljske jakosti *H*. Obe različici učinkovito zmanjšujeta konico magnetilnega toka ter posledično magnetne poljske jakosti, pri tem pa ohranjata amplitudo sekundarne inducirane napetosti nespremenjeno. Predstavljene so primerjalne meritve, opravljene na opisanem merilnem vezju brez in z uporabo nadrejene regulacijske zanke z repetitivnim regulatorjem. Podani so razlogi za izbiro ene od izvedb ter pridobljeni rezultati. Opravljene meritve potrjujejo izboljšave, ki jih doprinese regulirani sistem v primerjavi z nereguliranim.

Introduction

In the field of soft-magnetic cores manufacturing the measurement of magnetic field strength *H* at a predefined magnetic flux density *B* is of outmost importance to determine the quality of assembled magnetic cores. The measurement deviations, set by the standards regulating this field /1 - 2/, are relatively tolerant and allow various methods or power supply assemblies for achieving them. Nonetheless, the common denominator of all such devices is that they should keep the secondary induced voltage waveform sinusoidal even when the device under test (D.U.T.) requires high flux density. Such a device should be able to:

- perform B-H curve measurement of soft-magnetic cores which are used in low and medium- frequency applications such as voltage and current transformers, yokes for motors or line filters,
- perform hysteresis loss measurement, which is crucial for minimizing core losses and so enabling reduction in size of magnetic devices.

The accurate measurement of magnetic field strength *H* becomes especially important when estimating cores that are measured in high saturation region. A couple percents deviation of the measured value from the actual value can mean all the difference when considering the material to choose.

To obtain magnetic parameters of soft-magnetic materials, measurements are usually done using standard 25 cm (Epstein) test core assemblies /3 - 5/ consisting of several steel strips. In practice, however, it is desired to perform magnetic measurements not only on magnetic strips, but also to perform production quality control tests on ring cores after they have been assembled /6/.

The standards that regulate the field of magnetic measurements demand a secondary induced voltage of stable amplitude and accurate shape. During measurements, the voltage and frequency variations should not exceed ± 0.2 % of the required value. For the determination of:

- the specific total losses,
- the specific apparent power and
- the *rms* value of the magnetic field strength,

the form factor FF_U (which is the ratio of the *rms* value of the signal to its average rectified value) of the secondary voltage u_S must be maintained in a range of 1.111 ± 1% otherwise the above measurements (and other derivate quantities) are not valid. The given requirements can be

met in two different ways: solely with a feedback power amplifier and by using a superior digital control loop. Both cases are presented in this paper.

Theory

Parameters of a soft-magnetic ring core are usually measured in a well known measurement set-up, where the D.U.T. is magnetized by an alternating primary current i_P, causing a magnetic field strength /2/:

$$H = i_P \cdot N_P / l_{FE}, \quad (1)$$

where N_P is the number of primary turns and l_{FE} the effective magnetic path of the D.U.T., which can be calculated from the dimensions (the outer and inner ring diameters) of the ring core. As a consequence of the magnetic flux density B, voltage is induced in a secondary winding:

$$u_S = - N_S \cdot S_{FE} \cdot dB / dt, \quad (2)$$

where N_S and S_{FE} stand for a number of secondary turns and cross-sectional area of the D.U.T., respectively.

To minimize the impact of the shape of the primary current i_P to the measurement of the specific apparent power and the *rms* value of H, the international standard implies that the measurement should be made with a sinusoidal magnetic polarization B /1, 2/. In this case, the *rms* value of the induced voltage u_S, becomes proportional to the maximum value of B:

$$U_S = 4.44 \cdot \hat{B} \cdot f \cdot S_{FE} \cdot N_S, \quad (3)$$

where f is the frequency of the induced voltage.

The main problem when measuring a B-H curve is actually the deviation of the secondary induced voltage (or magnetic flux density B) from an ideal sinusoidal waveform, which is caused by a high (peak) current flowing when the soft-magnetic core is in a magnetic saturation. A deformed secondary induced voltage yields a higher peak current and consecutively declines the secondary voltage waveform from the optimal one, so corrupting the measurement of magnetic field strength. By correcting the shape of the induced voltage u_S, the peak current can be diminished and measurement of H improved!

System Description

One possible method to fulfill the required voltage shape criteria (FF_U) involves a power amplifier with an attached primary winding of the D.U.T. to its output, while the secondary voltage is fed back to its negative input in order to instantaneously control the secondary voltage waveform (Figure 1).

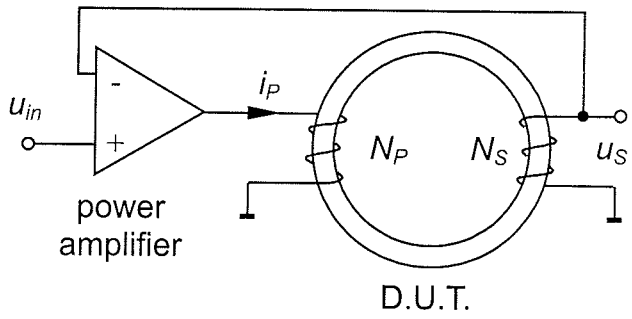

Figure 1: Principle of the power amplifier assisted measurement set-up

The voltage drop in the primary winding of the above set-up is compensated through the control of a power amplifier. Unfortunately, the DC offset voltage of the power amplifier (resulting in the pre-magnetized magnetic core) causes incorrect measurement results. Another potential problem is the power amplifier instability appearing at low impedance loads.

The problem of DC offset voltage can be successfully solved with the measurement set-up shown in Figure 2 /7/. Its main idea is to use an additional matching transformer (Tr.) placed between the power amplifier (PA) and the D.U.T. The matching transformer prevents the D.U.T. from being pre-magnetized with the remaining DC voltage offset at the PA output, which is left uncompensated through the use of a low-pass (LP) filter (f_C = 2 Hz). Since the transformer is a part of the control loop, no special requirements have to be met during its design stage, except that the possible pre-magnetization has to be taken into consideration. To keep the matching transformer size in reasonable limits, the primary feedback loop of the PA is upgraded with a low-pass filter. Due to its low cut-off frequency, it forces only the DC component of the PA output voltage into the summation point, thus reducing the DC pre-magnetization of the D.U.T. In addition, the matching transformer with a proper turn ratio adjusts the low impedance of the device's primary winding to the PA and therefore provides its nominal burden in spite of the primary turns N_P as well as secondary turns N_S reduction.

A request for the measurement set-up is that it must cover a wide range of ring core assortments with the possibility of the secondary voltage as well as primary magnetizing current swinging in wide dynamic ranges. Attempts to fulfill this demand can lead to PA instability or to measurement inaccuracy due to the insufficient signal to noise ratio. In order to raise the measurement accuracy, depending basically on the sensitivity of the magnetic flux evaluation that is obtained by means of numerical integration of the induced secondary voltage /3/, and expand the measurement range, programmable gain amplifiers (PGA) were installed in both measurement paths terminated with 12-bit analog-to-digital converters (ADCs) as well as in the negative feedback control loop.

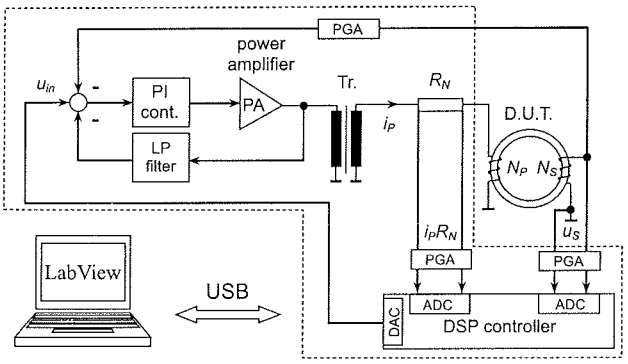

Figure 2: The proposed experimental set-up

Upon the given core data (outer diameter (O.D.), inner diameter (I.D.), height (H) and filling factor) and the preferred magnetization level, the appropriate gain is set by a digital signal processor (DSP). The same DSP also cares for data capturing and the generation of a sinusoidal reference voltage u_{in}.

Because the described system already comprises a DSP controller, an additional superior control loop is implemented in it, which further improves the overall accuracy of the secondary induced voltage u_S.

Superior Control Loop Design

The superior control of the described system is comprised of two successive controllers which are not active at the same time. The first is an I-like fuzzy logic controller (FLC) which oversees the magnitude of the reference voltage u_{in} necessary to achieve the desired amplitude of the induced secondary voltage u_S. It is activated every time the reference voltage is changed and deactivated when the secondary voltage u_S reaches the desired value. The second controller (enabled when the FLC is deactivated) is based on a repetitive (integral) action method which corrects the shape of the generated reference signal u_{in} in order to achieve a sinusoidal induced secondary voltage with a *THD* as low as possible. The requirement for minimal *THD* is a consequence of the desired form factor FF_U. The corrector basically adds a correction waveform u_{cor} to the sine reference voltage effectively forming the input waveform u_{in}'.

Fuzzy Logic Controller

Because of the design of the system it is impossible to accurately predict the amplitude of the secondary induced voltage in relation to the voltage applied on the primary winding. This is made worse by the DSP not knowing what kind of soft-magnetic material is being analyzed. The only known fact is that the ratio of the secondary induced voltage to the primary applied voltage (κ) varies from almost 1 to approximately 0.8, in dependence of the D.U.T., number of primary and secondary winding turns and gain factor of the power amplifier's feedback control loop.

Because of stated reasons behind the uncertainty of the amplitude of secondary voltage an I-like FLC is used to control the amplitude of the primary voltage u_{in}. There are two demands it must fulfill:

- it must convey the secondary induced voltage to its predestined value in at least ten periods and
- it must not overshoot.

The first demand is based on the maximum measurement time allowed, while the second is inherent of the measurement method itself: because the D.U.T. is in an unknown state (usually pre-magnetized) it must be demagnetized before the first measurement could take place. This is achieved by bringing the device close to saturation and then back down to zero. The problem arises if/when the D.U.T. enters deep into the saturation region and the current exceeds all anticipated values. At this point the induced secondary voltage is not sinusoidal any more and amplitude measurement/calculation becomes impossible thus hindering the functioning of the FLC.

The I-like FLC is of SISO type: the (single) input is the degree of deviation of the amplitude of the secondary induced voltage u_S from the desired value u_{Sref} (which is an internal DSP value send by the PC). The deviation is calculated as:

$$e = u_{Sref} - u_S, \tag{4}$$

where:

$$u_S = \kappa \cdot u_{in}. \tag{5}$$

The (single) output of the FLC (u_{in}) is the scaled (internal) sinusoidal reference waveform u_{ref}:

$$u_{in} = \alpha \cdot u_{ref}. \tag{6}$$

The gain α of the I-like FLC is altered until the voltage u_{in} produces the desired secondary induced voltage u_S ($e = 0$) in which case the attenuation of the system κ is completely compensated.

The action of the FLC is divided in dependence of the error e in four regions: L, M, S and Z. If the deviation e is very large (region L), the increase (or decrease) of the reference voltage u_{in} is large (meaning a small integral constant) and if the deviation is small (region S), the increase (or decrease) of the reference voltage is small (large integral constant). When the amplitude of the secondary induced voltage coincides with the desired value, the FLC sets the integral constant to zero and so effectively disabling itself and starting the repetitive action controller (see next chapter).

The cross points of the five regions are calculated from the known parameters of the source and the D.U.T. and their values are set to bring the secondary voltage to its final value in about ten periods. The initial integral constant of the FLC is calculated approximately and is chosen in a way to cause a change of secondary voltage of not less then about 12.5 % (taking into account an approximation of the

system attenuation). All the subsequent incrementations (or decrementations) can be only equal to or smaller than the initial value.

Repetitive Control Method

The proposed control method for the pertinent system is a variant of a repetitive action control method /8/, which is especially suitable for correcting periodic signals (of voltage and/or current). In the past, repetitive control methods have seen extensive application where correction of a periodic waveform is required /9 - 12/ (e.g. motor control applications and PWM switching power supplies like UPS devices), mainly because of their reliable operation, low cost and ease of implementation. In our case, we chose an integral repetitive action control method since the output waveform of the amplifier and the disturbance are always periodic, even when a nonlinear load is supplied by the voltage power amplifier /8, 13/. The control principle moreover does not depend on internal control loops of the voltage power amplifier nor does it require any special knowledge about its parameters. Besides the periodic occurrence of disturbances, the only condition that must be met for the implementation of the control principle is the stability of the amplifier.

A simplified representation of the voltage power source is shown in Figure 3. The periodic disturbances causing output voltage distortions are summarized in a load-dependent disturbance signal d, which is chosen intentionally to simplify the analysis. It is especially appropriate when analyzing the impact of periodic disturbances and nonlinear distortion of output voltage of a power supply with a nonlinear load.

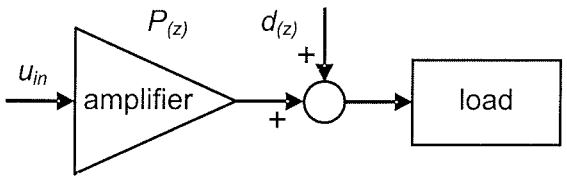

Figure 3: Described system in z domain with disturbance signal d.

Regardless of the type of repetitive control mechanism, they all rely on operation of a discrete number of period-based correctors. Figure 4 shows a plug-in repetitive controller /14/ processing the error ε, which is (at least in the first correction period) the difference between the input reference waveform u_{in} and the actual output waveform u_S. The calculated and stored values of the error $\varepsilon_{(n,T)}$ are used to form a periodical correction waveform u_{cor}, which is added to the original (in most cases a sine wave) reference waveform u_{in}, thus effectively reducing the error of the output waveform of the amplifier/compensating the disturbance d.

The basic idea of the repetitive controller is that a period T of the reference (and sampled output) voltage is divided in N discrete intervals of duration τ (where $T = N \cdot \tau$). In each interval n, the acquired sample of the amplifier output voltage $u_{S(n,T)}$ is subtracted from the reference value $u_{in(n)}$. The calculated error $\varepsilon_{(n,T)}$ at the present discrete interval n in a particular period T is then stored twice: unmodified in a table of correction values (which has N different positions) at the position corresponding to the discrete interval n, and scaled by $G_{(z)}$ in a second correction table (with N positions) at position n too. The same procedure is applied to all the intervals in a given period of the generated waveform.

In the next period ($T + 1$), the unmodified value of the error of a particular interval n (of the previous period) is scaled by the factor K_r and added to the other (already scaled) value of error of the previous period interval n. The sum of both values form a quant of the correction waveform:

$$u_{cor(n,T)} = K_r \cdot \varepsilon_{(n,T)} + \sum_{i=0}^{i=T} G_{(z)} \cdot \varepsilon_{(n,i)}, \qquad (7)$$

which is summed up to the reference voltage $u_{in(n)}$ and the result is a new input waveform:

$$u_{in}'_{(n,T+1)} = u_{in(n)} + u_{cor(n,T)}. \qquad (8)$$

The output voltage $u_{S(n,T+1)}$ of the amplifier is meanwhile sampled again and the new error $\varepsilon_{(n,T+1)}$ in a specific interval is recalculated. It is stored unmodified in the first table and scaled by $G_{(z)}$, summed to the previously scaled and stored error $\varepsilon_{(n,T)}$ of the n-th interval and stored again at the corresponding position in the (second) table of correction values for subsequent use in the following period ($T + 2$).

Owing to the repeating execution of the correction procedure, the (second) table of scaled errors contains the sums of all past errors $\varepsilon_{(n)}$ of all specific correction intervals n independently. Consequently, the correction waveform

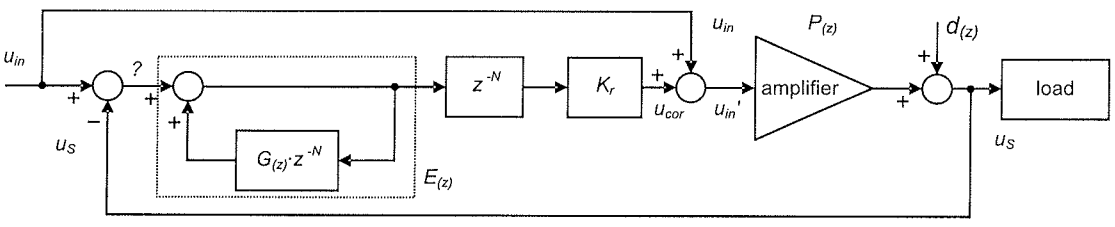

Figure 4: Block diagram of a classic repetitive action control method in z domain.

$u_{cor(n,T)}$ behaves as if it is formed with the help of N correctors, each correcting the value of one interval n. Due to the nature of the control method, a sub-cycle response is impossible, meaning that the error detected in a certain period can be suppressed at best in the following period.

Figure 4 shows a block diagram of the described control method in z domain, where the time delay unit z^{-N} delays the computed correction waveform for one entire period T (composed of N samples). Similarly, a time delay unit z^{-1} delays the execution for one sample. The key element of the repetitive action controller is the inner loop with the internal model $G_{(z)} \cdot z^{-N}$. Its closed loop transfer function is:

$$E_{(z)} = \frac{1}{1 - G_{(z)} \cdot z^{-N}}, \qquad (9)$$

where $G_{(z)}$ can be a constant or a function of z, e.g. a low-pass filter /15/ or a second order filter. In the time domain, this internal model is an integrator (if $G_{(z)} = 1$) summing up the error ε of the n-th correction interval from the first to all successive periods. As explained before, this sum is used to correct the n-th interval of the reference waveform.

While the implemented correction method was tried out and found to be good, at some point it aroused concerns linked with the usage of data memory space of the DSP in which the calculations where executed. Consecutively, a modified version of the correction method was implemented (Figure 5), which required one memory table less then the previous method and had some other modifications:

- the function $G_{(z)}$ of the closed loop model $I_{(z)}$ was chosen to be/set to one so effectively making the closed loop model $I_{(z)}$ a proper integrator,
- an additional proportional model Q, used before the closed loop model $I_{(z)}$ was introduced, which regulates the export of the error ε which is added to the already stored errors,
- the constant K_I was dropped,
- two time advance units (z^q and z^h) were added.

Although it was later found out, that the memory concerns were groundless, the correction method was retained. Its advantages were shorter calculation time and reduced data memory usage while having better stability and roughly the same ability to suppress waveform distortions (or lower *THD*).

Repetitive Action Control Method Implementation

Both described control methods (classic and adapted) were implemented in the described B-H analyzer and tested. They work well, although with some distinctions in speed and accuracy. While the first is a little better in terms of the ability to reduce *THD*, the second allows for a wider deviation of the parameters of the regulator from the optimal value with minimal deterioration of *THD*.

The reference signal u_{in} in both implementations consists of 1000 samples per period. This was also the sampling rate of the AD converter, meaning that the correction waveform u_{cor} is also formed of the same number of intervals. Taking into account the Nyquist theorem, frequencies up to 50 kHz were sampled and corrected.

The implemented correction method has also two time advance units:

- z^q in the direct path, which is used for correcting the various time delays (caused by the sampling time of the ADC, the conversion time of the digital-to-analog converter (DAC) and other time delays) and without which the actual realization of the correction method would not work,
- z^h in the feedback branch, which implementation is not necessarily required, but it is useful to reduce the amplitude of the correction waveform u_{cor} caused by the phase shift between the input and output of the system.

Measurements

All the following measurements were made on an experimental model of the described B-H analyzer. The frequency domain analyses were made by means of a dynamic signal analyzer HP35665A. The measured frequency range was 0 to 3.2 kHz and a flat top windowing method was selected. For the *THD* calculation the harmonic components up to the 64th were observed and averaged over 30 measurements. The D.U.T. was a thin metal M0 silicon-iron toroidal core O.D./I.D./H.: 53/39/18 mm with two primary and two secondary winding turns.

Figure 6 shows test conditions without and with the repetitive action control method enabled and after the desired value of the secondary voltage amplitude has been set by

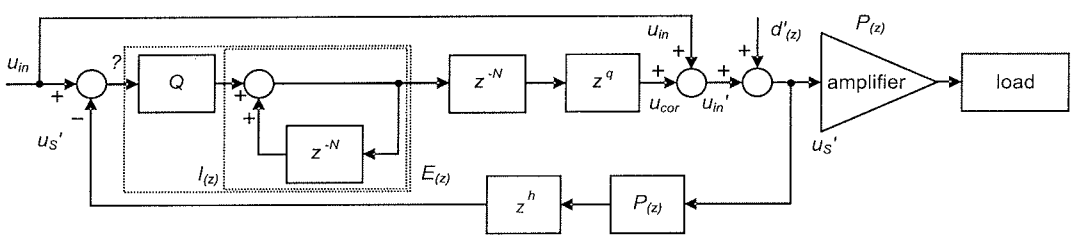

Figure 5: Block diagram of the implemented repetitive action control method in z domain.

the FLC. Shown are the secondary induced voltages, which are proportional to magnetic flux density B (3), and currents, which are proportional to magnetic field strength H (1). The voltage waveform u_{Scor} is shifted up by 0.2 of a division because off a better visual distinction from the u_S waveform, while currents i_P are not.

The voltage was set to 120 mV peak, which for the D.U.T. corresponds to a magnetic flux density of 1.600 T. The D.U.T. was clearly in magnetic saturation. In the case of uncorrected secondary voltage the calculated form factor FF_U was 1,113 % (which is well within the parameters prescribed by the standard). The effective value of magnetic field strength in this instance was 28.3 A/m.

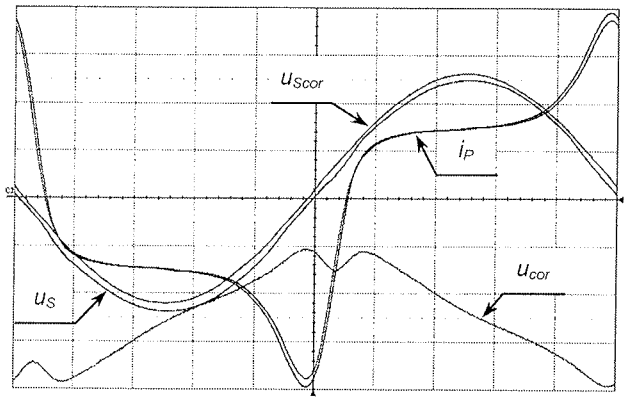

Figure 6: Secondary voltages u_S, *corrected secondary voltage* u_{Scor}, *primary currents* i_P *and correction waveform* u_{cor} *(*k_{Us} *= 200 mV/div,* k_{ip} *= 2 A/div,* k_{Ucor} *= 2 mV/div,* t *= 2 ms/div)*

In the second case, with the correction enabled and the same reference magnetic flux density, the calculated form factor was 1.1108 %. The measured effective value of magnetic field strength was 27.7 A/m. From the given values we can calculate, that a 0.2 % change in the form factor contributes to a 2.16 % decrease in the magnetic field strength.

Figure 6 shows also a fifth signal which is the correction waveform u_{cor} needed to achieve the low-distortion secondary induced voltage u_{Scor}. The waveform is again shifted down by 2.5 divisions because of clarity.

Both secondary voltage waveforms were analyzed in the frequency domain and their relative frequency spectra are shown in Figures 7 and 8. The first figure shows the frequency spectrum of the uncorrected and corrected voltage waveform of Figure 6 when the gain factor (Z) of the power amplifier's feedback loop was set to 1. The gray curve is the frequency spectra of the uncorrected voltage u_S. The measured *THD* is about 1.656 % and it was caused mainly by odd higher harmonics components between the 3rd and the 23rd. The black curve represents the conditions of the corrected system. The measured *THD* was 0.04 %. A slighter increase in the 52th and 53th higher harmonics can be observed which were preliminary absent.

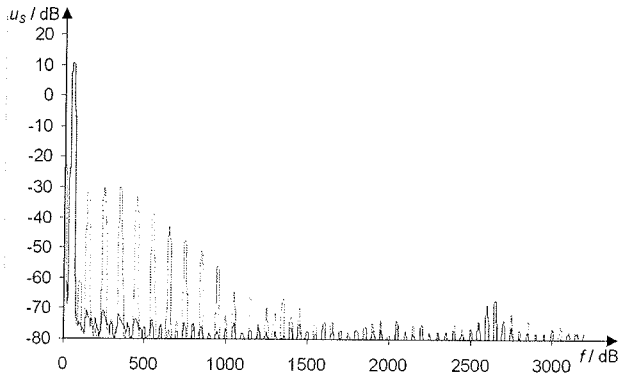

Figure 7: Frequency spectrum of an uncorrected and corrected system (Z = 1)

Another set of the same measurements was done, but with the gain of the power amplifier's feedback loop (Z) set to 4. The *THD* was in overall lower: 0.408 % with the correction disabled and 0.017 % with the correction enabled.

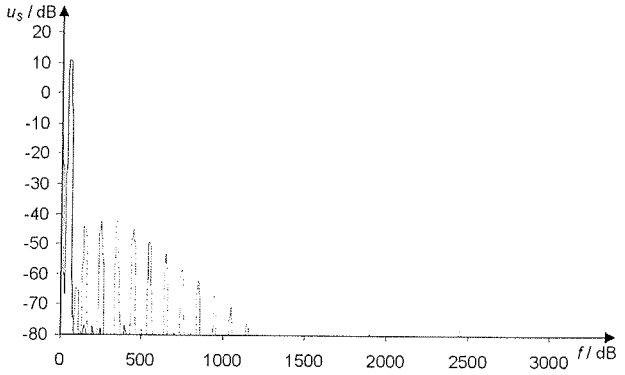

Figure 8: Frequency spectrum of an uncorrected and corrected system (Z = 4)

As can be seen from the figure above, the use of the gain factor in the power amplifier's feedback loop can greatly improve the *THD* factor because it forces a larger input voltage u_{in}, which can be set with greater accuracy. On the other hand, the gain factor must be used with care because of system stability concerns.

The following figure shows a B-H curve of the D.U.T. used for the presented measurements measured with the described system and with the repetitive action controller enabled.

As stated before, the same measurements were also done on a system controlled with a classical correction method (as seen in Figure 4). The acquired figures are not recorded in this paper because they deviate only minimally from the already presented. The measured form factor was the same while the calculated *THD* with correction enabled was actually a bit better: 0.016 %.

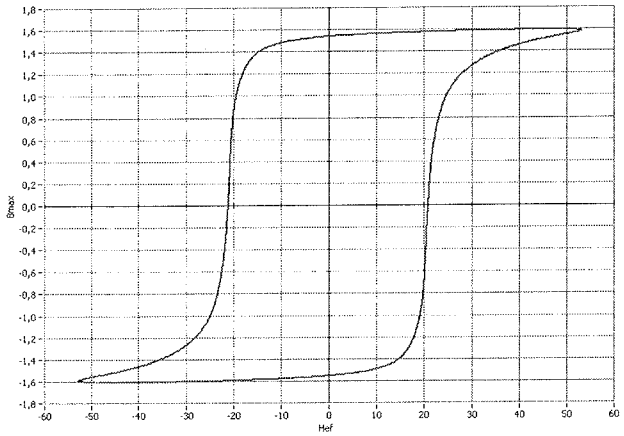

Figure 9: B-H curve of the D.U.T.

Conclusion

The aim of the presented paper was the comparison between an uncorrected measurement set-up suitable for measuring magnetic field strength *H*, which was based on a feedback power amplifier and was already compliant with the tolerances imposed by the standard defining magnetic measurements, with the same supply set-up, but upgraded with a superior digital control loop. Two repetitive action control methods were implemented. Their goal was to achieve a better, more faithful reproduction of a sinusoidal waveform secondary induced voltage.

The first tested was a classical repetitive action correction method. Its use proved to be very effective in reducing the *THD* level of the secondary induced voltage u_S. The drawback was the fine tuning of parameters that it required for achieving the best results and possible problems with system stability if they were mismatched.

The second correction method was a modified version of the previous one, which required less parameters optimization. It yielded slightly worse error correction (greater *THD*), but it was much more robust. Nonetheless, the achieved results of form factor improvement were very good and at the end it was the chosen one because of ease of implementation and usage. The slightly greater *THD* it produced was so small, thet it did not weigh up its other advantages.

With the use of the repetitive action control method improvement on magnetic field strength *H* measurements are more than perceivable. Although a couple of percents improvement (reduction) of *H* can not seem much, it can aid the end user's decision making process when choosing a soft-magnetic core.

References

/1/ International standard IEC60404-2, Methods of measurement of magnetic, electrical and physical properties of magnetic sheet and strip, 1996.

/2/ Deutsche Norm DIN 50 460, Bestimmung der magnetischen Eigenschaften von weich-magnetischen Werkstoffen, 1988.

/3/ E. Carminati, A. Ferrero, A Virtual Instrument for the Measurement of the Characteristics of Magnetic Materials, *IEEE Trans. Instrum. Meas.*, vol. 41, pp. 1005 - 1009, Dec 1992.

/4/ A. Boglietti, P. Ferraris, M. Lazzari, M. Pastorelli, F. Profumo, New Power Supply Method for Soft Magnetic Material Characterization at High Flux Density Values, *IEEE Trans. Magn.*, vol. 28, pp. 2459 - 2461, Sep 1992.

/5/ L. D'Alessandro, A. Ferrero, A Method for the Determination of the Parameters of the Hysteresis Model of Magnetic Materials, *IEEE Trans. Instrum. Meas.*, vol. 43, pp. 599 - 605, Aug 1994.

/6/ J. Buck J, Automatic Hysteresisgraph Speeds Accurate Analysis of Soft Magnetic Materials, *PCIM*, February 2000, on-line version at: http://www.walkerldjscientific.com/buck.pdf

/7/ M. Petkovsek, J. Nastran, P. Zajec, F. Pavlovcic, D. Voncina, Soft-magnetic ring core measuring system with a decreased number of primary and secondary winding turns, *IEEE Trans. Instrum. Meas.*, vol. 53, No. 2, 2004, pp. 444 - 447.

/8/ N. M. Oldham, O. B. Laug, B. C. Waltrip, Digitally Synthesized Power Calibration Source, *IEEE Trans. Instrum. Meas.*, vol. IM-36, No. 1, pp. 341 - 346, June 1987.

/9/ H. Lavric, D. Voncina, P. Zajec, F. Pavlovcic, J. Nastran, A precision hybrid amplifier for voltage calibration systems, *Inf. MIDEM*, vol. 34, No. 1, 2004, pp. 37 - 42.

/10/ T. Yokoyama, A. Kawamura, Disturbance Observer Based Fully Digital Controlled PWM Inverter for CVCF Operation, *IEEE Trans. Power Electron.*, vol. 9, No. 5, pp. 473 - 480, Sep.1994.

/11/ C. G. Anwar, M. Tomizuka, Plug in Repetitive Control for Industrial Robotic Manipulators, *Proc. IEEE Int. Conf. Robot. Automat.*, pp. 1970 - 1975, May 1990.

/12/ A. Gubisch, P. L. Lualdi Jr., P. N. Miljanic, J. L. West, Power Calibrator Using Sampled Feedback for Current and Voltage, *IEEE Trans. Instrum. Meas.*, vol. 46, No. 2, pp. 403 - 407, Apr. 1997.

/13/ C. Rech, H. Pinheiro, H. A. Gründling, H. L. Hey, J. R. Pinheiro, Comparison of Digital Control Techniques With Repetitive Integral Action for Low Cost PWM Inverters, *IEEE Trans. Power Electron.*, vol. 18, No. 1, pp. 401 - 410, Jan. 2003.

/14/ K. Zhang, Y. Kang, J. Chen, Direct Repetitive Control of SPWM Inverter for UPS Purpose, *IEEE Trans. Power Electron.*, vol. 18, No. 3, pp. 784 - 792, May 2003.

/15/ Y. Ito, S. Kawauchi, Microprocessor Based Robust Digital Control for UPS with Three-Phase PWM Inverter, *IEEE Trans. Power Electron.*, vol. 10, No. 2, pp. 196 - 204, Mar. 1995.

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MERITVE SVETLOBNO-TEHNIČNIH VELIČIN

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Kjučne besede: fotometrija, svetlobni tok, svetilnost, svetlost, osvetljenost, meritev svetlobe

Izvleček: Svetloba je fizikalno gledano elektromagnetno valovanje. Je pa tudi medij, ki omogoča naš vid in dojemanje sveta. Pri tem sodelujejo naše oči, živčni sistem in možgani in pokaže se, da ta sistem ni enako občutljiv za vse valovne dolžine. Zaradi tega je bilo poleg radiometrije, ki se ukvarja z merjenjem elektromagnetnega valovanja, vpeljati tudi fotometrijo, ki pa svetlobo meri tako, kot jo dojema naš vidni sistem. V članku so zato najprej opisane osnove dojemanja svetlobe in osnovne fotometrične veličine. V nadaljevanju pa sledi opis fotometričnih merilnih priprav torej fotometrov. Podana je tudi kratka zgodovina fotometričnih normal, predvsem normale za svetilnost. Na koncu pa je dodan še kratek opis Laboratorija za razsvetljavo in fotometrijo, ki že skoraj 80 let deluje v sklopu Fakultete za elektrotehniko na Ljubljanski univerzi.

Measurements of Photometric Quantities

Key words: photometry, luminous flux, luminous intensity, illuminance, luminance, measurement of light

Abstract: Light is part of the electromagnetic radiation and therefore a physical quantity. On the other hand, light is also a human sensation in similar fashion to sound, taste, smell and warmth. Light can so be considered as a radiation or as our response to it. As a radiation, light can be measured with the help of radiometry and radiometric quantities like radiant flux, radiant intensity, irradiance or radiance. But light as a response to this EM radiations involves also the behavior of our visual system (eye, nerves, brain). Our visual system, like other physical detectors of radiation, reacts only to a certain part of the spectrum. Moreover the sensitivity of the human eye to radiation is not the same for each of the wavelengths of the light. So the photometry was introduced to measure light in such a way that the results correlate with visual sensation that would be experienced by a human observer exposed to the same radiation. In order to fulfill the mentioned aim of photometry, a special function V(l) was introduced, which describes the relative spectral sensitivity of the (average) human eye. This function enables us, to calculate the photometry quantities like luminous flux, luminous intensity, illuminance and luminance from the radiometry ones.

In the paper first the photometry quantities and units are presented. Further the development of photometer, the device for measuring photometrical quantities, is described. Both visual and physical photometers are mentioned. At the end of chapter 3 the modern photometers, based on semiconductor photo-voltaic cell are introduced and its use for measurement of illumination, luminous intensity, luminous flux and luminance are described.

Chapter 5 deals with definitions of photometric units, especially with candela, the unit for luminous intensity. In this chapter also the photometric standards are introduced. The history of candela standard is described from use of candle to the realization of candela with a high accuracy cryogenic radiometer. Also the luminous flux standards and luminance standards are mentioned. In the last chapter some information about the Laboratory of lighting and photometry are given. The Laboratory, which has a 80 years long tradition, is part of the Faculty of Electrical Engineering at the University of Ljubljana, Slovenia.

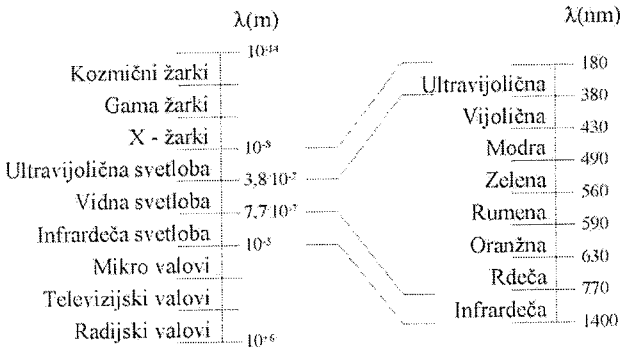
1. Uvod

Svetloba je elektromagnetno valovanje. Svetlobo lahko torej fizikalno obravnavamo enako, kot vsa elektromagnetna valovanja in jo enako lahko tudi merimo. Torej s pomočjo radiometrije. Vendar pa je svetloba tudi medij, ki nam posreduje preko 80% informacij iz našega okolja. Dojemanje svetlobe vključuje človeške oči, živčne povezave in možgane. Pokaže se, da se naš vidni sistem ne odziva na vse valovne dolžine svetlobe (elektromagnetnega sevanja) enako. Zato pri opisovanju oziroma merjenju svetlobe za potrebe vida ne moremo uporabiti radiometrije. Vpeljana je bila fotometrija, ki pri vrednotenju svetlobe upošteva tudi občutljivost človeškega vidnega organa na posamezne valovne dolžine svetlobe.

2. Fotometrija in fotometrične veličine

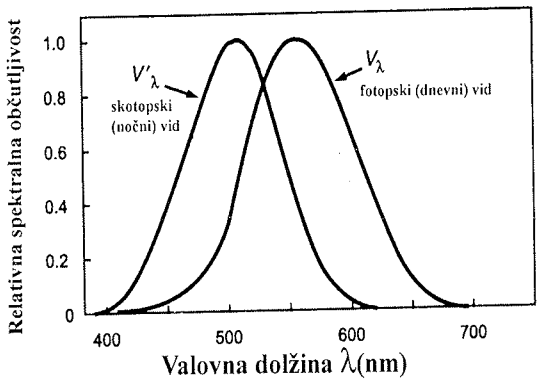
Fotometrija je torej znanost, ki se ukvarja z merjenjem svetlobe. Kot rečeno, svetlobo lahko opišemo fizikalno kot del elektromagnetnega sevanja. In kot tako jo lahko tudi ustrezno merimo s pomočjo radiometrije in radiometričnih enot: sevalnega toka, jakosti sevanja, obsevanosti in sevalnosti.

Človeške oči se ne odzivajo na vse valovne dolžine elektromagnetnega valovanja, ampak samo na valovne dolžine, ki so (grobo) omejene z 380 nm in 780 nm. Pravzaprav lahko le elektromagnetno valovanje s temi valovnimi dolžinami imenujemo svetloba. Pokaže pa se, da se človeške oči tudi ne odzivajo na vse valovne dolžine svetlobe enako. S poskusi in meritvami je bilo dokazano, da rumeno-zelena svetloba v možganih izzove večji občutek svetlosti kot recimo rdeča ali modra svetloba z enako energijo. Na podlagi teh raziskav je bila določena krivulja spek-



Slika1: Delitev spektra elektromagnetnega valovanja

tralne občutljivosti človeškega očesa, ki jo običajno označujemo z V(λ).



Slika 2: Krivulji spektralne občutljivosti človeškega očesa V(λ) in V'(λ)

Tabela1: Relativna občutljivost človeškega očesa na posamezne valovne dolžine pri fotopskem (dnevnem) vidu

Valovna dolžina (nm)	Vrednost krivulje V(λ)	Valovna dolžina (nm)	Vrednost krivulje V(λ)	Valovna dolžina (nm)	Vrednost krivulje V(λ)
380	0,000.04	520	0,710	650	0,107
390	0,000.12	530	0,862	660	0,061
400	0,000.4	540	0,954	670	0,032
410	0,001.2	550	0,995	680	0,017
420	0,004.0	555	1,000	690	0,008.2
430	0,011.6	560	0,995	700	0,004.1
440	0,023	570	0,952	710	0,002.1
450	0,038	580	0,870	720	0,001.05
460	0,060	590	0,757	730	0,000.52
470	0,091	600	0,631	740	0,000.25
480	0,139	610	0,503	750	0,000.12
490	0,208	620	0,381	760	0,000.06
500	0,323	630	0,265	770	0,000.03
510	0,503	640	0,175	780	0,000.015

Krivulja V(λ) ima pri valovnih dolžinah pod 380 nm in nad 780 nm vrednost nič, vrh pa doseže pri 555 nm. Nanaša se na spektralno občutljivost čepnic in torej velja pri dnevnem (fotopskem) vidu. Podobno je definirana tudi krivulja spektralne občutljivosti paličnic V'(λ), ki se nanaša na nočni (skotopski) vid in doseže vrh pri 507 nm.

2.1 Svetlobni tok

Na podlagi omenjene krivulje dobimo iz radiometričnih veličin štiri osnovne fotometrične veličine in enote: svetlobni tok, svetilnost, osvetljenost in svetlost. Preračun sevalnega toka v svetlobni tok lahko opravimo po spodnji enačbi:

$$\Phi = K_m \cdot \int_0^{\infty} \frac{d\Phi_e}{d\lambda} \cdot V(\lambda) \cdot d\lambda \qquad (1)$$

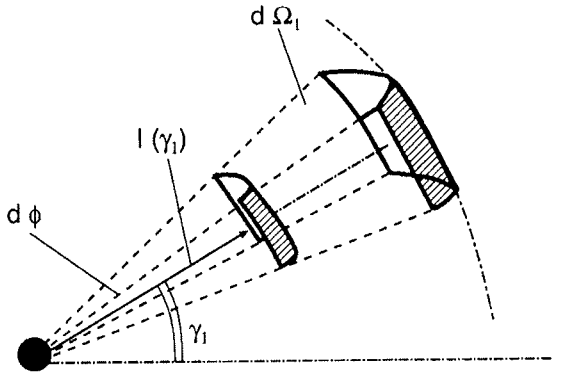
Kjer je Φ svetlobni tok, Φ_e sevalni tok in K_m konstanta z vrednostjo 683 lm/W.

Svetlobni tok (angleško: luminous flux) je merilo za količino energije, ki jo vir seva v prostor. Je ekvivalent moči v "Wattih" vendar z upoštevanjem občutljivosti oči na svetlobo posameznih valovnih dolžin. Enota za svetlobni tok je lumen z oznako lm. Za primerjavo: navadna 100W žarnica ima približno 1300 lm, fluorescenčna sijalka moči 58 W oddaja približno 5200 lm, 90 W nizkotlačna natrijeva sijalka pa kar 13500 lm.

2.2 Svetilnost

Svetilnost (angleško: luminous intensity) odgovarja v radiometriji jakosti sevanja. Predstavlja torej delež svetlobnega toka v določeni smeri oziroma v določenem prostorskem kotu.

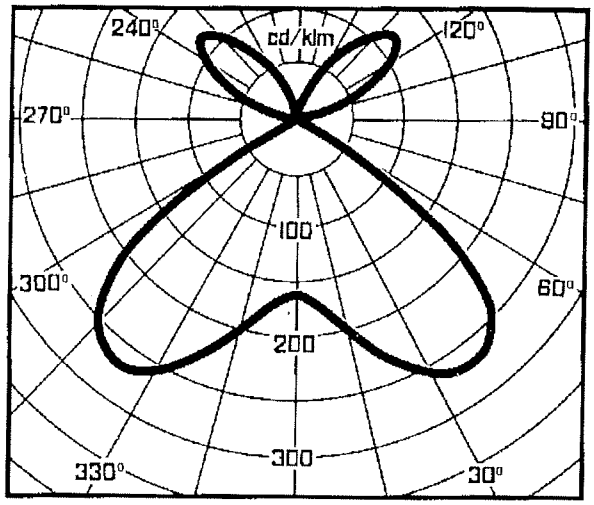
$$I = \frac{d\Phi}{d\Omega} \qquad (2)$$



Slika 3: Predstavitev svetilnosti s pomočjo svetlobnega toka in prostorskega kota

Vsota (integral) svetilnost v vseh smereh okoli vira, oziroma v polnem prostorskem kotu, je torej enaka svetlobnemu toku. Enota za svetilnost je kandela (oznaka: cd), ki je tudi ena od osnovnih enot SI merskega sistema. Zadnja definicija kandele je iz leta 1979 in pravi: 1 kandela (cd) je svetilnost v določeni smeri vira z monokromatsko svetlobo frekvence 540 x 10^{12} Hz, ki ima jakost sevanja v tej smeri 1/683 W/sr.

Svetilnost je odvisna od izbrane smeri, zato jo največkrat podajamo v polarnih diagramih. Nekaj karakterističnih vrednosti: sveča ima svetilnost 0,6 do 1,1 cd, navadna žarnica približno 110 cd, sonce zunaj atmosfere pa kar 3 x 10^{27} cd.



Slika 4: Prikaz kotne porazdelitve svetilnosti v polarnem diagramu

2.3 Osvetljenost

Osvetljenost (angleško: illuminance) je podana kot količina svetlobnega toka, ki konča na določeni ploskvi in je torej ekvivalent obsevanosti v radiometriji. Enota za osvetljenost je torej lm/m^2 oziroma luks (lx).

$$E = \frac{d\Phi}{dA} \tag{3}$$

Osvetljenost pa je možno določiti tudi s pomočjo svetilnosti. Zvezo podaja fotometrični zakon oddaljenosti, ki ga lahko, ob predpostavki, da je ploskev, na kateri opazujemo osvetljenost, pravokotna na smer širjenja svetlobe, zapišemo kot:

$$E = \frac{I}{r^2} \tag{4}$$

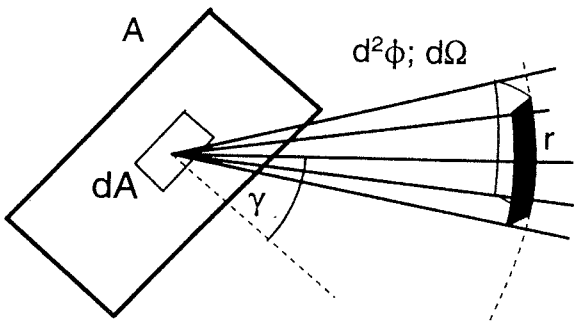
Osvetljenost je fotometrična veličina, ki jo je najlaže izmeriti, zato se jo tudi največ uporablja. Standardi, priporočila in predpisi podajajo tako na primer minimalne vrednosti osvetljenosti na delovnem mestu. Še nekaj karakterističnih vrednosti: osvetljenost poletnega travnika pri jasnem nebu opoldne je okoli 100.000 lx, v senci drevesa pa okoli 10.000 lx, osvetljenost pisalne mize v pisarni je 500 lx, osvetljenost pločnika ponoči pri uporabi ustrezne cestne razsvetljave doseže do 20 lx, na travniku v mesečini pa bi izmerili 0,05 lx.

2.4 Svetlost

Svetlost (opazovane točke) je definirana s pomočjo svetlobnega toka, ki ga točka na izbrani ploskvi oddaja v izbran prostorski kot. Določimo jo lahko po enačbi:

$$L = \frac{d^2\Phi}{dA \cdot \cos\gamma \cdot d\Omega} \tag{5}$$

Pri tem je $d\Phi$ del svetlobnega toka v prostorskem kotu $d\Omega$, dA je del ploskve, ki vsebuje izbrano točko in γ je kot med normalo te ploskve in smerjo snopa.



Slika 5: Prikaz definicije svetlosti

Kadar je opazovana točka del svetleče površine (vira svetlobe), lahko enačbo preoblikujemo tako, da svetlost izrazimo s pomočjo svetilnosti:

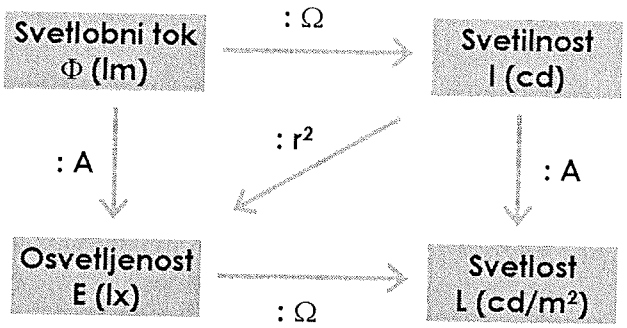
$$L = \frac{dI}{dA \cdot \cos\gamma} \tag{6}$$

Podobno lahko svetlost izrazimo tudi s pomočjo osvetljenosti, če je opazovana točka del osvetljene površine.

$$L = \frac{dE}{\cos\gamma \cdot d\Omega} \tag{7}$$

Svetlost (angleško: luminance) je tudi edina fotometrična veličina, ki jo lahko vsaj približno ocenimo z očmi, saj je v povezavi z občutkom svetlosti (angleško: brightness), ki ga v očesu povzročajo svetle ali osvetljene površine. Nekaj karakterističnih vrednosti: površina sonca ima svetlost 1.600.000 kcd/m2, žarilna nitka navadne žarnice 15.000 kcd/m^2, površina fluorescenčne sijalke 10 kcd/m^2, plamen sveče približno 8 kcd/m2 in mesec (luna) 2,5 kcd/m^2.

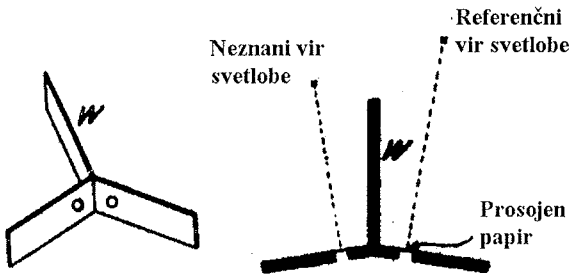
Vse štiri glavne fotometrične veličine so med seboj povezane z ustreznimi enačbami. Povezave so grafično prikazane na spodnji sliki.



Slika 6: Prikaz povezav med osnovnimi fotometričnimi enotami

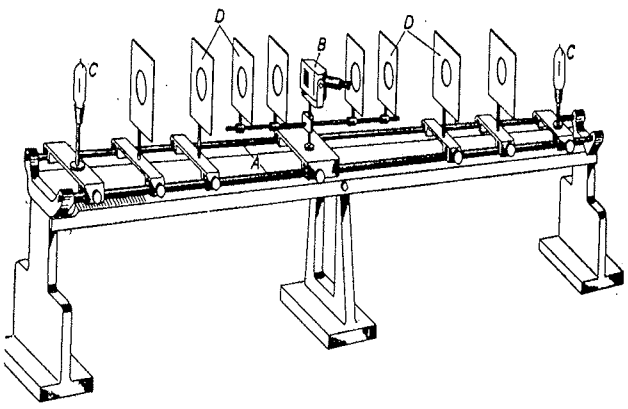
3. Fotometer

Inštrument, s katerim lahko izmerimo katero od fotometričnih veličin, v splošnem imenujemo fotometer. Prvi opis fotometra se pojavi v letu 1729 v delu "Essai d'optique sur la gradation de la lumiere" Pierra Bouguera (1698-1758), profesorja v Havre. Fotometer, ki je prikazan na spodnji sliki, je temeljil na primerjavi svetlosti dveh površin, ki ju osvetljujeta dva različna svetlobna vira. Na podlagi enakih svetlosti obeh površin je možno sklepati o enaki osvetljenosti, ki ju je, s pomočjo znanih (kvadratov) oddaljenosti od enega in drugega vira, možno preračunati v svetilnost neznanega vira. Seveda ob poznavanju svetilnosti drugega vira.



Slika 7: Slika prvega Bouguerjevega fotometra, objavljena leta 1760

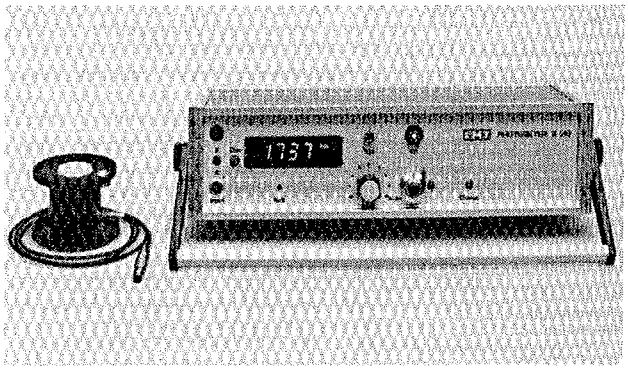
Opisani princip subjektivne fotometrije se je kasneje pojavil še v mnogih drugih znanstvenih delih znanih avtorjev s tega področja kot so Lambert, Thompson, Wedge Trotter in drugi. Zaradi lažjega in točnejšega določanja razdalje so v merilni postopek vpeljali še fotometrično klop, tako da ja priprava za meritev svetilnosti neznanega vira izgledala tako, kot je prikazana na spodnji sliki.



Slika 8: Fotometrična klop (A) s subjektivnim fotometrom (B), neznanim in referenčnim svetlobnim virom (C) in zaslonkami (D).

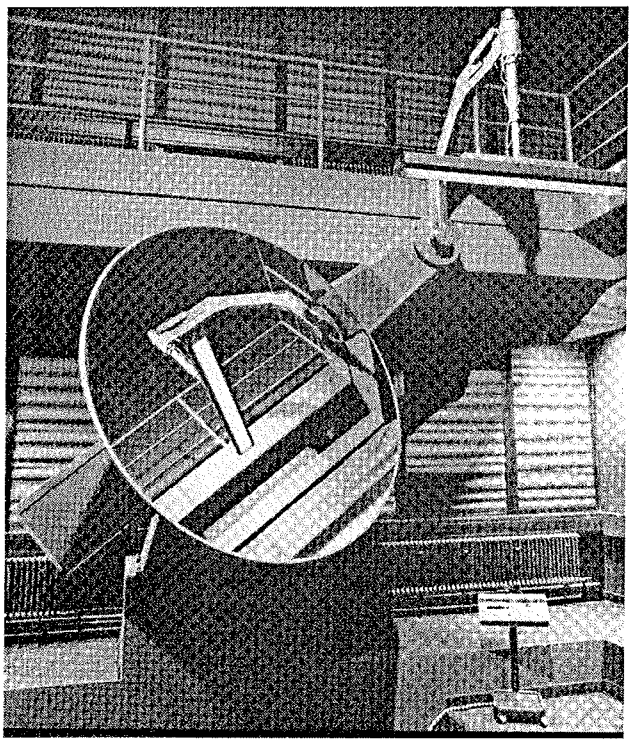
Vendar pa opisane subjektivne merilne metode, kljub natančnosti izdelave optičnih inštrumentov, kmalu niso več zagotavljale ustrezne točnosti.

Danes govorimo o objektivni fotometriji, ki temelji predvsem na optoelektronskih pretvornikih, kot so fotocelica, fotopomnoževalka, fotoupor in fotodioda. Vendar pa se v zadnjem času uporabljajo skoraj izključno le še silicijeve fotodiode. S pomočjo posebnih optičnih filtrov je možno njihovo spektralno občutljivost ustrezno prilagoditi spektralni občutljivosti človeških oči. Ob ustrezni povezavi fotodiode z merilnikom toka tako dobimo merilnik osvetljenosti ali lux-meter.



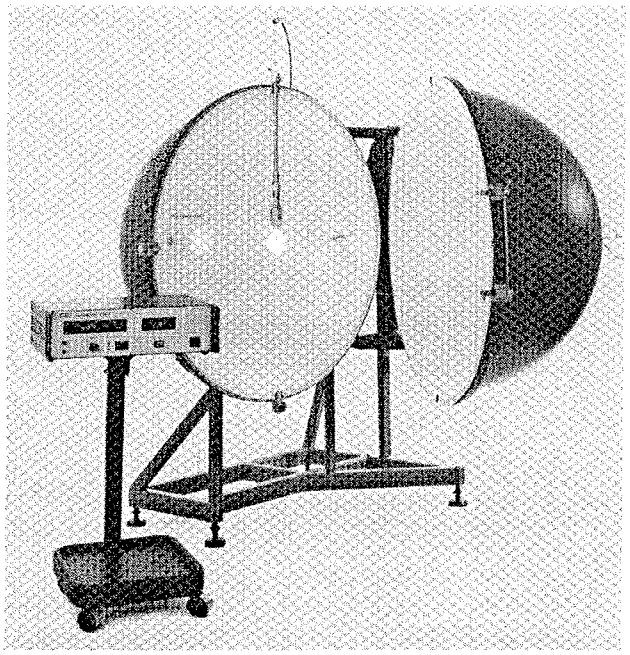
Slika 9: Laboratorijski lux-meter razreda točnosti L

Ostale tri osnovne fotometrične veličine je prav tako možno meriti s fotodiodo oziroma luks-metrom. Seveda ob upoštevanju določenih fizikalnih povezav in zakonov. Svetilnost merimo običajno na fotometrični klopi ob upoštevanju razdalje med virom in fotoelementom, kot je to že bilo opisano pri subjektivni fotometriji.. V kolikor pa nas zanima kotna porazdelitev svetilnosti, lahko uporabimo goniofotometer.

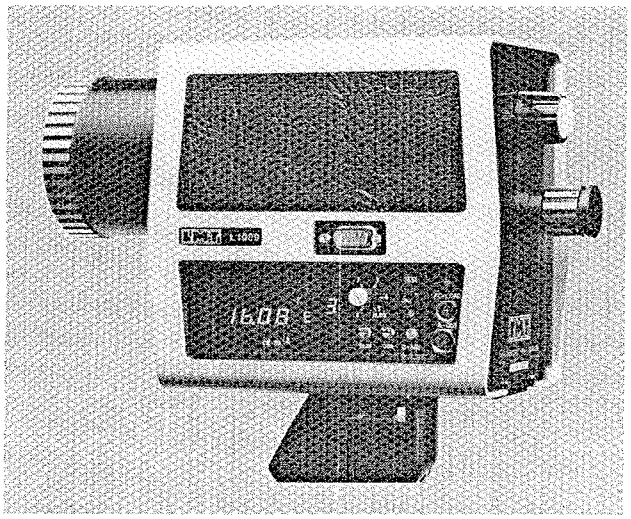


Slika 10:Goniofotometer z zrcalom

Svetlobni tok se prav tako da izmeriti z goniofotometrom in integracijo svetilnosti po celotnem prostorskem kotu. Hitrejša metoda pa je uporaba integrirne (Ulbrichtove) krogle. Opazovani svetlobni vir se namesti v sredino integrirne krogle. Premaz notranje stene krogle z ustreznimi refleksijskimi lastnostmi zagotavlja, da je notranja površina enakomerno osvetljena. Če del notranje površine krogle nadomestimo z fotodiodo oziroma lux-metrom, lahko iz izmerjene osvetljenosti in poznavanja velikosti krogle izračunamo svetlobni tok vira. Lahko pa meritev opravimo tudi primerjalno z virom, katerega svetlobni tok poznamo.



Slika 11: Integrirna krogla



Slika 12: Merilnik svetlosti

Z fotodiodo lahko izmerimo tudi svetlost, in sicer tako, da z ustrezno optično napravo omejimo kot, pod katerim svetloba pada na površino fotodiode. Taki merilni pripravi rečemo merilnik svetlosti. Izvedba je lahko enostavnejša, tako da optični objektiv samo nataknemo za glavo lux-metra. Lahko pa je merilnik svetlosti izdelan tudi z ustreznim okularjem, ki omogoča, da skozi objektiv tudi vidimo področje, katerega svetlost merimo. Opazovani kot je pri merilnikih svetlosti običajno velik 1 ° ali 3 °. Za meritve svetlosti na področju cestne razsvetljave pa se uporabljajo tudi merilniki z manjšimi koti opazovanja (20 ' (ločnih minut) ali tudi samo 6 ').

Zares prenosna fotometra sta samo merilnik osvetljenosti (lux-meter) in merilnik svetlosti. Zaradi tega standard DIN 5032, ki podaja osnove merjenja svetlobe, navaja samo

Tabela 2: Dovoljeni maksimalni pogreški za posamezne razrede točnosti pri merilnikih osvetljenosti po standardu DIN 5032

		Razred inštrumenta			
Pogrešek	oznaka (po DIN 5032)	**L**	**A**	**B**	**C**
prilagoditev V(λ) krivulji	f_1	1,5 %	3 %	6 %	9 %
UV občutljivost	u	0,2 %	1 %	2 %	4 %
IR občutljivost	r	0,2 %	1 %	2 %	4 %
prilagoditev cos φ krivulji	f_2	1,5 %	1,5 %	3 %	6 %
vrednotenje E_0	$f_{2,0}$	10 %	10 %	15 %	20 %
vrednotenje E_z	$f_{2,z}$	5 %	5 %	10 %	15 %
vrednotenje E_{zh}	$f_{2,h}$	5 %	5 %	10 %	15 %
pogrešek linearizacije	f_3	0,2 %	1 %	2 %	5 %
pogrešek kazalnika	f_4	0,2 %	3 %	4,5 %	7,5 %
utrujenost	f_5	0,1 %	0,5 %	1 %	2 %
temperaturni koeficient	α_0, α_{25}	0,1 %/K	0,2 %/K	1 %/K	2 %/K
modulirana svetloba	f_7	0,1 %	0,2 %	0,5 %	1 %
pogrešek odklona	f_{11}	0,1 %	0,5 %	1 %	2 %
skupni pogrešek	f_{ges}	**3 %**	**5 %**	**10 %**	**20 %**
spodnja frekvenčna meja	f_u	40 Hz	40 Hz	40 Hz	40 Hz
zgornja frekvenčna meja	f_o	10^5 Hz	10^5 Hz	10^4 Hz	10^3 Hz

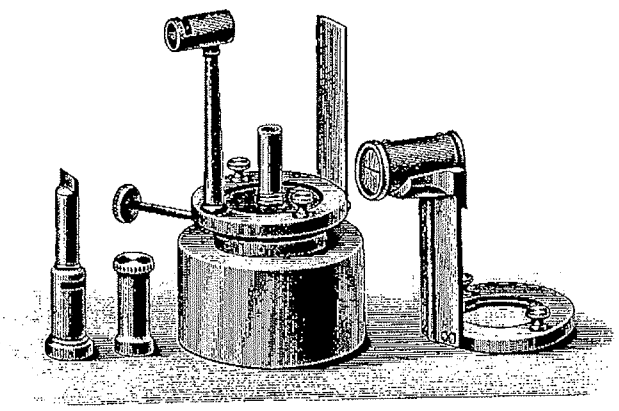
Tabela 3: Dovoljeni maksimalni pogreški za posamezne razrede točnosti pri merilnikih svetlosti po standardu DIN 5032

		Razred inštrumenta			
Pogrešek	oznaka (po DIN 5032)	**L**	**A**	**B**	**C**
prilagoditev V krivulji	f_1	2 %	3 %	6 %	9 %
UV občutljivost	u	0,2 %	1 %	2 %	4 %
IR občutljivost	r	0,2 %	1 %	2 %	4 %
prostorsko vrednotenje	$f_2(g)$	2 %	3 %	6 %	9 %
vpliv svetlosti okolice	$f_2(u)$	1 %	1,5 %	2 %	4 %
pogrešek linearizacije	f_3	0,2 %	1 %	2 %	5 %
pogrešek kazalnika	f_4	0,2 %	3 %	4,5 %	7,5 %
utrujenost	f_5	0,1 %	0,5 %	1 %	2 %
temperaturni koeficient	α_0, α_{25}	0,1 %/K	0,2 %/K	1 %/K	2 %/K
modulirana svetloba	f_7	0,1 %	0,2 %	0,5 %	1 %
pogrešek zaradi polarizacije	f_8	0,2 %	1 %	2 %	4 %
pogrešek odklona	f_{11}	0,1 %	0,5 %	1 %	2 %
pogrešek izostritve	f_{12}	0,4 %	1 %	1 %	1 %
skupni pogrešek	f_{ges}	5 %	7,5 %	10 %	20 %
spodnja frekvenčna meja	f_u	40 Hz	40 Hz	40 Hz	40 Hz
zgornja frekvenčna meja	f_o	10^5 Hz	10^5 Hz	10^4 Hz	10^3 Hz

razrede točnosti za ta dva inštrumenta. Tako za merilnik osvetljenosti kot za merilnik svetlosti so v standardu navedeni štirje razredi točnosti: L, A, B in C. Dovoljeni skupni pogreški so za posamezne razrede podani v tabeli 2.

Normale fotometričnih enot

Zgodovina normal v fotometriji se začne v začetku devetnajstega stoletja, ko so začeli uporabljati plamen sveče kot normalo za svetilnost. Od tod tudi ime enote za svetilnost (kandela), ki izhaja iz angleške besede *candle* za svečo. Taka normala je zadoščala le kratek čas, saj so z izboljšanimi fotometri kmalu odkrili, da je svetilnost plamena sveče zelo težko reproducirati, pa čeprav se predpisali sestavo, obliko in hitrost gorenja sveče.

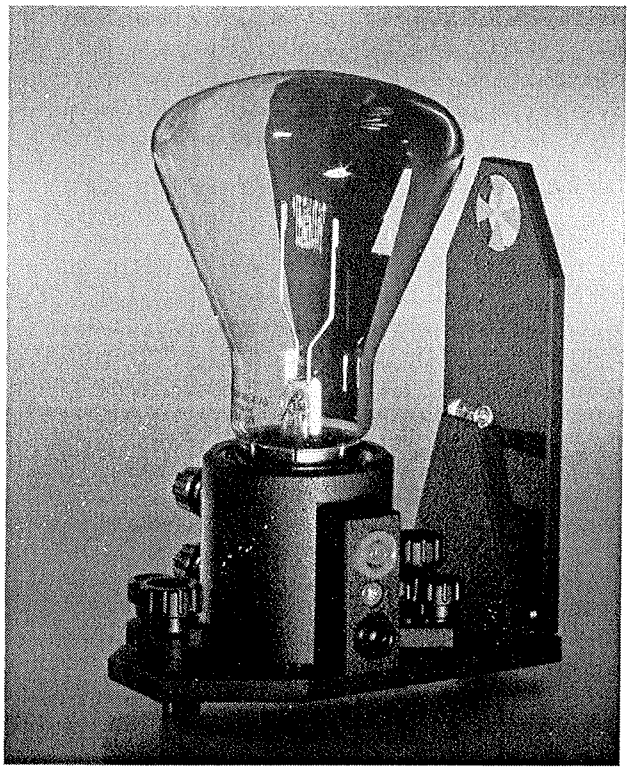


Slika 13:Hefnerjeva svetilka

Zato so svečo kmalu nasledile svetilke s plamenom, ki so uporabljale različne vrste goriva. Poznanih je bilo več vrst, med bolj znanimi pa je bila Hefnerjeva svetilka. Vendar pa se je z razvojem fotometrov tudi pri svetilkah pokazala ista slabost torej slaba ponovljivost svetlosti plamena. Zato so ob koncu devetnajstega stoletja začeli razmišljati o drugačni vrsti normale, ki bi temeljila na črnem sevalu znane površine in temperature. Pojavila so se prva sevala s staljeno platino, imenovana tudi Violla normale. Vendar pa so se tudi pri teh sevalih pojavljale težave zaradi nečistoč v platini, ki so povzročale razlike v svetlosti površine in s tem tudi v svetilnosti normale. V začetku dvajsetega stoletja so nekaj časa razmišljali, da bi normalo za svetlost izdelali v obliki električne žarnice. Vendar pa se je pokazalo, da ni možno dovolj natančno opredeliti in izdelati žarnico, ki bi lahko služila kot absolutna normala. So se pa žarnice uveljavile kot sekundarne normale za svetlost.

Leta 1909 so raziskovanja pripeljala do prvega standarda "mednarodne kandele", ki je temeljil na sevalu iz čistega torija, potopljenega v platino pri temperaturi trojne točke (2042 K). Platino so segrevali v visokofrekvenčni peči moči 7 kW. To normalo je leta 1921 sprejela tudi mednarodna komisija za razsvetljavo (CIE), leta 1948 pa tudi Mednarodna konferenca za mere in uteži. Ob tem so tudi spremenili ime enoti iz *candle* v *candela*.

Leta 1979 pa je Mednarodna komisija za mere in uteži sprejela novo definicijo kandele. Ta pravi, da je kandela svetilnost v dani smeri vira z monokromatskim sevanjem frekvence $540x10^{12}$ Hz, ki ima v tej smeri jakost sevanja 1/683 W/sr. Frekvenca $540x10^{12}$ Hz odgovarja valovni dolžini 555,016 nm v standardnem zraku, to pa je svetloba, na katero so človeške oči najbolj občutljive. Tako danes enota za kandelo ni več predstavljena s sevalom, pač pa na podlagi absolutne občutljivosti ustreznega detektorja (npr. visoko-točni kriogeni radiometer). Še vedno pa je kandelo možno predstaviti tudi z črnim sevalom.



Slika 14:Električna žarnica kot normala za svetilnost

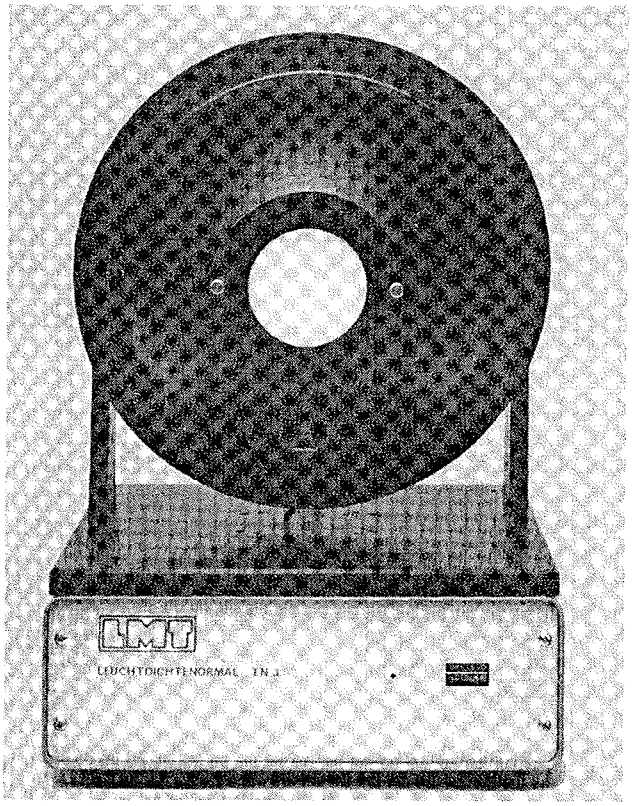
Poleg normal za svetilnost uporabljamo v fotometriji še normale za svetlobni tok ter normale za svetlost. Normale za svetlobni tok so večinoma izvedene v obliki žarnic. Lahko pa uporabimo tudi druge električne svetlobne vire, na primer fluorescenčne sijalke. Vendar pa moramo v tem primeru uporabiti tudi ustrezno umerjeno predstikalno napravo. Normale za svetlobni tok se uporabljajo pri primerjalnem merjenju svetlobnega toka v integrirni krogli. Sicer pa slednja omogoča tudi absolutno merjenje svetlobnega toka, tako da normala ni vedno potrebna.

Na podobnem principu kot integrirna krogla deluje tudi normala za svetlost. Sestavljena je iz manjše krogle v kateri je nameščen vir svetlobe, običajno žarnica. Notranja stena je obdelana s premazom, z visoko odsevnostjo z Lambertovo kotno porazdelitvijo, zaradi česar je osvetljenost notranje površine krogle enakomerna. Nato manjši del stene krogle nadomestimo okencem, ki je lahko prekrito s prosojnim materialom. Površina okenca ima zaradi enakomerne osvetljenost tudi enakomerno svetlost. Tako normalo se da umeriti s pomočjo merilnika osvetljenosti pri znani razdalji med njima in njuni geometriji.

Ne poznamo pa normale za osvetljenost. Merilnike osvetljenosti (lux-metre) zato umerjamo s pomočjo normale za svetilnost in znane razdalje med njima v skladu s fotometričnim zakonom oddaljenosti (enačba 4).

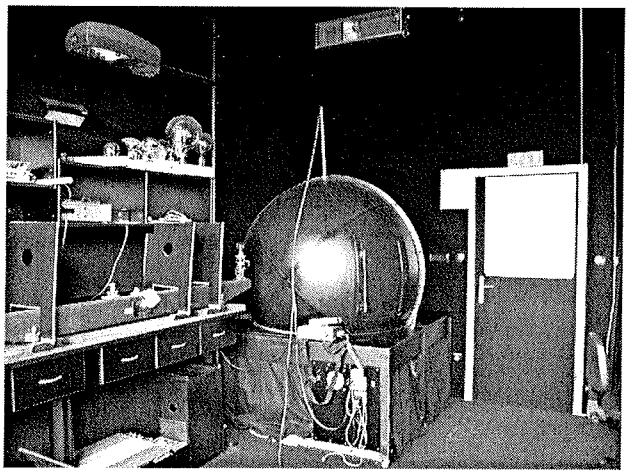
Laboratorij za razsvetljavo in fotometrijo

Laboratorij za razsvetljavo in fotometrijo se nahaja na Fakulteti za elektrotehniko Univerze v Ljubljani. Je eden od slovenskih merilnih laboratorijev z najdaljšim stažem.



Slika 15:Normala za svetlost

Ustanovljen je bil že jeseni leta 1921, ko se je Elektrotehniški oddelek takratne Tehniške fakultete preselil v nove prostore na Aškerčevi. Laboratorij se danes sicer nahaja v drugih prostorih, vendar je še vedno tako kot takrat "ves v črnem, ne le stene ampak tudi pod in oknice, ki zastirajo svetlobo, so črne" (citat iz knjige Zgodovina slovenske univerze v Ljubljani do 1929, izdane 1929).



Slika 16:Notranjost laboratorija

Vse od takrat se laboratorij uspešno razvija. Danes lahko v laboratoriju izvajamo praktično vse fotometrične meritve. Za merjenje svetlobnega toka je na voljo več normalnih žarnic in integrirna krogla. Meritev svetilnosti je možna na

fotometrični klopi dolžine 2 m ob uporabi različnih normalnih žarnic. Izdelali smo tudi preprost goniofotometer, ki omogoča osnovno merjenje kotne porazdelitve svetilnosti. Merjenje osvetljenosti je možno s precizijskim luks-metrom razreda L ter z različnimi prenosnimi luks-metri. Svetlost pa lahko izmerimo s pomočjo kombiniranega merilnika svetlosti, ki je hkrati tudi spektroradiometer. Torej nam omogoča tudi meritve spektralne vsebine svetlobe, barve svetlobe in indeksa barvnega videza. Na voljo so tudi stabilizirani viri enosmerne in izmenične napetosti ter merilni inštrumenti električnih veličin.

Z opremo v laboratoriju (normalnimi žarnicami in fotometrično klopjo) je možno umerjati merilnike osvetljenosti. V laboratoriju izdelane normale za svetlost pa omogočajo tudi umerjanje merilnikov svetlosti. Z uporabo normalnih žarnic, fotometrične klopi in integrirne krogle je možno umerjanje delovnih normal za svetlobni tok in svetilnost.

Poleg z meritvami, se v laboratoriju ukvarjamo tudi z razvojem merilne opreme. Eden zadnjih projektov je razvoj merilnika svetlosti na osnovi digitalne kamere. Prednost takega merilnika je, da omogoča tudi merjenje svetlosti majhnih površin, na primer presvetljenih piktogramov na stikalih. Del dejavnosti pa predstavlja tudi projektiranje razsvetljave in izračuni osvetljenosti in svetlosti v notranjih in zunanjih prostorih.

Laboratorij za razsvetljavo in fotometrijo trenutno še ni akreditiran za kalibracijo fotometričnih inštrumentov, se pa trudimo, da bi ta korak čim prej opravili.

Literatura

- Casimer DeCusatis, Handbook of Applied Photometry, American Institute of Physics, 1997
- Hans-Jürgen Hentschel, Licht und Beleuchtung, Hütnig Verlag Heidelberg, 2002
- Jahn W. T. Walsh, Photometry, Dover Publications Inc., 1958
- Joseph B. Murdoch, Iluminating Ingineering, Visions Communications, 2003
- Dietrich Gall, Grundlagen der Lichtechnik, Pflaum Verlag, 2004
- Arne Valberg, Light vision color, Wiley, 2005
- Katalog izdelkov LMT, LMT Berlin, 1998
- Grega Bizjak, Meritev svetlobno-tehničnih veličin, Posvet o meritvah TC Semto, Ljubljana, 2005

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O MERILNI TEHNOLOGIJI Z VIDIKA PODJETNIŠKEGA MIKROOKOLJA

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Kjučne besede: meritev, inovacija, metrologija, podjetje, globalnost, dodana vrednost, strošek, povezovanje, strategija, mikrookolje, makrookolje

Opisani so vidiki položaja podjetja v panogi merilne tehnike in v obdobju globalizacije.Posebej so poudarjeni notranji poslovni procesi v podjetju,položaj podjetja v globalnem okolju in pomen povezav in sodelovanja.Izraziteje so opredeljene spremembe v vsebini in delovanju mikrokolja v podjetju.

About metrology from entrepreneurial microenvironment point of view

Key words: measurement, innovation, metrology, globalisation, added value, cost,price, interconnection, strategy, microenvironment, macroenvironment

Era of globalisation at one hand and possibilities of positioning of the hightech company in the field of measurement technology on other hand is described. Integration of measurement in sophisticated engineering solutions is present in new produts and services. Therefore, there are more and more equipment with analysing and diagnostics perfornamance present on the market. Industry metrology is driving force for new products and services.

Quality should be measured and it is done by measurement of parameters and characteristics.

A company on global market is affected by different pressure like dangers and opportunities. Technology itself is not enough for the succes of the company. Management of the intellectual property in the company is a key issue to the success.

Open innovation circle is very important to realise most competitive solutions with best inputs and resources. Innovations portfolio in the company shows the presence of various innovation steps like continuous, by leaps and radical, innovation. All the time Business Opportunity Evaluation is part of decision making process. Collaboration of the company with the partners is very important but it must be part of core stratey, vision and goals. Analysig of mistakes in cooperation is very useful to improve relatioships. Only 30% business relationships are succesful, nearly 70% are finished premature.

Microenvironment of the company is most oriented to this categories of creations:

- permanet innovating
- strategyc planning
- customer is first
- R&D processes
- Manufacturing process
- Total predictive maintenance
- six sigma quality criteria
- cell manufacturing
- standartisation activities
- products placing
- purchasing marketing
- management of reductions
- continuously improvements
- measurement of succes

Uvod

Poslovno udejstvovanje na področju ustvarjanja dodane vrednosti v povezavi z izdelki in storitvami merilne tehnologije sodi v področje takoimenovanih »visokih tehnologij«. Tudi zato in ne samo zato je to področje, ki je v intenzivnem razvoju in kot tako tudi zelo razširjena strokovna disciplina v večini področij človekovega ustvarjanja in projektiranja naprav moderne dobe.

Temeljne zakonitosti metrologije povezane z novimi tehnologijami in merilnimi metodami ob uporabi mikroprocesorjev in druge proračunalniške koncepcije nudijo vsak dan nove naprave pa tudi nove do včeraj še neaktualne storitve. Nekatera podjetja delujejo tudi alternativno na povsem novih principih lahko bi rekli nadkukorenčno.

To pomeni iskanje še neodkritih priložnosti za določeno skupino uporabnikov.

Danes opažamo, da se je meritev sama, kot fizikalna operacija enostavno skrila v celovitost rešitve inženirskega izziva na določenem pojavu. Čeprav je meritev večkrat prektrita z procesiranjem, obdelavo signala in drugimi tehnološkimi danostmi še vedno nastopa v svojem bistvu ko je merjenje skupina eksperimentalnih postopkov, ki imajo za cilj določitev ene veličine. Merjenje je tudi proces primerjave vrednosti neznane veličine z veličino, ki je vzeta za enoto mere.

Znanstvena disciplina, ki tudi podpira gospodarske učinke podjetništva v področju merilnih tehnologij je Metrologija. Metrologija je znanost, ki se ukvarja:

- z metodami merjenja veličin
- realizacijo in vzdrževanjem etalonov fizikalnih veličin
- razvojem in izdelavo merilnih naprav
- obdelavo, analizo, pomnjnejm in prenosom merjenih rezultatov

Merjenje je nastalo kot rezultat potrebe za ugotavljanje količinskih (kvantitativnih) karakteristik naravnih pojavov in je neposredno rezultat potrebe po primerjavi. Od samega opažanja naravnega pojava na merjenje letega se je prišlo ravno zaradi razvoja znanosti v 17. stoletju/F. Bekon/.

Metrologija je razvejana na zakonsko, industrijsko in znanstveno metrologijo.

Zakonska metrologija je področje, ki ga določa država z zakoni in predpisi. Zakonska metrologija zagotavlja :mersko enotnost v državi, razvoj metrologije v skladu s tehnološkim razvojem države, povečanje kakovosti izdelkov in storitev, zaščito potrošnikov v kupoprodajnih odnosih in nadzor zaščite človekove bivalne in delovne sredine.

Industrijska metrologija je področje, ki omogoča, da se industrijski in drugi proizvodi izdelujejo v skladu z mednarodnimi standardi/SIST, IEC, VDE, ISO, CE,. . . /Kakovost izdelka predstavljajo lastnosti s katerimi se ustvarja kakovost dela in življenja. Ocenjevanje kakovosti se opredeljuje z meritvami karakteristik parametrov oziroma veličin.

Znanstvena metrologija je področje, ki povezuje razvojno in raziskovalno delo, ki vključuje merjenje največje točnosti in natančnosti v metroloških laboratorijih.

Nekater ključne besede za področje merilne tehnike so predvsem:točnost, preciznost, ločljivost, linearnost, občutljivost, prag delovanja, stabilnost, ponovljivost, histereza, vhodna in izhodna impedanca.

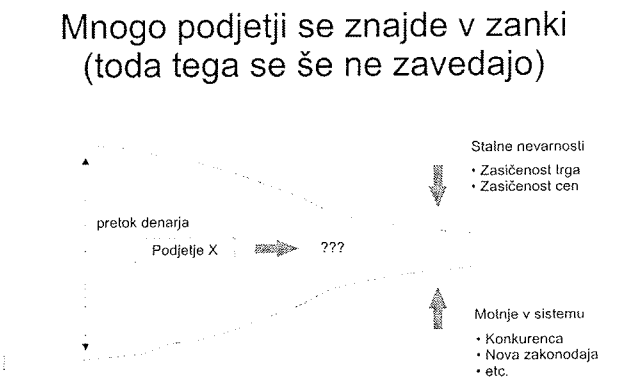
Podjetje v globalnem okolju

Položaj podjetja iz dejavnosti merilne tehnologije je vezano tako na nevarnosti kot tudi na priložnosti na tržišču. Med nevarnosti lahko štejemo zasičenost trga, vojna cen, konkurenca, nova zakonodaja, itd.

Ključno je, da podjetje vedno znova preverja in ugotavlja pretok denarja, dohodkovnost oziroma dodano vrednost. V globalnem prostoru tudi za panogo merilne tehnologije obstojijo izzivi in priložnosti a seveda tudi nevarnosti.

Tehnologija sama po sebi še ne določa uspeha managementa upravljanja inovacij. Za uspeh je potrebnih še več parametrov. Predvsem stalna inovacija v podjetju je zelo pomembna za uspešnost plasmana izdelkov. Svoje mesto v razvojnem procesu ima stalna, skokovita pa tudi radikalna inovacija. Kupci pravzaprav niso pretirano zainteresirani za tehniške lastnosti izdelka, več jim pomenjo prodajni argumenti v katere so preoblikovne tehniške lastnosti, ki prepričljivo kažejo na vrednost izdelka v vrednostni verigi kupca. Izdelki in storitve (instrumenti, testerji, umerjanje) v panogi merilne tehnologije so del poslovnih modelov, ki so zazanamovani predvsem z:

- naravnanim tržnim segmentom
- vrednoto za uporabnika vezano na aktualno zasnovo in tehnologijo



Slika 1: Nevarnosti in motnje, ki prežijo na podjetje

- usmeritvijo na ključno vrednoto ponudbe
- definiranjem verige vrednosti za oblikovanje ponudbe
- vzdržnim modelom dospetja plačil računov
- vzpostavitvijo prilagajanja vrednot za obstoj poslovnega modela

Portfolio inovacij v podjetju je slejkoprej vezano na presek dejavnikov med tržiščem oziroma uporabnikom in tehnologijo oziroma izdelkom

Slika 2: Proces inoviranja v industrijskem okolju

Narava dela in stalnih izboljšav zahteva v inovativnem podjetju vse vidike stalnega optimiranja programa:

- lijak idej novih poslov
- zametki novih poslov
- atraktivnost inovacij in izboljšav
- ustvarjanje projektov novih poslov
- ustanovitev novih podjetij
- ustanavljanje poslovnih enot

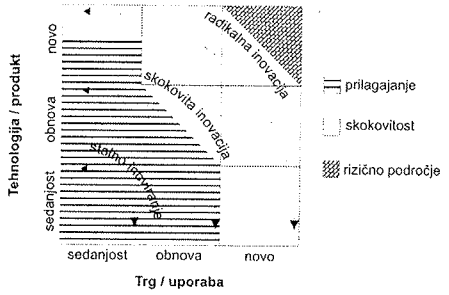
Sestavni del portfolia inoviranja so tudi naslednje situacije ter ukrepi:

- hitrost inovativnega procesa
- soočenje s tveganjem in stroški
- izločanje nezanesljivih trgov in tehnologij
- odločitev o vlaganju in številu projektov
- priprava poslovnega načrta

Poslovne priložnosti naj bi bile predmet stalne evaluacije predvsem z vidika merljive atraktivnosti za uporabnika na eni primerljivosti za podjetje na drugi strani. Opredelitev podjetja do inovacije je običajno ena od naslednjih odločitev:

- izločitev ideje
- podpora ideje
- odprodaja inovacije na določeni stopnji
- oblikovanje partnerstva na inovaciji ali ustanovitev podjetja
- formiranje nove dejavnosti v podjetju

Portfolio inovacij pri razvoju izdelkov in storitev



Slika 3: Stopnje inovativnosti v odnosu na razmerje med izdelkom in njegovo uporabnostjo

Ob klasičnem notranjem razvojno-raziskovalnem krogu se v podjetju uveljavlja tudi razvojno-raziskovalni krog, ki je obrnjen navzven. Pri navznoter naravnanem inovacijskem krogu obstoje nekakšne skrite predpostavke izvajalcev in sicer:

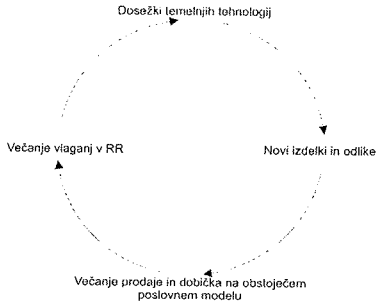
- v kolikor to odkrijem bom sam našel tržišče
- vkolikor to odkrijem prvi bo to moja last
- predvidevam, da je pomembna tehnologija, ki je potrebna tudi na voljo
- predvidevam da najboljši ljudje na tem področju delajo za nas

In kaj se je spremenilo z ozirom na povedano?

- vedno več je na voljo mobilnih strokovnjakov in delavcev z vrhunskimi sposobnostmi
- vedno več je kvalitetnih centrov znanja predvsem univerz
- manjši je tehnološki vpliv velesil
- prisotno je tržno prerazporejanje največjih dobaviteljev
- več je na voljo startnega in tveganega kapitala

Povedano pa narekuje potrebo , da podjetje podvzame ukrepe in reagira na zlom klasičnega inovacijskega kroga. Predvsem je to odnos do uvajanja odprte inovativnosti tudi z zapolnitvijo vrzeli z zunanjo tehnologijo oziroma znanjem. Le tako je možno ustvarjati vrednostno inovacijo, ustvarjati nove izdelke in storitve za nova tržišča in se vsaj nekoliko izogniti uničevalni tekmi s konkurenco za vsako ceno na enakih ali podobnih izdelkih.

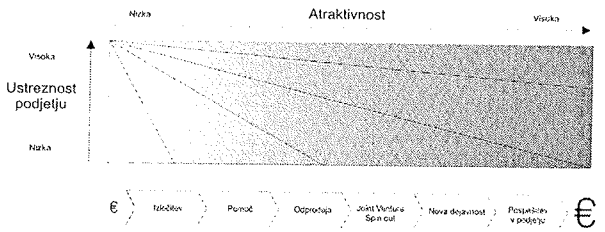
Klasičen RR krog



Slika 4: Razvojno raziskovalni krog v industrijskem podjetju

Logika odprte inovacije pomeni predvsem spoznanje, da so danes dobre ideje zelo razširjene in da ni monopola nad uporabo znanja. Posebej je treba gospodariti oziroma upravljati z industrijsko lastnino ter blagovno znamko. Za plemenitenje lastnega poslovnega modela potrebujemo tudi vzpostavitev odnosa z zunanjo industrijsko lastnino. Na drugi strani pa moramo iskati priložnosti, da se ustvarja dobiček tudi v drugih poslovnih modelih z našo industrijsko lastnino. Vedno pa moramo vedeti da ne delajo najpametnejši ljudje samo za nas.

Evaluacija poslovnih priložnosti



Slika 5: Shema upravljanja s poslovnimi priložnostmi

Vse to je potrebno zaradi iskanja novih neodkritih a obetavnih trgov in tehnologij za stopnjevanje poslovnega portfelja podjetja. Prav tako moramo ustvarjati verigo vrednosti s katero vsopamo v strateška poslovna zavezništva. Odprta inovativnost nam omogoča tudi ustvarjanje zunanjih in notranjih zametkov dejavnosti na različnih stopnjah razvoja in tehnologij. Tudi dejavnosti, ki (še) niso v jedru poslovne dejavnosti podjetja morajo ustvarjati prihodek od rezultatov dejavnosti.

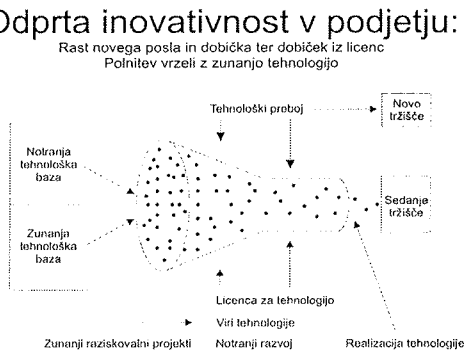
V Evropi naj bi nastala najbolj konkurenčna družba, temelječa na znanju na svetu. Veliko pobud in politik poskuša delovati v tej smeri a zaenkrat so makro kot tudi mikro gospodarski parametri pod težo bremen družbe, ki išče svojo priložnost.

Dejstvo je, da tehnologija sama po sebi še ne določa uspešnosti inovacij, dogaja se tudi da velik del dobičkonosnih inovacij ni vezan na znanje temelječe na znanosti. Vprašanje ali nizkozahtevne tehnološke inovacije temeljijo na znanju dobi odgovor na tisti strani, ko je znanje tudi podjetništvo, inovacija izdelka, iznajdljivost, prodornost in manj zanstveno pogojeno kreativnost. Za inovativnost v nizkozahtevnih tehnoloških panogah pa je značilen tisti del inovativnosti, ki se odraža s povezavo podjetij in izobraževalnega sistema (ne samo univerz). Take povezave pa bistveno spreminjajo odnos do uporabnega znanja.

Povezovanje podjetja s subjekti zunanjega okolja je zelo bistveno za doseganje poslovnih učinkov. Seveda mora podjetje imeti poslovno naravnanost, cilje, smotre, vizijo in strategijo. Da bi bili pripravljeni na kvalitetna partnerstva pa moramo posebno pozornost nameniti pripravi na sklepanje takih povezav. Te priprave pomenijo opredelitev naslednjih pojmov:

- strategija poslov podjetja
- strategija predvidene povezave
- stranke v povezavi
- način delovanja povezave
- pogoji za stalno napredovanje povezave
- identifikacija kompetenc v povezavi
- spremljanje razvoja in poslanstva razvoja povezave
- dopolnjevanje strategije povezave

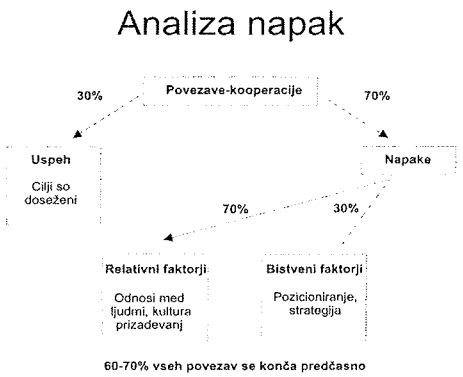
Da bi bile povezave čimbolj kakovostne je smiselna analiza na način kot kaže slika 6



Slika 6. Proces inoviranja v poindustrijskem okolju

Pri vzpostavljanju poslovnopartnerskih povezav je zelo pomembno: priprava, izbira poslovnega partnerja, vzajemni strateški cilj, pogajanja, vodenje sodelave pa tudi stalno preverjanje dosežkov poslovnega partnerstva.

V Evropi so še posebej aktualne povezave, ki so razvojno naravnane. Sem sodi lahko vstopanje podjetja v Tehnološke platforme, Tehnološke parke, 7. Evropski okvirni razvojni program, Eureko in tudi druge.



Slika 7: Nujnost povezovanja podjetij in analiziranje težav v povezovanju

Na svetovnem trgu uveljavljeno podjetje iz programa merilne tehnologije naj bi svoj, poslovni proces snovalo na najsodobnejših principih delovanja in med ključne besede sodijo naslednje aktivnosti:

- Inovacija kot stalnica
- Strateško načrtovanje
- Planiranje kooperacij
- Upoštevanje kupca
- Razvojno inovacijski sistem
- Proizvodni proces
- Celovito vzdrževanje
- Kakovost po»six sigma«
- Modeliranje proizvodnih celic
- Tehnike usposabljanja
- Poudarjanje vrednot
- Delo na standardih
- Vodenje redukcij
- Lansiranje izdelka
- Strategija nabavne verige
- Proces izboljšav
- Obvladovanje sprememb-KAIZEN
- Sprotno ugotavljanje uspešnosti
- Materialni tokovi
- Izvajanje poslovnega sistema podjetja

Poseben poudarek pripada naslednim dejavnostim:

*Procesu razvoja talentov v podjetju

*Organizaciji planiranja

*Usposabljanju za vrhunsko voditeljstvo

*Vzodbujanju šampionskega navdiha voditeljev

*Upravljanju z blagovno znamko

*Upravljanju industrijsko lastnino

Seveda pa moramo vedeti, da je hrbtenica poslovnosti v podjetju pogojena z:

LJUDMI, NAČRTOVANJEM, UČINKI, KUPCI, KAKOVOSTJO, STROŠKI IN INOVACIJO

Seveda moram posebej poudariti pomen najvišjih vodilnih v podjetju in s tem v zvezi pomen menedžmenta v podjetju. Ob tem velja v razmislek citirati Fredmunda Malika (menedžerski svetovalec in profesor na Univerzi v St. Gallenu).

»Neoliberalnemu polovičnemu znanju je treba pripisati, da je gospodarstvo v svojih temeljih ogroženo. Pravi liberalizem ne zahteva, da so vsi cilji podrejeni gospodarstvu. Tisto kar liberalizem res zahteva pa je, da je vsak odgovoren za svoje ravnanje. To mora veljati tudi za menedžerje. Številna načela liberalizma so bila preobrnjena v svoje nasprotje. . Zmotno je ljudem pridigati, da je tržno gospodarstvo čudovit sistem. Tržno gospodarstvo je slab sistem, tudi zato, ker ga ljudje iz dneva v dan kot takega doživljajo. Doživljajo ga kot brutalnega, neusmiljenega, nečloveškega in nepravičnega. Menedžerji bi morali tržno gospodarstvo sicer braniti, ne pa ga hvaliti. Tudi oni vedo da je tržno gospodarstvo slabo in neučinkovito. Vedo pa tudi, da so vsi drugi sistemi še veliko slabši in manj učinkoviti.

Naivno je reči, da bo vse uredil trg. Ta namreč ne prinaša nobenega gospodarskega učinka, ne prepreči nobene napake, temveč jih kaznuje potem, ko so se že zgodile. Da bi lahko popravili slabosti in škodo, ki jo prinaša trg, potrebujemo dobre menedžerje, ki poslanstva podjetij ne bi reducirali na intersese delničarjev in maksimiranje dobička. «

Podlaga za dinamične inovacije je prav gotovo znanje in sposobnost dojemanja temeljnih raziskav in še posebej aplikativnih raziskav po tehnološki in tržni strani. Inovacija je vedno časovno opredeljena, okvirom dodane vrednosti in tudi geografski namembnosti. Poudariti moramo še pomen oblikovanja (designa), patentov pa tudi standardov in tehnične regulative ter s komercialnega vidika ceno in predprodajno pa tudi poprodajno podporo uporabnikom.

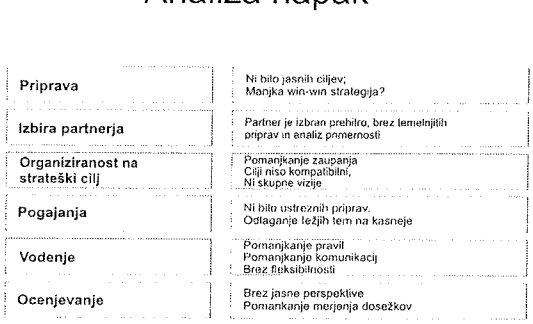
Izvedljivost razvojnega projekta v globaliziranem podjetju merilne tehnologije je vezana na izvedljivost tehnologije, ekonomike in pravne regulative. S pravnega vidika so pomembne tudi nacionalne zakonodaje, patenti pa tudi predpisi o eventuelnih nekomercialnih barierah. Študija izvedljivosti projekta je ključna za izvedbo glavne faze razvojnega projekta. Seveda je bistveno, da pridemo do izdelka z dobro tržno pozicijo, le tako se lahko nadejamo dobri prodaji. Parametrov, ki vplivajo na tržno pozicijo je seveda več, prav gotovo pa ne moremo mimo funkcionalne vrednosti izdelka ali storitve, cene, uveljavljenosti blagovne znamke pa tudi obsega ponudbe drugih proizvajalcev (konkurence).

V visoko tehnološki dejavnosti kar merilna tehnika zagotovo je, je pomembno tudi posredovanje aplikativnega znanja za izdelek do uporabnika. Organiziranje pred in poprodajne podpore je zelo bistveno za penetracijo izdelka na trgu. Posredovanje znanja na seminarjih in tudi preko elektronskega medija pa je stalna praksa za tekoči program in še posebej za nove izdelke.

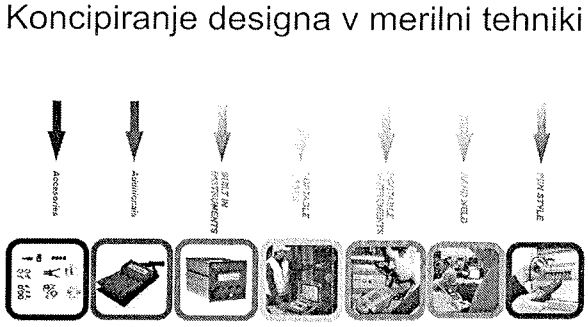
Merilna tehnika sodi v visokotehnološko tržno nišo in faktor časa v procesu inovacije še posebej pomembno vlogo. Posebej moramo poudariti estetske in ergonomske vidike pravočasnega oblikovanja izdelka. Poleg oblikovanja se tudi v industriji merilne tehnike realizira tehnični razvoj na določenih programskih vsebinah, ki jih opredeljuje poslovni načrt podjetja.

Pri tehničnem razvoju v panogi merilne tehnike so pomembna znanja predvsem eksaktnih ved fizike, mehanike, elektrotehnike in elektronike, kemije, programske opreme, aparaturne opreme in drugih. V samem tehničnem razvoju so RR (raziskovalno-razvojne) aktivnosti realizirane v simbiozi inženirjev v Tehničnem razvoju in tudi inženirjev v Marketingu. Faze razvoja so predvsem: priprava in izdelava tehničnega zahtevnika, eksperimentalni razvoj, funkcionalno modeliranje, izdelava prototipa, izvajanje preskušanja, razvojna serija in poskusna serija.

Področja uporabnosti končnih izdelkov v Merilni tehniki so največkrat opredeljene z naslednjimi ključnimi besedami: instrument, tester, analizator v povezavi z diagnostiko monitoringom, testiranjem, merjenjem, analiziranjem, preskušanjem, primerjanjem, presojanjem in drugimi možnostmi, ki jih merilna tehnika nudi.



Slika 8: Vzroki za težave v povezovanju



Slika 9: Izreden pomen snovanja »designa« za izdelke, pribor in dodatke

Brez meritev, kot so današnje, ne bi bil človek pametni - nikdar stopil na Luno, brez njih ne bi nikdar zvedel kako je na Marsu, Jupitru, Veneri, brez njih ne bi nikdar spoznal že grozljivo veličastnih dogajanj s snovjo Vesolja, vsega tega kar je, kar je kdaj bilo in kar kdaj še bo.

(prof. dr. F. Avčin,)

Uvodnik "Novicam na pot"društva za merilno procesno tehniko l1978

Slika 10:Uvodnik »Novicam na pot«

Smoter podjetja v merilno tehnični branži je snovati in realizirati izdelke oziroma storitve, ki ustrezajo zahtevam tržišča in temeljijo na interdisciplinarnih tehnoloških rešitvah za različne uporabnosti pri sodobnih tehničnih sistemih. Merilna tehnika je največkrat integrirana v moderne tehnološke rešitve in uvršča se v takoimenovano visoko tehnološko dejavnost.

Vsekakor pa moram pudariti tudi pomen makrookolja za podjetje in podjetništvo. V času globalnega delovanja, ko je bistvena vrhunska specialnost je računati na zanesljivo in podjetju prijazno okolje. V kolikor makrokolje ne pritegne k strategiji visokotehnoloških podjetij potem bodo podjetja postala del tradicionalne panoge z vsemi težavami nizke produktivnosti.

Kar se tiče makrookolja v Evropi je zanimiva navedba o hipotetičnem izračunu glede zaostajanja Evrope za ZDA, ki ga je podal dr Sicherl (3). Izračun pokaže, da bi države skupine EU-15 ujele ZDA pri kazalcu R&R na prebivalca v letu 2123, če bi bila njegova stopnja rasti v Evropi za 0, 5 odstotka višja kot v ZDA. Pri enoodstotni razliki pa bi to pomenilo leto 2063. Tako velike razlike se ne morejo zmanjševati z vztrajanjem pri zastarelih vzorcih prakse.

Osebno mislim, da je naše ožje makrokolje smiselno primerjati s podobnimi ekonomijami obsega, kot so na primer: Finska, Irska, Češka, Danska, Švedska, itd.

Tehnološki razvoj je pogoj za inovacijsko uspešnost gospodarstva. Vendar je to samo eden od pogojev. Pogoj je tudi boj za odličnost duha, ko prežema večino zaposlenih ambicioznost ustvarjalnosti, odpor do zastarelih miselnih vzorcev in rutine, volja do izboljšav in novosti, do odlike, izrednosti, edinstvenosti ter enkratnosti.

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Poročila s konferenc
Conference reports

Četrti evropski simpozij o mikroelektroniki in montaži elektronskih vezij EMPS-2006 (22. 5 do 24. 5. 2006) in satelitska delavnica "Feroelektrične tanke in debele plasti, priprava in njihova uporaba v mikroelektromehanskih sistemih (MEMS)" (21. 5. 2006), Terme Čatež

Od ponedeljka, 22. 5. 2006 do srede, 24. 5. 2006 je v Termah Čatež potekala 4. evropska konferenca o mikroelektroniki in montaži elektronskih vezij EMPS-2006. Dan prej, v nedeljo 21. 5., smo organizirali satelitsko Delavnico o pripravi feroelektričnih tankih in debelih plasti in njihovi uporabi v mikroelektromehanskih sistemih (MEMS).

EMPS je ena od dveh konferenc, ki ju organizira evropski IMAPS (International Microelectronics and Packaging Society). Obe konferenci sta dvoletni. Prva, ki poteka v lihih letih (npr. 2003, 2005) predvsem v državah nekdanje zahodne Evrope, je EMPC (European Microelecronic and Packaging Conference), druga, ki poteka v sodih letih (npr. 2004, 2006) v državah nekdanje vzhodne Evrope, pa EMPS (European Microelectronic and Packaging Symposium).

Delavnica o pripravi feroelektričnih tankih in debelih plasti in njihovi uporabi v mikroelektromehanskih sistemih (MEMS) (21. 5. 2006)

Satelitsko delavnico, posvečeno tankim in debelim feroelektričnim plastem ter njihovi uporabi, smo organizirali kot aktivnost centra odličnosti SICER, ki je projekt 5. okvirnega programa Evropske komisije in deluje v okviru Odseka za elektronsko keramiko Instituta Jožef Stefan. Delavnico sta delno finančno podprli tematska mreža POLECER (5. okvirni program) in mreža odličnosti MIND (6. evropski okvirni program). Delavnico je najprej pozdravila predsednica EMPS Marija Kosec (Institut Jožef Stefan, Ljubljana), nato pa začela predsednica delavnice Barbara Malič (Institut Jožef Stefan, Ljubljana).

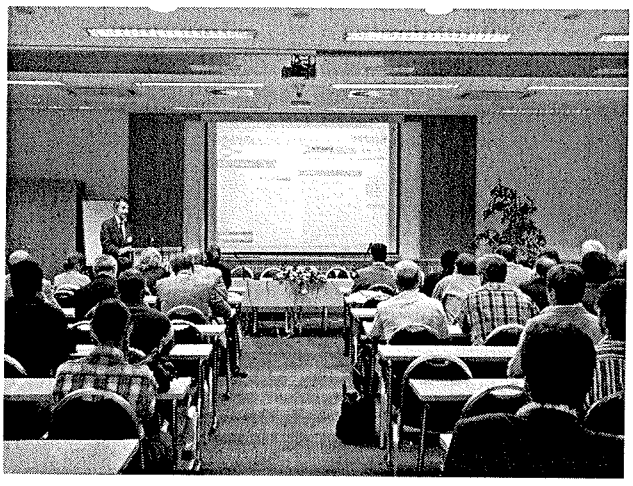
Delavnico je sestavljalo šest vabljenih predavanj. Paul Muralt (Ecole Polytechnique Federale de Lausanne - EPFL, Švica) je predaval o piezoelektričnih tankih plasteh na silicijevih podlagah in njihovi uporabi v MEMSih. Mark Stewart (National Physical Laboratory, Teddington, Velika Britanija) je predaval o različnih načinih meritev piezoelektričnih plasti in o problemih, povezanih s karakterizacijo plastnih struktur. Robert Dorey (Cranfield University, Velika Britanija) je govoril o integraciji tankih plasti na silicijevih podlagah v MEMSe,. Philippe Gaucher (Ecole Centrale Paris, Francija) je predstavil predvsem teoretični pristop k izračunavanju piezoelektričnih karakteristik plasti in monokristalov, Dou Zhang (University of Birmingham, Velika Britanija) je predaval o debelih plasteh na osnovi $(Ba,Sr)TiO_3$ z nizko temperatiro sintranja in o piezoelektrični keramiki v obliki, trakov, zvitih v spirale, ki dosežejo pomike do nekaj centimetrov. Jun Akedo (National Institute of Advanced Industrial Science and Technology, Tsukuba, Japonska) je predaval o nanašanju keramičnih plasti mikrometrskih debelin z novo metodo aerosolnega nanašanja, ki omogoča zgoščevanje že pri sobni temperaturi.

Simpozij EMPS-2006 (22. do 24. 5. 2006)

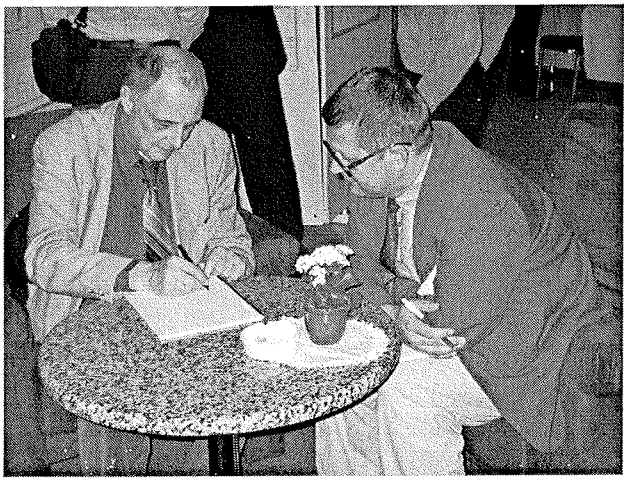
Simpozij EMPS-2006 sta organizirala MIDEM - Strokovno društvo za mikroelektroniko, elektronske sestavne dele in materiale, in Institut Jožef Stefan. Sponzorja simpozija sta bila Slovenska raziskovalna agencija in HYB d.o.o, Šentjernej, Slovenija. Sodelovalo je okrog 130 udeležencev iz 18 držav.

Simpozij so s pozdravi, kratkimi nagovori in informacijami začeli predsednik društva MIDEM Slavko Amon (Fakulteta za elektrotehniko, Univerza v Ljubljani), predsednik IMAPS-Europe Paul Collander (Poltronic, Finska), predsednik tehničnega programskega odbora Darko Belavič (HIPOT, d.o.o, Šentjernej) in predsednica konference M. Kosec (Institut Jožef Stefan, Ljubljana). Paul Collander je predlagal "starosto" organizacije IMAPS, Petra Barnwella, za častnega člana, kar je bilo seveda sprejeto z aplavzom.

Simpozij se je začel s plenarno sekcijo z vabljenimi predavatelji. Philippe Gaucher (Ecole Centrale Paris, Francija)



Simpozij



Strokovna diskusija

Organizatorji, WLC in Sponzor HYB

je v predavanju o funkcionalnih materialih v elektroniki predstavil tako teorijo kot možnosti uporabe tankih in debelih plasti na silicijevih rezinah. Franc Dolenc (Iskratel, d.d., Kranj) je opisal probleme in strategije njihovega podjetja na področju telekomunikacij v sedanji atmosferi globalizacije. Predsednik krovne organizacije IMAPS Jim Drehle iz Združenih držav Amerike je predstavil zgodovino organizacije od njenega začetka leta 1967. Takrat se je imenovala ISHM (International Society of Hybrid Microelectronics) in se je preimenovala v IMAPS leta 1997. Opisal je sedanje stanje in poudaril izzive, ki čakajo organizacijo v prihodnosti.

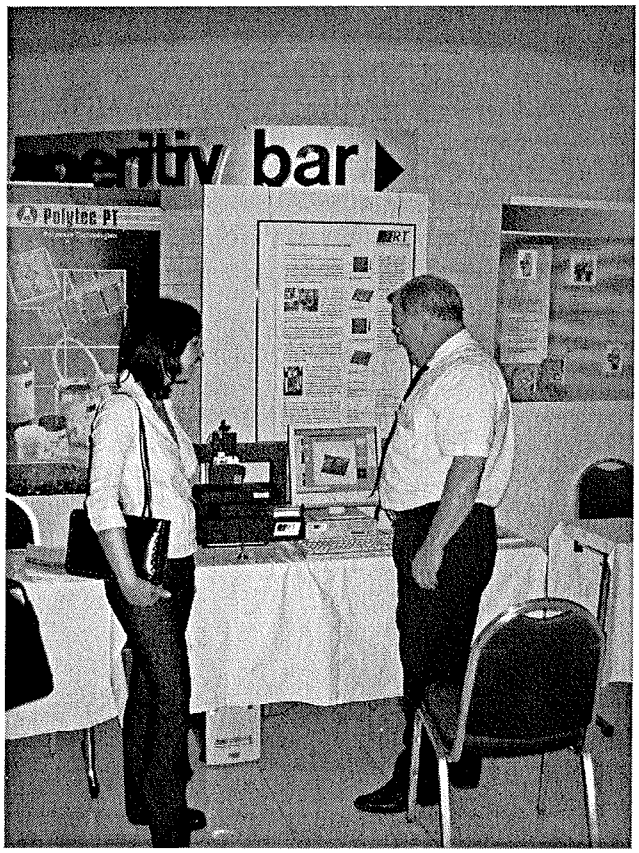
Na simpoziju je bilo predstavljenih okrog 70 prispevkov, od tega 50 referatov in 21 postrov. Referati so bili predstavljeni v 12 vzporednih sekcijah.

Naslovi sekcij so bili:

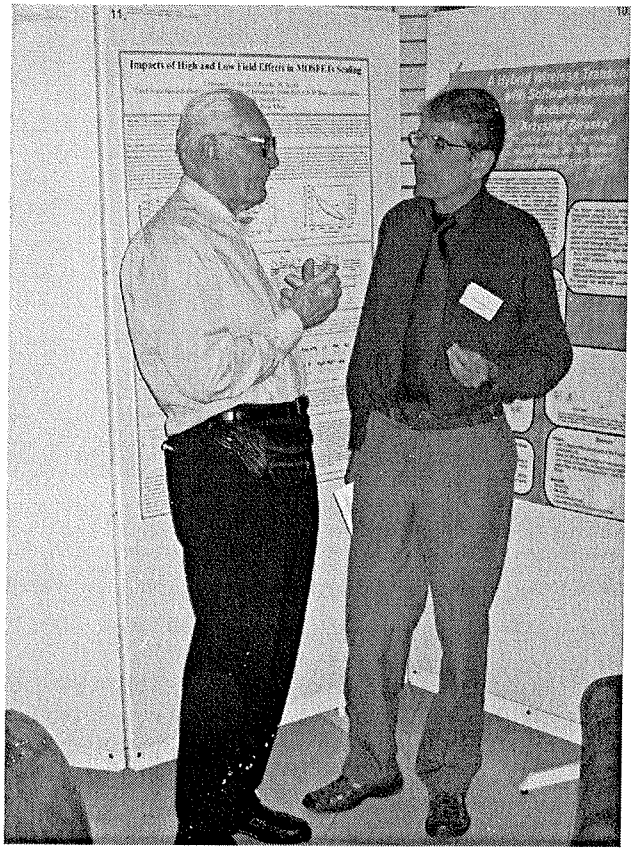
Sekcija 1:	Materiali in procesi
Sekcija 2.	Polprevodne strukture in vezja
Sekcija 3:	Napredek na področju keramike z nizko temperaturo žganja LTCC
Sekcija 4:	Mikroelektronske aplikacije
Sekcija 5:	Debele in tanke plasti
Sekcija 6:	„Vgrajene" aktivne komponente
Sekcija 7:	Tehnologije povezav
Sekcija 8:	Montaža
Sekcija 9:	Temperaturno načrtovanje in kvaliteta
Sekcija 10 in sekcija 12:	Materiali brez svinca in okolje
Sekcija 11:	Načrtovanje in simulacija

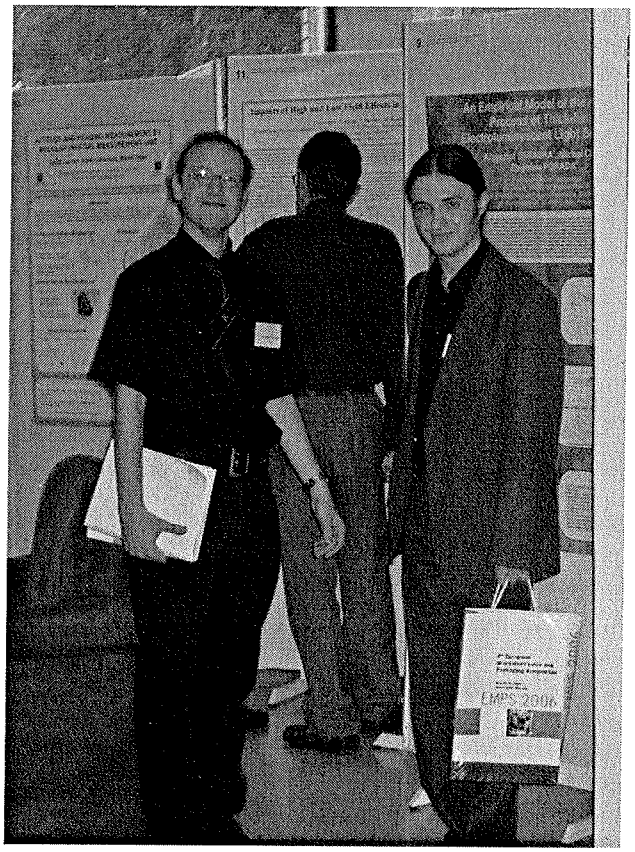
V posebni sekciji so, pod vodstvom Barbare Malič in Paula Collandra, predstavili sodelovanje v okviru evropskih mrež. Wanda Wolny (Ferroperm, KvistgardDanska) je predstavila tematsko mrežo o polarni elektronski keramiki POLECER. . Mreža ima 81 članov iz univerz, raziskovalnih organizacij in industrije, in 19 pridruženih članov. Mreža je začela delovati 1. aprila 2001 in se bo končala 31. marca 2007.

Potem bodo aktivnosti prenešene v mrežo odličnosti MIND o multifunkcijskih in piezoelektričnih integriranih elementih, ki jo je predstavil Marc Lethiecq (Universite Tours, Francija). Mreža ima 11 parnerjev, od tega 5 univerzitetnih laboratorijev, 3 raziskovalne organizacije in 3 industrijske laboratorije. Namen mreže je integracija evropskih raziskav na področju piezoelektričnih materialov in njihove uporabe. Matej Možek (Fakulteta za elektrotehniko, univerza v Ljubljani) je predstavil mrežo MINOS-EURONET (Micro-Nano Systems European Network). Mreža je pravzaprav grozd osmih projektov v 6. okvirnem programu in jo sestavlja 159



Razstava





Srečanje starih znancev in sklepanje novih poznanstev.

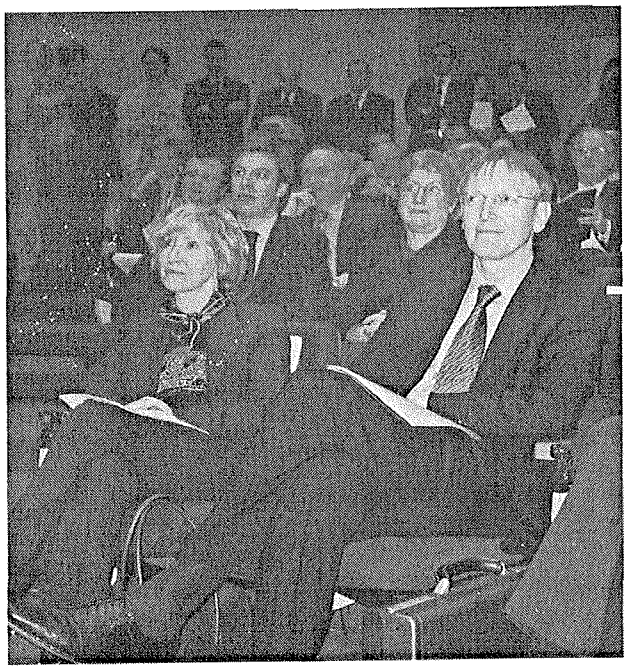
organizacij. Slovenski člani so Univerza v Ljubljani, Institut Jožef Stefan, Politehnika Nova Gorica in Zavod TC SEMTO. Poudarek mreže je na enem od strateških ciljev IST (Information Society Technologies), to je na mikro in nano sistemih. Miran Čeh (Institut Jožef Stefan, Ljubljana) je predstavil razširjeno mrežo ESTEEM (Enabling Science and Technology for European Electron Microscopy). Mreža je del integrirane infrastrukturne iniciative v 6 okvirnem programu Evroske komisije na področju elektronske mikroskopije. Projekt, v katerem sodeluje 11 partnerjev, bo potekal v obdobju od 2006 do 2011.

V torek popoldne je bil v okviru družabnega programa, ki ga je finančno omogočilo podjetje HYB, organiziran ogled galerije cisterijanskega samostana v Kostanjevici. Udeleženci so si ogledali razstave treh slovenskih umetnikov - slikarjev in kiparjev. V cerkvi v samostanu je bil koncert Adoramus okteta in Clarifour klarinetskega kvinteta. Prvi je predstavil v glavnem ljudske motive, drugi pa predvsem klasične skladbe. Zvečer je bila skupna večerja za vse udeležence v prijetnem gostišču Žolnir.

EMPS simpozij se je končal v sredo zgodaj popoldne. Ob zaključku sta Darko Belavič in Marija Kosec na kratko povzela dogajanje na simpoziju. Paul Collander je udeležence povabil na naslednjo EMPC konferenco, ki bo leta 2007 v Oulu-ju, Finska. Po zaključku simpozija je bil organiziran ogled sponzorja, proizvajalca hibridnih debeloplastnih vezij in senzorjev, HYB Šentjernej.

NOVICE
NEWS

European Commissioner Janez Potočnik visits IMEC



Flemish Minister Fientje Moerman and European Commissioner Jonez Potočnik,

On January 26, 2006, European Commissioner for Science and Research, Janez Potočnik, and Flemish Minister for Science and Innovation Fientje Moerman visited IMEC. The European Commissioner highlighted the importance of both regional developments and cross-border initiatives in the creation of the European knowledge economy.

In his speech, European Commissioner Potočnik pointed out the importance of knowledge regions such as Flanders, and Leuven in particular, in the creation of the European knowledge economy. The presence of several leading universities gives Flanders an excellent position to seize the many opportunities within the European Framework Programs. But not only regional development is important. Potočnik also stressed the necessity of cross-border initiatives, such as the European research platform for nanoelectronics, ENIAC, in which IMEC plays a vital role. According to Potočnik, one of Europe's contributions would have to be to create an attractive environment in which the mobility of researchers is encouraged and facilitated.

Flemish Minister Moerman underlined some recent initiatives that were realized in Flanders in order to boost the knowledge-based economy. In 2006, she will submit an international cooperation action plan to the Flemish government, in which the importance of international collaboration is emphasized.

The European Commissioner also visited the K.U.Leuven, where he was informed about the university's policy and had the chance to talk with young researchers.

Semi reports 2005 global semiconductor sales of $32,88 billion

SEMI, reported that worldwide sales of semiconductor manufacturing equipment totalled $32.88 billion in 2005, representing a year-over-year decrease of 11 percent, data from the Worldwide Semiconductor Equipment Market Statistics (SEMS) Report.

Compiled from data submitted by members of SEMI and the Semiconductor Equipment Association of Japan (SEAJ), the Worldwide SEMS Report is a summary of the monthly billings and bookings figures for the globalsemiconductor equipment industry. The report, which includes data for seven major semiconductor producing regions and 22 product categories, shows worldwide billings totalled $32.88 billion in 2005, compared to $37.08 billion in sales posted in 2004.

"This past year marked an anticipated decline in the global semiconductor equipment industry following a large expansion in 2004," said Stanley T. Myers, president and CEO of SEMI. "However, 2005 still posted the third all-time strongest year for the semiconductor equipment industry."

The South Korean market region grew the most in 2005, rising 26% to US$5.8 billion, surpassing Taiwan to become the second largest equipment market behind Japan. Japan, contracted 1 % to about US$8.2 billion. The Rest of World region, 'which aggregates Singapore, Malaysia, Philippines, other areas of Southeast Asia and smaller global markets, declined 36% with the market in China experiencing a 50% decrease. Taiwan, which led world growth in 2004 with a 166% expansion in equipment spending declined 23% in 2005. Equipment markets in Europe and North America decreased 5 % and 20% in 2005.

Region	2004	2005	% Change
China	2,683	1,327	-50.5
Europe	3,444	3,262	-5.3
Japan	8,276	8,183	-1.1
Korea	4,614	5,826	26.3
North America	5,812	5,702	-1.9
Taiwan	7,762	5,722	-26.3
Rest of World	4,490	2,862	-36.3
Total Regions $	37,081	32,884	-11.3

2004-2005 Semiconductor Capital Equipment Market by World Region
(Dollars in U.S. Millions; Percentage Year-over-Year)

Informacije MIDEM
Strokovna revija za mikroelektroniko, elektronske sestavine dele in materiale

NAVODILA AVTORJEM

Informacije MIDEM je znanstveno-strokovno-društvena publikacija Strokovnega društva za mikroelektroniko, elektronske sestavne dele in materiale - MIDEM. Revija objavlja prispevke s področja mikroelektronike, elektronskih sestavnih delov in materialov. Ob oddaji člankov morajo avtorji predlagati uredništvu razvrstitev dela v skladu s tipologijo za vodenje bibliografij v okviru sistema COBISS.
Znanstveni in strokovni prispevki bodo recenzirani.

Znanstveno-strokovni prispevki morajo biti pripravljeni na naslednji način:

1. Naslov dela, imena in priimki avtorjev brez titul, imena institucij in firm
2. Ključne besede in povzetek (največ 250 besed).
3. Naslov dela v angleščini.
4. Ključne besede v angleščini (Key words) in podaljšani povzetek (Extended Abstract) v angleščini, če je članek napisan v slovenščini
5. Uvod, glavni del, zaključek, zahvale, dodatki in literatura v skladu z IMRAD shemo (Introduction, Methods, Results And Discsussion).
6. Polna imena in priimki avtorjev s titulami, naslovi institucij in firm, v katerih so zaposleni ter tel./Fax/Email podatki.
7. Prispevki naj bodo oblikovani enostransko na A4 straneh v enem stolpcu z dvojnim razmikom, velikost črk namanj 12pt. Priporočena dolžina članka je 12-15 strani brez slik.

Ostali prispevki, kot so poljudni cčlanki, aplikacijski članki, novice iz stroke, vesti iz delovnih organizacij, inštitutov in fakultet, obvestila o akcijah društva MIDEM in njegovih članov ter drugi prispevki so dobrodošli.

Ostala splošna navodila

1. V članku je potrebno uporabljati SI sistem enot oz. v oklepaju navesti alternativne enote.
2. Risbe je potrebno izdelati ali iztiskati na belem papirju. Širina risb naj bo do 7.5 oz.15 cm. Vsaka risba, tabela ali fotografija naj ima številko in podnapis, ki označuje njeno vsebino. Risb, tabel in fotografij ni potrebno lepiti med tekst, ampak jih je potrebno ločeno priložiti članku. V tekstu je treba označiti mesto, kjer jih je potrebno vstaviti.
3. Delo je lahko napisano in bo objavljeno v slovenščini ali v angleščini.
4. Uredniški odbor ne bo sprejel strokovnih prispevkov, ki ne bodo poslani v dveh izvodih skupaj z elektronsko verzijo prispevka na disketi ali zgoščenki v formatih ASCII ali Word for Windows. Grafične datoteke naj bodo priložene ločeno in so lahko v formatu TIFF, EPS, JPEG, VMF ali GIF.
5. Avtorji so v celoti odgovorni za vsebino objavljenega sestavka.

Rokopisov ne vračamo. Rokopise pošljite na spodnji naslov.

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Informacije MIDEM
Journal of Microelectronics, Electronic Components and Materials

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Authors should suggest to the Editorial board the classification of their contribution such as : original scientific paper, review scientific paper, professional paper...
Scientific and professional papers are subject to review.

Each scientific contribution should include the following:

1. Title of the paper, authors' names, name of the institution/company.
2. Key Words (5-10 words) and Abstract (200-250 words), stating how the work advances state of the art in the field.
3. Introduction, main text, conclusion, acknowledgements, appendix and references following the IMRAD scheme (Introduction, Methods, Results And Discsussion).
4. Full authors' names, titles and complete company/institution address, including Tel./Fax/Email.
5. Manuscripts should be typed double-spaced on one side of A4 page format in font size 12pt. Recommended length of manuscript (figures not included) is 12-15 pages
6. Slovene authors writing in English language must submit title, key words and abstract also in Slovene language.
7. Authors writing in Slovene language must submit title, key words and extended abstract (500-700 words) also in English language.

Other types of contributions such as popular papers, application papers, scientific news, news from companies, institutes and universities, reports on actions of MIDEM Society and its members as well as other relevant contributions, of appropriate length , are also welcome.

General informations

1. Authors should use SI units and provide alternative units in parentheses wherever necessary.
2. Illustrations should be in black on white paper. Their width should be up to 7.5 or 15 cm. Each illustration, table or photograph should be numbered and with legend added. Illustrations, tables and photographs must not be included in the text but added separately. However, their position in the text should be clearly marked.
3. Contributions may be written and will be published in Slovene or English language.
4. Authors must send two hard copies of the complete contributon, together with all files on diskette or CD, in ASCII or Word for Windows format. Graphic files must be added separately and may be in TIFF, EPS, JPEG, VMF or GIF format.
5. Authors are fully responsible for the content of the paper.

Contributions are to be sent to the address below.

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