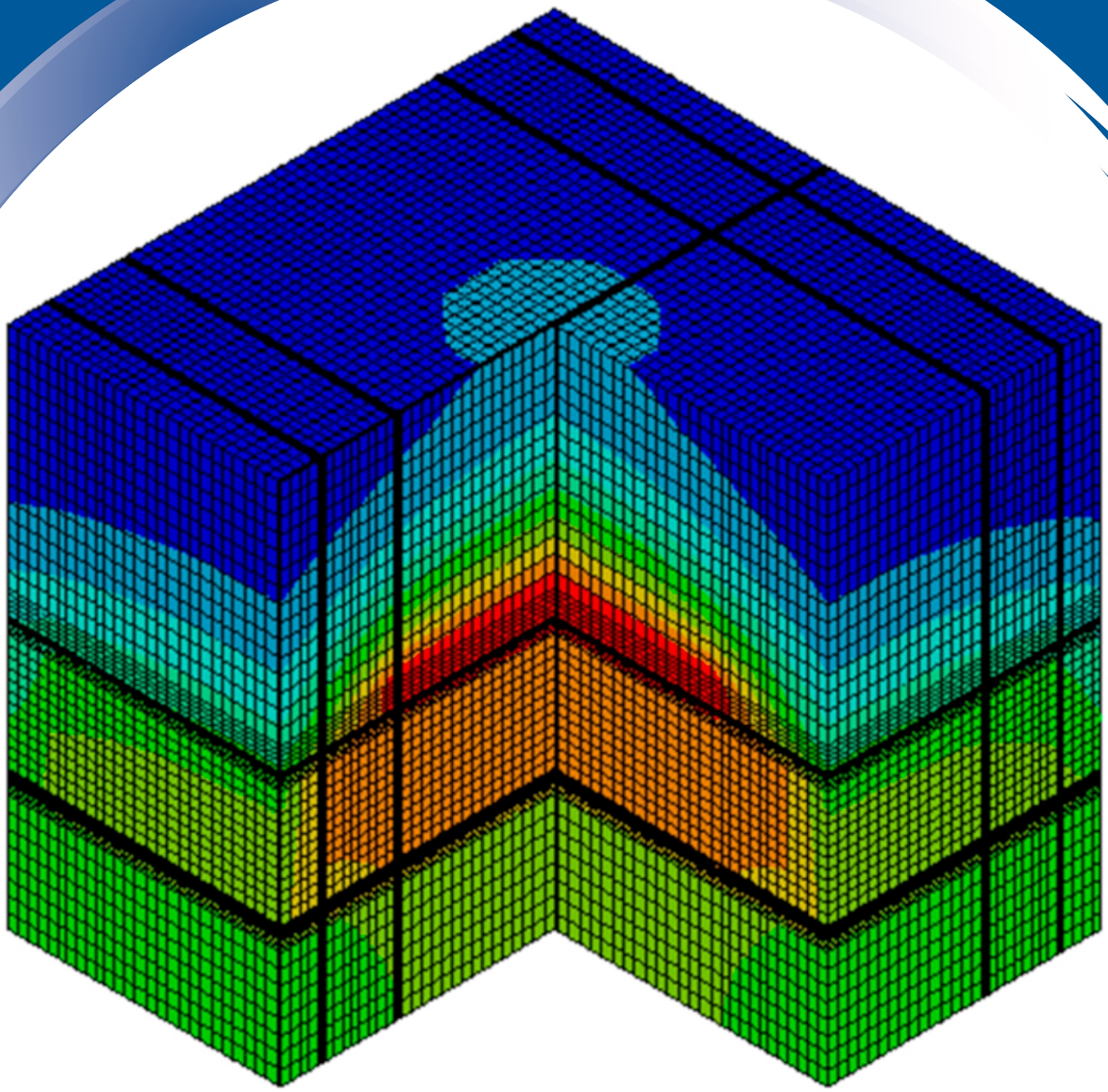
ISSN 0352-9045

Informacije MIDEM

Journal of Microelectronics, Electronic Components and Materials
Vol. 49, No. 2(2019), June 2019

Revija za mikroelektroniko, elektronske sestavne dele in materiale
letnik 49, številka 2(2019), Junij 2019



UDK 621.3:(53+54+621+66)(05)(497.1)=00 ISSN 0352-9045

Informacije MIDEM *2-2019*

Journal of Microelectronics, Electronic Components and Materials

VOLUME 49, NO. 2(170), LJUBLJANA, JUNE 2019 | LETNIK 49, NO. 2(170), LJUBLJANA, JUNIJ 2019

Published quarterly (March, June, September, December) by Society for Microelectronics, Electronic Components and Materials - MIDEM.

Headquarters | Naslov uredništva
Uredništvo Informacije MIDEM
MIDEM pri MIKROIKS
Stegne 11, 1521 Ljubljana, Slovenia
T. +386 (0)1 513 37 68
F. + 386 (0)1 513 37 71
E. info@midem-drustvo.si
www.midem-drustvo.si

Annual subscription rate is 160 EUR, separate issue is 40 EUR. MIDEM members and Society sponsors receive current issues for free. Scientific Council for Technical Sciences of Slovenian Research Agency has recognized Informacije MIDEM as scientific Journal for microelectronics, electronic components and materials. Publishing of the Journal is cofinanced by Slovenian Research Agency and by Society sponsors. Scientific and professional papers published in the journal are indexed and abstracted in COBISS and INSPEC databases. The Journal is indexed by ISI® for Sci Search®, Research Alert® and Material Science Citation Index™. |
Letna naročnina je 160 EUR, cena posamezne številke pa 40 EUR. Člani in sponzorji MIDEM prejemajo posamezne številke brezplačno. Znanstveni svet za tehnične vede je podal pozitivno mnenje o reviji kot znanstveno-strokovni reviji za mikroelektroniko, elektronske sestavne dele in materiale. Izdajo revije sofinancirajo ARRS in sponzorji društva. Znanstveno-strokovne prispevke objavljene v Informacijah MIDEM zajemamo v podatkovne baze COBISS in INSPEC. Prispevke iz revije zajema ISI® v naslednje svoje produkte: Sci Search®, Research Alert® in Materials Science Citation Index™.

Design | Oblikovanje: Snežana Madić Lešnik; Printed by | tisk: Biro M, Ljubljana; Circulation | Naklada: 1000 issues | izvodov; Slovenia Taxe Percue | Poštnina plačana pri pošti 1102 Ljubljana

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
vol. 49, No. 2(2019)

Content | Vsebina

Original scientific papers | Izvirni znanstveni članki

Original scientific paper
https://doi.org/10.33180/InfMIDEM2019.201

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 49, No. 2(2019), 53 – 60

Nano CMOS Charge Pump for Readerless RFID PLL

Md Torikul Islam Badal[1], Mamun Bin Ibne Reaz[2], Mohammad Arif Sobhan Bhuiyan[3], Chitra A. Dhawale[4]

[1]RMIT University, Department of Electronic and Telecommunication Engineering, Melbourne, Victoria, Australia
[2]University Kebangsaan Malaysia, Department of Electrical, Electronic and System Engineering, Bangi, Selangor, Malaysia
[3]Xiamen University Malaysia, Department of Electrical and Electronics Engineering, Sepang, Selangor, Malaysia
[4]P.R.Pote College of Engineering and Management, Department of MCA, Amravati, Maharashtra, India

Abstract: Readerless RFID has become more significant for reliable wireless communication. The Phase Locked Loop (PLL) is among the most crucial functional block in the Readerless RFID where the PLL performance greatly depends on the Charge Pump (CP). Conventional CP circuits suffer from current mismatching characteristics which generate phase offset and spurs in the PLL output signals. To overcome these problems, the CP current mismatch has to be minimized. An enhanced CP circuit with zero current mismatch is presented in this article adopting an ideal current mirror technique and an additional inverter to provide a rail-to-rail voltage. The post-layout simulation shows that the proposed CP maintains the steady current over a wide range of output voltage from 0.1-1.8 V consuming the substantially lower power of 0.178 µW. The CP circuit is designed in 130 nm CMOS process that operates at 1.8 V, and the core occupies 17 x 59.5 µm2. The proposed CP will be a good solution for low voltage, high-frequency PLL structure which suffers from poor performance.

Keywords: Charge pump; CMOS; Current mismatch; PLL; RFID

Nano CMOS črpalka energije za RFID PLL brez čitalca

Izvleček: RFID brez čitalca so postali pomembni za zanesljivo brezžično komunikacijo. Eden izmed kritičnih funkcijskih blokov RFID brez čitalca je, od črpalke energije (CP) odvisna, fazno sklenjena zanka (PLL). Konvencionalni CP trpijo z neuravnoteženo tokovno karakteristiko, ki vpliva na izhodni signal PLL. V izogib tem problemom je potrebno minimizirati CP. Članek opisuje izboljšan CP z ničelno tokovno neuravnoteženostjo z uporabo tehnike idealnega zrcaljenja toka in dodatnega inverterja za zagotavljanje napajanja. Simulacije nakazujejo da CP vzdržuje konstantni tok čez široko območje napajalne napetosti od 0.1-1.8 V in porabijo izredno malo moč 0.178 µW. Vezje je zasnovano v 130 nm CMOS tehnologiji pri napajalni napetosti 1.8 V. Velikost jedra je 17.0 x 59.5 µm2. Predlagana rešitev je dobra za uporabo v nizkonapetostnihvisokofrekvenčnih PLL strukturah z nizkim učinkom.

Ključne besede: črpaka energije; CMOS; tokovno neujemanje; PLL; RFID

** Corresponding Author's e-mail: torikul.uniten@gmail.com;*

1 Introduction

At present, Readerless RFID systems are experiencing rapid growth because of the advancement of the wireless communication system. RFID is an identification system, where data is transferred/received via radio frequency among antenna, reader, and transponder. In an RFID system, electronic product code which is also known as the identification code is attached to

an object for tracking. A frequency synthesizer (FS) is a feedback system that produces one or more frequencies from a single or several frequency sources. Charge pump based PLL (CPPLL) is broadly used in a wireless communication systems for frequency synthesis; especially in radio, telecommunications and other electronic applications due to its simple feedback system [1, 2]. CPPLL is preferred because of low bias current [3, 4], low static phase offset [5-7] and large system gain [8, 9]. Furthermore, it performs the key role to ensure the stability of frequency synthesis [10, 11]. The PLL is generally composed of a phase frequency detector (PFD), a charge pump (CP), a loop filter (LF), a voltage-controlled oscillator (VCO) and a frequency divider as depicted in Figure 1. Among all the functional blocks, CP is the most crucial block which significantly contributes to boosting the PLL's overall performance and stability. It changes the digital signal originating from PFD into an analog signal which in turn controls the VCO frequency [12]. The output voltage of the charge pump must be fixed when the PLL goes into a locked state at a specific frequency. Any change of that voltage results in frequency offset. [5, 13, 14]. In this regard, it is imperative to design a charge pump circuit that can generate a steady output current and can produce a superbly matched current with zero error in CPPLL.

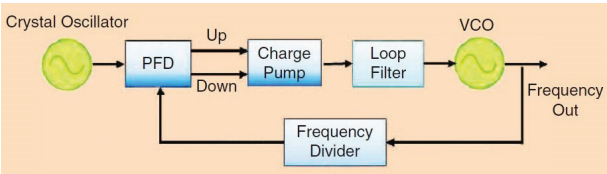


Figure 1: A Basic Block Diagram of CPPLL [4]

Charge pump (CP) is the subsequent stage to the PFD, i.e., the output (UP and DWN) signals of the PFD are fed to the CP circuit. The key principle of a charge pump is to translate the logic states of the PFD into suitable analog signals to control the voltage-controlled oscillator (VCO) through a loop filter. Fundamentally, the charge pump is made up of current sources and switches as shown in Figure 2. The output currents from the CP is usually filtered by a low pass filter (LPF) that converts the charge pump current to an equivalent control voltage for the VCO.

The conventional CP circuit consists of a charge and a discharge digital output current source, ICH and IDIS respectively described in Figure 2. A couple of transistor-based switches control both ICH and IDIS of the PFD. The two switches drive the loop filters and convert the output signals of the PFD to an analog voltage signal, Vcntrl, to tune the frequency of the VCO. The basic CP circuit suffers from many disadvantages, and as a consequence, several charge pump architectures have

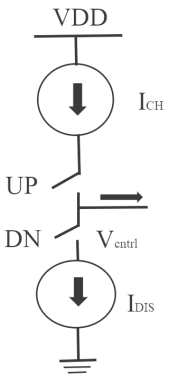


Figure 2: The basic concept of a charge pump circuit.

been reported with their pros and cons in the literature [14].

The imperfection of a CP can be estimated by the current mismatch, timing mismatch, power consumption, and charge sharing. But the current mismatch is the most vital parameter which leads the PLL performance. The current mismatch implies the magnitude dissimilarity between charging and discharging current which is a crucial concern for the CP design [8, 15]. Figure 3 represents the charging and discharging time diagram of a charge pump circuit.

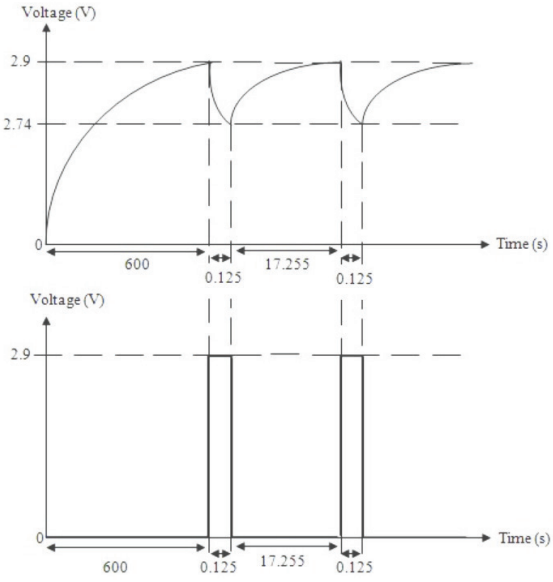


Figure 3: Charging and discharging time diagram of a charge pump circuit

The issues of current mismatch and leakage current introduce the phase error problem and produce PLL's reference spur [16, 17]. The current mismatch and leakage can be characterized as:

$$\Delta\emptyset = 2\pi \left(\Delta\emptyset_{timing} + \Delta\emptyset_{mismatch} + \Delta\emptyset_{leakage}\right) \quad (1)$$

Where, ΔØ, ΔØtiming, ΔØmismatch, and ΔØleakage, are the phase error, timing mismatch, current mismatch and leakage current of the CP circuit, respectively. Equation 1 shows that the current mismatch is directly associated with phase error and PLL's reference spur which is otherwise called dynamic jitter [7]. The measure of the reference spurs Pr can be defined by [18]

$$Pr = 20\log\left(\frac{\Delta Øf_{\mathrm{BW}}}{\sqrt{2f_{REF}}}\right) - 20\log\left(\frac{f_{REF}}{f_{PL}}\right)[dBc] \qquad (2)$$

and the loop bandwidth, f_{BW} is given by

$$f_{BW} = I_{CP}K_{VCO}R/(2\pi N) \qquad (3)$$

Where, Pr is the PLL reference spur, f_{REF} refer the reference frequency of the phase frequency detector (PFD), f_{BW} stands for the loop bandwidth, ΔØ is the phase error, and f_{PL} is the Loop filter's pole frequency. I_{CP} stands for the CP current flow, K_{VCO} refers to the VCO gain, R is the loop filter's resistor value where N is the divider value. Equation (2) describes that Pr is proportional to the loop bandwidth (f_{BW}) and phase error (ΔØ). Which means, the reference spurs can be reduced by increasing the reference frequency (f_{REF}) and minimizing the phase error (ΔØ) and loop bandwidth (f_{BW}). Therefore, a CP design is required, which can reduce the current mismatch and maintain the constant current over a wide range of output voltage. By decreasing the current variation and mismatch, the performance of CP can be significantly improved. This reduces the PLL's spurs and static phase offset. Therefore, a CP that can reduce the current mismatch and maintains the currents constant across a wide range of output voltage is the key block for creating an optimum CPPLL system.

Based on the literature review the current mismatch issue in CP design can be overcome in many ways [20-23]. Low-voltage cascade topology [19, 20] is a conventional approach for minimizing the current mismatch at the cost of high output resistance. With this conventional approach, the current mismatching features in these CPs [19, 20] are scaled down to 2%. Besides, current mismatching is reduced to <1% in [6, 8] by integrating operational amplifiers (Op-amp) technique. This method integrates a negative feedback amplifier along with op-amp where Op-amp controls the voltage node maintaining high amplifier gain and provides the advantage of the large input voltage of charge and discharge currents [21]. The current mismatch in [7] is reduced by executing a differential CP with an active loop filter (LF) and common-mode feedback scheme. This scheme integrated an op-amp, an analog adder, and a reference voltage circuit. Huh et al [22] proposed a replica CP where the current mismatch is compensated down to 1% by utilizing a bias generator. But, it requires a complicated circuit and creates a longer locking time. An unexpected current mismatch occurs in this architecture because of the fabrication mismatch between two CPs.

The variables that are responsible for current mismatch are current sharing, charge injection and clock feed. Controlling the switching circuit by the transistor causes charge injection. Charge injection arises when the transistor is utilized to govern the switching circuit and produce limited capacitance to the current sources [20, 23]. Keeping in mind the end goal to diminish current mismatch and current variation, the power consumption and the output voltage dynamic range must also be considered. Besides, the approach with double stage op-amps in three rail-to-rail amplifiers is competent and established for reducing the current mismatch. It adjusts the current mirror gate bias that results in matching the output of the switch current with the drain current. Thus, it reduces the static phase offset significantly and minimizes the current mismatch. This article proposes an improved CP design in 130 nm CMOS process based on the current mirror method employing an inverter at the gates of transistors for providing a rail-to-rail voltage swing to accomplish adequate current matching.

2 Proposed Charge Pump Circuit

A modified CP is designed based on current mirror technique integrating an inverter at the gates of the transistor to provide a rail-to-rail voltage swing that reduces the current mismatch and the voltage mismatch problem. The recommended CP circuit with current mirrors technique is presented in figure 4. The two current sources I1 and I2 are implemented as current mirrors. I1 and Up utilize PMOS transistors while I2 and Down use NMOS transistors. To increase the output resistance, the lengths of all transistors have been set to twice the minimal size at 700 nm [8]. To decrease the required amount of VGS the transistors with large widths were chosen so that the circuit could perform near the rail. An inverter is added at the PMOS transistor because its input must be inverted. Two inverters were set at the Dn gate to match the capacitances at the gates. Transistors M5 and M9 are connected to the node "aout" through the mirror transistors M6 and M8. This helps to decrease the impact of charge sharing. Moreover, the current mirror approach ensures that the charge and discharge currents retain a precise value for large voltage and guarantee that the Up and the Dn inputs are matched well. To assure both currents are equivalent, the current mirror is utilized for replicating current Up and current Dn from a single current source.

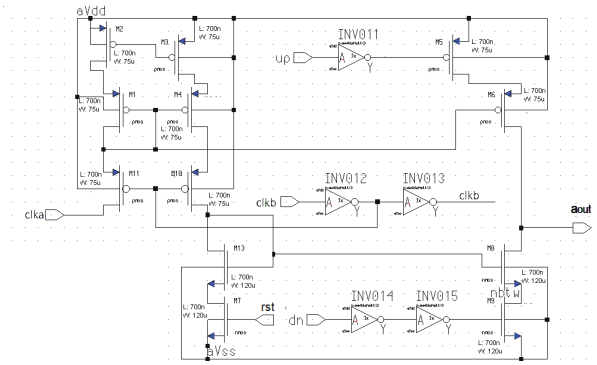


Figure 4: The proposed CP circuit based on current mirrors technique with inverters

3 Results and Discussions

The post-layout results of the designed CP circuit are depicted in figure 5-9. From the post-layout simulation, it is shown that the proposed CP can reach maximum output voltage of 1.8 V. Generally, schematic simulation is viewed as an ideal case, while the post-layout simulation is considered the actual case, which incorporates reverse charge sharing or body impact and parasitic capacitance. The post-layout simulation output voltage result is identical in comparison with the schematic simulation. The output results of the designed CP are verified using ELDONET simulators in TSMC 130 nm CMOS process. Usually, the voltage amplitudes of "clka" and "clkb" are equal to the power supply (VDD). The simulation parameters are used at 10 MHz pumping clock frequency along with 0.1 pF pumping capacitor and the input voltage connected to a 1.8V power supply. It is found that the designed CP circuit is successfully pumped up and down for the output voltage range from 0.1V to 1.8V. Figure 5 shows that when the reset transistor is disconnected, "clkb" is set to be delayed by 1.5 ns. As a result, the output waveform is observed to be charged up to Vdd, and the Up signal is wider than the Dn signal.

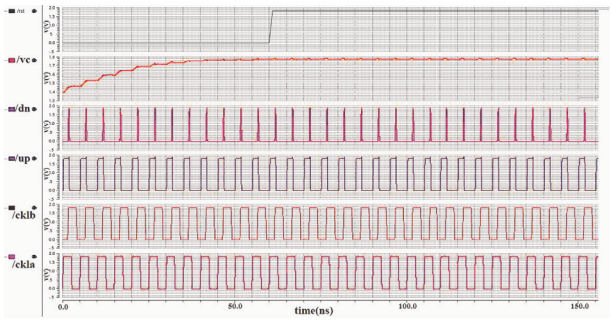


Figure 5: Post layout Result of Proposed CP Circuit: Pumping-Up @ (Vdd = 1.8 V, f = 10MHz)

Figure 6 clearly shows the voltage trend at the Vc node moving down, and the Dn pulse is wider than the Up pulse. When the reset transistor is connected, and "clka" signal is delayed by 1.5 ns. Figure 7 is the zoomed plot of the simulation where the Dn and Up signals are perfectly in phase with the pulse widths being 224.6 ps (Dn) and 222.8ps (Up). The voltage of pumping-up and pumping down for the modified CP is in the range between 0.1 V and 1.8V.

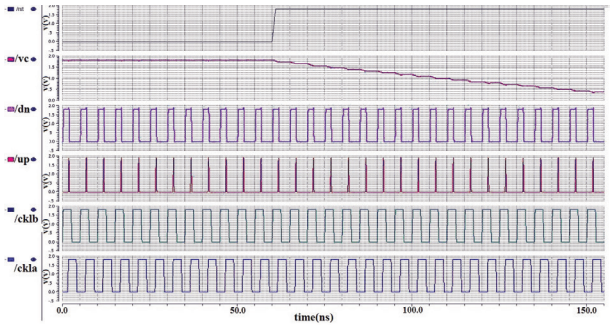


Figure 6: Post layout of the proposed CP Circuit: Pumping-down@ (Vdd = 1.8 V, f = 10MHz).

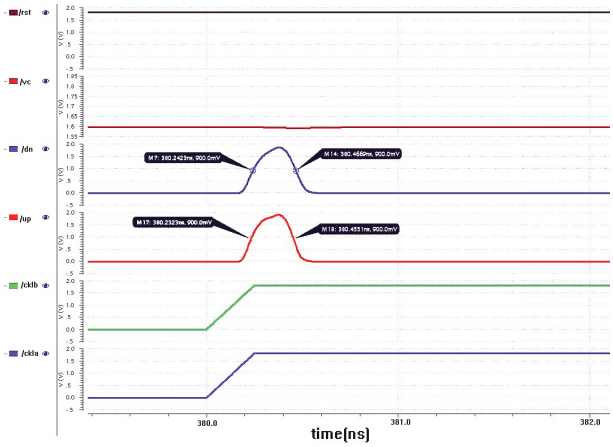


Figure 7: Simulation result of proposed CP Circuit (When both clock sources set are perfectly in-phase)

Figure 8 describes the current matching of the designed charge pump circuit, and it is observed that the maximum value for the current mismatch is zero. The curve (Figure 8 results) is taken from the Mentor Graphics EZwave analysis window. In EZwave window, the current mismatch is shown in the form of the graph instead of a percentage. The cyan and Blue, both graphs represent the current (Y-axis) graph with respect to time(X-axis). It can be seen in the figure that, the changes in the current of both graphs with respect to time (X-axis) is almost the same. There is no difference in current fluctuation which represent the Zero current mismatch. The zero current mismatches are achieved because of the low voltage NMOS cascade mirror technique and the addition of the M5 and M9 which are connected to the node "aout" through the mirror

transistors M6 and M8. For the PMOS switched mirror, the low-voltage cascade current mirror is connected to Gnd and for the NMOS switched mirror VDD is chosen as these are the values of Up and Dn signals at the lock which results in higher matching. Figure 8 proves that this modified scheme manages to decrease the effects of charge sharing and the current mismatch as well.

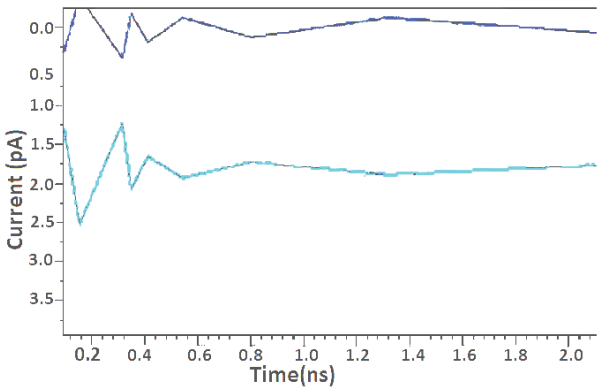


Figure 8: Current Up and Dn Plots (current matching)

Statistical analysis is very important in the absence of measured results. The Monte Carlo analysis of the proposed CP is presented in Figure 9 as a histogram representation. For 50 runs, the actual current mismatch of the proposed CP is zero. But randomly it shows the current mismatch varies from -2 to 2.5% which is very negligible. Besides, according to the netlist analysis of Monte Carlo simulation, the results showed that the current mismatch performance of the CP was stable around zero percentage. The Monte Carlo analysis was performed in the Mentor graphics environment.

The performance comparison among proposed CMOS charge pump circuit and recently reported other CMOS CP designs based on different input and output parameters are given in table 1.

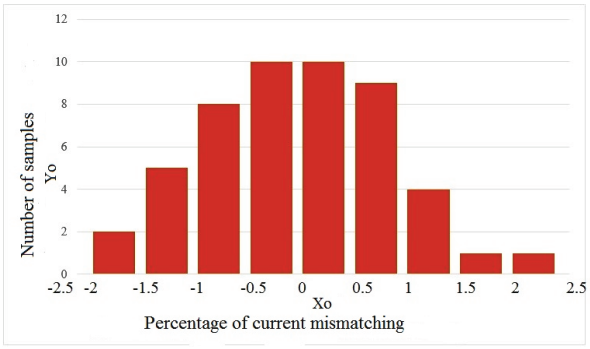


Figure 9: Monte Carlo simulation of current mismatch of the proposed CP

From table 1, it can be noted that the performance of the charge pump can be assessed by the current mismatch and power dissipation. For easy integration on a compact die, the designer tends to choose a simple circuit architecture for the charge pump. It can be observed from table 1 that the proposed CP circuit exhibits a many-fold reduction in both current mismatch and power dissipation compared to others designs. The major advancements have been achieved in the current mismatch of the proposed CP. The maximum current mismatch (<7%) occurs in [6] in table 1. The channel length modulation effect, the mismatch between PMOS and NMOS transistors and CMOS process variations cause this high current mismatch. Park et al.

Table 1: Comparison of proposed CMOS CP performance with other CMOS CP architectures.

Publication year and Ref.	CMOS CP scheme	CMOS process (µm)	Supply voltage (V)	Output voltage (V)	Current mismatch	Power consumed
[23] [2011]	Rail-to-rail op-amp	0.18	1.8	0.4-1.7	0.4%	0.9 mW
[24] [2013]	Basic CP-PLL	0.18	1.8	0.7-1.3	5%	1.6 mW
[8] [2013]	Digital calibration technique	0.18	1.8	-	1%	6.2 mW
[11] [2014]	Dickson CP with CTS's	0.18	1.8	1.8-4.2	-	1.2 mW
[25] [2015]	Feedback Op-amp	0.18	1.8	0.25- 1.	<5%	13 mW
[26] [2016]	Wide-swing current mirror	0.18	1.8	0.3- 1.5	0.32%	0.38 mW
[6] [2017]	Feedback loop	0.18	1.8	0.3-1.4	<7%	740 µW
Proposed CMOS CP	**Current mirror and chain inverter**	**0.13**	**1.8**	**0.1-1.8**	**0%**	**0.178 µW**

[25] suggested architecture also suffers from a high current mismatch of <5% because of the finite output impedance of the current source and highest power consumption of 13 mW. A high power consumption and current mismatch are achieved at the same time by Zhiqun et al. [6] Implementing a rail-to-rail operational amplifier. The recently reported CP proposed by Lozada et al. [8] managed to achieve a good current mismatch of 0.32% and less power consumption compared to [6, 11]. Therefore, compared to results mentioned in table 1, it can be concluded that the proposed charge pump circuit has the lowest power consumption of 0.178 mW and provides the lowest (zero) current mismatch by using the current mirror and chain inverter technique which leads to a high-performance CPPLL. Moreover, in the case of output voltage, it is clear that the output voltage of the proposed CP is significantly higher than those of all previously designed [24-26] charge pumps. This signifies the notable enhancement in output over those achieved in previous researches.

Figure 10 presents the complete layout of the proposed CP using TSMC 130 nm CMOS process. The dimension of the designed CP layout is 17 x 59.5 μm. Since the CP circuit covers only a small area, it reduces the cost as well. In this design, the triple-well isolated MOSFET structure has been used. Multi-finger structure has also been implemented for transistors with large aspect ratios to keep the conductivity within acceptable limits. The layout is designed for the convenience of cascading an extra pumping stage to the output voltage for additional improvement. Fabrication in CMOS technology makes it a good candidate for integration with other CMOS-based devices or modules in telecommunications and other electronic applications.

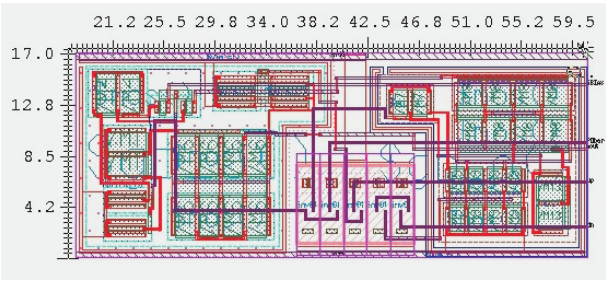


Figure 10: Layout diagram of proposed CMOS CP using TSMC 130 nm CMOS technology

4 Conclusions

The CP output parameters have a large impact on PLL performance. To meet the current demand of low power consumption, zero current mismatch and zero net charges, an enhanced charge pump circuit implementing the current mirror technique along with an inverter is presented in this research. The low voltage NMOS cascade mirror technique and additional transistors that are connected to the output node through the mirror transistors manage to achieve the lowest current mismatch. The post-layout result shows that the proposed charge pump circuit provides zero current mismatch at 1.8 V supply voltage with a pumping capacitor of 0.1 pF and consumes only 0.178 μW. The charge pump circuit is suitable for Readerless RFID applications and can be widely used in various low power wireless electronic devices such as a transceiver; disk read/write channels for high-speed data transmission, clock synthesis, synchronization, jitter reduction, etc.

5 Conflicts of Interest

"The authors declare no conflict of interest."

6 Acknowledgment

This research is financially supported by University Kebangsaan Malaysia. Project code: [AP-2017-008/1].

7 References

1. Jiang X., Yu X., Moez K., Elliott D. High-Efficiency Charge Pumps for Low-Power On-Chip Applications, IEEE journal of Solid State Circuit, 2018, 65(3): 1143 – 1153. https://doi.org/10.1109/tcsi.2017.2759767
2. Badal M T I, Reaz M B I, Bhuiyan M, Kamal N, CMOS Transmitters for 2.4-GHz RF Devices: Design Architectures of the 2.4-GHz CMOS Transmitter for RF Devices, IEEE Microwave Magazine, 2019, 20 (1), pp: 38-61. https://doi.org/10.1109/mmm.2018.2875607
3. Yun G S, KOK S L, Rahman, M B, Development of self-powered thermoelectric based RF transmitter circuit, IEEE International conference on Power and Energy, Nov, 2016, Melaka, Malaysia. https://doi.org/10.1109/pecon.2016.7951602
4. Badal M T I, Reaz M B I, Jalil Z and Bhuiyan M, Low Power High-Efficiency Shift Register Using Implicit Pulse-Triggered Flip-Flop in 130 nm CMOS Process for a Cryptographic RFID Tag, Electronics, 2016, 5(4), pp: 92. https://doi.org/10.3390/electronics5040092 5. Badal M T I, Reaz M B I, Yeng L S, Bhuiyan M, Advancement of CMOS transimpedance amplifier for optical receiver, Transactions on Electrical and

Electronic Materials, 2018, 20(2), pp:73-84. https://doi.org/10.1007/s42341-018-00092-5
6. Estebsari M, Gholami M, Ghahramanpour M. A Novel Charge Pump with Low Current for Low-Power Delay-Locked Loops, *Circuits System and Signal Processing*, 2017, 36(9), pp. 3514–3526. https://doi.org/10.1007/s00034-016-0481-6
7. Chen Y, Mak P I, Zhou Y. Self-tracking charge pump for fast-locking PLL, *Electronics letters*, 2010, 46(11), pp. 755-757. https://doi.org/10.1049/el.2010.3562
8. Jeong C H, Kim K Y, Kwon C K, Kim H, Kim S W. Digital calibration technique using a signed counter for charge pump mismatch in phase-locked loops, *IET Circuits, Devices, Systems*, 2013, 7(6), pp. 313-318. https://doi.org/10.1049/iet-cds.2013.0011
9. Choi Y S, Han D H. Gain-boosting charge pump for current matching in phase-locked loop, *IEEE Transactions on Circuits and Systems II, Express Briefs*, 2006, 53(10), pp. 1022-1025. https://doi.org/10.1109/tcsii.2006.882122
10. Zaziabl A. Low power 1 GHz charge pump phase-locked loop in 0.18 μm CMOS process, *Proceedings of the 17th International Conference Mixed Design of Integrated Circuits and Systems-(MIXDES)*, 2010, pp. 277-282.
11. Kailuke C, Agrawal P, Kshirsagar R. Design of phase frequency detector and charge pump for low voltage high frequency PLL, *IEEE International Conference On Electronic Systems, Signal Processing and Computing Technologies (ICESC)*, 2014. pp. 74-78. https://doi.org/10.1109/icesc.2014.21
12. Badal M T I, Reaz M B I, Farayez A, Ramli S, Kamal N, "Design of a low-power CMOS Level Shifter for low-delay SoCs in silterra 0.13 μm CMOS process", Journal of Engineering Science and Technology Review, 2017, 10(4), pp. 10-15. https://doi.org/10.25103/jestr.104.02
13. Park J, Kim N, Won D, Choi H. High performance two-stage charge-pump for spur reduction in CMOS PLL, *Proceeding of the 11th IEEE International Multi-Conference on Signal, System and Device (SSD)*, 2014, pp. 1-7. https://doi.org/10.1109/ssd.2014.6808749
14. Badal M T I, Mashuri M B, Reaz M B I, Kamal N, Hashim F H, Low power high speed current comparator using 130nm CMOS technology, International Conference on Advances in Electrical, Electronic and System Engineering, 2016, pp: 72-76, Malaysia. https://doi.org/10.1109/icaees.2016.7888012
15. Gupta J A, Sangal A, Verma H. High speed CMOS charge pump circuit for PLL applications using 90nm CMOS technology, *Proceedings of the IEEE world Congress on Information and Communication Technologies (WICT)*, 2011, pp. 346-349. https://doi.org/10.1109/wict.2011.6141270
16. Paemel M V. Analysis of a charge-pump PLL, a new model. *IEEE Transactions on communications*, 1994, 42(7), pp. 2490-2498. https://doi.org/10.1109/26.297861
17. Cheng S, Tong H, Martinez J S, Karsilayan A I. Design and Analysis of an Ultrahigh-Speed Glitch-Free Fully Differential Charge Pump With Minimum Output Current Variation and Accurate Matching, *IEEE Transactions on Circuits and Systems II, Express Briefs*, 2006, 53(9), pp. 843-47. https://doi.org/10.1109/tcsii.2006.879100
18. Rhee W. Design of high-performance CMOS charge pumps in phase-locked loops, *Proceeding of the 1999 IEEE International Symposium on Circuits and Systems (Florida, USA)*, 1999, pp. 545-548. https://doi.org/10.1109/iscas.1999.780807
19. Larsson P. A 2-1600-MHz CMOS clock recovery PLL with low-Vdd capability, *IEEE Journal of Solid-State Circuits*, 1999, 34(12), pp. 1951-60. https://doi.org/10.1109/4.808920
20. Ahola R, Halonen, K. A 1.76-GHz 22.6-mW ΔΣ fractional-n frequency synthesizer, *IEEE Journal of Solid-State Circuits*, 2003. 38(1), pp. 138-140. https://doi.org/10.1109/jssc.2002.806261
21. Lee J S, Keel M S, Lim S I, Kim S. Charge pump with perfect current matching characteristics in phase-locked loops, *Electronics Letters*, 2000, 36(23), pp. 1907-1908. https://doi.org/10.1049/el:20001358
22. Huh H. et al, A CMOS dual-band fractional-N synthesizer with reference doubler and compensated charge pump, *Proceeding of the IEEE International Solid-State Circuits Conference (ISSCC), Digest of Technical Papers*. 2004, pp. 100-101. https://doi.org/10.1109/isscc.2004.1332613
23. Zhiqun L, Shuangshuang Z, Ningbing H. Design of a high-performance CMOS charge pump for phase-locked loop synthesizers, *Journal of Semiconductors*, 2011, 32(7), pp. 075007. https://doi.org/10.1088/1674-4926/32/7/075007
24. Yoshimura T, Iwade S, Makino H, Matsuda, Y. Analysis of pull-in range limit by charge pump mismatch in a linear phase-locked loop, *IEEE Transactions on Circuits and Systems I, Regular Papers*, 2013, 60(4), pp. 896-907. https://doi.org/10.1109/tcsi.2012.2215393
25. Park J W, Choi H Y, Kim N S. Two-stage feedback-looped charge-pump for spur reduction in CMOS PLL, *Analog Integrated Circuits and Signal Processing*, 2015, 83(2), pp. 143-148. https://doi.org/10.1007/s10470-015-0517-z

26. Lozada O, Espinosa G. A charge pump with a 0.32% of current mismatch for a high speed PLL, *Analog Integrated Circuits and Signal Processing*, 2016, 86(2), pp. 321-326. https://doi.org/10.1007/s10470-015-0676-y

Arrived: 18. 11. 2018
Accepted: 14. 05. 2019

https://doi.org/10.33180/InfMIDEM2019.202

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 49, No. 2(2019), 61 – 68

Linearly Tunable CMOS Voltage Differencing Transconductance Amplifier (VDTA)

Worapong Tangsrirat

Faculty of Engineering, King Mongkut's Institute of Technology Ladkrabang (KMITL), Bangkok, Thailand

Abstract: This paper proposes an alternative way to implement a linearly tunable CMOS voltage differencing transconductance amplifier (VDTA). It has been designed by using the floating current source (FCS) and the current squaring circuit. The circuit achieves its linear tunability by squaring the long-tail biasing current of the FCS. In this way, the transconductance gains of the proposed CMOS VDTA can be varied linearly through adjusting the DC bias currents. As an application example, the proposed VDTA is used in the design of an actively tunable voltage-mode multifunction filter. The derived filter possesses the following desirable properties: simultaneous realization of three standard filter functions; employment of only two grounded capacitors; and electronic tunability of the natural angular frequency and the quality factor. The performance of the proposed circuit and its filter design application were examined by PSPICE simulations with TSMC 0.25-mm CMOS real process technology.

Keywords: Voltage Differencing Transconductance Amplifier (VDTA); Current Squarer; MOS analog circuits; Low-voltage circuits; Electronically tunable.

Linearno nastavljiv CMOS napetostni transkonduktančni diferencialni ojačevalnik (VDTA)

Izvleček: Članek predlaga alternativno rešitev uporabe linearno nastavljivega CMOS napetostnega trnskonduktančnega diferencialnega ojačevalnika (VDTS). Načrtovan je z uporabo plavajočega tokovnega vira (FCS) in kvadriranjem toka. Vezje dosega linearno nastavljivost s kvadriranjem počasnega deleža toka FCS. Na ta način se lahko z nastavitvijo napajalnega toka linearno spreminja transkonduktančno ojačenje. Filter ima naslednje lastnosti: sočasna realizacija treh standardnih funkcij filtra, uporaba le dveh ozemljenih kondenzatorjev in elektronska nastaljivost wo in Q. Lastnosti so bile simuliranje v PSPICE okolju v TSMC 0.25-mm CMOS tehnologiji.

Ključne besede: napetostni transkonduktančni diferencialni ojačevalnik; (VDTA); tokovni kvadrirnik; analogna MOS vezja; nizkonapetostna vezja; elektronska nastavljivost

** Corresponding Author's e-mail: drworapong@gmail.com*

1 Introduction

A brief review of the recently reported active elements and an introduction to several new controllable elements are given in [1]. Among other things, the voltage differencing transconductance amplifier (VDTA) is one of attractive active devices with two-parameter control [2-6]. This device is a modified version of the previously introduced current differencing transconductance amplifier (CDTA) element, in which the current differencing unit at the input stage is replaced by the voltage differencing unit. Usually, the VDTA solution can be realized by composing two voltage-controlled current sources, which are interconnected internally. Each of them provides two independent transconductance gains (g_{mF} and g_{mS}), which are electronically adjustable by external DC biasing currents [5]. Therefore, the VDTA element is very useful in active circuit synthesis and quite suitable for electronically controllable analog circuits. Another advantageous feature of this element is that it can easily be used for transconductance-mode solutions due to its input signals being voltages while the output signals are current [2]. Several CMOS reali-

zations of the VDTA circuit have been described in the literature [2-4]. Previously, the CMOS implementation of the VDTA employing basic floating current sources (FCSs) and supply voltages of ±0.9 V was introduced in [2]. The improved CMOS VDTA was suggested in [3], in which the ideal current sources are realized with swing cascade current mirrors. This kind of current mirrors is used because it has good accuracy and high-output impedance, and the minimum output voltage swing is approximated to $2V_{DS(sat)}$ [7]. In [4], the design of the CMOS VDTA was also reported, where both transconductance sections were derived from the structure presented in [5]. In this structure, the well-known configuration of multiple-output second-generation current conveyor (MO-CCII) has been supplemented to obtain the required number of current outputs of the first transconductance section. However, their major disadvantage though is the well-known fact that their performance (namely the gain g_m) is directly proportional to the square root function of the external DC biasing current. Due to this the tunability is non-linear, and their linear transconductance ranges are rather limited.

The motivation of this paper is to develop the CMOS VDTA with linearly tunable transconductance. To this aim, the proposed CMOS VDTA utilizes the floating current source (FCS) in its voltage-to-current conversion. In the presented work, the CMOS current squaring functional circuit with the output current proportional to the square of the input current is employed as a biasing circuit for the FCS. The main feature of the proposed VDTA is that it exhibits an ability to linearly tune its transconductane gains by electronic means through the external DC bias currents. To illustrate the application of the proposed VDTA, the design of active voltage-mode multifunction filter with single input and triple outputs is considered. It realizes simultaneously the three standard biquadratic filters namely lowpass (LP), bandpass (BP) and highpass (HP) from each output of the circuit. Orthogonal electronic programmability of ω_o and Q is also discussed in detail. PSPICE simulations with TSMC 0.25-µm CMOS process parameters are also reported, which demonstrate the linearity and effectiveness of the proposed VDTA and its application.

2 Basic concept of the VDTA

Basically, the VDTA is an alternative versatile active building block, having five high-impedance terminals, as symbolically shown in Fig.1. The characteristic between terminal voltages and currents can be described by the following matrix relation:

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ i_x \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_{mF} & -g_{mF} & 0 & 0 \\ 0 & 0 & g_{mS} & 0 \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_x \\ v_z \end{bmatrix}, \quad (1)$$

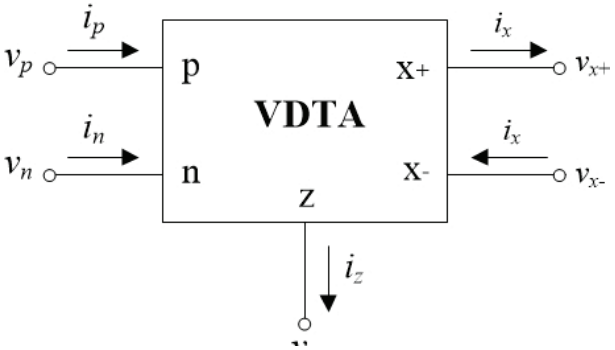


Figure 1: Circuit symbol of the VDTA.

where g_{mF} and g_{mS} are the first and second transconductance gains of the VDTA, respectively. In (1), the differential input voltage applied across the p and n terminals (v_p - v_n) is converted to a current flowing out of the z terminal (i_z) by g_{mF}. Similarly, a voltage across the z terminal (v_z) is transformed to the current outward from the x+ and x- terminals by g_{mS}.

3 Basic functional circuits

3.1 Current-squaring circuit

Fig.2 shows a current squaring circuit (M_1-M_3) based on the square-law characteristic of MOS transistors biased in the strong inversion region [8-10]. The current-controlled biasing circuit (M_{B1}-M_{B2}) is introduced in order to supply the bias voltage V_B, where I_A is the bias current. Assuming that all transistors are properly biased to operate in saturation mode and obey the ideal square-law function, the relation between the output current I_{SQ} and the input current I_B is given below.

$$I_{SQ} = \frac{I_B^2}{8I_A} \quad . \quad (2)$$

To guarantee a proper operation, the input current I_B is restricted within the range:

$$-4I_A < I_B < 4I_A \quad . \quad (3)$$

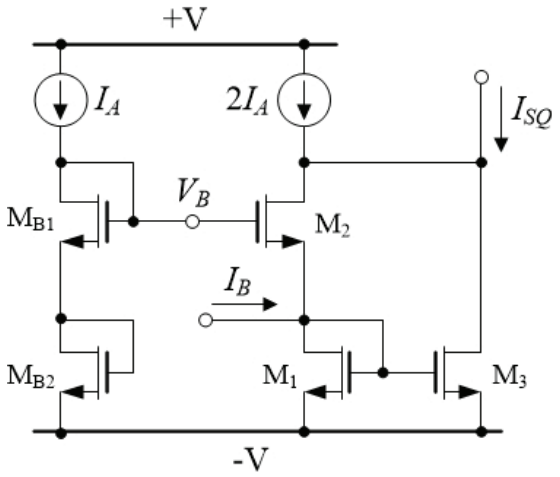


Figure 2: Current squaring functional circuit.

We observe from eq. (2) that I_{SQ} is the squaring function of I_B with the gain equal to $(1/8I_A)$. In addition to eq. (2), the current I_{SQ} is ideally temperature insensitive.

3.2 Floating Current Source

Fig.3 shows the circuit diagram of the floating current source (FCS) [11], which will be used as a fundamental circuit for exhibiting the transconductance gain of the proposed VDTA. The circuit can be viewed as two long-tailed differential pairs of PMOS and NMOS connected in parallel. It converts the differential input voltage ($v_{id} = v^+ - v^-$) into two balanced output currents i_{o+} and i_{o-}. The NMOS transistors M_4 and M_5 are identical and the PMOS transistors M_6 and M_7 are also identical. Assuming that all the transistors are working in saturation region, an effective small-signal transconductance of the FCS can be expressed as [11]:

$$g_m = \frac{i_{o+}}{v_{id}} = \frac{i_{o-}}{v_{id}} \cong \frac{g_{mn} + g_{mp}}{2} \quad , \tag{4}$$

where g_{mn} and g_{mp} are respectively the transconductance values of the NMOS and PMOS transistors, equal to :

$$g_{mn(p)} = \sqrt{K_{n(p)} I_O} \quad . \tag{5}$$

In above expression, $K_{n(p)} = \frac{\mu_{n(p)} C_{ox}}{2} \frac{W}{L}$ $\mu_{n(p)}$ is the average carrier mobility for NMOS and PMOS transistors, C_{ox} is the gate-oxide capacitance per unit area, W and L are the effective channel width and length, and I_O is the external DC bias current. Evidently from eqs.(4) and (5), the g_m-value of the FCS circuit in Fig.3 is proportional to a square-root of the control current I_O.

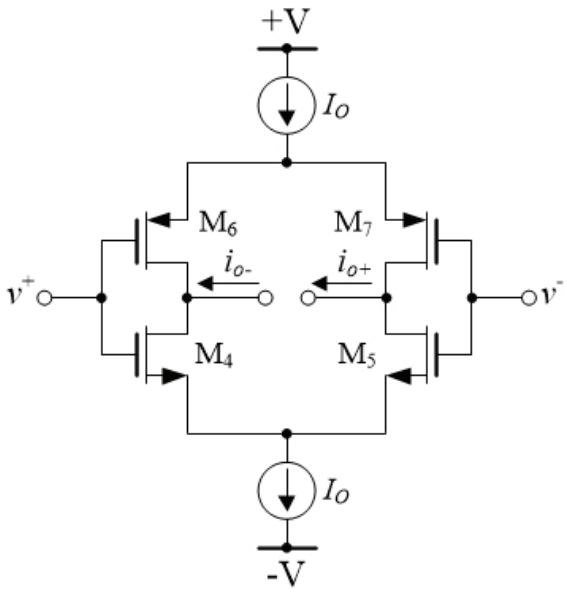


Figure 3: CMOS FCS circuit.

4 Proposed linearly tunable VDTA

A complete circuit diagram of the proposed linearly tunable VDTA (LT-VDTA) and its symbol are shown in Fig.4. Basically, it consists of two FCSs (M_{9F}-M_{11F} and M_{9S}-M_{11S}) in Fig.3 and two current squaring circuits (M_{1F}-M_{3F} and M_{1S}-M_{3S}) in Fig.2. The current-controlled DC level-shifting circuit M_{B1}-M_{B2} and I_A provide a bias voltage V_B for the circuit. As seen in Fig.4, the currents I_{SQF} and I_{SQS} are mirrored to be the bias currents I_{OF} and I_{OS} of two FCSs by means of the current mirrors M_{4F}-M_{8F} and M_{4S}-M_{8S}, respectively. It can be arranged that if $(W/L)_{6F} = (W/L)_{5F} = 8(W/L)_{4F}$ and $(W/L)_{6S} = (W/L)_{5S} = 8(W/L)_{4S}$, then, using eq.(2) and considering $I_{OF} = 8I_{SQF}$ and $I_{OS} = 8I_{SQS}$, we have :

$$I_{OF} = \frac{I_{BF}^2}{I_A} \quad , \tag{6}$$

and

$$I_{OS} = \frac{I_{BS}^2}{I_A} \quad . \tag{7}$$

Substituting eqs.(6) and (7) into (5), and solving for the first and second transconductance gains of the proposed LT-VDTA in Fig.4, the results are :

$$g_{mF} = K_m I_{BF} \quad , \tag{8}$$

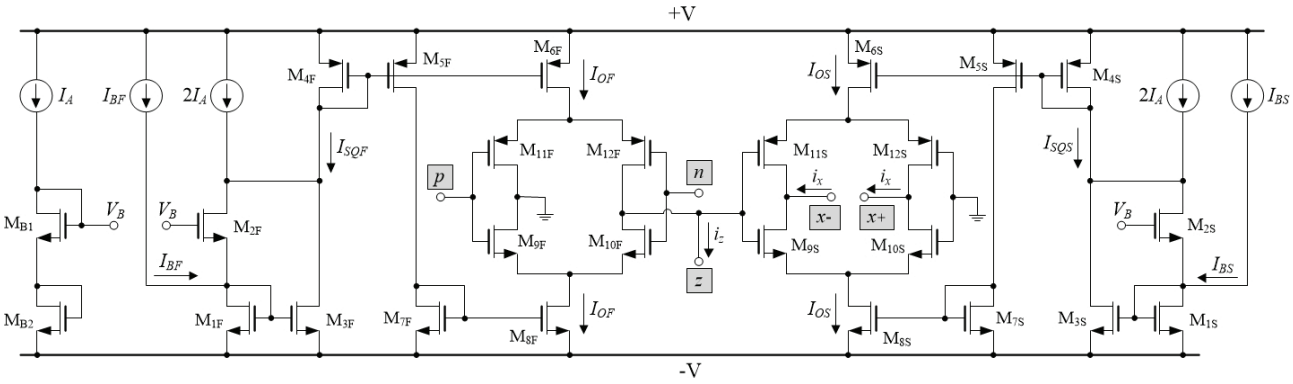
and

$$g_{mS} = K_m I_{BS} \quad , \tag{9}$$

where

$$K_m = \frac{\sqrt{K_n} + \sqrt{K_p}}{2\sqrt{I_A}} \quad . \tag{10}$$

(a)



(b)

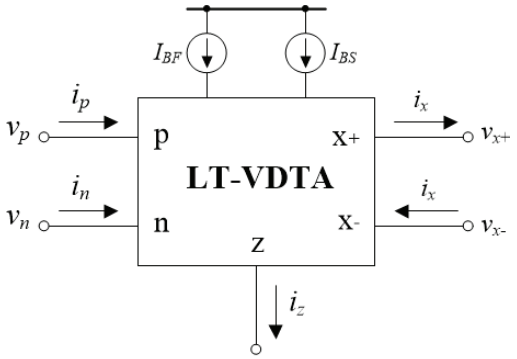


Figure 4: Proposed CMOS VDTA with linearly transconductance tuning. (a) complete circuit diagram; (b) its circuit symbol

Since K_m is considered as a constant value, eqs.(8) and (9) imply that the transconductances g_{mF} and g_{mS} of the proposed LT-VDTA can be adjusted electronically and linearly by I_{BF} and I_{BS}, respectively. As was stated earlier, in order for the proposed circuit to operate correctly, the linear operating condition for the input controlling currents I_{BF} and I_{BS} is bounded according to eq.(3).

Owing to the performance of the traditional FCS stage used in the proposed LT-VDTA structure of Fig.4, the output resistances at terminals z, x+ and x- are not high enough for some applications. In order to increase the output resistance level, the improved FCS [12] can be employed for this structure. However, while the output resistance value is improved, the output voltage swing drops by up to $V_{DS(sat)}$.

5 Simulations, results and discussions

For all the circuits examined in this work, the computer simulations with PSPICE are performed using model parameters of TSMC 0.25-µm CMOS technology. The transistor sizes used for simulation are listed in Table 1. Bias voltages were ±V = 1.5 V and bias currents I_A were 50 µA.

Table 1: Transistor sizes of the proposed LT-VDTA in Fig.4.

Transistors	W (µm)	L (µm)
M_{B1} - M_{B2}, M_{1F} – M_{2F}, M_{1S} - M_{2S}, M_{4F}, M_{4S}, M_{7F}, M_{7S}	7	0.25
M_{3F}, M_{3S}	6	0.25
M_{5F} - M_{6F}, M_{5S} - M_{6S}	49	0.25
M_{8F}, M_{8S}	6.2	0.25
M_{9F} - M_{10F}, M_{9S} - M_{10S}	17	0.25
M_{11F} - M_{12F}, M_{11S} - M_{12S}	24	0.25

The CMOS current squaring circuit in Fig.2 is simulated. Fig.5 illustrates the DC current transfer curves of the current squaring circuit in Fig.2, obtained for the input controlling current I_B value ranging from -200 µA to 200 µA. It can be deduced from the simulation results that the circuit performs the current squaring operation as expected.

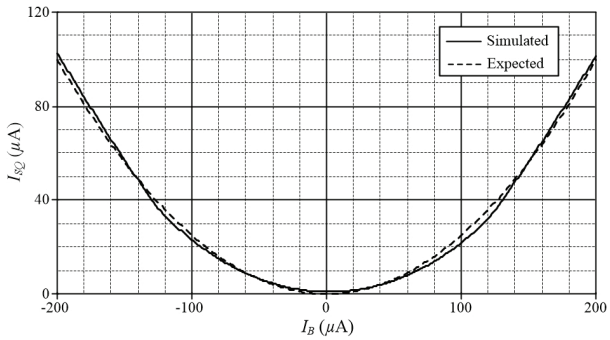


Figure 5: DC current transfer curves of the current squaring circuit in Fig.2.

In order to demonstrate the linear tuning performance of the proposed LT-VDTA in Fig.4, the simulation for the

transconductance g_{mF} is carried out. Fig.6 shows the g_{mF} variations as a function of the input controlling current I_{BF}. In these plots, the simulated results and the expected values are compared, and in good agreement over a considerable input range from 20 μA to 180 μA. It is clear from the curves that the proposed circuit can be tuned linearly by means of the current I_{BF}.

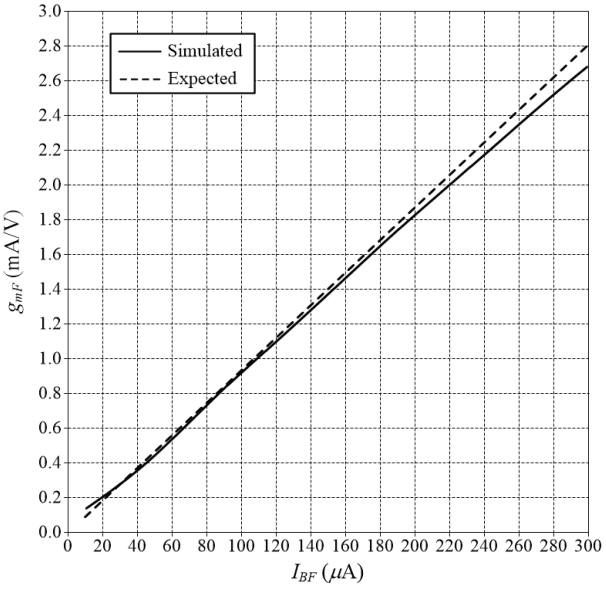


Figure 6: Expected and simulated g_{mF} of the proposed LT-VDTA of Fig.4 as a function of I_{BF}.

The DC transfer functions of the proposed LT-VDTA in Fig.4 are also simulated and shown in Fig.7, with v_{id} (= $v_p - v_n$,) continuously changing from -400 mV to 400 mV, and I_{BF} being equal to 50 μA, 100 μA and 150 μA, respectively. For I_{BF} = 150 μA, the circuit has a linear region over ±180 mV and non-linearity error is less than 9.16%.

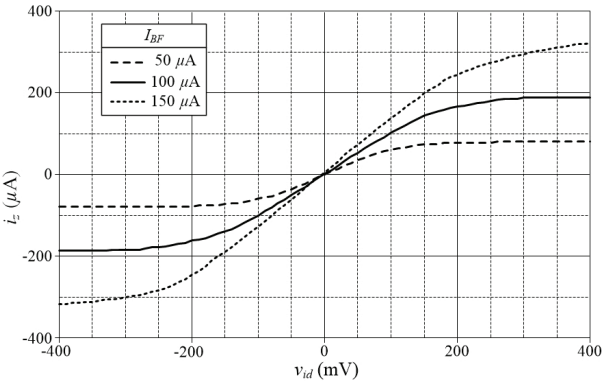


Figure 7: Simulated DC transfer characteristics between v_{id} and i_z with tuning I_{BF}.

To study the AC transfer characteristic of the proposed LT-VDTA, the simulated frequency responses for g_{mS} when I_{BS} is swept from 50 μA to 150 μA with 50 μA step size are plotted in Fig.8. According to Fig.8, the useful bandwidth of about 400 MHz can be observed. In addition to the simulation results, the maximum power dissipation is 6.25 mW, when v_{id} = 180 mV, and $I_{BF} = I_{BS}$ 150 μA. The quiescent power dissipation is 1.34 mW, when v_{id}, I_{BF} and I_{BS} are zero.

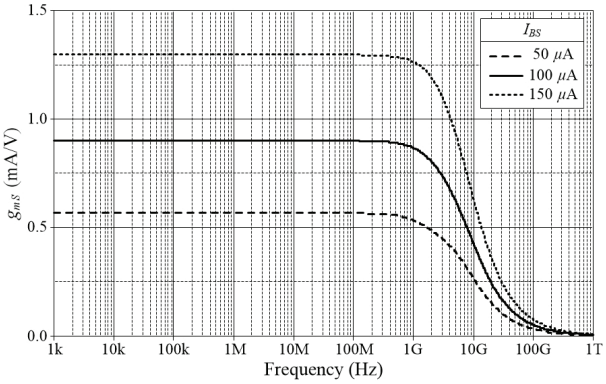


Figure 8: Simulated frequency characteristics of g_{mS} with tuning I_{BS}.

6. Active voltage-mode multifunction filter realization

To demonstrate the effectiveness of the proposed LT-VDTA, an active voltage-mode multifunction filter of Fig.9 is realized as a design example [13]. The circuit consisting of two proposed LT-VDTAs in Fig.4 and two grounded capacitors realizes three standard biquadratic filtering functions, i.e. lowpass (LP), bandpass (BP) and highpass (HP), simultaneously without changing its configuration and without the need to impose component constraints. Straightforward analysis of Fig.9 using eq.(1) yields the following three voltage transfer functions.

$$H_{LP} = \frac{V_{LP}(s)}{V_{in}(s)} = H_0\left(\frac{g_{mF2}g_{mS2}}{C_1C_2}\right)\left[\frac{1}{D(s)}\right], \quad (11)$$

$$H_{BP} = \frac{V_{BP}(s)}{V_{in}(s)} = H_0\left(\frac{g_{mF2}}{C_1}\right)\left[\frac{s}{D(s)}\right], \quad (12)$$

and

$$H_{HP} = \frac{V_{HP}(s)}{V_{in}(s)} = H_0\left[\frac{s^2}{D(s)}\right], \quad (13)$$

where

$$H_0 = \frac{g_{mF1}}{g_{mS1}}, \quad (14)$$

$$D(s) = s^2 + \left(\frac{g_{mF2}g_{mS2}}{g_{mS1}C_1}\right)s + \left(\frac{g_{mF1}g_{mF2}g_{mS2}}{g_{mS1}C_1C_2}\right), \quad (15)$$

and g_{mFi} and g_{mSi} (i = 1, 2) are respectively first and second transconductance gains of the i-th LT-VDTA. It follows from eqs.(11)-(15) that the natural angular frequency (ω_o) and the quality factor (Q) of the filter are

$$\omega_o = \sqrt{\frac{g_{mF1}g_{mF2}g_{mS2}}{g_{mS1}C_1C_2}} \quad , \quad (16)$$

and

$$Q = \sqrt{\frac{g_{mF1}g_{mS1}C_1}{g_{mF2}g_{mS2}C_2}} \quad . \quad (17)$$

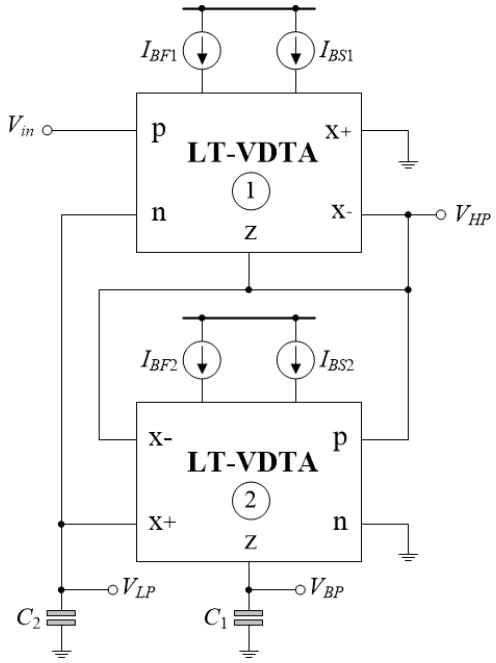


Figure 9: Actively tunable voltage-mode multifunction filter realization using the proposed LT-VDTAs.

To achieve independent filter parameter control, a proper design can be developed by setting equal transconductances such that $g_{m1} = g_{mF1} = g_{mS1}$ and $g_{m2} = g_{mF2} = g_{mS2}$, then ω_o and Q from eqs.(16) and (17) turn to

$$\omega_o = \sqrt{\frac{g_{m2}}{C_1C_2}} \quad , \quad (18)$$

and

$$Q = \frac{g_{m1}}{g_{m2}}\sqrt{\frac{C_1}{C_2}} \quad . \quad (19)$$

The parameter ω_o can be tuned separately by changing g_{m2}. The transconductance ratio of g_{m1} and g_{m2} can be used for an adjustment of the parameter Q. However, if independent electronic control is needed, only g_{m1} could be used for Q control.

Furthermore, from eqs.(16) and (17), the active and passive sensitivities of ω_o and Q can be expressed as:

$$S^{\omega_o}_{g_{mF1},g_{mF2},g_{mS2}} = -S^{\omega_o}_{g_{mS1}} = \frac{1}{2} \ , \ S^{\omega_o}_{C_1,C_2} = -\frac{1}{2} \quad (20)$$

and

$$S^{Q}_{g_{mF1},g_{mS1}} = -S^{Q}_{g_{mF2},g_{mS2}} = \frac{1}{2} \ , \ S^{Q}_{C_1} = -S^{Q}_{C_2} = \frac{1}{2} \quad (21)$$

Both are low, and equal to 0.5 in magnitude.

As a design example, the multifunction filter of Fig.9 has been realized to obtain the LP, BP and HP responses with the natural angular frequency $f_o = \omega_o/2\pi \cong 5.50$ MHz and the quality factor Q = 1. For this purpose, the circuit components were set to: $I_B = I_{BF1} = I_{BS1} = I_{BF2} = I_{BS2}$ = 70 µA ($g_m = g_{mF1} = g_{mS1} = g_{mF2} = g_{mS2} \cong 0.66$ mA/V), and $C_1 = C_2$ = 20 pF. The simulated LP, BP and HP amplitude responses of the circuit are shown in Fig.10, where the simulated values of f_o were found to have a maximum deviation of 2.83% from the expected values. In this simulation, the total power consumption of the designed filter is about 4.51 mW.

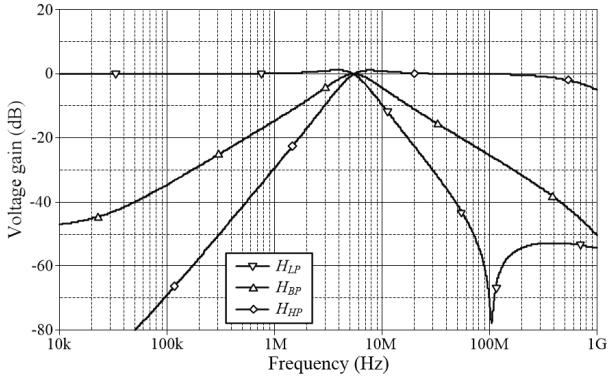


Figure 10: Simulated AC transfer responses for the actively voltage-mode multifunction filter in Fig.9.

In Fig.11, the electronic adjustment of the BP characteristic is illustrated by simulating multiple values of f_o (i.e. f_o = 4.50 MHz, 7.60 MHz, and 11.35 MHz), and keeping a constant Q = 1. Its responses for three values of f_o are obtained by tuning identical bias currents I_B = 50 µA, 100 µA, and 150 µA, respectively.

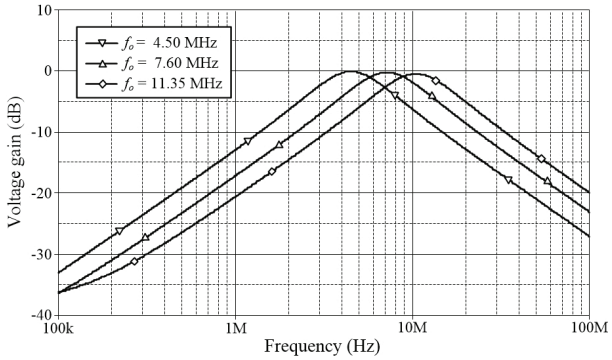


Figure 11: Simulated BP responses of Fig.9 with tuning f_o.

The simulation results of the BP response for variable Q and fixed f_o are given in Fig.12. In this way, the values of Q were tuned via LT-VDTA 1, for Q = 5, 7, 10, which correspond to I_{B1} (i.e., $I_{B1} = I_{BF1} = I_{BS1}$) = 250 µA, 350 µA, 500 µA ($g_{m1} \cong$ 2.40 mA/V, 3.33 mA/V, 4.86 mA/V). A constant f_o = 4.50 MHz was set with the bias currents of LT-VDTA 2, i.e., $I_{B2} = I_{BF2} = I_{BS2}$ = 50 µA ($g_{m2} \cong$ 0.57 mA/V).

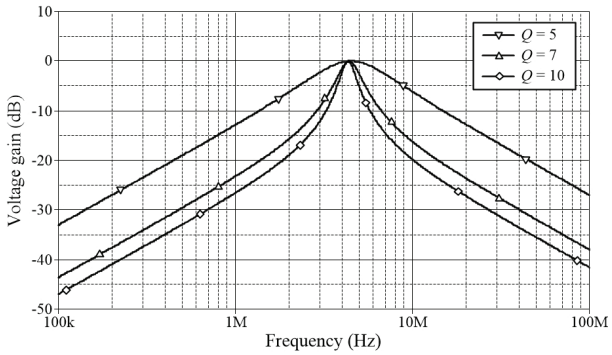


Figure 12: Simulated BP responses of Fig.9 with tuning Q.

7 Conclusions

In this work, a linearly and electronically tunable CMOS VDTA circuit is realized. The circuit realization is based on floating current sources (FCSs) for implementing the transconductance stages. The CMOS current squaring circuit is used for supplying the long-tail bias current of the FCs stages. Its transconductance gains are linearly tuned and accurately determined by the external DC supplied currents. The use of the proposed VDTA is illustrated with a realization of an electronically tunable voltage-mode multifunction filter, which employs two VDTAs and two grounded capacitors. PSPICE simulations, performed using TSMC 0.35-µm CMOS technology and confirming the performance of the proposed circuit and its application, are also given.

8 Acknowledgements

This work was supported by King Mongkut's Institute of Technology Ladkrabang Research Fund [grant number KREF116001]. The author is grateful to Mr. Natchanai Roongmuanpha for his circuit simulation on an earlier version of the manuscript. Also, the author gratefully acknowledges the constructive comments and suggestions of all the anonymous reviewers, which have been very useful in the preparation of the revised version of the manuscript.

9 References

1. D. Biolek, R. Senani, V. Biolkova, Z. Kolka, "Active elements for analog signal processing: classification, review, and new proposals", *Radioengineering*, vol.17, no.4, pp.15-32, 2008.
2. A. Yesil, F. Kacar, H. Kuntman, "New simple CMOS realization of voltage differencing transconductance amplifier and its RF filter application", *Radioengineering*, vol.20, no.3, pp. 632-637, 2011.
3. A. Yesil, F. Kacar, "Electronically tunable resistorless mixed mode biquad filters", *Radioengineering*, vol.22, no.4, pp.1016-1024, 2013.
4. J. Jerabek, R. Sotner, K. Vrba, "Electronically adjustable triple-input single-output filter with voltage differencing transconductance amplifier", *Rev. Roum. Sci. Techn.– Électrotechn. et Énerg.*, vol.59, no.2, pp.163-172, 2014.
5. J. Satansup, W. Tangsrirat, "Compact VDTA-based current-mode electronically tunable universal filters using grounded capacitors, *Microelectron. J.*, vol.45, no.6, pp.613-618, 2014. https://doi.org/10.1016/j.mejo.2014.04.008
6. W. Tangsrirat, S. Unhavanich, "Voltage differencing transconductance amplifier-based floating simulators with a single grounded capacitor", *Indian J. Pure & Appl. Phys.*, vol.52, no.6, pp.423-428, 2014.
7. P. E. Allen, D. R. Holberg, *CMOS Analog Circuit Design*, New York : Oxford, 2002.
8. K. Bult, H. Walliga, "A class of analog CMOS circuits based on the square-law characteristic of an MOS transistor in saturation", *IEEE J. Solid-State Circuits*, vol.SC-22, no.3, pp. 357-365, 1987. https://doi.org/10.1109/jssc.1987.1052733
9. O. Landolt, E. Vittoz, P. Heim, "CMOS self-biased euclidean distance computing circuit with high dynamic range", *Electron. Lett.*, vol.28, no.4, pp.352-354, 1992. https://doi.org/10.1049/el:19920220
10. C. Popa, "CMOS logarithmic curvature-corrected voltage reference by using a multiple differential

structure", *Rev. Roum. Sci. Techn.– Électrotechn. et Énerg*., vol.55, no.4, pp.436-444, 2010.
11. A. F. Arbel, L. Goladminz, "Output stage for current-mode feedback amplifiers, theory and applications", *Analog Integr. Circ. Signal Process*., vol.2, no.3, pp. 243-255, 1992. https://doi.org/10.1007/bf00276637
12. M. Altun, H. Kuntman, "Design of a fully differential current-mode operational amplifier with improved input-output impedances and its applications", *Int. J. Electron. Commun. (AEU)*, vol.62, no.3, pp. 239-244, 2008. https://doi.org/10.1016/j.aeue.2007.03.020
13. J. Satansup, W. Tangsrirat, "Voltage-mode multifunction filter using VDTA and grounded capacitors", *Proc. the 6th Conf. Electrical Eng. Network of Rajamangala University of Tech. 2014 (EENET 2014*), pp.533-536, 2014.

Arrived: 11. 04. 2019
Accepted: 21. 05. 2019

https://doi.org/10.33180/InfMIDEM2019.203

Informacije MIDEM
Journal of Microelectronics, Electronic Components and Materials
Vol. 49, No. 2(2019), 69 – 77

Simulation on the Interfacial Singular Stress-strain Induced Cracking of Microelectronic Chip Under Power On-off Cycles

Xiaoguang Huang

China University of Petroleum (East China), Department of Engineering Mechanics, Qingdao, China

Abstract: Thermal fatigue failure of a microelectronic chip usually initiates from the interface between the solder joint and substrate due to the mismatch in coefficients of thermal expansion (CTE). Because of the viscoelastic creep properties of the solders, the stress and strain at the solder/substrate interfaces are strongly dependent on temperature and time. Based on the established creep constitutive models of the solder materials, a three-dimensional thermomechanical analysis of the microelectronic chip undergoing power on-off cycles is conducted based on the finite element method (FEM). The singular interfacial stress-strain fields are obtained and the singular field parameters are quantitatively evaluated. Furthermore, the crack nucleation in power on-off fatigue test of the microelectronic chip is observed, to verify the conclusion that the singular stress-strain induces thermal fatigue failure from the solder/substrate interface.

Keywords: Thermal fatigue; microelectronic chip; creep; singular field; crack nucleation

Simulacija razpok mikroelektronskega čipa zaradi posameznih mejnih stresov pri ciklih vklapljanja napajanja

Izvleček: Različni termični koeficienti materialov so večinoma vzrok za odpvedi zaradi termične utrujenosti in pri čipu izhajano iz stične površine med lotom in substratom. Zaradi viskoelastičnosti lota je stress na mejni površini močno odvisen od časa in temperature. Uporabljena je tridimenzionalna termo-mehanična analiza vplivov ciklanja vklapljanja napajalne napetosti z uprabo metode končnih elementov. Kvantitativno so ocenjeni posamezni parametri in opažen je bil pojav nastajanja razpok zaradi stresa na stiku lot/substrat.

Ključne besede: termična utrujenost; mikoelektronski čip; polzenje; nastanek razpok

* *Corresponding Author's e-mail: huangupc@126.com*

1 Introduction

The flip flat package technology is currently widely used in electronic engineering to meet the demands of high-speed functions and system miniaturization [1]. The high density and cost-effective requirements of the package structure have led to the emergence of small size and multiple input/output (IO) points in chip design. Solder joints, as the mechanical, electrical and heat-dissipating components, require excellent reliabilities during soldering and service [2-3]. In the soldering process, the formation of intermetallic compounds (IMCs) is a necessary condition for the formation of solder joints, and the reliability of solder joints is highly dependent on the formation and growth of IMC at the interface [4]. With the growth of intermetallic compounds, stress concentration easily appears at the interface of solder joint due to the mismatch of coefficients of thermal expansion of the materials, which causes the cracking and reduces the service life of solder joints [5-6]. Due to the increase of packaging density, both the size and shape of solder joints appear in various combinations, a quantitative evaluation method of the strength and life for solder joints is strongly expected.

Under thermal cyclic loading, failure or fatigue crack generally initiates from the interface edge or near to the interface between the solder joint and substrate, and its mechanism is strongly affected by the stress singularity at the interface edge or stress concentration induced by the interface [7-9]. Therefore, it is of practical importance to determine the stress state at the interface, so that the susceptibility to thermomechanical failure can be predicted for new geometry-to-material combinations. The traditional strength-based methods are not suitable since the stresses are singular even at the idealized interface edges or corners [10-12]. To overcome this concern, Hattori et al. [13] have suggested a singularity parameter approach for the interface reliability of plastic IC packages using two stress intensity parameters that characterize the stress distribution near a bonded edge along with the interface. Other authors [14-16] argued that the two parameters: singular order λ and stress intensity factor *K*, can be used in a criterion for crack initiation or delamination for certain structure configurations. Generally, FEM is a valuable tool for determining the constants λ and *K*. At the same time, finite element modeling enables the design to be evaluated before it is physically produced thus minimizing time and cost. The results obtained from the FEM modeling will be useful in suggesting design changes in terms of package geometry and choice of packaging materials.

The purpose of this study is to develop an objective method to analyze the thermal cyclic behavior and to evaluate the failure of solder joints in a microelectronic chip. According to the creep results of solder materials, the nonlinear creep constitutive models are established. The three-dimensional thermomechanical analysis of the microelectronic chip under power on-off cycles is conducted, and the time-dependent stress and strain at the solder/substrate interfaces are obtained. Finally, the details that the singular stress-strain promotes the thermal fatigue failures from these interfaces are discussed when compared with the results from fatigue tests.

2 Package description

The structure of the microelectronic chipset is presented in Fig. 1. It has nineteen pieces of chips, including two pieces of chip Q1, one piece of chip Q2, six pieces of chip Q3, four pieces of chip Q4 and six pieces of chip Q5, respectively. Their working powers are 35.7, 33.3, 25.8, 20.0 and 14.5 w, respectively. The schematic cross-sections of chip Q1-5 in layered structure are similar, i.e., substrate, insulate layer, Cu, SnAg3Cu0.5, Cu, Pb-5Sn, wafer and silica gel from bottom to top, as shown in Fig. 2. The main dimensions of chips Q1-5 are listed in Table1.

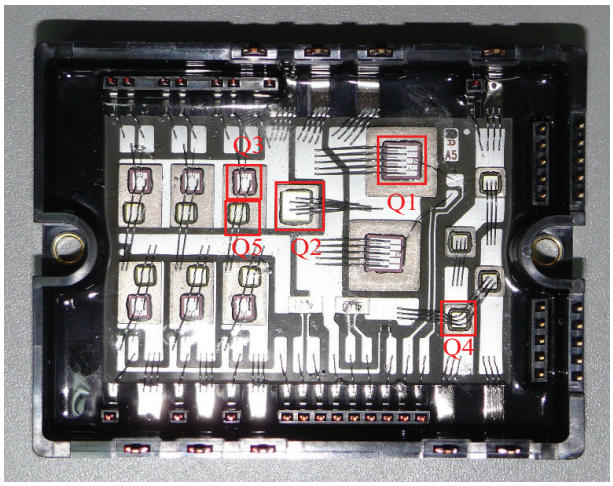


Figure 1: Structure of the microelectronic chipset

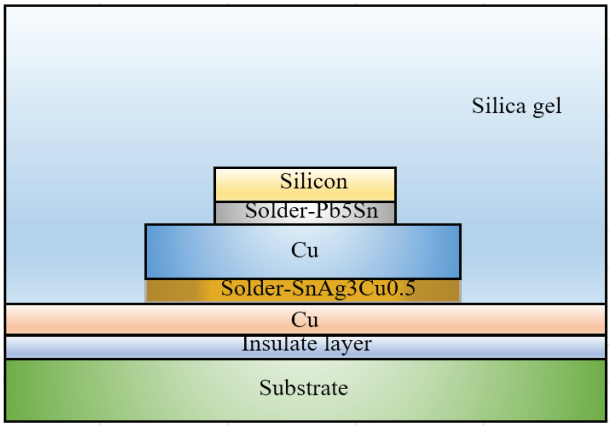


Figure 2: Schematic cross-section of the single chip

Table 1: Dimension of five different types of chips (unit: mm)

Chip type	Wafer $A_0 \times B_0 \times C_0$	Solder Pb-5Sn $A_1 \times B_1 \times C_1$	Solder $SnAg_3Cu_{0.5}$ $A_2 \times B_2 \times C_2$
Q1	6.6×6.6×0.38	6.6×6.6×0.08	13×13×0.12
Q2	5.4×5.4×0.46	5.4×5.4×0.08	8×8×0.12
Q3	3.6×4.2×0.38	3.6×4.2×0.08	8×11.5×0.12
Q4	3.3×3.3×0.25	3.3×3.3×0.08	5.5×5.5×0.12
Q5	3.2×3.2×0.46	3.2×3.2×0.08	8×11.5×0.15

3 Numerical simulation process

3.1 Constitutive model of solder materials

According to the theory of viscoelasticity, the typical strain rate-stress relationship of the solder is linear at

low stress, and power law creep at middle and high stresses. On the basis of the previous literature [17-18], a hyperbolic sine power constitutive model is adopted, in which the relationship of strain rate with stress is linear at low stress and is hyperbolic sine power at middle and high stresses, as shown in Eq. (1). At each temperature T, there exists a critical stress σ_v (T), which is used to separate the linear and power law creep stages. According to the creep results of two solder materials Sn3Ag0.5Cu and Pb5Sn, the strain rates under various stress levels and temperature-dependent σ_v are determined, as shown in Table 2 [19].

Sn3Ag0.5Cu: $$\dot{\varepsilon}=\begin{cases} A(\sinh B\sigma)^n \exp(-H/RT) & \text{if } \sigma > \sigma_V \\ A_0 \exp(A_1/T)\sigma \exp(-H/RT) & \text{if } \sigma \le \sigma_V \end{cases}$$

Pb5Sn: $$\dot{\varepsilon}=\begin{cases} A(\sinh B\sigma)^n \exp(-H/RT) & \text{if } \sigma > \sigma_V \\ (A_0 - A_2(T-T_R))\sigma \exp(-H/RT) & \text{if } \sigma \le \sigma_V \end{cases} \quad (1)$$

$$\sigma_V = C_0 - C_1(T-T_R) + C_2(T-T_R)^2 \quad (2)$$

where σ is the equivalent stress, σ_v is the linear viscous creep limit, H is the activation energy, R is the universal gas constant, T is the absolute temperature value, and T_R is 273 Kelvin (K).

3.2 FEM analysis and results

The FEM model of the whole chipset is shown in Fig. 3, and the related material constants are shown in Table 3.

Before the power-driven transient thermal analysis, the coefficients of heat transfer are determined by comparison of the temperatures obtained from numerical analysis and measured results in tests. The chipset maintains power on at the first 30 s, then power off. The measured temperature at the center of the bottom surface increases linearly from 21.2 °C to 70 °C within the first 19 s, keeps at 70 °C till 25 s, and decreases linearly from 70 °C to 35.2 °C within 25-44 s, finally maintains at 35.2 °C in the remained times. By adjusting the coefficients of heat transfer in the FEM model until the temperature at the center of the bottom and upper surfaces agree with the measured ones, the actual values of coefficients of heat transfer at the bottom and upper surfaces are finally determined.

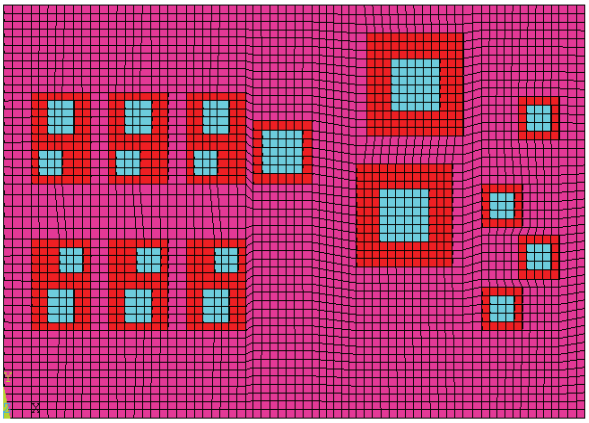


Figure 3: FEM model of the chipset

Table 2: Material parameters and coefficients in Equations (1)-(2)

Eq. (1)	A (s^{-1})	B (MPa^{-1})	n	H/R (K)	A_0 ($MPa\text{-}1.s^{-1}$)	A_1 (MPa)	A_2 (MPa)
Sn3Ag0.5Cu	2.08×106	0.145	5.85	12993	2.039×10-4	8484	—
Pb5Sn	3.16	0.18	4.2	6535	8.168	—	0.0524
Eq. (2)	C_0 (MPa)			C_1 ($MPa.K^{-1}$)		C_2 ($MPa.K^{-2}$)	
Sn3Ag0.5Cu	17.357			0.1219		2.457×10^{-4}	
Pb5Sn	8.0667			0.0017		1.1364×10^{-4}	

Table 3: Material constants in the analysis

Material	Elastic modulus GPa	Poisson's ratio	Coefficient of thermal expansion 10^{-6}/K	Coefficient of heat transfer W/(m.K)	Density kg/m^3	Specific Heat J/(kg.m)
Silicon	187.0	0.25	5.05	150.0	2330	678.262
Pb5Sn	16.1	0.44	29.4	35.2	11160	129.791
Cu	110.0	0.35	16.5	398.0	8960	385.186
SnAg3Cu0.5	41.6	0.36	21.7	64.2	7400	234.461
Cu	110.0	0.35	16.5	398.0	8960	385.186
Insulate layer	5.4	0.34	67.0	4.0	3100	962.964
Al	73.0	0.33	23.6	237.0	2700	900.162
Substrate	0.1	0.36	50.0	0.17	980	1507.25

In the actual power-driven transient thermal analysis, the chipset is repeatedly powered on and off, and both the dwell times are 3 minutes. The transient thermal conduction analysis of the whole chipset is carried out at first, then followed by thermal stress submodel analysis of each chip according to the temperature fields obtained from the thermal conduction analysis of the whole chipset, to get the stress and strain distributions at the solder/substrate interfaces. The boundary conditions in the submodel of each chip are obtained by automatic interpolation of the ANSYS software, as shown in Fig. 4.

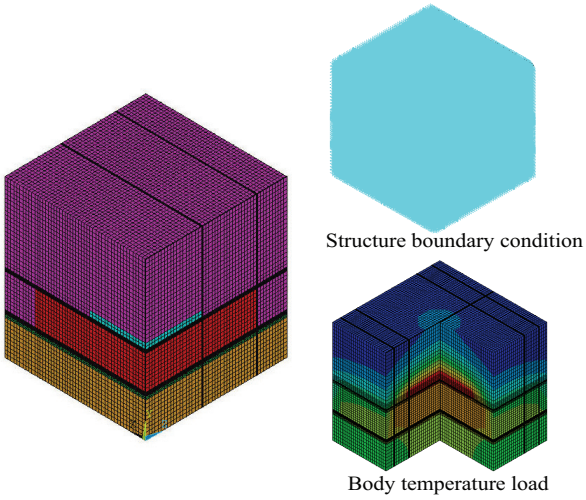


Figure 4: The detailed mesh and boundary conditions of chip Q1

Fig. 5 shows the temperature and strain rate at the center of material 2 (solder Pb5Sn) and 4 (solder Sn3Ag0.5Cu). Due to the shock of power on, high temperature gradient and stress appear in solder Pb5Sn since it is just beneath the power layer. The high stress is presently relaxed because the strain rate reaches a balanced state. After the temperature gets to a saturated state, the strain rate decreases. Because the heat flux is difficult to pass through the thermal insulate layer (material 6) beneath it, the temperature gradient and stress in Sn3Ag0.5Cu solder are very small at the beginning of power on. Therefore, the strain rate at the initial state is very small and gradually increases with the rise of temperature. At the edges around the interface, the heat flux comes from the directions that are not blocked by the thermal insulate layer, as a result, the thermal shock appears. The instant thermal stress and strain distribution in the symmetry plane of chip Q1 at 30 s are shown in Fig. 6, it can be seen obvious stress and strain concentration at the interfacial edge between wafer and Pb5Sn (denoted by E12 in follows), and SnAg3Cu0.5 and Cu (denoted by E45 in follows).

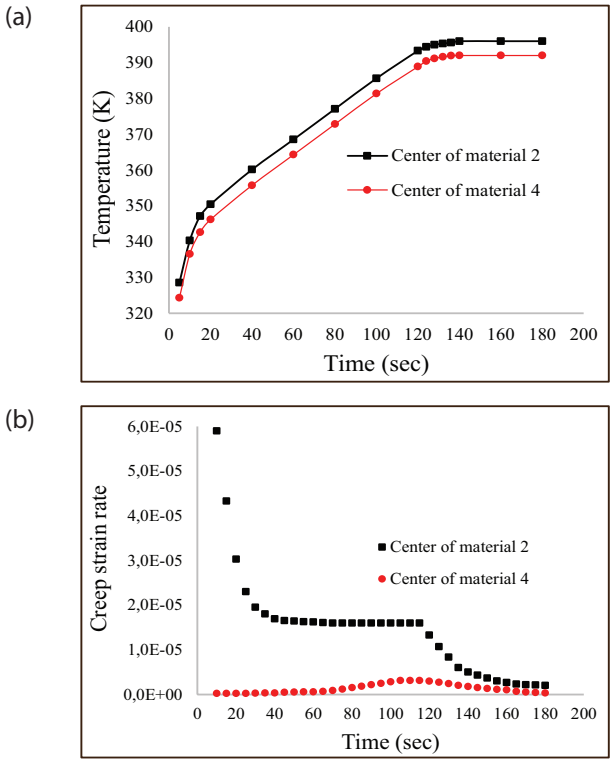


Figure 5: Variations of temperatures and creep strain rates of the solders: (a) temperature, (b) creep strain rate (material 2: Pb5Sn, material 4: Sn3Ag0.5Cu)

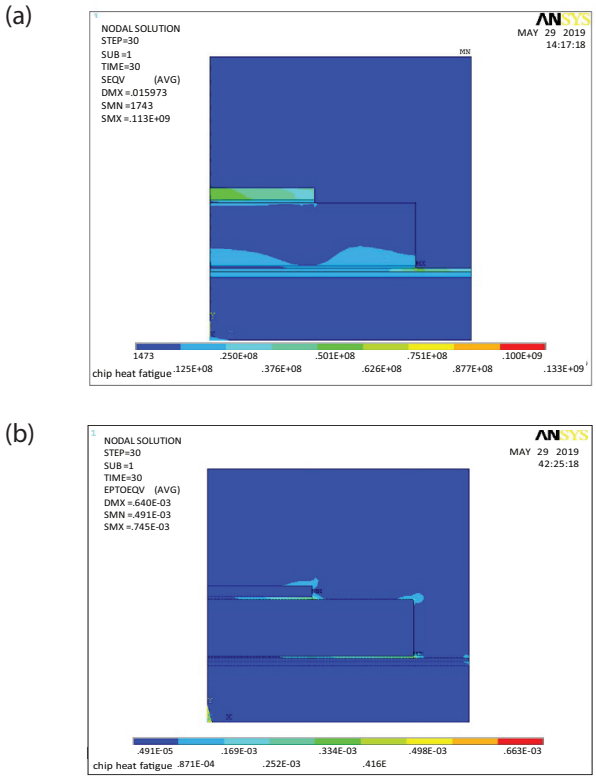


Figure 6: Equivalent stress and strain distribution in the symmetry plane at 30 s: a) stress; b) strain

Fig. 7 shows the equivalent stress distribution in materials 1, 2 and 3 near the interfacial edges. The stress concentration is found at the interfacial edge between materials 1 and 2. Fig. 8 depicts the equivalent strain distribution in materials 3, 4 and 5, and we can also see a severe strain concentration appearing at the interfacial edge between materials 4 and 5. Here the failures of solder joints are mainly concerned, it can be understood from the stress and strain distributions that the failures may occur at the interfacial edges of either E12 or E45. Therefore, the singular stress and strain near these interfacial edges need to be investigated carefully. For this purpose, two data points A and B at E12 and E45 are selected, respectively, as shown in Fig. 9.

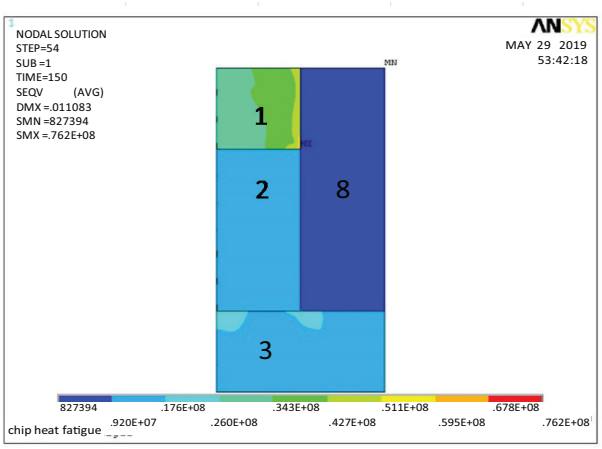


Figure 7: Equivalent stress at 30 s

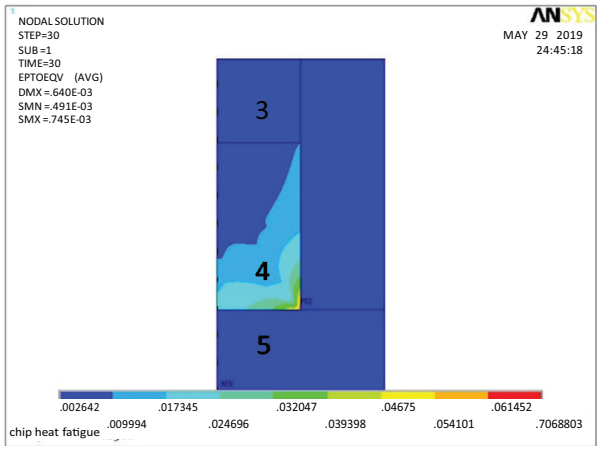


Figure 8: Equivalent creep strain at 30 s

Figs.10 and 11 show the cyclic stress variations of points A and B with power on-off cycles. The severest stress case appears just after power on and finally tends to be steady. Since the normal stress at interface E12 is always compressive, we use the maximum shear stress to define the maximum stress state. Similarly, the maximum traction stress $\sigma_t=(\sigma^2+\tau^2)^{1/2}$ is adopted to

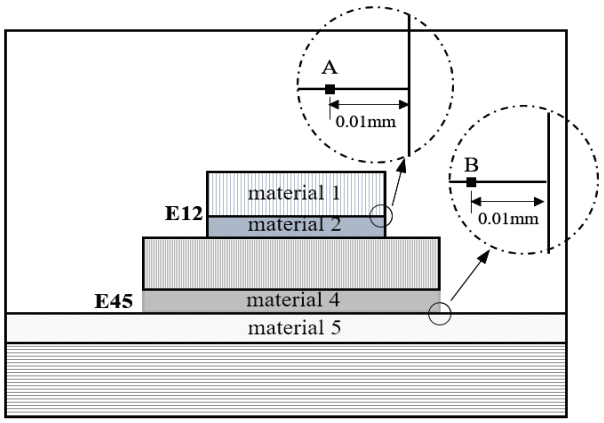


Figure 9: Selected data points A and B

define the maximum stress state because the normal stress at E45 is tensile. Fig.12 presents the cyclic strain variations of points A and B with power on-off cycles, and the maximum strain state appears just at the moment of power off. The maximum creep strain increase with cycle since the creep strain can accumulate.

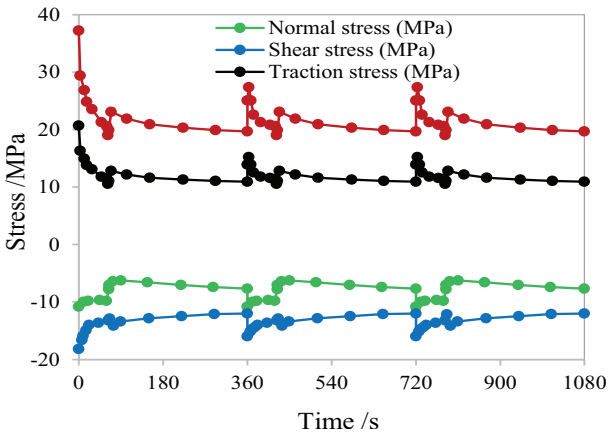


Figure 10: Stress distribution vs time at point A

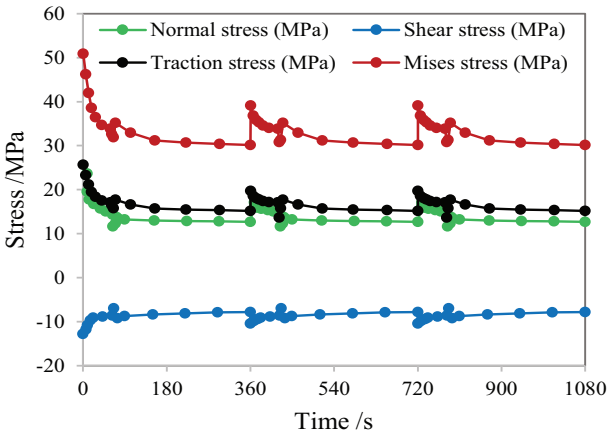


Figure 11: Stress distribution vs time at point B

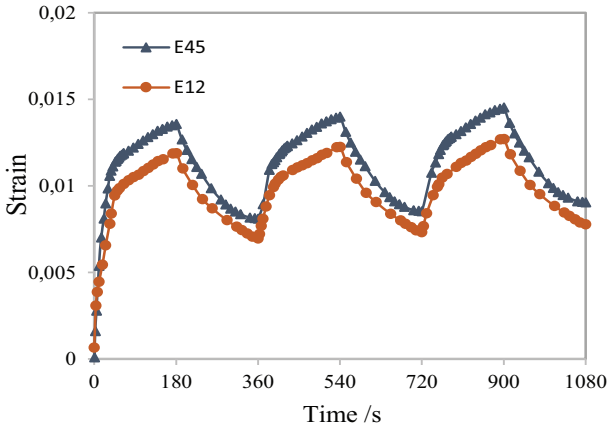


Figure 12: Strain distribution at points A and B

4 Stress-strain singularity and thermal fatigue failure

4.1 Singularity analysis

High stress-strain singularity weakens the connection strength and promotes the crack nucleation from the solder/substrate interface. Therefore, the interfacial singular characteristics, as the key factor affecting the fatigue life, should be discussed in detail. According to the singular field theory, the instant singular stress and strain fields can be expressed as [20]

$$\sigma_i = \frac{K_i(t)}{r^{\delta_i(t)}}, \quad \varepsilon = \frac{K_\varepsilon(t)}{r^{\zeta(t)}} \tag{3}$$

where $K_i(t)$ and $K_\varepsilon(t)$ denote stress and strain intensity factors, $\delta_i(t)$ and $\zeta(t)$ are the stress and strain singular orders, r denotes the distance from the interfacial corner, and i=1, 2 denotes the normal and shear stress, respectively.

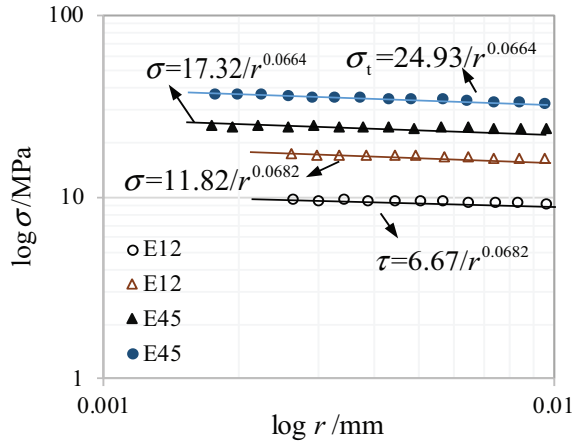


Figure 13: Logarithmic stress distribution

Fig. 13 shows the logarithmic stress distributions along with the distance from the corner at the interfaces E12 and E45. According to the fitting results, the stress intensity factors and singular orders of E12 and E45 are different. Fig. 14 shows the strain distributions at the interfaces E12 and E45, we can see that the singularity of strain is far stronger than that of stress. This fact indicates the strain field may be the dominant factor of failure. The singular orders of stress and strain are different due to the nonlinear constitutive relationships adopted in this analysis.

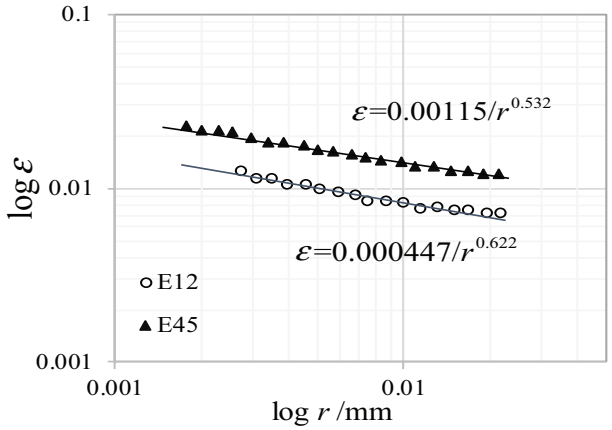


Figure 14: Logarithm strain distribution

The stress and strain singularities of the five types of chips are analyzed by the above method. The stress intensity factors and singular orders at the maximum stress state are shown in Table 4, where K_t is the intensity factor of tensile traction, i.e., $\sigma_t = K_t/r^\delta$. The strain intensity factors and singular orders at the maximum strain state are listed in Table 5. It is noted that the normal stress at E12 is always compressive, so the stress intensity factor K_σ, in this case, has no physical meaning. Since the traction stress combined by the tensile normal stress and shear stress at E45 is the dominant factor for the failure from the interface, it is not necessary to give K_τ separately in this case. Regarding the state before power on as the zero stress-strain states, the stress and strain intensity factors listed in Tables 4 and 5 represent the variation ranges dominating the fatigue failure.

Table 4: Analysis results of the maximum stress field (* CS denotes normal compressive)

Chip Type		Maximum stress state			
		δ	K_t	K_σ	K_τ
		(MPa mm$^\delta$)			
Q1	E12	0.068	11.8	CS	-6.76
	E45	0.067	17.3	24.9	--

Q2	E12	0.112	9.11	CS	-5.21
	E45	0.078	13.3	19.6	--
Q3	E12	0.098	9.93	CS	-5.64
	E45	0.087	12.9	19.2	--
Q4	E12	0.048	13.8	CS	-7.54
	E45	0.098	13.4	18.9	--
Q5	E12	0.120	6.53	CS	-3.64
	E45	0.112	9.94	14.8	--

Table 5: Analysis results of the maximum strain field

Chip Type		Maximum strain state	
		ζ	$K_ζ$ ($mm^ζ$)
Q1	E12	0.622	0.000447
	E45	0.532	0.001150
Q2	E12	0.789	0.000151
	E45	0.687	0.000238
Q3	E12	0.762	0.000138
	E45	0.705	0.000176
Q4	E12	0.745	0.000157
	E45	0.678	0.000163
Q5	E12	0.658	0.000221
	E45	0.784	0.000067

4.2 Power on-off fatigue failure test

Based on the three-dimensional thermomechanical analysis, the interfaces E12 and E45 both undergo a cyclic creep strain during power on-off cycles. To observe the fatigue failure of the microelectronic chip, the cyclic power on-off tests of the chipset are carried out to observe the failure situation. The dwell times of power on-off at the fatigue tests are set as same as that in the FEM analysis. It is found the fatigue failure of the microelectronic chip causes the increase in electronic resistance, so the in-situ resistance measurement is adopted to determine the fatigue failure when the resistance increase exceeds a specific threshold value that followed by 10 % resistance increase [21]. The cutting sections and crack morphologies of the chips are observed by the JSM-6301F scanning electron microscope (SEM) (JEOL, Tokyo, Japan). The samples are covered by carbon before and the analysis is conducted under 20 KeV in the SEI mode. The selected images of chip Q1 and Q5 are shown in Fig. 15. It can be found that there exists a main crack both at the interface E45 (SnAg3Cu0.5/Cu) of chip Q1 and Q5. Many micro cracks are also seen around the main crack, while no crack is observed at E12 (Pb5Sn/wafer). The results from FEM analysis are in good agreement with the test results. Considering the crack nucleation of the failed chips and the results obtained from finite element analysis, it can be drawn that the fatigue failure of the microelectronic chip is attributed to the interaction of singular stress and strain at the interface E45.

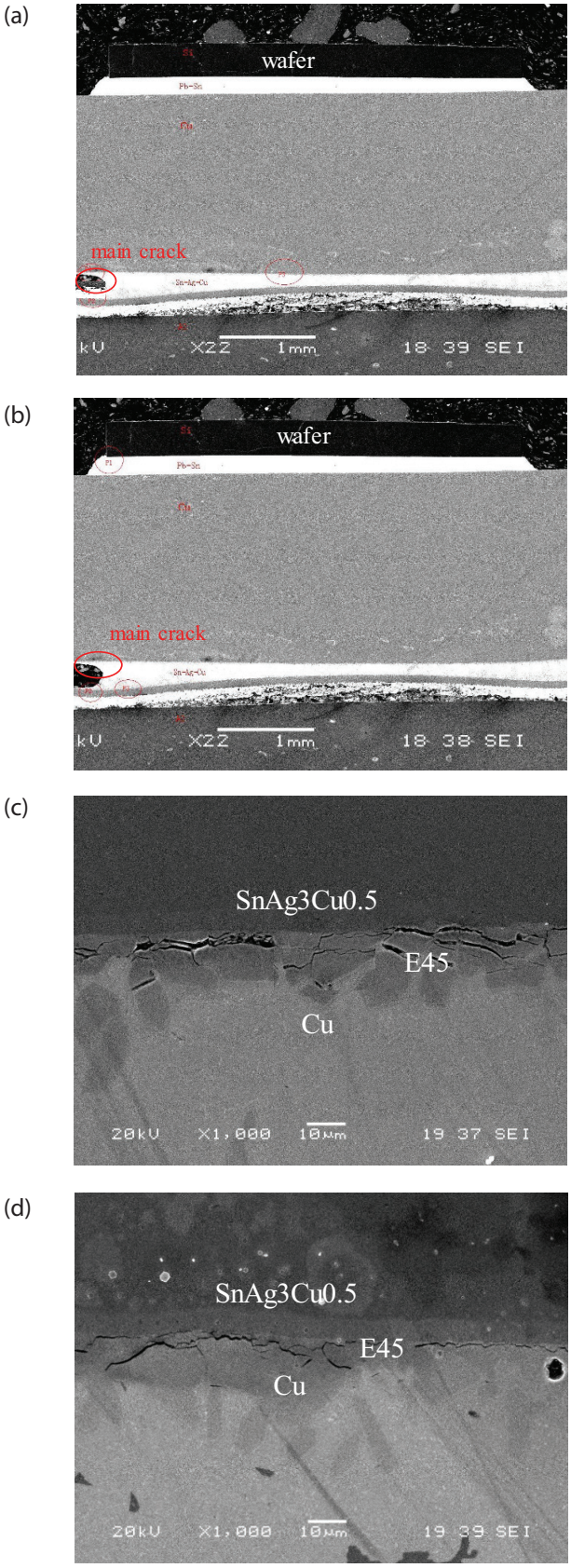


Figure 15: Crack morphology of selected fatigued chip: (a)(c) chip Q1, (b)(d) chip Q5

5 Conclusions

In this paper, we have demonstrated a three-dimensional finite element model that can provide a unique insight into the localized stress and strain concentrations at the solder/substrate interfaces in a microelectronic chip that undergoes power on-off cycles. Based on the calculated stress-strain distributions and singularity parameters, the conclusions are summarized as follows:

The variations of interfacial stress-strain fields are time dependent. The maximum stress appears just after the moment of power on and finally tends to be steady. The creep strain continues to increase after power on and reaches the peak value until power off. The singular order of strain is larger than that of stress, owing to the adopted nonlinear stress-strain relationships of the solders. The stress and strain intensity factors and singular orders at E45 are higher than that at E12, indicating that E45 undergoes a more severe stress-strain fluctuation. From the SEM observation of the fatigued chip, the fatigue crack indeed initiates firstly from E45. The test results are in good agreement with that from the FEM analysis, and the fatigue failure of the microelectronic chip is mutually controlled by the singular stress and strain at the SnAg3Cu0.5/Cu interface.

6 Acknowledgements

This research work was supported by the National Natural Science Foundation of China (No. 51404286), and the Fundamental Research Funds for the Central Universities of China (No. 17CX02065). The author is also grateful for the financial support from China Scholarship Council (No. 201806455016).

7 References

1. QS Zhu, F Gao, HC Ma, ZQ Liu, JD Guo, L Zhang. Failure behavior of flip chip solder joint under coupling condition of thermal cycling and electrical current. Journal of Materials Science: Materials in Electronics, 2018, 29(6): 5025-5033. https://doi.org/10.1007/s10854-017-8464-3.
2. P Yang, W Li. Numerical analysis on thermal characteristics for chip scale package by integrating 2D/3D models. International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, 2009, 22: 43-55. https://doi.org/10.1002/jnm.694.
3. MY Xiong, L Zhang. Interface reaction and intermetallic compound growth behavior of Sn-Ag-Cu lead-free solder joints on different substrates in electronic packaging. Journal of Materials Science, 2019, 54: 1741-1768. https://doi.org/10.1007/s10853-018-2907-y.
4. AT Tan, AW Tan, F Yusof. Influence of nanoparticle addition on the formation and growth of intermetallic compounds (IMCs) in Cu/Sn-Ag-Cu/Cu solder joint during different thermal conditions. Science and Technology of Advanced Materials, 2015, 16(3): 033505. https://doi.org/10.1088/1468-6996/16/3/033505.
5. T Xu, XW Hu, YL Li, XX Jiang. The growth behavior of interfacial intermetallic compound between Sn-3.5Ag-0.5 Cu solder and Cu substrate under different thermal-aged conditions. Journal of Materials Science: Materials in Electronics, 2017, 28(24): 18515-18528. https://doi.org/10.1007/s10854-017-7799-0.
6. M Yang, M Li, J Kim. Texture evolution and its effects on growth of intermetallic compounds formed at eutectic Sn37Pb/Cu interface during solid-state aging. Intermetallics, 2012, 31:177-185. https://doi.org/10.1016/j.intermet.2012.07.004.
7. M Erinc, PJG Schreurs, MGD Geers. Integrated numerical-experimental analysis of interfacial fatigue fracture in SnAgCu solder joints. International Journal of Solids and Structures, 2007, 44: 5680-5694. https://doi.org/10.1016/j.ijsolstr.2007.01.021.
8. SP Zhu, HZ Huang, LP He, Y Liu, ZL Wang. A generalized energy-based fatigue-creep damage parameters for life prediction of turbine disk alloys. Engineering Fracture Mechanics, 2012, 90: 89-100. https://doi.org/10.1016/j.engfracmech.2012.04.021.
9. AR Akisanya, CS Meng. Initiation of fracture at the interface corner of bi-material joints. Journal of the Mechanics and Physics of Solids, 2003, 51: 27-46. https://doi.org/10.1016/s0022-5096(02)00076-5.
10. HR Ghorbani, JK Spelt. Analytical elasto-creep model of interfacial thermal stresses and strains in trilayer assemblies. International Journal of Solids and Structures, 2006, 43: 7424-7449. https://doi.org/10.1016/j.ijsolstr.2006.02.003.
11. SS Pageau, PF Joseph, SB Biggers. Finite element analysis of anisotropic materials with singular in-plane stress fields. International Journal of Solids and Structures, 1995, 32(5): 571-591. https://doi.org/10.1016/0020-7683(94)00152-m.
12. DH Chen, K Ushijima. Plastic stress singularity near the tip of a V-notch. International Journal of Fracture, 2000, 106: 117-134. https://doi.org/10.1023/a:1007693716844.

13. T Hattori, S Sakata, G Murakami. A stress singularity parameter approach for evaluating the interfacial reliability of plastic encapsulated LSI devices. Journal of Electronic Packaging, 1989, 111: 243-248. https://doi.org/10.1115/1.3226542.
14. PA Gradin. A fracture criterion for edge-bonded bimaterial bodies. Journal of Composite Materials, 1982, 16: 448-456. https://doi.org/10.1177/002199838201600601
15. HL Groth. Stress singularities and fracture at interface corners in bonded joints. International Journal of Adhesion and Adhesives, 1988, 8: 107-113. https://doi.org/10.1016/0143-7496(88)90031-0.
16. ED Reedy Jr, TR Guess. Comparison of butt tensile strength data with interface corner stress intensity factor prediction. International Journal of Solids and Structures, 1993, 30(21): 2929-2936. https://doi.org/10.1016/0020-7683(93)90204-k.
17. S Wiese, E Meusel. Characterization of lead-free solders in flip chip joints. Journal of Electronic Packaging, 2003, 125(4): 531-538. https://doi.org/10.1115/1.1604155.
18. JW Kim, DG Kim, SB Jung. Evaluation of displacement rate effect in shear test of Sn-3Ag-0.5Cu solder bump for flip chip application. Microelectronics Reliability, 2006, 46: 535-542. https://doi.org/10.1016/j.microrel.2005.06.008.
19. JH Liu, XQ Meng, JQ Xu. Creep constitutive relationship and cyclic behavior of Sn96.5Ag3Cu0.5 under high temperature. International Journal of Modern Physics B, 2008, 22(2): 5438-5444. https://doi.org/10.1142/s0217979208050620.
20. H Koguchi, N Suzuki. Singular stress fields in anisotropic bonded joints considering interface stress and interface elasticity. Journal of Applied Mechanics, 2014, 81(7): 1003-1012. https://doi.org/10.1115/1.4026840.
21. AR Syed. Accumulated creep strain and energy density based thermal fatigue life prediction models for SnAgCu solder joints. Proceeding of the 54th Electronic Components and Technology Conference, 2004, 737-746. https://doi.org/10.1109/ectc.2004.1319419.

Arrived: 08. 04. 2019
Accepted: 17. 06. 2019

https://doi.org/10.33180/InfMIDEM2019.204

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 49, No. 2(2019), 79 – 90

Implementation of a Digital TRNG Using Jitter Based Multiple Entropy Source on FPGA

Ali Murat Garipcan, Ebubekir Erdem

Firat University, Department of Computer Engineering, Elazig, Turkey

Abstract: In this study, hardware implementation and evaluation of a true random number generator (TRNG) is presented. For the implementation, Field Programmable Gate Array (FPGA) hardware, in which numerical processes based on an algorithmic basis are carried out, was used. In the system, ring oscillators (ROs) with similar structures were used as a noise source, and true randomness was obtained by sampling the jitter signals originating from the oscillators. However, the most critical cryptographic disadvantage of jitter-based TRNGs is the statistical inadequacy of the system. At this point, in contrast to existing designs, entropy sources derived from the subsets of ROs were used in the sampling and post-processing stage. The statistical quality of the system was improved by using true random numbers/inputs obtained from these entropy sources in the sampling and post-processing stage. With sampling and post-processing inputs, the use of complex post-processing techniques that limit the output bit rate of the generator in the system was not required. Thus, a high-performance adaptable TRNG model with reduced hardware resource consumption is obtained. The statistical validation of the TRNG, which was tested in 6 different scenarios for two separate ring oscillator (RO) architectures and three different operating frequencies, was performed with the NIST 800-22 and AIS31 test packages.

Keywords: Jitter; oscillator rings; FPGA; true random number generators; cryptography.

Uporaba digitalne TRNG na FPGA z uporabo več entropijskih virov na osnovi tresenja

Izvleček: V prispevku je obravavana strojna oprema in ocenitev pravega generatorja naključnih števil (TRNG). Izvedba je bila narejena na FPGA strojni opremi. Za vir šuma je bil uporabljen krožni oscillator, naključnost pa je zagotovljena s tresenjem originalnega signal oscilatorjev. Kriptografska slabost TRNG na osnovi tresenja je njihova statstična nezadostnost. V nasprotju z obstoječimi sistemi so za reševanje tega problema uporabljeni entropijski viri RO v fazi vzorčenja in naknjanje stopnje obdelave. Statistična kvaliteta je bila z uporabo pravih naključnih števil iz entropijskih virov močno izboljšana in to brez uporabe kompleksnih tehnik naknadnega procesiranja. Validacija šestih scenarijev in dveh RO je bila opravljena na testnih paketih NIST 800-22 in AIS31.

Ključne besede: tresenje; krožni oscilator; FPGA; generatov naključnih števil; kriptografija

** Corresponding Author's e-mail: agaripcan6223@gmail.com*

1 Introduction

In computer science, random numbers are used in many different fields such as programming, simulation, statistical sampling, chance games, and cryptography. While simple statistical features are often sufficient, random numbers must meet strict requirements when it comes to cryptography because the understanding of security in cryptographic systems is based on the confidentiality of randomly generated numbers used for performing critical functions in the system. In addition to their excellent statistical properties, random numbers, which are the complementary element of cryptographic systems, should not contain hidden or explicit patterns between their elements and should be unpredictable. Random numbers, which do not meet these characteristic requirements, jeopardize the reliability of cryptographic systems in which they are used.

Generation of random numbers, which provide the characteristic requirements needed in cryptography, forms an essential and challenging problem area [1]. For obtaining these numbers, customized components known as the Random Number Generators (RNGs) are needed. Random numbers are obtained from two separate design classes: PRNG (pseudo RNG) and TRNG

(true RNG). A TRNG is a mechanism that generates true random numbers which are difficult to predict and impossible to reproduce, by using physical events/situations as an entropy source. A TRNG design architecture is presented in Figure 1 consists of the noise source, sampler, and post-processing hierarchical components. The uncontrollability of the physical processes used as the noise source makes the outputs of the generator unpredictable and unreproducible. Pure random numbers with a poor statistical quality obtained by the digitalization of noise sources in the system are post-processed and passed to the output.

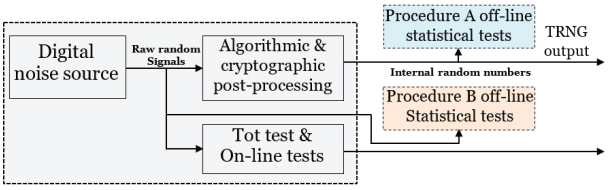


Figure 1: Overall design architecture of a true RNG.

The overall design architecture and characteristic behavior of any RNG should coincide with the ideal definition of cryptographic random numbers. In contrast to TRNGs, the PRNG, which corresponds to a standard definition, is a deterministic function. Although their quality of randomness is good, the fact that their outputs appear to be random, yet are predictable limits the use of PRNGs in sensitive cryptographic applications. Although TRNGs are usually slow, costly, and hardware-dependent, they are frequently preferred since they can meet cryptographic requirements.

Random numbers should not be generated on uncontrolled hardware and should not be taken out of the system. If possible, cryptographic systems should be implemented as a whole in a secure computing zone where direct access and programming are not possible on embedded systems [2, 3]. Therefore, the implementation of random number generators is critical. Non-deterministic events/situations on these devices, in which algorithmic processes are performed at the hardware level, adversely affect the behavior of the system. Although non-deterministic processes are minimized by device manufacturers, they cannot be completely eliminated. This situation demonstrates that randomness/noise sources, which are the most critical design components of a TRNG, can be obtained from these devices. Jitter [4-5] and metastability [6-7] on FPGA are frequently used randomness sources, for TRNG designs based on digital design techniques. Especially ROs are used as a source of jitter signals. The clock signals obtained from ROs occur with a deviation from the ideal positions because of the unstable propagation delay in the delay chain. The fact that jitter signals are truly random and easily obtainable has made ROs an important component of TRNGs [8].

In this study, the hardware implementation and evaluation of a TRNG on an FPGA in which ROs were used as the source of noise/randomness are presented. In contrast to the studies in the literature, additional sources of true randomness are used for triggering signal sampling and as an additional input for the post-processing components of the system. In addition to improving the statistical quality of the system, the way in which the entropy sources for additional inputs are implemented further simplifies the system in terms of hardware. Besides to simplifying the system and improving its statistical quality, additional inputs have also eliminated the necessity of complicated post-processing techniques that limit the output bit rate. Therefore, the output bit rate of TRNG is high, although the sampling input is non-periodic. Furthermore, the fact that the additional inputs used in the hierarchical components of the system are truly random made the system cryptographically secure.

The remaining part of the study is organized as follows: Developments in the literature are presented in Section II. In addition to the architectures of the used RO, the conceptual infrastructure of the proposed system is displayed in Section III. Detailed information about the hardware implementation of TRNGs and the results of the experimental analysis are presented in Sections IV and V, respectively. Finally, the study is terminated by presenting the conclusion and recommendations in Section VI.

2 Related works

In cryptography, implementation of an RNG, which is the most important component of the system, in a computation zone where access and manipulation are not possible, is essential regarding the security of the system. Again, the possible attacks on the principles representing the generator and the sub-components of the generator can change the constant theoretical safety limit of TRNGs over time. This causes analytic attacks to occur on the cryptographic system in which the generator is used in a shorter time than expected. By keeping the theoretical safety limit constant, the ability to re-configure implementation platforms to minimize the impact of possible attacks is another important step in system security. For providing these basic requirements, FPGA hardware, in which cryptosystems can be applied as a whole, is a popular platform. Therefore, obtaining the noise source, which is the most critical design component of a TRNG, on these devices is a desired feature [9, 10].

Noise sources such as jitter, metastability, and clock jitter, which mostly emerge as a result of the use of digital devices such as FPGA, are inefficient in terms of cryptographic competencies [11]. In the literature, there are many TRNG designs in which these randomness sources are used. The focus of the designs is to improve the basic design parameters and cryptographic competencies of the generator, as in this study. Some of these studies are as follows:

Phase-Locked Loop (PLL) [4], [12] and multi-ROs [13-14] are used to obtain jitter on digital devices. In [13], 114 free-running ROs, each consisting of 13 inverters, were used in the system. The sampling frequency and output bit rate of the system, in which resilient functions are used as the post-processing technique, are 40 MHz and 2 Mbps, respectively. Due to the complexity of the system, the energy consumption is high, and the output bit rate is low. An improved version of the model proposed by Sunar was proposed by Knuth in [14]. Post-processing was not required in the system, in which the number of inverters and free oscillation ROs was reduced. The most significant deficiency of the system proposed by Wold in [11] was that the generator became insecure due to the entropy loss caused by the reduction of the number of oscillators in the system and occurrence of deterministic randomness. In another study [15], in which the model of Sunar was referenced, a total of 110 free oscillation oscillators each comprising 3 inverters were used in the system. The output bit rate of the system implemented on the Xilinx Virtex II Pro FPGA was measured to be 2.5 Mbs. Other TRNG designs using ROs were also proposed by Kollhenberger and Gaj [16], Golic [17], Dichtl and Golic [18], Tuncer [19], and Avaroglu [8].

In the literature, ROs, in which jitter represents the source of randomness, are also used in Physically Unclonable Function (PUF) based TRNG designs [20-21]. In [20], for two separate PUF circuits in the system, 64 ROs, each consisting of 13 inverters, were used. Random numbers obtained from the RO-PUF (Ring Oscillator-Physically Unclonable Function) implemented on two different FPGA cores against the same query were passed through the post-processing technique, and successful results were obtained. In [21], the query input of the PUF circuit with 128 ROs, each consisting of 3 inverters, was obtained from the logistic map with chaotic behavior. In [4] and [12], instead of ROs, jitter signals obtained by the numerical implementation of analog PLL components were used. The most significant disadvantage of both systems is that a limited number of PLL components can be used on digital devices and a limited number of outputs can be obtained from these components.

A hard-core TRNG design in which the R-S flip-flop is used as a metastability-based source of randomness was presented in [22]. In the system in which the NAND gates of the R-S latch are applied as LUT (look-up table), the outputs of 64, 128, 256 parallelly connected R-S latches were sampled by combining them with the XOR (exclusive OR) operation. The TRNG which did not need post-processing passed NIST tests successfully. Another metastability-based TRNG design was presented in [23]. The system, in which cross-linked NAND gates were used as a source of metastability, was implemented on the Xilinx Virtex XC5VLX50T FPGA chip. The system that reached an output bit rate of 30 Mbps by using the Von Neumann and XOR post-processing techniques passed the NIST tests successfully.

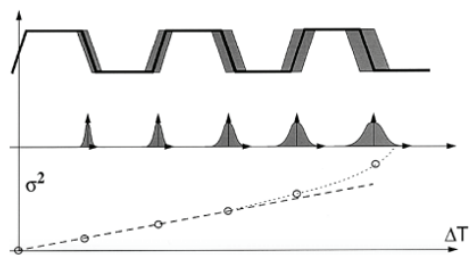
3 Generic architecture of the proposed TRNG

Within the FPGA, each of the digital circuit elements that make up the integrated structure has its own specific unstable time delay. This instability can also be observed on closed or open loop combinational structures, such as ROs, which are used for generating clock signals and which consist of a certain number of delay elements. The temporal deviations caused by the propagation delay occurring on the inverters of the RO cause a period irregularity (jitter) in clock signals [2]. The amount of this irregularity is one of the most important performance metrics of TRNGs and directly affects the quality of the generated random numbers. The jitter occurs in two different ways as deterministic and random. The random jitter which is unpredictable for any sampling time is usually expressed with the Gaussian distribution presented in Equation 1. The jitter occurs as a natural result of flicker, shot and thermal noise which depend on the generation and operating conditions of the logic circuit elements. Periodic irregularity and uncertainty occurring in clock signals due to jitter increases over time as depicted in Figure 2 (a) [2, 9, 19].

$$J_{RJ}(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\left(\frac{x^2}{2\sigma^2}\right)} \quad (1)$$

The RO (Figure 2 (b)) is a combinational structure in which an odd number of inverters is sequentially connected forming a delay chain. In addition to their simple combinational definitions, free oscillation ROs have a structure that is easy to implement on digital devices. Therefore, they are frequently used in TRNG designs for obtaining jitter signals.

(a)



(b)

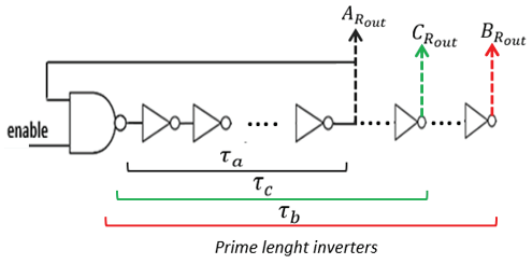


Figure 2: (a) Occurrence of jitter and its time-dependent change, **(b)** combinational structure of the ring oscillator.

The fundamental characteristic of the jitter occurring on ROs is as follows [3, 13]:
The RO-based architecture used as the true randomness source of TRNG is depicted in Figure 3. In the system, $(f_{i1}, f_{i2} \ldots . f_{iN})$ N denotes the number of ROs, and f_i is the ideal square wave signal obtained at each oscillator output. The average period of the f_i signal at any oscillator output T_0 is given by Equation 2, where n is the number of inverters and τ is the delay of a single inverter. The periodic nature of f_i is given by Equation 3.

$$T_0 = 2n\tau \tag{2}$$

$$f_i(t) = f_i(t + T_0) \tag{3}$$

However, f_i signals at the oscillator outputs are not in an ideal form due to the instability of the delay occurring on the inverters. In the system in which this unstable delay is represented by $T_{GAUSS,}$ the actual period of the oscillator output signal f_i is given by Equation 4. $T_{GAUSS,}$ which represents the jitter, is the random variable of the system and can take values from $(-T_0/2, T_0/2)$ for any time t. The true randomness of TRNGs required in terms of cryptography is based on the jitter's Gaussian distribution in Equation 1 [3].

$$f_i(t) = f_i(t + T_0 + T_{GAUSS}) \tag{4}$$

The generic design architecture of the system proposed within the scope of the study is depicted in Figure 3. System consists of three separate oscillator-based hierarchical true randomness sources used for sampling and post-processing inputs together with the noise source. In the system, two separate RO scenarios, taken from [8, 13] consisting of 3 and 13 inverters, respectively, were tested as noise/entropy source. These oscillator scenarios are represented by the block structure in Figure 3 (A). The block structures in Figure 3 (B) and 3 (C) are other entropy sources obtained with a minimum design cost from the noise source of the generator. True random signals obtained from these entropy sources are used as sampling and post-processing inputs of TRNG in the system.

The operation logic of the system can be briefly described as follows: The RO outputs of each entropy source combined with XOR process were sampled through D-type flip-flops to obtain f_s, f_p, and f_k true random outputs. In the system, the non-periodic f_s signal is obtained by sampling from the entropy source in Figure 3 (B). Three different clock signals with a frequency of 50, 100 and 200 MHz are used for sampling. For each sampling scenario, the f_s signal is used as the non-periodic sampling input of the other oscillator clusters and f_p and f_k true random outputs are obtained. In the system, f_k and f_p are obtained from the entropy sources in Figure 3 (A) and (C), respectively, and are raw true random numbers with poor statistical quality. True random outputs of TRNG are obtained by XORing the bit leve f_p and f_k outputs generated in the system at equal times depending on the state of f_s, as in Figure 3 (D).

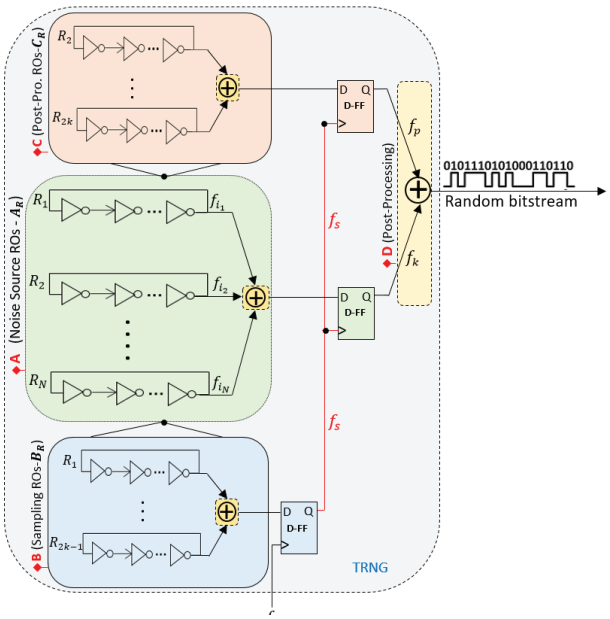


Figure 3: The generic architecture of the proposed system.

The design details of TRNG's oscillator-based entropy sources can be explained as follows. In Figure 3 (A), with the oscillator cluster representing the block structure (noise source) $A_R = \{R_1, R_2, R_3 \ldots . R_{114}\}$ and $1 \leq k \leq 57$. The selection of other RO clusters representing the other block structures of Figures 3 (B) and (C) from this cluster

are formed as follows: The RO cluster selected for the sampling frequency (f_s) in Figure 3 (B) is $B_R = \{R_1, R_3, R_5, \ldots R_{2k-1}\}$, and the RO cluster selected for the post-processing input (f_p) in Figure 3 (C) is $C_R = \{R_2, R_4, R_6, \ldots R_{2k}\}$. The use of free-running ROs in the TRNG design was proposed by Sunar in [13]. In the proposed system, it was assumed that the ROs are independent. References [2] and [11] indicate that dependency (also described as phase locking) occurs in 25% of ROs that are supposed to be independent. This caused a loss of entropy in the system. In order to minimize the possible loss of entropy due to this dependence, B_R and C_R oscillator clusters from which additional inputs were obtained were uniformly spread across the whole set of A_R oscillators.

The oscillators in Figure 3 (B) and (C) were converted into a semi-open cycle combinational structure in Figure 2 (a) defined on the noise source, to reduce the energy consumption associated with the system's hardware resource demand. A certain number of the inverters of semi-open cyclical structures are defined on the noise source oscillators, and the oscillation continuity is provided by the feedback loop of these oscillators. In the system, the delay chain of any closed or semi-open cycle RO consists of an odd number of inverters. Therefore, inverters used additionally for semi-open cyclical structures will not change the oscillator outputs at the logic level. However, they will randomly modify the time-dependent periodic irregularity of the output signals. At this point, the basic idea is to increase true randomness time-dependently by making the random behavior of ROs as different as possible from each other and the noise source.

The relationship between the prime number of inverters in a RO and randomness is explained in [13]. Attention was paid to this relationship when increasing the number of inverters. Let τ_a, τ_b and τ_c denote the number of inverters (which must be prime). Then $\tau_c = \tau_a + p$, $\tau_b = \tau_c + k$, and $k \geq p$ (see Figure 2 (a)). In order to minimize the power consumption of ROs in the system, values of k and p were kept at a minimum.

4 Hardware implementation

TRNG scenarios were created with dataflow and schematic design techniques on the Quartus II implementation development platform. In order to measure the real-time performance of the system, the Altera EP-C4GX150 FPGA development board was used during

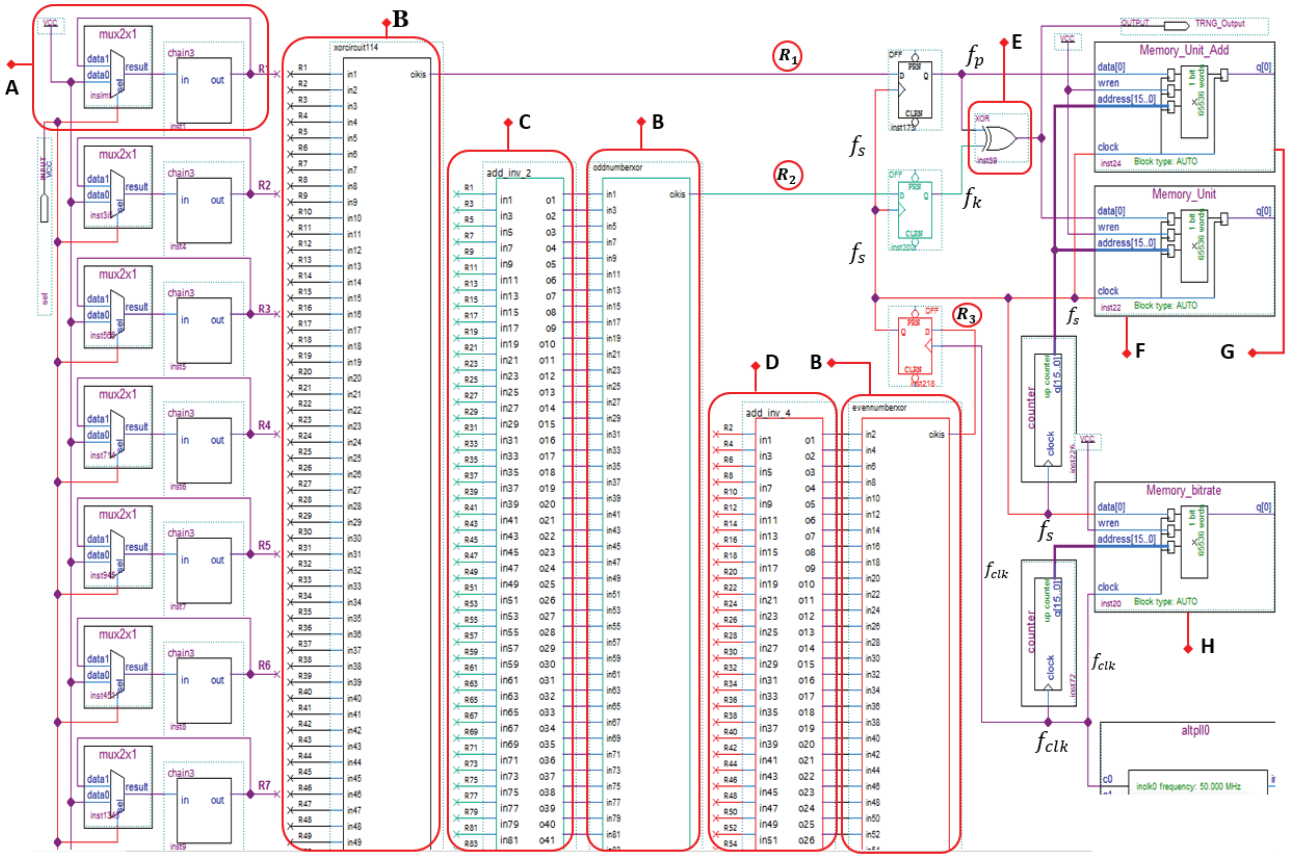


Figure 4: Hardware modeling of the TRNG for a (114,13) scenario

the implementation stage. The overall structure of the proposed system is presented in Figure 3. In the system, two separate RO architectures (114,3) and (114,13) were used as noise sources. The TRNG was tested in six different scenarios for two different noise source architectures and three different operating frequencies. Entropy sources were obtained by modifying the design parameters of these architectures.

The hardware implementation of a TRNG for the (114,3) oscillator architecture is depicted in Figure 4. Figure 4 (A) is the core oscillator structure which is used as the noise source of the TRNG and that consists of three inverters. 2x1 mux was used as the control variable of the oscillator (Figure 2 (a)). The oscillator output is obtained by applying the output of the mux to the input of the block structure containing the inverters forming the delay chain of the oscillator. The data0 and data1 pins of the mux are the enable and feedback inputs, respectively. The selection pin (sel) of the mux is an excitation signal obtained from the physical environment. For the logic '0' value of the selection pin, the oscillator outputs are constant. For the logic '1' state, the RO is in the feedback position, and the outputs oscillate. The noise source is formed by connecting 114 core structures in parallel. For synchronization of the system, the data0 and sel pins of the muxs at the input of the ring oscillators are common and the data0 pin is connected to the + VCC. In the system, by combining the high oscillating RO outputs, which were used for the noise/randomness source, post-processing input, and sampling operation, with the XOR operation (Figure 4 (B)), R1, R2, and R3 outputs were obtained. Unlike Reference [13] in which a fixed sampling frequency was used, R1 and R2 outputs were sampled with truly random signals (f_s) obtained from R_3.

In Figure 4, R_1, R_2, and R_3 are the combined RO outputs. The oscillator architecture was used for obtaining the combined oscillator outputs R_2 and R_3. Even-numbered outputs of the (114,3) ROs, the noise source, were used for the output R_3 while odd-numbered outputs were used for the output R_2. Before they were obtained, the high oscillation R_2 and R_3 outputs were combined with the XOR operation after they were passed through the block structure as depicted in Figure 4 (C) and (D). In Figure 4 (C), as a result of passing each single oscillator output through two extra inverters, the RO cluster with the (57,5) R_2 post-processing input was obtained. In Figure 4 (D), the oscillator cluster, in which (57,7) R_3 non-periodic sampling signals were attained by using four extra inverters, was obtained. The true random numbers/signals (f_s) in Figure 4 (E) used for sampling the outputs R_1 and R_2 in the system were obtained from the output R_3. For this purpose, the output R_3 was sampled with the help of a type D flip-flop at three different frequencies of 50, 100 and 200 MHz obtained from the PLL for each scenario. The obtained true random numbers and the true random outputs obtained by a synchronized sampling of R1 and R2 outputs were combined with the XOR operation in Figure 4 (E), and the outputs of the TRNG were obtained. The simulation results of the random numbers obtained from the system for the 50 MHz sampling frequency are as shown in Figure 5 (a). The real-time experimental setup of the TRNG in which real-time results are obtained and the real-time variation of the bits produced are depicted in Figures 5 (a) and 5 (b).

(a)

(b)

(c)

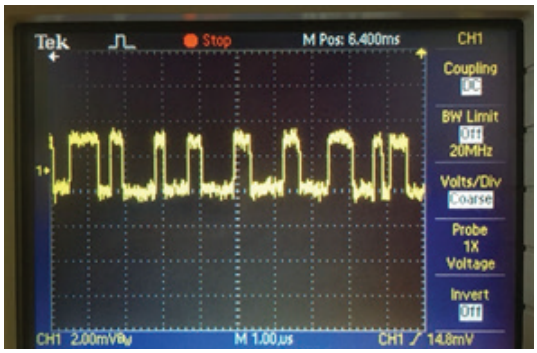


Figure 5: (a) Simulation results**, (b) r**eal-time experimental setup of a TRNG**, (c)** random numbers generated in real time.

In order to measure the statistical adequacy of TRNG, two separate test techniques with different application methods were used. Therefore, two different embedded memory components, such as in Figure 4 (F) and (G), were used to obtain suitable random numbers to each test technique from TRNG. Raw true random numbers (digital noise) sampled from the noise source and post-processed (internal) random numbers were recorded to the memory components, respectively. The width of the memory components using the 16-bit up counter for addressing is 1 bit, and depth is 65536 bits.

Therefore, the sample length of each random number sequence obtained for statistical verification from the TRNG is 65536 bits.

In Figure 4, the non-periodic sampling input (f_s) was used at the same time as the clock signal of the counter circuit and memory component. Thus, truly random numbers at the bit level sampled at equal times in the system are simultaneously recorded the memory cells indicated by the counter. The other embedded memory architecture given in Figure 4 (H) is used to measure the output bit rate of the TRNG. Unlike other memory architectures, the periodic sampling input (f_{clk}) is used as the clock signal of the counter and memory component. Thus, the non-periodic f_s signal is also recorded to the memory component in Figure 4 for output bit rate analysis of TRNG.

5 Experimental results

Cryptographically, one of the most important design evaluation criteria of any TRNG is the process of statistical verification of randomness. This process is essential for the security of TRNGs based on physical noise sources. To what extent the robust randomness criteria are met should be measured by the statistical test tools. There are different test groups developed for the evaluation of randomness. There are different test groups, such as FIPS140, Diehard, Crypt-X, NIST, AIS31, and TestU01 developed to evaluate randomness for TRNGs. However, in the scope of the study, two different hypothesis-based test techniques which has high validity and compelling structure compared to other test groups such as NIST 800-22 and AIS31 were used for statistical verification of TRNG.

Table 1: NIST 800-22 statistical test results

Test Criteria	Stage I		Stage II (sampling true rand. num.)						Stage III (with additional inputs)					
	(114,3)	(114,13)	(114,3)			(114,13)			(114,3)			(114,13)		
	50 MHz	50 MHz	50 MHz	100 MHz	200 MHz	50 MHz	100 MHz	200 MHz	50 MHz	100 MHz	200 MHz	50 MHz	100 MHz	200 MHz
Frequency test	-	-	-	-	-	-	-	-	0.302	0.020	0.576	0.932	0.331	0.403
Frequency test with a block	-	-	-	-	-	-	0.147	0.207	0.077	0.657	0.972	0.515	0.263	0.899
Run test	-	-	-	-	-	-	-	-	0.709	0.0357	0.912	0.112	0.193	0.203
Test for the longest run of ones in a block	-	-	-	-	-	0.019	0.592	0.547	0.668	0.022	0.716	0.256	0.791	0.715
Binary matrix rank	0.457	0.232	0.222	0.621	0.410	0.849	0.602	0.058	0.599	0.917	0.599	0.496	0.308	0.208
Discrete Fourier transform	0.169	-	0.703	0.291	0.561	0.709	0.846	0.630	0.897	0.460	0.818	0.875	0.869	0.962
Non-Overlapping template	-	-	0.894	0.871	0.511	0.200	0.302	0.174	0.825	0.505	0.803	0.725	0.209	0.701
The overlapping template	0.420	0.157	0.222	0.335	0.321	-	0.445	0.056	0.788	0.498	0.055	0.918	0.731	0.394
Universal test	-	0.012	0.039	-	-	0.750	0.015	-	0.813	0.892	0.633	0.564	0.052	0.955
Linear complexity	-	-	0.303	0.540	-	0.837	0.387	0.884	0.866	0.976	0.776	0.506	0.260	0.901
Serial test	-	-	-	-	0.032	0.382	0.423	0.783	0.661	0.812	0.738	0.676	0.344	0.228
	0.219	0.041	0.114	0.545	0.941	0.758	0.613	0.821	0.825	0.980	0.662	0.928	0.667	0.054
Approximate entropy	-	-	-	-	-	-	-	-	0.419	0.451	0.842	0.447	0.165	0.229
Cumulative sums	-	-	-	-	-	-	-	-	0.329	0.292	0.097	0.586	0.139	0.518

The NIST 800-22 test suite consists of 15 different sub-test criteria. The *p-value* (probability value), which corresponds to the randomness probability of the number sequence subjected to the test for each sub-test criterion, is measured. This value is expected to be absolutely greater than parameter *a*, which changes according to the typical importance level [0.001-0.01] of cryptographic applications, for each test criterion [1, 8]. Statistical validation for a random number sequence for any test criterion where this condition is not met is considered to be unsuccessful.

The real-time test setup, in which statistical results were obtained for NIST 800-22, is presented in Figure 5. The test technique was applied in three stages in order to observe the effect of additional true random inputs on statistical results in the system. In the first stage, the combined outputs of the (114,3) and (114,13) ROs were sampled independently with 50, 100 and 200 MHz clock signals. Then, the sampling process was repeated with true random signals/numbers, and the effect of the sampling input on statistical results was observed. In this stage in which partial statistical success was achieved, the successful results presented in Table 1 were obtained by including the post-processing input in the system.

AIS31 test proposed by BSI (German Federal Office for Information Security) was used another statistical validation tool for TRNG. The AIS31 test, which can be used as a statistical verification tool for generators, is also accepted an international standardization process for RNG designs. For this reason, it is frequently used as a popular test technique in recent studies. AIS31 consists of two separate test protocols A and B applied to raw random numbers (digital noise) and internal random numbers (after the post-processing), respectively. In procedure A, the statistical tests cover only the randomness of the bits and they do not cover their unpredictability. In other words, the statistical tests may detect defects of the randomness source, but they cannot verify its randomness. For this reason, in procedure B the entropy tests are added (Coron's test, Collision test etc.) which can verify the unpredictability of the bits and thus the randomness of the source [24, 25].

The test technique consists of a total of 9 separate statistical test criteria, 6 (T0-T5) of these are for procedure A and 3 (T6-T8) for procedure B. Procedure A's T1-T5 test criteria are identical to FIPS-140 tests, another statistical verification tool for TRNGs. Statistical verification fails if more than one test criterion is not met for random numbers in which Procedures A and B are applied. In cases where only one test criterion fails, procedures A and B are repeated for a different random number sequence. If at least one test criterion for the second repetition fails, validation is considered unsuccessful again [26, 27].

As in the NIST 800-22 test, the AIS31 test was applied to the TRNG offline as in Figure 1 and the results in Table 2 were obtained. All tests from the test procedure A (T0-T5) were executed on the internal random numbers, and all tests from the test procedure B (T6-T8) were executed on the raw random numbers. Target random numbers in which A and B procedures are applied in the system are different from each other. Therefore, a second additional memory architecture as in Figure 5 (G) was used to obtain the raw random numbers needed for procedure A. In addition, for procedures A and B, the minimum length of the target random number sequences must be 5.140.000 bits (20000 * 257 = 5140000 bits) and 7.200.000 bits, respectively.

However, the maximum length of each random number sequence obtained from the system for the test is equal to the depth (65536 bits) of 16-bit counter-supported memory units. Quartus II allows export of block memory contents to a text file in address format at run time. In order to obtain sufficient long random number sequence for test, the memory contents of Figure 5 (F) and (G) were consecutively exported to a text file 80 (80*65536=5.242.880) and 110 (110*65536=7.208.960) times respectively. Then, the memory contents in text format were combined in MATLAB and sufficient length two different test files for AIS31 test were obtained. The number of export process is quite high for six different scenarios in the system. Therefore, the AIS31 test was applied only to random numbers obtained from the 50 MHz sampling scenario and test results are given in Table2. In the system, 100 and 200 MHz sampling scenarios are ignored.

Upon examining the results in Table 1 and Table 2, it is observed that the TRNG provides statistical efficiency needed in terms of cryptography for six different scenarios. When the test results were evaluated, it was demonstrated that the proposed system could also be used for cryptographic applications. . In the system, with additional inputs derived from the noise source in order to provide statistical randomness, a TRNG model, which is simple in terms of hardware and which is easy-to-implement with a push button control on digital devices, was obtained. In contrast to complicated post-processing techniques, XOR post-processing technique was used in the system and the output bit rate of the system was not reduced with the post-processing input. Furthermore, the results given in Table 2 show that TRNG has high entropy per bit and its outputs are unpredictable.

Table 2: AIS 31 test results of TRNG for 50 MHz sampling frequency

Procedure		Tests Criteria		(114, 3) Raw random num.	(114, 13) Internal random num.
AIS31	A	T0 (Disjointness test)		Passed	Passed
		T1 (Monobit test)	FIPS 140	Passed	Passed
		T2 (Poker test)		Passed	Passed
		T3 (Run test)		Passed	Passed
		T4 (Long Run test)		Passed	Passed
		T5 (Autocorrelation test)		Passed	Passed
	B	T6 (Uniform distribution test)		Passed	Passed
		T7 (Comparative test for multinomial distributions)		Passed	Passed
		T8 (Entropy test)		Passed	Passed

The output bit rate of TRNG is directly dependent on the frequency of the non-periodic sampling input f_s obtained from the R3 input. Because the one-bit true random output of TRNG occurs dependent on the changes in the logical level of f_s. The f_s sampling signal obtained from both noise source scenarios is also non-periodic in other words, it is truly random. In addition to statistical verification for TRNG, the measurement of the output bit rate, another important evaluation criterion, is based on the off-line analysis of the non-periodic f_s sampling signal in MATLAB.

Random changes of the non-periodic sampling input f_s are recorded to the memory architecture given Figure 5 (H). Thus, 20 different text files, each consisting of 65536 bits, were obtained for the analysis process for two separate scenarios from the memory architecture at run time. In the system, rising-edge triggered D-type flip-flops were used for sampling. Therefore, the output bit rate of the system is determined by looking at the total number of "01" logical transitions randomly occurred in each text file for f_s. The logical validation of the method is as in Figure 6. In Figure 6, the R1 and Q represent the combined noise source outputs (R_1) and raw true random numbers (f_k) obtained from the noise source in Figure 4, respectively. The total number of sampling transitions of f_s for two separate RO scenarios (57,7) and (57,19) is as in Table 3. The f_{clk} is 50 MHz for both RO scenarios in the system.

Table 3: Number of '01' random sampling transitions in text files for f_s

Fclk	(57,7) RO	Average output bit rate of TRNG	(57, 19) RO	Average output bit rate of TRNG
50 MHz	15.639	15.567 (Mbps)	15.621	15.41 (Mbps)
	15.565		15.516	
	15.562		15.615	
	15.526		15.618	
	15.512		15.506	
	15.599		15.376	
	15.518		15.322	
	15.590		15.396	
	15.642		15.378	
	15.520		15.377	

The total number of logic transitions given in Table 3 also represents the average output bit rate of TRNG. The minimum average output bit rate of TRNG is 30.82 and 61.64 Mbps for 100 and 200 MHz values of f_{clk}, respectively. The performance of the proposed TRNG architecture in terms of output bit rate is considerably higher than the other known oscillator-based studies in the literature. When the comparison results given in Table 4 are examined, it is seen that TRNG is successful in terms of output bit rate, which is another important evaluation criterion besides safety.

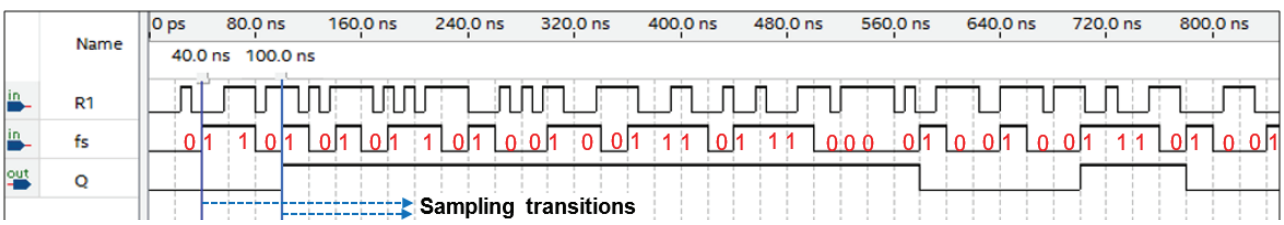


Figure 6: Time-dependent variation of sampling transitions

Table 4: The output bit rate of various FPGA-based TRNGs in the literature

Reference	Oscillator Type	Output bit rate (Mbps)
Avaroğlu et al [8]	Ring+chaos	20.45
Sunar and Stinson [13]	Ring	2.5
Schellekens et al [15]	Ring	2.5
Kohlbrenner and Gaj [16]	Ring	0.5
Fischer et al [17]	PLL	1.0
Dichtl an Golić [18]	Ring	12.5
Tuncer [21]	Ring+chaos	2.17
Hata and Ichikawa [22]	Metastability	12.5
Li et al [23]	Metastability	30.0
Danger et al [28]	Metastability	20.0
Wieczorek and Golofit [29]	FF (flip-flop)	5.0
Istvan et al [30]	Jitter	1.92
Çiçek et al [31]	Chaos	3.2
Tuncer [32]	Ring+chaos	4.77
Koyuncu and Ozcerit [33]	Chaos	58.0
Proposed study (for 200 MHz)	Ring	61.64

6 Conclusions

For TRNGs implemented on digital devices, the entropy of sources of randomness is low. Therefore, it was observed that the statistical quality of random numbers obtained by the pure sampling of ROs in the system was not sufficient to meet the cryptographic competencies. The design architecture was simplified by using true random inputs obtained from the noise source to provide these competencies in the system. The proposed TRNG passed the statistical tests successfully for six different scenarios. The hardware cost of the system, which does not require any additional input from the outside and which does not need the complex post-processing techniques which limit the bit generation rates of the generators, is very low. Therefore, the number of programmable logic elements required for the implementation is less than 1% of the number of the programmable logic elements of the FPGA device used. Thus, it can even be applied to restricted devices.

The designed TRNG has low power consumption, and the final output can pass the NIST800-22 and AIS31 statistical tests, for a minimum output bit rates of 15.41, 30.82 and 61.64 Mbps. The average power consumption of the TRNG for any scenario is 131 milliwatt (mW). This situation can constitute a disadvantage when the increased structural complexity of cryptographic applications depending on security needs is considered. Therefore, the generator can be stopped and operated for critical applications in which energy consumption is important. A true RNG, which can be controlled easily, is fast enough for cryptographic applications and is easily integrable into the system. Besides, the TRNG has an easily adaptable structure for a hierarchically different scenario, frequency, and post-processing techniques. Again, the fact that the additional inputs obtained from entropy sources are truly random made the generator more secure against possible attacks.

7 References

1. Ozkaynak F., "Cryptographically secure random number generator with chaotic additional input", *Nonlinear Dynamics*, 2014;78(3):2015–20. https://doi.org/10.1007/ s11071-014-1591-y
2. Fischer V., "A closer look at security in random number generators design", In International Workshop on Constructive Side-Channel Analysis and Secure Design (pp. 167-182), 2012, Springer, Berlin, Heidelberg. https://doi.org/10.1007/978-3-642-29912-4
3. Yang B., "True Random Number Generators for FPGAs", Ph.D. dissertation, Dept. Elect. Eng., Arenberg Doctoral School, Leuven-Belgium, 2018.
4. Fischer V., Drutarovský M., "True random number generator embedded in reconfigurable hardware", In *International Workshop on Cryptographic Hardware and Embedded Systems* (pp. 415-430), 2002, Springer, Berlin, Heidelberg. https://doi.org/
5. Golic´ J.D., "New methods for digital generation and postprocessing of random data," *IEEE Trans. Comput*., vol.55, no.10, pp.1217– 1229, 2006. https://doi.org/10.1109/tc.2006.164
6. Vasyltsov I., Hambardzumyan E., Kim, Y.S., and Karpinskyy B, "Fast digital TRNG based on metastable ring oscillator", in Proceedings of the 10th International Workshop on Cryptographic Hardware and Embedded Systems (CHES '08), E. Oswald and P. Rohatgi, Eds., vol. 5154 of Lecture Notes in Computer Science, pp. 164–180, Springer, Washington, DC, USA, August 2008. https://doi.org/10.1007/978-3-540-85053-3_11
7. Varchola M., Drutarovsky M., "New high entropy element for FPGA based true random number generators", *in Proceedings of the 12th International Workshop on Cryptographic Hardware and Embedded Systems (CHES '10),* S. Mangard and F.-

X. Standaert, Eds., vol. 6225 of Lecture Notes in Computer Science, pp. 351–365, Springer, Santa Barbara, Calif, USA, August 2010
https://doi.org/10.1007/978-3-642-15031-9_24

8. Avaroğlu E., Tuncer T., Özer A. B., Ergen B., & Türk M., "A novel chaos-based post-processing for TRNG", *Nonlinear Dynamics*, 81(1-2), 189-199, 2015
https://doi.org/10.1007/s11071-015-1981-9
9. Garipcan A.M., Erdem E., " Hardware design and analysis of ring oscillator based noise source for true random number generators," *presented at the International Artificial Intelligence and Data Processing Symposium (IDAP'18)*, 2018.
https://doi.org/10.1109/IDAP.2018.8620811
10. Buchovecká S., Lórencz R., Kodýtek F., & Buček J., "True random number generator based on ring oscillator PUF circuit", *Microprocessors and Microsystems*, *53*, 33-41, 2017
https://doi.org/10.1016/j.micpro.2017.06.021
11. Bochard N., Bernard F., Fischer V., & Valtchanov B., "True-randomness and pseudo-randomness in ring oscillator-based true random number generators", *International Journal of Reconfigurable Computing*, *2010*.
https://doi.org/10.1155/2010/879281
12. Fischer V., Drutarovský M., Šimka M., Celle F., & Komenského P., "Simple pll-based true random number generator for embedded digital systems", In *Proceedings of IEEE Design and Diagnostics of Electronic Circuits and Systems Workshop–DDECS* (pp. 129-136), 2004.
13. Sunar B., Martin W.J., Stinson D.R., "A provably secure true random number generator with built-in tolerance to active attacks", *IEEE Trans. Comput*., vol.56, no.1, pp.109–119, 2007.
https://doi.org/10.1109/tc.2007.250627
14. Wold K., Tan C.H., "Analysis and Enhancement of Random Number Generator in FPGA Based on Oscillator Ring", *International Conference on Reconfigurable Computing and FPGAs*, pp.385-390, 2008
https://doi.org/10.1155/2009/501672
15. Schellekens, D., Preneel, B., Verbauwhede, I., "FPGA vendor agnostic true random number generator", *In: Proc. 16th Int. Conf. Field Programmable Logic and Applications* - FPL 2006
https://doi.org/10.1109/FPL.2006.311206
16. Kohlbrenner P., Gaj K., "An embedded true random number generator for FPGAs", *Proc. ACM/SIGDA 12th Intl. Symp. Field Pro- grammable Gate Arrays (FPGA 2004)*, pp.71–78, ACM, 2004.
https://doi.org/10.1145/968280.968292
17. Fischer V., Drutarovský M., Šimka M., Bochard N. "High performance true random number generator in Altera Stratix FPLDs", *In International Conference on Field Programmable Logic and Applications*, 2004.
https://doi.org/10.1007/978-3-540-30117-2_57
18. Dichtl M., Golic´ J.D., "High-speed true random number generation with logic gates only", *Proc. Cryptographic Hardware and Embedded Systems - CHES 2007*, LNCS 4727, pp.45–62, Springer, 2007.
https://doi.org/10.1007/978-3-540-74735-2_4
19. Tuncer T., "Implementation of duplicate trng on fpga by using two different randomness source", *Elektronika ir Elektrotechnika 21(4),* 35–39, 2015.
https://doi.org/10.5755/j01.eee.21.4.12779
20. Tuncer S. A., "Real-time random number generation with RO-based double PUF", *Informacije MIDEM,* 48(2), 121-128, 2018.
21. Tuncer, T., "The implementation of chaos-based PUF designs in field programmable gate array", *Nonlinear Dynamics*, *86*(2), 975-986, 2016.
https://doi.org/10.1007/s11071-016-2938-3
22. Hata H., Ichikawa S., "FPGA implementation of metastability-based true random number generator", *IEICE TRANSACTIONS on Information and Systems*, *95*(2), 426-436, 2012
https://doi.org/10.1587/transinf.E95.D.426
23. Li C., Wang Q., Jiang J., Guan N., "A metastability-based true random number generator on FPGA", In *ASIC (ASICON), 2017 IEEE 12th International Conference on*(pp. 738-741). IEEE, 2017
https://doi.org/10.1109/ASICON.2017.8252581
24. Killmann W., Schindler W., "A proposal for: Functionality classes for random number generators, version 2.0. Tech. rep.", BSI, Bonn, 2011.
25. Hector (Hardware enabled crypto and randomness) Project, Robustness tests on TRNGs and PUFs Technical Report (V1.0), 2015, available: https://hector-project.eu/downloads/HECTOR-D2.4-PU-M41.pdf
26. Marinakis G., "Design and evaluation of random number generators", *Journal of Applied Mathematics and Bioinformatics*5.3 : 155, 2015.
27. Balasch J., Bernard F., Fischer V., Grujić M., Laban M., Petura O., ... & Yang B., "Design and testing methodologies for true random number generators towards industry certification", *IEEE 23rd European Test Symposium (ETS)*, pp. 1-10, 2018. IEEE.
https://doi.org/10.1109/ETS.2018.8400697
28. Danger J.-L., Guilleya S., Hoogvorsta, P., "High speed true random number generator based on open loop structures in FPGAs", *Microelectronics Journal*, Apr 2, 2009.
https://doi.org/10.1016/j.mejo.2009.02.004
29. Wieczorek P. Z., Gołofit K., "Dual-metastability time-competitive true random number generator", *IEEE Transactions on Circuits and Systems* I: Regular Papers, 61(1), 134-145, 2013.
https://doi.org/10.1109/TCSI.2013.2265952

30. Istvan H., Suciu A., Cret O., "FPGA based TRNG using automatic calibration", *IEEE 5th International Conference on Intelligent Computer Communication and Processing*, pp. 373-376, 2009. https://doi.org/10.1109/ICCP.2009.5284733
31. Cicek I., Pusane A.E., Dundar G., " A novel design method for discrete time chaos based true random number generators", *Integration, the VLSI journal,* 47(1), 38-47, 2014 https://doi.org/10.1016/j.vlsi.2013.06.003
32. Tuncer T., Avaroglu E., Türk M., Ozer A. B., "Implementation of non-periodic sampling true random number generator on FPGA", *Informacije Midem*, *44*(4), 296-302, 2015.
33. Koyuncu I., Ozcerit, A.T., "The design and realization of a new high speed FPGA-based chaotic true random number generator", *Comput. Electr. Eng.* 58, 203–214, 2017. https://doi.org/10.1016/j.compeleceng.2016.07.005

Arrived: 01. 05. 2019
Accepted: 22. 07. 2019

https://doi.org/10.33180/InfMIDEM2019.205

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 49, No. 2(2019), 91 – 100

Fault Prediction of Online Power Metering Equipment Based on Hierarchical Bayesian Network

Da Cheng[1, 2], Penghe Zhang[2], Fan Zhang[3], Jiayu Huang[4]

[1]Hunan University, Department of Electronic Science and Technology, Hunan, China.
[2]China electric power research institute, Beijing, China.
[3]Huludao Power Supply Company, Huludao, China;
[4]Beijing Normal University, Beijing, China.

Abstract: The failure rate assessment of online metering equipment is significant for power metering. For traditional methods, the performance of the model is not satisfactory especially in the case of small samples. In this paper, an online power measuring equipment fault evaluation method based on Weibull parameter hierarchical Bayesian model is proposed. Firstly, the z-score method is used to eliminate outliers in the raw failure data. Then, a generalized linear function with variable intercept is established according to the characteristics of failure data. The information of each region is merged using the characteristics of multi-layer Bayesian network uncertainty reasoning. The model parameters are updated based on the Markov chain Monte Carlo method. Thereafter, the trend of failure rate is provided with time-dependent. Finally, the proposed method is verified by the failure samples of the online measurement equipment in three typical environmental areas. The accuracy and validity of the hierarchical Bayesian model is verified by a series of experiments.

Keywords: failure rate; hierarchical Bayesian model; variable intercept; Weibull

Napovedovanje izpada na opremi merjenja moči na osnovi hierarhične Bayesianove mreže

Izvleček: Ocena stopnje izpada na merilni opremi moči je zelo pomembna. Pri klasičnih metodah je učinkovitost ni zadostna, kar se pokaže predvsem pri majhnih vzorcih. V pripsevku je predlagana metoda napovedi izpadov merilne opreme na osnovi Wibullovega parametra hierarhičnega Bayesianovega modela. Najprej so iz surovih podatkov odstranjeni neuporabni podatki na osnovi metode z-ocene. Informacija je nato združena z uporabo karakteristik večslojne Bayesianove mreže in nadgrajena z Markovo verigo po Monte Carlo metodi. Trendi so časovno odvisni. Rezultati so preverjeni in ovrednoteni z meritvami v treh tipičnih okoljih.

Ključne besede: stopnja odpovedi; hierarhičen Bayesianov model; Weibull

** Corresponding Author's e-mail: 13910761850@126.com*

1 Introduction

Energy metering equipment, such as electric meters and collectors, have a large amount and wide distribution in the power grid. As the nerve endings of the smart grid, electricity meters play an irreplaceable role in electricity information collection and energy monitoring [1]. Meanwhile, the reliability of the metering equipment is also related to the safety of household electricity consumption. Inaccurate energy metering affects the strategic planning of power generation, transmission and use of electricity [2]. The failure rate evaluation of the metering device over time and the fault are limited because it is difficult to collect large amounts of sample information. Therefore, it is of great significant to establish a scientific and reliability evaluation scheme for the reliability design of metering equipment.

In recent decades, a large number of methods are applied to target prediction and fault analysis. Generally,

these methods can be classified into two categories, namely deterministic method and probability method [3]. The Support Vector Regression (SVR) model is employed to identify fault and predict the remaining life of the reciprocating compressors based on the sensory data [4]. In addition, accurate bearing remaining useful life of machine's breakdown and maintenance's cost is proposed based on the artificial neural network [5]. These algorithms and methods achieve high precision prediction. However, enough samples are required to train the models before the effective prediction results is given. Moreover, the data is relatively simple, which limits its accuracy. The Principal Component Analysis (PCA) is utilized to select fault-relevant variable [6], so that a subset of variables based on training and validation data sets can be obtained to achieve better possible performance [7]. But this method has an unsatisfactory performance, especially in the absence of prior information. Consequently, the deterministic method lacks probability information for uncertain problems.

Probabilistic methods, one that can detect uncertainty in the data and provide more information, often used for failure analysis [8]. Fault Tree Analysis (FTA) is one of the most commonly used probabilistic methods. A system level electric field exposure assessment by FTA is proposed in [9]. However, the detailed system structure is needed for fault tree analysis. The Gaussian Process (GP) is another method for probability analysis [10]. The remaining useful life prediction for service units is used to improve the accuracy [11]. But the unexplained nature of this nonparametric model limits its application. Then, the Bayesian estimation is widely used in failure rate analysis [14]. For example, a Bayesian method is proposed for the hazard rate analysis of electronic devices [15]. Moreover, the fuzzy evidence theory, can be combined with Bayesian to solve the problem of insufficient samples [12][13]. Intuitively, probability method can provide more information, such as confidence interval and quantile, and is more suitable for the processing of small sample data.

To achieve failure rate analysis of online metering equipment, a Hierarchical Bayesian Network (HBN) is proposed based on a small number of electrical meters fault samples. A segmented Weibull parameter model is introduced for failure rate analysis at different times to better fit the data. Considering the different environments in different regions, part of the information fusion method is used in measurement equipment. Moreover, the real fault samples in three typical environments are used to verify the validity of HBN. The reliability of the metering device is calculated, and the parameters of the model are interpretable compared to traditional FTA and GP models.

The remaining part of this paper is organized as follows: Section II describes the outlier detection method in sample data. The proposed Weibull hierarchical Bayesian model is presented in Section III. Thereafter, the fault data of electrical meters in different regions is analyzed in Section IV. Finally, the conclusion is presented in Section V.

2 Failure rate data outlier detection

In the actual process of data collection, abnormal values may exist in the raw failure rate data due to the operational errors of researchers. The outliers not only affect the model's evaluation of the power metering equipment reliability, but also easily cause the model to be overfitting [16]. Traditional failure assessment methods are difficult to balance in small sample, failure rate data with missing data and outliers.

In order to clean up the abnormal value of the raw failure rate data and reduce the information loss, the Z-score method is used to clean the outliers in the fault rate data. The Z-score method determines the outliers by solving the relative standard distance of the data from the mean, which is suitable for the outlier detection under small samples.

Let $\mathbf{Y}=\{y_{s,t,j}\}$, where $y_{s,t,j}$ denotes the fault rate of the measuring device measured in the j^{th} time, t=1,...,L, j=1,...,N, and in the s area at the measurement time t. The standard deviation σ_t of the failure rate data for each measurement is:

$$\sigma_t = \sqrt{\frac{1}{N}\sum_{t}^{L}\left(y_{s,t,j} - u_{s,t,j}\right)^2}, \qquad t = 1,2,...,L \tag{1}$$

where N is the total number of failure rate data when the measurement time is t, $u_{s,t,j}$ is the average of the failure rate data for each measurement and $y_{s,t,j}$ denotes the fault rate of the measuring device measured in the jth time. Considering the discontinuity of the sample data and reducing the loss of valid data, a window of length three is used to analyze the outliers in failure rate data, and the window is composed of three measurements of [t, t+1, t+2]. That is, the standard deviation of three consecutive measurements is calculated each time, and the Z score Z_j of each data point $y_{s,t,j}$ is calculated as

$$Z_j = \frac{y_{s,t,j} - u'_{s,t,j}}{\sigma'_t} \tag{2}$$

where $u'_{s,t,j}$ are the mean failure rate of three consecutive measurements, σ'_t is the standard deviation of $u_{s,t,j}$=

$u'_{s,t,j}$ in equation (1), at which point Z_j can be regarded as obeying the normal distribution N(0, 1). Finally, the threshold for determining the abnormal data is set to three times the standard deviation of N(0, 1). The outliers of the original failure rate data with the score $|Z_j|$ greater than the threshold is replaced by the mean $u'_{s,t,j}$. Then the failure rate data $\mathbf{Y}^*=\{y^*_{s,t,j}\}$ without the outlier is obtained.

3 Weibull parameter model for metering equipment failure rate

3.1 Other Recommendations

The commonly used online power metering equipment includes electrical meters, power quality detecting devices and concentrators, etc. This paper takes the electrical meter as the target to analyze. The electric energy metering equipment is a high-precision measuring instrument. The damage of the weakest link of the system will directly lead to the failure of the measuring equipment. The Weibull distribution is used as the fault description of the commonly used electronic instruments [17], so the Weibull distribution is used to fit the electric energy meter data, the probability density function of Weibull is

$$f(t\,|\,\lambda,\alpha,\chi)=\lambda\alpha(t-\chi)^{\alpha-1}\exp[-\lambda(t-\chi)^{\alpha}]$$
$$t>0,\ \lambda>0,\alpha>0,\chi\geq 0 \tag{3}$$

where t is the fault time, λ is the scale parameter, α is the shape parameter, and χ is the location parameter. We set χ to 0 considering that the failure starts after t=0. Then the χ is reduced to a two-parameter Weibull distribution. When the Weibull distribution probability density function f(t) is integrated, the value is always not less than 0, which is consistent with the condition that the number of failures is not less than 0.

The observed data $\mathbf{Y}^*$ obeys the Weibull regression model, which can be expressed as

$$\mathbf{Y}^*\sim \text{Weibull}(\lambda,\ \alpha) \tag{4}$$

Generally, the change of the shape parameter α indicates that the failure mechanism changes. Therefore, the shape parameter a is set to obey the fixed distribution function. At this time, the regression model can be established by changing the scale parameter λ in the Weibull regression model.

When the observed data $\mathbf{Y}^*$ is the metering device fault data, the fault number $\mathbf{Y}^*$ will change according to the time variable x. Therefore, Weibull distribution function will change, and a regression model can be established based on λ

$$\lambda=\beta_0+\beta_1x_1+\cdots+\beta_kx_k=\mathbf{x}^{\mathrm{T}}\boldsymbol{\beta} \tag{5}$$

where β_k is the regression coefficient, x_k is the covariate. Considering the condition that the scale parameter λ is greater than 0, the value of the regression coefficient is limited. To select a wider distribution parameter as the prior distribution of β_k, the log() correlation function is used to limit the range

$$\log(\lambda)=\mathbf{x}^{\mathrm{T}}\boldsymbol{\beta}+w_i \tag{6}$$

where w_i is the measurement error when measuring the number of failures $\mathbf{Y}^*$, i is the number of sub-sample categories divided by the HBN model based on the total sample information. The log(λ) range becomes (−∞, +∞), and λ is inversely solved from equation (4).

$$\lambda=\exp(\mathbf{x}^{\mathrm{T}}\boldsymbol{\beta}+w_i) \tag{7}$$

At this time, there is no limit to the prior distribution of β_k. When the covariate changes to Δx, the contribution to the scale factor becomes exp(Δ$x\beta$).

3.2 Structure of Hierarchical Bayesian Model

In order to realize the failure rate evaluation and prediction of the measuring equipment, Bayesian networks (BN) are used to fuse data from different regions. BN takes full advantage of early prior information and sample data information to achieve a full estimate of the latest events [18]. In particular, HBN takes advantage of information between levels to provide better data fitting capabilities [19].

For BN, the posterior probability density based on prior parameters θ is

$$p\left(\theta\,|\,\mathbf{Y}^*\right)=\frac{f(\mathbf{Y}^*\,|\,\theta)p(\theta)}{\int f(\mathbf{Y}^*\,|\,\theta)p(\theta)\mathrm{d}\theta} \tag{8}$$

where $f(\mathbf{Y}^*\,|\,\theta)$ is the likelihood function of the Bayesian model, p(θ) is the model prior distribution. The HBN model refers to the different levels of data parameters elaborated by other layer parameters, which specifies another layer of prior knowledge for a layer of parameters.

The denominator in equation (8) is independent of the parameter θ. When the Weibull distribution is used as the likelihood function of the model, the parameter posterior distribution is proportional to the numerator of (8), and it can be further expressed as

$$p(\theta\,|\,\mathbf{Y}^*)\propto f(t\,|\,\theta)p(\theta\,|\,\alpha,\boldsymbol{\beta},w_i) \tag{9}$$

where $p(\theta|\alpha, \beta, w_i)$ represents the prior distribution of the parameters α, β, w_i.

In the Weibull distribution, the size of the parameter α determines the increase and decrease of the failure rate. When α>1, it indicates that the instrument is in the wear stage. And when α<1, which is suitable for the early failure stage of the instrument. Therefore, the parameter prior selection must meet certain conditions.

In the absence of any prior information α, according to the influence of α on the shape of Weibull distribution, the prior distribution *f* can be obtained by the HalfCauchy distribution.

$$p(\theta \mid \mathbf{Y}^*) \propto f(t \mid \theta) p(\theta \mid \alpha, \boldsymbol{\beta}, w_i) \tag{10}$$

where *b* is the scale parameter of the distribution, and equation (10) can be abbreviated as HalfCauchy(*b*).

For the regression coefficient β, the setting of the log correlation function avoids limiting the range of coefficient values, and the prior distribution *f* of the regression coefficient β can be set to normal distribution, which can be defined as

$$f(u, \tau \mid t) = \sqrt{\frac{\tau}{2\pi}} \exp\left\{-\frac{\tau}{2}(t-u)^2\right\} \tag{11}$$

where *u* is the normal distribution mean, 1/τ is the distribution variance. The measurement error w_i value is small, so the prior distribution of w_i may take a normal distribution with a small variance as well as the mean *u* = 0, and equation (11) can be abbreviated as N(*u,* 1/τ).

Substituting equation (10) and (11) into (7), the joint prior distribution of the parameters λ and α can be calculated as

$$p(\boldsymbol{\beta}, b, w_i) = \frac{2\exp(\mathbf{x}^{\mathrm{T}}\boldsymbol{\beta} + w_i)}{\pi b[1 + (t/b)^2]} \tag{12}$$

Similarly, substituting equation (12) and (3) into (9), the joint posterior distribution λ and α can be expressed as

$$p(\lambda, \alpha \mid \mathbf{Y}^*) \propto \frac{2\exp(\mathbf{x}^{\mathrm{T}}\boldsymbol{\beta} + w_i - \lambda t^{\alpha})}{\pi b[1 + (t/b)^2]} t^{\alpha-1} \tag{13}$$

Then the posterior distributions of the parameters λ and α in the hierarchical Bayesian model are

$$p(\lambda \mid \alpha, \mathbf{Y}^*) \propto t^{\alpha-1} \exp(w_i - \lambda t^{\alpha}) \times \exp(\mathbf{x}^{\mathrm{T}} \sqrt{\frac{\tau}{2\pi}} \exp\left\{-\frac{\tau}{2}(t-u)^2\right\}) \tag{14}$$

$$p(\alpha \mid \lambda, \mathbf{Y}^*) \propto \frac{\exp(w_i - \lambda t^{\alpha})}{\pi b[1 + (t/b)^2]} t^{\alpha-1} \tag{15}$$

After the parameter posterior distribution is obtained, the influence of the variation of the covariate **x** on the failure rate of the model can be reflected by the parameter mean value and the confidence interval.
When the new covariate **x** changes to **z**, the fault value can be calculated based on the existing fault number $\mathbf{Y}^*$, and the posterior distribution of the parameter is

$$p\left(\mathbf{z} \mid \mathbf{Y}^*\right) = \sum\sum f(\mathbf{z} \mid \theta) p(\theta \mid \mathbf{Y}^*) \mathrm{d}\theta \tag{16}$$

3.3 Failure rate Prediction of Metering Equipment

When the equipment fails, the rate of failure change does not always obey the fixed distribution. At this time, the regression coefficient β can be segmented according to the trend of failures number **x**. Then **β** can be expressed as

$$\boldsymbol{\beta} \sim \begin{cases} N(u_1, 1/\tau_1), & x < \sigma \\ N(u_2, 1/\tau_2), & x \geq \sigma \end{cases} \tag{17}$$

where σ is the time node at which the failure rate changes. Since only the trend of data can be observed, the failure rate change node cannot accurately specified. Thus, no information can be specified on the prior distribution *σ*

$$f(\sigma) = \frac{1}{\eta_1 - \eta_2} \tag{18}$$

where η_1 and η_2 are upper and lower limits of the density function. The regression model after segmentation can better follow the change of the failure rate of the metering equipment.

4 Fault analysis of metering equipment

4.1 Failure Data of Electrical Meters

In order to verify the effect of HBN model on the failure rate of metering equipment in different provinces, we analyze partial fault samples of Electrical Meters produced by the same company in Xizang (XZ), Xinjiang (XJ) and Heilongjiang (HLJ) province in the period of 2012-2017.

The fault data is collected from multiple locations, as shown in Fig. 1. The operating status of the electrical meter is transmitted to the concentrator via the power line carrier. Then the failure data in different areas are

transmitted to the base station through GPRS. Particularly, Fig. 1 demonstrates an example of an electricity meter with a measure fault. In this way, the number of electrical meter faults in different regions can be statistically analyzed in real time.

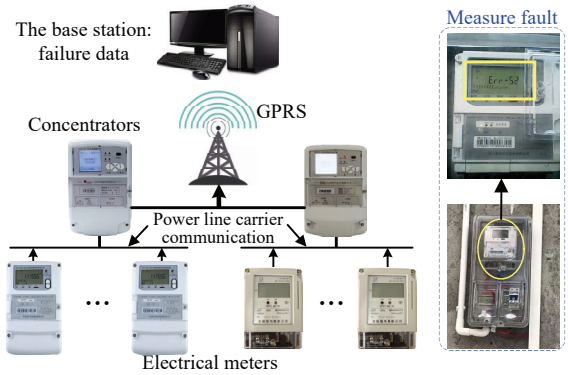


Figure 1: The fault data acquisition framework of the measuring equipment

Fig. 2-4 show the failure rates of the three areas, respectively. From the Fig. 2-4, it can be seen that there are seven groups of data in XZ and XJ, six groups in HLJ. All data are extracted independently, and each set of data contains six data points for the period 2012-2017. The failure rate is calculated by dividing the number of failures of the electrical meters by the total operation of the metering equipment each year.

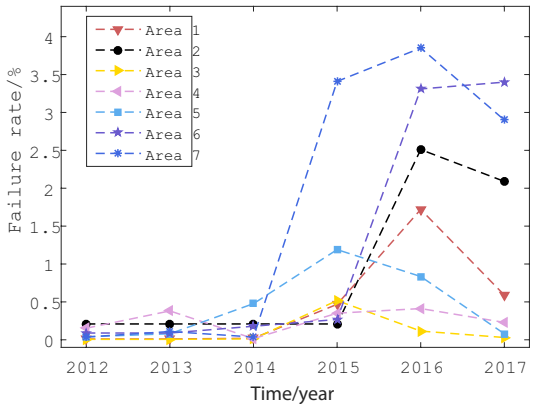


Figure 2: The electrical meters failure rate curve of XZ

As we can see from Fig. 2 and 3, the failure rate increased in the first five years and decreased in the sixth year and the failure rate of XZ is slightly higher than XJ. Fig. 2-4 show that the failure rate of metering equipment varies in different provinces. Therefore, through modeling and analysis of this example, the reliability variation relationship of metering equipment in different provinces can be found and the accurate prediction results is given. In addition, the data of 2014 in

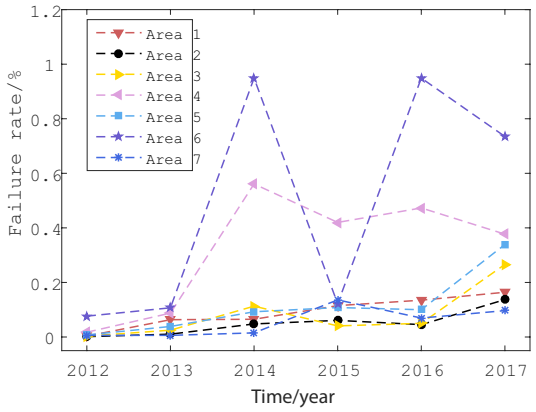


Figure 3: The electrical meters failure rate curve of XJ

Fig. 3 and one point in 2013 in Fig.4 are too large to be outliers.

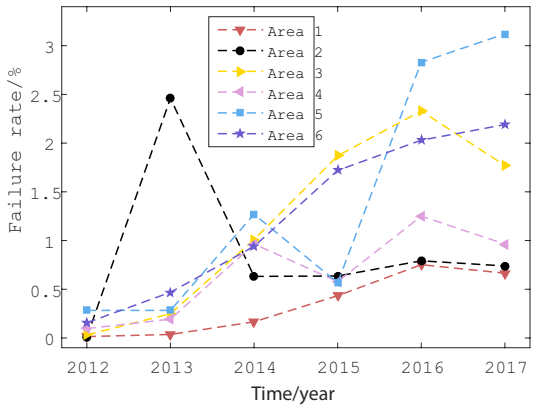


Figure 4: The electrical Meters failure rate curve of HLJ

The model analysis software uses the simulation platform based on Pycharm. Moreover, the Pymc3 based on Python is used to analyze the collected data [20].

4.2 Model structure and experimental steps

The structure of the hierarchical Bayesian model for the failure rate of online power metering equipment is as follows:

First floor:

$$Y \sim \text{Weibull}(\lambda, \alpha) \tag{19}$$

$$\lambda = \exp(\beta_i + x\beta_x + w_i) \tag{20}$$

$$\alpha \sim HalfCauchy(10) \tag{21}$$

Second floor:

$$\beta_i \sim N(0, 10^5) \tag{22}$$

$$\beta_x \sim \begin{cases} N(0,10^5), & x < \sigma \\ N(0,10^5), & x \geq \sigma \end{cases} \quad (23)$$

$$\sigma \sim \text{DiscreteUniform}(3,6) \quad (24)$$

$$w_i \sim N(0,10^{-3}) \quad (25)$$

According to the data of three provinces, the intercept *i* of formula (20) is set to 3 to reflect the difference of fault data of metering equipment in the three provinces. The covariant *x* takes one term, and the regression coefficient β_x of the three provinces is set to the same value to reflect the commonness of the products produced by the same company. According to the change of data, the failure rate change node σ can be set between 3-6 years, that is, the period of fault change fluctuation is 2014-2017. The flow chart of algorithm experiment is shown in Fig. 5.

According to flowchart Fig. 5, in order to accurately analyze the occurrence of faults in the three provinces, the algorithm flow can be summarized into the following four steps:

- Data preprocessing: The failure number of electrical meters is transformed into the failure rate. Different environmental characteristics are normalized to reduce the impact of units.
- Model establishment: Establish fault prediction model based on HBN. Then a priori distribution of model parameters is specified in conjunction with no information prior.
- Model solving: Combined simulation platform Pymc3, the MCMC posterior sampling method is used to get the target optimization parameter [21]. We use the NUTS sampling method to achieve fast convergence, where the HBN model sampling iterations are set to 10000, and the pre-firing period is set to 2000.
- Model verification: If the acceptance probability does not match the target, we than increase the number of samples or adjust the model prior distribution until it satisfies the acceptance probability.

In the process of establishing Markov chain by using MCMC sampling method to solve the Model, NUTS sampling has good effect on high-dimensional and long data, avoiding the influence of step size on sampling robustness and converges faster than Gibbs sampling method. Therefore, NUTS algorithm is used to sample the model to achieve fast convergence [22][23].

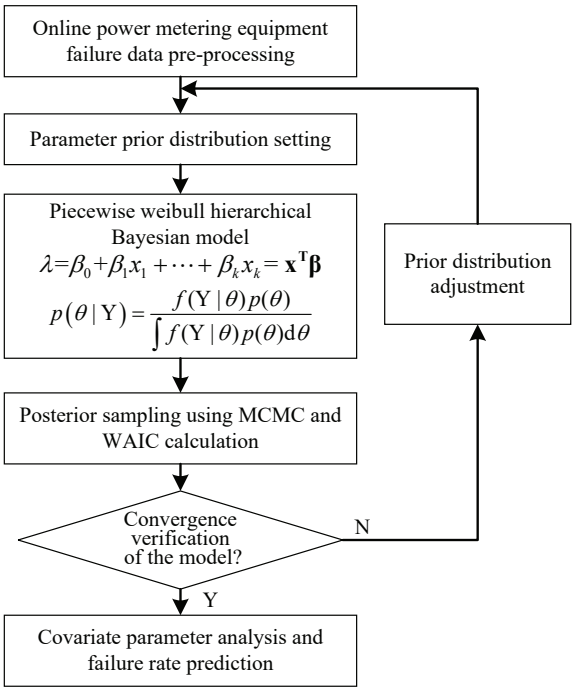


Figure 5: The experimental flowchart of HBN model algorithm

In order to verify the accuracy of the model, after solving the parameters of the prior distribution, the likelihood function is sampled to verify whether the posterior distribution of the failure rate conforms to the original failure rate data distribution. According to the posterior mean of the parameters, the prior parameters of the model are continuously adjusted to achieve the fitting of the model to the original failure rate data. Finally, the posterior distribution of linear function parameters with variable intercept is obtained, and the failure rate of metering equipment in the next year in three provinces is predicted respectively.

4.3 Experimental results analysis

The HBN model sampling iterations are set to 10, 000, and the pre-firing period is set to 2, 000. In order to verify the accuracy of the parameter results of the HBN model, the Maximum a Posteriori (MAP) estimate of the optimal solution is compared with the results of the HBN model. And Table I shows the results of the HBN model and the parameters calculated by MAP.

It can be seen from Table I that the intercept β difference of linear function is about 1, indicating that there is a certain difference in metering equipment in the three provinces, and this difference is related to the province. The difference of time coefficient early_β and late_β indicates that the increasing trend of failure rate has changed. In 2014, the change trend of failure rate

of metering equipment changed, and the failure rate showed a downward trend before 2015. The value of measurement error *w* is small, which indicates indicating that the error in the measurement process has little influence on the failure rate of metering equipment. The error between the mean value of the HBN model and that of the MAP model is small, which indicates the validity of the HBN model.

Table 1: Parameter results of HBN model

Variable	Mean	Standard deviation	2.5% quantile	97.5% quantile	MAP estimation
β0	-3.388	0.311	-4.010	-2.803	-3.412
β1	-4.510	0.303	-5.120	-3.939	-4.603
β2	-2.939	0.306	-3.518	-2.293	0.932
early_βx	0.761	0.087	0.003	0.459	0.724
late_βz	0.593	0.067	0.002	0.796	0.917
α	0.938	0.066	0.001	0.816	1.075
w	2×10^{-6}	1×10^{-4}	2×10^{-6}	1.8×10^{-4}	2×10^{-4}

Fig. 6 shows the Weibull posterior distribution of the failure rate in the three provinces. The red dashed line is the mean value of the original failure rate data in the three provinces. The mean value of the Weibull posteriori distribution is consistent with the location of the red line, indicating that the distribution of the failure rate data in the last six years obeys the Weibull parameter model.

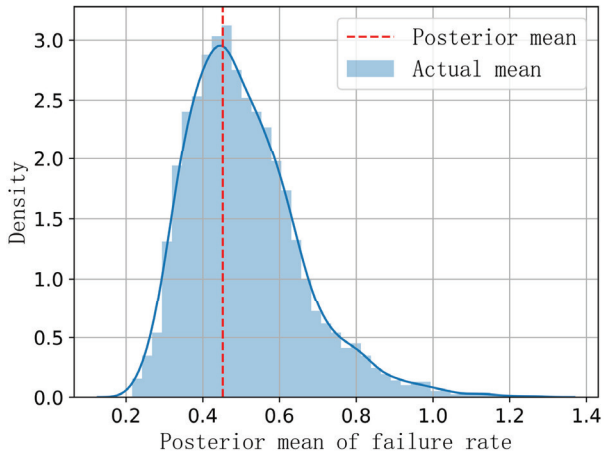


Figure 6: Posterior mean distribution of HBN model

To verify the validity of the model, we compare the proposed model with the pooling HBN, Poisson model and Cauchy model. Note that the all parameters have only one value in pooling HBN. On the other hand, the difference between proposed method and Poisson model, Cauchy model is the observed values follow different distributions. For example, the Poisson model means that the observed data Y^* obeys the Poisson regression model. It's worth mentioning that all the prior distributions are the same for a fairer comparison.

Fig. 7-9 show a comparison of linear fitting curve mean, confidence interval and original failure rate data, respectively. Note that many of the gray lines are derived from predicted values within the confidence interval. The lowest and highest gray curves are confidence intervals of approximate 95% linear function. The failure data of measuring equipment are basically within 95% confidence interval after the fusion analysis of fault data using the method presented in this paper. The linear function can follow the jump trend of failure rate, which shows that the HBN model can fit the fault data of metering equipment well.

Moreover, all the other methods only have good performance on partial data. For example, the Poisson model can follow the trend of the data in XZ and HLJ. However, it have poor performance in XZ, which has a lower failure rate. At the same time, the pooling HBN cannot follow the trend of failure rate in XJ due to the model assumes the same trend for data in all regions.

In order to accurately predict the failure rate of measuring equipment, the time data is set to 7, which means the failure rate in 2018. After the model is substituted, the mean value of the failure rate in 2018 can be predicted as follows: the average failure rate of measurement equipment in XZ is 2.531, the average failure rate in XJ is 0.778 and the HLJ is 2.546. The predicted failure rate is within the confidence interval of 2017, which indicates that the model has the ability of short-term prediction.

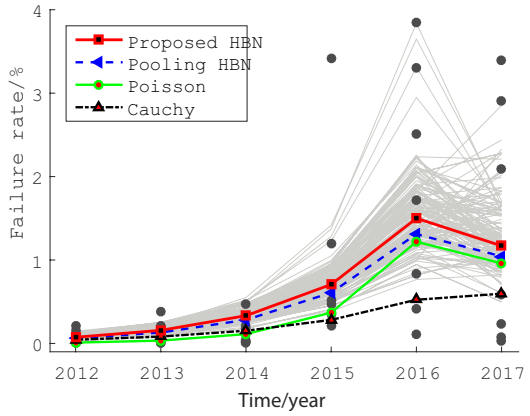


Figure 7: Comparison of fitting curve and the failure rate of the XZ Province

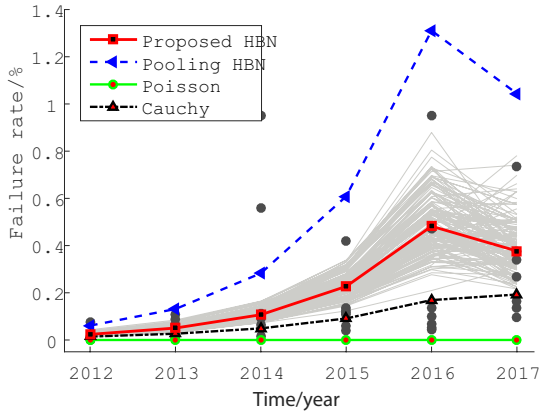


Figure 8: Comparison of fitting curve and the failure rate of XJ

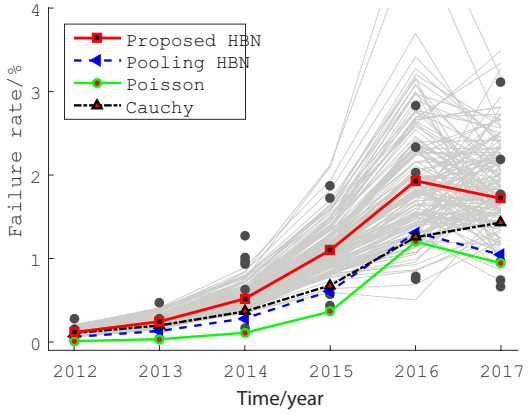


Figure 9: Comparison of fitting curve and the failure rate of HLJ

In order to evaluate the effect of partial information fusion of HBN model and realize the evaluation of different models, the Widely Available Information Criterion (WAIC) is more accurate than the traditional DIC when considering the whole posteriori distribution of the model [24]. Table II gives the WAIC calculation values of the four models under the same linear function condition and the same observation data.

Table 2: The comparison of WAIC between HBN and other models

Models	WAIC	pWAIC	weight	SE
HBN	-24.43	7.13	0.95	38.39
Pooling-HBN	7.26	3.71	0	35.39
Possion	123.3	5.03	0.05	19.32
Cauchy	138.04	14.09	0	36.5

It can be seen from Table II that the information criterion of partial information fusion HBN model is smaller, the number of effective parameters of the model is 7.13, and the weight of model is 0.95, which is much larger than the rest models. The SE of the proposed method (HBN) is slightly larger than other models. HBN has better and the smallest WAIC value, which means that its uncertainty is consistent with its accuracy. Thus the effectiveness of partial information fusion HBN model is demonstrated. Conversely, the rest of the models have higher WAIC values, including that the models cannot effectively fit the raw data.

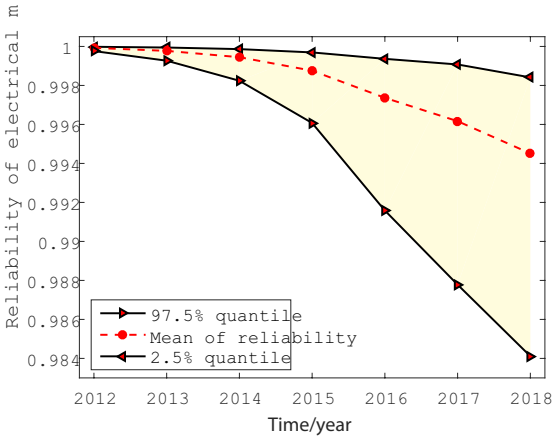


Figure 10: Reliability Curves and Confidence Intervals of power metering equipment

When the new electric energy meter equipment is put into use in the region, the failure rate of the electric energy metering equipment can be calculated according to equation (16). The reliability of the short-term prediction result of the new electric energy meter equipment is shown in Fig. 10. Fig. 10 shows that the reliability of the failure rate of the energy metering equipment decreases with time. After 6 years of operation, the reliability of the energy metering equipment is about 0.93, indicating that the type of energy metering equipment has a higher reliability under the three regional environmental conditions. In addition, the reliability curve approximates a straight line, indicating that the failure rate trend of the energy metering equipment is relatively flat in the short term. Moreover, the confidence interval of the reliability of the energy metering equipment is gradually increased, indicating that the uncertainty becomes large. Overall, the operation strategy does not need to change greatly.

5 Conclusion

By analyzing the fault data characteristics of online power metering equipment in different regions, a multi-bass Bayesian-based Weibull parameter regression model is established. Firstly, the Z-score method is used to clean the data outliers to reduce the interference of the outliers on the model. Then, according to the fault

data of the three regions, the intercept variable regression model of partial information fusion is established, and the failure rate data change node is fully considered. In the case, the influence of time factor on the failure rate of metering equipment in the three regions is obtained, and the average forecasting rate of the metering equipment failure rate in the seventh year is given. The example results verify that the method can effectively evaluate the failure rate relationship between the measuring equipment and different areas, and prove the feasibility of the scheme. Prior selection in small samples remains a challenge, and future work will focus on parameter settings for small sample models.

6 Acknowledgment

This paper is supported by Research on influence and evaluation of key components on relay protection performance.

7 References

1. H. Qing, L. Fangxing, W. Lei, et al. „Smart Meter Working Status Evaluation Method Based on Evidence Theory," 2018 Conference on Precision Electromagnetic Measurements (CPEM 2018), Paris, 2018, pp. 1-2, 2018. https://doi.org/ 10.1109/CPEM.2018.8501081.
2. MT. Mohammadat, SM. Nafie, FB. Sharief, On electronic energy meters diagnosis exploiting components' susceptibility to failure. 2015 International Conference on Computing, Control, Networking, Electronics and Embedded Systems Engineering (ICCNEEE). pp. 418-421, 2015. https://doi.org/10.1109/ICCNEEE.2015.7381404.
3. Q. Xu, D. He, N. Zhang, et al. „A Short-Term Wind Power Forecasting Approach With Adjustment of Numerical Weather Prediction Input by Data Mining," IEEE Transactions on Sustainable Energy, vol. 6, no. 4, pp. 1283-1291, 2015. https://doi.org/10.1109/TSTE.2015.2429586.
4. X. Li, F. Duan, I. Bennett, et al. „Canonical variate analysis, probability approach and support vector regression for fault identification and failure time prediction," Journal of Intelligent & Fuzzy Systems, vol. 34, no. 6, pp. 3771-3783, 2018. https://doi.org/10.3233/JIFS-169550.
5. J. Ben Ali, B. Chebel-Morello, L Saidi, et al. „Accurate bearing remaining useful life prediction based on Weibull distribution and artificial neural network," Mechanical Systems and Signal Processing, vol. 56-57, pp. 150-172, 2015. https://doi.org/10.1016/j.ymssp.2014.10.014.
6. Q. Jiang, X. Yan, B. Huang. „Performance-Driven Distributed PCA Process Monitoring Based on Fault-Relevant Variable Selection and Bayesian Inference," IEEE Transactions on Industrial Electronics, vol. 63, no. 1, pp. 377-386, 2016. https://doi.org/10.1109/TIE.2015.2466557.
7. K. Ghosh, M. Ramteke, R. Srinivasan. „Optimal variable selection for effective statistical process monitoring," Computers & Chemical Engineering, vol. 60, no. 10, pp. 260-276, 2014. https://doi.org/10.1016/j.compchemeng.2013.09.014.
8. M. Ram. „On system reliability approaches: a brief survey," International Journal of System Assurance Engineering and Management, vol. 4, no. 2, pp. 101-117, 2013. https://doi.org/urn:issn:0975-6809.
9. L. Jin, C. Peng, T. Jiang. „System-Level Electric Field Exposure Assessment by the Fault Tree Analysis," IEEE Transactions on Electromagnetic Compatibility, vol. 59, no. 4, pp. 1095-1102, 2017. https://doi.org/10.1109/TEMC.2017.2647961
10. D. Lee, R. Baldick. „Short-Term Wind Power Ensemble Prediction Based on Gaussian Processes and Neural Networks," IEEE Transactions on Smart Grid, vol. 5, no. 1, pp. 501-510, 2014. https://doi.org/10.1109/TSG.2013.2280649.
11. R. Kontar, S. Zhou, C. Sankavaram, et al. „Nonparametric-Condition-Based Remaining Useful Life Prediction Incorporating External Factors," IEEE Transactions on Reliability, vol. 67, no. 1, pp. 41-52, 2018. https://doi.org/10.1109/TR.2017.2717190.
12. Yazdi M, Kabir S (2018). "Fuzzy evidence theory and Bayesian networks for process systems risk analysis". Hum Ecol Risk Assess An Int J (0),1–30. https://doi.org/10.1080/10807039.2018.1493679.
13. Yazdi M, Kabir S (2017). "A fuzzy Bayesian network approach for risk analysis in process industries". Process Saf Environ Prot, (111) ,507–19. https://doi. org/10.1016/j.psep.2017.08.015.
14. M. Han. „E-Bayesian estimation and hierarchical Bayesian estimation of failure rate," Applied Mathematical Modelling, vol. 33, no. 4, pp. 1915-1922, 2009. https://doi.org/10.1080/03610926.2010.498643.
15. T. Yuan, Y. Kuo. „Bayesian Analysis of Hazard Rate, Change Point, and Cost-Optimal Burn-In Time for Electronic Devices," IEEE Transactions on Reliability, vol. 59, no. 1, pp. 132-138, 2010. https://doi.org/10.1109/TR.2010.2040776.
16. M. Gupta, J. Gao, CC. Aggarwal, et al. „Outlier Detection for Temporal Data: A Survey," IEEE Transactions on Knowledge and Data Engineering, vol. 26, no. 9, pp. 2250-2267, 2014. https://doi.org/10.1109/TKDE.2013.184.

17. B. Benedik, K. Taškova, J. Tavčar, et al. „Prediction of vacuum cleaner motor brush life: a regression approach," IET Electric Power Applications, vol. 9, no. 9, pp. 569-577, 2015. DOI: 10.1049/iet-epa.2014.0437. https://doi.org/10.1049/iet-epa.2014.0437
18. B. Cai. „Bayesian Networks in Fault Diagnosis," IEEE Transactions on Industrial Informatics, vol. 13, no. 5, pp. 2227-2239, 2017. https://doi.org/10.1109/TII.2017.2695583.
19. M. Han. „E-Bayesian estimation and hierarchical Bayesian estimation of failure rate," Applied Mathematical Modelling, vol. 33, no. 4, pp. 1915-1922, 2009. https://doi.org/10.1080/03610926.2010.498643.
20. J. Salvatier, TV. Wiecki, C. Fonnesbeck. „Probabilistic programming in Python using PyMC3," PeerJ Computer Science, vol. 2, pp. e55, 2016. https://doi.org/10.7717/peerj-cs.55.
21. Z. Hao, J. Guo, S. Zeng. „Fully Bayesian reliability assessment of multi-state systems with overlapping data," Journal of Systems Engineering and Electronics, vol. 28, no. 1, pp. 187-198, 2017. https://doi.org/10.21629/JSEE.2017.01.21.
22. S. Watanabe. „Asymptotic Equivalence of Bayes Cross Validation and Widely Applicable Information Criterion in Singular Learning Theory," Journal of Machine Learning Research, vol. 11, no. 18, pp. 3571-3594, 2010. https://doi.org/10.1002/rnc.1572
23. S. Sun, Y. Feng, C. Dong, et al. „Efficient SRAM Failure Rate Prediction via Gibbs Sampling," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 31, no. 12, pp. 1831-1844, 2012. https://doi.org/10.1109/TCAD.2012.2209884.
24. A. Vehtari, A. Gelman, J. Gabry. „Practical Bayesian model evaluation using leave-one-out cross-validation and WAIC," Statistics and Computing, vol. 27, no. 5, pp. 1413-1432, 2017. https://doi.org/10.1007/s11222-016-9696-4.

Arrived: 23. 02. 2019
Accepted: 19. 08. 2019

https://doi.org/10.33180/InfMIDEM2019.206

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 49, No. 2(2019), 101 – 111

Piezoelectric Micropump Driving Module With Programmable Slew-Rate and Dead-Time

Matej Možek, Borut Pečar, Drago Resnik and Danilo Vrtačnik

University of Ljubljana, Faculty of Electrical Engineering, Laboratory of Microsensor Structures and Electronics (LMSE), Ljubljana, Slovenia

Abstract: High efficiency piezoelectric micropump driving module with programmable slew-rate and dead-time has been designed, implemented and characterized for driving custom made piezoelectric micropumps. Developed driver enables independent setting of several rectangular output signal parameters, such as frequency, positive and negative amplitudes, slew-rates, dead time, and modes of operation (pump/valve).
Implemented driver can achieve amplitudes up to 250 VPP on a frequency range from DC to 1 kHz, slew-rate up to 18 V/µs at maximum power consumption 1.6 W (180 mA @ 9 V). In comparison with our previous driver with RC charge/discharge signal shape, presented version increases air flow capability of micropumps from 1.6 sccm to 4.2 sccm. It enables driving of 200 µm thick PZT actuators with 12 nF capacitance.

Keywords: Piezoelectric micropump; driving module; slew-rate; dead-time

Krmilni modul piezoelektričnih mikročrpalk z nastavljivo hitrostjo spremembe in mrtvim časom krmilnega signala

Izvleček: V prispevku so predstavljeni razvoj, izvedba in meritve krmilnega modula piezoelektričnih mikročrpalk z nastavljivo hitrostjo spremembe in mrtvim časom krmilnega signala. Predstavljeni krmilni modul omogoča neodvisno nastavljanje nekaterih parametrov pravokotnega krmilnega signala kot npr.: frekvenca, pozitivna in negativna amplituda napetosti, hitrost dvižne in upadne spremembe, mrtvi čas in način delovanja (črpalni/ventilski).
Izdelani krmilni modul omogoča nastavljanje napetosti do 250 VPP na frekvenčnem področju do 1 kHz, pri hitrosti spremembe signala do 18 V/µs pri največji porabi 1.6 W (180 mA @9 V). V primerjavi s preteklimi izvedbami krmilnega modula, s kvazi-pravokotno obliko krmilnega signala, ki poustvarja RC polnjenje/praznjenje, smo povečali pretok mikročrpalk iz 1.6 sccm na 4.2 sccm. Izdelani modul omogoča krmiljenje PZT aktuatorja debelin do 200 µm in kapacitivnosti do 12 nF.

Ključne besede: piezoelektrična mikročrpalka; krmilni modul; hitrost spremembe krmilnega signala; mrtvi čas krmilnega signala.

** Corresponding Author's e-mail: matej.mozek@fe.uni-lj.si*

1 Introduction

Piezoelectric micropumps are often used in advanced microfluidic applications where accurate pressure, flow control and monitoring are required. In applications where small flow rate of ml/min range and lower is needed, they often represent the most appropriate solution due to their small size and low power consumption. In order to optimize the micropump flow rate and backpressure performance, piezoelectric actuator driving signal has to have appropriate signal shape, amplitude and frequency. Available drivers are often either large in size and therefore inappropriate for portable applications [1] or are optimized for driving a specific type of piezoelectric micropump. Most of them feature only a rectangular driving signal with fixed slew rate [2] and limited signal flexibility. Some drivers [3] offer energy recuperation, but they don't employ grounding one of micropump electrodes, which is prerequisite in medical applications. In our previous work [4] a three channel, high voltage analog linear amplifier was de-

veloped. Though this amplifier enables a detailed insight into micropump operation by covering different pump excitation signals, supplied by an arbitrary function generator, it is not size optimized. Recently [5], we implemented a miniature, transformerless version of a piezoelectric micropump driving module. It features two mutually exclusive switched mode power supply (SMPS) boost converters, with piezoelectric micropump actuator shared as a common output capacitor. This module offers synthesis of standard rectangular-like driving signal, which resembled an RC network charging/discharging through the piezoelectric micropump. Though such output signal shape is far from ideal, it is still suitable for cost sensitive applications. Analyzed results have shown a significant discrepancy in positive and negative driving amplitude, which has to be individually adjusted to particular type of piezoelectric actuator. To address these drawbacks, we present a novel, cost-effective, version of a miniature high voltage piezoelectric micropump driving module, which generates a true rectangular micropump driving signal with independently settable positive and negative driving signal amplitudes, slew-rate, dead-time and frequency.

In order to achieve these functionalities, a simplified high-voltage driving stage was designed. Usual approach is to design a D-class amplifier, with some type of high-side MOSFET driver (e.g. IR2113), which would enable driving with arbitrary shape of signals. On the other hand, it would require several additional components, which would compromise our low-cost approach. In our previous work [6] we have shown, that the most appropriate driving signal shape is square wave with settable frequency, duty cycle, both amplitudes and both slew rates. Low value of both slew rates yield a more trapezoid-like driving signal, which results in lower power consumption, but with a reduced flow-rate compared to steeper slew rate signal. In order to reduce overall driving module cost, the micropump high-voltage switching stage was designed using optocouplers, which significantly simplify the design, due to lack of a dedicated level-shifter stage for high-side switch and bootstrapping capacitor, found in high-side driver components.

2 Microcylinder pump

Recently presented microcylinder pump [7], was selected for a driver evaluation. Instead of employing check-valves, it operates on a principle of active sequential expansion (opening) and compression (closing) of the centrally placed inlet cylindrical rectifying element and outlet throttle rectifying element. Micropump expansion and compression are performed by an actuated glass membrane that is loosely attached via a resilient elastomer to the top of the supporting glass. Exploded view of a typical thermoplastic (TP) microcylinder pump structure with constituent materials and corresponding bonding processes is shown in Fig. 1.

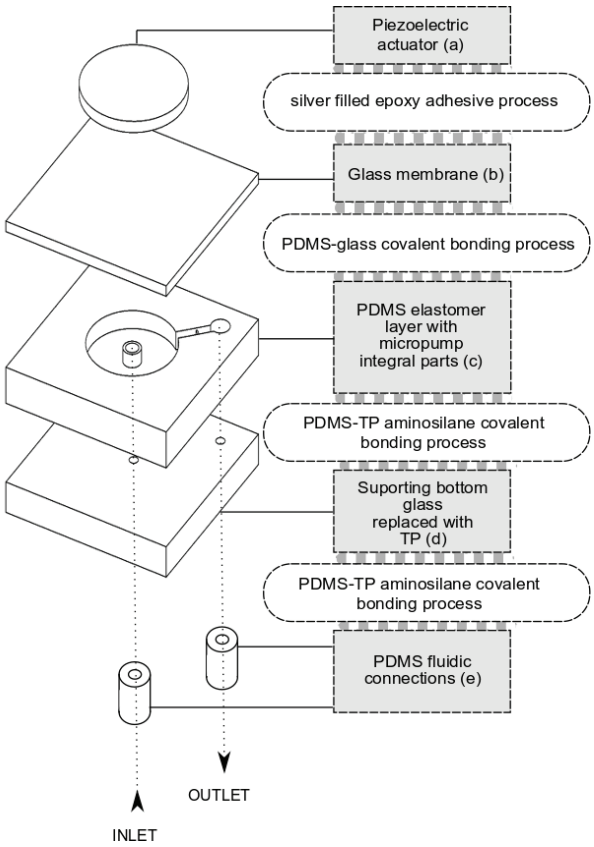


Figure 1: Exploded view of a typical TP microcylinder pump structure with constituent materials and corresponding bonding processes.

The TP microcylinder pump comprises polydimethylsiloxane (PDMS) elastomer layer with molded micropump chamber, fluidic microchannel and rectifying elements (Fig. 1 c). Additionally, two through-holes are punched into an elastomer, one into the center of the micropump chamber and the other one at the end of the channel. PDMS elastomer layer (Fig. 1 c) and PDMS fluidic connections (Fig. 7 e) are covalently bonded to the supporting TP substrate (Fig. 1 d) by employing developed amine-PDMS linker bonding process. One inlet and one outlet fluid port is drilled through a supporting TP substrate that supply and drain the fluid into and out of the pump. The micropump chamber and the microchannel are sealed with a thin glass membrane (Fig. 1 b) by employing oxygen plasma PDMS-glass covalent bonding process. Piezoelectric actuator (Fig 1 a) is positioned in the axis of a micropump chamber, coupled rigidly to the micropump membrane through silver filled epoxy adhesive (EPO-TEK EE129-4, Billerica, MA, USA).

3 Module operation

High voltage power supply section of the investigated circuit is designed around two independent boost SMPS power supplies, which provide micropump positive and negative driving voltage (Figure 1). Lower boost converter, comprised of inductance L2, transistor M2, diode D3 and capacitor C3, provides a source of negative micropump driving voltage, while the upper boost converter (comprised of inductance L1, transistor M1, diode D1 and capacitor C1) provides a source of positive micropump driving voltage. Each SMPS features a resistor divider feedback, which enables independent monitoring of both power supply voltage levels. Both SMPS converters are driven using pulse-width modulation (PWM) signal (see Figure 1, sources V1 and V2) with base frequency 32 kHz in range from 10% do 90%. Depending on duty cycle setting, both SMPS converters can deliver output voltage in range from ±10 V to ±150 V. Our previous designs did not allow independent setting of power supply voltage level, therefore the half period amplitude symmetry could only be achieved by adjusting the duty cycle of an individual switching half-cycle.

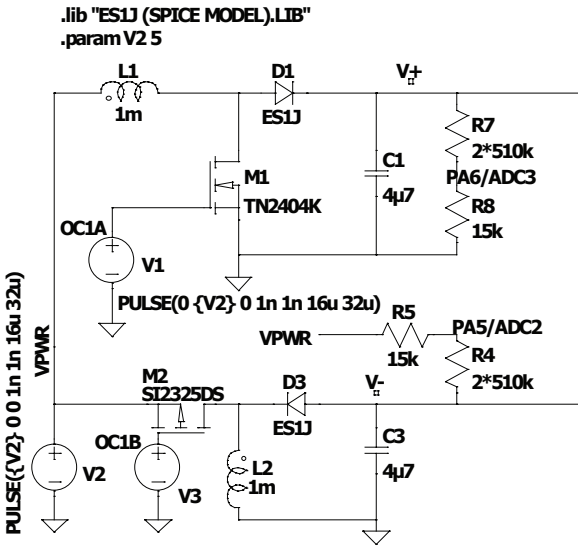


Figure 2: High-voltage part of the driver.

Both positive and negative supply voltages (Figure 1, V^+ and V^-) are connected to the micropump via two Darlington output high-voltage optocouplers TLP187 (Figure 2, circuit U1 and U2). Using such setup, frequency, duty cycle and slew-rate for front and rear micropump driving signal edge can be independently set. Slew rates can be digitally set using several microcontroller outputs, which effectively form a simple digital-to-analog converter. In Figure 2, only resistors SR_1 and SR_2 are shown for simplicity.

In order to generate an alternating rectangular-like excitation signal, positive (V+) and negative (V-) power supply are switched exclusively by driving signals V6 and V7. Both driving signals feature an obligatory, programmable dead time gap, which is downwards limited by optocoupler turn-off-time (80 µs for TLP187).

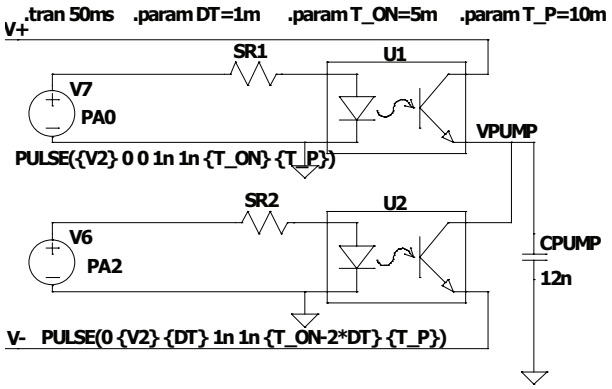


Figure 3: Excitation part of the driver.

4 Circuit simulations

Initial simulations of above described circuit were performed in LTSpice XVII [8]. In presented case, measured capacitance of piezoelectric (PZT) actuator C_0 was 12 nF, while the microcylinder pump excitation frequency was set at 100 Hz with 50% symmetry. Switching frequencies of both power supplies were set at 32 kHz and the PZT actuator driving voltage was recorded. Transient analysis of circuit, presented in Figure 3, was simulated for first 50 ms. Simulation results of micropump driving voltage rise at 100 Hz are shown in Figure 4.

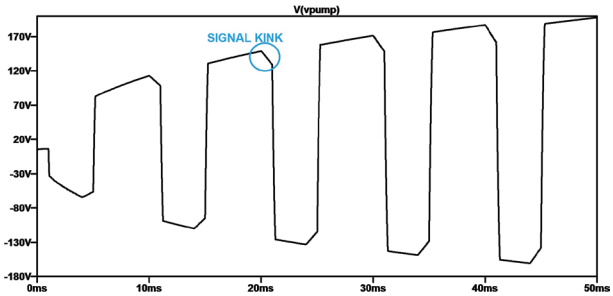


Figure 4: Piezoelectric micropump driving voltage build-up after first 50 ms of operation.

Simulation parameters, dead time (DT), positive half-cycle (T_ON) and period (T_P) are listed on the top of schematic in Figure 2.

Figure 3 shows a signal kink in square wave signal edge transition, which originates from dead-time, when no

optocoupler is driven and the micropump piezoelectric actuator is discharged. Excitation of two optocouplers was provided by two phase-exclusive signals (see Figure 4, V6 - dashed line and V7 - solid line) with dead time (DT) of 1 ms, on-time T_ON of 5 ms and a period T_P of 10 ms were applied in simulation (see top of Figure 3).

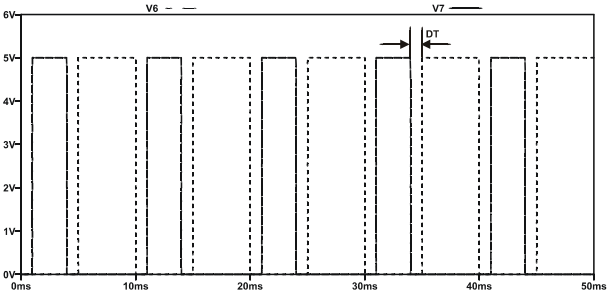


Figure 5: Optocoupler diode driving voltage after first 50 ms of operation.

Micropump switching period is divided into four states as follows: Active positive voltage driving state (solid line, Figure 5), during which positive SMPS power supply (V^+ on Figure 2) is connected to the micropump using optocoupler U1 (Figure 3), followed by a positive dead time state, where both optocouplers (U1, U2 in Figure 3) are turned off, superseded by a active negative driving state (dashed line, Figure 5), during which negative SMPS power supply (V^-, Figure 2) is connected to the micropump using optocoupler U2 (Figure 3), and finalized by a negative dead time state, where both optocouplers (U1, U2) are switched off. Splitting the micropump switching period into four independent states gives maximum control over micropump driving signal properties and module power consumption.

Increasing the value of optocoupler base resistors (SR1, SR2 in Figure 3) results in lower micropump driving signal slew-rates, which enables the selection between high-flow performance with high slew-rate, and low flow-performance mode with low slew-rate. Although a single resistor (SR1, SR2) is shown in Figure 3 for clarity, controlling signals V6 and V7 can be fed to the optocouplers via a network of resistors, connected to a multiplexed power source.

Multiplexing power supply via different base resistors enables seamless interchanging between performance modes and different signal shapes: When setting both slew-rates low (a single, high value resistor is fed to base), a sinewave-flanked signal (sinewave signal with time-extended flat extrema) can be obtained. Setting both slew-rates high by turning on multiple resistors results in a square wave signal. Setting rising edge slew rate high, and falling edge low results in the sinewave - rectangular signal (SRS signal).

5 Module control

Micropump control is based on a cost-effective 8-bit microcontroller, an ATMEL Tiny 104 in a 14-pin SOT-23 package [9].

Selected microcontroller features a single 8-bit timer (TMR0), which is configured to count using 8 MHz internal clock (no prescaler). Counter overflow interrupt is used for transitioning between active and dead-time stages by implementing a state-machine, which preloads next timer-expiration period based on corresponding stage duration. TMR0 state machine can also be configured in the "valve mode", in which either a constant positive or negative voltage is fed to the micropump. Microcontroller PWM unit is configured in "fast" (phase non-aligned) mode, with two output compare registers (OCR0A/OCR0B), running at 31.25 kHz with 8-bit resolution. PWM outputs (OC0A/OC0B), whose value results from comparison between OCR0x and TMR0 value, are connected to corresponding SMPS MOSFET transistor (M1, M2 Figure 2). Both PWM outputs operate in free-running mode. Each SMPS output is fed back to the corresponding microcontroller analog-to-digital converter input (ADC2/ADC3, Figure 2). An analog-to-digital converter interrupt is triggered by TMR0 interrupt routine only during positive and negative dead-time switching phase. During positive dead-time state, ADC2 is monitored, and the value of OCR0A is altered accordingly. During negative dead-time state, ADC3 is sampled, and the value of OCR0B is altered. Microcontroller UART receiver was used to set all micropump driving signal settings: frequency, positive and negative dead time, amplitudes, slew-rates and mode of operation (pump/valve). In order to minimize microcontroller calculations, an Excel VBA based script was developed. This script translates human-readable parameters such as frequency and dead time to TMR0 state-machine expiration periods, determines slew-rate resistor multiplexing state and configures the mode of module operation.

6 Initial prototype

In order to evaluate simulated circuit, initial prototype based on V_{PWR}= 5 V power supply, as shown in Figure 6, was designed and implemented.

Switching optocouplers PC817 (U1, U2 in Figure 3), which were used during simulations, were replaced with high-voltage, Darlington output type (Toshiba TLP187), due to better switching characteristics and high-current transfer ratio, which allows higher slew rates. Large (100 µF/100 V) rectifying capacitors (C1, C3

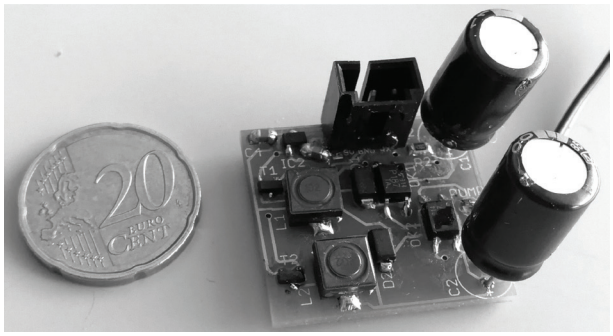


Figure 6: Initial driver prototype.

in Figure 2) were initially used to minimize the power supply ripple.

A LeCroy WaveRunner 64 Xi oscilloscope was connected to initial prototype in Figure 6. Tested module was driving the microcylinder micropump with PZT capacitance 12 nF. Both micropump signal driving extremes were tested:

1.) A "full drive" condition, with dead time set to DT = 200 µs, which sets driving micropump voltage almost for entire corresponding half-cycle (Figure 4).

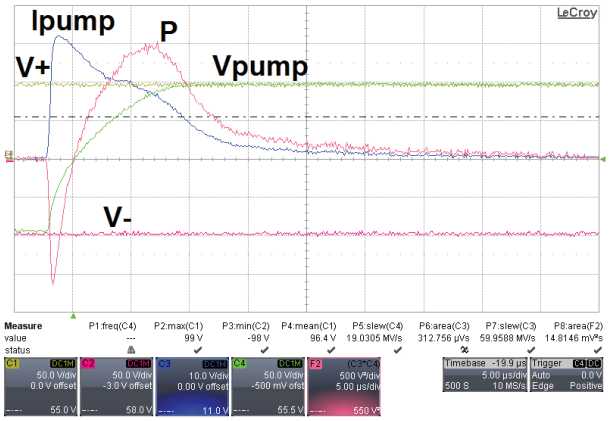


Figure 7: Initial prototype "full drive" front edge.

Figure 7 is showing the micropump "full drive" output signal front-edge detail at 100 Hz and 100 V amplitude. Actual achieved micropump power supply amplitudes was 98 V. The detail in Figure 7 also shows the micropump current (trace I_{PUMP}), measured as a voltage drop on a current-to-voltage op-amp circuit with a 100 Ω resistor. Micropump current achieves its peak value of 302 mA immediately after start of transition and then slowly decays towards zero in approximately 35 µs. A specific kink in the current decay is caused by Darlington transistor output. Area of current oscilloscope channel (micropump transition charge) was measured at 3.12 µAs. Oscilloscope was configured to measure the product of voltage and current and produce the micropump power (trace P, Figure 7). Although the micropump power peaks at approx. 16 W (Figure 7), its duration is only about 5 µs, therefore average power, delivered to the micropump in a half-period, is only 1.6 mW.

2.) A "minimum drive" condition on the other hand sets *only* 200 µs of driving time. Note that the dead-time (DT) during "minimum drive" condition is depending on the driving signal period (DT = T/2 - 200 µs). Time difference of 200 µs was selected to accommodate optocoupler on/off switching times and analog-to-digital converter conversion time in order to avoid shorting both optocouplers. Figure 8 shows the micropump "minimum drive" output signal of initial prototype at 100 Hz, ±100 V amplitude. After initial driving with amplitude ±98V for 200 µs (flat max/min part, Figure 8), the piezoelectric actuator voltage decays as an RC discharge down to 50 V. The decay RC time constant is independent of voltage polarity, but depends on the pumped media viscosity for particular pump construction.

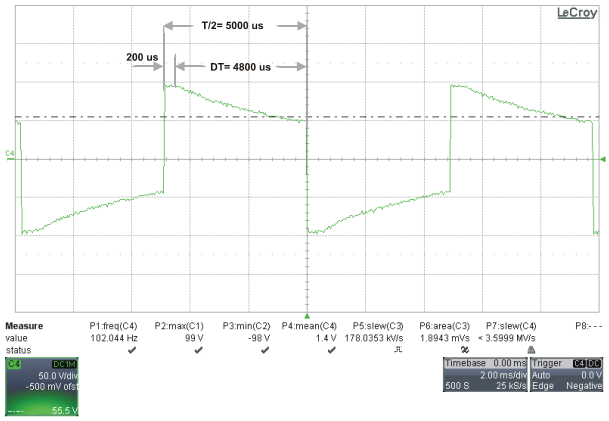


Figure 8: Initial prototype "minimum drive" micropump signal.

Micropump frequency was swept in the range from 50 Hz to 1 kHz in both "full drive" and "minimum drive" modes. Excel control software was set to maximum piezoelectric actuator voltage of 125 V. Actual positive and negative driving signal amplitudes, slew rates and power consumption were measured at each micropump frequency setting. Micropump amplitude vs. excitation frequency results are presented in Figure 9.

Micropump driving signal voltages were limited to ±125 V due to piezoelectric actuator limitations. In the low-frequency range (i.e. around 100 Hz), actual amplitudes of ±100 V were achieved.

Module current consumption I_{CC} is presented in Figure 10. At the target operating frequency of 100 Hz, in

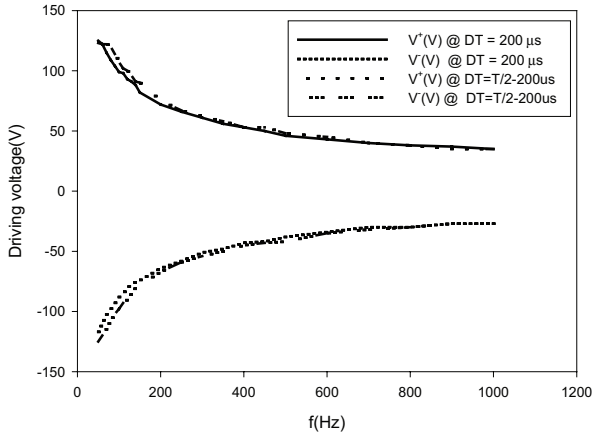


Figure 9: Voltage -frequency sweep of the initial prototype.

"full drive" mode with $SR^+ = SR^- = 11$ V/µs, module current consumption was 108 mA, afterwards the current consumption levels out. The majority of current consumption is attributed to high-voltage power supplies, which enter saturation, whenever their PWM duty cycle is clamped to a maximum value. Full driving voltage regulation frequency range can only be achieved up to a point, where actual voltage level becomes less than desired value. According to Figure 9, maximum piezoelectric voltage of 125 V can be set only in the range up to 70 Hz. Afterwards, due to increased output load, both high voltage power supplies achieve maximum admissible PWM duty cycle, resulting in ever lower actual driving voltage.

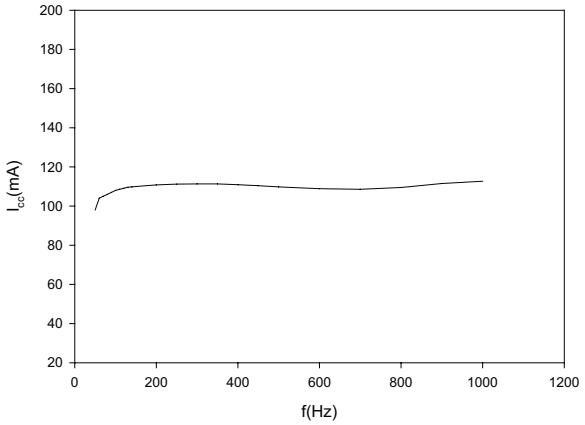


Figure 10: Current consumption of the initial prototype.

Figure 11 is showing positive and negative slew rate (SR^+ and SR^-, respectively), which were the most promising improvements in driving signal.

In comparison with our previous micropump driver designs [4, 5], which achieved typical slew rates of 200 V/*ms*, presented initial prototype exhibited slew rates in order of several V/*µs*. Frequency dependent decrease of both slew rates ($\Delta V/\Delta t$) is directly related to a decrease of driving voltage ($\Delta V = V^+ - V^-$), as shown in Figure 9. Although presented initial prototype exhibited a significant improvement in terms of slew-rate, it still *failed* to achieve maximum admissible driving signal amplitude of ±125 V @ 100 Hz.

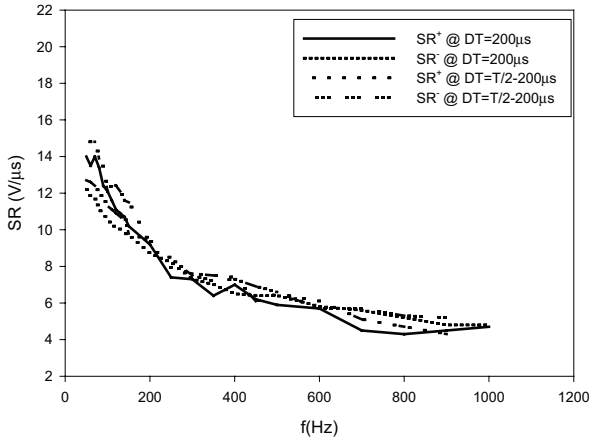


Figure 11: Positive and negative slew rate vs. frequency of the initial prototype.

7 Module improvement

In order to improve the micropump driving signal, power supply voltage regulation range would have to be extended over micropump excitation frequency. To achieve this, output voltage levels would have to be regulated at a lower PWM duty cycle setting on both high-voltage power supplies. First limitation in this process is the selected MOSFET on-resistance (typ. 4 Ω, for TN2404), which together with turn-on delay time (10 ns, TN2404) set the boost SMPS inductance range in order of mH, so output voltages in between 100 and 150 V can be achieved. Furthermore, the series resistance of applied inductor (Bourns, SRR0603, L1 and L2 on Figure 2) is typically 8 Ω and its maximum admissible DC current 200 mA. In our case, we limited the selection of transistor housings to SOT-23, to minimize the size of entire module. Consequentially abovelisted design limitations narrow the options only to an increase in SMPS input power supply voltage (V_{PWR}, Figure 2) from 5 V to 9 V. Microcontroller operates from a 5 V power supply, which was provided by additional linear regulator (MCP1703CB). Another modification was to use a dual power MOSFET driver (TC4427) as a voltage-level translator between 5 V PWM microcontroller outputs (OC1A/OC1B) and 9 V input power supply. Rectifying capacitors (C1, C3 Figure 2) were reduced from 100 µF

to 47 µF/ 100 V, which are available in Φ=6 mm footprint. As with initial prototype, the measurements were repeated under same conditions, only this time a 9 V power supply was used. Micropump amplitude vs. excitation frequency results are presented in Figure 12.

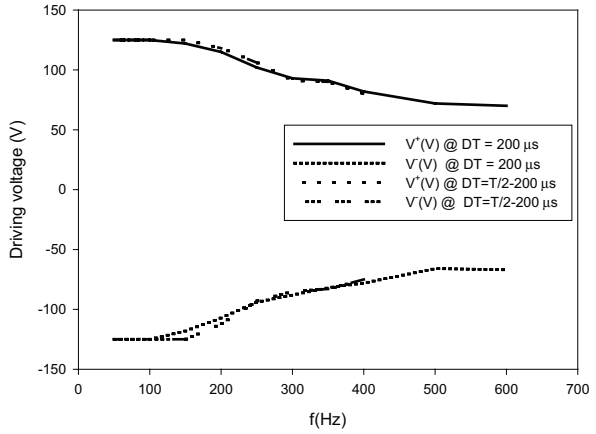


Figure 12: Voltage -frequency sweep of the improved prototype.

In low-frequency range, micropump driving signal reached admissible voltage limit of ±125 V. In comparison to the voltage scan of the initial prototype, the clamping interval extended from 70 Hz to 150 Hz. Such an improvement in driving signal amplitudes comes at a cost of an increased module current consumption I_{CC}, which is presented in Figure 13.

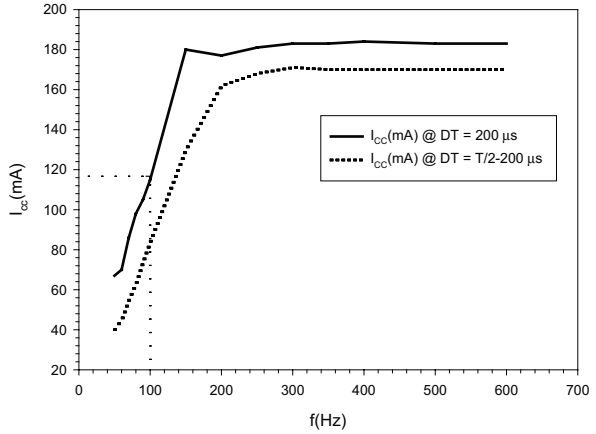


Figure 13: Current consumption of the improved prototype.

At the target operating frequency of 100 Hz, in "full drive" mode with $SR^+ = SR^- = 16$ V/µs, module current consumption was clamped to 118 mA, at 150 Hz the current consumption levels out to 180 mA. In "minimum drive" mode, the current consumption levels out at 170 mA. Due to 10 mA difference between "full" and "minimum" driving mode, the majority of current consumption is attributed to design of SMPS boost converters. Current consumption of 180 mA could be marginally extended to 200 mA due to SRR0603 inductance limitation. This was achieved by rising the power supply value from 9 V to 10.5 V. After that point, at 11 V, the switching optocouplers power dissipation limitation (150 mW) is exceeded.

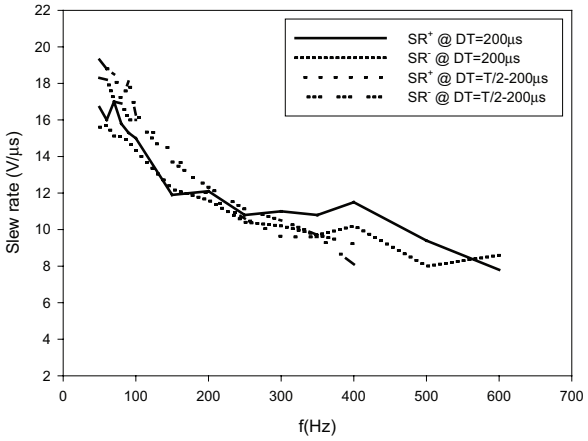


Figure 14: Positive and negative slew rate vs. frequency of the improved prototype.

Due to extended operation at maximum driving amplitude of ±125 V, shown in Figure 12, both slew rates also improved from initial 11 V/µs to 16 V/µs in "full drive" mode at 100 Hz, as depicted in Figure 14. In "minimum drive" mode, this value is even higher (18 V/µs). More important is the fact, that this slew rate remains over 10 V/µs up to 400 Hz, which enables testing of our microcylinder micropumps, with smaller (Φ= 6 mm) piezoelectric disc with capacitance of 4 nF. We also tested the ability for setting various slew-rates using different optocoupler base resistances. This feature can be applied, when slew rate is to be changed during operation. Such instance occurs during pump starting process, where a trapped bubble in the pumping chamber has to be expelled or when flow control is coarse-adjusted by altering the slew rate (Figure 22).

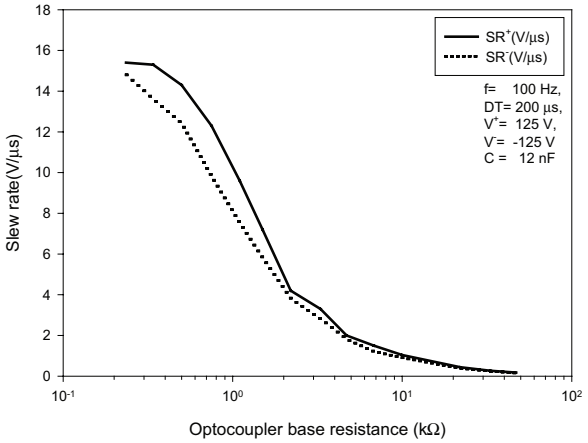


Figure 15: Driving signal slew-rates vs. optocoupler resistances.

Again, micropump excitation frequency was set to 100 Hz, with ±125 V amplitude and the driving module was configured in the "full drive" mode. Module current consumption was evaluated against slew rate. According to Figure 13 in "full drive" mode (dashed line), with 100 Hz and both slew-rates set to 16 V/µs, the module current consumption is 118 mA. Both slew rates and area measurements were calculated on-the-fly by the oscilloscope. Optocoupler base resistance was limited to 220 Ω due to microcontroller output driving capability. On the other hand, upper base resistance limit was set by driving signal shape. Whenever slew-rate fell below 1 V/µs, resulting signal became sinewave-flanked.

Module current consumption, shown in Figure 16, remains practically independent (125 mA in "full drive" mode) of slew-rate just to the point, where the slew-rate falls under 1 V/µs. An increase in current consumptions in "full drive" mode can be attributed to measurement error, since average current measurements at high slew rates are hard to establish, due to constantly changing SMPS duty cycle. Such a discrepancy could be rectified using a larger output capacitor. The majority of current consumption is attributed to both SMPS power sources. In "minimum drive" mode, the current consumption is reduced to 70 mA. Such "minimum drive" mode consequentially enables power-saving feature during operation with reduced flow. On the other hand, "full drive" mode with its high slew-rate improves the micropump purging (air pumping) capability.

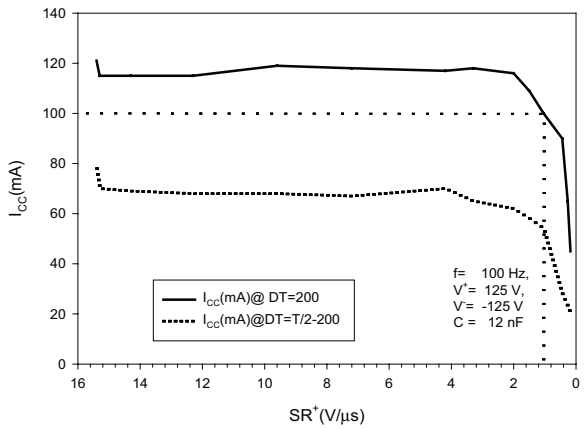


Figure 16: Power consumption vs. positive slew-rate.

Performed set of measurements was also repeated on our microcylinder micropump which uses a smaller piezoelectric disc with capacitance of 4 nF. Compared to 12 nF microcylinder micropump, the limit voltage (125 V) regulation area extended to 400 Hz. Both slew rates improved even more, reaching the levels of 22 V/µs in "full drive". Likewise, the current consumption in both modes, compared to Figure 13, reduced only slightly - 175 mA in "full drive" and 160 mA in "minimum drive" mode.

8 Fluidic characterization

After the initial micropump driver testing, the system for computer controlled characterization of piezoelectric micropumps was set up (Figure 17). Analyzed driving module was connected to tested microcylinder pump. DI water filled tank was connected on micropump input and pressure/flow evaluation equipment on its output.

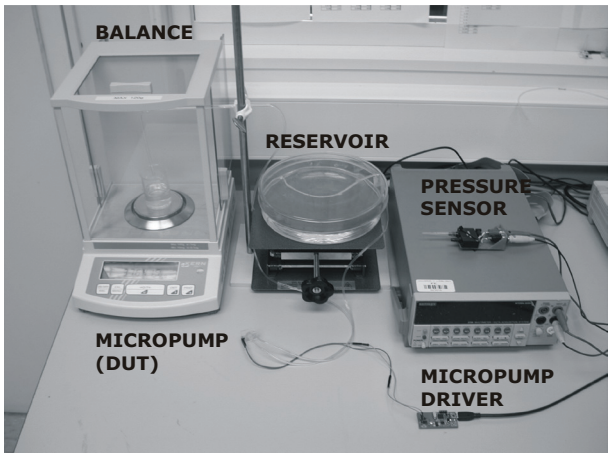


Figure 17: Measurement setup.

Micropump flow rate was measured using a Kern ABJ 120-4M precision balance. Presented micropump driving module was compared to previous driving modules, designed in our Laboratory [5]. These versions produce a rectangular signal with RC charge/discharge front and rear edge transitions (RC asymmetric driver). Our previous research of micropump performance on signal shape [6] has demonstrated better micropump flow and backpressure performance, when positive and negative voltage of RC signal are made symmetric (RC symmetric driver).

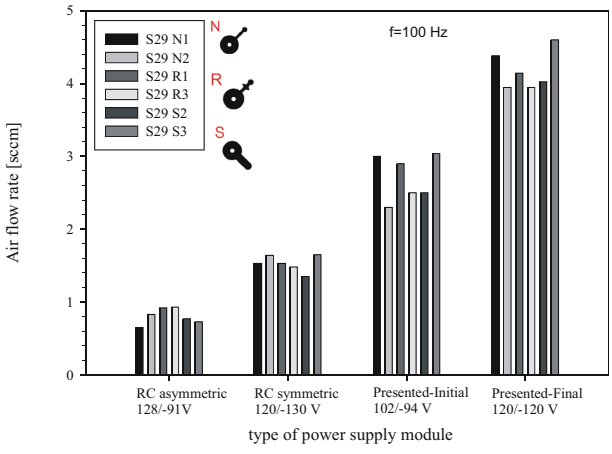


Figure 18: Air flow comparison of developed micropump driving modules.

Three distinct micropump designs (N, R, S), each with different outlet channel geometry, were compared using RC asymmetric/symmetric driver and both initial and final version of the presented driver. Air flow rate (Figure 18) and DI water flow rate (Figure 19) measurements were performed at 100 Hz, while the presented driver was configured in "full-drive" mode in both initial and final version.

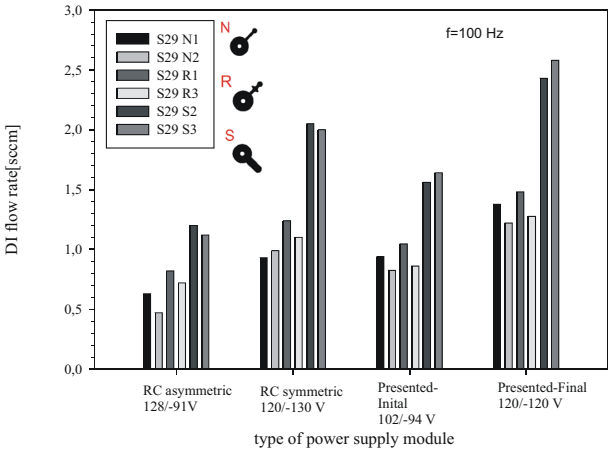


Figure 19: DI water flow comparison of developed micropump driving modules.

While both presented driver versions perform significantly better than previous ones, especially final version of presented driver dominates the air pumping, where it significantly increases the air flow rate (from 1.6 sccm to 4.2 sccm) in comparison with symmetric RC driver.

Compared with symmetric and asymmetric versions of RC-like driver, presented driver surpasses all previous performances. Flow rate increase for DI water from 2.2 sccm to 2.6 sccm is not so substantial.

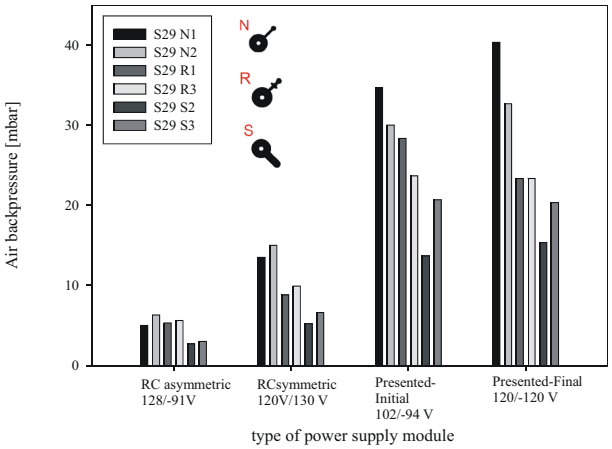


Figure 20: Air backpressure comparison of developed micropump drivers.

Both versions of presented driver almost doubled air backpressure performance, compared to both RC type drivers (see Figure 20). Final driver version is achieving its peak value of 39 mbar on N1 type micropump in "full drive" mode.

Final version of presented driver improved DI water backpressure of initial version by 30%, achieving its peak value of 240 mbar on N1 type micropump (see Figure 21). Both presented versions improved DI water backpressure performance over RC-type drivers.

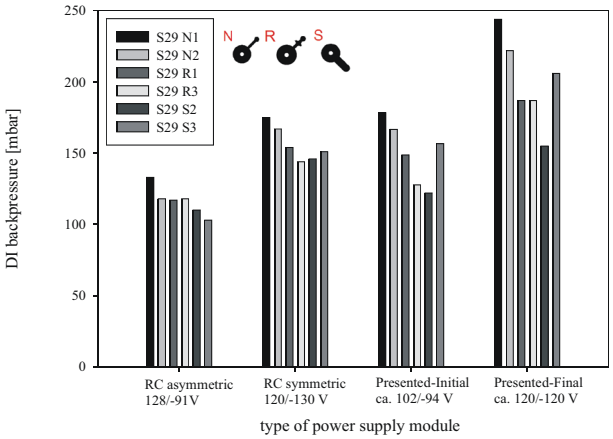


Figure 21: DI water backpressure comparison of developed micropump drivers.

Final version of presented driver was configured in "full drive" mode and amplitudes were set at ±105 V at 100 Hz using the micropump S29R1. DI water and air flow rate were measured, while both slew-rate values were adjusted. Results in Figure 22 show that flow rate in both cases is practically independent of slew-rate (only SR^+ displayed). Backpressure characteristics, depicted in Figure 23, deteriorate with slew rate less than 4 V/µs. If slew-rate is lowered down to 1 V/µs, maximum flow rate can be achieved, with reduced power consumption to 100 mA (see Figure 16). Even with slew rate

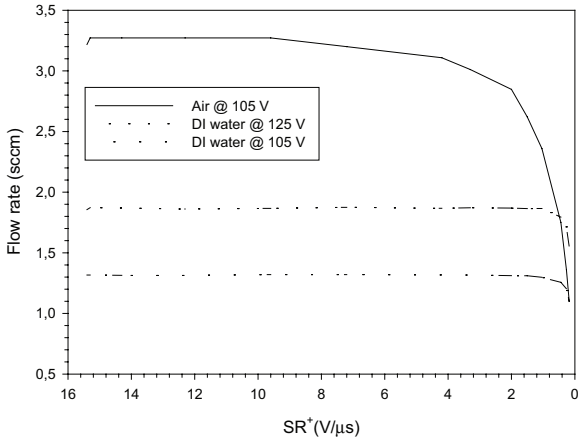


Figure 22: Flow rate vs. slew rate in "full drive" mode.

kept at 1 V/µs, resulting flow rate is significantly larger compared to our previous RC driving modules, which achieved slew rates of 200 V/ms. Power consumption can be further reduced using "minimum drive" mode.

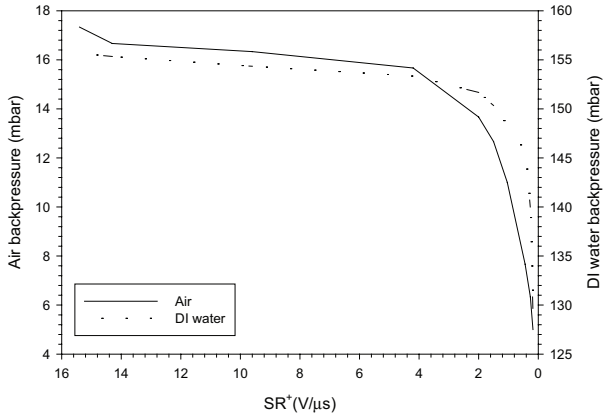


Figure 23: Backpressure vs. slew-rate in "full drive" mode.

Despite the fact, that keeping slew-rate in range of 16 V/µs has no significant influence on flow rate and backpressure characteristics, we believe that higher slew-rate improves other micropump characteristics such as self-priming and bubble tolerance and makes the micropump operation more reliable in different operating conditions.

9 Conclusion

Design and characterization of an advanced piezoelectric micropump driver with programmable slew-rate and dead-time for driving custom made piezoelectric micropumps was presented. Developed driver enables independent setting of several rectangular output signal parameters, such as frequency, positive and negative amplitude, slew-rates, dead time, and modes of operation (pump/valve).

Driving signal frequency range from several Hz to 1 kHz was investigated. Amplitudes up to 250 V_{pp} were achieved in lower frequency range (up to 150 Hz). In this lower frequency range, positive and negative signal slew-rates up to 18 V/µs were achieved. Optimal micropump actuation frequency range from 50 to 400 Hz was found using DI water. In comparison with our previous driver designs with RC charge/discharge signal shape, presented version increases air flow capability of micropumps from 1.6 sccm to 4.2 sccm. Maximum module power consumption was 1.6 W (180 mA @ 9 V). Presented module is capable of driving a 200 µm thick piezoelectric actuator with a capacitance in order of several nF. Small size of (25 mm x 25 mm x 5 mm) makes presented driver suitable for integration inside micropump housing.

In order to further investigate the impact of slew-rate on micropump reliability, other characteristics, such as self-priming and bubble-tolerance, should be measured.

10 Acknowledgements

This work was performed within the framework of a project supported by the Slovenian industrial partner KOLEKTOR Group and the Ministry of Education, Science, Culture and Sport (Grant No P2-0244).

11 References

1. "Bartels mp-x Controller", http://www.bartels-mikrotechnik.de/index.php/produkte/elektronik, [Accessed: 18. 7. 2019],
2. "Bartels mp6-OEM Controller", http://www.bartels-mikrotechnik.de/index.php/produkte/elektronik, [Accessed: 18. 7. 2019],
3. C. Chao, P. Huang, M. Chen, L. Jang, »Design and analysis of charge-recovery driving circuits for portable peristaltic micropumps with piezoelectric actuators« *Sensors and actuators. A, Physical,* 2011, vol. 168, pp. 313–319, https://doi.org/10.1016/j.sna.2011.04.027
4. M. Antonijevič, T. Dolžan, B. Pečar, U. Aljančič, M. Možek, D. Vrtačnik, D. Resnik, S. Amon, "Characterization system for piezoelectric micropumps", in *Conference 2012 proceedings 48th International Conference on Microelectronics, Devices and Materials & the Workshop on Ceramic Microsystems, September 19 - September 21, 2012, Otočec, Slovenia.* Ljubljana: MIDEM - Society for Microelectronics, Electronic Components and Materials, pp. 357-362,
5. M. Možek, B. Pečar, U. Aljančič, D. Resnik, D. Vrtačnik, "Low-power piezoelectric micropump driving module", in *Conference 2017 proceedings /53rd International Conference on Microelectronics, Devices and Materials & the Workshop on Materials for Energy Conversion and their Applications: Electrocalorics and Thermoelectrics*, October 4 - October 6, 2017, pp. 157-162,
6. D. Resnik, B. Pečar, M. Možek, N. Lokar, D. Vrtačnik, *Analyses of micropump performances under rigorous operating conditions.* Conference proceedings 2018, in *Conference 2018 proceedings 54th International Conference on Microelectronics, Devices and Materials & the Workshop on Sensors and Transdu-*

cers, October 3 - October 5, 2018, pp. 49-52,
7. T. Dolžan, B. Pečar, M. Možek, D. Resnik, D. Vrtačnik, »Self-priming bubble tolerant microcylinder pump«. *Sensors and actuators. A, Physical,* 2015, vol. 233, pp. 548-556, http://dx.doi.org/10.1016/j.sna.2015.07.015
8. LTSPICE, Linear Technologies: http://ltspice.linear-tech.com/software/LTspiceXVII.exe, 16.7.2019
9. 8-bit AVR Microcontroller ATtiny102 / ATtiny104 Datasheet complete: http://ww1.microchip.com/downloads/en/devicedoc/atmel-42505-8-bit-avr-microcontrollers-attiny102-attiny104_datasheet.pdf, [Accessed: 15. 7. 2019]

Arrived: 25. 07. 2019
Accepted: 02. 09. 2019

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 49, No. 2(2019), 113 – 115

Doktorske disertacije na področju mikroelektronike, elektronskih sestavnih delov in materialov v Sloveniji v letu 2018

Doctoral theses on Microelectronics, Electronic Components and Materials in Slovenia in 2018

Univerza v Ljubljani / University of Ljubljana

Fakulteta za elektrotehniko / Faculty of Electrical Engineering

1	Avtor Author	Klemen Strojan		
	Naslov	**Proteomska karakterizacija nanodelcev za ovrednotenje njihove citotoksičnosti in imunotoksičnosti ter razvoj novih vrst nanodelcev**		
	Title	Proteomic characterization of nanoparticles for evaluation of their cytotoxicity, immunotoxicity and development of new types of nanoparticles		
	Mentor Supervisor	Viš. zn. sod dr. Mojca Pavlin	Somentor Co-Supervisor	Znan. sod. dr. Vladimir B. Bregar

2	Avtor Author	Jaka Ogorevc
	Naslov	**Sledljivost do mednarodnega sistema enot v biomedicinski merilni instrumentaciji**
	Title	Traceability to SI in biomedical measuring instrumentation
	Mentor Supervisor	Prof. dr. Janko Drnovšek

3	Avtor Author	Aljaž Kramberger
	Naslov	Avtonomno učenje robotskih operacij v kontaktu z okolico
	Title	**Autonomous learning of robot actions in contact with the environment**
	Mentor Supervisor	Izr. prof. dr. Aleš Ude

4	Avtor Author	Tadeja Forjanič
	Naslov	**Modeliranje biološkega odziva na elektroporacijo v elektrokemoterapiji in genski terapiji**
	Title	Modeling the biological response to electroporation for electrochemotherapy and gene therapy
	Mentor Supervisor	Prof. dr. Damijan Miklavčič

5	Avtor Author	Dejan Knez		
	Naslov	Računalniško podprto načrtovanje in analiza vstavitve pedikularnih vijakov na podlagi medicinskih slik hrbtenice		
	Title	**Computer-assisted design and analysis of pedicle screw placement based on medical images of the spine**		
	Mentor Supervisor	Izr. prof. dr. Tomaž Vrtovec		

6	Avtor Author	Kristina Bašnec		
	Naslov	**Termokromni indikatorji temperaturnega nihanja živil v hladni verigi**		
	Title	Thermochromic indicators of temperature abuse in cold food chain		
	Mentor Supervisor	Izr. prof. dr. Marta Klanjšek Gunde	Somentor Co-Supervisor	Prof. dr. Peter Raspor

5	Avtor Author	Nasr Hassan Khedr Gad
	Naslov	Načrtovanje širokopasovnih ravninskih tiskanih anten z necelimi ravninami mase za večpasovno uporabo
	Title	**Design of wideband planar printed antennas using defected ground structures for multiband applications**
	Mentor Supervisor	Prof. dr. Matjaž Vidmar

Univerza v Mariboru / University of Maribor

Fakulteta za elektrotehniko, računalništvo in informatiko / Faculty of Electrical Engineering and Computer Science

1	Avtor Author	Robert Brezovnik
	Naslov	**Vpliv preklopne frekvence sistema za uporovno točkovno varjenje na varilni tok in na izgube**
	Title	The impact of switching frequency of a resistance spot welding system on welding current and power losses
	Mentor Supervisor	Izr. prof. dr. Jožef Ritonja

2	Avtor Author	Andraž Javernik
	Naslov	**Hitri merilni sistemi na osnovi Fabry-Perotovih interferometrov**
	Title	High-speed Fabry-Perot sensor interrogation system
	Mentor Supervisor	Prof. ddr. Denis Đonlagić

3	Avtor Author	Dunja Srpak		
	Naslov	Vplivi proizvodnje vetrnih elektrarn na načrtovanje regulacijske rezerve		
	Title	**The impact of wind-power generation on the planning of regulating reserve**		
	Mentor	Izr. prof. dr. Josip Voršič	Somentor	Izr. prof. dr. Boštjan Polajžer
	Supervisor		Co-Supervisor	

4	Avtor Author	Primož Sukič
	Naslov	**Fotonapetostne elektrarne kot vodeni aktivni členi razdeljevalnih omrežij**
	Title	PV systems as controlled active elements of distribution networks
	Mentor Supervisor	Prof. dr. Gorazd Štumberger

Mednarodna podiplomska šola Jožefa Stefana / Jožef Stefan International Postgraduate School

1	Avtor Author	Lovro Fulanović		
	Naslov	**Relaxor-ferroelectric-based ceramic multilayer elements for viable electrocaloric cooling**		
	Title	Keramični večplastni elementi na osnovi relaksorskih feroelektrikov za izvedljivo elektrokalorično hlajenje		
	Mentor	Prof. dr. Barbara Malič	Somentor	Prof. dr. Vid Bobnar
	Supervisor		Co-Supervisor	

Bold font is used for the original title of the thesis (and language in which the thesis is written), normal font for title translation.

Boards of MIDEM *Society* | *Organi društva* MIDEM

MIDEM *Executive Board* | *Izvršilni odbor* MIDEM

President of the MIDEM Society | Predsednik društva MIDEM
Prof. Dr. Marko Topič, University of Ljubljana, Faculty of Electrical Engineering, Slovenia

Vice-presidents | Podpredsednika
Prof. Dr. Barbara Malič, Jožef Stefan Institute, Ljubljana, Slovenia
Dr. Iztok Šorli, MIKROIKS, d. o. o., Ljubljana, Slovenija

Secretary | Tajnik
Olga Zakrajšek, UL, Faculty of Electrical Engineering, Ljubljana, Slovenija

MIDEM Executive Board Members | Člani izvršilnega odbora MIDEM
Darko Belavič, HIPOT-RR d.o.o., Otočec, Slovenia
Dr. Slavko Bernik, Jožef Stefan Institute, Ljubljana, Slovenia
Dr. Miha Čekada, Jožef Stefan Institute, Ljubljana, Slovenia
Prof. DDr. Denis Đonlagič, UM, Faculty of Electrical Engineering and Computer Science, Maribor, Slovenia
Prof. Dr. Leszek J. Golonka, Technical University Wroclaw, Poland
Dr. Vera Gradišnik, Tehnički fakultet Sveučilišta u Rijeci, Rijeka, Croatia
Leopold Knez, Iskra TELA d.d., Ljubljana, Slovenia
mag. Mitja Koprivšek, ETI Elektroelementi, Izlake, Slovenia
Prof. Dr. Miran Mozetič, Jožef Stefan Institute, Ljubljana, Slovenia
Prof. Dr. Janez Trontelj, UL, Faculty of Electrical Engineering, Ljubljana, Slovenia
Dr. Danilo Vrtačnik, UL, Faculty of Electrical Engineering, Slovenia

Supervisory Board | Nadzorni odbor

Prof. Dr. Franc Smole, UL, Faculty of Electrical Engineering, Ljubljana, Slovenia
prof. dr. Drago Strle, UL, Faculty of Electrical Engineering, Ljubljana, Slovenia
Igor Pompe, Ljubljana, Slovenia

Court of honour | Častno razsodišče

Darko Belavič, Slovenia
Dr. Marko Hrovat, Slovenia
Dr. Miloš Komac, Slovenia

Informacije MIDEM
Journal of Microelectronics, Electronic Components and Materials
ISSN 0352-9045

Publisher / Založnik:
MIDEM Society / Društvo MIDEM
Society for Microelectronics, Electronic Components and Materials, Ljubljana, Slovenia
Strokovno društvo za mikroelektroniko, elektronske sestavne dele in materiale, Ljubljana, Slovenija

www.midem-drustvo.si