ISSN 0352-9045

Informacije MIDEM

Journal of Microelectronics, Electronic Components and Materials
Vol. 55, No. 4(2025), December 2025

Revija za mikroelektroniko, elektronske sestavne dele in materiale
letnik 55, številka 4(2025), December 2025

UDK 621.3:(53+54+621+66)(05)(497.1)=00 ISSN 0352-9045

Informacije MIDEM *4-2025*

Journal of Microelectronics, Electronic Components and Materials

VOLUME 55, NO. 4(196), LJUBLJANA, DECEMBER 2025 | LETNIK 55, NO. 4(196), LJUBLJANA, DECEMBER 2025

Published quarterly (March, June, September, December) by Society for Microelectronics, Electronic Components and Materials - MIDEM.

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Design | Oblikovanje: Snežana Madić Lešnik; Printed by | tisk: Biro M, Ljubljana; Circulation | Naklada: 1000 issues | izvodov; Slovenia Taxe Percue | Poštnina plačana pri pošti 1102 Ljubljana

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
vol. 55, No. 4(2025)

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Original scientific paper
https://doi.org/10.33180/InfMIDEM2025.401

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Journal of Microelectronics,
Electronic Components and Materials
Vol. 55, No. 4(2025), 201 – 217

Design and analysis of Low power Rapid Charge Holding Dynamic Latched Comparator

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Abstract: The need for portable devices with high precision has raised the demand for optimization of power and delay in various dynamic comparator topologies. In this paper, an efficient architecture that does timely yet rapid comparison with reduced power dissipation and optimal energy per comparison is proposed. Introducing an extra tail transistor in preamplifier of comparator, assists in holding the high gain, thereby reducing delay as well as power. The latch is meanwhile ready with a minimum threshold value at its output nodes with the help of a pass transistor in between latch output nodes. The conventional, hybrid, and proposed architecture, namely Low power Rapid Charge Holding Dynamic Latched Comparator (LRCHDLC) are simulated and verified for power, delay, and energy efficiency in Cadence Virtuoso Spectre. The proposed technique shows a significant improvement in delay and power consumption when compared to conventional comparators. Monte Carlo simulation shows that the proposed technique is robust to the process mismatch, sustaining optimal power, delay and energy efficiency.

Keywords: Average Power consumption, Latch regeneration delay, Hybrid Dynamic Latched Comparator, Rapid Charge holding Latched comparator

Oblikovanje in analiza dinamičnega komparatorja z zapahom z nizko porabo energije in hitrim polnjenjem

Izvleček: Potreba po prenosnih napravah z visoko natančnostjo je povečala povpraševanje po optimizaciji moči in zamika v različnih dinamičnih topologijah komparatorjev. V članku je predlagana učinkovita arhitektura, ki omogoča pravočasno in hkrati hitro primerjavo z zmanjšano porabo energije. Dodajanje dodatnega repnega tranzistorja v predojačevalnik komparatorja pomaga ohraniti visoko ojačenje, s čimer se zmanjša zakasnitev in poraba energije. Zapah je medtem pripravljen z minimalno mejno vrednostjo na izhodnih vozliščih. Konvencionalna, hibridna in predlagana arhitektura, imenovana Low power Rapid Charge Holding Dynamic Latched Comparator (LRCHDLC), je simulirana in preverjena glede moči, zakasnitve in energetske učinkovitosti v Cadence Virtuoso Spectre. Predlagana tehnika kaže znatno izboljšanje zakasnitve in porabe moči v primerjavi s konvencionalnimi komparatorji. Simulacija Monte Carlo kaže, da je predlagana tehnika odporna na neskladje procesov, pri čemer ohranja optimalno moč, zakasnitev in energetsko učinkovitost.

Ključne besede: Povprečna poraba energije, zakasnitev regeneracije zapaha, hibridni dinamični komparator z zapahom, hitro polnjenje

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How to cite:
J. V. S. Thirunavukkarasu et al., "Design and analysis of Low power Rapid Charge Holding Dynamic Latched Comparator", Inf. Midem-J. Microelectron. Electron. Compon. Mater., Vol. 55, No. 4(2025), pp. 201–217

1 Introduction

Miniaturization and portability in electronic products are highly demanded in an environment of rapid technological growth. The efficiency of any electronic system is reflected in the individual performance of every subsystem within the product. The efficacy of a comparator is reflected in the efficacy of the whole system and any device that employs it as a subcomponent. The need for high speed, low power and low offset has increased due to the demand for highly precise and fast Analog to Digital Conversion units, Operational Transconductance Amplifiers, voltage references, feedback amplifier setups and many other consumer electronic products. Comparators can be broadly classified into static and dynamic topologies. In general, Static comparators which offers high power consumption and slow switching during latch regeneration phase are of less priority. In contrast Dynamic comparators are widely preferred since they offer better switching speed and low power consumption through positive feedback. Dynamic comparators are further categorized into single tail and double tail comparators. Single tail dynamic comparators offer optimized delays, notable offset voltage, and high dynamic power consumption. Due to single tail current path, the kickback noise is high. Most preferred parent topology of single tail comparator, namely strong-arm latch is highly influenced by the range of V_{CM} values. An advanced version and alternative to this is the double tail dynamic latched comparator. The double tail dynamic comparators incorporate two tail transistors, weakening the coupling between the preamplifier output and the outputs of the latch. Double tail comparators offer significant reduction in kickback noise due to two separate current paths which further optimize power and delay in its conventional as well as various architectures. Topological changes for power and delay optimization require a preamplifier that not only amplifies the input voltages with enough gain but also that consumes low power by remaining dormant during evaluation phase. Every topological change must ensure that the necessary output swing will be fed to latch at an appropriate time lapse for comparison. Also, the topological changes in latch always aim at a timely comparison of the preamplifier outputs with optimized power intake and less voltage headroom. Most of the comparator topologies fail to either provide a full swing output at an instant when comparison occurs or consumes power during evaluation phase.

The trade-off between power and offset, delay and kickback noise need to be counterbalanced with architectural innovations. Beyond a superseded phase of unending circuit topologies, in alteration to existing CMOS technology, emerging devices like FinFETs, TFETs, Nanosheet transistors, and Nanowires assist in fast switching and low power consumption.

2 Related works

Ata Khorami [1] has proposed a low offset low power comparator that extends full swing output of the first stage for effective comparison. Their proposed preamplifier consumes less power in addition to fast decision making for lower common mode voltages. Also, When V_{CM} values are higher, latch activation becomes complex and influences the delay even though latching process is made easy. Latch topologies that rely on positive feedback, especially sense amplifier type-based latches are usually dependent on common mode voltages despite offering low offset voltages [2]. Savani [3] embedded a pass transistor between the output nodes of latch to sustain the NMOS transistors of the cross connected inverters receive its threshold voltage. Hence the time lapse for the outputs of the preamplifier to discharge is decreased. The time taken for latch initiation is also reduced, resulting in a delay of 51 ps and power consumption of 33 µW. Uneven charging of preamplifier output nodes results in static power consumption, which is avoided in their proposed work by the inclusion of pass transistor in between the output nodes.

One of the vital reasons for kickback noise is the capacitive coupling between the output nodes of the first stage and the input transistors of the second stage. This can be eliminated when the output nodes of preamplifier are cross coupled to pull up pair, which also reduces power dissipation at the time of evaluation phase. A significant delay reduction is achieved by cascading the input transistors and latch of second stage. [4]

To address the kick back noise reduction, yet another modified latch [5] with a wider path resulting in both output nodes in same state is recorded. This architecture cuts off the direct coupling between the outputs of first stage and the inputs of second stage thus resulting in reduced kickback noise with negligible counter effect on delay. Meanwhile, this topology increases the intermediate output nodal resistance thereby significantly reducing the power consumption.

Many architectures show a significant reduction in performance parameters especially power and delay, by modifying conventional preamplifier topologies [6] [7] [8], latch topologies [9], adding intermediate stages to minimize noise [10] and few architectures that neglect either of the stages and introducing compensatory combined architectures [11]

Introducing transistors (with specific bias) parallel to latch inputs makes the first stage consume power for only a short period of entire evaluation phase [12]. These architectures are designed for applications where low power is prioritized over speed. Topological improvisations have always demonstrated a trade-off amongst the performance metrics, mostly between power and delay. Using heuristic algorithms, it is validated in [9] that power and CMOS scaling have tradeoff with delay and offset, respectively.

Numerous architectures have been proposed to avoid static power consumption in either reset or comparison phase. Whenever extra transistors are introduced to improve comparison speed or minimize power consumption, reduced power generates counter-effects leading to significant rise in delay and vice versa. Notable single stage architecture [14] links the latch through preamplifier currents rather than voltage. It is driven by a clock and a delayed version of the same clock that improves latching speed. Introducing currents to the latch nodes reduces both power and the number of transistors significantly. Delayed clock and specific time sequence can also be achieved by introducing control gates [15].

Most of the recorded literature proves to improve one of the performance metrics compromising the other. The tradeoff between power and delay is seen in most of the comparators where topological changes are made in either preamplifier or latch. For applications that demand less operating voltage, regenerative type comparators with doubled transistor latch with two fully NMOS / PMOS based preamplifiers are used. This avoids completely charging and discharging of the output nodes of preamplifier reflecting a significant reduction in power concurrently increasing the speed of latch [19].

An effective topology is required to overcome these drawbacks without significant increase in area and counter effects like kickback noise. In this paper, a topology that helps reduce delay and power consumption during nodal charging and discharging of preamplifier as well as latch is proposed. The modified preamplifier and latch in tandem help in avoiding complete charging and discharging of all the output nodes during every clock transition. The proposed comparator has made a noteworthy effort to diminish power consumption by holding the minimum required charge at latch output nodes that negotiates charging and discharging time. Section 3 describes the working of the basic conventional double tail comparator and its transient response. Section 4 describes the working and circuit implementation of the proposed architecture, Low power Rapid Charge Holding Dynamic Latched Comparator (LRCHDLC) and its parent architecture, Hybrid Dynamic Latched Comparator HDLC. Section 5 describes the analysis of performance metrics with its sub sections describing the detailed analysis of delay, power and energy efficiency. Subsection 5.1.1 & 5.1.2 includes mathematical analysis of delay of the conventional comparator and proposed comparator respectively. The analysis of performance metrics with V_{CM} and V_{DIFF} is presented in section 5.1.3. Section 6 describes the comparison of the performance metrics of the proposed architecture with existing literature, process corner, influence of transistor sizing ratio, Monte Carlo analysis for various performance parameters, summary of results and key advantages. With progressive simulation results, it can be observed that there is simultaneous improvement in delay and power with minimal trade off. Section 7 concludes the paper.

3 Conventional double tail dynamic latched comparator

Figure 1 shows the topology of conventional dynamic latched comparator [7], and its transient response can be seen in Figure 2. The comparator works on recharging its intermediate and output nodes during the reset phase and performs the comparison during evaluation phase. No direct coupling of intermediate output nodes to the input terminals in conventional topology makes it more resistant to kickback noise and, this architecture lowers offset voltage. Preamplifier and latch circuits have lesser and larger tail currents respectively, thereby accomplishing lower offset voltage and high speed.

During the precharging phase where the clock is high and the clock bar is low, M_5 remains off thereby ensuring no static power consumption. In the case of the latch circuitry, the pull-down transistors M_{10} and M_{13} fed by clock turn on, forming a path for the output nodes with temporarily available charges to drain to ground. The pull up network M_1 and M_2 of the first stage fed by clock bar, turns on and charges the nodes F_n and F_p to V_{DD}. At the end of precharging phase, the preamplifier output nodes F_n and F_p are at V_{DD} and the latch output nodes out_n and out_p are at ground.

During the decision-making phase, the clock is low, and the clock bar is high. Also, with inputs fed, the tail transistor of the preamplifier turns on creating a path for the output nodes F_n / F_p to discharge.

Depending upon the ratio of input values, the output nodes discharge with different proportions. For example, when $V_{inp}>V_{inn}$, F_p discharges faster than F_n. Once

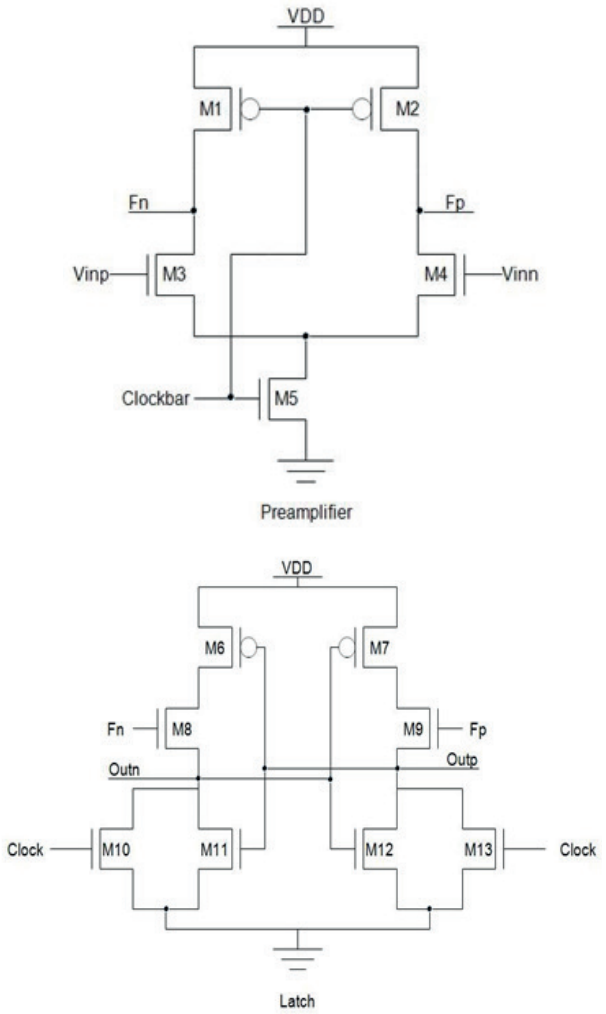

Figure 1: Conventional architecture

the charge at the output nodes of the preamplifier reaches the threshold of pull up transistors of latch circuit, latching is initiated. Meanwhile, in the latch circuit, the pull-down transistors M_{10} and M_{13} fed by clock turn off and both the pull-down transistor of cross connected inverter is activated resulting in latching. Latching

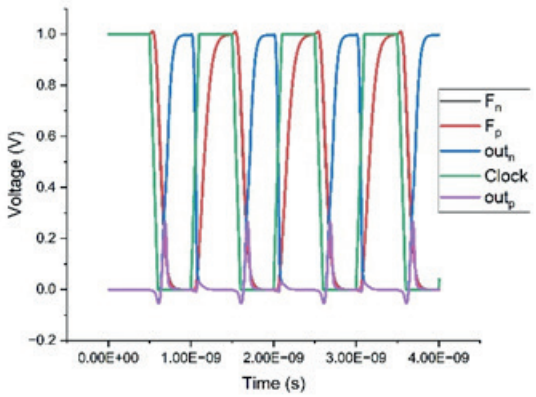

Figure 2: Transient Response of Conventional architecture

results in one of the output nodes of the latch pulled high and the other pulled down to zero.

4 The proposed comparator

The proposed comparator shown in Figure 3 is the Hybrid Dynamic Latched Comparator (HDLC) combining the principles of shared charge reset [2] and charge sharing techniques [3]. Figure 5 shows the proposed architecture Low-power Rapid Charge Holding Dynamic Latched Comparator (LRCHDLC) which is an architectural improvisation from a hybrid dynamic latched comparator architecture (HDLC). The transient re-

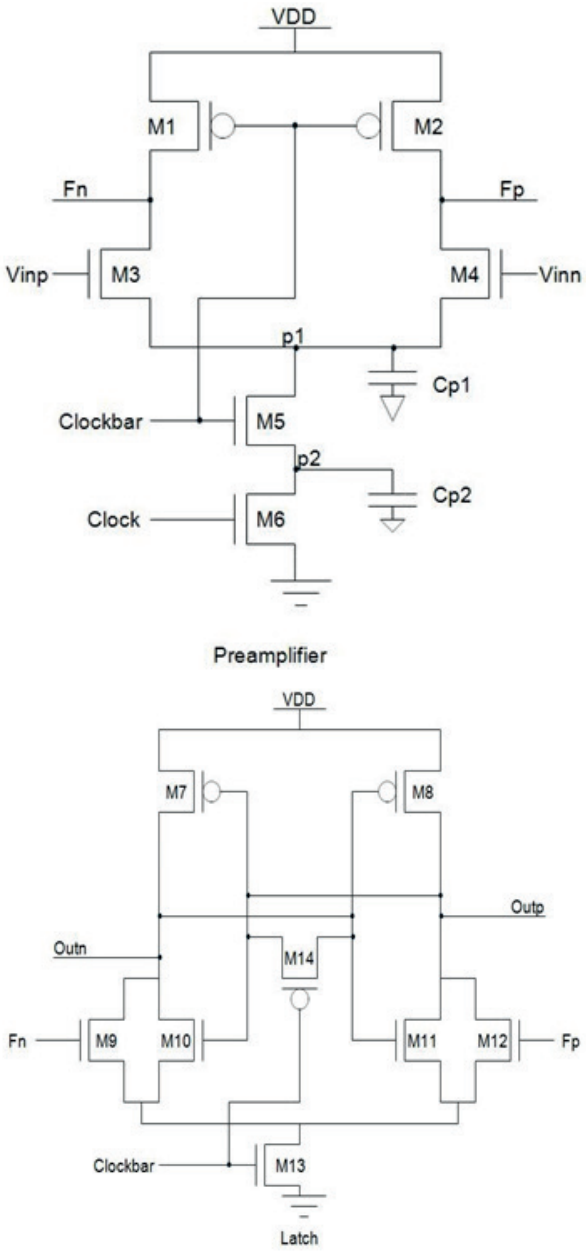

Figure 3: Schematic diagram of HDLC

sponse of the hybrid architecture HDLC and proposed LRCHDLC are shown in Figures 4 and 6 respectively.

HDLC aims at effective optimization of power and delay with minimal tradeoff for wider range of V_{CM} and $V_{DIFF.}$ The countereffect recorded in [3] was a high delay during high range of V_{CM} values. Similarly, the counter effect that is witnessed in [2] was high power consumption despite achieving a shorter time lapse for latching. The hybrid architecture is carefully designed with an appropriate choice of transistor sizing and capacitance values. The transient response of this HDLC architecture implemented in 90 nm CMOS technology shows a slight logic degradation in the output voltages. Also, when power and delay were analyzed for wider V_{CM} and V_{DIFF} values, the corresponding architecture offers power as well as delay without much countereffects. This concurrent optimization of power and delay using charge shared preamplifier and shared charge latch is taken as the base for the improvised architecture, LRCHDLC. In LRCHDLC, the concurrent optimization of power and delay is retained with no logical degradation, by shifting of a modified NAND based latch. The charging / discharging path is simplified and channelized smoothly in the proposed architecture, LRCHDLC.

The topological changes in HDLC have paved the way for further power and delay reduction, whereas switching to NAND based modified latch in LRCHDLC helps in overcoming logical degradation. In both LRCHDLC shown in Figure 5 and its parent architecture HDLC shown in Figure 3, a pass transistor presets both the output nodes, out_p and out_n ,to a minimum threshold voltage (as shown in transient waveform, around 0.5 to 0.6 V for second evaluation phase after charge shared between the nodes through pass transistor) to overcome the time lapse of the nodes to charge and discharge, making the comparison faster. The forementioned factor assures almost similar voltage levels

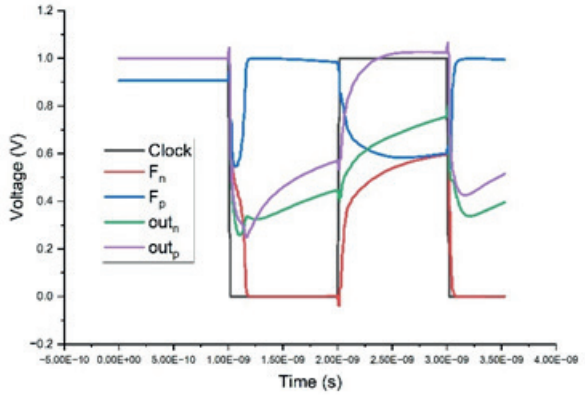

Figure 4: Transient response of HDLC simulated at 45 nm technology with V_{DD}- 1V, F_{clk} – 1 GHz, V_{CM}- 0.7 V and V_{DIFF} – 20 mV

at the latch inputs pulling both the latch outputs to a strong 1 and strong 0 at precise times even though NAND type latches are prone to metastable conditions.

The sustained gain from preamplifier is available exactly at the time instant when comparison happens which is achieved with the help of extra tail transistors with parasitic capacitances C_{P1} and C_{P2} at the drain of M_5 and M_6. The correct outputs are transferred to the latch within an appropriate time frame with less power consumption because of the extra tail transistors in preamplifier.
The reset phase occurs in similar fashion in both HDLC and LRCHDLC architectures. During the reset phase,

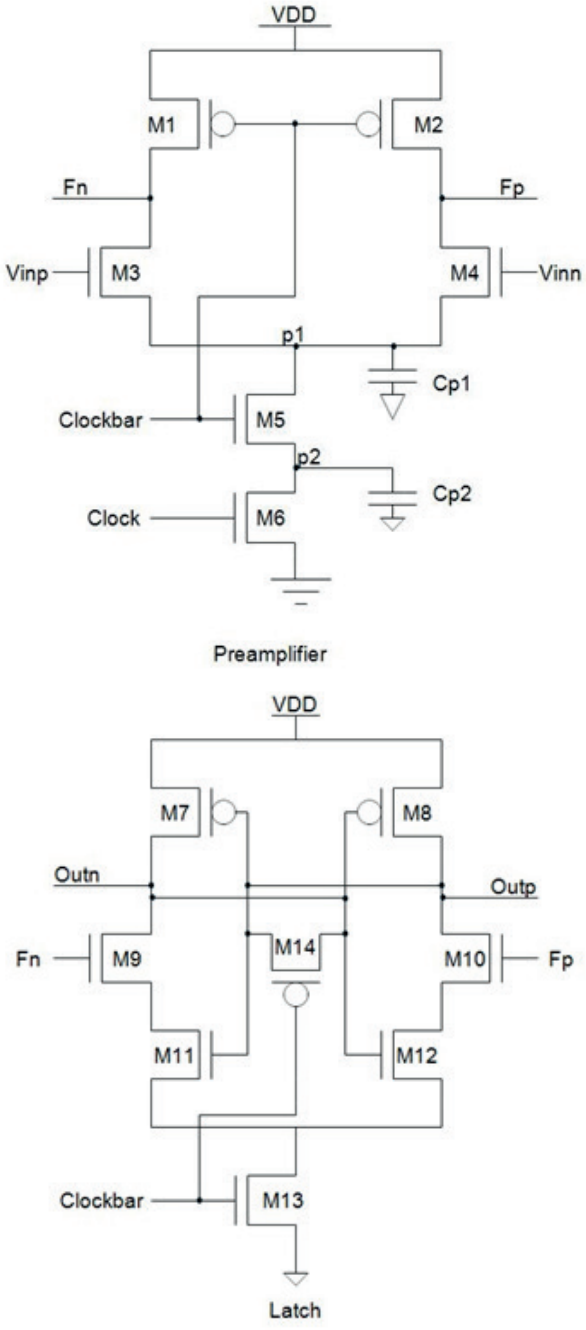

Figure 5: Schematic diagram of LRCHDLC

the clock is high, and the clock bar is low. During this phase the output nodes of preamplifier charges to V_{DD} and only M_6 is active with no parasitic capacitances being charged. These high outputs of preamplifiers are connected to input pull down transistors M_9 and M_{10} of the latch which turns them on. The pass transistor is on through a low clock bar, which distributes the available charges at the output nodes of the latch equally.

During the evaluation phase, the inputs V_{inp} and V_{inn} are given, the clock goes low, and the clock bar goes high. Assuming V_{inp} is greater than V_{inn}. Thus, the transistors M1 and M_2 go off, unable to sustain the output nodes high, further. The available charge at the output nodes of preamplifier follows the path to discharge via M_3/M_5 and M_4/M_5 charging both C_{P1} and C_{P2}. Since V_{inp} is larger, the node F_n discharges faster than F_p, making the input NMOS transistor of latch circuit, say M_9 go off faster than the other one M_{12}.

In the case of hybrid architecture (HDLC), the tail transistor M_{13} of latch is on since the clock bar is high, thus draining the charge of both out_n and out_p to ground through M_{10} and M_{11}.

Similarly, in the case of LRCHDLC, the tail transistor M_{13} is on. Since $V_{inp} > V_{inn}$, the node F_p discharges faster than F_n. The sooner F_p discharges, the sooner it switches M_{10} off. It is significant that the pass transistor is off since the clock bar is high. Hence the already available shared charge at out_n and out_p is around 0.6 V. At this threshold, M_{11} and M_{12} are still in active region. In the short time of F_p falling below the threshold voltage required by M_{10}, there is discharge of out_n through $M_9/M_{11}/M_{13}$. Whereas the out_p still at 0.5 is raised to V_{DD} with regeneration of cross connected inverters.

This effectively reduces power dissipation and shortens the discharge time. Once M_9/M_{10} goes off, the latching begins. The cross connected inverters pull up the node out_n to V_{DD} and pull down the node out_p to zero both in HDLC and LRCHDLC. Also, the availability of output nodes linked to ground directly in hybrid architecture, makes it dissipate only minimal charge. Hence constant high output is not attained at the end of comparison, which can be observed as a slight decrease from 1 V in the transient response of HDLC in Figure 4. This is overcome in LRCHDLC, which prevents the leakage at the end of comparison, offering a strong 1 as shown in Figure 6.

In conventional dynamic comparators, when there is a transition from reset to evaluation phase, the moment the clock changes, the differential discharging of preamplifier outputs is rapid, and the effective differential voltage is channelized into the latch for comparison.

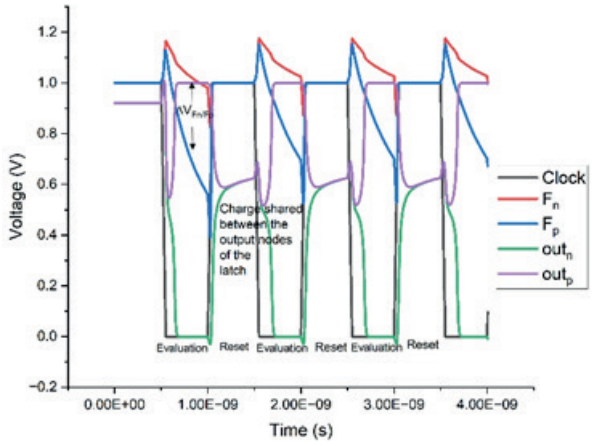

Figure 6: Transient response of LRCHDLC simulated at 45 nm technology with V_{DD}- 1V, F_{clk} – 1 GHz, V_{CM}- 0.7 V and V_{DIFF} – 20 mV

The differential voltage deteriorates before serious latching starts. Most of the conventional topologies showcases more power consumption as well as dissipation with notable delay because of this phenomenon. There are few options to overcome this technical challenge to obtain a significant performance.

i) Deactivate the preamplifier when the differential output voltage is high enough for effective latching process.
ii) Preactivated latch when the preamplifier offers maximum differential gain.

Moving the preamplifier into idle state when the output differential voltage is high, thereby sustaining the maximum differential voltage until the latch turns on is the first option. The second option creates the same power during latch activation and the time required for latch initiation remains the same. Also, the differential voltage will eventually go down during the latch initiation period. Prior activation of latch as well as freezing the preamplifier to hold its maximum output differential voltage requires separate clocking and control techniques [20] which will introduce additional power and delay.

Beyond these options, without complex gating techniques or clocking techniques, introducing parasitic capacitance is preferred. Using an extra tail transistor with parasitic capacitances holds the maximum output differential voltage of preamplifier with alternative activation of tail transistors. Proper sizing of both the tail transistors and input transistors with channelized charging of parasitic capacitances guarantee holding of maximum difference gain at the preamplifier outputs. Meanwhile latch activation is also fastened by prior charging of output nodal voltages of latch so that the time taken for latch initiation is neglected. In the

conventional comparator, during the evaluation phase the output nodes of preamplifier start discharging and once it goes less than threshold required for input transistors of second stage, the latch gets activated. In the proposed comparator, when the clock moves into a transition for evaluation phase, the preamplifier is ready with maximum differential voltage and latching starts without taking time for initiation thereby significantly reducing power consumption and delay.

The proposed comparator has made significant efforts to reduce power by sustaining the latch output nodal voltages at a minimum voltage which reduces the time lapse of complete discharging down to zero and charging from initial value. In preamplifier, larger input transistors are employed to increase the transconductance which in turn deteriorates the offset voltage [4]. Amongst many topologies that render fast latching process, introducing pass transistor guarantees equal charging at both output nodes in due course reducing power consumption.

5 Analysis of performance metrics

Three performance metrics, namely delay, power and energy efficiency are analyzed for the proposed architecture to prove its suitability for high end applications. Section 5 discusses all the three-performance metrics in detail in the subsections with necessary graphs and mathematical analysis. Section 5.1 discusses the analysis of delay with sub sections discussing the mathematical analysis of delay and influence of input voltage over delay. Section 5.2 and 5.3 discusses the analysis of average power consumption and energy efficiency, respectively.

5.1 Delay

To compare the factors that influence the delay in conventional as well as proposed architectures, detailed derivation of both the architectures is presented in this section.

5.1.1 Delay of Conventional Comparator

The delay associated with conventional double tail dynamic latched comparator architecture comprises two factors, namely t_1 and $t_{latching}$. t_1 is the time taken by the output capacitance to discharge until anyone of the NMOS transistors of the cross connected inverters is on as shown in Eq. (0).

$$t_1 = R_1 C_L \tag{0}$$

The effective resistance R_1 during the discharging of C_L at output nodes can be replaced as ratio of threshold voltage and the drain current of M_{11} or M_{12} as depicted in Eq. (1)

$$t_1 = \frac{C_L V_{thn}}{I_{M11/M12}} \tag{1}$$

where V_{thn} is the threshold voltage of NMOS transistor of cross connected inverter to be on. $I_{M11/M12}$ can also be approximated as half of the tail current of T_3. Hence $I_{M11/M12}$ can be written as shown in Eq. (2)

$$t_1 = \frac{2 C_L V_{thn}}{I_{tail3}} \tag{2}$$

The second component $t_{latching}$ is the time taken for regeneration to begin which involves the latching process and is given in Eq. (3) as follows

$$t_{latching} = \frac{C_L}{g_{m,eff}} \ln \frac{V_{DD}}{2\Delta V_o} \tag{3}$$

Where ΔV_o is the initial output voltage difference, g_{meff} is the effective transconductance of the latch stage, especially covering transistors that couple the preamplifier and latch stage. C_L is the output load capacitance. The initial output voltage difference can be derived through Eq. (4), Eq. (5), Eq. (6) and Eq. (7).

$$\Delta V_o = I_O R_O \tag{4}$$

The initial output voltage difference can be written as the product of effective resistance R_o and current difference I_o. I_o can be expanded as the product of transconductance g_{m0} and input voltage V_{io} of the corresponding stage. Also, effective resistance Ro can be written as the ratio of output nodal voltage difference $\Delta V_{Fn/Fp}$ in the preamplifier stage and the tail current of second stage.

$$\Delta V_O = g_{mo} V_{io} \quad \frac{\Delta V_{Fn/Fp}}{I_{tail3}} \tag{5}$$

The input voltage V_{io} is the threshold requirement of pull-down transistors of preamplifier and hence replaced as follows in equation (7).

$$\Delta V_o = 2\left(V_{thn}\right) g_{mo1,2} \frac{\Delta V_{Fn/Fp}}{I_{tail3}} \tag{6}$$

The preamplifier output nodal difference can be derived as shown in eq. (7) and eq. (8). The resistance is written with time constant equivalent and hence written as the time lapse for discharging C_L.

$$\Delta V_{Fn/Fp} = \Delta I_{Fn/Fp} R_{o,preamp} \tag{7}$$

$$\Delta V_{Fn/Fp} = \Delta V_{diff} g_{m1,2} \frac{t_1}{C_{L,\ preamp}} \tag{8}$$

Substituting eq. (2) in the above eq. (8), the final equation of $\Delta V_{Fn/Fp}$ is given as,

$$\Delta V_{Fn/Fp} = \Delta V_{diff} g_{m1,2} \frac{C_L 2V_{thn}}{I_{\text{tail3}} C_{L,\ preamp}} \tag{9}$$

The final value of ΔV_o after substituting the preamplifier output nodal difference as

$$\Delta V_o = \frac{4\left(V_{thn}\right)\left(V_{thn}\right) g_{mo1,2} \Delta V_{diff} g_{m1,2\ C_L}}{C_{L,\ preamp} I_{tail3}^2} \tag{10}$$

The total latching delay can be further obtained as equation (15) by substituting in (4).

$$t_{latching} = \frac{C_L}{g_{m,eff}} \ln V_{DD} \frac{1}{2\Delta V_O} \tag{11}$$

Which can be rewritten as follows as shown in eq. (14)

$$\frac{C_L}{g_{m,eff}} \ln \frac{V_{DD} C_{L,preamp} I_{tail3}^2}{8\left(V_{thn}^2\right) g_{mo1,2} \Delta V_{diff} g_{m1,2} C_L} \tag{14}$$

The total delay for a conventional comparator is derived by adding t_1 and $t_{latching}$ given in eq. (15)

$$T_{total,Conventional} = \frac{2 C_L V_{thn}}{I_{tail3}} + \\ + \frac{C_L}{g_m, eff} \ln \frac{V_{DD} C_{L,preamp} I_{tail3}^2}{8\left(V_{thn}^2\right) g_{mo1,2} \Delta V_{diff} g_{m1,2} C_L} \tag{15}$$

5.1.2 Delay of Low power Rapid Charge Holding Dynamic Latched Comparator (LRCHDLC)

For the proposed comparator LRCHDLC, the first component of delay t_1 can be derived as shown in eq. (16). In proposed comparator, the necessary threshold is offered by the charge equally shared between the output nodes by the PMOS pass transistor which is represented as V_{DD}- $2V_{tp.}$

$$t_1 = \frac{C_L (V_{DD} - 2V_{tp})}{I_{tail3}} \tag{16}$$

The second component of total delay, $t_{latching}$ as shown in eq. (3) can be approximated for the proposed comparator as shown below.

To find ΔV_o for the proposed comparator, it is significant to note that the preamplifier, which is equipped with two tail transistors generating only the minimum required tail current for amplification. This necessary tail current helps in sustaining the maximum gain with low power consumption. Figure 7 illustrates the tail currents of transistor M_5 in both the conventional and proposed comparators. The gain can also be increased further and sustained further with a compromise on power consumption. The differential output voltage for the proposed comparator is shown in eq. (17).

$$\Delta V_o = 2\left(V_{DD} - V_{tp}\right) g_{mo1,2} \frac{\Delta V_{Fn/Fp}}{I_{tail3}} \tag{17}$$

The sizing of the tail transistors is chosen in such a way that the preamplifier will offer maximum gain (optimal tail current which will in turn not increase the power) during the initiation of the latch. This helps with effective and fast decisions during the latching phase. The threshold offered by the PMOS pass transistor takes the place of the threshold of NMOS transistor of cross connected latch as shown below in eq. (18). Substituting $\Delta V_{fn/fp}$, the ΔV_o can be expanded as eq. (19).

$$\Delta V_{Fn/Fp} = \Delta V_{diff} g_{m1,2} \frac{C_L 2\left(V_{DD} - 2V_{tp}\right)}{I_{\text{tail3}} (C_{P1} + C_{P2})} \tag{18}$$

$$\Delta V_o = \frac{2\left(V_{DD} - V_{tp}\right)\left(V_{DD} - 2V_{tp}\right)\left(V_{thn}\right) g_{mo1,2} \Delta V_{diff} g_{m1,2\ C_L}}{(C_{P1} + C_{P2}) I_{tail3}^2} \tag{19}$$

In proposed comparator, the parameter ΔV_o is not only improved since the capacitance $C_{P1} + C_{P2}$ is lesser when compared to the output capacitance $C_{L,\ preamp}$ in case of conventional comparator. The $t_{latching}$ can now be updated as eq. (19)

$$\frac{C_L}{g_{m,eff}} \ln \frac{V_{DD} (C_{P1} + C_{P2}) I_{tail3}^2}{2\left(V_{DD} - V_{tp}\right)\left(V_{DD} - 2V_{tp}\right) g_{mo1,2} \Delta V_{diff} g_{m1,2} C_L} \tag{19}$$

The total delay for the proposed comparator LRCHDLC is shown in eq. (20)

$$T_{total,Proposed} = \frac{C_L (V_{DD} - 2V_{tp})}{I_{tail3}} + \\ + \frac{C_L}{g_{m,eff}} \ln \frac{V_{DD} (C_{P1} + C_{P2}) I_{tail3}^2}{2\left(V_{DD} - V_{tp}\right)\left(V_{DD} - 2V_{tp}\right) g_{mo1,2} \Delta V_{diff} g_{m1,2} C_L} \tag{20}$$

Both the discharging of preamplifier output nodes and charging of latch output nodes (to threshold required for latching) is not required in the proposed architecture. Hence the component t_1 as well as $t_{latching}$ is reduced. The

transient response of the proposed comparator in Figure 6 depicts the improvement in ΔV_o through change in $\Delta V_{Fn/Fp}$.

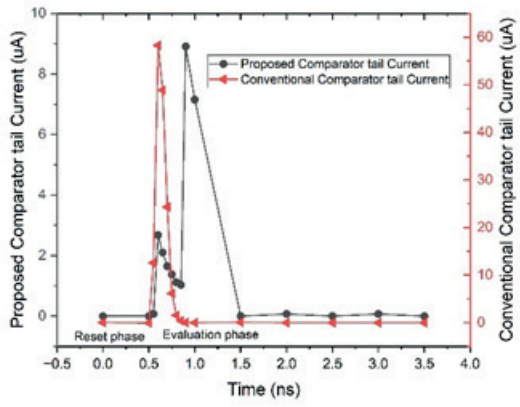

Figure 7: Tail currents of the preamplifier in conventional as well as proposed comparator

With respect to the proposed comparator, the influence of the component t_1 on the total delay is reduced qualitatively. The reason is that the proposed architecture utilizes the internal parasitic capacitances. The load capacitances are replaced by parasitic capacitances ($C_{P1} + C_{P2}$) predominantly to take up the charge from F_n/F_p nodes, rather than C_L. The outcome of t_1 which is latch initiation, is already achieved through pass transistor precharging the out_n/out_p to 0.5 V during reset phase itself. Also, the preamplifier with two tail transistors transfers the maximum gain earlier to the latch. Added advantage is that the preamplifier is not actively consuming any power for amplification after the maximum gain is transferred. The need for NMOS threshold is now replaced as the threshold of PMOS Pass transistors since they pull up out_n/out_p to 0.5 V or $V_{DD}/2$. There is a major reduction in $t_{latching}$ as the out_n and out_p are already charged up to 0.5 V during the reset phase, way before the latching is initiated.

5.1.3 Variation of delay with V_{CM} and V_{DIFF}

A meticulous study of the variation in delay with various factors such as V_{CM}, V_{DIFF} and supply voltage is also presented in this section. A fast-decision-making process is one of the key requirements of high-speed ADC, that can be assured by analyzing the variation of delay with V_{CM} and V_{DIFF}. To determine the robustness and efficiency of the proposed architecture, rigorous and multiple simulations are carried out for a wide range of V_{CM} and V_{DIFF}. The proposed architecture offers consistent range of delay and power even when V_{CM} and V_{DIFF} drops down proving its high sensitivity in decision making during evaluation phase. Simulations were carried out for observing delay at various V_{CM} values (0.5 V to 0.9 V with a step size of 0.1 V) and V_{DIFF} values (10 mV to 100 mV with a step size of 10 mV) on conventional comparator, LRCHDLC (90 nm) and LRCHDLC (45 nm) as shown in Table 1.The conventional comparator records delays ranging from 138 ps to 592 ps for various V_{CM} and V_{DIFF} values, whereas the proposed comparator shows less and consistent delay values, within lower range varying from 26.79 ps to 25.73 ps in case of LRCHDLC using 90 nm technology and from 19.79 ps to 29.09 ps in case of LRCHDLC using 45 nm technology. This implies that in case of proposed comparator, only minimal standard time lapses are taken for charging and discharging at the output nodes of the proposed comparator. Wide varying V_{CM} and V_{DIFF} does not influence the range of delays in the proposed comparator due to minimum t_1 and $t_{latching}$. Figure 8 and 9 shows the transient response of LRCHDLC and conventional architecture at 45 nm for various sets of V_{CM} ranging from 0.5 V to 0.9 V. Figure 10 shows the variations in the output nodal voltages, out_n and out_p in the transient response for various V_{DIFF} ranging from 20 mV to 100 mV with a step size of 20 mV for V_{CM} – 0.7 V. During second evaluation phase, Figure 8 shows that out_p rises first for V_{CM} – 0.5 V first and then it can be observed that it is followed by V_{CM} – 0.6 V upto 0.9 V. Similarly, in Figure 9, out_n rises first for V_{CM} – 0.9 V and then goes down to V_{CM}- 0.5 V. In case of conventional comparator, Delay is inversely proportional to V_{CM} and V_{DIFF}. Whereas, in the case of proposed comparators, the delay is directly proportional to V_{CM} and inversely proportional to V_{DIFF}. The mathematical equations for total delay of conventional and proposed comparators are derived in the previous section as seen in Equations (15) and (20) respectively. The initial output voltage difference ΔV_o , which is directly proportional to $\Delta V_{fn/fp}$ is observed to be proportional to the differential voltage, ΔV_{diff} as shown in Equations (5), (6) and (8). From Equation (3), $T_{latching}$ is inversely proportional to ΔV_o proving the indirect proportionality between V_{DIFF} and delay. The reduction of delay with increase in V_{DIFF} can be explained with respect to two factors. The first factor is that when the V_{DIFF} becomes larger, the gain naturally increases,

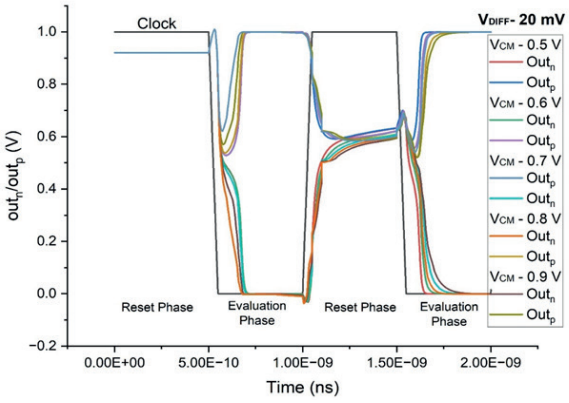

Figure 8: Transient response of LRCHDLC (45 nm) with V_{DIFF} = 20 mV for various V_{CM} values from 0.5 V to 0.9 V

Table 1: Analysis of delay for various V_{CM} and V_{DIFF} for conventional (90 nm) and LRCHDLC (90 nm & 45 nm)

V_{DIFF} (mV)	Conventional Comparator					LRCHDLC (90 nm)				LRCHDLC (45 nm)					
	V_{CM} (V)					V_{CM} (V)				V_{CM} (V)					
	0.9	0.8	0.7	0.6	0.5	0.9	0.8	0.7	0.6	0.5	0.9	0.8	0.7	0.6	0.5
10	179	206	261	404	592	26.79	26.41	26.1	25.92	25.86	19.79	19.51	19.31	19.2	19.13
20	166	190	240	369	584	26.57	26.26	26	25.86	25.83	19.72	19.46	19.28	19.18	19.12
30	158	182	228	346	578	26.37	26.11	25.91	25.81	25.81	19.64	19.41	19.25	19.17	19.12
40	153	175	219	329	572	26.2	25.98	25.84	25.76	25.79	19.57	19.37	19.23	19.15	19.11
50	150	171	212	314	567	26.06	25.85	25.76	25.72	25.78	19.51	19.32	19.2	19.14	19.11
60	147	167	206	301	560	25.91	25.75	25.69	25.68	25.76	19.45	19.29	19.18	19.13	19.1
70	144	163	200	290	554	25.78	25.66	25.63	25.65	25.75	19.39	19.25	19.17	19.12	19.1
80	142	160	195	280	545	25.66	25.58	25.58	25.63	25.74	19.34	19.22	19.15	19.11	19.1
90	140	157	191	270	535	25.55	25.51	25.53	25.61	25.74	19.28	19.19	19.13	19.11	19.09
100	138	154	186	262	521	25.46	25.44	25.48	25.59	25.73	19.25	19.16	19.12	19.1	19.09

and the topology also supports by transferring maximum gain to the readily precharged latch. Secondly, the charging and discharging time during evaluation phase is well sustained by precharging of output nodes during reset phase itself, which significantly reduces the latching delay, $t_{Latching}$.

In all conventional dynamic comparator topologies, a lower V_{CM} makes it difficult for the input transistors of preamplifier to switch to linear state for amplification. Also, insufficient gain further slows down the decision-making process. However, the proposed architecture precharges the output nodes out_n and out_p during reset phase, making it easier to proceed to latching phase more easily on time. In LRCHDLC, during the second evaluation phase after charge sharing, the latching time increases with a rise in V_{CM} as seen in Figure 8

Whereas in conventional architecture, Figure 9 shows that the latching time decreases with rise in V_{CM} but results in a larger delay due to the absence of a charge sharing mechanism. Quantitatively, this can also be observed seen in Table 1 where there is a direct proportionality between V_{CM} and delay values. It can be observed from Figure 8 and 9 shows that the decision-making time is larger in the case of conventional architecture, when compared to the proposed architecture, LRCHDLC.

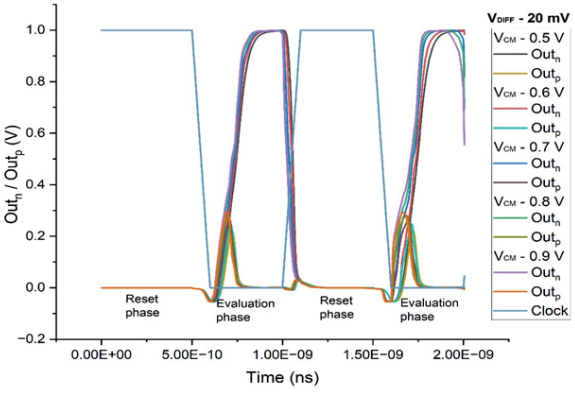

Figure 9: Transient response of Conventional comparator (45 nm) with V_{DIFF} = 20 mV for various V_{CM} values from 0.5 V to 0.9 V

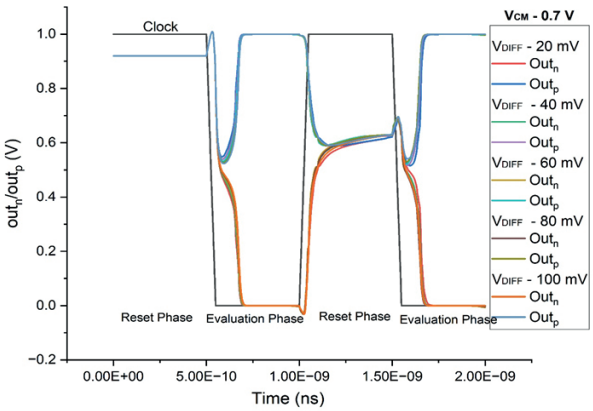

Figure 10: Transient response of LRCHDLC (45 nm) with V_{CM} – 0.7 V for various V_{DIFF} values from 20 mV to 100 mV.

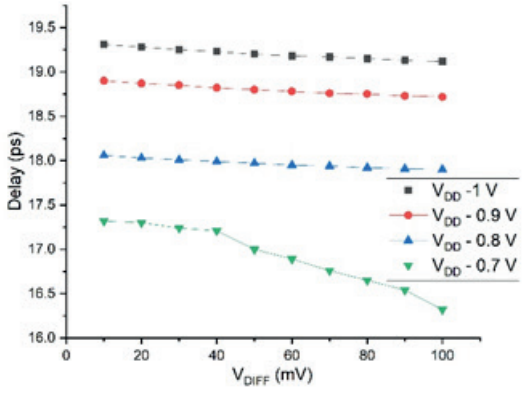

Figure 11: Variation of delay with V_{DD} for V_{CM} - 0.7 V and V_{DIFF} – 20 mV, F_{clk} – 1GHz (LRCHDLC – 45 nm)

Table 2: Analysis of power consumption for various V_{CM} and V_{DIFF} for conventional (90 nm) and LRCHDLC (90 nm & 45 nm)

V_{DIFF} (mV)	Conventional Comparator (90 nm)					LRCHDLC (90 nm)					LRCHDLC (45 nm)				
	V_{CM} (V)					V_{CM} (V)					V_{CM} (V)				
	0.9	0.8	0.7	0.6	0.5	0.9	0.8	0.7	0.6	0.5	0.9	0.8	0.7	0.6	0.5
10	5.01	4.96	4.91	4.87	4.76	2.62	2.54	2.47	2.4	2.31	1.49	1.32	1.11	0.88	0.69
20	4.94	4.9	4.85	4.81	4.71	2.61	2.53	2.46	2.39	2.3	1.49	1.32	1.1	0.88	0.68
30	4.9	4.86	4.81	4.76	4.67	2.59	2.51	2.44	2.38	2.3	1.5	1.32	1.09	0.87	0.68
40	4.88	4.83	478	4.72	4.64	2.58	2.5	2.44	2.37	2.3	1.5	1.31	1.09	0.86	0.67
50	4.86	4.81	4.75	4.69	4.61	2.57	2.49	2.43	2.37	2.29	1.5	1.31	1.08	0.85	0.67
60	4.84	4.79	4.73	4.66	4.58	2.55	2.48	2.42	2.36	2.29	1.49	1.3	1.07	0.85	0.66
70	4.82	4.77	4.71	4.64	4.56	2.54	2.47	2.41	2.35	2.29	1.49	1.29	1.07	0.84	0.66
80	4.8	4.75	4.69	4.62	4.54	2.54	2.47	2.4	2.34	2.28	1.49	1.29	1.06	0.84	0.65
90	4.79	4.74	4.68	4.6	4.53	2.53	2.46	2.4	2.34	2.28	1.48	1.28	1.05	0.83	0.65
100	4.78	4.72	4.66	4.59	4.51	2.52	2.45	2.39	2.33	2.27	1.48	1.28	1.05	0.83	0.65

The delay of the proposed architecture, LRCHDLC (45 nm) is analyzed for various supply voltages ranging from 0.7 V to 1 V as shown in Figure 11. As the supply voltage increases, the charge quantity to be held by the nodes also increases. As per the latching mechanism in the proposed circuit, $t_{latching}$ increases as the minimum charge to be held at the output nodes also increases. The regeneration time required for decision making also proportionally increases. It can be noted from Figure 11 that the proposed architecture offers stable delay irrespective of V_{DIFF} values for V_{DD} values from 1 V to 0.8 V, reassuring the robustness of the proposed architecture.

5.2 Average power consumption

Analogous to delay, power consumption is also analyzed for the conventional dynamic comparator, LRCHDLC (90 nm), and LRCHDLC (45 nm) with respect to variations in V_{CM} and V_{DIFF}, as shown in Table 2. With respect to average power consumption, conventional architecture reflects a direct proportionality with V_{DIFF} and indirect proportionality with V_{CM}. The significant change in the case of the proposed comparator is that the overall range has dropped to a greater extent, maintaining the same direct proportionality with V_{CM} and indirect proportionality with V_{DIFF}. Power consumption at each instant is measured for two cycles of complete comparison process for both conventional and LRCHDLC simulated at 45 nm technology, as shown in Figure 12.

In the case of LRCHDLC, the modified preamplifier with two tail transistors limits power dissipation by turning off the preamplifier once maximum gain is transferred. Figures 13 and 14 show power consumption at every instant of the proposed architecture for various sets of V_{DIFF} and V_{CM} respectively, to observe their influence on the performance. Power consumption during the second evaluation phase shows a significant drop when compared to the evaluation phase before successful charge sharing, ensuring minimal power consumption. Also, the time lapse of active state of preamplifier is less in the case of proposed comparator, thereby offering a

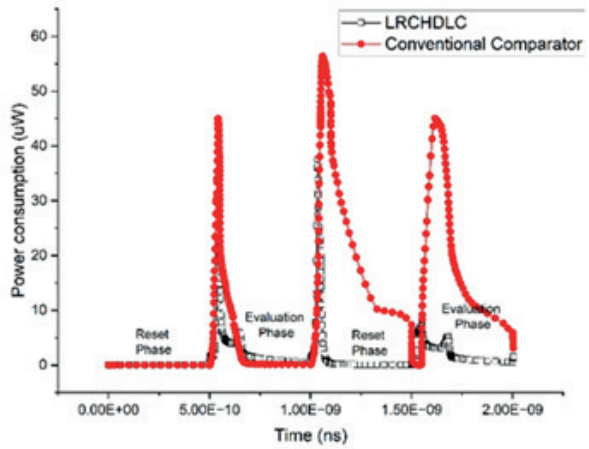

Figure 12: Power consumption of Conventional and proposed comparator, LRCHDLC with V_{DIFF} – 20 mV, V_{CM} – 0.7 V, V_{DD} – 1V at 45 nm technology

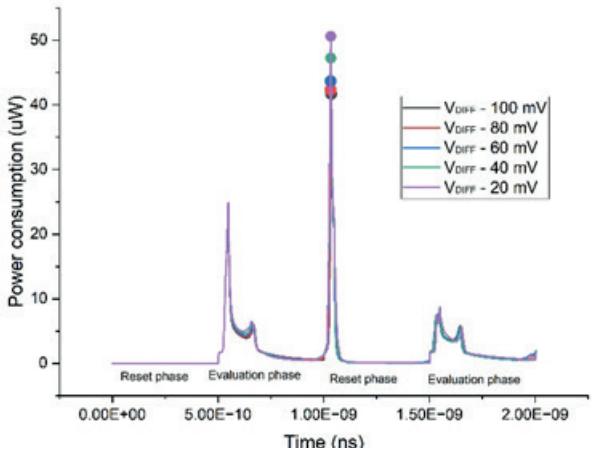

Figure 13: Power consumption of LRCHDLC (45 nm) at every instant for various V_{DIFF} values

regularized power consumption for all wide variations in V_{CM} and $V_{DIFF.}$

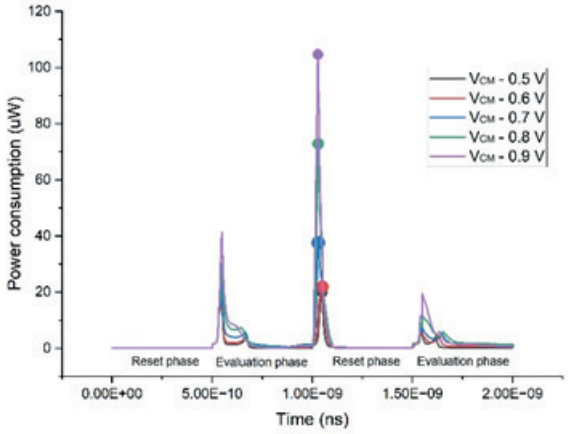

Figure 14: Power consumption of LRCHDLC (45 nm) at very instant for various V_{CM} values

Figures 13 and 14 clearly align with Table 2, proving the direct proportionality with V_{CM} and indirect proportionality with V_{DIFF}. Peak power consumption points are highlighted for various V_{CM} and V_{DIFF} values. The peak power is consumed exactly at the onset of the second reset phase where charge sharing is set to occur. It is highly significant to note that the power consumed during the second evaluation phase is lower than the previous evaluation phase, irrespective of changes in V_{CM} and V_{DIFF}.

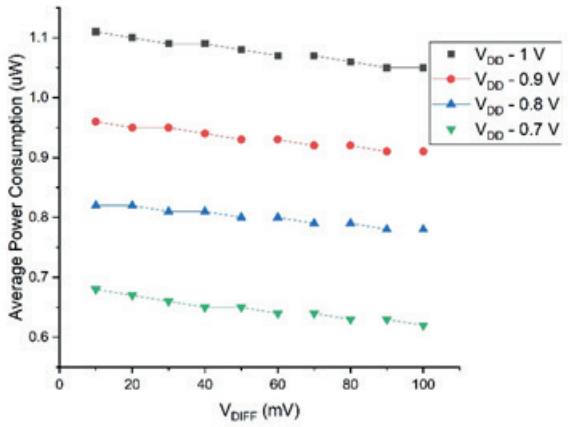

Figure 15: Variation of power consumption with V_{DD} for V_{CM} -0.7 V and V_{DIFF} – 20 mV, F_{clk} – 1GHz

Like delay, average power consumption is analyzed for proposed architecture for various supply voltages ranging from 0.7 V to 1 V as shown in Figure 15. The power consumption of any analog circuit is directly proportional to V_{DD} until there is no major variation in current proportionality due to change in device physics. Both delay and power are highly stable irrespective of V_{DIFF} for V_{DD} values ranging from 1 V to 0.8 V.

5.3 Energy efficiency

Energy efficiency is a metric that indicates the ability of the comparator to complete a full cycle of reset phase and comparison phase, with minimal power consumption while maintaining maximum accuracy and performance. By integrating the power formulae over a period of two full cycles, energy efficiency is calculated. In the case of proposed comparator, the range of energy efficiency has drastically decreased when compared to the conventional architecture as seen in Table 7.

This can be aligned with the drastic reduction in overall power consumption. This is mainly because complete charging and discharging of output nodes is not required in the proposed architecture, which reduces power and energy efficiency. Because of this charge held at the output nodes of the latch by the pass transistor, significant amount of power dissipated during charging and discharging of latch output nodes at every cycle (reset & evaluation) is reduced and hence there is a reduction in energy spent per comparison. The energy spent for effective comparison is observed varying the supply voltages for proposed architecture, LRCHDLC with V_{CM} – 0.7 V varying the value of V_{DIFF} from 10 to 100 mV, as shown in Figure 16.

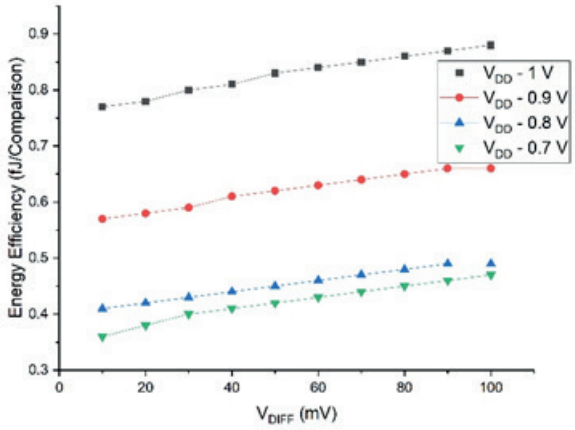

Figure 16: Variation of energy efficiency with V_{DD} for V_{CM} - 0.7 V and V_{DIFF} – 20 mV, F_{clk} – 1GHz

The overall range of energy efficiency decreases with a reduction in V_{DD}, but the individual response shows direct proportionality with V_{DIFF}, whereas delay and power show stable responses with V_{DIFF}. This is one of the reasons that as the technology of the proposed comparator goes from 90 nm to 45nm, energy efficiency increases as seen in Table 7.

6 Results and discussion

6.1 Monte Carlo analysis

Monte Carlo simulations were performed for all the performance parameters which in case of hybrid architecture, gives a delay of 56 ps, power consumption of 8.6µW, and energy efficiency of 98 aJ/comparison. For the final proposed architecture, LRCHDLC simulated in 90 nm, Monte Carlo simulation offered better performance parameters such as a delay of 15.32 ps, power consumption of 2.42 µW, and energy efficiency of 37.15 aJ/comparison. When Monte Carlo simulations performed for LRCHDLC at 45 nm CMOS technology, the architecture offered Power consumption of 890.62 nW, an energy efficiency of 1.1 fJ/comparison and delay of 18.67 ps. The mean and standard deviation of the performance metrics say power consumption, delay and energy efficiency for the proposed comparator (both 90 nm and 45 nm technology) are listed in Table 3.

Monte Carlo simulations are carried out to analyze the robustness of the proposed architecture for every mismatch and fabrication errors. Mathematically, it can be proven that the histogram follows a gaussian distribution since 99% of the samples in histogram lie between +3 σ and -3 σ.

Table 3: Mean and standard deviation of performance metrics using Monte Carlo Simulation

Monte Carlo simulation (N=1000)		
	Mean	Standard deviation
LRCHDLC at 90 nm technology		
Power consumption	2.42 µW	195.37 nW
Delay	15.32 ps	2.48 ps
Energy efficiency	37.15 aJ	16.09 aJ
LRCHDLC at 45 nm technology		
Power consumption	890.62 nW	23.81 nW
Delay	18.67 ps	1.32 ps
Energy efficiency	1.11 fJ	53.17 aJ

Also, more than 90% of the samples lie between +2σ and -2σ and 70% of samples in the histogram fall between +1σ and -1σ. The lower standard deviation values in the case of the proposed comparators ensure consistency and reliability of the design. Most of the values fall within +1σ and -1σ in the normal distribution, proving the robustness of the design. Also, the histogram matches the Gaussian curve with slight skewness.

6.2 Influence of transistor sizing ratio on performance

The sizing ratio of the transistors is chosen after wide variation of widths of all transistors to optimize delay and power without causing any logic degradation, thereby ensuring accurate transient response for every comparison. For the proposed architecture LRCHDLC simulated at 45 nm technology, the variation of performance parameters like delay, energy efficiency and power with respect to transistor sizing are depicted in Figures 17, 18 and 19 respectively.

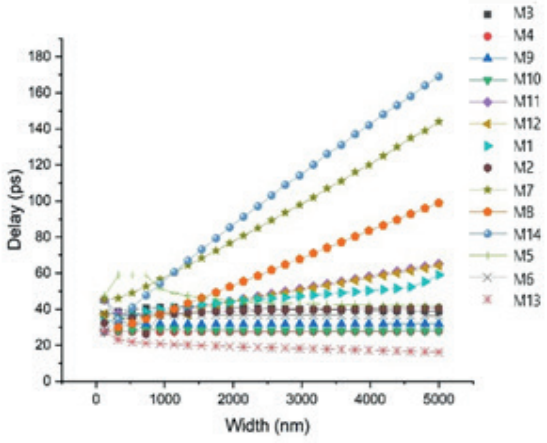

Figure 17: Variation of delay with respect to width of the transistors in LRCHDLC (45 nm)

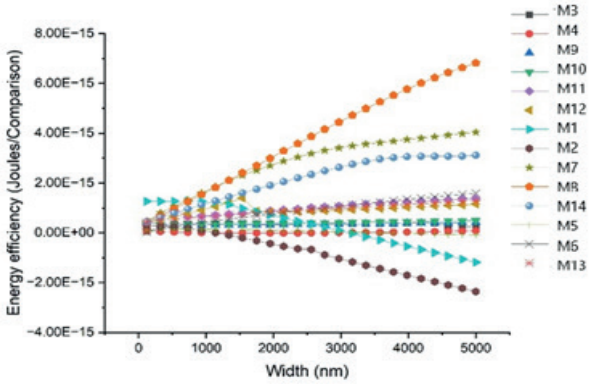

Figure 18: Variation of Energy Efficiency with respect to width of the transistors in LRCHDLC (45 nm)

Table 4: Sizing of the transistors used in the proposed architecture, LRCHDLC (45 nm)

Transistors	Width (m)
M_1	3µ
M_2	1 µ
M_3, M_4	120n
M_5	3.1 µ
M_6	1 µ
M_7 – M_{12}	120n
M_{13}	300n
M_{14}	120n

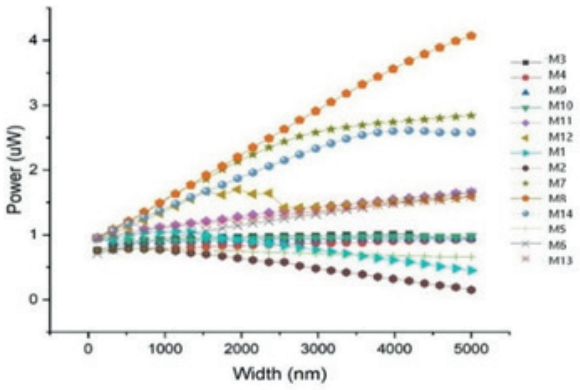

Figure 19: Variation of Power consumption with respect to width of the transistors in LRCHDLC (45 nm)

The sizing of the transistors influences the transconductance thereby causing a major change in power consumption and delay of the circuit. From Figure 17, it is observed that there is a drastic increase in delay when the transistor width increases in the case of pass transistor M_{14} and Pull up transistors M_7 and M_8, ranging up to 160 ps. This influence tends to decrease in the case of the pull-down input transistors of the latch M_9 and M_{10}. The rest of the transistors show stable yet minor variations in the range of 20 ps to 40 ps.

The graph in Figure 18 shows the variation of energy efficiency with respect to transistor width. The pull up transistors of the preamplifier M_1 and M_2 shows a decline in energy efficiency per comparison, whereas the pass transistor M_{14} as well as pull up transistors of the latch M_7 and M_8 shows a significant increase in energy efficiency per comparison. The rest of the transistors show very minor variation in the range of atto joules rather than femto joules from which it can be inferred that the overall range of energy efficiency is narrow and robust to sizing changes. The graphical plot depicted in Figure 19 shows the variation of power with respect to the width of the transistors. The pass transistor M_{14} as well as pull up transistors of the latch M_7 and M_8 offers a notable increase in power consumption up to 4 µW. The intensity of variation is reduced yet minimal rise in power until 2.5 µW is seen when the width of transistors M_{11}, M_{12}, M_5, and M_{13} is increased.

The input pull-down transistors of the preamplifier as well as latch say M_3, M_4, M_9, and M_{10} offer almost constant power consumption in the range of 0.9 nW to 1 µW. On the contrary, the transistors M_5, M_1 and M_2 offer a decline in power when their widths are increased. The transistor sizing used in LRCHDLC (45 nm) is shown in Table 4. It is inferred from simulations and mathematical study that the delay and power solely depend not only on transistor sizing but also on the supply voltage, the input differential voltage, load capacitances used in preamplifier and latch, and the common mode voltage. The transistor sizing impacts the delay by enhancing the effective transconductance of preamplifier and latch input transistors. Inferred from mathematical analysis of delay, the differential voltage ΔV_0 is increased in the proposed architecture.

6.3 Summary and discussion

For proper comparison, the conventional and proposed comparator LRCHDLC are designed in 90 nm as well as 45 nm technology with a clock frequency of 1 GHz for optimized transistor sizing ratios using Cadence Virtuoso Spectre Simulator. Also, process corner variations are analyzed for power, delay, and energy efficiency in case of conventional, hybrid and proposed architectures shown in Table 7. The simulation results in Table 7 are carried out using Cadence Virtuoso Spectre using 90 nm and 45 nm CMOS technology, for V_{DD} =1 V, F_{CLK}=1 GHz, V_{CM} = 0.7 V and V_{DIFF} = 20 mV.

Table 5 shows the comparison of the performance metrics of the proposed architecture with existing architectures from literature. When compared to the existing works in the literature review, the proposed architecture demonstrates a significant reduction in power consumption, energy efficiency and delay without any compromise between each other. Compared to the existing works as seen in Table 5, it is significantly evident that the Power delay product is optimized with optimization in both power and delay rather than increased power with lowered delay or vice versa. The proposed comparator shows significant improvement in delay and power when compared to conventional architecture, [1], [4], [8], [17], and [21]. Rather than achieving drastic improvement in one of the performance parameters, compromising the other performance metrics, concurrent improvement in power and delay is achieved in the proposed architectures. The trade-off observed between power and delay in the proposed comparator is low when compared to the existing topologies of the literature. Table 6 shows the progressive reduction of power and delay right from conventional architecture to the proposed architecture. The modified preamplifier with an extra tail transistor and latch with pass transistor to hold charge shows a drastic improvement in power consumption, reduced three times when compared to conventional comparator architectures. The drastic reduction in power and delay simultaneously is solely due to the architectural change in latch and the tail transistors in preamplifier that helps in parallel sustaining of charge in output nodes and holding maximum gain in preamplification respectively.

Table 5: Comparison of the proposed work with existing literary works

Ref	[1]	[8]	[4]	[21]	[17]	[2]	Conventional	HDLC	LRCHDLC	LRCHDLC
Technology (nm)	65	90	180	180	90	90	90	90	90	45
Operating frequency (GHz)	5	1	1.5	0.5	0.5	1	1	1	1	1
VDD (V)	1	1	1.8	1.8	1	1	1	1	1	1
Offset voltage(mV)	8	2.44	2.60	2.19	1		-	-	-	-
Power (μW)	73	-	-	347	140.76	32.62	4.8	6.53	2.46	1
Delay (ps)	-	20.95	196.9	-	91.19	-	276	47	26	19
Energy efficiency(fJ)	0.253	8.18	40.45	-	-	32.6	12.61	0.48	0.33	0.969
No of transistors	14	18	19	15	15	14	13	14	14	14
PDP (fJ)	-	-	-	-	12.8	-	0.41	0.30	0.063	0.019

Table 6: Comparison of delay and power of literature and proposed work for V_{CM} = 0.7 V and V_{DIFF} = 20 mV

Technology	Architecture	Delay(ps)	Power(μW)
90 nm	Conventional DTDLC	276	4.83
65 nm	Charge sharing DTDLC [1]	-	73
90 nm	Shared charge reset DTDLC [2]	51	32.62
90 nm	Hybrid DTDLC	47	6.53
90 nm	Low power Rapid Charge Holding Dynamic Latched Comparator (LRCHDLC)	26	2.46
45 nm	Low power Rapid Charge Holding Dynamic Latched Comparator (LRCHDLC)	19	1

Table 7: Comparison of conventional and proposed architecture with improvisation for V_{CM} =0.7 V V_{DIFF} = 20 mV F_{clk} = 1 GHz for various process corner variations

	Conventional architecture (90 nm)			Hybrid Architecture HDLC (90 nm)			Proposed architecture LRCHDLC (90 nm)			Proposed architecture LRCHDLC (45 nm)		
	Average power (μW)	Delay (ps)	Energy efficiency (fJ)	Average power (μW)	Delay (ps)	Energy efficiency (fJ)	Average power (μW)	Delay (ps)	Energy efficiency (fJ)	Average power (μW)	Delay (ps)	Energy efficiency (fJ)
FF	5.02	130	13.21	8.68	41	0.834	2.65	19	0.581	1.32	14	0.563
SS	4.63	645	11.91	4.99	58	0.250	2.28	36	0.170	0.675	28	1.5
SF	4.60	590	11.91	5.10	43	0.285	2.35	38	0.185	0.888	24	1.2
FS	4.89	192	12.81	8.03	56	0.743	2.55	18	0.536	1.15	14	0.655
TT	4.83	276	12.61	6.53	47	0.480	2.46	26	0.332	1	19	0.969

The layout of the proposed architecture using 45 nm CMOS technology is shown in Figure 20. The proposed architecture LRCHDLC using 45 nm CMOS technology holds an area of 23.66 μm^2. (4.855 μm * 4.875 μm).

6.4 Key advantages of the proposed architecture

The power consumption of the proposed topology, LRCHDLC, is reduced by restricting the active duration of the preamplifier and prior precharging of the output nodes of the latch.

The process of latching starts without waiting for the latch output nodes for charging up to minimum threshold as its already completed in reset phase, thereby reducing the overall time for completing decision making phase.

Peak differential voltage is sustained by ensuring maximum voltage swing with the help of the additional tail transistor (through nodal parasitic capacitances) in the preamplifier circuit. This helps with accurate decision making and improves the sensitivity of the comparator. The proposed architecture achieves concurrent optimization of power and delays using a simplified control phenomena with an additional transistor in both preamplifier and latch, say M_6 and M_{14} respectively.

The proposed architecture is suitable for Flash ADC which requires high speed and low power consumption, with minimum complexity in clocking and control schemes.

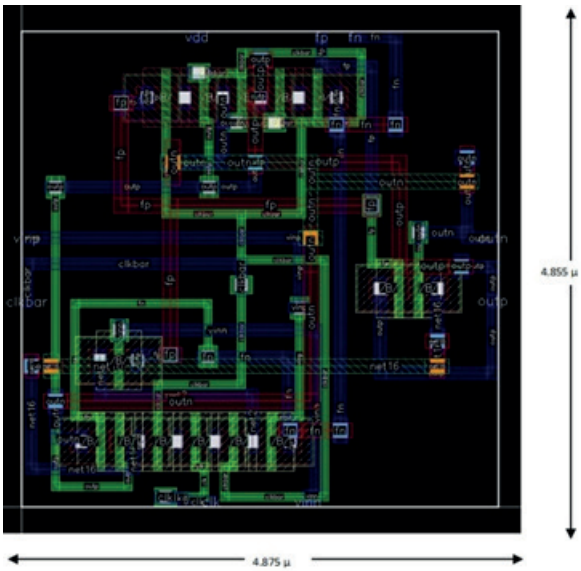

Figure 20: Layout of the proposed architecture, LRCH-DLC

7 Conclusion

This paper demonstrates that the proposed latch stage is more effective in achieving optimized power and delay without any counter mechanisms rising one another parameter. Monte Carlo analysis considering corner and mismatch concludes that the proposed comparator LRCHDLC simulated at 45 nm CMOS technology offers a delay of 18.67 ps, power consumption of 0.890 µW, and an energy efficiency of 1.1fJ/conversion. A thorough simulation study validates the effectiveness of managing the counter effects that arise when there is a rise in power with a delay reduction. When the proposed LRCHDLC (90 nm) is compared to conventional architecture, the delay is reduced by 91%, energy efficiency is reduced by 92%, and the average power consumption is reduced by 49%.

8 Conflict of Interest

The authors declare no conflict of interest.

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Arrived: 26. 11. 2024
Accepted: 11. 07. 2025

Original scientific paper
https://doi.org/10.33180/InfMIDEM2025.402

Informacije MIDEM
Journal of Microelectronics, Electronic Components and Materials
Vol. 55, No. 4(2025), 219 – 228

Smart Prediction and Trust-based Transmission in Delay-Targeted Networks for Aviation Communication

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Abstract: Delay Targeted Networking (DTN) facilitates communication in environments with sporadic connectivity and long delays, such as space missions and isolated locations. The rise of 5G technology has increased the demand for in-flight services, challenging aviation communication to provide reliable data through satellite systems and traditional macro-cellular networks. However, airborne communication's dynamic nature poses significant challenges, including irregular connections and variable delays. To tackle these challenges, a novel Smart Prediction and trAnsmission mechanism for delay taRgeted networK (SPARK) technique has been proposed to enhance the efficiency and reliability of DTNs in aviation communication. The proposed SPARK method includes a comprehensive node trust evaluation system, utilizing direct and indirect trust metrics to ensure network reliability. After evaluating node trustworthiness, the proposed method restricts heavy load traffic based on trustworthiness. The Prediction and Transmission Module incorporates the Cooperative Watchdog System (CWS) to dynamically update each node's reputation score. Nodes are classified into cooperative, partially cooperative, neutral, mislead, and selfish nodes. Experimental results demonstrate the effectiveness of the suggested SPARK framework utilizing evaluation parameters including delivery rate, delay, overhead, hop count, throughput, complexity, and resource utilization. The delay rate of the proposed SPARK method is 18.67%, 19.87%, and 14.45% is lower than the existing OPRNET, IDRL, and CCMA, techniques respectively. The distribution of the proposed SPARK framework attains a forwarding rate of 11% for selfish, and 9.2% for misleading based on their packet forwarding behavior.

Keywords: Delay Targeted Network; transmission; routing; prediction; communication

Pametno napovedovanje in prenos na podlagi zaupanja v omrežjih z zamikom za letalsko komunikacijo

Izvleček: Omrežje z zamikom (DTN) olajšuje komunikacijo v okoljih z naključno povezljivostjo in dolgimi zamiki, kot so vesoljske misije in izolirane lokacije. Razvoj tehnologije 5G je povečal povpraševanje po storitvah med letom, kar predstavlja izziv za letalsko komunikacijo, da zagotovi zanesljive podatke prek satelitskih sistemov in tradicionalnih makrocelularnih omrežij. Vendar pa dinamična narava letalske komunikacije predstavlja pomembne izzive, vključno z nepravilnimi povezavami in spremenljivimi zamiki. Za reševanje teh izzivov je bila predlagana nova tehnika Smart Prediction and trAnsmission mechanism for delay taRgeted networK (SPARK), ki izboljšuje učinkovitost in zanesljivost DTN v letalski komunikaciji. Predlagana metoda SPARK vključuje celovit sistem ocenjevanja zaupanja vozlišč, ki uporablja neposredne in posredne metrike zaupanja za zagotavljanje zanesljivosti omrežja. Po oceni zanesljivosti vozlišč predlagana metoda omeji promet z veliko obremenitvijo na podlagi zanesljivosti. Modul za napovedovanje in prenos vključuje sistem Cooperative Watchdog System (CWS) za dinamično posodabljanje ocene ugleda vsakega vozlišča. Vozlišča so razvrščena v sodelujoča, delno sodelujoča, nevtralna, zavajajoča in sebična vozlišča. Rezultati poskusov dokazujejo učinkovitost predlaganega okvira SPARK, ki uporablja parametre ocenjevanja, vključno s hitrostjo dostave, zamudo, režijskimi stroški, številom skokov, prepustnostjo, kompleksnostjo in izkoriščenostjo virov. Stopnja zamude predlagane metode SPARK je 18,67%, 19,87% in 14,45% nižja od obstoječih tehnik OPRNET, IDRL in CCMA. Porazdelitev predlaganega okvira SPARK doseže stopnjo posredovanja 11% za sebične in 9,2% za zavajajoče vozlišča na podlagi njihovega vedenja pri posredovanju paketov.

Ključne besede: Mreža z zamikom; prenos; usmerjanje; napovedovanje; komunikacija

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How to cite:
D. Shanmugavel et al., "Smart Prediction and Trust-based Transmission in Delay-Targeted Networks for Aviation Communication", Inf. Midem-J. Microelectron. Electron. Compon. Mater., Vol. 55, No. 4(2025), pp. 219–228

1 Introduction

Delay Targeted Networking (DTN) is a networking protocol that is intended to function well across very long distances and in conditions that conventional networking may find challenging [1,2]. In the realm of aviation communication, the advent of 5G technology has raised passenger expectations for in-flight services [3-5]. Presently, data services for both passenger and airline operations are facilitated through macro-cellular networks, inflight satellite systems, or air-to-ground (A2G) links [6-8]. However, the considerable financial expense and propagation delays associated with satellite communication, notably the Ad hoc Network utilizing Air-to-Air (A2A) radio broadcasts [9-11]. This approach offers power and transmission rate advantages over traditional methods, which is especially crucial for air traffic management and offshore coverage enhancement [12-15].

Despite its potential benefits, the dynamic nature of airborne communication poses significant challenges, including irregular connections, inadequate links, and variable delays during data transfer [16-19]. Moreover, existing research often overlooks the intermittent nature of connections, limiting the exploration of flexible transmission methods and impeding the development of efficient DTNs [20-23]. To address these challenges, this paper focuses on assessing the interactions among key network properties within a DTN framework, considering its fast-changing topology and occasional connectivity. By enabling opportunistic transmissions and employing realistic transatlantic data traces, aim to quantify the efficacy of DTNs, with a particular emphasis on data flow, transmission delays, and system overhead. In this paper, a novel SPARK method has been proposed to enhance the efficiency and reliability of DTNs in aviation communication. The major contributions of the proposed method are as follows:

- Nodes within the DTN are evaluated for trust using both direct and indirect trust metrics.
- After trust evaluation, heavy load traffic is restricted based on node trustworthiness. The prediction and Transmission Module incorporates the CWS which dynamically updates each node's reputation score based on several factors and categorizing nodes into five types: cooperative, partially cooperative, neutral, mislead, and selfish.
- After classification, cooperative, partially cooperative, and neutral nodes proceed to data forwarding.
- This process involves efficiently routing data packets through the network to ensure reliable delivery to the destination node.

The rest of the work are ordered in the following manner. Section II provides the literature evaluation, while Section III describes the proposed methodology. Section IV examines the experiment results. Section V contains the paper's conclusion.

2 Literature review

In recent years, numerous models have been introduced to improve the efficiency of DTNs. This section discusses some of the most prominent models and their respective benefits and limitations.

In 2021, Parameswari et al., [24] introduced OPRNET, an Opportunistic Routing Protocol that utilizes global location data for routing verdicts. OPRNET aims to enhance network capacity, while also increasing distribution opportunities and reducing latency and overhead. In 2021, Chourasia et al., [25] created a routing technique that gives packet scheduling priority over copy distribution counts in the network. The results indicate that the suggested method performs better than the current VDTN routing techniques.

In 2023, Gupta and Khaitan [26] introduced a queueing network model to depict message dissemination in hybrid VANET architecture. The paper offers an analysis of hybrid VANET with two conventional VANET architectures. In 2023, Yu et al., [27] presented a MANET routing technique for high-speed applications. The outcomes demonstrate that the suggested algorithm reducing communication delays by 75% and increasing data arrival rates by 15%.

In 2023, Han et al., [28] presented a hybrid routing technique with dynamic addressing that integrates the concepts of static setup. Then, an analysis and comparison are conducted on the performance metrics of each algorithm. In 2023, Upadhyay et al., [29] presented a routing method for enhanced deep reinforcement learning (IDRL) that minimizes augmented control overhead. The suggested IDRL routing strategy performs better than the innovative in terms of data dependability, PDR, and latency.

In 2024, Nakayima et al., [30] offered a cutting-edge method for improving VANET performance using a centralized-controller multi-agent (CCMA) algorithm that combines Reinforcement Learning (RL) with SDN and DTN principles. Evaluations show that the suggested approach performs better in a variety of VANET circumstances. Table 1 describes the comparison of existing techniques.

Table 1: Comparison of existing techniques

Techniques	Aim	Strengths	Weaknesses
OPRNET [24]	To enhance network capacity, including energy consumption, optimization latency, and storage	Reducing latency and overhead	Increased energy consumption
Routing technique [25]	VDTNs that limits the number of copies distributed to enhance efficiency.	Improved delivery performance, reduced network congestion, and enhanced packet prioritization.	High buffer usage, increased processing overhead.
Queueing network model [26]	Analyze end-to-end delay and backlog in a hybrid VANET	Improving network performance	Increased computational complexity
MANET routing technique [27]	To enhance routing decisions and network stability	Reducing communication delay and increasing data arrival rates	High computational complexity
A hybrid routing technique [28]	To reduce network overhead and increase network longevity	Lower routing discovery delay, and improved reliability.	Increased processing load, and potential routing inefficiencies.
IDRL [29]	To reduce control overhead and transmission delay.	Reduced latency, improved PDR, enhanced data reliability.	Increased resource consumption.
CCMA [30]	Enhance VANET performance	Reduced latency, and better buffer management,	High computational complexity

However, several significant studies have been undertaken on efficiency issues in DTNs. Despite notable advancements, existing approaches exhibit limitations such as scalability challenges, high overhead, complexity, delay, etc. To overcome these challenges, a novel SPARK technique has been suggested in this paper, which is covered in the following section 3 and the subsections.

3 Smart prediction and transmission mechanism for delay-targeted network

In this section, a novel SPARK technique has been suggested to enhance the efficiency and reliability of DTNs in aviation communication.

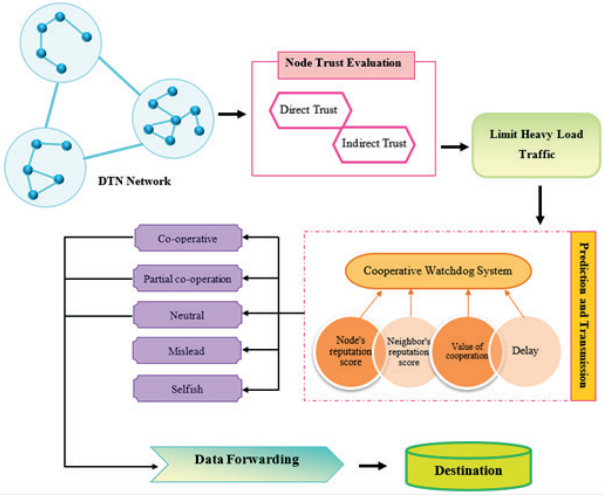

Figure 1: Proposed SPARK Methodology

Direct and indirect trust metrics are used to assess nodes in the DTN for trustworthiness. While indirect trust considers the opinions of nearby nodes to enhance overall network stability, direct trust assesses node behavior based on direct interactions. Following the trust assessment, heavy load traffic is limited according to the trustworthiness of the node. The CWS, which dynamically adjusts each node's reputation score depending on several variables, is incorporated into the Prediction and Transmission Module. Five node categories such as cooperative (class 0), partially cooperative (class 1), neutral (class 2), misleading (class 3), and selfish (class 4) are created from the CWS scores assigned to nodes. Cooperative, moderately cooperative, and neutral nodes move on to data forwarding after classification. Data packets are effectively routed through the network during this step to guarantee dependable delivery to the destination node. The overall workflow of the suggested SPARK model is given in Figure 1.

Node trust evaluation

Nodes' trustworthiness is evaluated through a combination of direct and indirect trust. Direct trust is based on the actual interactions between nodes, while indirect trust considers past behaviors and the level of confidence in those assessments. Ultimately, weighted values of both are used to compute the overall trust value.

3.1 Direct trust (DT)

DT is the immediate impression of the assessed node by the evaluation node. For the direct trust computation, the three elements listed as trust factors, where x stands for trust in the assessed node and y for the node that has to be assessed.

3.1.1 Direct trust bayesian trust degree (BTD)

BTD model uses the trust degree as an arbitrary variable with a possibility circulation to predict future node behavior (posterior) based on past node interactions (prior). The parameter b indicates the number of unsuccessful interactions. Equation (1) gives the Bayesian trust degree, which used to visually represent the node's packet forwarding success rate and trend.

$$BTD_{xy} = \frac{a}{a+b} = \frac{o_s + 1}{o_s + o_u + 2} \tag{1}$$

Where o_s is the record of effective y connections and o_u denotes the record of failed y interactions.

3.1.2 Data similarity degree (DSD)

The degree of comparison among 2 nodes transmitting data is indicated by data similarity; and incorporating resemblance into the trust value control might help mitigate malicious assaults to some extent. The calculation is done using equation (2).

$$DSD_{xy} = \frac{MsgSame}{\left(List_x + List_y\right)/2} \tag{2}$$

Where *MsgSame* indicates how many comparable packets there are between nodes x and y and ($List_x$ + $List_y$)/2 indicates how many packets on average are stored in each node's cache.

3.1.3 Node activity degree (NAD)

The quantity of nodes encountered in a given amount of time determines a node's activity level inside the network. To prevent malicious assaults, node activity is zeroed at the beginning of each unit time. This is its calculating in equation (3).

$$NAD_{xy} = \frac{t}{\varnothing} \times \frac{Internum}{No} + \left(1 - \frac{t}{\varnothing}\right) \times NAD_{xyOld} \tag{3}$$

Where *t* is the time in units, *Internum* is a representation of the number of nodes encountered in the network. The entire number of nodes in the present network is denoted as *No* and NAD_{xyOld} is the activity of the node at the most recent reset. As a result, equation (4) can be used to define the DT value (D).

$$D_{xy} = V_1 \times BTD_{xy} + V_2 \times DSD_{xy} + V_3 \times NAD_{xy} \tag{4}$$

The weight coefficients are the parameters V_1, V_2 and V_3. Depending on the network environment, the weights may have varying values allocated to them.

3.2 Indirect trust

A Node x should reflect the "view" of neighboring nodes on y, just like in social life, to evaluate node y more completely. Let x and y be two nodes that have neighbors in common. The trust threshold is determined by averaging the trust values found in the node x's trust table, which is given in equation (5).

$$H_{threshold} = \frac{\sum_{i=1, i\neq x}^{m} H_{xi}}{m-1} \tag{5}$$

Where H_{xi} is the node x's direct trust value to its common neighbor nodes, where m is the number of common nodes at present. Afterward solving equation (5), m co-neighboring nodes remain. The departure of the number of contacts between node y and nearby nodes from the number of connections between node x and node y, which is determined as in equation (6).

$$\rho = \frac{\sqrt{\sum_{r=1}^{n}\left(IN_{r,y} - IN_{x,y}\right)^2}}{n} \tag{6}$$

$$I_{xy} = \frac{\sum_{i=1}^{c} D_{x,i} \times D_{i,y}}{c} \tag{7}$$

The above equation (7) provides the ultimate indirect trust computation algorithm. Where ρ defines the calculated metric, *n* represents the total number of elements, $IN_{r,y}$ is the number of interactions that a neighbor node r has had. At node r, the "view" will be deemed invalid if $IN_{r,y} < IN_{x,y-} - \rho$, c indicates the remaining shared neighbor nodes.

3.3 Limit heavy load traffic

Limiting heavy load traffic after Node Trust Evaluation involves a crucial assessment process aimed at enhancing network reliability and security. This ensures that only nodes deemed trustworthy are allowed to handle heavy loads, thereby reducing the risk of network congestion, and potential breaches. Once heavy load traffic is limited, it enters the prediction and transmission phase where nodes are categorized for efficient data transmission.

3.4 Prediction and transmission

After reducing heavy traffic load, optimized input is fed into the prediction and transmission phase for efficient data transfer. The core of the Prediction and Transmission module is the CWS, which aims to ensure network access while identifying non-compliant nodes. The node's reputation score (RSI), its neighbors' reputation score (RS_N), a value of cooperation offered by the watchdog (CV_W), and Delay. The node's associated cooperative value (CV_W). Eq. (8) determines a cooperative value for node *n*.

$$CV_{w_n} = \beta.\gamma_n \tag{8}$$

Where γ represents the punctuation that the classification module assigns to node *n* is the node performance coefficient represented by β. Eq. (9) is used by the classification module to generate this value, where R_{Bi} is the number of bundles that have been relayed from node *i*, D_{Bi} is the number of packages that have already been delivered from node *i* and D_{pBi} is the number of bundles that have already been dumped from node *i*. Eq. (10) is used to determine the value.

$$x = \frac{\sum_{i=I}^{N}\left(R_{B_i} - D_{B_i}\right)}{\sum_{i=I}^{N}\left(R_{B_i} - DP_{B_i}\right)} \tag{9}$$

$$\beta = \frac{x - \min\left(x\right)}{\max\left(x\right) - \min\left(x\right)} \tag{10}$$

The neighbor assessment module establishes the RS_N of each node. The module for neighbor evaluation polls *N* neighbors (N_g) for feedback on the participating nodes at each contact opportunity. These neighbors provide the corresponding RS_N value in response to the evaluation module request from the neighbor. Each time a neighbor creates a direct communication channel with a node (*n*), the node's RS_N value is modified is given in equation (11).

$$RS_N\left(n\right) = \frac{\sum_{i=I}^{N} RS_{R_i}}{N} \tag{11}$$

The reputation score that the node itself (RS_I), the neighbor's evaluation module (RS_N), and the categorization module (CV_W) have seen are all taken into consideration by the decision module when updating a network node's reputation score () following a contract opportunity. An updated node reputation scores (∞_n) which is the sum of the three ratings and is determined as follows in equation (12).

$$\propto_n = \theta.RS_{I_n} + \left(I - \theta\right).RS_{N_n} + CW_{W_n} \tag{12}$$

where ∞_n represents the degree to which the CWS relies on nodes' self-reported observations and ranges from [0,1]. The classification module updates its classification table after receiving the decision module's updated nodes' reputation scores. Using this score finally the nodes are classified into 5 types they are class 0, class 1, class 2, class 3, and class 4. Subsequently, the classified output is transferred to the data forwarding phase.

3.5 Data forwarding

After node prediction, if classified as class 0, class 1, or class 2, nodes proceed to data forwarding. Immediate neighbors of the downstream node assist in this process. The next upstream sender is noted in the failed node's Pending Credit Table. Once the forwarder timer expires, a neighboring node broadcasts the data packet to lower-layer nodes using the credit table. When the designated lower-layer node retransmits the packet, nearby nodes with the same data in their credit table delete their cache and stop their timers. This process reduces transmission delays, prevents redundant transmissions, and enhances the interest satisfaction ratio. The process of data packet forwarding and routing is shown in Figure 2.

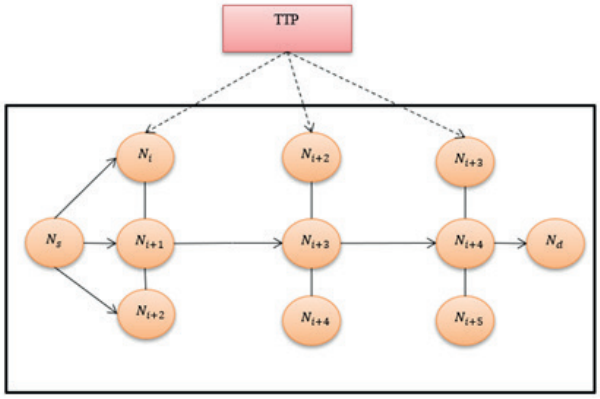

Figure 2: Data forwarding and routing mechanism

Algorithm: Proposed SPARK model data forwarding in DTN network
Input Data: DTN network topology, Node interaction data, Trust evaluation parameters
Output: Data forwarding to the destination
Step-1: Initialize the DTN network and establish communication links.
Step-2: Perform node trust evaluation
Step-2.1: Determine direct trust based on the past node interactions (prior) using equation (1)
Step-2.2: Determine indirect trust from neighboring nodes using equation (5).
Step-3: Limiting heavy load traffic to enhance network reliability and security
Step-4: Perform prediction and transmission to identify optimal paths.
Step-4.1: Compute the node's reputation score based on forwarding behavior
Step-4.2: Analyze neighbor's reputation score to assess cooperation level
Step-4.3: Evaluate the value of cooperation to identify malicious nodes
Step-4.4: Measure delay to detect misbehavior
Step-5: Classify the network nodes using cooperative watchdog system (CWS)
Step-6: Forward data based on trust scores and cooperative behavior
Step-7: Deliver data to the destination efficiently and securely.

4 Results and discussion

The suggested SPARK model's simulation findings are examined and a discussion of efficacy is done in terms of numerous evaluation parameters within this section. The effectiveness of the proposed SPARK method is tested using the ONE (opportunistic network environment) simulator. The efficacy of the suggested SPARK approach is examined using four metrics: hop count, overhead, delivery ratio, delivery delay throughput, complexity, and resource utilization. All of the significant factors that were utilized in the simulation are enumerated in Table 2.

Figure 3 presents the distribution of the proposed SPARK model categories based on their packet forwarding behavior. This provides how node behaviors are evaluated and categorized within the DTN. A cooperative node is defined as one that forwards packets in 39.4% of interactions, while a partially cooperative node forwards packets in 26.6% of the time. Nodes that attain a forwarding rate of 13.8% are neutral, and misleading nodes are forward less than 9.2% of packets. Finally, selfish nodes that function correctly in 11% of interactions within the DTN.

Table 2: Parameter setup

Parameter	Value
Region	5000m*5000m
Data size	500 KB
Interval	40s
TTL	4 hours
Time	10 hours
Transmission range	10 m
Transmission speed	250 KB/s

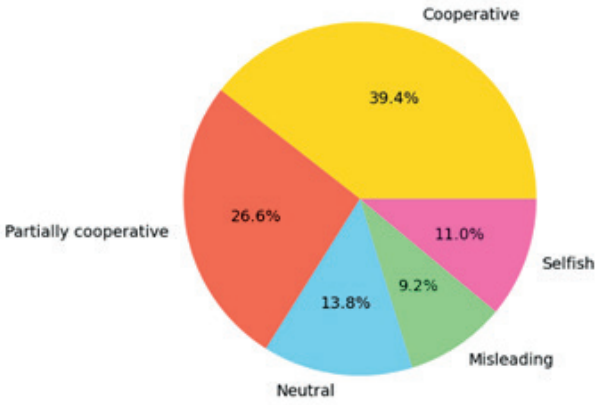

Figure 3: Classification distribution of the proposed SPARK framework

4.1 Comparative analysis

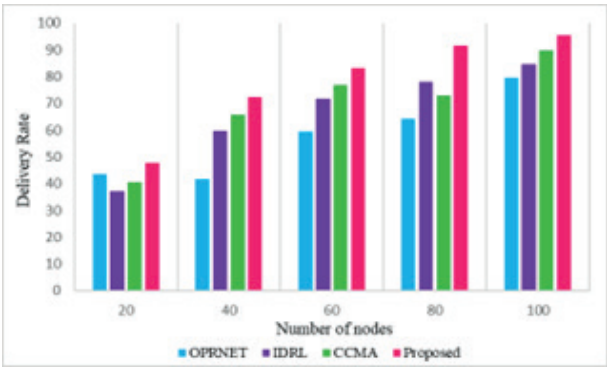

Figure 4: Comparison in terms of delivery rate

Figure 4 illustrates a comparison of delivery rates between existing methods and the proposed SPARK method. Our proposed work effectively minimizes the packet drops by utilizing an optimized routing mechanism, which selects the most reliable route dynamically. This demonstrate that the greater performance of

the proposed SPARK method in ensuring higher delivery rates under the given conditions.

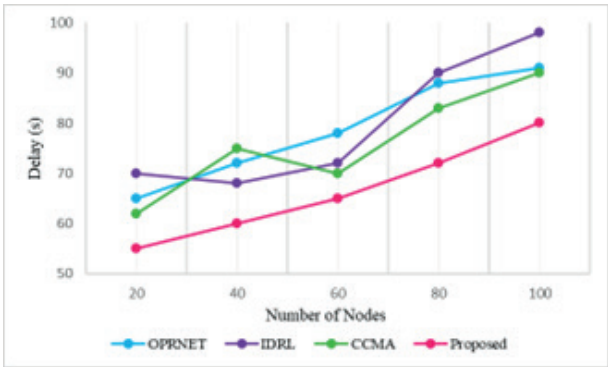

Figure 5: Comparison in terms of delay

Figure 5 presents a comparative analysis of delay times with existing techniques and a proposed method. By implementing the efficient path selection, our proposed SPARK method reduces the time required for packet transmission. The delay rate of the proposed SPARK method is 18.67%, 19.87%, and 14.45% is lower than the existing OPRNET, IDRL, and CCMA techniques respectively.

Figure 6 illustrates a comparative analysis of overhead. For reducing the network control traffic, the suggested work employs a routing mechanism through optimized control message transmission. It shows that the suggested model's effectives significant efficiency in reducing overhead, highlighting its potential advantages over the other methods.

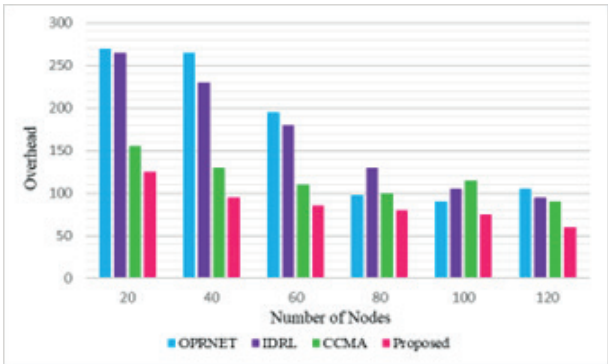

Figure 6: Comparison in terms of overhead

Figure 7 presents a comparison of hop counts. The proposed method constantly attains advanced hop counts associated with the other protocols, particularly noticeable at larger network sizes. OPNET consistently results in the lowest hop counts across all network sizes, demonstrating a more efficient routing performance in terms of hop count.

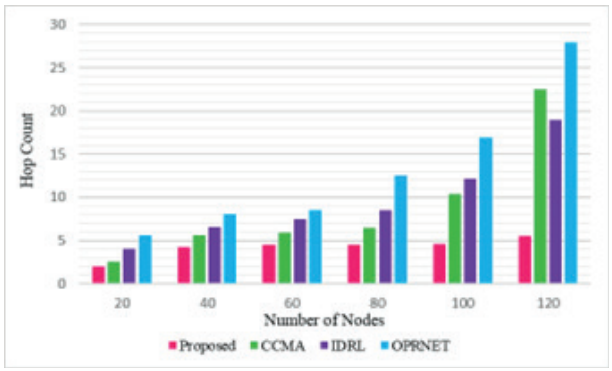

Figure 7: Comparison in terms of Hop Count

Figure 8 illustrates a comparison of throughput among the proposed SPARK method and the existing methods. The proposed SPARK method maintains a relatively stable and high throughput. Overall, the proposed SPARK method shows superior presentation in terms of maintaining consistent and high throughput related to the other protocols.

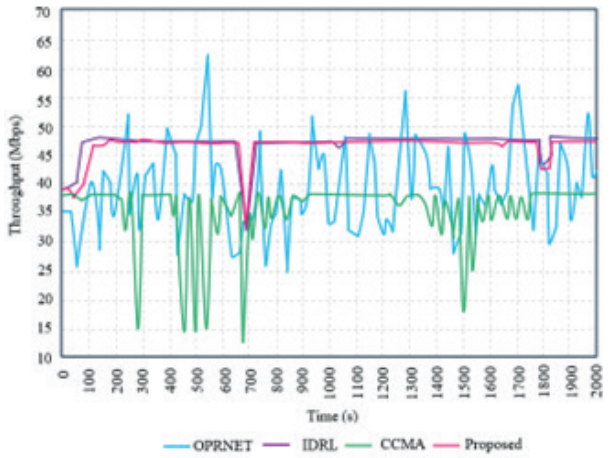

Figure 8: Comparison in terms of Throughput

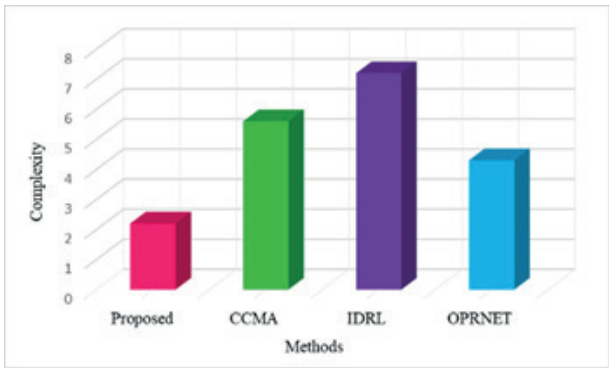

Figure 9: Comparison in terms of Complexity

Figure 9 illustrates the comparation of complexity between the suggested SPARK approach and current methods. The proposed method shows the lowest complexity, while IDRL is the most complex. This shows

the proposed SPARK method's maintaining lower complexity compared to the others.

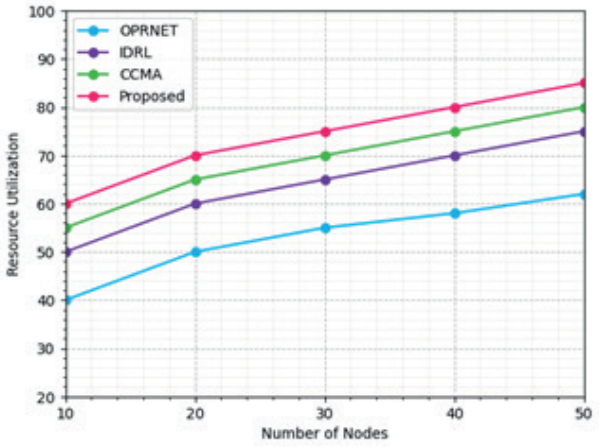

Figure 10: Comparison of Resource utilization

Figure 10 shows the comparation of resource utilization between the proposed SPARK method and existing approaches. It is evident that the Proposed model consistently achieves higher resource utilization across all node counts compared to the other models. The increasing trend in resource utilization for all Models indicates that they scale with the number of nodes, with the Proposed model demonstrating superior efficiency and scalability.

5 Conclusions

In this paper, a novel SPARK technique has been proposed to enhance the efficiency and reliability of DTNs in aviation communication. By incorporating a robust node trust evaluation system, the methodology ensured that only trustworthy nodes handle heavy traffic loads, thereby enhancing overall network security and performance. The proposed SPARK method was assessed using various performance parameters including delivery rate, delay, overhead, hop count, throughput, complexity, and resource utilization. The proposed SPARK approach consistently achieved higher delivery rates, lower delays, reduced overhead, and higher hop counts, indicating its effectiveness in managing the unique challenges of DTNs in aviation environments. The delay rate of the proposed SPARK method is 18.67%, 19.87%, and 14.45% is lower than the existing OPRNET, IDRL, and CCMA, techniques respectively. Future research should focus on integrating AI and machine learning methods for anomaly detection, traffic control, and predictive analytics to further improve the resilience and effectiveness of DTNs.

6 Acknowledgments

The author would like to express his heartfelt gratitude to the supervisor for his guidance and unwavering support during this research for his guidance and support.

7 Conflict of interest

No financial or interpersonal conflicts have been reported by the authors that would have affected the study's finding

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Arrived: 05. 10. 2024
Accepted: 01. 10. 2025

Original scientific paper
https://doi.org/10.33180/InfMIDEM2025.403

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 55, No. 4(2025), 229 – 238

A Wireless Optical Gate and IMU System for Agility Assessment: Architecture, Synchronization and Validation

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Abstract: Accurate, field-ready timing and motion capture are essential for assessing agility beyond the limits of manual stopwatches. We present a modular measurement system that fuses infrared (IR) optical gates for robust event detection with a trunk-worn inertial measurement unit (IMU) for kinematic profiling. Each sensing node is built on an Adafruit Feather M0 Wi-Fi microcontroller and communicates via UDP to a laptop server. Time alignment is accomplished without internet connectivity: the server establishes a relative epoch and executes a triple-handshake broadcast protocol, while timestamps are generated at the edge to avoid latency bias from transport or processing. Module- and device-level characterization shows that IR-receiver processing combined with interrupt service routine latency yields a per-event timestamp error of 0.54 ms ± 0.14 ms (latency ± uncertainty), and local clocks remain stable over the durations relevant to agility trials. In wireless operation, accepted synchronization attempts form tight response clusters in favorable RF conditions, whereas congested environments may require retries; for section times across different gates we therefore report a conservative inter-node uncertainty. End-to-end validation across laboratory, entry-hall, and gym venues using the Agility T-test confirms that total test time measured on the same start/finish gate remains below 1 ms error over 10–20 s trials. Synchronized IMU waveforms add explanatory value beyond total and split times by revealing braking, change-of-direction, and re-acceleration phases. The system provides a deployable workflow with substantially improved precision over manual timing. Future work will target more robust synchronization and expanded analytics, including automated phase detection, asymmetry indices, and optional integration with indoor positioning.

Keywords: infrared gates; IMU; embedded systems; wearable sensor device; wireless synchronization; agility testing

Brezžični sistem za ocenjevanje agilnosti na osnovi optičnih vrat in kinematičnih senzorjev: arhitektura, sinhronizacija in validacija

Izvleček: Natančno merjenje časa in zajem gibanja na terenu sta ključna za ocenjevanje agilnosti onkraj omejitev ročnih štoparic. Predstavljamo nizkocenovni, modularni merilni sistem, ki združuje infrardeča (IR) optična vrata za robustno zaznavanje dogodkov in na trupu nameščeni inercialni merilni senzor (IMU) za kinematično profiliranje. Vsako merilno vozlišče temelji na mikrokrmilniku Adafruit Feather M0 Wi-Fi in z uporabo UDP komunicira s strežnikom na prenosniku. Časovno uskladitev izvedemo brez internetne povezave: strežnik vzpostavi relativno epoho in izvede oddajni protokol s trojnim rokovanjem, medtem ko se časovni žigi tvorijo na robu sistema (na napravi), da se izognemo pristranskosti zaradi zakasnitev prenosa ali obdelave. Karakterizacija na ravni modulov in naprav pokaže, da kombinacija obdelave v IR sprejemniku in zakasnitve prekinitvene rutine prinese napako časovnega žiga na dogodek 0.54 ms ± 0.14 ms (zakasnitev ± negotovost), lokalne ure pa ostanejo stabilne v časovnih intervalih, pomembnih za preizkuse agilnosti. Pri brezžičnem delovanju sprejeti poskusi sinhronizacije v ugodnih RF-razmerah tvorijo tesne skupke odzivov, medtem ko v zasičenih okoljih lahko zahtevajo ponovitve; zato pri časih odsekov med različnimi vrati navajamo večjo negotovost. Celovita validacija v laboratoriju, avli in telovadnici z uporabo T-testa agilnosti potrjuje, da ima skupni čas testa, izmerjen na istih začetnih/končnih vratih, napako manjšo od 1 ms pri poskusih, dolgih 10–20 s. Sinhronizirani IMU signali dodajo pojasnjevalno vrednost onkraj skupnih in delnih časov, saj razkrivajo faze zaviranja, menjave smeri in ponovne pospešitve. Sistem omogoča enostavno uvedljiv potek dela z bistveno izboljšano natančnostjo v primerjavi z ročnim merjenjem. V prihodnje načrtujemo še zanesljivejšo sinhronizacijo in razširjeno analitiko, vključno s samodejnim zaznavanjem faz, indeksi asimetrije ter po potrebi integracijo s pozicioniranjem v zaprtih prostorih.

Ključne besede: infrardeča vrata; IMU; vgrajeni sistemi; nosljiva senzorska naprava; brezžična sinhronizacija; testiranje agilnosti

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How to cite:
A. Kos et al., "A Wireless Optical Gate and IMU System for Agility Assessment: Architecture, Synchronization and Validation", Inf. Midem-J. Microelectron. Electron. Compon. Mater., Vol. 55, No. 4(2025), pp. 229–238

1 Introduction

Time–motion tests, especially change-of-direction (COD) tasks, remain a staple of field-based performance assessment because they are simple to administer and show good reliability and construct validity across sporting populations [1]. One example of COD task is T-test studied in this work. However, manual timing introduces human start and stop reaction latency and split-time variability when compared with electronic solutions [2]. Infrared (IR) timing gates and photoelectric cells help reduce operator delay, but their accuracy can still be affected by several factors. Athlete posture (e.g., knee or arm swing), beam geometry, and starting procedures can interfere with triggering, and performance also differs between single- and dual-beam configurations. Recent systematic evidence further shows that commercial systems can produce significant offsets and are not universally comparable, particularly during the first 5–10 m of acceleration of the linear speed test [3].

In parallel, inertial measurement units (IMUs) have become a practical way to capture kinematics in environmentally valid settings. A 2021 scoping review concluded that IMUs can quantify COD performance, but highlighted heterogeneity of metrics and the need for rigorous validation in sport-specific tasks [4]. Newer studies have started to fill this gap: single-sensor wearables can segment COD and derive interpretable performance markers in the field [5]; multi-IMU systems can capture lower-limb kinematics with high sagittal-plane agreement to optoelectronic references, albeit with greater error in frontal and transverse planes [6], [7]; and foot-mounted IMUs show promising validity for velocity tracking in team sports [8]. There is also growing interest in combining IMUs with phone-based markerless methods to balance practicality and accuracy [9].

A persistent systems-engineering challenge is precise time alignment across distributed, wireless nodes so that timing-gate events and IMU signals are fused without drift. Energy-efficient clock discipline for Wi-Fi/IoT devices has been proposed (e.g., ecoSync) to trade synchronization accuracy for battery life in multi-sensor settings [10]. Precision Time Protocol (PTP) over Wi-Fi can reach microsecond-level accuracy with careful tuning/hardware support, but performance depends on network interface capabilities and timestamping paths [11], while Network Time Protocol (NTPv4) remains a robust baseline for general deployments [13]. When spatial context is needed (e.g., split timing plus trajectories), Ultra-Wideband (UWB) real-time locating systems are an established option for indoor positioning with high update rates and robustness to multipath [12].

Motivated by the lack of systems that provide synchronized timing gate events and IMU signals in real-world settings without Internet access, and aiming for a low-cost, hardware-independent solution, we present a wireless synchronized sensor system that integrates (i) IR gates for robust, low-latency location-bound event timing, (ii) body-worn IMUs for rich kinematic profiling, and (iii) a synchronization layer to ensure sub-frame timestamp coherence across nodes. Building on our prior engineering work that demonstrated millisecond-level timing accuracy at the device level [14], we target sports-relevant tasks (e.g., agility tests) where both total time and movement quality matter.

Our contributions are: (1) a low-cost, modular, field-deployable architecture that unifies IR-gate events and IMU streams under a common clock, (2) a synchronization strategy compatible with commodity Wi-Fi while remaining energy-aware, and (3) an analysis pipeline that provides both standard split times and additional kinematic micro-metrics of execution.

2 Background & related work

Timing technologies. Manual timing is convenient but systematically biased relative to electronic systems [2]. Photoelectric timing gates reduce operator error, but the height of the beam and the number of beams, the starting protocol and the morphology of the object affect the triggers and thus the measured times. A recent systematic review found that double-beam gates reduce false triggers more effectively than single-beam systems. It also reported that different systems are not always interchangeable, particularly in the early acceleration phase. This emphasizes the need to specify device models and setups in studies [3]. Recent validation studies characterize the differences between systems (e.g. Chronojump vs. Witty) and propose fitting equations for comparability [3].

Wearable sensing for agility tests. IMUs are widely used to capture movement quality alongside total time. The scoping review by Alanen et al. summarizes reliability/validity evidence and calls for standardized metrics in COD analysis [4]. Subsequent work shows that a single trunk-worn GNSS-IMU can decompose standard agility tests into interpretable phases [5], while laboratory-grade comparisons indicate high waveform agreement in the sagittal plane and task-/plane-dependent limitations elsewhere [6], [7]. Foot-mounted IMUs have been shown to provide valid measurements of velocity in team sports [8]. Early studies also suggest they can work well alongside modern phone-based markerless systems [9].

Clock synchronization and spatial context. Multisensor fusion in the field depends on stable sub-millisecond alignment. Energy-aware Wi-Fi synchronization (ecoSync) reduces overhead for battery-powered nodes [10]; PTP over Wi-Fi can reach ≈1 µs accuracy with careful engineering, though commodity hardware support is uneven [11], while NTPv4 remains a practical, standards-based baseline [13]. For positioning, UWB RTLS offers accurate, robust indoor tracking and is widely reviewed for real-time deployments [12].

Compared with timing-only protocols that report total or coarse split times and remain sensitive to beam setup and inter-system offsets [1]–[3], our approach fuses robust IR-gate events with IMU signals under a common clock. This yields not only how much time was spent, but where and why within each section; IR gates also curb the segmentation uncertainty that affects IMU-only pipelines [4]–[9]. We further quantify the full error budget, per-device measurement error, local clock drift, and inter-node synchronization, so uncertainties propagate to both total and section-level metrics.

In our system, we implement lightweight Wi-Fi synchro-nization positioned between NTP (practically ms-level, but dependent on the network connection) and hardware-assisted PTP (µs-level, but less commodity-friendly) [10], [11], [13], along with edge timestamping, compact UDP transport, and a stable time base. In practice, this provides sub-ms device coherence and explicitly characterized uncertainty between nodes in congested RF environments. This results in a field-suitable workflow for agility testing with comparable times and explanatory IMU waveforms [3], [5]–[9]. Thus, our solution is comparable to NTP, but network independent, and although less accurate than PTP, it is independent of specific network interface functionalities.

3 Materials and methods

3.1 System architecture

The system shown in Figure 1 comprises (1) distributed measurement nodes of two different types: IR timing gates and a wearable IMU unit, (2) a laptop server connected to (3) a Wi-Fi access point (AP). Nodes transmit ASCII-encoded UDP packets to the server; UDP was chosen to minimize head-of-line blocking and reduce latency from acknowledgments. As the system operates without connection to the internet, synchronization does not use NTP; instead, devices align to a relative time established by the server at a synchronization instant. Devices are uniquely identified and assigned roles (gate index, wearable) by the server before a trial.

3.2 Hardware

Microcontroller & radio. Each mobile node (IR timing gates and wearable IMU devices) uses an Adafruit Feather M0 Wi-Fi microcontroller board (SAMD21 + ATWINC1500) [15]–[17]. The AP used in development was a TP-Link Archer C7 (802.11b/g/n); the server is wired to the AP for stability and reduced radio use.

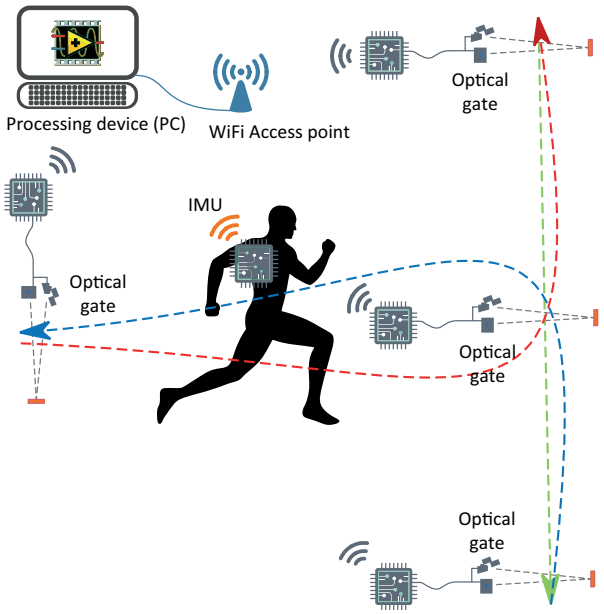

Figure 1: System architecture with a processing device (server), multiple IR optical gates, wearable IMU, Wi-Fi Access point. Configuration showing a T-test case.

IR timing gates. Gates consist of a 940 nm IR emitter and modulated receiver (IS471F), see Figure 2. The IS471F's data sheet specifies a 400–670 µs internal processing delay, i.e., an absolute uncertainty of up to ±135 µs around a ~535 µs mean [18].

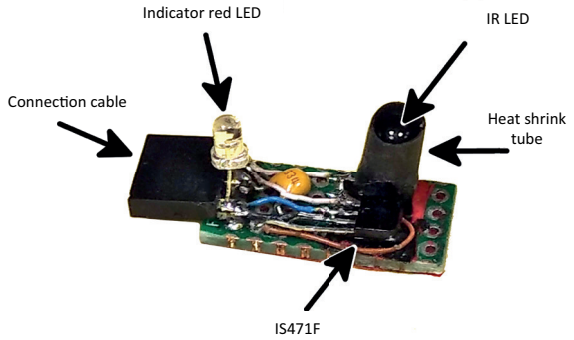

Figure 2: IR timing gates.

Wearable IMU. We used LSM6DS33 (accelerometer & gyroscope, set to ±16 g and ±2000 dps, 100 Hz) and BNO055 (orientation/acc/gyro/mag, 100 Hz) mounted

at users' lower back, near the center of mass of the body. Logged channels, depending on a sensor, include fused orientation, linear acceleration (gravity-compensated), raw accelerometer/gyroscope, magnetometer, and battery voltage [21], [22].

3.3 Firmware and communication

Node operation. Gate crossings trigger interrupts that immediately store the local timestamp and raise a flag; packet assembly and transmission occur in the main loop to keep interrupt service routines (ISRs) minimal. IMU sampling follows a fixed-interval loop (read LSM → read BNO → check send window → send). Both flows are implemented as lightweight state machines.

Server application. The LabVIEW program manages (1) synchronization exchanges, (2) receive loops for UDP, (3) role assignment and configuration, and (4) logging and live visualization. The code modules and GUI tabs for sync/config and packet reception are documented with block diagrams and front-panel screenshots [14].

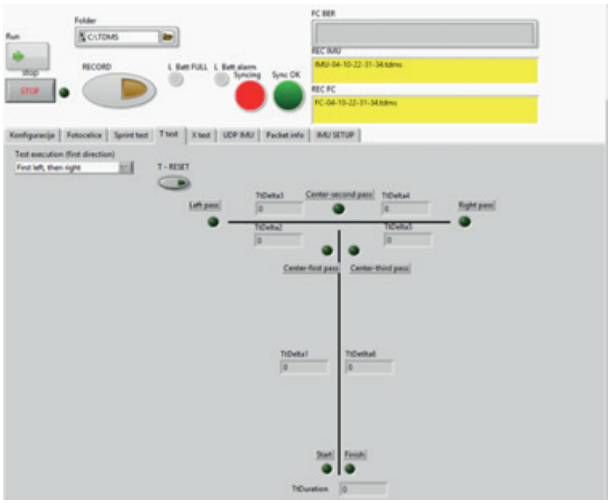

Figure 3: Appearance of the LabVIEW application graphical interface when performing a T-test.

3.4 Time measurement accuracy

During operation, the system's primary function is time measurement; either for event stamping or sensor sampling. Owing to imperfections, timing errors arise at both intra- and inter-device levels. We decompose the total timing error into: (a) electronics, (b) local clock drift, and (c) inter-node synchronization.

For intra-device outcomes, only (a) and (b) are relevant. A typical case is the total test time when the athlete starts and finishes at the same gate (as in our T-test); synchronization error is irrelevant because the result derives from timestamps produced by a single gate. For inter-device outcomes, e.g., partial (split) times between successive gates, component (c) is critical, since the result combines timestamps from different, imperfectly synchronized nodes.

Notably, processing and communication latencies do not bias timestamp accuracy. As illustrated in Figure 4, delays in the system stem from sensor device, microcontroller processing, communication, and the processing device. Only the first contributes to time-measurement error; the others affect overall system performance and are therefore not analyzed further in this paper.

Figure 4: Delay sources in the system.

3.5 Device synchronization

During system development, two synchronization methods were implemented: (a) wired and (b) wireless.

In the wired approach, all devices (optical gates or wearable sensors) are physically connected to a synchronization apparatus that provides a common trigger signal simultaneously, as shown schematically in Figure 5. This method is suitable when the test setup allows straightforward handling of optical gates and wearable sensors.

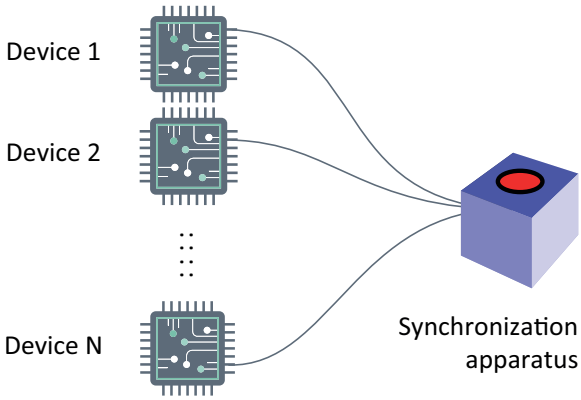

Figure 5: Wired synchronization scenario in which an apparatus drives the sync signal for gates/sensors.

In the wireless approach, the processing device broadcasts a Wi-Fi synchronization packet to all mobile nodes. This method is particularly advantageous when regular synchronization is needed but physical manipulation of the gates and/or wearable devices is impractical, or when time constraints limit access to athletes,

as is often the case with elite teams. To address these scenarios, we developed and implemented a triple-handshake synchronization protocol:

- The server is configured with the number of microcontrollers in the system (*N*).
- Before each measurement, all microcontrollers wait for a synchronization packet.
- The server initiates synchronization by broadcasting a packet containing the current synchronization attempt index (0–9).
- Upon reception, each microcontroller records its current local time from system startup.
- Each microcontroller responds to the server with a packet that includes the synchronization attempt index.
- Once the server has received responses from all *N* nodes, it broadcasts a confirmation packet to conclude synchronization.
- Each microcontroller then stores the most recent recorded timestamp as t_0, which is used as the reference time for subsequent measurements.

The messages used in this protocol are defined as:

- TREQ-N: server synchronization request with attempt index *N*,
- TRESP-N: microcontroller response to synchronization attempt *N*,
- TSUCC: server broadcast confirming successful synchronization to all nodes.

Protocol diagrams for the server and device sides are shown in Figure 6. The server controls communication by sending TREQ and TSUCC messages based on the number of successfully received responses from the devices (TRESP) and any possible timeouts. If the maximum number of unsuccessful synchronization attempts is reached, synchronization ends and the user is notified. Some internal operations, such as setting the local time or advancing counters, are not shown in the diagram.

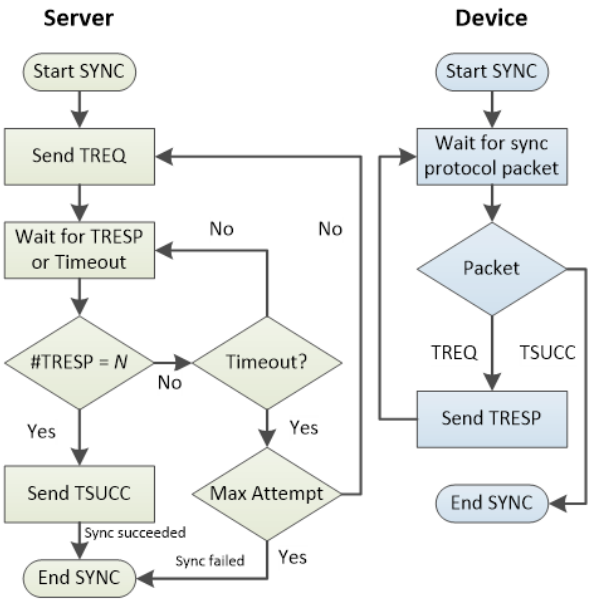

Figure 6: Server and device side protocol diagrams.

Figure 7 illustrates the synchronization process of an example system with four devices, showing one failed and one successful synchronization attempt. The initial synchronization request, TREQ-0, at time t_{r0} receives only three responses, TRESP-0, at the server, resulting in a failed attempt. After the protocol timeout, the next attempt, TREQ-1 at time t_{r1} succeeds, as all four responses TRESP-1 are received. The successful synchronization is communicated to the devices with the confirmation message TSUCC.

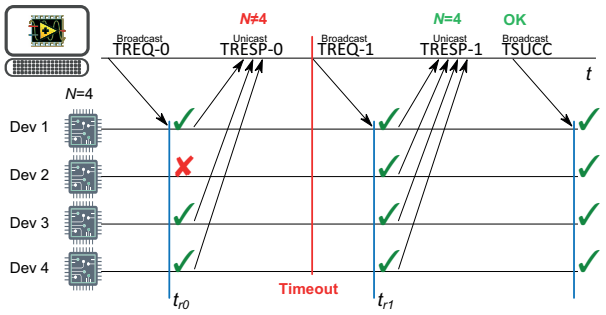

Figure 7: Triple-handshake synchronization protocol.

4 Results

The focus in this section is on time measurement and synchronization inaccuracies and not on the actual athletes' results of the performed agility tests.

4.1 Agility T-test

Agility T-test trials were conducted in three environments: the laboratory (device functionality testing), the faculty entry hall (initial system validation), and the gymnasium (real-world conditions). The configuration of optical gates for the left-side execution is shown in Figure 8. In this mode, the athlete turns left after the first passage through gate 2. Both IMUs were configured as described previously (LSM6DS33 at 100 Hz; BNO055 at 100 Hz). Field measurements outcomes are reported as split times and basic kinematic signals [14]. Detailed sport-science interpretation is planned in collaboration with domain experts.

4.2 Device-level timing measurements

As noted in Section 3.2, the IS471F introduces an internal processing delay of 400–670 µs (mean ≈ 535 µs),

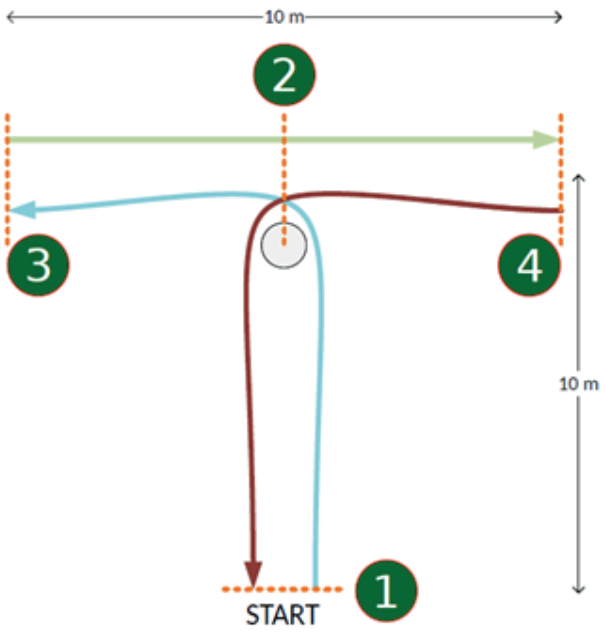

Figure 8: Setup of measurement gates for the T-test: green circles indicate the sequential numbering of gates for the left-side execution.

yielding an absolute uncertainty of ± 135 µs as specified in the data sheet [18]. Digital toggling contributes < 100 ns and is therefore negligible [14]. Oscilloscope measurements show a constant ISR entry latency of ≈ 1.6 µs from input edge of the IR optical gate signal to the first MCU output transition (Figure 9). Together, the per-event timestamp at a gate is 536.6 ± 135 µs (mean latency ± uncertainty).

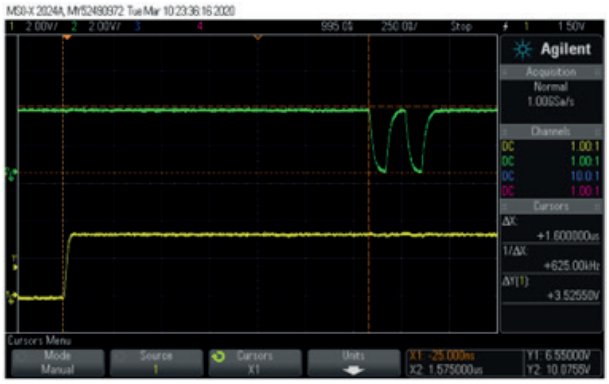

Figure 9: Oscilloscope screenshot of interrupt service routine latency measurement. The yellow trace shows the signal at the digital input, while the green trace represents the signal at the digital output of the microcontroller.

4.3 Microcontroller clock drift

When assessing timing performance, a fundamental question is whether the obtained results can be regarded as reliable. If the measurement clock exhibits excessive error, deviations may accumulate over longer intervals and exceed acceptable limits. To address this, we evaluated the clock accuracy of the microcontrollers used in our measurement system, which depends on quartz crystal tolerances.

As shown in Figure 10, four microcontrollers were tested. Following thermal stabilization, the devices were synchronized, and a series of measurement episodes was performed to monitor differences in recorded times relative to the initial synchronization. After approximately 400 s of operation, individual devices exhibited drift of up to ±2.5 ms, corresponding to about 6.25 µs/s. At this rate, a single microcontroller would accumulate a timing error of 1 ms in roughly 160 s, what is more than suitable for standard agility tests that generally do not last more than 20 s.

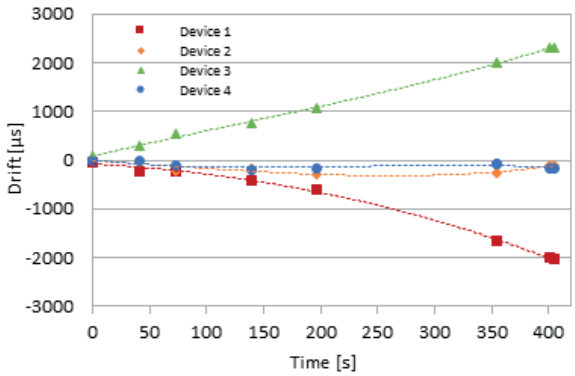

Figure 10: Deviation of microcontroller clocks within a 400 seconds interval relative to the average event time.

4.4 Synchronization error

Because the system is not connected to the internet, devices are not disciplined to absolute time. The server sends a synchronization request; devices record local times on receipt and reply, after which the server assigns a relative epoch and estimates offsets and rates per device.

In wired scenarios, synchronization errors are in the range of microseconds and are therefore negligible. In wireless scenarios, the errors can become much larger. By conducting measurements of the delay of the triple handshake protocol in different environments, we obtained these results. In favorable RF conditions (gym), the inter-device spread during sync was ≈45–55 µs. Under congested RF (faculty hall), sync quality degraded to several milliseconds and many retries were needed. Conservatively, we report an upper-bound system-level synchronization term of 15 ms ± 10 ms for inter-node section times. Unfavorable results can be improved via a dedicated radio channel [14].

4.5 End-to-end and section timing accuracy

Combining electronics delay, ISR latency, local drift and favorable synchronization, we can see that: (a) the error for total T-test time, which is of duration between 10 and 20 seconds, remains well below 1 ms, and (b) for section times spanning different gates we propagate the drift and sync terms alongside device-level error when reporting uncertainty. In favorable RF conditions the clock drift and synchronization error add less than 100 µs, while in unfavorable conditions the additional error can be up to 25 ms (conservatively).

4.6 System validation

We validated the system in stages: module, device, network, and end-to-end. We used procedures designed to mirror real use and to isolate each source of uncertainty reported in Sections 4.2–4.5.

Module level. To characterize sensing and stamping, we drove controlled interruptions of the IR beam and observed the signal path with an oscilloscope: IR receiver output → MCU interrupt pin → ISR entry marker (test firmware toggles a GPIO on ISR entry). This bench setup verified that timestamps are produced at the interrupt edge, that ISR handling is constant across repeats, and that transport/processing downstream (UDP, server logging) does not bias event times. The resulting timing budget is summarized in Section 4.2 and in Figure 9.

Device level. To evaluate clock stability independently of networking, four microcontrollers were wired in parallel to a common trigger that emulates an optical-gate event. After thermal stabilization and an initial sync, we issued repeated triggers at variable intervals and compared each node's recorded time to the run's reference trace. This procedure reveals relative drift and informs the practical re-synchronization policy used in trials (Figure 10).

System level. Wireless synchronization was exercised with the triple-handshake procedure (Figure 7). Before each trial, the server broadcast a sync request; nodes stamped local receipt time and replied; the server accepted the attempt only if responses formed a tight cluster (indicating near-simultaneous delivery). Otherwise, the attempt was retried. This acceptance–retry policy was tested in two RF environments (quiet gym, congested hall) and motivates the conservative inter-node term we propagate for section times (see Section 4.4).

End-to-end (T-test workflow). Finally, we validated the complete workflow across the three venues used in this study: laboratory shakedown, entry-hall pilot, gym deployment (real-world conditions). Each trial began with node discovery and sync, followed by execution of the left-side Agility T-test layout (Figure 8). Quality control included: (i) internal consistency checks (sum of section times vs. total time from the start/finish gate), (ii) visual alignment of IMU bursts with gate crossings on the server UI, (iii) trial-level flags for atypical packets or missed replies, and (iv) manual time measurement with a stopwatch. Because timestamps are generated at the edge (ISR), measured network and processing latencies affect throughput and visualization but not timing accuracy. The laboratory shakedown and entry-hall pilot validation were conducted by the authors, while the gym validation was performed with the help of 13 cadets from the Slovenian men's cadet volleyball team, each completing two trials. We emphasize again that the measurements were intended solely for validating the system under real-world conditions, not for assessing the athletes' abilities.

Together, these procedures verify that per-event stamping and intra-device timing behave as expected on the bench, that local clocks remain stable over the durations of interest, that the wireless sync protocol provides an explicit and enforceable quality threshold, and that the full system yields coherent total and section times with aligned kinematic signals in realistic field conditions. Quantitative outcomes referenced above are reported in Sections 4.2–4.5.

5 Discussion

The results confirm that a low-cost, modular system combining infrared gates with a body-worn IMU can achieve timing accuracy sufficient for field-based agility assessment. Device-level uncertainty is dominated by the IR receiver's processing delay and ISR latency, yielding a per-event timestamp error of 0.54 ms ± 0.14 ms (latency ± uncertainty). This translates into a total-time error below 1 ms for trials lasting 10–20 s, which is well within the requirements of standard agility protocols and clearly superior to manual stopwatch timing. It also satisfies sports measurement precision requirements, which are typically set at 0.01 s [2].

Integrating gate events with IMU signals extends beyond conventional timing by enabling interpretation of how performance is achieved. Binding IMU streams to IR events reduces segmentation ambiguity and supports extraction of kinematic markers such as braking and re-acceleration, complementing total and split times. This approach is consistent with recent studies that highlight the utility of IMUs for COD tasks, particu-

larly in the sagittal plane [4]–[9]. Sagittal-plane COD is a core component of real-world agility, so agility tests that meaningfully stress sagittal braking and re-acceleration provide more valid, sport-relevant assessments of an athlete's ability to change speed and direction under realistic conditions.

The main limitation arises from inter-node synchronization in wireless conditions. In favorable RF environments, synchronization spreads remained below 55 µs, but congestion increased jitter and required retries, leading us to conservatively report 15 ms ± 10 ms for section times across gates. It should be noted, that our system is specifically designed for sports halls, where the T-test is typically conducted and where RF conditions are favorable. This positions our approach between NTP-level accuracy and hardware-assisted PTP, while remaining deployable with of-the-shelf Wi-Fi hardware [10], [11], [13].

For practical deployment, several recommendations emerge: stable access point hardware with a wired server connection, consistent beam height and alignment, reliable and consistent body placement of the IMU, and reliance on a watch-crystal time base to bound drift. These practices improve robustness across venues and align with known sources of variability in photocell and IMU-based systems [3]–[7], [21], [22].

Limitations include the reliance on commodity Wi-Fi without hardware timestamping, which constrains synchronization in noisy environments, and the plane-specific accuracy of IMU kinematics reported in the literature [6], [7], and [9].

Beyond controlled laboratory validation, the presented system can be directly applied in sports science and coaching environments for performance assessment, return-to-play testing, and individualized training monitoring. The modular, wireless design makes it suitable for team sports agility drills, rehabilitation progress tracking, and educational use in biomechanics or embedded systems courses. Because the setup requires only a laptop, access point, and portable sensor units, it can also serve as a mobile testing kit for field conditions where commercial optical timing systems are impractical or cost-prohibitive.

In practical terms, the system offers coaches and sports scientists a portable and low-cost alternative to commercial timing systems, providing sub-millisecond accuracy and kinematic insight in everyday training environments. Its modular design and reliance on standard Wi-Fi hardware allow rapid setup and easy adaptation to different sport-specific drills, thereby bridging the gap between laboratory instrumentation and field practice.

6 Conclusions

We presented a wireless, modular measurement system that fuses infrared timing gates with a body-worn IMU for precise, field-ready agility assessment. Device-level total-time errors are below 1 ms over 10–20 s trials, meeting practical requirements for sports testing while preserving a simple, deployable workflow.

By combining gate events with IMU signals, the system provides explanatory value beyond total or split times: aligned kinematic waveforms capture braking, change-of-direction, and re-acceleration phases, supporting technique-aware feedback. For section times across gates, uncertainty is dominated by inter-node synchronization; this term is explicitly quantified to ensure transparent interpretation.

Future work will focus on (i) replacing or augmenting the AP-based synchronization with a dedicated radio channel or hybrid time-sync method to reduce inter-node error, (ii) expanding analytics toward automatic phase classification and asymmetry indices using synchronized IMU signals, and (iii) optional integration with indoor positioning technologies such as UWB for spatial trajectory analysis.

7 Acknowledgments

This work was supported in part by the Slovenian Research and Innovation Agency within the research program ICT4QoL-Information and Communications Technologies for Quality of Life (research core funding no. P2-0246).

8 Conflict of interest

The authors declare no conflict of interest. The manufacturers of the equipment referenced in this work had no role in the study design; in the collection, analyses, or interpretation of data; in the writing of the manuscript; or in the decision to publish the results.

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Arrived: 03. 10. 2025
Accepted: 20. 11. 2025

Original scientific paper
https://doi.org/10.33180/InfMIDEM2025.404

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 55, No. 4(2025), 239 – 254

Memristor based Majority Logic Adders for Error Resilient Image Processing Applications

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Abstract: Approximate Computing (AC) enables energy-efficient and high-performance computation for error-resilient applications such as data analytics, image processing, and multimedia. With the growing demand for low-power, high-density storage in Artificial Intelligence and Machine learning applications, researchers are exploring emerging technologies like FinFETs, memristors, Carbon Nano Tube FET(CNTFET), and Quantum-dot Cellular Automata (QCA) to mitigate the constraints of CMOS scaling. This paper proposes an efficient majority logic design using hybrid memristor-CMOS technology for low-power arithmetic applications. A power-efficient 1-bit adder, comprising three majority gates and one inverter, is designed and compared with existing memristor-based adders. Three Approximate Adder designs such as MAA1, MAA2, and MAA3 are implemented in 8-bit fully approximate ripple carry structure and 8-bit error-tolerant ripple carry structure, integrating four approximate and four accurate adders. Circuit performance, including power and delay, is analyzed using Cadence Virtuoso, where MAA1 achieves the lowest Power-Delay Product (PDP) in both structures. Image quality metrics, assessed using MATLAB with 8-bit pixel depth images, indicate that MAA3 attains the highest Peak Signal-to-Noise Ratio (PSNR) in the fully approximate structure. Error analysis using Verilog coding shows that the proposed MAA2 design achieves a 24.12% error rate reduction in the error-tolerant structure compared to its fully approximate counterpart, demonstrating its efficiency in balancing accuracy and power consumption.

Keywords: memristor, majority logic, approximate computing, image processing, HRTEM image

Memristorski logični večinski seštevalniki za aplikacije za obdelavo slik, odporne proti napakam

Izvleček: Približno računanje (AC) omogoča energetsko učinkovito in visoko zmogljivo računanje za aplikacije, odporne na napake, kot so analiza podatkov, obdelava slik in multimedija. Zaradi naraščajočega povpraševanja po nizkoenergijskem shranjevanju z visoko gostoto v aplikacijah umetne inteligence in strojnega učenja raziskovalci raziskujejo nastajajoče tehnologije, kot so FinFET, memristorji, FET z ogljikovimi nano cevkami (CNTFET) in kvantno-točkovni celični avtomati (QCA), da bi zmanjšali omejitve CMOS-skaliranja. Članek predlaga učinkovit večinski logični dizajn z uporabo hibridne memristor-CMOS tehnologije za nizkoenergijske aritmetične aplikacije. Oblikovan je energijsko učinkovit 1-biten seštevalnik s tremi vrati in inverterjem. Tri zasnove seštevalnikov, kot so MAA1, MAA2 in MAA3, so implementirane v 8-bitno strukturo polne propagacije prenosa in propagacije prenosa tolerantne na napako. Delovanje vezja, vključno z močjo in zakasnitvijo, je analizirano z uporabo Cadence Virtuoso, kjer MAA1 doseže najnižji produkt moči in zakasnitve (PDP) v obeh strukturah. Merila kakovosti slike, ocenjena z uporabo MATLAB-a s slikami z 8-bitno globino pikslov, kažejo, da MAA3 doseže najvišje razmerje med signalom in šumom (PSNR) v polni približni strukturi. Analiza napak z uporabo kodiranja Verilog kaže, da predlagana zasnova MAA2 doseže 24,12-odstotno zmanjšanje stopnje napak v strukturi, tolerantni do napak, v primerjavi s polno približno strukturo, kar dokazuje njeno učinkovitost pri uravnoteženju natančnosti in porabe energije.

Ključne besede: memristor, večinska logika, približno računanje, obdelava slik, HRTEM slika

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1 Introduction

The rapid evolution of Artificial Intelligence and Machine Learning applications, particularly in big data processing, has amplified the demand for high-density storage solutions, driven further by the extensive integration of the Internet of Things (IoT). Efficient han-

How to cite:
N. Natarajan et al., "Memristor based Majority Logic Adders for Error Resilient Image Processing Applications", Inf. Midem-J. Microelectron. Electron. Compon. Mater., Vol. 55, No. 4(2025), pp. 239–254

dling of these data-intensive tasks necessitates storage technologies characterized by low power consumption, high density, and fast operation speeds. AC has gained recognition as an efficient technique to reduce power and area requirements in arithmetic circuits, making it well-suited for error-resilient tasks such as data analytics, image and video processing, multimedia, and signal processing in communication systems. Unlike conventional computing paradigms that prioritize absolute accuracy, AC architectures emphasize performance and efficiency by allowing controlled imprecision in computations [1].

As conventional CMOS technology approaches its scaling limits, challenges such as leakage current, power dissipation, and reduced switching speed hinder further miniaturization and performance improvements. To address these limitations, alternative nanoelectronic devices such as FinFETs, Ferroelectric FETs (FeFETs), memristors, CNTFETs, and QCA are being explored for advanced logic applications [2]. Among these, memristors, first theorized by L. Chua in 1971 and experimentally proven by HP Labs in 2008, have shown promise in enabling high-density, energy-efficient computing [3]. The HP researchers fabricated nanoscale TiO_2 junction devices with platinum electrodes, demonstrating fast bipolar non-volatile switching. Memristors are made from organic or inorganic materials, with inorganic options such as TiO_2, Ta_2O_5, HfO_2, and ZnO offering high electrical performance, stability, energy efficiency, and CMOS compatibility. In contrast, organic materials, including polymers, graphene oxide derivatives, and biomaterials, exhibit lower performance and reproducibility [4].

Device modeling is essential for developing semiconductor devices, providing accurate insights, optimal designs, and specification compliance [5]. Various models with window functions for memristors have been developed, each optimized for specific applications, balancing accuracy, complexity, and computational efficiency. Among this, SPICE and Verilog-based models like linear ion drift and VTEAM are widely used for their simplicity in circuit-level implementation [6]. Memristive logic designs, advancing VLSI and CMOS scaling, use memristors for logic gates with resistance states representing logic '0' and '1.' IMPLY [7] and MAGIC [8] are key memristive logics, with IMPLY facing high latency and MAGIC suffering with gate connections. Memristor-based design faces challenges like signal degradation, fanout, and sneak-path currents, which hinder performance and scalability. Integrating memristors with CMOS improves logic density and mitigates degradation, particularly in AND, OR, NOR, and NAND gate implementations. Memristor Ratioed Logic (MRL) [9] integrates with CMOS inverters for low-power designs, while Hybrid NMOS-Memristor logic replaces PMOS transistors for efficient NOR logic [10]. In [11], a comprehensive survey on Memristive Threshold Logic (MTL)-based circuits is presented, which forms the foundation for our proposed work.

This research investigates the implementation of majority logic using an experimentally demonstrated memristor. Initially, an Al2O3/HfO2-based memristor device was fabricated, and its structural and electrical properties were thoroughly characterized. High-Resolution Transmission Electron Microscopy (HRTEM) analysis confirmed the correct formation of the device structure. The electrical characteristics, measured using a DC probe station, were subsequently modelled mathematically through Verilog-A coding for integration into circuit simulations within the Cadence Virtuoso environment [12]. A comprehensive description of the process flow and device modelling is provided in Section 3. Further, this paper is structured as follows: Section 2 surveys the preliminary works related to memristor based adders, along with previously implemented approximate adders using both CMOS and emerging technologies. Section 3 presents the experimental details of the proposed memristor. Section 4 details the implementation of memristor-based majority logic. Section 5 explores the design of a 1-bit adder using the majority logic and provides a comparative analysis with existing memristor-based adders. Section 6 introduces and implements majority logic-based approximate adder designs in 8-bit complete approximate and error-tolerant adder structure. Finally, Section 7 discusses the results and performance analysis.

2 Prior studies

The comprehensive review of memristor-based 1-bit adders are detailed as follows:

A 4T-1M-based XOR gate and a non-volatile full adder using an Ag/AIST/Ta memristor were modelled with a threshold memristor model in 0.35µm CMOS technology. This hybrid memristor-CMOS XOR gate achieves significant area and power reductions, offering a compact, energy-efficient solution. However, issues such as signal degradation in cascading stages and the necessity of CMOS inverters for level restoration remain bottlenecks [13]. The memristor-based MeMOS approach streamlines integration with existing CMOS processes and provides a flexible platform for computational architectures [14]. A Silver-Chalcogenide-based Memristor-CMOS design was introduced for primitive logic blocks and extended to specialized logic structures [15]. In this approach, the memristor is set to its ON state while the NMOS transistor remains open, and a

pull-up nanowire resistor controls the charging rate of the load capacitor to maintain proper voltage levels at the node.

Memristor Ratioed Logic (MRL) has been widely employed for designing universal logic gates, including AND, OR, and XOR functions [16]. However, these designs often lack detailed power and delay analysis. A combinational circuit using TiO_2 memristors replaced PMOS transistors with memristors to reduce leakage current and improve speed and energy efficiency, particularly in 180nm CMOS technology. An MRL-based full adder, consisting of XOR, AND, and OR gates along with two inverters, was simulated in 180nm CMOS technology using SPICE, demonstrating potential for reduced area and power consumption [17]. Similarly, a full adder using silver chalcogenide memristors incorporated multifunctional XOR and AND gates, achieving a delay improvement compared to conventional CMOS designs [18]. Additionally, it combines traditional MRL logic with a 1-memristor 1-NMOS (1M1N) design to address output signal amplification issues.

A transistor-free memristor-based full adder employing XOR and OR gates in MRL logic, using 14 memristors and two inverters [19], yielding a simplified design similar to prior MRL based implementations reported in [16]. Further advancements in memristor-based logic include the 1T2M design, which exploits the non-volatile nature of memristors for XOR/XNOR operations, reducing power consumption and circuit complexity while integrating one-bit full adder and comparator functionalities [20]. Additionally, a Y_2O_3-based memristor model was designed to enhance signal integrity and prevent output degradation, though it requires initialization of memristance value for proper operation [21]. A calibrated HfO_2 memristor model was assessed for variability and timing analysis in a full adder circuit [22], while yttrium oxide memristors were employed for low-power logic circuit designs where, the memristor functions as a programmable resistor controlled by an NMOS transistor for enhanced logic performance [23].

A Hybrid Memristor-CMOS (HMC) logic-based adder design, combining transmission gates, MRL-based AND/OR gates, and 1T-1M inverters, demonstrated efficiency through its simple structure and implementation in 32-bit ripple carry adders [24].A TaO_x memristor, modelled with a compact Verilog-A model, demonstrated correct functionality in a 1-bit full adder. Minor glitches from delay mismatches between MRL and CMOS components had minimal impact on performance at 1 MHz frequency [25]. In [26], a full adder implementation using a universal logic circuit improve integration density and reduce power consumption by enabling multiple logic functions within a single structure. The hybrid full adder by combining MRL based AND and OR gates with NMOS-memristor based inverter is proposed in [27].

The preliminary studies related to approximate adders are as follows:

Approximate computing (AC) is applied at various levels, but its most critical use is in circuit design, particularly for arithmetic circuits. This approach intentionally introduces errors to optimize parameters such as power, delay, energy, and area. AC aims to balance performance trade-offs, where reducing transistor count lowers power consumption but increases error rates. Thus, transistor count and error rate remain crucial considerations in circuit design. The Approximate Mirror Adder (AMA) designs are implemented by modifying conventional mirror adder for low complexity digital applications [28]. The CMOS based energy efficient and variation aware Approximate Full Adder (AFA) designs are introduced for imprecision tolerant image processing applications [29]. The Approximate Adder (AA) designs aim to integrate adders and multipliers at the fundamental level of Digital Signal Processor design [30]. Area and power efficient reversible full adders were implemented using GDI logic in [31].

Beyond CMOS-based designs, emerging technologies such as FinFET, CNTFET, QCA, memristors and spintronic devices based approximate adders have been explored. Gate Diffusion Input (GDI) logic implemented using 11nm FinFET technology based approximate adders known as FFA face challenges related to output voltage level degradation [32]. CNTFET-based approximate adders such as GMFA design suffer from non-full swing operation, leading to voltage level degradation [33]. QCA-based majority logic adders have been designed [34] and labelled as PAA, but their practical adoption is hindered by fabrication complexity, temperature sensitivity, defect tolerance, scalability issues, clocking overhead, and high-power dissipation. Spintronic full adders using Magnetic Tunnelling Junctions (MTJs) exhibit high power consumption and delay, though reconfigurable magnetic full adders have been explored to mitigate some of these drawbacks [35, 36]. Additionally, approximate adders and subtractors using memristor-based architectures have been explored, further highlighting the advantages of memristors in logic circuit implementations [37].

Among emerging technologies, memristors have gained significant prominence due to their high compatibility with CMOS transistors, enabling the development of compact and energy-efficient logic circuits.

3 Experimental section

The fabrication process for the Pt/Al_2O_3/HfO_2/Ti/TiN nanoscale device, outlining the specific materials, deposition techniques, and process parameters used to achieve its precise dimensions and well-defined structure is illustrated in Figure 1. The device was annealed at 400 °C, and the incorporation of a Ti capping layer enables forming-free switching behavior with reduced set and reset voltages. The annealing process, combined with the forming-free nature of the device, contributes to improved uniformity and reduced variability. A detailed analysis of its electrical characteristics is provided in our previous work [38]. HRTEM analysis was employed to examine the morphological and structural properties of the device, confirming the uniformity, interface quality, and thickness consistency of the deposited layers. Additionally, Energy Dispersive Spectroscopy (EDS) mapping, shown in Figure 2. provides a detailed representation of the elemental distribution within the fabricated device. The observed elemental distribution closely matches the expected outcomes based on the fabrication process flow, confirming the consistency and accuracy of the device fabrication.

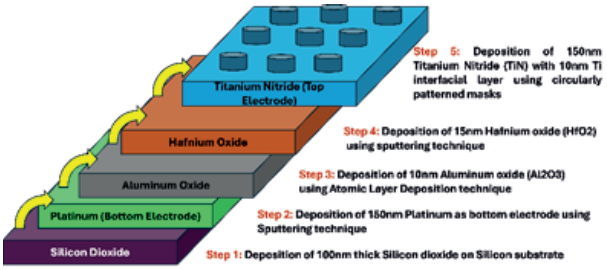

Figure 1: Fabrication process flow of proposed device

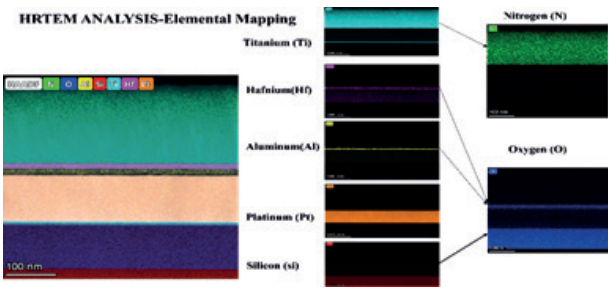

Figure 2: The nanostructure and interfacial morphologies of the proposed Al2O3/HfO2bi-layer RRAM device were investigated using HRTEM.

3.1 Experimental and modelled IV characteristics

The electrical performance of the fabricated device was rigorously characterized using a DC probe station, enabling precise measurement of key electrical parameters such as resistance states and switching voltages. The mathematical modelling is done using the model [12]. The Table 1. describes the modelling parameters implemented using Verilog-A in Cadence virtuoso environment. The comparison of experimental I-V characteristics and modelled I-V characteristics with a compliance current of 100 µA are illustrated in Figure 3. The memristor device is implemented in Cadence Virtuoso, and its compatibility with CMOS technology is validated through the design and simulation of a memristor–NMOS-based inverter [38]. In this configuration, the proposed memristor functions as a resistive pull-up element, replacing the PMOS transistor. This design maintains acceptable noise margins in the CMOS circuit, as the memristor provides an optimal resistance that results in minimal voltage drop at the output.

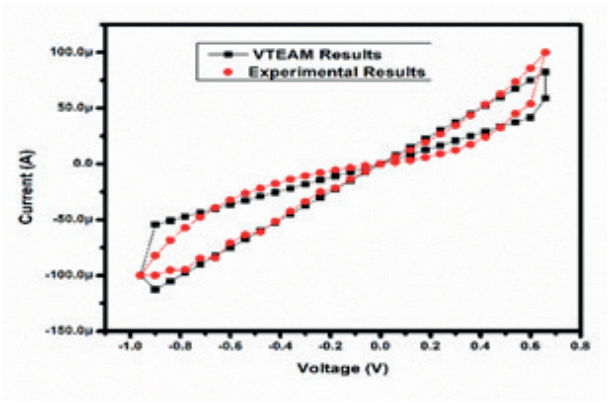

Figure 3: Comparison of Experimental and modelled I-V Characteristics

Table 1. Mathematical Model Parameters

Parameters	Pt/Al2O3/HfO2/Ti/TiN Memristor device
Roff (off-Resistance)	36729
Ron (on-Resistance)	6600
Von(on voltage)	-0.93
Voff (off Voltage)	0.66
Koff (Fitting parameter)	8e-5
Kon(Fitting parameter)	-8e-5
Alphaoff (Fitting parameter)	2.25
Alpha on (Fitting parameter)	3.2

These experimental findings provide valuable insights into the device's behaviour, serving as a foundation for performance optimization and further studies.

4 Memristor majority logic (M-ML)

Majority logic is a crucial component in the approximate computing paradigm, and is widely adopted across various emerging technologies, including QCA, ferroelectric devices, spintronic devices, and CNTFETs. In these technologies, majority logic is typically im-

plemented using capacitive or resistive elements, enhancing area and power efficiency. Majority logic is commonly utilized in the design of adders and can be extended to approximate compressors with minimal error distance. These compressors are integral components in multipliers and digital filters, which are used to develop area-efficient image processing architectures with a reduced number of transistors. This reduction in transistor count leads to lower overall power consumption and enables high-speed computing, where minor compromises in accuracy have negligible impact on image quality. However, implementing majority logic in CMOS technology is often area-inefficient due to the requirement of a greater number of transistors.

The M-ML logic circuit is implemented by combining memristors and CMOS inverters as shown in Figure 4. In this design, two inputs A and B, along with a control input, are fed into a CMOS-based inverter Via memristors. When the control input is set to either 0 or 1, the input voltages at A and B determine the resistances of M1 and M2 memristors respectively. To configure the circuit as a NAND gate, the control input is set to '0' or below the threshold voltage; in this case, the output is logic '1' for all input combinations except when A=B=1, where both memristors conduct and the output becomes logic '0'. Conversely, to operate the circuit as a NOR gate, the control input is set to 1, resulting in an output of logic '0' for all combinations except when A =B=0, where the output is logic '1'.

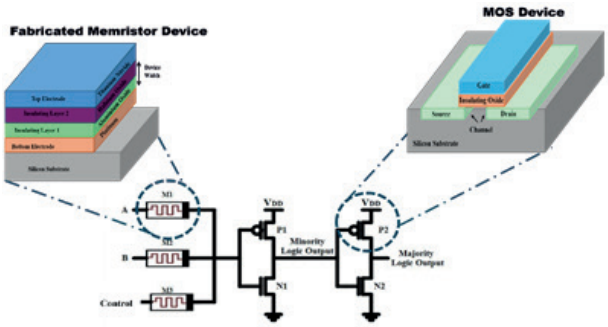

Figure 4: Majority and Minority logic circuit with device structure

Additionally, the circuit can be configured to operate as minority logic, where the least frequent input value determines the output. For instance, if A=0, B=1, and the control input is 1, the output is logic '0'. Similarly, the output is '1' for all '0' inputs and '0' for all '1' inputs. When an inverter consisting of transistors P2 and N2 is integrated into the proposed circuit, the resulting configuration implements majority logic, producing the output corresponding to the majority value of the inputs. For instance, when A=B=Control=0, the output is 0. Conversely, when A=B= Control = 1, the majority of the inputs is 1, thus the output is 1. Functionally, the circuit behaves as an AND gate when the Control input is set to 0, and as an OR gate when the Control input is set to 1 as given in Table 2.

Table2: Truth table for majority logic

Inputs			Working condition of transistors		Outputs	
Control	B	A	P1	N1	Minority Logic	Majority Logic
0	0	0	ON	OFF	1	0
0	0	1	ON	OFF	1	0
0	1	0	ON	OFF	1	0
0	1	1	OFF	ON	0	1
1	0	0	ON	OFF	1	0
1	0	1	OFF	ON	0	1
1	1	0	OFF	ON	0	1
1	1	1	OFF	ON	0	1

5 M-ML based 1-bit adder (M-MLA)

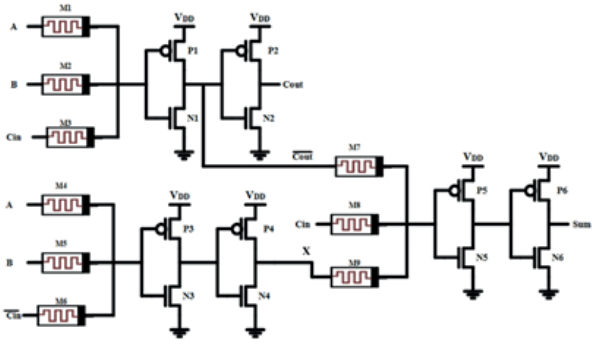

Figure 5: 1-bit Majority Logic based full adder

The proposed M-MLA circuit shown in Figure 5. is designed using majority logic. The carry circuit is constructed with transistors P1-P2, N1-N2 and M1, M2, M3 . When Cin=0, the output is A AND B; when Cin=1, the output is A OR B. The sum circuit is realized using transistors P3–P6 and N3– N6. At node X, the circuit generates the output A OR B when Cin=0 and A AND B when Cin=1. The final sum output is derived by using Cin as a control input, with X and Cout' as inputs. The Table 3 illustrates the functionality of the majority logic in generating the sum and carry output.

Table 3: Truth table for output of 1-bit M-MLA

Inputs			Intermediate Inputs			Sum output	Carry Output
Cin'	B	A	Cin	Cout'	X	Maj (Cin,Cout',X)	Maj (A,B,Cin)
1	0	0	0	1	0	0	0
1	0	1	0	1	1	1	0
1	1	0	0	1	1	1	0
1	1	1	0	0	1	0	1
0	0	0	1	1	0	1	0
0	0	1	1	0	0	0	1
0	1	0	1	0	0	0	1
0	1	1	1	0	1	1	1

The M-MLA is simulated in Cadence Virtuoso and compared with other memristor-based adders implemented in 180 nm technology, using the process parameters specified in [23]. The experimental section 3 provides detailed information on the memristor's design parameters, structural configuration, and electrical characteristics for implementing the proposed majority logic in memristor-based architectures.

Table 4 provides a comparative analysis of traditional memristor based adders with proposed majority logic adder. The logic circuits reported in [14, 17, 26] employ titanium dioxide (TiO_2)-based memristors, which exhibit set and reset voltages exceeding 1 V and require an electroforming voltage above 2 V. The design presented in [23] utilizes an yttrium oxide (Y_2O_3)-based memristor with relatively high switching voltages of > 4V. Although operated at a 1 V input level, this implementation achieves a power consumption of about 38 µW and a delay of approximately 200 ps. The work in [25] employs a tantalum oxide (TaO_x)-based memristor with a set voltage of 0.7 V, but it still requires an electroforming step. In contrast, the proposed memristor demonstrates a low set voltage of 0.66 V and forming-free operation. A comparison of various mathematical models, as discussed in Section 1, indicates that threshold-based approaches such as TEAM and VTEAM are preferred for their simplicity and ability to capture asymmetric switching behavior, resulting in minimal deviation between experimental and simulated characteristics.

The adders presented in [23] employ 1NMOS-1Memristor-based inverters, where the gate terminal of the transistor in the off state consistently experiences a high output, contingent on the high off-resistance value. MRL logic is utilized exclusively for AND and OR gate implementations and necessitates CMOS-based inverters for other logic circuit implementation [14,17,25]. By modifying MRL logic through the inclusion of a memristor with a control input, a stacked NAND/NOR output is achieved. Additionally, integrating an extra inverter facilitates majority logic implementation. Majority logic exhibits higher power consumption compared to MINI logic [39], but MINI logic is affected by output voltage level degradation. Conversely, post-CMOS majority logic offers high output driving capability and does not require additional buffers or resistors to restore output levels, as indicated in [26]. The proposed post-CMOS majority logic-based memristor adders offer the potential for extending the design towards more complex logic circuit implementations, enhancing their applicability in advanced computing architectures.

6 M-ML based approximate adder (MMA) designs

The approximate adders are increasingly being utilized for high-density image processing applications, where performance is prioritized over perfect accuracy. Three distinct types of approximate adders are proposed and numbered based on the number of inverters required

Table 4. Performance Evaluation of Proposed vs. Existing Memristor based Adders in 180nm Technology

Adder Types	Model Used	Device count	Power	Delay	References
MeMOS logic	TEAM	16T+18M	17.87uW	212.3ps	[14]
MRL Logic	Non-Linear dopant drift	24T+18M	53.08uW	62.4ps	[17]
Hybrid Memristor-NMOS only logic	Analytical	23T+14M	38uW	200ps	[23]
Transmission gate logic with 1T1M inverters and MRL based AND/OR logic	VTEAM	12T+6M	8.2uW	112.7ps	[24]
CMOS logic with MRL logic	Compact	16T+10M	0.615mW	1.78ns	[25]
MRL logic with 1T-1R inverter and CMOS inverter	Non-Linear	14T+12M+2R	121.78uW	62.55ps	[26]
M-ML Logic	VTEAM	14T+9M	4.752uW	218ps	Proposed Logic

*R-Resistors; M-Memristors; T-Transistors

such as MAA1, MAA2, MAA3 respectively shown in Figure 6(a-c). Table 5 compares the proposed approximate adders with accurate full adders and calculates the error distance (ED) by obtaining the absolute difference between exact and approximate output.

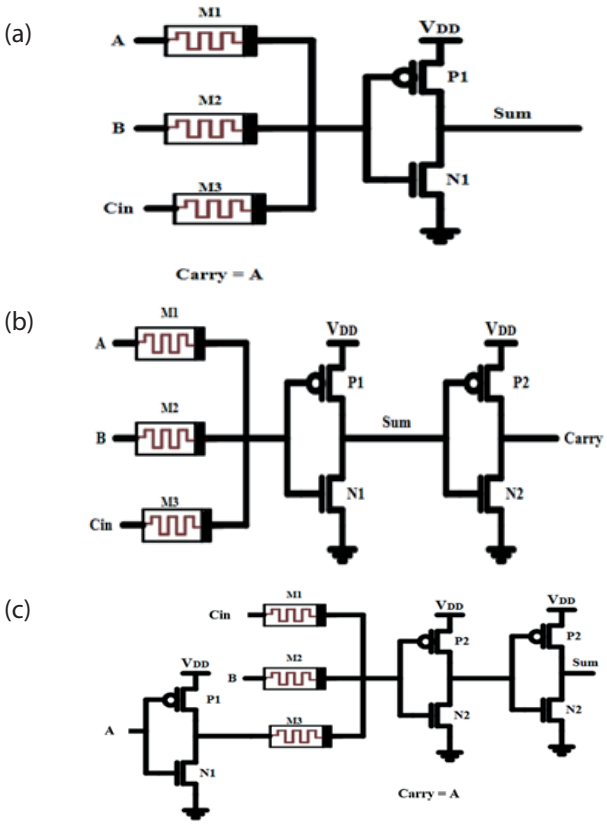

Figure 6: Proposed approximate adder designs (a) MAA1 (b) MAA2 (c) MAA3

The MAA2 is designed to introduce two errors in the sum output while maintaining an error-free carry output. The carry output, being error-free, is propagated to the next stage, effectively reducing the overall error rate in the adder. This feature makes the MAA2 particularly suitable for applications where minimizing carry propagation errors is essential, such as in arithmetic units of image processing systems. However, due to the nature of the majority logic, the MAA2 may experience a slight degradation in sum accuracy, which is compensated by its error-free carry output.

The MAA1 incorporates two errors in both the sum and carry outputs. It uses one inverter and three memristors, resulting in a smaller area footprint compared to other adder designs. This reduction in area translates directly to lower power consumption and improved speed efficiency, making the MAA1 a suitable candidate for high-performance, power-efficient image processing applications. This efficiency comes at the cost of increased image quality degradation compared to the MAA2, as the additional errors in both sum and carry outputs contribute to more significant distortion in the processed image.

The MAA3 is designed using 3 memristors and 3 inverters. It introduces two errors at the sum and carry output for same combinations of inputs.

6.1 Comparison of 1-bit approximate adders

Tables 6 and 7 present the outputs of approximate adders along with the corresponding error distance (ED) for conventional CMOS logic and emerging logic technologies, respectively.

The ED is calculated using eq. (1). The error rate (ER) quantifies the percentage of ED occurrences relative to the total possible input combinations as shown in eq. (2). The normalized mean error distance (NMED) is computed for each approximate output by dividing the ED by the total number of inputs as shown in eq. (3).

The error metrics for approximate adders are evaluated using the parameters formulated as follows:

$$ED_i = \left| Exact_{Output_i} - Approximate_{Output_i} \right| \quad (1)$$

Table 5: Truth table of Proposed Majority logic based Approximate adders

Inputs			FA			MAA1			MAA2			MAA3		
a	b	Cin	Carry	Sum	ED	Carry	Sum	ED	Carry	Sum	ED	Carry	Sum	ED
0	0	0	0	0	0	0✓	1×	1	0✓	1×	1	0✓	0✓	0
0	0	1	0	1	0	0✓	1✓	0	0✓	1✓	0	0✓	1✓	0
0	1	0	0	1	0	0✓	1✓	0	0✓	1✓	0	0✓	1✓	0
0	1	1	1	0	0	0×	0✓	2	1✓	0✓	0	0×	1×	1
1	0	0	0	1	0	1×	1✓	2	0✓	1✓	0	1×	0×	1
1	0	1	1	0	0	1✓	0✓	0	1✓	0✓	0	1✓	0✓	0
1	1	0	1	0	0	1✓	0✓	0	1✓	0✓	0	1✓	0✓	0
1	1	1	1	1	0	1✓	0×	1	1✓	0×	1	1✓	1✓	0

$$ER = \frac{Number\ of\ Erroneos\ Outputs}{n} \times 100 \quad (2)$$

$$NMED = \frac{1}{n}\sum_{i=1}^{n} \frac{\left| Exact_{Output_i} - Approximate_{Output_i} \right|}{Exact_{Output_{max}}} \quad (3)$$

Table 8 outlines the logic equations for 1-bit existing approximate adders, detailing the number of errors, Device Count (DC), ER and NMED. The memristor-based approximate adder (MFA) exhibits a high error rate of 62.5%, with five errors exceeding the 50% threshold. Adders with an error rate of ≤ 50% have been selected for the implementation of 8-bit approximate adder architectures. Furthermore, the PAA1 and PAA2 adders, originally designed in QCA technology, have been re-simulated utilizing the proposed memristor-based majority logic to ensure a fair comparative analysis.

7 Performance analysis of 8-bit approximate adders

This section investigates the effects of seventeen approximate full adders, as described in Table 8, by implementing them within 8-bit Ripple Carry Adder (RCA) structures. Two types of memristor-based approximate adder architectures have been designed: the 8-bit Memristor-based Complete Approximate Adder (MCAA), which utilizes approximate adders for all eight bits, as illustrated in Figure 7 (a), and the 8-bit Memristor-based Error-Tolerant Adder (META), which employs a hybrid approach. In the META design, the least significant 4 bits (LSBs) are implemented using approximate adders, while the most significant 4 bits (MSBs) utilize exact adders based on majority logic for PAA's and MAA's and CMOS based conventional full adder for other approximate adders, as shown in Figure 7 (b).

7.1 Circuit metrics of 8-bit approximate adders

The 1-bit adder structure were simulated at a frequency of 100 MHz, with power and delay metrics extracted for comparative analysis. The performance of the 1-bit adders were evaluated in the context of 8-bit META and 8-bit MCAA architectures. The FFA and GMFA, implemented using Gate Diffusion Input (GDI) logic, exhibit non-full-swing voltage output characteristics. Instead of achieving the expected 1V VDD output level, an output voltage of 0.702V was obtained, with some instances producing VDD/2. While this voltage level remains above the noise margin, the output driving capability

Table 6: CMOS Logic based Approximate adders

Inputs			FA	AMA1	AMA2	AMA3	AMA4	AFA1	AFA2	AFA3	AA2	AA4
a	b	Cin	CS	CS (ED)	CS (ED)	CS (ED)	CS (ED)	CS (ED)	CS (ED)	CS (ED)	CS (ED)	CS (ED)
0	0	0	00	00	01(1)	01(1)	00	01(1)	00	00	00	00
0	0	1	01	01	01	01	01	01	00(1)	00(1)	01	01
0	1	0	01	10(1)	01	10(1)	00(1)	01	01	01	01	01
0	1	1	10	10	10	10	01(1)	01(1)	11(1)	01(1)	10	01(1)
1	0	0	01	00(1)	01	01	10(1)	01	01	01	10(1)	10(1)
1	0	1	10	10	10	10	10	10	11(1)	11(1)	10	10
1	1	0	10	10	10	10	10	10	11(1)	11(1)	10	10
1	1	1	11	11	10(1)	10(1)	11	10(1)	11	11	10(1)	11

Table 7: GDI Logic and emerging logic based Approximate adders

Inputs			FFA2	FFA3	GMFA	MFA	PAA1	PAA2
A	b	Cin	CS (ED)	CS (ED)	CS (ED)	CS (ED)	CS (ED)	CS (ED)
0	0	0	00	00	01(1)	00	00	01(1)
0	0	1	01	01	00(1)	11(2)	01	00(1)
0	1	0	01	01	00(1)	00(1)	00(1)	01
0	1	1	01(1)	00(2)	10	11(1)	11(1)	10
1	0	0	00(1)	00(1)	01	00(1)	00(1)	01
1	0	1	11(1)	11(1)	10	00(2)	11(1)	10
1	1	0	10	10	10	10	10	11(1)
1	1	1	11	11	10(1)	11	11	10(1)

*ED-Error Distance, C-carry output, S-Sum output

(a)

(b)

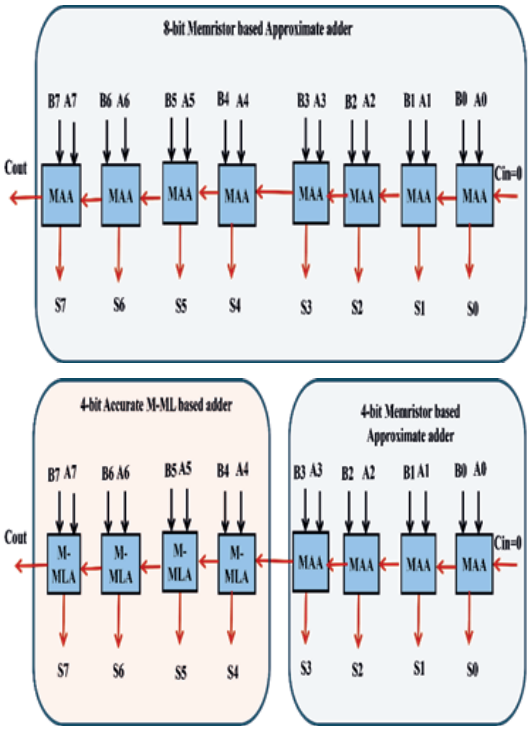

Figure 7: Block diagram of 8-Bit Memristor based (a) Complete Approximate Adder (MCAA) (b) Error Tolerant adder (META)

for ripple-based structures is significantly reduced. The comparative analysis of DC, power consumption, and delay is presented in Figure 8(a-c).

The MAA1 adder is designed with a minimal DC, utilizing only three memristors and two transistors. In contrast, the AMA1 and AA2 adders incur significant area overhead due to their reliance on 20 transistors. The AFA1 and GMFA architectures exhibit area efficiency comparable to MAA-based designs within the 8-bit MCAA configuration. However, in error-tolerant 8-bit META architectures, the DC increases. Notably, the MAA1 requires only 5 DC, achieving a reduction of 41.67% and 75% compared to AMA1 and AA2 in 8-bit META and MCAA structures, respectively. Moreover, conventional adders such as AMA and AA, as well as most AFA designs except AFA1, implemented using standard CMOS logic, require a significantly higher DC compared to emerging logic-based approximate adders, resulting in increased area and power consumption.

Power analysis reveal that MAA1 exhibit better power efficiency compared to all evaluated cases. Within the 8-bit MCAA configuration, GMFA consume less power than MAA3 and AFA1 due to its non-full-swing output

Table 8: Error Metric Analysis of Approximate adders

Approximate adder	Sum Equation	Carry Equation	Number of Errors	DC	ER (%)	NMED
AMA1 [28]	$\overline{A}.\overline{B}.Cin + ABCin$	$B + A.Cin$	2	20	25	0.083
AMA2 [28]	$\overline{Cin}.(\overline{A}+\overline{B})+(\overline{A}.\overline{B})$	$A.B + B.Cin + A.Cin$	2	16	25	0.083
AMA3 [28]	$\overline{B+(A.Cin)}$	$B+(A.Cin)$	3	13	37.5	0.125
AMA4 [28]	$Cin.(\overline{A}+B)$	A	3	15	37.5	0.125
AFA1 [29]	$\overline{A.(B+Cin)}$	$A.(B+Cin)$	3	8	37.5	0.125
AFA2 [29]	$A+B$	$Cin.(A+B)+A.B$	4	18	50	0.167
AFA3 [29]	$A+B$	$A.(B+Cin)$	4	14	50	0.167
AA2 [30]	$\overline{(BCin+\overline{B}.\overline{Cin})+A}$	$A+(B.Cin)$	2	20	25	0.083
AA4 [30]	$Cin.\overline{(A\oplus B)}+B(A\oplus B)$	A	2	14	25	0.083
FFA2 [32]	$(\overline{A}.B+Cin)$	$A.(B+\overline{B}.Cin)$	3	10	37.5	0.125
FFA3 [32]	$(\overline{A}.B\oplus Cin)$	$A.(B+\overline{B}.Cin)$	3	12	37.5	0.125
GMFA [33]	$\overline{B+Cin}$	$\overline{A}.B.Cin+A.(B+Cin)$	4	8	50	0.167
MFA [37]	$\overline{A}.\overline{B}.Cin+\overline{A}.B.\overline{Cin}+A.\overline{B}.\overline{Cin}+A.B.Cin$	$\overline{A}.B.Cin+A.\overline{B}.Cin+A.B.\overline{Cin}+A.B.Cin$	5	10M+6T	62.5	0.208
PAA1 [34]	Cin	$Maj(A,B,Cin)$	4	3M+4T	50	0.167
PAA2 [34]	$\overline{Cin}$	$Maj(A,B,Cin)$	4	3M+6T	50	0.167
MAA1	$Min(A,B,Cin)$	A	4	3M+2T	50	0.167
MAA2	$Min(A,B,Cin)$	$Maj(A,B,Cin)$	2	3M+4T	25	0.083
MAA3	$Maj(\overline{A},B,Cin)$	A	2	3M+6T	25	0.083

characteristics. The delay analysis is calculated for the longest propagation path, where the sum output exhibits the highest delay in most approximate adders. However, in architectures such as PAA, FFA, and AFA, the carry output experienced the highest delay. Among the evaluated circuits, AMA1 and AA2 demonstrate the highest worst-case delay. Additionally, GDI logic-based approximate adders exhibit increased delay compared to MAA-based designs.

The PDP analysis for the 1-bit adder, as illustrated in Figure 9(a), includes a Conventional Full Adder (CFA) implemented using CMOS transistors. The CFA exhibits a power consumption of 5.771 µW and a delay of 0.289 ns. Additionally, the power and delay characteristics of the Majority Full Adder (MFA) are presented in Table 4. The Power-Delay-Area-Product (PDAP) analysis is done by calculating

$$PDAP = PDP \times DC$$

and graphically represented in Figure 9(b). The PDP analysis, as depicted in Figure 10, is presented in decreasing order for the 8-bit MCAA and 8-bit META structures, evaluated using all approximate adders. The MAA1 show an improvement of 23.40% and 33.85% compared to MAA2 and MAA3 respectively in 8-bit META architecture. Similarly, MAA1 shows 71.37% and 79.99% improvement in PDP compared to MAA2 and MAA3 designs in 8-bit MCAA architecture. These findings provide insights into the trade-offs between area, power, and delay in various approximate adder designs, highlighting the advantages and limitations of different implementation approaches for low-power and energy-efficient arithmetic circuits.

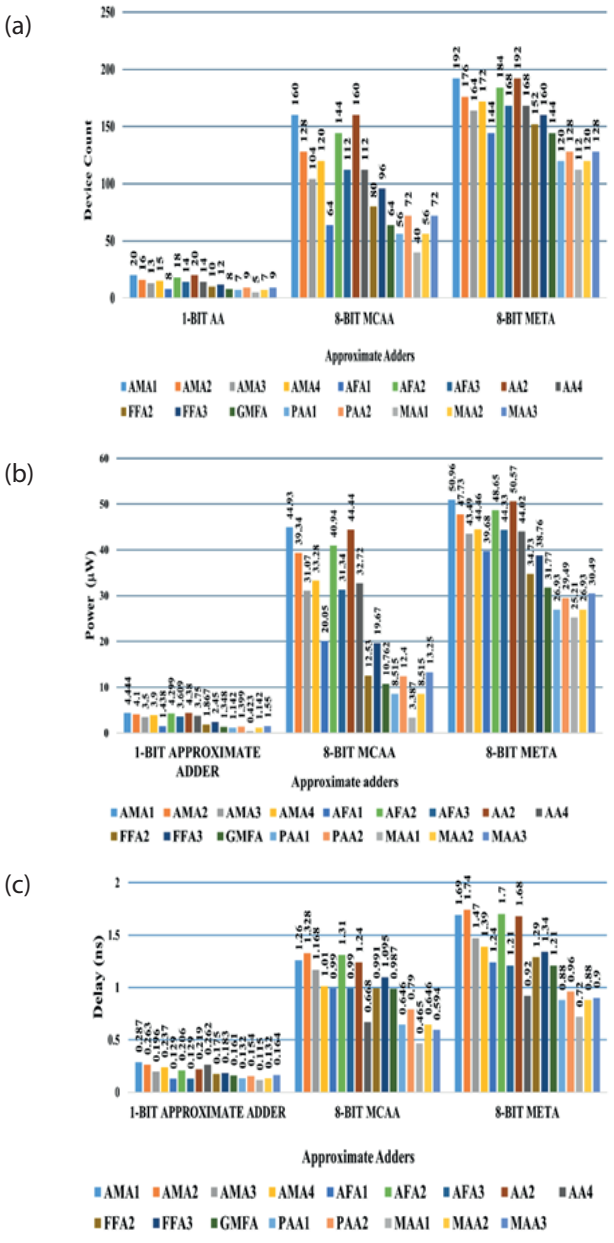

Figure 8: Comparative analysis of 1-Bit AA, 8-Bit MCAA, 8-Bit META structures in terms of (a) Device Count (b) Power (c) Delay

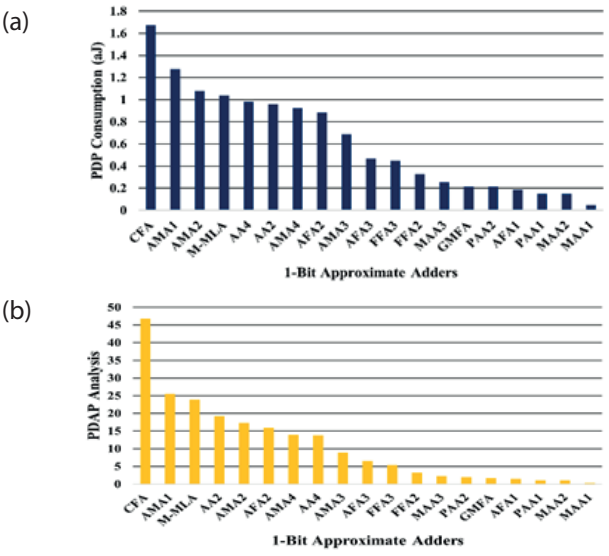

Figure 9: Comparison of 1-bit accurate and approximate adders (a) PDP analysis (b) PDAP analysis

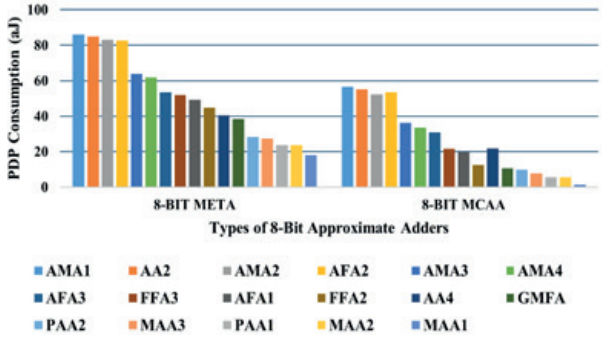

Figure 10: PDP analysis of approximate adders in 8-Bit META and MCAA structure

7.2 Error metrics of 8-bit approximate adders

The accuracy of the proposed majority-based adders is evaluated using key error metrics, including the NMED, ER, and Mean Absolute Error (MAE). These adders are compared with previously reported approximate adders by implementing in 8-bit architectures and testing them against all possible input combinations using a Verilog-based testbench. Table 9 presents the average PDAP values alongside the error metrics. The analysis indicates that for the 8-bit META adders, MAA2 and AMA2 exhibit the lowest error rates with minimal error distances. However, in terms of PDAP, MAA2 demonstrates superior efficiency, achieving an 80.54% reduction in PDAP compared to AMA2. Additionally, MAA1 in META and MCAA architectures also report lower PDAP values at the cost of reduced accuracy.

Furthermore, the error rates of PAA's and FFA2 designs are significantly higher than those of other adders. Notably, MAA2 exhibits the lowest MAE value, contributing to a reduction in NMED. In the case of the 8-bit MCAA adder, AMA1 achieves a lower error rate than MAA-based designs, albeit with an increase in PDAP. The analysis of PDP versus NMED highlights the trade-off between accuracy and circuit performance in majority-logic-based adders compared to other adder designs. The majority-logic-based adders demonstrate efficiency, as their PDP values predominantly fall within the left half of the vertical axis in both 8-Bit MCAA and 8-bit META structure as shown in Figure 11 (a) and (b) respectively.

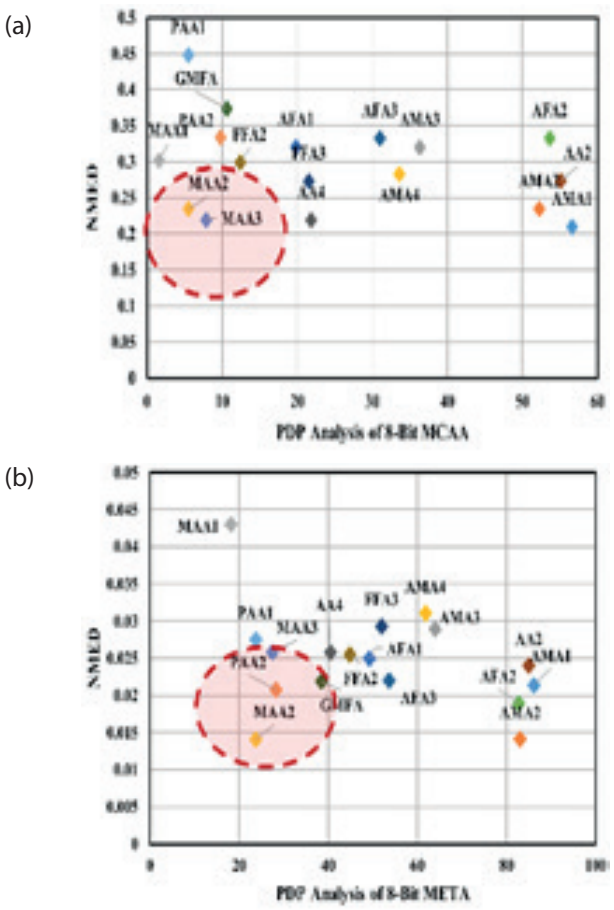

Figure 11: PDP vs NMED analysis for (a) 8-Bit MCAA (b) 8-Bit META structure

Additionally, MAA2 and MAA3 exhibit lower error rates, positioning them in the first half of the horizontal axis, along with GMFA and PAA2 in 8-Bit META structure as shown in Figure 11(b). However, GMFA produces a non-full-swing output, reinforcing the advantage of majority-logic-based adders in achieving an optimal balance of performance, accuracy, and efficiency.

7.3 Image quality metrics of 8-bit approximate adders

Three distinct sets of 512 X 512 sized input images with 8-bit pixel depth were selected from an image database [40] and processed using accurate adders. For comparison, the same images were processed using all proposed approximate adders implemented in MCAA and META based 8-bit ripple carry structures. The adders were implemented using Verilog and integrated into MATLAB via the importhdl command for image quality analysis. Image quality metrics, including PSNR and Structural Similarity Index (SSIM), are evaluated.

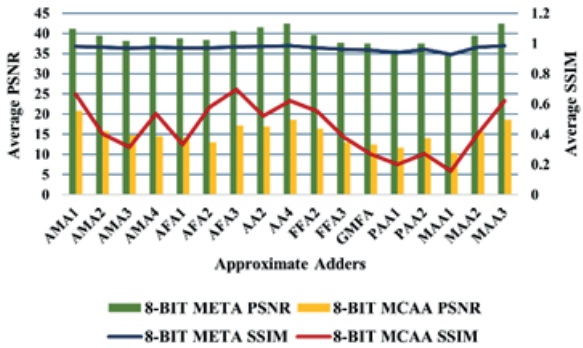

Figure 12: Comparative analysis of image quality metrics in 8-bit META and MCAA

The graphical representation of PSNR and SSIM analysis for 8-bit META and 8-bit MCAA adders is shown in Figure 12. The majority-logic-based adders demonstrate superior performance, achieving higher PSNR and SSIM values, particularly in the META structure. Among them, MAA3 exhibits the highest PSNR and SSIM values; however, it requires an additional inverter compared to MAA2.

Table 9. Comparison of error metrics with average PDAP for 8-bit approximate adders

Approximate adder	8-BIT MCAA				8-BIT META			
	Average PDAP	NMED	MAE	ER	Average PDAP	NMED	MAE	ER
AMA1	9057.888	0.2099	255	86.05	16535.5	0.02138	255	73.63
AMA2	6687.171	0.2342	255	89.98	14616.84	0.014101	15	68.27
AMA3	3774.135	0.3198	255	97.44	10484.57	0.02892	255	86.57
AMA4	4033.536	0.2827	255	97.57	10629.5	0.031062	255	86.72
AFA1	1270.368	0.3201	255	96.12	7085.261	0.02499	254	78.42
AFA2	7722.922	0.3321	255	89.81	15217.72	0.01890	15	68.22
AFA3	3474.979	0.3321	255	89.81	9011.402	0.0220	255	68.22
AA2	8816.896	0.2733	254	89.97	16311.86	0.0240	252	68.17
AA4	2447.98	0.2189	254	90.08	6803.731	0.0258	255	68.26
FFA2	993.3784	0.2988	255	96.05	6809.858	0.0255	253	78.37
FFA3	2067.71	0.2728	254	95.09	8310.144	0.0293	252	78.37
GMFA	679.814	0.3734	255	99.60	5535.605	0.0219	15	93.78
PAA1	308.0386	0.4475	255	99.58	2843.808	0.02751	15	93.76
PAA2	625.312	0.3335	255	99.60	3623.731	0.02078	15	93.74
MAA1	62.9982	0.3013	255	97.86	2032.934	0.0430	254	88.68
MAA2	308.0386	0.2342	255	89.98	2843.808	0.01410	15	68.27
MAA3	566.676	0.2189	254	90.08	3512.448	0.0258	255	68.26

7.4 Figure of merit

The circuit performance analysis and Error metrics can be jointly analysed using Figure of Merit (FOM) calculations in approximate computing [36]. The FoM is calculated using the formula:

$$FoM = \frac{Normalized\ PDAP}{1 - Average\ NMED}$$

It must be noted that the circuit performs better for lower FoM. The FoM values for the 8-bit META and 8-bit MCAA adders are presented in decreasing order, highlighting the optimal performance of the proposed majority-logic-based designs compared to existing adders. Among these, MAA1 achieves the lowest FOM due to its minimal power-delay product (PDP); however, its output image quality is inferior to that of MAA2 and MAA3. For fully approximate adders, MAA2 and MAA3 provide a better trade-off between accuracy and efficiency. Conversely, in error-tolerant applications, where only the least significant bits (LSBs) utilize approximate adders, MAA1 emerges as the most efficient choice due to its low FOM.

The post-CMOS majority-logic-based approach demonstrates greater efficiency compared to traditional CMOS logic, making it a promising alternative for arithmetic circuit design. Each of the proposed approximate adders is tailored to specific application requirements, with MAA1 proving highly efficient for error-tolerant computing by ensuring an optimal balance between power consumption and accuracy. Meanwhile, MAA2 and MAA3 are well-suited for fully approximate architectures, excelling in applications that tolerate higher error rates in exchange for reduced power consumption and delay.

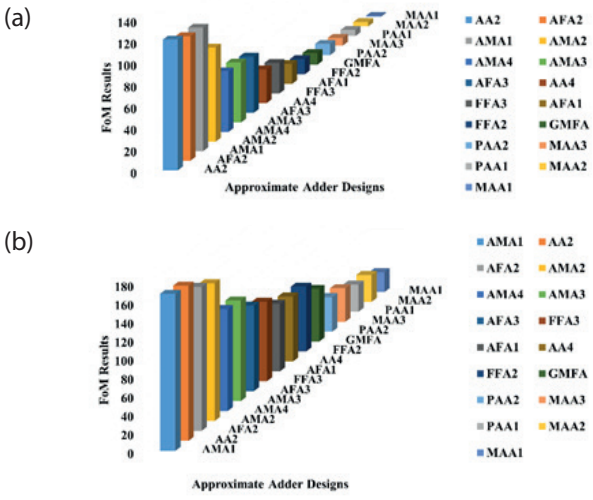

Figure 13: FoM analysis for 8-bit adders using (a) MCAA (b) META

Compared to conventional CMOS-based designs such as AMA, AFA, and AA adders, the FOM of emerging logic-based designs is significantly lower, reflecting their superior performance. Notably, the PAA2 and MAA3 designs, as well as the PAA1 and MAA2 designs, have an equal device count. However, the proposed MAA2

and MAA3 architectures achieve a lower FOM, resulting in improved performance over PAA1 and PAA2, primarily due to their lower error rates and reduced normalized mean error distance (NMED). Additionally, GDI logic, an optimized variant of conventional CMOS logic, demonstrates a relatively small FOM difference when compared to the proposed majority-based designs in the MCAA architecture, while a more significant difference is observed in the META architecture as shown in Figure 13 (a) and (b) respectively.

The proposed 8-bit approximate adder can be scaled to higher bit-width versions using a modular design, with LSBs approximated and MSBs kept accurate to limit worst-case error. In 16-bit implementations, MCAA architecture shows higher error rates compared to the META architecture. Simulations of 16-bit META architecture with 50% approximation is validated by writing Verilog testbench and results show error rates of 90% for MAA2 and MAA3, still lower than other designs reaching up to 99%, indicating better error efficiency.

Accuracy can be enhanced by reducing the approximation ratio or employing dynamic approximation techniques based on input sensitivity. However, decreasing the extent of approximation introduces area overhead due to the increased transistor count in the accurate portion of conventional designs. For instance, at a 25% approximation level, the accurate adder section using conventional design requires 60 additional transistors compared to a majority logic-based implementation in error tolerant architecture. Notably, majority logic in the META architecture proves efficient across all metrics, offering improved PDAP and linear scalability, making it ideal for larger arithmetic units. Overall, these adders provide a balanced trade-off among power, delay, and accuracy, making them effective for energy-efficient, high-performance computing.

8 Conclusion

This work presents the design and analysis of a majority-logic-based 1-bit adder using experimentally assessed and modelled memristor technology. The proposed design is evaluated against various existing memristor-based adders to assess its performance and efficiency. Additionally, three 1-bit approximate adders are developed using majority logic by integrating memristors with CMOS inverters, offering a balance between performance, power consumption, and circuit complexity. Among the designed approximate adders, MAA1 achieves the lowest Power-Delay-Area Product (PDAP) and Power-Delay Product (PDP), making it the most suitable choice for error-tolerant adder structures, where power efficiency and computational accuracy need to be balanced.

Conversely, MAA2 and MAA3, incorporating two and three inverters respectively, offer an optimal solution for fully approximate adder architectures, enabling enhanced performance in applications that can accommodate higher levels of approximation while benefiting from reduced power consumption and latency. The analysis of both META and MCAA architectures positions MAA2 as an intermediate solution, balancing the trade-offs between MAA1 and MAA3.

Comparative evaluation with conventional CMOS and Gate Diffusion Input (GDI)-based approximate adders demonstrates that majority-logic-based designs offer significant advantages in device count optimization, leading to reduced circuit complexity and improved efficiency. Extensive simulations assess key performance parameters, including power consumption, propagation delay, error metrics, and image quality metrics. These evaluations contribute to the estimation of the Figure of Merit (FoM), where majority-logic-based adders consistently outperform conventional logic-based approximate adders. By considering various design parameters, trade-offs, and application-specific requirements, the most suitable adder architecture can be selected for integration into complex logic circuits.

The results highlight the potential of emerging memristor-based majority logic for designing high-performance, energy-efficient adder architectures. Applications such as neural network accelerators, digital signal processing (DSP), and encryption circuits can leverage the power and area benefits of approximate computing. Neural networks and DSP algorithms are inherently error-tolerant, while non-critical components in encryption circuits can be approximated without compromising security. As memristor technology continues to advance, majority-logic-based designs could play a pivotal role in the development of next-generation computing systems. Broadening the application scope to these domains further underscores the practical relevance and impact of the proposed design for next-generation energy-efficient computing systems.

9 Acknowledgments

This research was partially supported by Institutional SEED grant from Kumaraguru College of Technology, Coimbatore-641049.

10 Conflict of interest

The authors declare that they have no conflict of interest.

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Arrived: 11. 04. 2025
Accepted: 09. 08. 2025

Original scientific paper
https://doi.org/10.33180/InfMIDEM2025.405

Informacije MIDEM
Journal of Microelectronics, Electronic Components and Materials
Vol. 55, No. 4(2025), 255 – 262

Enhanced Neutron-Gamma Discrimination Using Deep Neural Networks for Precision Nuclear Medicine

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Abstract: Scintillator detectors, widely used in nuclear medicine and industrial applications such as radiation monitoring and material analysis, are sensitive to both neutrons and gamma rays (n/γ). A key challenge in neutron detection is minimizing gamma-ray interference to ensure accurate measurements. Neutron-gamma discrimination is difficult because the two particle types often produce overlapping signals in scintillator detectors, with similar pulse amplitudes but subtle differences in shape and timing. Traditional methods struggle to distinguish these subtle features, leading to misclassification and reduced detection accuracy.To address this, we propose a deep neural network (DNN)-based approach combined with pulse shape discrimination (PSD) techniques to achieve high-precision particle discrimination in mixed n/γ fields. Leveraging DNN's ability to learn complex patterns, our method effectively classifies neutron and gamma-ray pulses. The trained DNN model was evaluated against traditional discrimination algorithms, including the charge comparison method, rise-time analysis, frequency-domain gradient analysis, and K-means clustering. Quantitative results demonstrate a discrimination accuracy of 99%, significantly outperforming conventional techniques. Furthermore, the proposed DNN method not only enhances discrimination reliability in mixed radiation fields but also reduces processing time compared to existing methods, making it suitable for real-time applications in medical imaging and industrial neutron detection.

Keywords: neutrons and gamma rays, deep neural network, pulse shape discrimination

Izboljšana razločevanje med nevtroni in gama žarki z uporabo globokih nevronskih mrež za natančno nuklearno medicine

Izvleček: Scinilatorji, ki se pogosto uporabljajo v nuklearni medicini in industrijskih aplikacijah, kot so nadzor sevanja in analiza materialov, so občutljivi tako na nevtrone kot na gama žarke (n/γ). Ključni izziv pri zaznavanju nevtronov je zmanjšanje motenj gama žarkov, da se zagotovijo natančne meritve. Razlikovanje med nevtroni in gama žarki je težko, ker ti dve vrsti delcev v scinilatorjih pogosto proizvajajo prekrivajoče se signale s podobnimi amplitudami impulzov, vendar z neznatnimi razlikami v obliki in časovnem poteku. Tradicionalne metode težko razlikujejo te subtilne značilnosti, kar vodi do napačne klasifikacije in zmanjšane natančnosti detekcije. Da bi to rešili, predlagamo pristop, ki temelji na globoki nevronski mreži (DNN) v kombinaciji s tehnikami razlikovanja oblike impulza (PSD), da bi dosegli visoko natančno razlikovanje delcev v mešanih n/γ poljih. Naša metoda izkorišča sposobnost DNN za učenje kompleksnih vzorcev in učinkovito razvršča nevtronske in gama impulze. Usposobljeni model DNN je bil ocenjen v primerjavi s tradicionalnimi algoritmi razlikovanja, vključno z metodo primerjave naboja, analizo časa vzpona, analizo gradienta v frekvenčnem prostoru in združevanjem K-povprečij. Kvantitativni rezultati kažejo 99-odstotno natančnost razlikovanja, kar znatno presega

How to cite:
M. Jiang et al., "Enhanced Neutron-Gamma Discrimination Using Deep Neural Networks for Precision Nuclear Medicine ", Inf. Midem-J. Microelectron. Electron. Compon. Mater., Vol. 55, No. 4(2025), pp. 255–262

zmogljivosti konvencionalnih tehnik. Poleg tega predlagana metoda DNN ne le izboljša zanesljivost razlikovanja v mešanih sevalnih poljih, ampak tudi skrajša čas obdelave v primerjavi z obstoječimi metodami, zaradi česar je primerna za uporabo v realnem času v medicinskih slikah in industrijskem zaznavanju nevtronov.

Ključne besede: neutroni in gama žarki, globoka nevronska mreža, razlikovanje oblike impulza

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1 Introduction

Neutron detection technology plays a crucial role in various applications within nuclear medicine, including material analysis for medical isotopes [1], ensuring safety in radiopharmaceutical handling [2-3], monitoring environmental radioactivity that could impact healthcare facilities [4], and supporting advanced diagnostic imaging in aerospace medicine [5]. Additionally, it is vital for the nuclear industry to ensure safe and effective medical radioisotope production [6-11]. However, the challenge arises from the omnipresence of γ-rays in the vicinity of neutron sources. Scintillator detectors, which are widely relied upon for neutron detection, are also sensitive to γ-rays [12]. This sensitivity can compromise the accuracy of neutron detection, underscoring the need to enhance detector performance through the development of effective discrimination techniques.

In 1958, Owen [13] first discovered the property of different decay times of blinking light produced by n/γ interacting with scintillator materials, then proposed a pulse shape discrimination (PSD) technique and successfully discriminated n/γ mixed signals using the PSD technique based on analogue circuits. As a result, a large number of researchers have combined digital techniques with earlier discrimination methods that required the construction of analogue circuits, while other digital-based n/γ discrimination algorithms have also been proposed. For example, Jastaniah et al. [14] implemented a rise time algorithm in 2004 based on digital techniques. In 2007, Flaska [15] achieved a charge comparison algorithm and Liu [16] et al. proposed a time-domain pulse gradient algorithm [17], which can reduce the effect of time-domain noise on the discrimination results of n/γ pulse signals. In 2018, Huang [18] applied the K-means clustering algorithm to discriminate n/γ mixed pulse signals to reduce the influence of human factors in the processing. However, these methods face inherent limitations, rise-time analysis struggles with pulse pileup and electronic noise, charge comparison fails when n/γ pulses exhibit similar charge distributions, and K-means clustering requires pre-labeled data and performs poorly with overlapping pulse features. Moreover, the above discrimination methods can only extract signal features from the time domain or frequency domain, relying on a particular signal feature to identify and classify the discriminated information, which requires a long calculation time for the n/γ discrimination results.

Artificial intelligence (AI) techniques have developed rapidly in recent years, and there has been a growing trend to use deep learning (DL) methods to analyse data. Deep learning generally refers to neural networks consisting of interconnected artificial neurons, which combine low-level features to create abstract high-level attributes. It can be used to identify distributed features in data, which plays a key role in modeling artificial intelligence. The advent of this technology offers a new perspective and an innovative approach to the rapid prediction of complex tasks. DL is not only applicable to computer science fields such as natural language processing [19] and computer vision [20] but also be applied to interdisciplinary studies such as the mechanical design of materials [21], biosensors [22], marine research [23], redox flow batteries [24], and nanogenerator performance prediction [25]. The combination of AI algorithms and PSD techniques has evolved significantly, transitioning from early feature-augmented approaches to hybrid systems that merge PSD features with neural networks, and finally to modern end-to-end deep learning models capable of raw pulse classification without manual feature extraction. The combination of AI algorithms and PSD techniques has also achieved good results in the field of n/γ signal discrimination. In 1998, the first application of AI algorithms to n/γ signal discrimination was proposed by Cao [26] et al., who used the time-of-flight method to identify particle species and verify the feasibility of the algorithm. Esposito [27] and Ronchi [28] used AI algorithms to solve the signal stacking problem well during 2004-2009, respectively. And then, Liu [29] and Zhou [30] further developed neural network algorithms in the field of n/γ pulse signal discrimination. Despite these advances, earlier AI methods still faced challenges such as limited accuracy and high computational costs, necessitating further innovation in model architecture and training efficiency.

This paper uses deep neural network (DNN) algorithms to address the problems of n/γ signal discrimination. DNNs were specifically chosen for this task due to their

exceptional capability in handling complex pattern recognition problems, which can discover subtle, nonlinear relationships in the temporal and spectral characteristics of n/γ signals that are often imperceptible to conventional analysis techniques. The test samples are compared with the charge comparison algorithm, rise time algorithm, frequency domain gradient analysis algorithm, and K-means clustering algorithm, and the DNN discrimination method can successfully discriminate n/γ mixed pulse signals. The results show that the proposed DNN discrimination method not only provides effective discrimination of the mixed radiation fields but also improves the discrimination time compared with other discrimination methods. This dual advantage of high accuracy and computational efficiency makes the DNN approach particularly suitable for real-time applications in nuclear medicine and industrial radiation monitoring, where both precision and speed are critical requirements.

2 Materials and methods

2.1 Scintillator detector principle

Neutrons cannot directly cause ionization or excitation of matter, so they cannot be detected directly [31]. However, scintillator detectors are sensitive not only to neutrons but also to γ-rays, which can be helpful for the detection of n/γ mixed pulse signals [32]. When neutrons or γ-rays are irradiated in the scintillator detector, the atoms in the astragalus crystal can be ionized and excited. Weak scintillation photons are generated when the atoms jump from the excited state back to the ground state. The photomultiplier tube converts these weak scintillations into photoelectrons after the photoelectrons enter the photomultiplier tube through the electro-optical input system. The photoelectrons are multiplied and all electrons are collected by the anode of the photomultiplier tube to form a pulse signal digital (PSD) and then enter the signal processing circuit [33]. The commonly used scintillator neutron detector consists of four parts, including scintillator material, photomultiplier tube, high voltage supply unit, and electronics. The structure of the scintillator neutron detector is shown in Fig. 1.

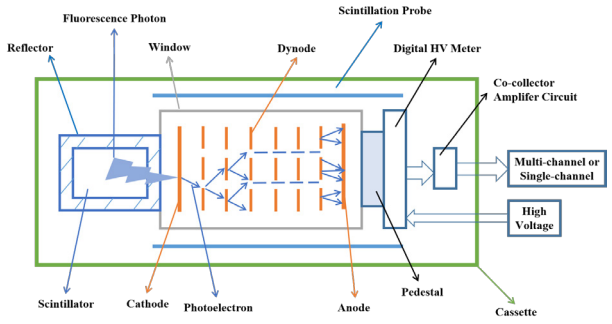

Figure 1: Working principal diagram of scintillator detector.

2.1 Data processing

We have considered the experiments in reference [34] with a neutron source of ^{252}Cf and a detector module using the plastic scintillator EJ-299-33. The power supply unit provides the operating voltage for the photomultiplier, which amplifies the scintillation light produced by the scintillator under the irradiation of the neutron source ^{252}Cf and transforms it into a pulse signal. The amplified signal is then transferred to a 12-bit 65 MS/PS digital converter, where the ADC converts the amplified analog signal into a digital signal. The digital signal is transmitted via an optical bridge to a computer for subsequent processing and analysis.

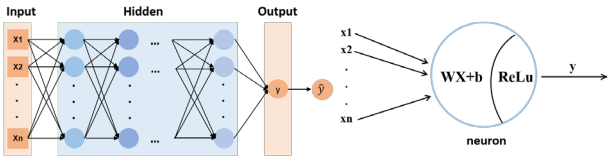

Figure 2: The workflow of the DNN modeling process.

As shown in Fig. 2, the DNN model with input, hidden, and output layers are proposed to implement neutron and γ-rays discrimination. The layers of the model are connected in a fully connected manner, with any neuron in layer ***i*** necessarily connected to any neuron in layer ***i+1*** [35]. Each local model is composed of a linear relationship and an activation function. The input x is used to provide the initial information (including PSD corresponding to neutrons and gamma rays), which is then propagated to the hidden units in each layer to produce the output categories y. The data information flows forward through the network to achieve forward propagation until a scalar cost function Cost is generated, and the back propagation is achieved when the information of the cost function flows backward through the network to calculate the gradient. All data samples are used for training and evaluation of the model, and the cross-entropy loss error $J(\boldsymbol{\theta})$ is used to evaluate the accuracy of the model with the formula.

$$\text{Cost} = \min_{\theta} J(\theta) \tag{1}$$

$$J(\theta) = -\frac{1}{N}\sum_{n=1}^{N} y_n \log \hat{y}_n + (1 - y_n)\log(1 - \hat{y}_n) \tag{2}$$

Where θ is the optimal parameters, N is the number of samples, y_n $\mathbf{y_n}$ is the DNN model output value, and $\hat{y}_n$ is the test value.

The cost function can be decomposed into the sum of the cost functions of each sample, and a small batch of samples is drawn uniformly from the training set using the stochastic gradient descent algorithm (SGD). When the training set size M grows and m remains constant, the estimate of the gradient *g* can be expressed as:

$$g = \frac{1}{\mathrm{M}} \nabla_\theta \sum_{i=1}^{m} \mathrm{Cost}(x^{(i)}, y^{(i)}, \theta) \tag{3}$$

$$\theta \leftarrow \theta - \alpha g \tag{4}$$

where $x^{(i)}$ is the ***i***-th sample, $y^{(i)}$ is the true label of the ***i***-th sample, and α is the learning rate.

The SGD enables the training of deep network models on large-scale data. For a fixed-size model, the computation of each step of stochastic gradient descent update does not depend on the size of the training set, thus effectively reducing the computational cost of the model with good fitting performance. The relevant parameter settings are as follows, the corresponding network outputs of neutron and γ-ray events are 1 and 0, the epochs are 3000, the batch size is 256, the optimizer is SGD, the learning rate is 0.000001, the momentum is 0.9, and the early stop is 200. The model environment is a Windows 10 system, 2.3 GHz Intel Core (TM) i7–11800 H GPU, 16.0 GB memory, 3050Ti graphics card, utilizing Python 3.8, Pytorch 1.9.0 + cuda 11.1.

3 Results

3.1 Discrimination results based on DNN

In this research, the data of neutron pulse signal and γ-rays pulse signal from 252Cf scintillation detectors are extracted using Python tools, and the sampled 7291 pulse signals are used to construct the data set, which is divided into an 80% training set and a 20% test set. The deep neural network algorithm model is constructed to achieve the classification process of neutron and γ-rays particle identification, as shown in Fig. 3 and Fig. 4. The training samples of 5832 pulse signals are fed into the DNN model, and the discrimination results of the training set are shown in Fig. 3. The neutron and gamma samples in the training set are well discriminated out. Fig. 4 shows the discrimination results of 1459 test samples of n/γ mixed pulse signals into the trained DNN network. Since the pulse signals in both the training and test sets are well discriminated out, the DNN model can separate the mixed n/γ well.

3.2 Comparative analysis of results

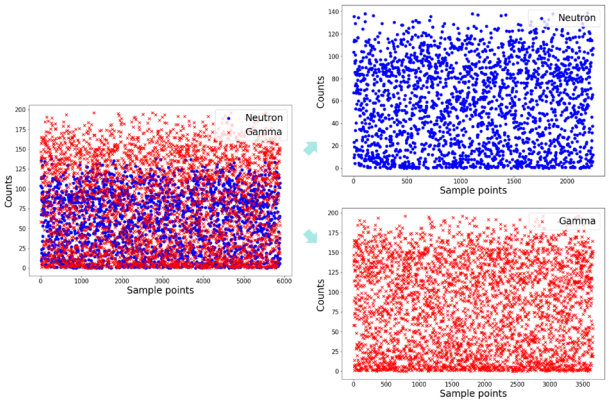

Figure 3: The discrimination results of DNN on the training set. Blue means neutrons and red means gamma rays.

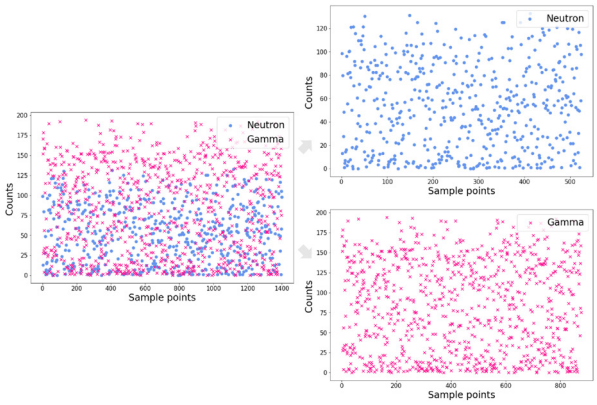

Figure 4: The discrimination results of DNN on the test set. Blue means neutron and red means gamma rays.

The discrimination results using the charge comparison algorithm (Fig. 5a), the rise time algorithm (Fig. 5b), the frequency domain gradient analysis algorithm (Fig. 5c), and the K-means clustering algorithm (Fig. 5d) are shown in Fig. 5, respectively. The five discrimination methods are used to discriminate the same 5000 sets of n/γ mixed pulse signals and the results showed that they are all successful in discriminating the n/γ mixed pulse signals, as shown in Table 1. In terms of discrimination accuracy, the discrimination accuracy rate (DAR) is improved compared to other discrimination algorithms, the DNN achieves the highest accuracy (DAR_N: 99.60%, DAR_G: 99.93%), outperforming charge comparison (99.20%, 99.86%) due to its ability to automatically learn subtle pulse-shape features. Rise-time analysis shows significantly lower neutron accuracy (89.75%, 98.19%) because of overlapping rise times in mixed radiation fields, while K-means clustering performs worst (75.77%, 95.72%) as its unsupervised approach struggles with overlapping pulse distributions. In terms of speed, the DNN is fastest (1.6s), being twice as quick

as traditional methods (3-4s) and four times faster than K-means (6.4s), thanks to GPU processing. Traditional methods like charge comparison and frequency-domain gradient analysis are slower due to per-pulse mathematical operations, while K-means suffers from iterative distance calculations. The DNN clearly provides the best balance, offering superior accuracy with significantly reduced processing time, making it ideal for real-time applications. Charge comparison remains a viable alternative where marginal accuracy loss is acceptable or DNN deployment is constrained, whereas K-means should only be considered when labeled training data is unavailable. The results demonstrate that while all methods can discriminate n/γ pulses, the DNN delivers optimal performance where both precision and speed are critical.

$$DAR_{\_N}=(1-\frac{\left|N_{Pre\_N}-N_{Mea\_N}\right|}{N_{Mea\_N}})\times 100\% \quad (5)$$

$$DAR_{\_G}=(1-\frac{\left|N_{Pre\_G}-N_{Mea\_G}\right|}{N_{Mea\_G}})\times 100\% \quad (6)$$

Where N_{Pre_N} represents the number of correctly discriminated neutron pulse signals, N_{Mea_N} represents the number of neutron pulse signals tested, N_{Pre_G} represents the number of correctly discriminated gamma pulse signals, and N_{Mea_G} represents the number of gamma pulse signals tested.

In implementing the five discrimination algorithms, it is found that each discrimination method has its advantages. The charge comparison algorithm is the simplest in principle, therefore, the easiest of all the discrimination methods to implement. Although the largest difference between the neutron and γ-ray pulse signals is only in the falling edge of the pulse, the rising time algorithm maximizes the difference between the two particle-induced signals by taking into ac-

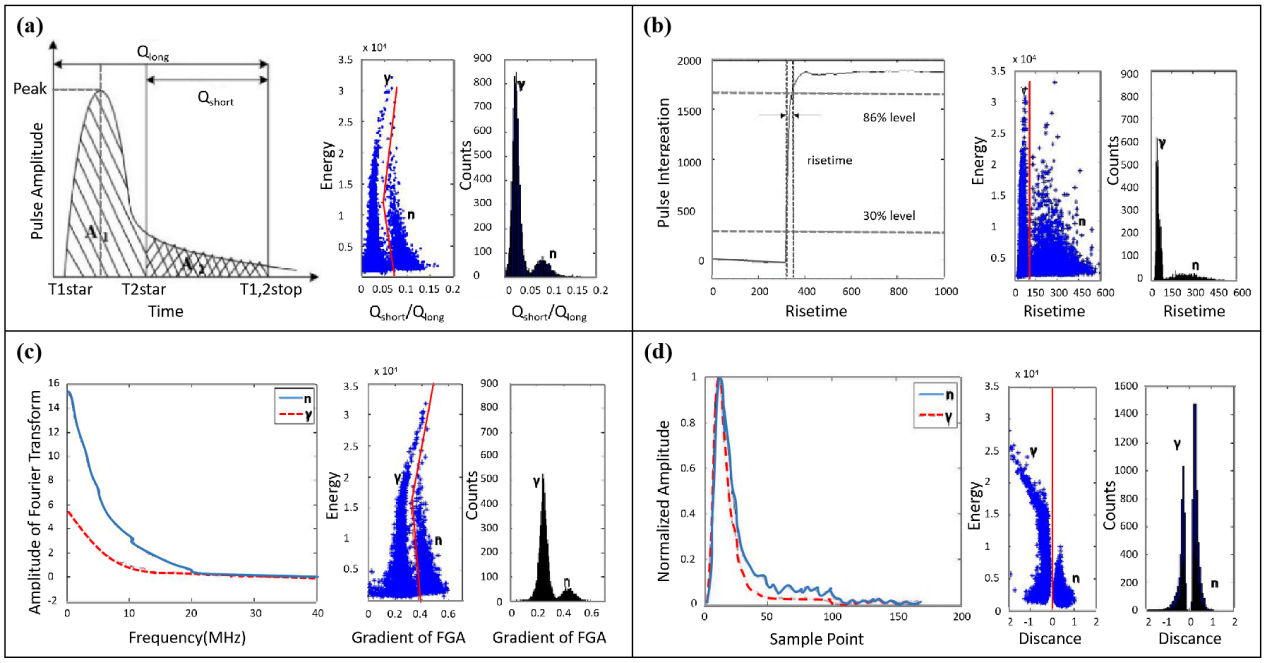

Figure 5: Four discrimination algorithms. (a) Charge comparison integration time scale diagram and charge comparison algorithm discrimination results. (b) Signal of time integration and rise time algorithm discrimination results. (c) The spectrum graph of the n/γ signal and the discrimination result of the frequency domain gradient analysis algorithm. (d) Two cluster centers are determined by K-means and the after-time integration result of the K-means clustering algorithm.

Table 1: Comparison of the results of five n/γ discrimination methods

Method	Neutron	Gamma	DAR_N	DAR_G	Time
Charge Comparison	757	4243	99.20%	99.86%	3.4s
Rise time	828	4172	89.75%	98.19%	3.5s
Frequency Gradient Analysis	742	4258	98.80%	99.79%	3.9s
K-means Clustering	933	4067	75.77%	95.72%	6.4s
DNN	748	4252	99.60%	99.93%	1.6s

count the rising and falling edges of the entire pulse signal in extracting the eigenvalues. The frequency domain gradient analysis algorithm is more resistant to interference by extracting features in the frequency domain, so it is not sensitive to changes in the shape of the pulse caused by noise. The K-means clustering algorithm does not rely on the selection of time windows to extract features in the separation of n/γ mixed pulse signals and can make direct judgments on signal categories without the need for prior parameter adjustment. However, the existing discrimination methods need to be further improved in terms of discrimination time and accuracy. The number of n/γ obtained using the five discrimination methods in this paper is relatively consistent, indicating that the discrimination process based on the DNN algorithm in this paper can successfully discriminate n/γ mixed pulse signals. This method enables the accuracy of n/γ mixed pulse signal discrimination to be improved and the computation time to be reduced.

4 Conclusions

This paper investigates the discrimination of neutrons and γ rays from scintillator detectors by combining PSD and DNN algorithms. The particle pulse signal data samples are collected from the scintillator detector and divided into training and test samples. We use the training samples to train the DNN model and realize the discrimination of the particles in the test samples. We compare the result with other discrimination methods, such as the charge comparison algorithm, the rise time algorithm, the frequency domain gradient analysis algorithm, and the K-means clustering algorithm. The five discrimination methods are applied to the same 5000 sets of n/γ mixed pulse signals. The results show that all five methods can successfully discriminate the n/γ mixed pulse signals, and the number of n/γ obtained is more consistent. In addition, the DNN method has improved the discrimination time compared with other methods, indicating that the DNN model proposed in this paper is feasible for n/γ discrimination.

5 Acknowledgments

This work was supported by the the Project of South Zhejiang Institute of Radiation Medicine and Nuclear Technology (No. ZFY-2023-K-004)，Beibei District scientific research project（2025zzcxyj-07） and the Science and Technology Research Program of Chongqing Municipal Education Commission (Grant No. KJZD-K202500202）.

6 Conflict of interest statement

The authors declare that there are no conflict of interests.

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Arrived: 11. 10. 2024
Accepted: 25. 09. 2025

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