TWO OPTICAL RING COMMUNICATION BETWEEN POWER ELECTRONIC BUILDING BLOCKS: A CASE STUDY

Žarko Čučej, Karl Benkič

Univerza v Mariboru, FERI fakulteta, Maribor, Slovenia

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Abstract: Power electronic building blocks initiated and sponsored by the Office of Naval Research, are based on the integration of power semiconductor elements with some degree of intelligence and data communication capability in compact form.

This article addresses the communication issues of power electronic building blocks. After brief overview of common used topologies in power electronic building blocks there is an analysis of requirements of communication between power electronic building block and detailed description of case of the two-optical ring communication topology with schemas for of complete implementation of slave nodes in a single FPGA circuit.

Komunikacija dvojnega optičnega obroča med gradniki močnostne elektronike: študija primera

Kjučne besede: Komunikacije, gradniki močnostne elektronike, vodenje

Izvleček: Gradniki močnostne elektronike, ki jih je vpeljala in sponzorirala ameriška vojna mornarica (Naval Research Office) temeljijo na integraciji močnostnih polprevodnikov z določeno stopnjo inteligence in sposobnostjo prenosa podatkov v kompaktni obliki.

Članek se osredotoča na komunikacijo med gradniki močnostne elektronike . Po kratkem pregledu najbolj pogosto uporabljenih topologij v gradnikih močnostne elektronike naredimo analizo komunikacijskih zahtev med gradniki močnostne elektronike. Nadaljujemo z detajlnim opisom primera topologije dvojnega optičnega obroča in podamo sheme za implementacijo enot tipa suženj v FPGA vezju.

1. Introduction

Recently the development of the electric power supply systems as well as power supply equipment are directed toward miniaturization (doable with new semiconductor materials and use higher switching frequencies) and distribution/integration of supply sources with their loads enabling optimization of their joint features or achieve other desirable features as reliability, survivability, low cost production etc.

This new design paradigm, the first time clearly exposed by of the Office of Naval Research initiation for development of power electronic building block (PEBB), anticipate that each PEBB will have standardized input/output connections, some smartness enabling safe control, state observation with power electronics hardware managing, and software determination of their function/behavior. Further, introduction of digital communication ability between PEBBs and master or distributed control system open new bunch of operabilities for new developments, research and sophisticated solutions yet not imaginable /1/, /2/, /3/, /4/, /5/.

1.1 The most common PEBB topologies

Basic switching element in PEBB is half power switching bridge usually schematically presented independently of used switch technology by symbol for switch (Fig. 1). The PEBB also can be consisted from main power half bridge switch and auxiliary half bridge for so call zero-voltage or zero-current switches.

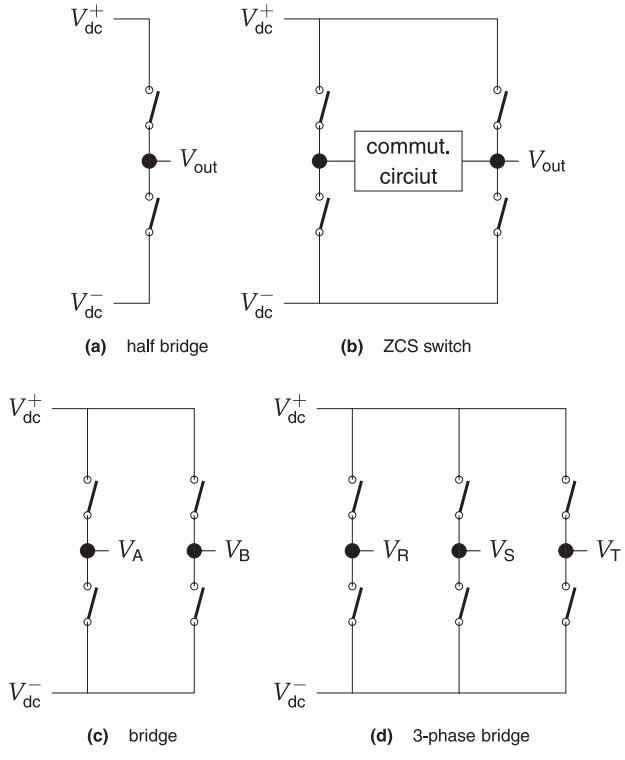

Fig. 1: The most common topologies of switches in PEBB

1.2 Universal PEBB Controller

Replacing control signals with digital communications lead to use of digital controller. This now can be universal and can be easily adapted to application with adequate algorithm software /1/, /3/, /4/.

The switching frequencies of today's medium power converters already cross a switching frequency of over 100 kHz and the recent development of fast semiconductor switches and converters' topologies shows that, in the near future medium power PEBBs will cross at a class higher switching frequency, consequently the controller as well communications connecting them to power switches should be capable to perform their tasks in 10 μs sample intervals. To copy with this it is sensible to use cascade control structure and divide task on high speed inner control loop and lower speed outer loop (Fig. 2).

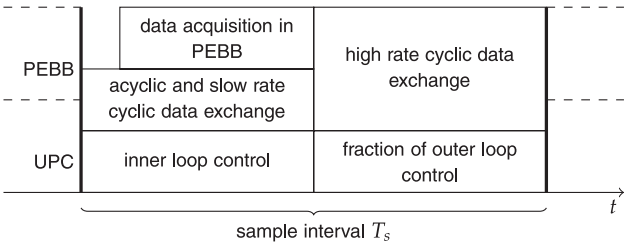

Fig. 2: Sample interval sharing between inner control algorithm, data acquisition and cyclical data communication. The outer control algorithm can be distributed over a number of cyclical data communication intervals.

Determining sample interval share for fast cyclic communication depends on the number of PEBB's linked by IPC, the kind of PEBB (for example direct controlled, PWM controlled) and a reasonable cost for communication hardware. Similarly, the duration of inner loop algorithm execution should be longer than data acquisition in PEBB.

1.3 Communication issues

The systems and equipment built-up with PEBBs, according to control and design strategy requires up to three levels of communication:

1. PEBB internal high speed serial communications connecting local Hardware Management Logic (HML) with PEBB components as analog-digital converters, timers, protection logic circuits etc,
2. fast local network linking PEBB's and central controllers, i.e. Inter-PEBB Communication (IPC), and
3. a local area network connecting equipment or systems based on PEBB to some central supervisor and monitoring system.

The major requirement for the first two communication levels is hard real-time /8/, /9/, /10/. This means that the data has to be correct in time, as well as in content. Any failure in both demands can lead to catastrophic events hazardous to devices, systems or even users. Therefore the requirements for IPC are:

1. deterministic,
2. immune to the disturbance, crosstalk, and interference as much as possible on the physical level already,
3. capable of allowing the diverse IPC traffic needed for normal PEBB functioning, support reconfiguration of PEBB, monitoring of PEBB states by boundary scan, etc,
4. capable to adopt to different control strategies of PEBB output voltage strategies (using pulse-width modulation or use of variable structure control approach with direct switch state control)
5. reliable, scalable, and survivable.

Analysis of enumerated requirements shows that the communication on one hand should be implemented in hardware and used optical fiber(s) for transmission media and on another hand to be adaptable to different control strategies and with this to be adaptable to different data formats.

2. A case study

The starting point of the case study was an existing IPC based on MACRO protocol /5/. From it the *master/slave* concept was preserved. The physical layer was enriched with the second optical ring with traffic direction opposite to the direction in the first ring (Fig. 3). Function of TAXI chips with the latter described extensions was implemented in FPGA (consequently achieved data rate on one ring due to speed limitation of used FPGA was reduced to 25 Mbit/s). New synchronizer was developed, as well as a function for topology reconfiguration. Besides this the new frame organization, forward error coding scheme, and the simplification of those protocols implemented in slave node, i.e. in a PEBB, were tested.

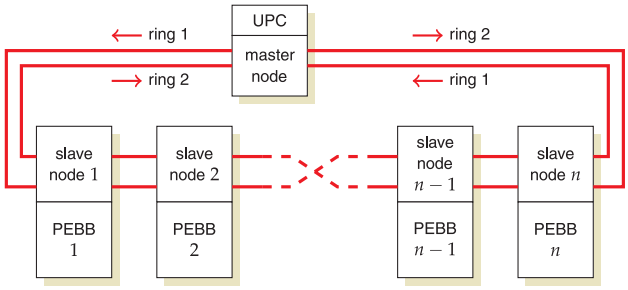

Fig. 3: IPC with two active optical ring topology.

Two optical rings topology gives opportunities as doubling the maximal number of PEBBs, or halving the sampling interval, and thus doubling the total switching frequency or halving the one ring IPC bit rate and not on the end gives very desirable reliability, scalability, and survivability. From the aforementioned possibilities, the following are consid-

ered in the case study:

- reconfiguration of two-ring topology in one sample interval,
- doubling the number of PEBBs in an IPC,
- locally performed synchronization, which is based on measurements of the frames' propagation times.

Besides the aforementioned, the structure of all frames was revised in comparison to known solutions /7/ for better utilizations of sampling intervals.

2.1 Frames

All frames have fixed length and are in the cyclic traffic send in convoys (Fig. 5). Data (i.e. information) frames (Fig. 4a), in short I-frames, contain two 16-bit long slots, which enables UPC to send two words of switch on/off occurrence data and, at the same time, to collect the same amount of fast changing measured data in PEBB. Two slots follow FEC which contain Bose-Chodhuri-Hasquenghen parity code generated by generator polynomial $x8+x2+x+1$, the same as used in ATM /6/. Parity bit gives enough redundancy for correction 1-bit error and discovering any 2-bit error and 8-bit burst error. The second slot also contains the address of PEBB, which is superimposed on the data. This additional PEBB address serves many purposes, as described later.

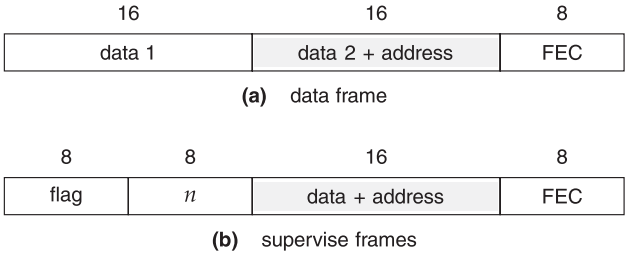

Fig. 4: Formats of frames (before 4B/5B encoding).

Supervise frames (Fig. 4b), in short S-frames, have the same size as I-frames. Instead of the first data slot they have an 8-bit long flag with repeated 4-bit code with a type of S-frame (Table I). The 8-bit field is followed by the number of I-frames.

Table I: S-frames.

from UPC to PEBB	from PEBB to UPC
Start of Convoy	Switching Error
Sample Instant Synchronization	Synchronization Mismatch
Master Reset	Broken Ring
Initialization	
Discover node	
Acknowledge	

During the cyclical data exchange, the data frames are sent in a convoys started with S-frame *Start of Convoy* as head and followed by I-frames in opposite order to PEBBs down the ring and with S-frame *Sample Instant Synchronization* as a trailer. The gap between the trailer and the end of sample interval is padded with padding bits (Fig. 5).

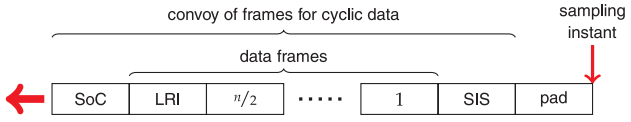

Fig. 5: Structure of convoy. SoC: S-frame Start of Convoy, LRI: low rate I-frame, SIS: Sample Instant Synchronization, pad: padding bits. The data frame numbers are equal to the position of slave nodes in the direction of the convoy propagation down the optical ring.

2.2 Transceiver circuit in the slave nodes

The core of IPC is transceiver circuit (Fig. 6). It is the same in slave and in the master nodes. Designed is FPGA and it enables wire speed detection of S-frames. Since the data frames travel in convoy with the SoC frame as header and the SIS frame as trailer, it is easy to determine those time slots in when ADM in particular PEBB's nodes copy data on the ring into the receiver shift register, and simultaneously, replace this data with their own. Slots are determined by the cyclical data frame counter and slot decoder, which is configured during the initialization phase using S-frame *Discover node*.

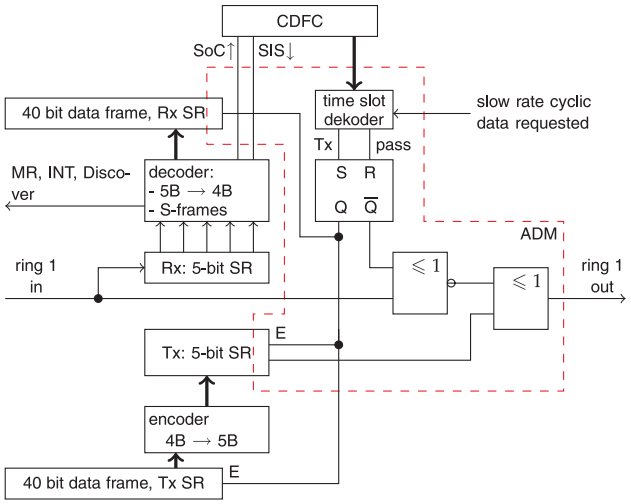

Fig. 6: Principle of innovative transceiver circuit in the first ring. CDFC: Cyclic Data Frame Counter, ADM: Add Drop-a-way Multiplexer.

2.3 Synchronization

The key problem in IPC is determining and maintaining sampling instants' synchronization in each PEBB. Synchronization is based on the measurement of time difference between SIS frame recognition instant in frame convoys which are simultaneously transmitted, each on its own ring. Since convoys propagate in opposite directions down the ring, both SIS frames pass each other close to midway. At this point the time difference between them is zero. At each other slave node this difference is twice the offset gap between the SIS frame recognition instant, and the sampling instant. This gap is padded with padding bits (Fig. 5).

Synchronization is performed by two counters, one buffer, a comparator, and two pre-scaler counters (Fig. 7). Counter 1 serves for determining the gap between the occurrence of synchronization frame detection and sampling instant, the second counter serves for measuring frame propagation time. It has a complex structure, because, for the sake of generality, it can determine half and full differences between both frames' convoys, and also supervise if a ring is broken. The measured difference is stored in a buffer since it is used for the next sampling interval. The buffer also stores data from this SIS frame, which determines ratio *VCO clock/bit rate* (×2,×4,×8,×16) and the ratio between the measured time difference of SIS frames, and the gap to sampling instant (can be 1:1 or 2:1).

Blocks "pad" and "pre-scaler" PS_2 serves for adjusting padding bits. When resetting PS_2 the first padding bit width is adjusted such that any jitter of sampling instants is minimized. The amount of jitter depends on the accuracy of the difference measurement, i.e. from ratio *VCO clock/bit rate*. If this ratio is 2:1, then the jitter is less than ± 0.*000*5 %, in the case of 16:1 it is improved to ±0.00006 %. Since only the length of the first padding bit in the sample interval can vary, this does not disturb the bit synchronization very much.

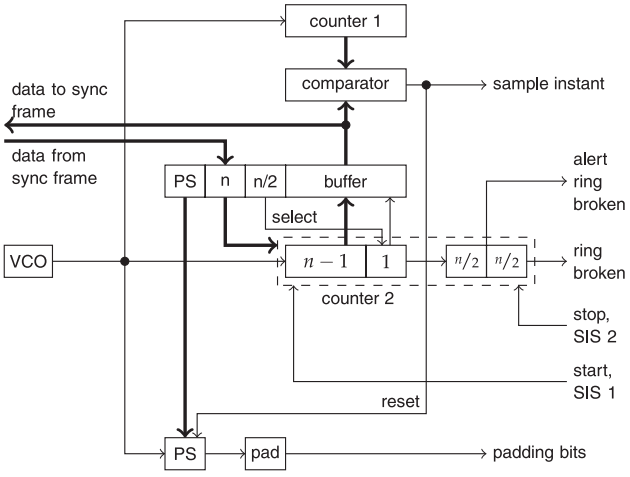

Fig. 7: Scheme of synchronizer. For meaning of label see text below.

3. Traffic

IPC traffic constitute:

- Connectionless cyclic data exchange, which in regular sample intervals deliver switching commands to the PEBB and collect data in acquired in them.
- Connectionless acyclic data with confirmation for irregular events and starting initialization.

Both traffic flows are in transmitter handled on the same way. In wire-speed the data ere exchanged between rings and PEBBs' nodes.

3.1 Acyclic traffic

Acyclic traffic is used on two occasions:

1. during the initialization phase,
2. When an irregular event in PEBB happens.

During the initialization phase, the traffic is initiated and controlled in a master/slave fashion by UPC. Among the S-frames used for initialization are *master reset*, *Initialization*, *Discover node*, *Acknowledge* and *Sample Instant Synchronization*.

When collecting irregular events, UPC, in the sample subinterval intended for acyclic traffic, successively sends empty frames *Switching Error* (SE) and *Synchronization Mismatch* (SM). These frames in the data field carry a set of 16 flags, each assigned to one PEBB. If the PEBB experiences this failure, PEBB's nodes set-up an assigned flag to it. If there are more than 16 PEBBs connected in one ring, they are segmented into groups of 16 PEBBs and the groups are assigned within the field *n*.

A broken ring is signaled by S-frame *Broken Ring* (BR) on the second ring, immediately after detecting ring breakdown. Apparently, the broken ring is detected successively in all nodes after failure (in the second ring direction) on the ring. For resolving possible collision and for detecting the place of failure, BR frames are sent successively as long as that slave nodes from the master node receive:

- ACK frame with instructions/confirmation for reconfiguration two-ring network into two one-ring networks, or
- MR frame with request to shutdown the PEBB (all switches go to the off-state)

A collision arises if the next node detects a broken ring before it detects the arrival of a BR frame from a node closer to failure. In this case the signal *alert rings broken* in nodes activate sending their BR frames, which is discontinued by detection of the incoming BR frame. With detection of an incoming BR frame, the flag *ring is broken before previous node*, is set. This flag after momentarily sending of BR frame heading prevents any further sending from this node (Fig. 8). Consequently, the master node rich least one complete BR frame header, which on its way to the master node set in the all passed slave nodes the flag *ring is broken before previous node*. This procedure clean-up the ring for the BR frame from node which is closest to the ring failure.

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Frames received without errors or with one error corrected by FEC, are acknowledged by the ACK frame in a packet of up to 16 data frames, following the initialization frame. Under normal circumstances the IPC is set-up during the design of PED/PES. For the sake of reliability at the fault

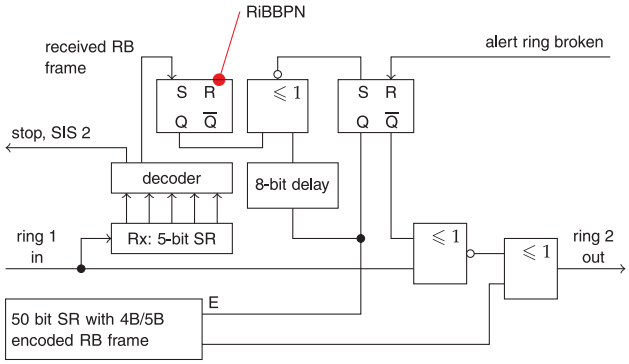

Fig. 8: Block scheme of transceiver circuit parts in the second ring involved in physical protocol "Broken Ring". RiBBPN: flag "Ring is Broken Before Previous Node", SR: Shift Register, E: enable.

tolerant design of PED/PES, the PEBB's nodes support reconfiguration, in the case of ring break as described in section 3-A, as well as the auto- configuration of IPC at the initialization of the communication system.

3.2 Initialization

Initialization has two parts:

1. initialization of PEBB
2. auto-configuration of communication system

Slave nodes executes initialization of equipment or system consist of PEBBs by delivering the received initialization data into the PEBB control registers, reading PEBBs' status registers, and supporting acknowledged connectionless services of the acyclic data transfer.

The main goal for the auto-configurations of PEBB's nodes is the determination of the nodes' serial order in the optical ring. This procedure has two steps. In the first step, the master node in the UPC sends S-frame "Discover node", which activates the automaton for setting-up the decoder for read or setting the flags in the S-frames (in accordance with a node place in the ring), in the second step the master node successively sends the logical addresses of the nodes by frame pairs 'Discover node" and I-frame. In the S-frame's data field node is assigned by its place in the ring, and in the followed data frame the data slots contain the nodes' logical addresses, determined by the master node.

4. Conclusions

IPC is very demanding at function execution times, consequently communication protocols have to be executed at so-called wire-speed at a bit rate of a least 100 Mbit/s. Therefore, all functions are simplified as much as possible and implemented by automaton, counters and registers like to physical protocols in ISO/OSI model. It can be easy implemented in FPGA.

Two-ring topology compensates for the double cost of transmission media and the necessary electro-optical couplers with high value benefits such as:

- enabling independent self synchronization in each node on IPC
- higher reliability and survivability of PED/PES

From the performed simulations in VHDL and the implemented parts of IPC, it can be concluded that, today, FPGA enables the building up of compact IPC slave nodes with integrated HML functions, in a single chip.

References

/1/ D. Borojevic: "Some Control, communications, and modeling issues for PEBB-based power distribution systems", white paper, presented as part of the *Control and Intelligent Systems Control Panel*, 1995

/2/ J. Borraccini, R. Cooley, M. Cannell, D. McLaughlin, D. Flamm, T. Duong, S. Lane, D. Borojevic: "PEBB Controller Interface". http://www.pebb.onr.navy.mil/techpapr.nsf

/3/ I. Milosavljevic: "Power electronic system communications" MSc. thesis, 1999, Virginia Tech, Blacksburg, http://scholar.lib.vt.edu/theses/available/etd-021299-141947/unrestricted/IMTHESIS.PDF

/4/ Ž. CUCEJ: Power electronic building blocks: a survey. Inf. MIDEM, 2001, letn. 31, št. 2, str. 94-101.

/5/ Ž. Cucej: "Power electronic building blocks: communication issue". Proceedings of Int. conference Elmar 2003, Zadar, 2003

/6/ W. Stalings: *Network standards*, Addison-Wesley, 1996

/7/ G. Francis, R. Burgos, F. Wang, D. Boroyevich: "A Universal Controller for Distributed Control of Power Electronics Conversion Systems, Proceedengs IEEE COMPEL 2006.

/8/ Rodd: "Communications for real-time Industrial Control: The Design Issues". Dept. of Electrical & Electronic Engineering, University College of Swansea, UK

/9/ I. Torngren, U. Backman: "Evaluation of Realtime Communication Systems for Machine Control", DAMEK mechatronic group, Dept. of Machine design, The Royal Institute of Technology, Stockholm, Sweden

/10/ D. Decotignie, P. Plaeinevaux: "A survey of industrial communication networks", Swiss Federal Institute of

Technology (EPFL), Lausanne, CH, in Ann. Telecommun., 48, no.9-10, 1993

/11/ Delta-Tau Data Systems, Inc.: Motion and Control Ring Optical, Specification. http://www.macro.org,May 1998.

/12/ Taxi chip: CY7C9689A Datasheet, Cypress, 2003. http://www.cypress.com/products/datasheet.cfm?partnum=CY7C9689A-AC

Žarko Čučej, Karl Benkič
Univerza v Mariboru, FERI fakulteta, Smetanova 17, 2000 Maribor
zarko.cucej@uni-mb.si karl.benkic@uni-mb.si

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