RF MIXERS COMPRISING ACTIVE FEEDBACK LOAD

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Key words: RF conversion mixer, active feedback, integrated circuit, RFID

Abstract: Down converting mixing circuits are essential components of every radio-frequency receiver. A state of the art down conversion mixing system is expected to operate at low supply voltage and to fulfill at least three requirements. It has to eliminate the DC and low frequency components arising from self-jammer signal either in the mixing circuitry or in the connection to next signal processing stage. It has to provide minimum setting time in case of change of DC and/or low frequency components during operation or at power-up. The mixing stage has also to provide an optimal compromise among the allowed input signal dynamic range, noise properties of the system and minimum supply voltage. To fulfill these requirements and thus design down-conversion mixing stage suitable for battery supplied digital radio systems as well as UHF RFID readers a topology of mixing system employing close loop current sink load stage was developed. The comparison to classical topology employing resistor load is given in section 2. Then special advantages of the proposed topology are highlighted with respect to improved input signal dynamic range, adaptability to different link frequencies and the possibility to employ methods to speed-up the settling of the system. The usefulness of proposed improvements for RFID readers operating on EPC Gen2 standard was proven in praxis.

RF Mešalna vezja z aktivnim zaprtozančnim bremenom

Kjučne besede: RF mešalno vezje, aktivna povratna vezava, integrirano vezje, radio – frekvenčna identifikacija

Izvleček: Mešalna vezja so bistveni sestavni del vsakega radio-frekvenčnega sprejemnika. Od sodobnega mešalnega vezja je pričakovati, da deluje pri nizki napajalni napetosti in hkrati izpolnjuje še vsaj tri dodatne zahteve. Mešalno vezje mora samo, ali pa v povezavi z naslednjo stopnjo sprejemnika izločevati DC in nizkofrekvenčne komponente, ki nastajajo kot rezultat množenja signala lokalnega oscilatorja s signalom iste frekvence. Mešalno vezje se mora tudi čim hitreje prilagajati, ko pride do spremembe teh nizkofrekvenčnih komponent, oziroma mora biti sposobno v kar najkrajšem času preiti iz staja mirovanja v stanje delovanja. Mešalno vezje mora tudi zagotoviti optimalen kompromis med dinamičnim območjem vhodnega signala, šumnimi lastnostmi mešalnega veza in napajalno napetostjo. Da bi v kar največji meri izpolnili te zahteve in tako skonstruirali mešalno vezje, primerno za uporabo v baterijsko napajanih digitalnih radijskih sistemih, kakor tudi v visokofrekvenčnih izpraševalnikih pametnih kartic, smo razvili mešalno vezje, ki uporablja aktivno zaprtozančno breme. V drugem razdelku podamo primerjavo s klasično topologijo, ki uporablja uporovno bremensko stopnjo. V nadaljevanju pa analiziramo prednosti predlagane topologije glede na izboljšano dinamično območje vhodnega signala, možnost prilagajanja na različne frekvence sprejemnega signala in na možnost uporabe metod za skrajšanje časa vzpostavitve sistema. Opisane prednosti so izkazane v praksi pri sistemih izpraševalnikov pametnih kartic, delujočih na frekvenčnem področju UHF po standardu EPC Gen2.

1. Introduction

Down conversion mixer is basically a multiplier multiplying input signal with the local oscillator signal. The results are the sum and the difference of the two frequencies providing both input signals as sine-wave shaped. Since the frequencies of the input and local oscillator signal are typically closely spaced or even identical the resulting frequency sum is a high frequency component while the resulting frequency difference is a lower frequency component. In down-converting mixers the high frequency component is eliminated using low pass which is typically an integral part of mixer load network. This is represented by the capacitor Clp in combination with load resistors Rb1 and Rb2 in fig. 1 representing the classical down conversion mixer topology using resistor load /1/. The input signal voltage is converted to a current difference by the differential transistors pair Mdp and Mdn. Four transistors (Mlpp, Mlpn, Mlnp and Mlnn) controlled by the local oscillator signal steer the differential currents in two branches. The load stage is composed of two resistors Rb1 and Rb2 where the current is converted to voltage. As mentioned the capacitor Clp eliminates the high frequency component of the frequency mixing. In case linearity is required for larger input signal amplitude the linearization resistors can be added as it is in case with Rs1 and Rs2 in fig. 1.

Another component resulting from the multiplication is a DC component. It is a result of input signal having same frequency as local oscillator signal. In radio receivers it appears as a result of leakage of local oscillator signal in the input signal, but in RFID interrogators so called self-jammer signal is a system issue and can have extremely large amplitude. The high DC component on the mixer outputs resulting from large self-jammer signal must be eliminated not to saturate subsequent receiver stages. A typical solution represented on fig. 1 is to use AC coupling to the next receiver stage.

The limitations of such topology for use in systems with high level of self-jammer are obvious. The load resistors value which is also the key element defining the voltage gain of the mixing must be kept at sufficiently low value so that even the highest value of DC component is not limiting the required dynamic of the input signal. Unfortunately we can expect highest level of DC component when the amplitude of the input signal is high also. This means that for high self-jammer levels the load resistor's value must be kept low. The available mixer gain is thus limited to smaller values what has negative impact on the noise performance of the system. The use of automatic regulation of input signal amplitude /2/ is not applicable since the signals are often AM modulated. The problem gets worse if the

system requires change in the AC coupling time constant to accommodate different signaling frequencies. As there is little freedom on the selection of load resistors value the AC coupling change must be done by changing the coupling capacitors value. For low noise systems the AC coupling capacitors are often external (not integrated) so their value cannot be changed dynamically. The problem is made worse in case of low supply voltage were the available voltage range must be divided between the input signal range and output voltage range. There are lots of low voltage solutions available for other blocks like references /3/ but low supply voltage mixers development is still a big challenge.

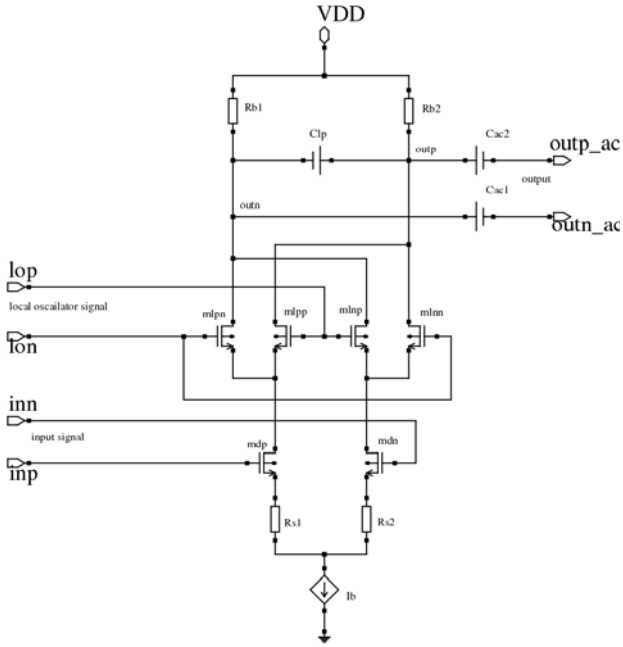

Fig. 1: Simplified schematic of typical down-conversion mixer

2. Concept of closed loop current sing load down converting mixer

As shown in previous chapter the main problem of classical resistor load stage arises from the fact that there is same signal path for DC component as wheel as the desired AC signal. Both current components are converted to voltage using same load resistor pair. The systematic solution is to separate the two current components before the desired AC signal is converted to output voltage. The basic concept of proposed solution is presented on fig. 2.

The DC current component is compensated by the two voltage controlled current sources Isi1 and Isi2. Each current source is controlled by a closed loop system which forces the average value of each output signal (outp and outn) to be equal to the output reference voltage Vro. The two current sources cannot compensate the desired AC signal since their response frequency is limited by the pole inserted between the output of error amplifier and the control input of current source. This requires pole to be set well below the minimum desired AC frequency. Being the lowest frequency pole in the loop makes this pole also the dominant pole for the loop stability. The closed loop system implementation can also be implemented using a digital algorithm employing A/D conversion for signal detection and D/A converter /4/.

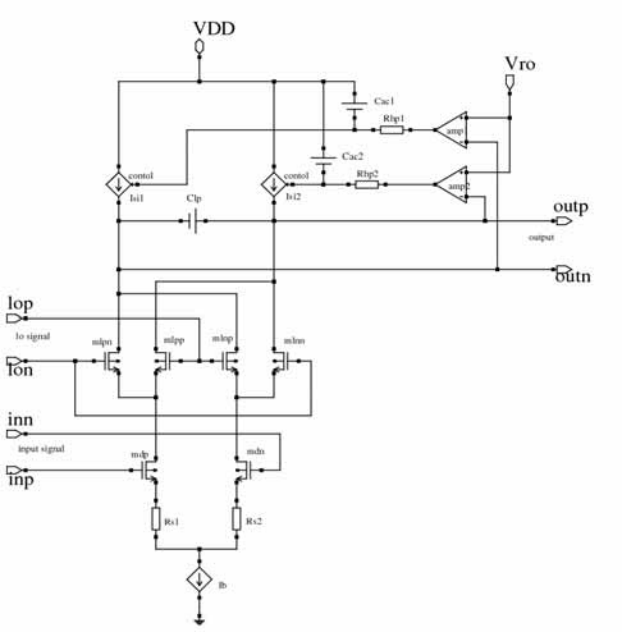

Fig. 2: Simplified schematic of mixer employing closed loop current source load.

Since DC current component is eliminated by the controlled current sources there is no need for AC coupling to the next gain stage. This is represented on figure 2 by the differential amplifier (ampsig) where the desired AC signal is converted to voltage using the differential amplifier and feedback resistors Rff1 and Rff2. The value of the two feedback resistors is now defining the gain for the AC signal which is completely independent of the DC current component. The high pass characteristic is defined by the pole in the control loop where it is relatively easy to adjust it by changing the value of resistors Rhp1 and Rhp2. The available dynamic range of input signal is significantly higher since the potential of output nodes does not change with the DC current level. Topologies with current feedback have been published before /5/ but they in general did not have separate loop for each side of the load which makes all the difference in coping with high level of DC mixing component.

3. Dynamic range of the input signal

The improvement in available dynamic range of the input signal resulting from the use of closed loop current source load stage is well illustrated in on fig. 3a and 3b. They represent the response of two mixers one having classical architecture (fig. 3a) and one having the closed loop current source load stage (fig. 3b) to same input signal. The mixing gain is identical in both cases. The input signal is AM modulated with 1MHz 200mVpp signal. The Carrier signal frequency is

200MHz and the amplitude changes from 100mVpp at the begging of simulation to 600mVpp and 1200mVpp. The input signal has same phase as local oscillator signal to highlight the problem of DC component on the mixer output.

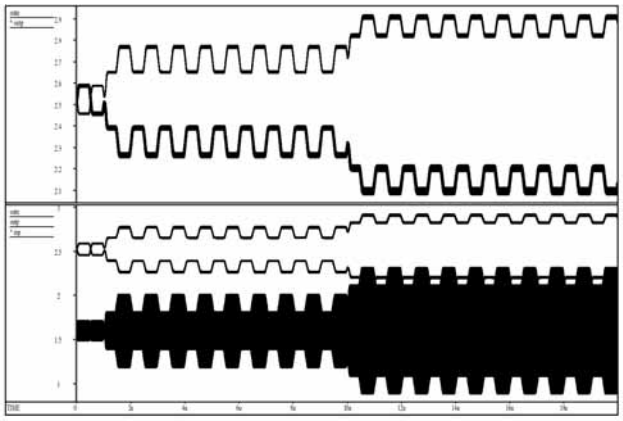

Fig. 3a: Simulation results of classical mixer architecture.

The differential output signal is displayed in canvas one. Canvas two presents the input signal together with the differential output signal to show how the available supply range (3.5V) is distributed between dynamic of the input and output signal. In case of classical mixer architecture we can see the increase of DC unbalance of the differential output signal resulting from increase in input signal amplitude. When the input signal amplitude is increased to 1200mVpp (at simulation time equal to 10us) the increased DC signal level causes the saturation of the mixer resulting in decrease of mixing gain for 3dB. This does not happen in case of mixer employing closed loop current source load (fig 3b). The closed loop system reacts to the increased DC current level by changing the current level of current sources composing the DC load stage. The control voltages for both load current sources are presented in canvas three of the figure 3b. The correction of DC current level is not instantaneous since the bandwidth of DC correction loop has to be well below the bandwidth of the desired AC signal. When the loop settles to the new DC current value, the DC component of the output voltage is eliminated thus leveling enough room for the increased input signal amplitude. The result is unchanged gain at high input signal amplitude.

The mixer gain used for both simulations was only 2. Increasing the mixing gain causes no problem in case of mixer employing closed loop current source load, while in case of classical topology it would lead to further reduction of allowed dynamic range of the input signal.

4. Adapting the AC coupling time constant to different signal frequencies

As mentioned before the settling time and high pass characteristic of the classical mixer architecture depends on

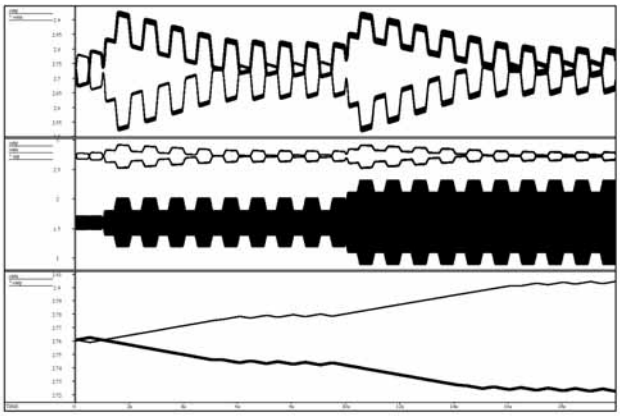

Fig. 3b. Simulation results of mixer employing closed loop current source load.

the value of AC coupling capacitors, value of load resistors in mixing load stage and the input impedance of the next stage. In case of low noise system, the AC coupling capacitors are usually external (not integrated) capacitors having relatively large values and thus cannot be changed dynamically. We already learned that there is little freedom in value of load resistors we can choose. It is also not possible to significantly change the impedance of the next gain stage mixer output is connected to without seriously impacting the noise performance. This means the classical mixer architecture enables only limited adjustments of low pass characteristic of the AC coupling.

In EPC Gen2 protocol which is becoming the dominant protocol for UHF RFID systems the tag's link frequency can vary from 40kHz to 640kHz. To accommodate this mixer topology employing closed loop current source load offers significant advantage. In this system the high pass characteristic of the mixer can be set with relative ease even if the capacitors are external and thus have fixed value. The AC time constant can be changed by varying the value of the resistors defining the pole in the feedback loop (Rlp1 and Rlp2 on figure 2). This has no effect on the gain and DC component of the mixer and has relatively small impact on the system noise. The EPC Gen2 reader system designed using the proposed mixer topology can cover all the link frequencies required by the standard and has equal spot noise performance for all link frequencies.

5. Method for reduction of load loop settling time

The same parameters defining the high pass characteristic parameters define also the required settling time the system needs to establish steady state condition after power up of transition from transmit operation to receive. In system design there is always pressure to shorten this time to minimum required. One reason is to save time and thus current in case of on/off operation mode where the system powers on and scans for the presence of the signal and powers down again if there is no signal present. The second reason is to achieve

minimum settling time between transmit and receive operation since some protocols like EPC Gen2 allow only very short setting time between transmit and reactive period.

To enable shortening of settling time the value of the resistors defining the pole in the feedback loop (Rlp1 and Rlp2 on figure 2) has to be significantly reduced during the time the speed-up is preformed. It is vital to precisely define the start and the end of the speed-up duration since high pass characteristic of the system is drastically changed during that time. Typically the speed-up is initiated when the switch from transmit to receive operation occurs on when the system is powered on. The load loop time constant is reduced for a factor of 4 to 10 as long as there is a high level of unbalance of the DC level between the differential outputs. This is detected by the window comparator observing both outputs. Since also the AC signal manifest itself as temporary unbalance of the differential outputs the comparator output is evaluated by a timing system which discriminates between the AC signal and the unbalance of the outputs to detect the time the speed-up is required. Fig. 4 presents simulation results for same input signal sequence as on fig. 3. The difference is that at the time of input signal increase at (simulation time equal 10us) the speed-up is activated. The time constant of the pole in the feedback loop is reduced for a factor of 4 resulting in faster change of the control signals of the current sources. Increased speed of correction is clearly visible on canvas three presenting the control voltages of the current sources. We can also see that the speed-up mode ends at simulation time equal 12us when the unbalance of the differential output signals is resolved. Comparison between the settling behavior with and without speed-up can be made by comparing the settling to first input signal amplitude change at simulation time equal to 2us, which is preformed without using speed-up mode, and the input signal amplitude change a simulation time equal to 10us which employs speed-up. Settling time is reduced for more than factor as shown on fig. 4.

6. Conclusions

Down conversion mixer topology employing closed loop current source load and settling speed-up system has proven to be an optimal solution for RFID systems. These systems must handle high amplitude of input signal due to self-jammer effect, typically require fast switching from transmit to receive operation and must handle a wide range of communication link frequencies.

Closed loop current source load stage eliminates input signal dynamic degradation due to DC component on the mixer output, thus maximizing the input dynamic range for a give supply voltage.

Closed loop current source load stage enables simple change of the high pass behavior of the mixer by changing the value of the resistors defining the dominant pole of the feedback loop. This can be done also in case the AC defining capacitors are external (not integrated) elements

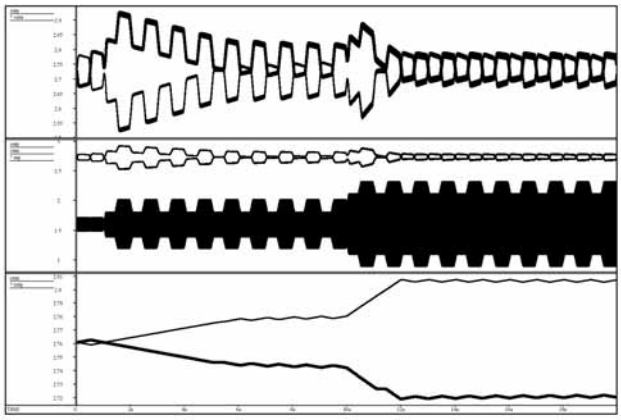

Fig. 4. Simulation results of mixer employing closed loop current source load and speed-up system

which have relatively large value to ensure low system noise. This makes the system adaptable to wide range of communication link frequencies.

Changing the value of the resistors defining the dominant pole of the feedback loop can also be used to speed-up the settling time of the receiver after power-up or transition from transmit to receive mode.

The proposed solution was used for a family of integrated RFID readers operating on UHF Gen2 standard where it has clearly demonstrated its advantages over the classical architecture.

References

/1/ J. Ledworatawee, W. Namgoong, R. Weigel, *Generalized linear periodic time-varying analysis for noise reduction in an active mixer,* IEEE Jurnal of Solid-State Circuits, vol. 42, pp 1339–1351, June 2007.

/2/ A. Pleteršek, A., Vodopivec, *Postopek za samodejno reguliranje amplitude vhodnih signalov : patent št. 22403, podeljen z odločbo z dne 5. 5. 2008 : št. prijave P-200600218, datum prijave 21. 9. 2006*. Ljubljana: Urad Republike Slovenije za intelektualno lastnino, 2008.

/3/ A. Pleteršek, A compensated bandgap voltage reference with Sub-1-V supply voltage, *Analog integr. circuits signal process.*, vol. 44, str. 5-15, 2005.

/4/ R. Benković, K. Kovačič, A. Pleteršek, Integral nonlinearity determined by selection order of current array units in DA converters, *Inf. MIDEM*, vol. 35, št. 3, pp. 140-143, sep. 2005.

/5/ K. Dufene, Z. Boos, R. Weigel, *Digital adaptive IP2 calibration scheme for CMOS down-conversion mixers,* IEEE Jurnal of Solid-State Circuits, vol. 43, pp 2434 – 2445, Nov. 2008.

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