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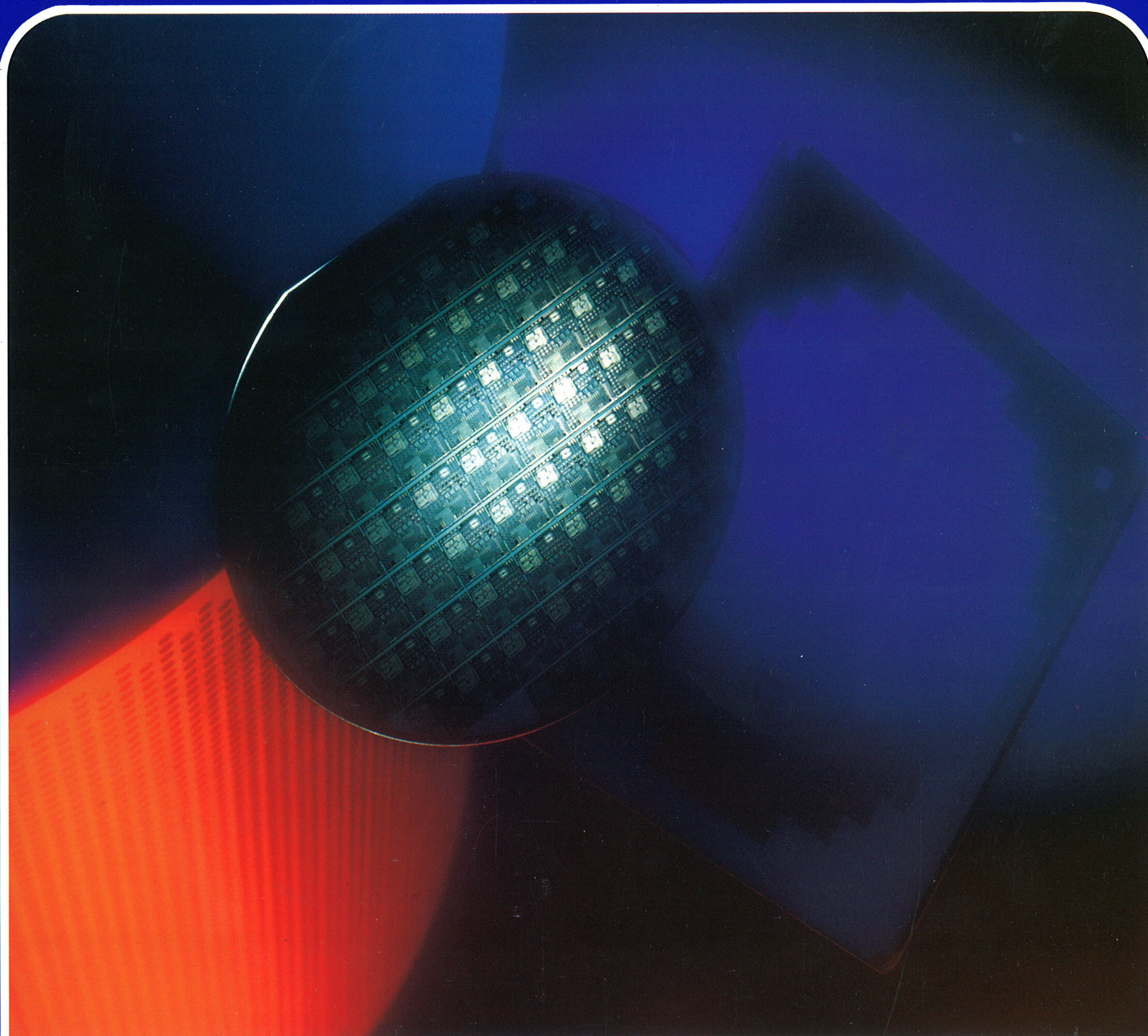

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ZNANSTVENO STROKOVNI PRISPEVKI		PROFESSIONAL SCIENTIFIC PAPERS
N. Sinnadurai: Testabilnost, pomemben dejavnik za MCM tehnologijo	**165**	N. Sinnadurai: Testability, a Vital Ingredient for MCM Technology
D. Belavič, S. Šoba, M. Hodnik, M. Pavlin, S. Gramc, M. Hrovat: Cenen senzor sile za elektronsko tehtnico	**172**	D. Belavič, S. Šoba, M. Hodnik, M. Pavlin, S. Gramc, M. Hrovat: Low Cost Force Sensor for an Electronic Scale
V. Cindro, M. Mikuž: Radiacijske poškodbe v mikropasovnih detektorjih	**177**	V. Cindro, M. Mikuž: Radiation Damage in Si Microstrip Detectors
J. Černetič: Ekološko varnejši visokotemperaturni elektrolitski kondenzator	**182**	J. Černetič: Ecologically Safer High-temperature Electrolytic Capacitor
M. Završnik, De. Đonlagić, Da. Đonlagić: Polarimetrični temperaturni senzor: analiza polarizacijskega ločitvenega razmerja in dolžine senzorskega dela	**188**	M. Završnik, De. Đonlagić, Da. Đonlagić: Polarimetric Temperature Sensor: Extinction Ratio and Sensing Lenght Examination
D. Osebik, B. Kostanjevec, B. Jarc, M. Solar, R. Babič: Izvedba nerekurzivnega digitalnega sita s programirljivim poljem logičnih vezij v strukturi porazdeljene aritmetike	**195**	D. Osebik, B. Kostanjevec, B. Jarc, M. Solar, R. Babič: The FIR Digital Filter Realization with the Field Programmable Gate Array in the Distributed Arithmetic Structure
PREDSTAVLJAMO PODJETJE Z NASLOVNICE		REPRESENT OF COMPANY FROM FRONT PAGE
AMS - Austria Mikro Systeme International	**203**	AMS - Austria Mikro Systeme International
VESTI	**204**	NEWS
KOLEDAR PRIREDITEV	**209**	CALENDAR OF EVENTS
MIDEM prijavnica	**211**	MIDEM Registration Form
Slika na naslovnici: AMS je ena od vodilnih firm v Evropi na področju načrtovanja in izdelave ASIC vezij		Front page: AMS is one of the leading European companies in design and manufacture of ASIC integrated circuits

VSEBINA **CONTENT**

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TESTABILITY, A VITAL INGREDIENT FOR MCM TECHNOLOGY

Nihal Sinnadurai
Principal Consultant, TWI, Cambridge

Keywords: microelectronics, IC, integrated circuits, complex electronics, testability, ULSI circuits, ultra large scale integration circuits, MCM, multi-chip modules, products cost, test costs, BScan, boundarx scan, BIST, built-in self-test, impacts on quality, impacts on reliability, SM, surface mounting, KGD, know good dice, CAMELOT, computer aided measure of logic testability, ATPG, automated test pattern generation, LSSD, level sensitive scan design, ATG, automatic test generation, DLBI technology, die level burn-in technology, SiBIS, silicon burn-in substrates, JTAG, joint test action group, AFM inspection system

Abstract: MCMs use bare-chip complex ICs which are wafer-probe tested and also sometimes hazardously temporarily packaged for full parametric test and burn-in depending on the specific known-good-die procedure, prior to assembly. Wafer-probe testing today can be developed hierarchically to provide parametric and diagnostic testing. The ideal solution is to achieve maximum fault coverage of every die and the assembled MCM circuit so that the total MCM technology is viable. Such a design policy must invoke IEEE P1149.1 embedded Boundary Scan or test access in all ICs and in the full MCM circuit. Thus enabling actual or virtual probing of all nodes and interconnects for circuit diagnostics and thus to know good dice and assembly. The addition of a little more internal "tester" logic provides built-in self-test (BIST), which simplifies testing during wafer probing and delivers more authentic information on "Known Good Dice". Indeed this takes wafer probing beyond the hierarchical and towards a more intelligent approach, for instance to enable selective probing of only some 30% of the connection pads of the ICs in order to exercise the whole IC and to stimulate self test and retrieve test data. A design for testability policy which is applied early in the development cycle, has maximum impact on life cycle quality and reliability and therefore is also most cost-effective than the temporary package test approach which is applied later in the production cycle.

Testabilnost, pomemben dejavnik za MCM tehnologijo

Ključne besede: mikroelektronika, IC vezja integrirana, elektronika kompleksna, preskusljivost, ULSI vezja integracije stopnje ultra visoke, MCM moduli multichip, cene proizvodov, cene preskušanja, BScan skaniranje mejno, BIST preskušanje vgrajeno vase, vplivi na kakovost, vplivi na zanesljivost, SM montaža površinska, KGD tabletke poznane dobre, CAMELOT preskusljivost logike z merjenjem računalniško podprtim, ATPG generiranje vzorcev testnih avtomatizirano, LSSD snovanje s skaniranjem nivojsko občutljivim, ATG generiranje vzorcev testnih, DLBI tehnologija za življenjski preskus na nivoju tabletke, SiBIS substrati silicijevi za življenjski preskus, JTAG skupina delovna za preskušanje spojev, AFM sistem nadzora z mikroskopijo sile atomske

Povzetek: V MCM module vgrajujemo kompleksna integrirana vezja v obliki tabletk, ki jih predhodno testiramo na nivoju rezine. Občasno jih pred vgraditvijo v MCM modul začasno montiramo v ohišja, da bi jih v popolnosti parametrično stestirali in na njih opravili ostale potrebne življenjske teste, odvisno od zahtevanega postopka za ugotovitev "zanesljivo dobre tabletke", KGD (Known Good Dice).
Testiranje na nivoju rezine lahko danes razvijemo hierarhično in tako zagotovimo parametrično in diagnostično testiranje. Idealno gledano bi s tem dosegli največjo možno stopnjo ugotovitve napak na nivoju tabletke in celotnega MCM modula. Ta pristop zahteva vgrajen IEEE P1149.1 Boundary Scan test ali dostopnost vseh vgrajenih int. vezij in MCM modula v celoti za testiranje. To omogoča dejansko in navidezno preskušanje vseh priključkov in povezav, oz. omogoča ugotavljanje dobrih tabletk in celotnega testiranega vezja.
Z dodatkom notranje "testne" logike pa omogočimo vgrajeno samotestiranje, BIST (Built-in-self-test). Le-to poenostavi testiranje na nivoju rezine in omogoči zanesljivejše ugotavljanje KGD. Na ta način presežemo preje omenjeno hierarhično testiranje z bolj inteligentnim pristopom. Tako npr. z izbirnim testiranjem samo 30% priključnih blazinic vzpodbudimo samotestiranje in omogočimo testiranje in zbiranje testnih podatkov iz celotnega int. vezja.
Politika načrtovanja za testiranje, ki jo uporabljamo zgodaj v razvojni fazi int. vezja, ima največji vpliv na njegov kvalitetni življenjski cikel in zanesljivost in je torej tudi bolj cenovno učinkovita kot občasna zapiranja v ohišja in naknadno testiranje, ki ga je potrebno izvajati kasneje v fazi proizvodnje.

1. THE NEED FOR TESTABILITY?

MCMs use bare-chip complex ICs which, if not fully tested prior to assembly in the module, will lead immediately to a poor yield of the MCM, and subsequently also pose reliability hazards because of their unknown performance and ageing characteristics. Conventional wafer-probe testing achieves rudimentary fault coverage. The consequence of inadequate testing is passed on to the assembled MCM. MCM technology is essentially a hybrid solution to semiconductor integration. Yet some test solutions are more akin to archaic board level approaches. Some intermediate solutions are very complicated and add a number of process steps and potential damage to the KGD, for instance requiring temporary bonding into carrier packages for testing and burn-in and then de-mounting and rebonding into the final packaging or interconnection location /1/. Such extra handling and processing add extra hazards and cost and do not fully represent eventual die performance. Such steps also contradict the aims of semiconductor foundries who iteratively test and improve their manufacturing practices to eliminate the need for burn-in. Therefore embedded generic solutions are required which commence at the source of the IC dice.

2. THE MAGNITUDE OF THE PROBLEM

The burden of cost borne by design for test and actual testing in production has progressively increased (Fig 1), as a consequence of increasing complexity of monolithic ULSI ICs and the recent complicated approaches to KGD and MCM testing. The expectation is that the present inexorable trend towards increased costs will be eased as more intelligent and embedded approaches to testability are adopted. The rate of rise of test cost is already slowing, because the problem of design for testability is being addressed and embedded solutions are being delivered by many, but not all, manufacturers. However, the ideal solution of fully embedded solutions is not yet available, and therefore interim solutions are necessary. As the circuits become more complex and are no-longer assemblies of simple discrete ICs, they may no longer be probed to achieve in-circuit testing and diagnostics. Even today, in advance of the expected rapid advance of MCMs early in the next millennium the problems of ULSI testability to achieve high fault coverage are quite severe and are solved either by partitioning, adding extra test pins, long test sequences or by reconfiguring the circuits to create sequentially testable paths.

	1970	1980	1990	2000
Complexity	SSI	LSI	ULSI	MCM
Gate Count	10	5k	200k	2000k
Memories	256	16k	16Mb	10Gb
Transistors	10^2	10^5	10^9	10^{14}
Speed (Hz)	100k	10M	100M	500M
Pins	14	44	356	1000
Test/Total Cost %	5%	20%	60%	60%

Fig.1. Technology and cost trends

3. EARLIER SOLUTIONS FOR TESTABILITY

ICs do not lend themselves to mechanical in-circuit testing. Nevertheless, weaknesses in design or realisation have to be diagnosed and solved. As ICs became more complex, electronic access to internal nodes became difficult, and required corporate test strategies to ensure the design incorporated one or more testability features, such as partitioning, test access connections, breaking of loops, Level Sensitive Scan Design (LSSD) /2/. LSSD is a rigorous technique whereby every register in a circuit resides on, and can be configured into, a scan path separating complex combinatorial circuits into smaller blocks for ease of testing. The registers are configured into the scan path for testing together with the use of a scan input and a scan output, enabling a stimulus (Controllability) pattern to be clocked onto the scan path and the response (Observability) shifted out. The benefits of LSSD are revealed by the dramatic improvement in automatic test generation (ATG) that can be achieved for, say, a 2000 gate IC within about 14 minutes for 99.9% fault coverage, contrasted with the laborious fault grading techniques which took over 50 hours to achieve about 60% fault coverage. Indeed today there exist commercial CAE tools which combine logic simulation and testability measures to achieve ATG. Meanwhile, the problem of in-circuit testing of high density micropackage assemblies may be probed by special fixtures /3/ with "pogo probes", or fixtureless robotic controlled probes, to gain access to small test access pads. Today probe resolution is typically as small as 6 microns and pad separation typically 100 microns. The contact pad options range from the generous use of extended test pads through to probing the leads of the micropackages (e.g. Fig 2). The presence of components on the same side as the probes adds complication to the design of the test assembly, requiring precise guide holes and the use of a physical stop to halt the travel of the probe bed. The problem is more severe with leadless packages and where designs incorporate buried vias. Therefore, an alternative philosophy for in-circuit testing of high density assemblies is needed /4/ and has been delivered.

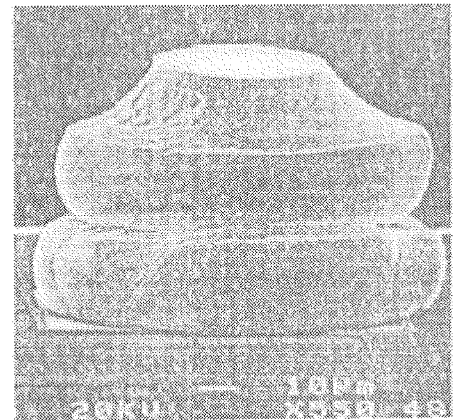

Fig. 2. Ball-on-ball wire bonding

4. EMERGING PHYSICAL ACCESS SOLUTIONS FOR KGD

4.1 Temporary connections for KGD Assessment

An useful comparison of die level burn-in (DLBI) carrier technologies was produced by Vasquez and Lindsey /5/ in which trade-offs are that permanent micropackages offer fully tested dice but take up more area on the substrate, semi-permanent attachments require either force or energy (heat) to detach the tested chip, thereby deliver a stressed contact surface into the subsequent permanent joints with the potential impairment to their reliability. An example of such temporary connection is that reported by Kim et al /1/ uses gold ball-wedge bonding onto a burn-in PCB from which the chips are

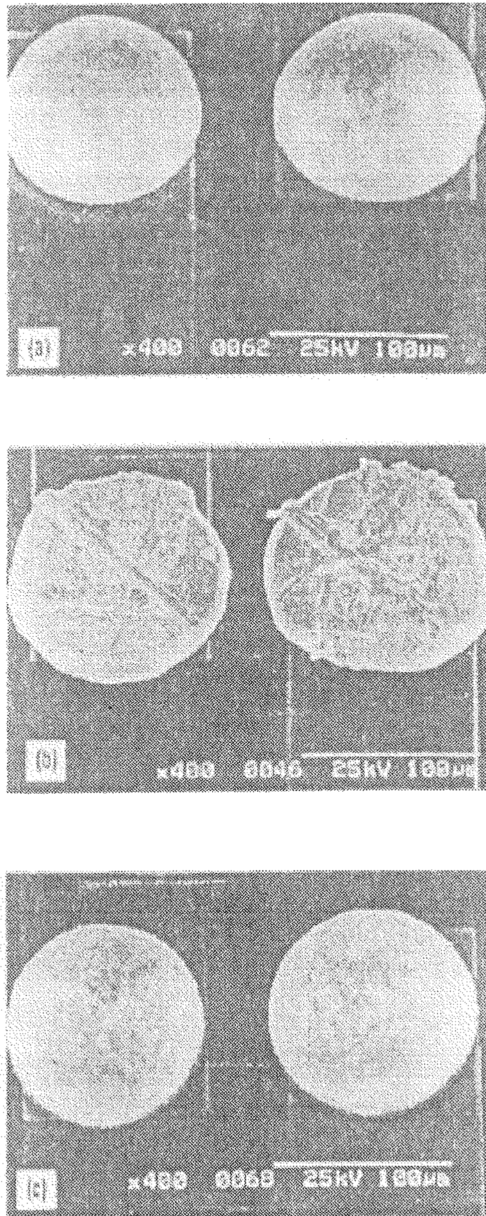

Fig. 3. Solder ball after bonding

excised after burn-in by cutting the wires above the balls, which then serve as the bonding pads for subsequent ball bonding, i.e. ball-on-ball (Figure 2). Thus the underlying ball is subjected twice to bonding stress which is a condition that accelerates ageing of the joint with the IC bond pad. An alternative promising development by nChip for their silicon burn-in substrate (SiBIS) which incorporates compliant solder bumps for wafer-probe testing. The solder bumps on a silicon probe card are softened and distorted into ohmic contact with the IC bond pads on the wafer. The solder bump shapes are re-established by reflow to achieve up to 1000 reuses. The bump distortion is illustrated in Figure 3 indicating that a corresponding force must have occurred on the wafer surface. Also, this force would progressively increase as the solder bumps become less amorphous with each reflow. Despite this critical comment, there is promise from this technology which may yet be developed into a manifold reuse technique and be translated into a production technology.

A third option is the use of temporary carriers (Figure 4) /5/, which also add the hazards of introducing stress at the IC bond pads in order to ensure good ohmic contact for measurement and burn-in. The contact is initiated by deforming the bond pad to break through the native oxide layer requiring more force per contact than the normal wirebond. Another form is piercing contacts which employed irregular sharp edged surface texture. A third form is to establish ohmic contact by scrubbing which also causes damage to the bond pad surfaces.

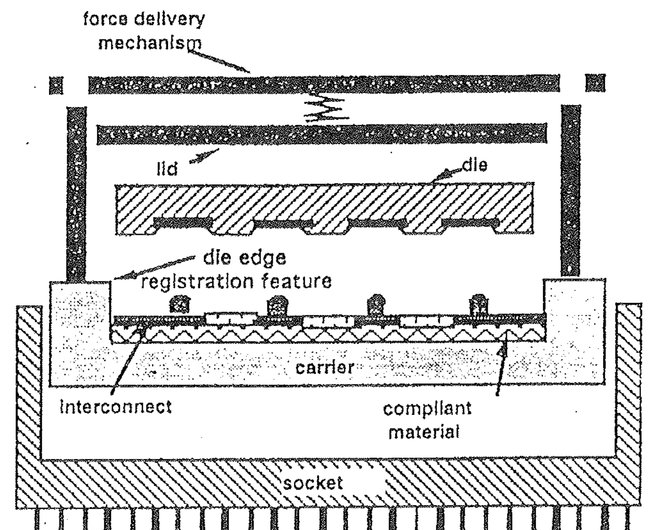

Fig. 4. Temporary die carrier

5. COMBINED PHYSICAL AND ELECTRONICS SOLUTION TO IN-CIRCUIT TESTING

The initiatives of the Joint Test Action Group (JTAG) in Europe, produced and defined the concept of "Boundary Scan", which allows "virtual probing" of internal nodes beyond the I/O buffer, which is now the IEEE Standard 1149.1 /6/. Major IC manufacturers are delivering VLSI and ULSI conforming to the testability standard. The alternative CrossCheck /7/ technique for high density logic ASICs involves embedding a test point array in the design - ensuring that each node is located at an intersection of an x-y line - thereby providing access to all nodes. CrossCheck can deal with synchronous and asynchronous logic and covers bridging and stuck-at faults and transistor defects. Despite the promise, it has not emerged as the preferred option because of the required added interconnection complexity that has to be embedded in the IC and thereafter in the system. Boundary Scan, on the other hand, can be used hierarchically and is now in widespread use. Boundary Scan which is now an established standard and already is being used to

develop a testability hierarchy up to system level. This recognises the ongoing activity on IEEE standards 1149.X for equipment design (e.g. P1149.5 for communicating maintenance messages between field replaceable units in a system).

5.1 An Integrated Approach

Modern design-to-test policies require the inclusion of appropriate test features and testing at the chip level, as the key building blocks to board level testability, and also rigorous IC and bare-board (substrate) inspection and testing to ensure the subsequent MCM testability is not compromised. Prototype testing of wafers can make use of scanning electron microscope (SEM) electron beam probing of IC chips to verify the design and diagnose faults /8/. Such DFT methods were instrumental in the 80386 programme in enabling early delivery of a fully functional device and testing of production parts quickly.

Integrated test strategies are employed by a number of IC and original equipment manufacturers of MCMs who no longer find the temporary packaging option acceptable for reasons of cost, quality and reliability. Electronics design automation (EDA) tools incorporate many of the tools to enable electronics design for testability, with some dedicated tools in place for some time, as indicated above. EDA assisted design-to-test begins at simulation to verify functionality and to develop and verify test stimuli, facilitating LSSD, built-in self-test (BIST), test ROMS, design partitioning and the addition of consequent extra pins and packaging.

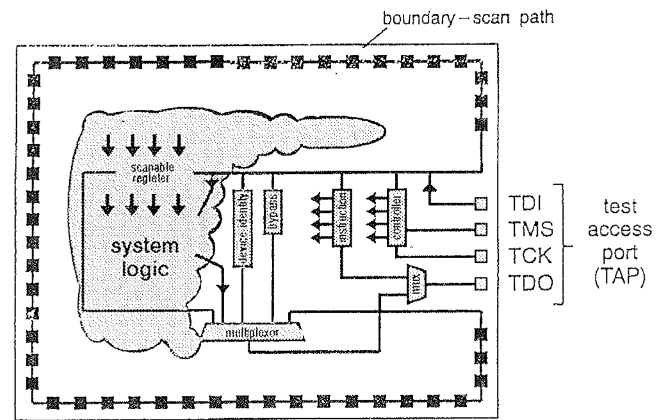

Fig. 5. Boundary scan for an IC

5.2 Boundary Scan for ICs

The incorporation of Design for Testability (DFT) of systems starts with the critical components, namely the VLSI and ULSI. Boundary Scan requires the incorporation of a 4-wire serial test bus comprising 'Test Data In' (TDI), 'Test Data Out' (TDO), 'Test Mode Select' (TMS), and 'Test Clock' (TCK), and a boundary scan register (Fig 5) /9/. The additional test circuitry consumes about 10% of the chip area. The technique takes full advantage of Scan Path design, described earlier, which today is no longer an interesting option, but an essential solution to the need to deliver tested

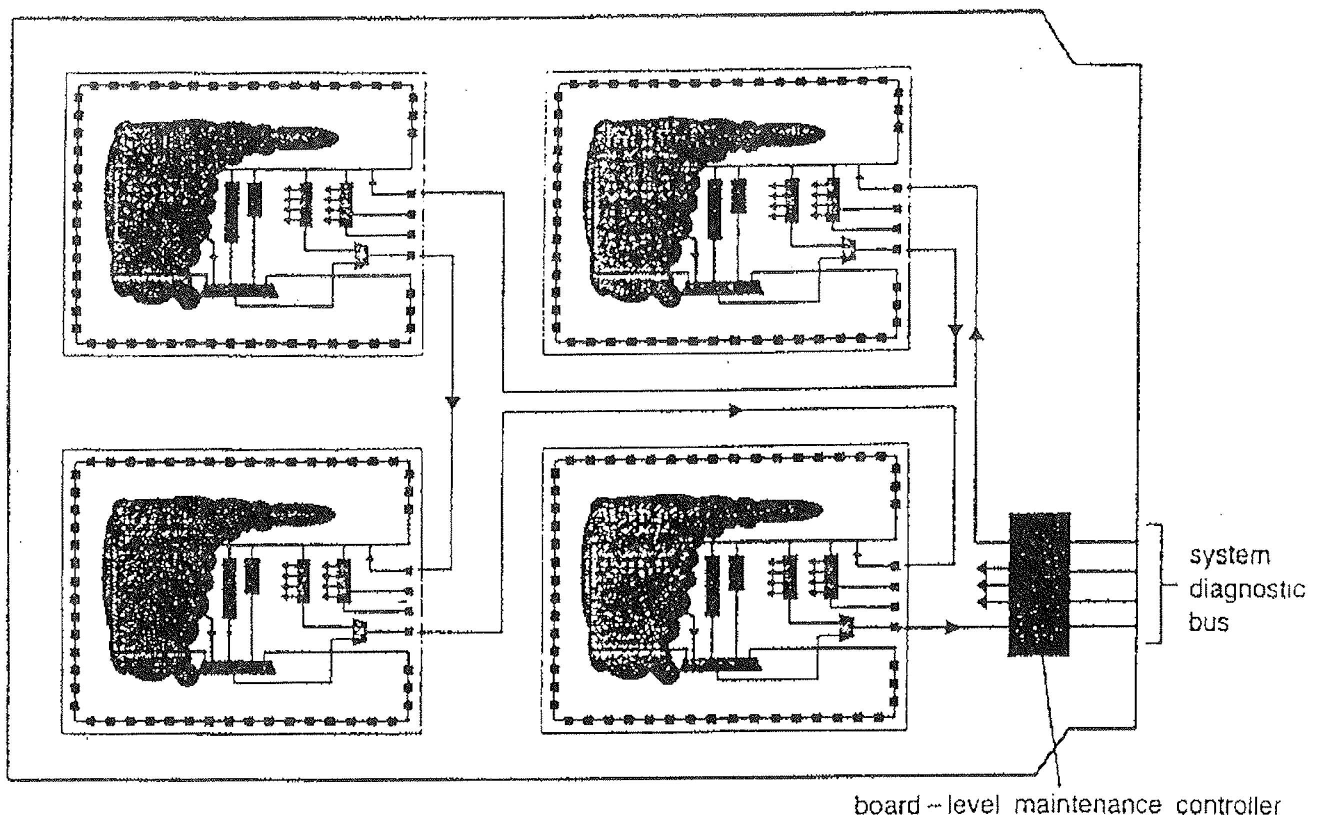

Fig. 6. Boundary scan extended to circuit boards and MCMs

and testable chips - it is the key to reducing overall product cost through significant increases in quality and reductions in production costs. The IC test functions are controlled by a Test Access Port (TAP) controller which is a state machine communicating over the test bus. TDI and TMS are kept at logic-high unless otherwise driven. TDO is normally high impedance, and can acquire one of 3 states according to the data shifted through the IC. TMS initiates the state of the TAP, which selects the test mode. TCK clocks data into the IC through TDI and out through TDO. Either test instructions or test data can be scanned through the IC.

The addition of a little more internal "tester" logic to the IC provides built-in self test (BIST). Such logic typically comprises a linear feedback shift register and a pseudo-random test pattern generator, thus minimising the stimulus and response vectors to be stored in the BIST circuitry. Because BIST uses the same types of transistors as the rest of the circuit, the tests can run at the maximum clock rate. The availability of Boundary Scan and BIST greatly improves the information gained, and simplifies the testing during wafer probing. By probing just a few of the IC pads and the four TAP terminals instead of probing all pads, and initiating the test routine, a significant portion of the logic can be exercised. For example, Vertex Semiconductors (San Jose, California) has achieved 99% fault coverage by accessing just 20 pads per chip, thereby avoiding the cost (up to $10,000) and alignment problems of a 300 pin probe card.

5.3 Modelling Approach to Testing Analog and Mixed Signal ICs

The problem of testability is different when testing analog circuits, because access is not the problem, duration is. Testing mixed signal devices, in particular analog-to-digital converters (ADC), can be very time consuming - testing all possible output codes of a 13 bit ADC requires 213 (8192) different values of input voltage. An effective alternative /10/ is to solve the 13 independent equations from 13 sets of information obtained by measurements made at each binary exponent, thereby obtaining the data to calculate, rather than measure, all 8192 values. Hence the skills of the test engineer may now be directed at defining the variables and the reduced set of test points and setting up the calculation program, in order to fully characterise the ADC. Commercially developed aids such as QR Factorisation (QRF) (factoring a right (R) triangular matrix and an orthogonal (Q) matrix) are available to make machine solutions less subject to computer rounding errors. Where mixed signal circuits are more complex, then partitioning into individual testable segments and extra test access terminals are necessary to permit board level diagnostics, as described later.

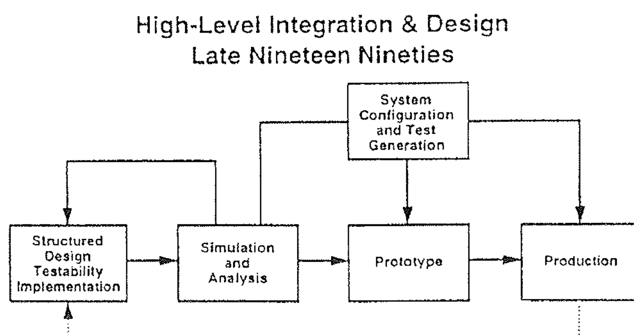

Fig. 7. Design to test

6. EXTENSION OF TESTABILITY TECHNIQUES TO CIRCUIT BOARDS AND MCMs

6.1 Board Level Testability

Ideally, the circuit design can extend the test bus throughout the PCB or the MCM (Fig 6) /11/. Testing is then effected through a board-level maintenance controller to facilitate production testing of the assembled PCB or MCM. Boundary scan at this level works by passing test data or instructions from TDO of one IC to TDI of the next, allowing test information to be scanned through the interconnected ICs and enabling access to each IC to be interrogated in turn. If the ICs were previously tested, then the same static vectors can be reused for testing the IC when it has been assembled on the PCB or MCM. The versatility of the technique is such that the testability can then be hierarchically escalated to the equipment level to enable the PCBs to be tested and diagnosed at the system level in the field by means of a system diagnostic bus. This would avoid the return of some 60% of boards from the field, subsequently found to be fault-free, saving considerably in logistics and cost. Standards are already emerging in this area, for instance the IEEE proposals:

- P896 FutureBus+ for modules, backplanes and chassis,
- P1396 COMBUS for a standard backplane interface bus protocol for high speed communications access to Synchronous Optical Network (SONET) and Synchronous Digital Hierarchy (SDH) based networks,
- P1149.x series for equipment design for testability.

Proprietary systems already in use include IBM's Diagnostic Expert for Testing (DEFT) /12/ and BT's Line Card diagnostics system. Both systems make use of field experience and expertise to build the rules for knowledge bases covering the range of faults identified. Thereafter, because the rules are the same for all users, and they are guided through the diagnoses, the users' skills are reinforced with use, and gets fed back into the knowledge base.

ATE is already available from many suppliers to test JTAG ICs and PCBs. In parallel, Computer Aided Engineering (CAE) software emphasis enables involvement of test designers in the earliest stages of design and HDL methodology /13/. Already there are novel simulation tools such as the TI SimuBoard which provides software "breadboard" simulation of a DSP application by combining ASICs, standard device models, JTAG DFT functions and board timing delays.

6.2 LSSD and Boundary Scan Solutions for MCMs

Motorola provides both IC and systems solutions, and has developed expertise in volume production of MCMs, including the essential test methodology /14/. The individual chips incorporate special features for their testability in production as monolithic ICs. The solution consists of LSSD for random logic fault coverage greater than 95% of individual chips, and boundary scan corresponding to P1149.1, together with some non-standard P1149.1 instructions via TAP. Thus the need for additional special sort die /15/ to invoke special test instructions is eliminated. In the example, high MCM yield is achieved by a combination of Main Control Chip and a smaller support chip which has high fault coverage (>99%) at wafer probe which may be tested at high speed at 66 MHz. The yield is then limited by the lesser fault coverage Control chip. MCM testing is effected by using the LSSD test control pins (multiplexed) to set the combined die function pins (databus and address) into a high impedance tri-state condition and de-select chips not being tested while using the original pattern structure to test the selected chip with LSSD and functional patterns. This fulfills the requirements for cost-effective MCM production that there are no extra overheads in space, pin-out or test procedures.

Complex MCMs incorporate many costly VLSI chips built on costly multilayer substrates. Therefore, they must be designed with diagnostics testability to enable rework. Not all available VLSI incorporate P1149.1 testability features. In these circumstances either the substrate can be designed to facilitate testability or additional circuitry is necessary. A complex DRAM MCM developed by Blood and Flint /16/ incorporates P1149.1 featured buffer circuits on all Address and Control inputs and bidirectional input/output (I/O) data lines. Thus all MCM I/O terminals have P1149.1 registers connected in a scan path for board/MCM assembly and diagnostics. Although the RAM chips do not have P1149.1 features, those on the buffer internal ports provide for MCM assembly fault (wirebonds, tracks) diagnostics via an MCM P1149.1 TAP. The outcome comprises nine P1149.1 buffer chips to verify I/O and interconnect, six extra pin out nodes connected to the DRAM RAS and CAS signals for DRAM diagnostics plus fifty two test probe points for MCM internal diagnostics. A similar exploitation of partial population of an MCM P1149.1 ICs is reported by Posse /17/ in which an MCM comprising four P1149.1 featured ICs and two non conforming ICs, in which diagnosis was achieved by disabling the non-conforming ICs from terminations on MCM. Today, complex MCMs are built onto active silicon substrates incorporating simple switching functions. Current testability developments, for example by NS, are exploiting this opportunity to build scan rings into such active substrates in order to access chips which do not have P1149.1 capability. Clearly practical solutions are therefore optimised using P1149.1 boundary scan chips where possible, with additional partitioning and test point access to provide diagnostics access into the assembled MCM.

7. AT WHAT STAGE OF THE PRODUCT SHOULD TESTABILITY BE ADDRESSED?

7.1 Design to Test

Design engineers may no longer "Design for Test" and pass their designs "Over the Wall" to Production Test engineers. Instead, it is clear that design and production engineers have learned that they are part of the same team, that the wall has to be removed (Fig 7) and they now have to "Design to Test".

7.2 Cost Benefit of Design-to-Test

A new analysis for this paper of an earlier analysis by Mitre /18/ has taken account of product lifecycles in today's marketplace (Fig 8). The new analysis shortens the lifecycle to around 10 years from the previous 20 years and finds that there is a consequential marginal increase of the impact of design on subsequent lifecyle costs - that 72% of operation and maintenance costs are determined at the design stage of a product, a further 13% being influenced at the subsystem development stage. In other words, only 15% of operation and maintenance costs can be controlled by those responsible for operation and maintenance! Therefore Design-to-Test is crucial in controlling logistics and consequent costs of all systems operations.

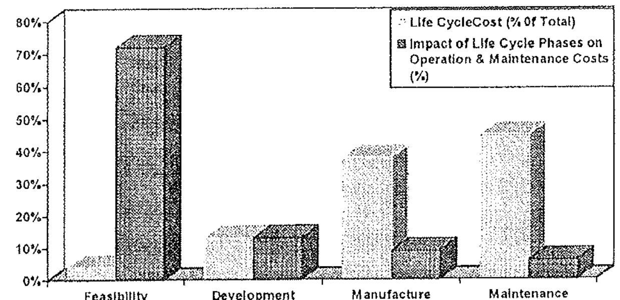

Fig. 8. Causes of life-cycle costs

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A LOW COST FORCE SENSOR FOR AN ELECTRONIC SCALE

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Keywords: kitchen scales, electronic scales, low cost, thick film sensors, thick film technologies, thick film resistors, piezoresistivity, thick film strain gauges, Wheatstone bridges, spring elements, double bending beams, signal processing, microcontrollers, electronic modules, LCD displays

Abstract: A low cost electronic scale with a weighing range from 10g to 3kg was developed by taking advantage of a low cost thick film strain gauge on a double bending beam as a spring element. After accelerated tests the characteristics of the low cost thick film load sensor were measured and evaluated. In the light of the results and economic aspects, the materials and construction with optimum characteristics were chosen. An appropriate electronic circuit provides the sensor signal conditioning and converts the measured load into a digital display of the weight. A battery operated electronic circuit with low current consumption, based on a microcontroller, was developed and constructed for an electronic scale module.

Cenen senzor sile za elektronsko tehtnico

Ključne besede: tehtnice gospodinjske, tehtnice elektronske, cene nizke, senzorji debeloplastni, tehnologije debeloplastne, upori debeloplastni, piezoupornost, senzorji sile debeloplastni, Wheatstone mostički, elementi vzmetni, konzole upogibne dvojno, procesiranje signalov, mikrokrmilniki, moduli elektronski, LCD prikazalniki

Povzetek: Predstavljamo razvoj gospodinjske elektronske tehtnice z merilnim obsegom od 10g do 3kg. Raziskave na področju senzorjev sile so omogočile izbiro optimalnih materialov in tehnoloških postopkov za izdelavo cenenega senzorskega elementa v debeloplastni tehnologiji. Razviti analogni in digtalni elektronski moduli pa omogočajo obdelavo senzorskega signala od ojačanja, A/D pretvorbe, mikroprocesorske obdelave do krmiljena LCD prikazalnika. Baterijsko napajan elektronski modul z nizko tokovno porabo je realiziran z uporabo mikrokontrolerja in ustrezne elektronske periferije.

1. INTRODUCTION

The most important aspects for successful development of an electronic kitchen scale are good-looking design, functionality and low price. Our task was to develop an appropriate sensor element and the electronics.

The required characteristics are: a weight measuring range from 10 g to 3 kg, and an accuracy $\pm 0.2\%$ of the full range. Other requirements are battery operation, self calibration, automatic turn OFF and taring mode function. The weight value must be displayed on a $3^1/2$ digit LCD display.

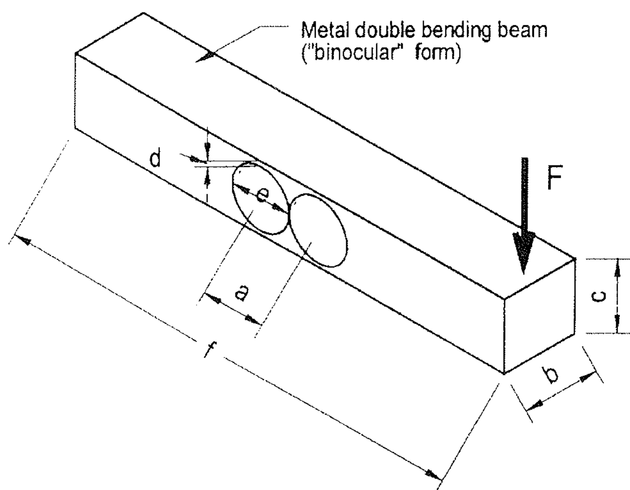
For this application the spring element and strain gauge were designed and analog and digital electronics for signal processing were developed. Cost breakdown analysis shown that a conventional metal foil strain gauge is the most expensive element in an electronic kitchen scale. Therefore, the right choice of strain gauge can effectively reduce the price of the force sensor element. Available and well known thick film technology was used to design a strain gauge based on thick film resistors. A thick film strain gauge offers the advantages of an enhanced sensitivity as compared with a metal foil strain gauge, due to higher gauge factors, and a lower temperature coefficient of resistivity than a silicon strain gauge /1/.

2. FORCE SENSOR

The force sensor element is the "heart" of an electronic kitchen scale. The force sensor element consists of the spring (elastic) element and the attached strain gauge. In our case the force (load) is translated into a signal voltage by the resistance change of the thick film strain gauge which is printed and fired on a ceramic (Al_2O_3) substrate and bonded with adhesive directly to the aluminium double bending beam of the spring element.

2.1. Spring element

The most critical mechanical component in the scale is the spring element for the force sensor. It must direct the applied load (force) into a uniform, calculated strain path for precise measurement by the bonded strain gauge. For our application we designed an aluminium double bending beam ("binocular" form) shown in Figure 1. Due to its high resistance to bending moments and torsion, the double bending beam is less sensitive to disturbance resulting from incorrect application of loads. It exhibits significantly better guidance properties than a simple bending beam. The material ($AlCuMg_2$) for the double bending beam has a Young' modulus of 73,000 N/mm^2 with a temperature coefficient of $-580\times10^{-6}/K$ and thermal expansion coefficient of $23\times10^{-6}/K$.



Strain of double bending beam:

$$\varepsilon = \frac{1.5xFxa}{Exbxd^2}$$

E .... Young's modulus (N/mm^2)
F .... Force (N)

Dimensions of dual bending beam:
a ...... 10.6 mm
b ...... 13.0 mm
c ...... 12.0 mm
d ...... 1.0 mm
e ...... 10.0 mm
f ...... 80.0 mm

Fig. 1: Aluminum double bending beam

The working principle of the double bending beam is shown in Figure 2. When a force is applied to the sensing element, the strain is concentrated at two points of the beam. The sensing resistors are located at these two points. The resistors of the attached strain gauge form a Wheatstone bridge (Figure 3 and Figure 4). R1 and R3 are under tensile strain, and the resistors R2 and R4 are under compressive strain.

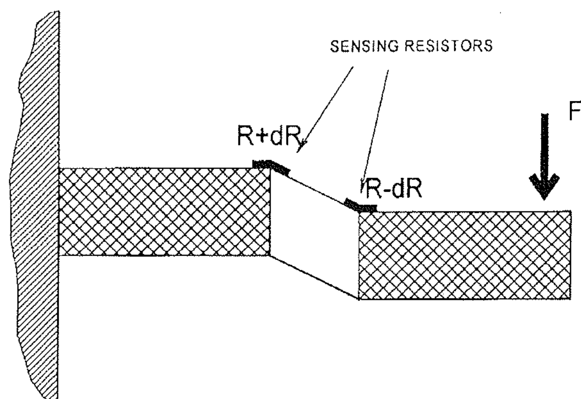


Fig. 2: Working principle of the double bending beam.

2.2. Thick film strain gauge

A strain gauge is a device capable of translating a deformation (strain) into an electrical signal. The working principle is piezoresistivity which is the property of materials to change resistivity under strain. The sensitivity to strain of a certain material is indicated as a gauge factor (GF). The gauge factor is defined as the ratio between the fractional change in resistance (dR/R) and the strain induced in the resistor by an applied stress.

The thick film strain gauge is designed with four thick film resistors printed and fired on the alumina substrate. The shape and dimensions of the ceramic substrate with the thick film resistors are shown in Figure 3. The four sensing resistors having a size of 2.0 mm × 1.5 mm form a Wheatstone bridge (Figure 4). After previous investigation of the piezoresistivity of thick film resistors /2,3,4,5/, we chose resistor material with a sheet resistivity of 1,000 Ohm/square. Thick film resistor materials have gauge factors up to 20. For the specific demands of our application we chose material with a gauge factor of around 8.

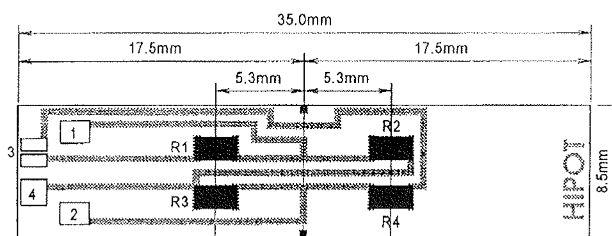


Fig. 3: Ceramic substrate with thick film resistors connected in Wheatstone bridge.

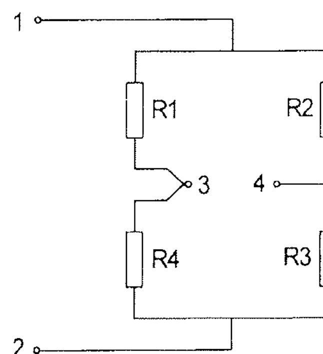


Fig. 4: Wheatstone bridge

2.3. Assembly

An important factor in optimising the force sensor characteristics is the assembly technology /6/. The force must be transferred to the sensing element without distortion. This problem was solved by the mechanical construction. Special attention was paid to mounting the ceramic substrate on an aluminium beam (Figure 5), because this process has a great influence on the

linearity, repeatability, stability and creep of the force sensing element. For better linearity, repeatability and stability, it is vital that the bonding material has a high adhesion between ceramic and metal, and a high resistance to plastic deformation.

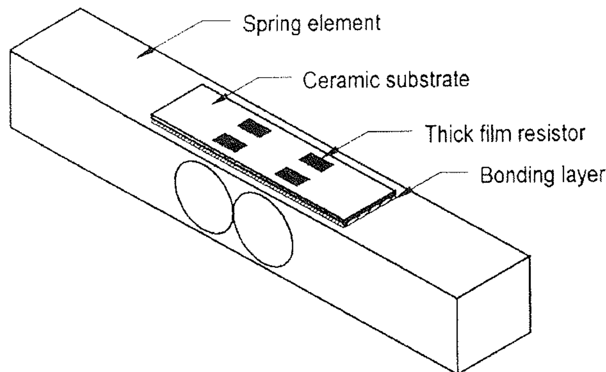


Fig.5: Spring element with thick film strain gauge attached

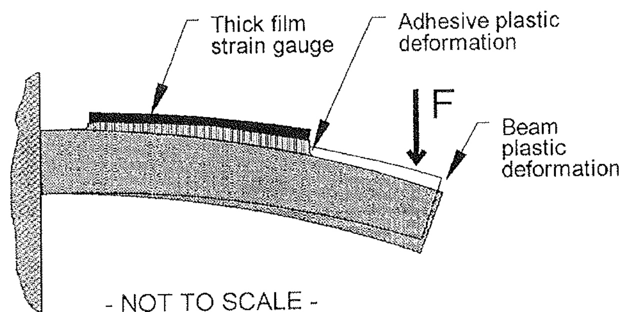


Fig. 6: Principle of compensation of adhesive plastic deformation with beam plastic deformation

If the force sensor is subjected to a static strain, its resistance changes with time, despite the constant strain in the sensor element. These changes in the measured signal take place very slowly and the sensor output is said to be subject to "creep". The cause lies in the characteristics of the bonding layer between the ceramic substrate and the aluminium beam, and also in the beam itself, which transfers the strain. The creep of the bonding layer depends on the bonding material and the thickness of the layer. The creep of the beam depends on its material and construction. Plastic deformation of the bonding material leads to a decrease of signal, and plastic deformation of the beam material leads to an increase of signal. Therefore it is possible to compensate one creep by the other with the right combination of dimensions and materials in the bonding layer and beam. The principle of creep compensation is shown in Figure 6.

2.4. Testing

For a low cost force sensor we investigated the bonding of the thick film strain gauge on the spring element using different bonding materials. All the tested materials were polymeric adhesives used for ceramic-metal bonding. To evaluate the results we compared them with reference samples made with metal foil strain gauges. These force sensors were made under supervision of a metal foil strain gauge producer. The sensor elements were prepared with different bonding materials and tested for sensitivity, temperature coefficient of sensitivity, offset, creep, stability, linearity and repeatability.

The accelerated tests consisted of:

- long term ageing at 100°C
- temperature cycling (1 cycle: 15 min/-25°C, 5min/25°C, 15min/125°C, and 5min/25°C)
- constant loading (30 N),
- overloading (100 N)
- periodical loading (30N with 2.5 seconds period)

After each test the samples were inspected. The output signal of the Wheatstone bridge with a stabilised bridge voltage of 5V was measured as a function of increasing and decreasing applied force with several repeats. For creep measurments the force sensors were loaded for 10 minutes with 30N and then unloaded for 10 minutes. During this test the output signal of the Wheatstone bridge was measured automatically.

2.5. Results

Figure 7 shows the measured output signals of the force sensors with thick film and metal foil strain gauges, and Figure 8 shows the creep of the same samples.

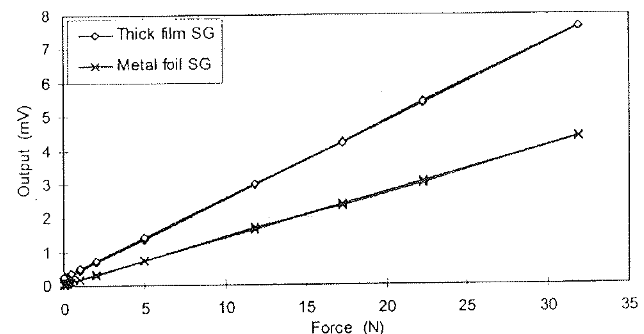


Fig. 7: Output characteristics of the force sensor with thick film and metal foil strain gauges (SG)

Other characteristics of the thick film force sensors such as sensitivity, temperature coefficient of sensitivity, offset, creep, linearity and repeatability are shown in Table 1 and Table 2. Linearity and repeatability are presented as the R-squared value. R-squared values near 1 indicate a good fit to linearity and repeatability.

After the experimental investigation of the low cost force sensors with a thick film strain gauge and different polymer adhesives, compared with metal foil strain gauge and analysis of the results, we chose the polymer material with optimal characteristics. In comparison with a metal foil strain gauge, sensors made with a thick film strain gauge have higher sensitivity, a lower tempera-

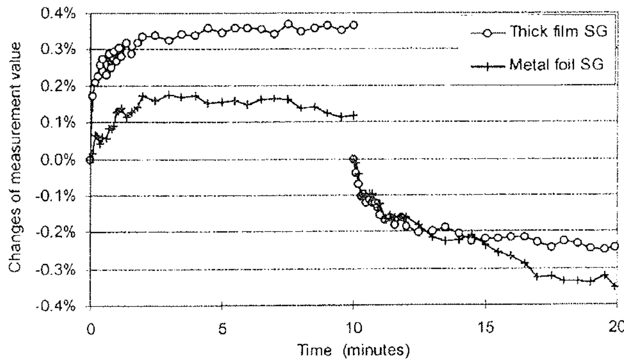


Fig. 8: Creep dependence of the force sensor with thick film and metal foil strain gauges (left-loaded, right-unloaded).

ture coefficient of sensitivity, a relatively high offset, higher uncompensated creep and better long time stability. The offset is adjusted later with an electronic circuit. Creep can be reduced by optimising the thickness of the bonding layer.

Table 1: Characteristics of the force sensor

	Metal foil strain gauge	Thick film strain gauge
Sensitivity (μV/V/N)	30	45
TC of Sensitivity (10^{-6}/K)	-1.000	±150
Offset (mV)	/	±4
Linearity - R Squared (number of nines)	5	5-6
Error because of uncompensated creep after 1 hour constant loading at 30 N	0.2%	0.4%

Table 2: Linearity and Repeatability of thick film force sensors (R Squared)

	Metal foil strain gauge	Thick film strain gauge
Initial value	0.999997	0.999999
After 100 temperature cycles	0.999954	0.99996
After ageing 1.000h/100°C	0.999928	0.999998
After 11.000 load cycles	0.999992	0.999999

The final form of two low cost force sensors with thick film strain gauges are shown in Figure 9. Both sensors are intended for use in an electronic kitchen scale with a weighing range from 10 g to 3 kg, and an accuracy of ±0.2% of the full range. One sensor element is constructed with an aluminium double bending spring element, and other with a steel simple bending beam.

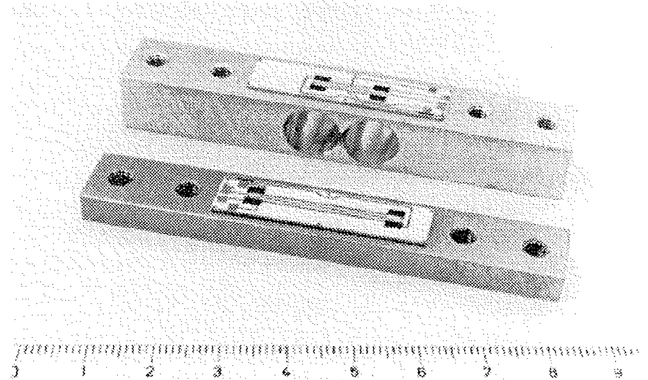


Fig. 9: Low cost force sensors for use in an electronic kitchen scale. The thick film strain gauge is mounted on a double bending spring element (above) or on a simple bending beam (below)

3. SIGNAL PROCESSING

The electronic circuit for signal processing was developed with the objectives of function requirements, battery operation and request for a low cost. The block diagram of the electronic circuit is shown in Figure 10 and consists of voltage regulator, temperature sensor, signal amplifier, microcontroller, EEPROM, LCD display and two keypads.

The electronic circuit is supplied by one 9V battery. A low consumption voltage regulator stabilises the supply voltage at 5V. The circuit was designed for a current consumption of 2mA during weghing and only 10 μA in the power down mode. Measuring units are "g" and "kg" or "oz" and "lb". A tare function can be achieved by pushing the Tare key. The ON/OFF key activates the scale or puts it into the power down mode. By switching the scale ON, automatic tare and autozero are activated. When the scale is not in use for 3 minutes, it goes into auto power down mode. Calibration of the scale is done after assembly and and can be repeated any time. The calibration procedure simply requires loading the scale with two different known loads and conforming them by

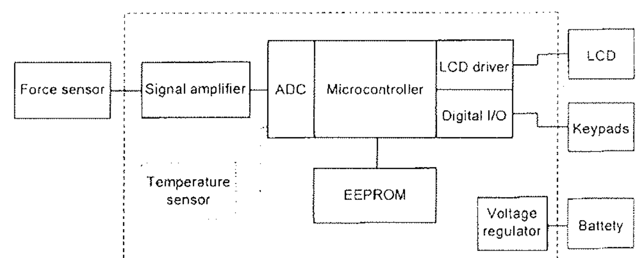


Fig. 10: Block diagram of electronic scale module

pushing the key. After this procedure the characteristic of the sensor element is saved in EEPROM. The electronic scale module has the possibility of including a temperature sensor for tempereture compensation. The outline and dimensions of the electronic scale module are shown in Figure 11.

Features of the scale:

- Weighting capacity: 10g ÷ 3kg
- Units; g, kg, (optionally oz, lb)
- Resolution:
  - d = 1g (10g ÷ 1000g)
  - d = 1.5g (1000g ÷ 3000g)
- 3½ digit LCD display
- Tare function
- Autozero function
- Calibration function
- Auto power down mode
- Battery operation (1 battery - IEC R6 PF 22 9V)
- Current consumption:
  - 2 mA in use
  - 10 μA in power down mode
- Operating temperature: +5°C ÷ +40°C
- Storage temperature: +0°C ÷ +84°C

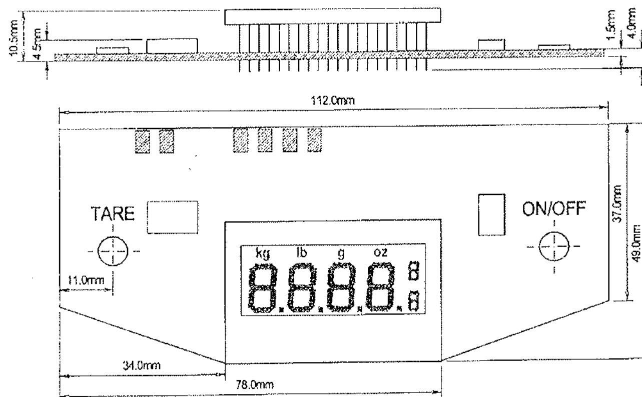


Fig.11: Electronic scale module

4. CONCLUSIONS

A low cost force sensor was developed by taking advantage of the piezoresistive effect in thick film resistors printed and fired on a ceramic substrate. The substrate was bonded on a metal double bending beam. With the chosen materials and procedures the following results were obtained; a sensitivity of the load cell of 40÷50 μV/V/N, a sensitivity stability of ±0.5%, a temperature coefficient of stability lower than $\pm 100 \times 10^{-6}$/K, a maximum offset of ±4mV, an offset stability of ±0.5mV, and the drift of the output signal due to creep of less than 0.2%. For this force sensor an electronic scale module was developed. An electronic circuit with low current consumption based on a microcontroller ensures that it satisfies all purpose requirements.

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RADIATION DAMAGE IN Si MICROSTRIP DETECTORS

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Keywords: semiconductors, silicon devices, Si silicon microstrip detectors, radiation damages, irradiation damages, radiation defects, irradiation of detectors, test measurements, nuclear instruments, HEP, high energy physics, radiation hardness, ionization damages, ionizing radiation, NIEL, non-ionizing enegy loss, PKA, primary knock-on atoms, LHC, large hadron colliders, FDV, full depletion voltage, CV method, capacitance-voltage method, CCE, charge collection efficiency

Abstract: Radiation damage in silicon microstrip detectors will play an important role in the design of tracking devices at future high luminosity experiments. Overview of macroscopic effects is given. Increase of leakage current, change of depletion voltage and decrease of charge collection efficiency are the most important effects, however operation after irradiation with few 10^{14} particles cm^{-2} is still possible.

Radiacijske poškodbe v mikropasovnih detektorjih

Ključne besede: polprevodniki, komponente silicijeve, Si detektorji mikrotrakasti, poškodbe vsled sevanja, poškodbe vsled obsevanja, napake vsled sevanja, obsevanje detektorjev, merjenja preskusna, instrumenti jedrski, HEP fizika energij visokih, odpornost proti sevanju, poškodbe vsled ionizacije, sevanje ionizirajoče, NIEL izguba energije neionizirajoče, PKA atomi izbiti prvotno, LHC trkalniki hadronski veliki, FDV napetost osiromašenja polnega, CV metoda kapacitivnost-napetost, CCE izkoristek zbiranja naboja

Povzetek: Radiacijske poškodbe v mikropasovnih detektorjih so pomembne pri načrtovanju sledilnikov nabitih delcev v prihodnjih eksperimentih z visoko luminoznostjo. Podan je pregled makroskopskih posledic, ki jih povzročijo delci.
Glavne posledice so: porast mrtvega toka, sprememba napetosti, potrebne za osiromašenje detektorja in zmanjšanje učinkovitosti zbiranja naboja. Rezultati meritev so pokazali, da je sledenje nabitih delcev možno tudi po prehodu več kot 10^{14} delcev cm^{-2}.

1. Introduction

Silicon microstrip detectors became a common tool in high energy physics experiments after introduction of planar technology on low resistivity silicon for production of silicon devices /1/. This technology allows segmentation of the junction and the use of the segments to determine particle positions. In microstrip detectors these segments are narrow strips with widths around 100 microns. Each of them represents a p-i-n diode, which is then used to detect the traversal of an ionizing particle through silicon. Commonly, p strips are produced on n bulk material yielding single sided segmentation and detection of particle position in one dimension. Double sided detectors, having strips on p and n sides, have been also produced and used in experiments /2,3/.

To make use of the high resolution of microstrip detectors for tracking, the precision should not be compromised by multiple Coulomb scattering. Therefore it is important to have thin detectors. The normal thickness of existing detectors is about 300 microns determined by the practical limit of processing 4-inch wafers. In addition, the signal for high energy particles is proportional to the detector thickness. Therefore a further reduction of detector thickness would degrade the signal. For applications with a large number of detection channels a sufficient signal to noise ratio is critical for a good position resolution and low background occupancy.

Detector development has been accompanied by the development of readout electronics. Low noise and power, and large density of input channels are the main constraints for the chip design. For microstrip detectors, various strip pitches have been used, depending on the resolution requirement /4,5,6/. Currently 25 micron readout pitch is a practical limit in detector fabrication. With that, a few micron position resolution has been achieved in a test beam.

Most currently running colliding beam experiments have a large vertex detector made of several layers of silicon microstrip detectors /4,5,6/. Radiation in existing experiments does not cause any significant damage to the detectors and several years of running time could be achieved without considerable degradation in the detector performance. However, the new experiments in construction (HERA-B at DESY, Hamburg and ATLAS, CMS at LHC, CERN, Geneva) at high-rate and energy proton accelerators will put new requirements to the radiation hardness of detectors. Particle fluences and the associated radiation dose will by far exceed that encountered by any existing tracking detector. The area covered by detectors will be in the order of few ten m^2 and the number of channels will be of the order of 10 million. Unlike the existing detectors, there is little prospect of replacing them during the lifetime of the experiment (~ 10 years) and maintenance access for repairs will be restricted. Therefore the detectors should be sufficiently radiation hard to survive in the hostile environment during the whole data taking period. Radiation

hardness of readout electronic is a separate problem, studies may be found elsewhere /7/.

2. Radiation effects

The effects of radiation to silicon microstrip detectors may be divided into two categories. The surface damage depends on detailed processing steps and on detector design, while the bulk damage relates to generic properties of the crystal itself.

Surface damage is caused by ionizing radiation (e.g. electrons, γ rays) causing irradiation damage by ionization in the silicon dioxide layer and at the Si-SiO_2 interface. The charge built up due to holes being trapped in the oxide causes an increase of the electron density in the accumulation layer at the silicon surface. Ionizing radiation doses expected at future experiments are of the order of 100 kGy (10 Mrad). Interstrip resistance and capacitance measurements are used to estimate the damage of ionization to microstrip detectors. Measurements of the CERN RD-20 collaboration have shown only a slight (20-30%) increase of the capacitance, saturating at doses higher than 10 kGy (Figure 1., from ref. /8/). This effect is tolerable in future applications, since it would only marginally increase the electronic noise - depending on detector size. The same collaboration measured the ionizing radiation effects on n sided detectors. With a proper design of the interstrip isolation /9/, radiation resistance was achieved.

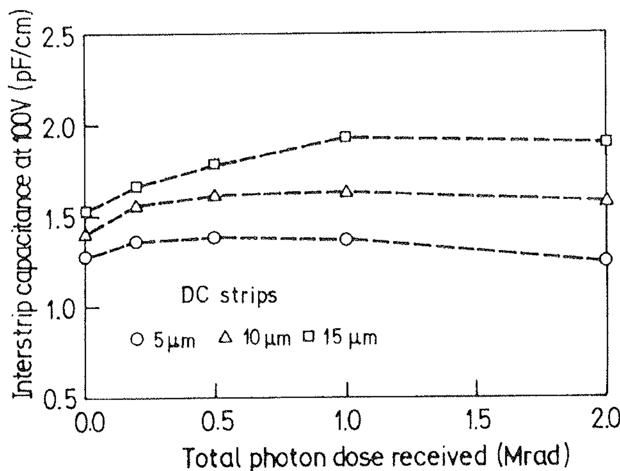

Fig. 1: Interstrip capacitance at 100V, 1 MHz as a function of photon dose /8/.

Bulk damage in Si lattice causes more concern to future high energy physics applications. The ionization energy loss in silicon bulk is a reversible process in itself (electron-hole pairs recombine) and causes no durable defects. However, due to the interaction of the radiation with silicon atoms the periodic structure of the lattice is destroyed locally, i.e. silicon atoms are dislocated. The displacement damage in the silicon bulk corresponds to the non-ionizing energy loss (NIEL). Lattice atoms displaced by incoming particles are termed primary knock-on atoms (PKA). An average energy E_d of about 25 eV /10/ is required to dislocate a PKA. The maximum energy transferred from a particle of energy E_n to a silicon atom can be deduced from collision kinematics:

$$E_{max} = 4\, E_n\, M_n\, M_{Si}/(M_n + M_{Si})^2$$

where M_n and M_{Si} are the incoming particle and Silicon atom masses, respectively. More energy is transferred for heavy particles than for light ones. For example, for 1MeV neutrons E_{max} = 130 keV, while for 1MeV electrons E_{max} = 120 eV only. Therefore, heavy particles are causing considerably more displacement damage to the bulk. If more than Ed energy is transferred, the PKA will lose the surplus of energy by ionization or further displacements of lattice atoms which may proceed in a cascade manner. Consequently, from a primary PKA, a number of vacancies (V) and interstitial (I) atoms are created along its path, forming a cluster. In the interior of the cluster, where initial concentrations of vacancies and interstitials are high, direct recombination occurs and most I-V pairs annihilate on a very short time scale. Those that do not get annihilated may move to the surface or form relatively stable complex defects. Interstitial atoms diffuse out from clusters more rapidly than vacancies. So the main known complex defects are vacancy-related: the divacancy (V-V), the silicon E centre (V-P) composed of a vacancy and phosphorus atom in adjacent lattice positions, and the silicon A centre (V-O) composed of an oxygen atom and a vacancy. The actual ratio of defects formed depends on the concentration of impurities present in the silicon.

Non ionizing energy loss per unit length may be calculated from:

$$(dE/dx)_{NIEL} = \rho\, N/A \int E_r\, d\sigma/dE_r\, L(E_r)\, dE_r$$

where ρ is density, N and A are Avogadro's number and the atomic weight of silicon, $d\sigma/dE_r$ is the differential cross section to produce a recoil fragment with energy E_r and $L(E_r)$ is the fraction of this energy which appears as NIEL at the particular recoil energy E_r /11/. Extensive calculations have been performed for silicon /12,13,14/ for various particles (Fig. 2).

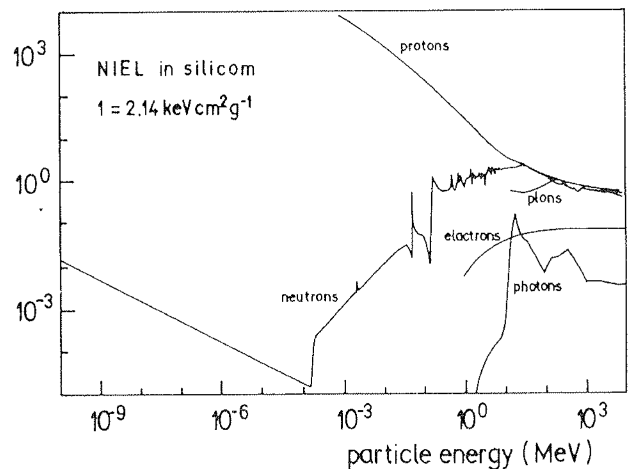

Fig. 2: NIEL data for use in detector damage projections

Study of bulk defects and predictions for future applications are obscured by the fact that most of the damage to the detectors will be caused by pions and neutrons, while irradiation studies of detector performance have been done predominantly with neutrons and protons. In order to allow a universal comparison of results it is common practice to refer damage to the equivalent fluence of 1 MeV neutrons which would have caused the same NIEL as the fluence really applied. As a standard, $(dE/(\rho.dx))_{NIEL}$ = 2.14 keV cm^2g^{-1} is usually assumed for 1 MeV neutrons. Measurements up to now have generally confirmed that, within the accuracy of calculations, NIEL adequately reproduces the dependence of bulk damage on particle type and energy.

3. Macroscopic effects

Microscopic defects produced by bulk damage manifest themselves as a change of macroscopic behavior. There are three important effects for microstrip detectors: increase of reverse current, change of depletion voltage and degradation of charge collection efficiency. In high energy physics experiments it is very important to have the efficiency of charged particle detection as high as possible. All of the above mentioned macroscopic effects deteriorate detector performance.

3.a. Increase of leakage current

The increase of leakage current with particle fluence Φ is commonly described by:

$$\Delta J = \alpha\Phi$$

where ΔJ is the difference of current density before and after irradiation, and α is the current damage constant. The microscopic explanation of the constant alpha relies on proportional production of current generation centres to the fluence. The radiation induced current reduces after irradiation due to self annealing of defects, with several different time constants /15/.

$$\alpha = \sum_i \alpha \exp(-t/\tau_i) + \alpha_\infty$$

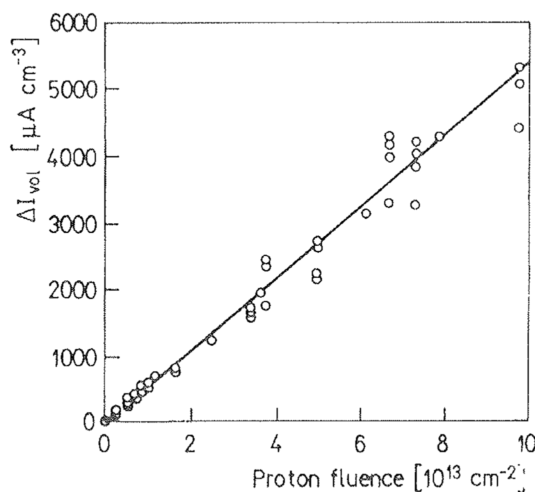

Fig. 3: The change in volume leakage current (normalized to 20°C and corrected for self annealing) versus proton fluence /16/.

The range of time constants τ_i at room temperature is from a few minutes to a few days. The constant part of the leakage current increase has a value

$$\alpha = 4\ 10^{-17}\ \mathrm{A\ cm^{-1}}$$

at room temperature and represents roughly 40 % of the initial increase.

In order to compare measurements taken at different times it is important to correct for annealing. Figure 3 /16/ shows that the change in the leakage current is linear with fluence over two orders of magnitude. There is almost no difference between different resistivity n-type ad the p-type detectors. Measured current densities have shown that we may expect high leakage currents after 10 years of running experiments at LHC. One obvious way to reduce the current and its effect is to cool down the detector. This reduces the electronic noise and the probability of thermal runaway of detectors. Therefore it is foreseen to cool down the detectors to about -10°C during operation.

3.b. Change of the depletion voltage

The depletion voltage is an important parameter for running silicon microstrip detectors, the practical limit due to electrical breakdown of detectors and safety aspects in large experiments being about 500 V. It is essential to be able to bias the detectors above the full depletion voltage, otherwise some of the signal created by charged particles would be lost. Therefore microstrip detectors are usually made on high resistivity silicon wafers (resistance few kΩ cm and higher) in order to have a low depletion voltage. However during the irradiation new defects are created and the effective doping concentration (N_{eff}) changes, resulting in a change of the full depletion voltage (FDV). Neff and FDV are related by:

$$|N_{eff}| = 2\ \mathrm{FDV}\ \varepsilon\ \ \varepsilon_{Si} / (q\ d^2)$$

where epsilon is the dielectric constant, q the elementary charge and d the detector thickness.

FDV (and thereby N_{eff}) may be determined by different methods, for example measuring the pulse-height spectrum of charged particle signals (charge collection) or the detector capacitance value as a function of the bias voltage. The latter method (CV) has been adopted as a standard technique for FDV evaluation in irradiation studies.

N_{eff} has been measured for various bulk materials and at different particle fluences. A non-linear change of Neff measured on biased detectors can be observed for both n and p type materials at fluences below 10^{13} while at larger fluences Neff increases linearly. For low resistivity n starting material $|N_{eff}|$ drops close to zero and then increases with fluence (Figure 4, from /17/) thus changing the n-type silicon to p-type material. The latter effect is explained as generation of acceptor-like states in proportion to the fluence. It has to be noted that only the effective space charge changes from positive to negative. If the resistivity, i.e. the density of electrons and

holes, is measured in thermal equilibrium, silicon is found to become intrinsic with increasing fluence and the Fermi level adjusts close to mid-gap /18/. Experimental evidence for the type inversion behaviour is given by charge collection measurements which have shown that the space charge region starts to grow from the n side of the detector after type inversion /19/.

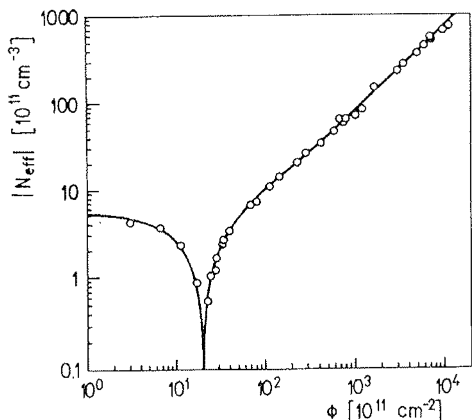

Fig. 4: Change of effective impurity concentration for 1 MeV normalized fluences /17/.

An explanation for the behaviour at lower fluences has not been generally adopted yet. There are two possible explanations. The first is primary donor (substitutional P) and acceptor (substitutional B) removal, and new acceptor creation /20/ while the second explanation assumes deep-level acceptor creation only /21/.

Donor removal could proceed through creation of V-P or C-P defects, which both have high annealing temperatures (~400 K, /22, 23/), and acceptor removal through the reaction $Si_i + B_s > B_i + Si_s$. Interstitial boron is known to be electrically inactive /24/, so acceptors are removed via this reaction by interstitial silicon atoms, produced by irradiation.

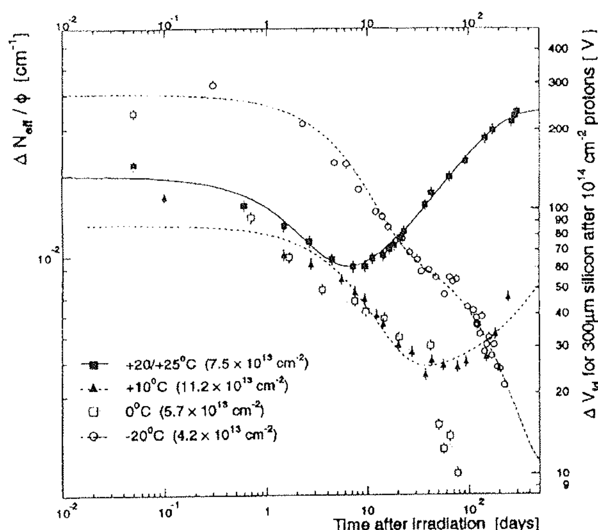

Fig. 5: Evolution of effective impurity concentration and depletion voltage normalized to proton fluence as a function of time after irradiation for detectors kept at the temperature indicated /15/.

The deep acceptor model just assumes creation of an acceptor level close to the mid-gap. Using the measured values of current density with fluence and occupancy from Shockley-Read-Hall statistics, a qualitative agreement with measured depletion voltages was found /21/ by adjusting the introduction rate of the acceptor state as a free parameter.

The time evolution of the depletion voltage has been measured (Figure 5 from /15/) at different temperatures. It may be noticed that two different processes are present. Annealing - reduction of N_{eff} after irradiation - is followed by reverse (long-term) annealing. Annealing may be explained as a first order process involving a dissociation of defects. The dissociation rate is proportional to their concentration resulting in an exponential time behaviour. More complicated and less understood is the reverse annealing process. In the case of two homogeneously distributed defects with concentrations N_{X1} and N_{X2}, which combine to a defect complex Y the creation rate is:

$$-dN_{X1}/dt = -dN_{X2}/dt = k\, N_{X1}\, N_{X2}$$

where k is reaction constant. If $N_{X1} << N_{X2}$ the equation reduces to the first order

$$N_Y(t) = N_{X1o}\,(1 - \exp(-k\, N_{X2}\, t)),$$

N_{X1o} being the defect concentration at t = 0, while if $N_{X1} = N_{X2}$ the reaction is of second order

$$N_Y(t) = k\, N_{Xo}^2\, t \,/\, (1 + k\, N_{X1o}\, t)$$

The main difference in time behaviour between first and second order reactions is the dependence of the characteristic time on the initial concentration for the second order. Good agreement for time dependence was found by fitting the measured data with a second order fit /25/.

Acceptor removal by irradiation may explain such behaviour. If interstitial Boron, which is electrically inactive, combines with a vacancy to produce substitutional Boron, a shallow acceptor is regenerated. This results in a decrease of bulk resistance and increase of depletion

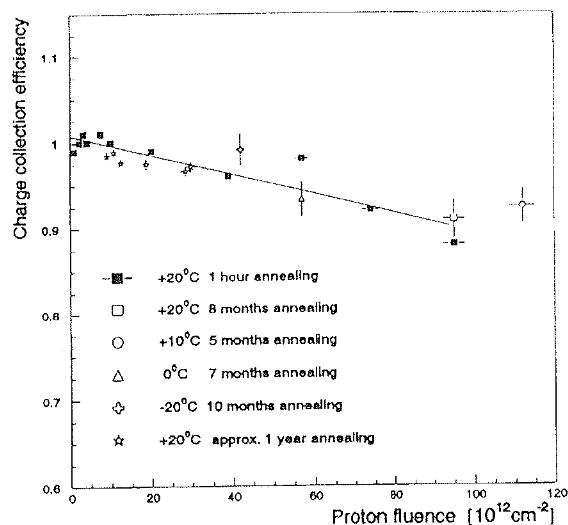

Fig. 6: CCE for relativistic electrons and for collection time of 20ns as a function of proton fluence /15/.

voltage with time. Both effects were confirmed by measurements /20/.

For detectors used at LHC experiments both annealing and reverse annealing have to be taken into account. The reverse annealing time constant strongly depends on temperature. This represents an additional argument for maintaining the detectors below 0°C since it effectively hibernates the reverse annealing process.

3.c. Charge collection efficiency

The charge collection efficiency (CCE) is defined as the charge collected for irradiated detectors normalized to the value measured before irradiation. In addition to the fact that it is sometimes impossible to fully deplete the detector after irradiation, due to the high voltages needed, additional trapping of charge may occur. This is caused by trapping centres produced by NIEL in the silicon. Charge collected by the readout electronics is therefore reduced since the charge trapped is not seen in the signal if detrapping does not occur within the time short compared to the shaping time of the readout electronics. The few existing data for detectors irradiated to 10^{14} particles/cm^2 /12,15/ with electronics having shaping times of about 20ns show that a CCE of 90 percent is still maintained (Fig. 6 from /15/) above the full depletion voltage.

4. Conclusions

A lot of research has been done in recent years in order to estimate possible radiation defects in silicon microstrip detectors after 10 years of operational time at future HEP experiments. Depletion voltages in excess of a few hundred volts have been identified as the main problem for stable operation of microstrip detectors at a large scale. All irradiations of detectors in test measurements have been done at at least two orders of magnitude shorter time than the actual running time of future experiments. A clear microscopic picture for the damage and reverse annealing is also not complete yet. Since radiation defect production and time evolution may still depend on the flux rate and temperature, still more work is needed in the next years if reliable predictions are to be made.

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EKOLOŠKO VARNEJŠI VISOKOTEMPERATURNI ELEKTROLITSKI KONDENZATOR

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Ključne besede: kondenzatorji elektrolitski aluminijevi, kondenzatorji visokotemperaturni, kondenzatorji nizkonapetostni, kondenzatorji visokonapetostni, kondenzatorji ekološko varnejši, elektroliti tekoči, varnost ekološka, območje temperaturno: -40°C do +125°C, napetosti naznačene: 10 V do 63 V, 200 V do 350 V, preskušanje vzdržljivosti, IEC 384-4 LL standardi = preskušanje vzdržljivosti, ESR upornost serijska ekvivalentna nizka, tok izmenični superponirani visoki

Povzetek: V članku je opisan razvoj ekološko varnejših, zahtevnih, visokotemperaturnih elektrolitskih kondenzatorjev (ELKO), katerih temperaturno območje uporabe je od -40°C do +125°C. Njihove glavne karakteristike so naslednje:

- nazivne napetosti od 10 V do 63 V in od 200 V do 350 V
- izvedbe: radialna, aksialna
- življenjska doba IEC 384-4, LL: min. 1000 ur / 125°C
- nizek ESR, visok superponiran izmenični tok

Ecological Safer High-temperature Electrolytic Capacitor

Keywords: aluminium electrolytic capacitors, high temperature capacitors, low voltage capacitors, high voltage capacitors, ecologically safer capacitors, liquid electrolytes,ecological safety, temperature range: -40°C to +125°C, rated voltages: 10 V to 63 V, 200 V to 350 V, endurance testing, IEC 384-4 LL standards = endurance testing, low ESR, low equivalent series resistance, high ac ripple current

Abstract: The development of the ecological safer radial and axial electrolytic capacitors (ELKO) for the temperature range from -40°C to +125°C is described. Their main properties are:

- rated voltages from 10 V up to 63 V and from 200 V up to 350 V
- series: axial and radial
- endurance test (IEC 384-4, LL): min. 1000 hours / 125°C
- low ESR, high ripple current

1. UVOD

Prve informacije o visokotemperaturnih elektrolitskih kondenzatorjih so se pojavile že pred več kot 20 leti in kmalu zatem so nekateri proizvajalci že dali na tržišče prve tovrstne elektrolitske kondenzatorje. Tudi naša tovarna se je že takrat intenzivno ukvarjala z razvojem tovrstnih ELKO in tudi uspela dobiti prve pozitivne rezultate z manjšimi, nizkovoltnimi ELKO. Takratna konstrukcija visokotemperaturnega kondenzatorja pa je bila dokaj draga, pogojevala je uporabo teflona kot materiala za zapiranje kondenzatorja. Poleg tega smo takrat uporabili elektrolit, katerega glavno topilo je bilo N,N dimetilformamid. Kot je znano, so formamidi topila, ki so med sedaj uporabljanimi topili v delovnih elektrolitih za ELKO najbolj ekološko nezaželjeni zaradi svoje toksičnosti. Visoka cena kondenzatorja in ekološka neprijaznost sta bila vzroka, zaradi katerih se proizvodnja ELKO za temperaturno območje uporabe od -40 do +125°C takrat v naši tovarni ni resno začela.

V zadnjih dveh letih smo dobili od naših kupcev kar precej povpraševanj po kvalitetnih visokotemperaturnih ELKO, zato smo začeli z razvojem teh ELKO na novih osnovah. Predvsem smo uporabili nove, cenejše materiale za zapiranje ELKO, nove anodne folije, ELKO papirje in pa elektrolite na osnovi manj nevarnih topil. Razvili smo radialno (tip RTH) in aksialno (ATH) izvedbo ELKO za napetostno območje od 10 V do 63 V in pa od 200 V do 350 V. Kupci, ki se pri nas zanimajo za te ELKO, jih nameravajo uporabiti pretežno v avtomobilski elektroniki.

V tem članku opisujemo rezultate razvoja elektrolitskih kondenzatorjev, ki lahko delujejo v temperaturnem območju od -40°C do +125°C. Njihova življenjska doba, preizkušena po IEC 384-4 je minimalno 1000 ur, njihovi parametri po 1000 urah življenjske dobe na +125°C in nazivni napetosti pa ustrezajo standardu IEC 384-4 LL.

2. SESTAVNI DELI ELEKTROLITSKEGA KONDENZATORJA

Radialni ali aksialni ELKO je sestavljen iz zvitka, ohišja, čepka, priključnih žic in izolacijske plastične prevleke. Zvitek je navit iz anodne in "katodne" folije (obe sta iz aluminija) in papirja. Anodna folija je že predhodno jedkana in elektrokemično obdelana (formirana) do določene napetosti, s čimer se ustvari na njej ustrezna plast oksida, ki predstavlja dielektrik kondenzatorja. Zvitek impregniramo v delovni elektrolit, ki opravlja funkcijo katode v kondenzatorju. Skici radialnega in aksialnega ELKO v prerezu sta prikazani na slikah 1 in 2.

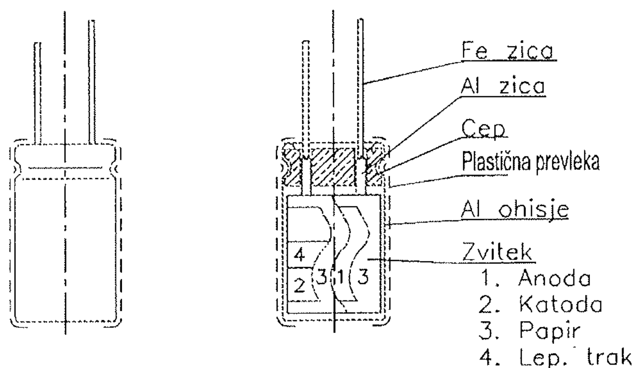
Stopnja jedkanosti anodne folije se stalno povečuje, kajti predvsem od nje je odvisna velikost kondenzatorja. Ker pa tudi z večjo jedkanostjo narašča omska upornost

kondenzatorja, ki jo izrazimo z ekvivalentno serijsko upornostjo (ESR), je potrebno poiskati kompromis med željo po majhnosti in s tem cenenosti ELKO in med zahtevanimi karakteristikami.

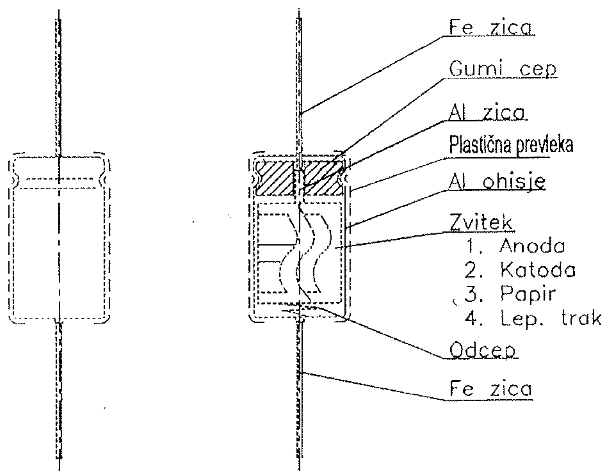
Napetost, do katere formiramo anodno folijo, je odvisna predvsem od nazivne napetosti kondenzatorja, maksimalne temperature obratovanja in zahtevane življenjske dobe ELKO.

Drugi velik vpliv na ESR ima uporabljen ELKO papir, s katerim navijemo zvitek.

Tretji delež vpliva na ESR ima uporabljen delovni elektrolit. Zato je naš cilj, da uporabimo delovni elektrolit s čim manjšo upornostjo ob istočasno zagotovljeni dovolj visoki iskrni napetosti, visokem vrelišču in nizkem ledišču.



Slika 1. Radialni ELKO



Slika 2. Aksialni ELKO

3. EKSPERIMENTALNI DEL

Opravljeno eksperimentalno delo lahko razdelimo v naslednje sklope:

- razvoj in izbor delovnih elektrolitov
- izbor elektrolitu ustrezne anodne folije
- izbor elektrolitu ustreznega ELKO papirja
- izbor elektrolitu ustrezne inkapsulacije
- izbor skrčljive plastične prevleke
- meritve parametrov ELKO in dovoljenega superponiranega izmeničnega toka
- preizkusi življenjske dobe ELKO

3.1. Delovni elektroliti

Iz pregleda literature smo se seznanili s stanjem na področju visokotemperaturnih delovnih elektrolitov /1,2,3/. Na kratko bi ta pregled lahko strnili v naslednje vrste aktualnih elektrolitov:

1. nizkovoltni elektroliti, katerih glavno topilo so formamidi
2. nizkovoltni elektroliti, ki vsebujejo kot ionogen kvarterne amonijeve soli in gamabutirolakton kot topilo
3. nizkovoltni elektroliti, ki vsebujejo kot ionogen sol organske kisline in terciarnega amina, topilo je gama-butirolakton
4. visokovoltni elektroliti, katerih ionogeni so amonijeve soli višjih organskih kislin, topila so glikoli

S prvo vrsto elektrolitov se zaradi ekoloških problemov nismo ukvarjali, mnogo pozornosti smo posvetili ostalim vrstam elektrolitov.

Za impregnacijo nizkovoltnih ELKO smo preizkušali elektrolite na bazi kvarternih amonijevih soli in pa elektrolite na bazi soli terciarnih aminov.

Elektroliti na bazi kvarternih amonijevih soli predstavljajo znaten napredek na področju elektrolitskih raztopin. Njihovo topilo je gama-butirolakton, ki je v primerjavi s formamidi ekološko mnogo sprejemljivejši. Ti elektroliti imajo to veliko prednost pred doslej znanimi, da so časovno in temperaturno zelo stabilni. Njihova pomanjkljivost je agresivnost do butilne gume. Uspelo nam je najti gumo, ki je tovrstni elektroliti ne korodirajo. Njihova druga pomanjkljivost je sorazmerno nizka iskrna napetost, zanesljivo delovanje omogočajo pri +125°C le kondenzatorjem do vključno 40V nazivne napetosti. Zato je bilo potrebno preizkušati tudi elektrolite na bazi soli terciarnih aminov, ki omogočajo zanesljivo delovanje ELKO nazivnih napetosti do vključno 63V pri +125°C. Za impregnacijo visokovoltnih ELKO smo preizkušali elektrolite na bazi glikolov in v njih raztopljenih amonijevih soli višjih organskih kislin.

Oznake preizkušanih elektrolitov, glavni ionogeni in topila:

A - tetrametilamonijev ftalat, gama-butirolakton

B - tetraetilamonijev maleinat, gama-butirolakton

C - tetraetilamonijev maleinat, gama-butirolakton

D - sol terciarnega amina in ftalne kisline, gama-butirolakton

E - sol terciarnega amina in ftalne kisline, gama-butirolakton

F - amonijeva sol višje organske kisline, etilen- in dietilen-glikol

Parametri elektrolitov:

oznaka	specifična upornost (Ωcm, 30°C)	iskrna napetost (V)	pH
A	110-125	80-90	6,8-7,3
B	80-90	80-100	6,0-6,7
C	105-115	110-120	6,2-6,5
D	125-145	100-110	6,8-7,0
E	160-180	120-130	6,5-7,5
F	550-650	460	6,8-7,8

Razlike, ki izhajajo le iz vrste uporabljenega elektrolita (oznaka DEL), so razvidne iz izmerjenih začetnih parametrov ELKO ATH 3300μF/10V:

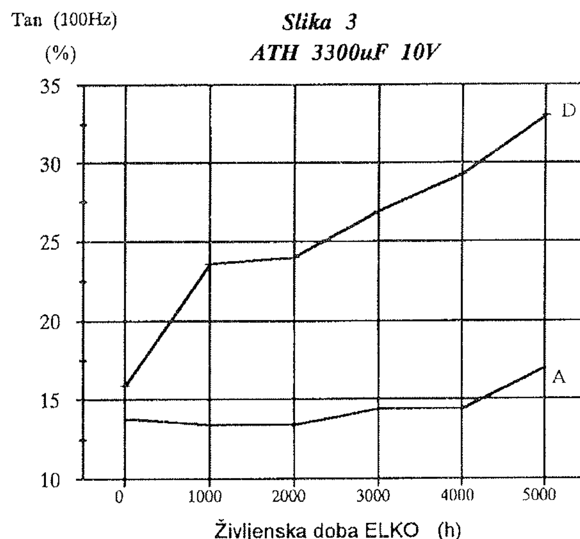
ELKO	DEL	C(μF)	tan delta (%)	Ipr (μA, 1min)
ATH3300/10	A	3281	11,8	33
	B	3301	11,3	30
	C	3316	13,5	23
	D	3330	15,9	26
	E	3333	20,3	28

Rezultati življenjske dobe (10V, 125°C) istih kondenzatorjev so naslednji:

ELKO	DEL	-dC(%) 500 ur	tan(%) 500 ur	-dC(%) 1000 ur	tan(%) 1000 ur
ATH3300/10	A	4,2	13,1	5,2	13,4
	B	2,3	12,8	3,3	13,5
	C	2,1	15,1	3,0	16,0
	D	5,4	21,4	6,6	23,6
	E	4,2	22,8	5,3	25,0
kriterij		-	-	15,0	33,8

-dC - sprememba kapacitivnosti po določeni življenjski dobi

Kot je razvidno iz rezultatov življenjske dobe ELKO ATH 3300μF/10V so vsi ELKO uspešno prestali 1000 urno življenjsko dobo, so pa precejšnje razlike v naraščanju tangens delta med življenjsko dobo: medtem ko se je tan delta ELKO, impregniranih v elektrolite A, B, C le malo povišal, se je precej bolj poslabšal pri ELKO, impregniranih v elektrolita D in E. Njihovo naraščanje



Slika 3. ATH 3300 μF 10V

tangens delta se v nadaljevanju življenjske dobe upočasni, kar je razvidno iz slike št. 3.

Že začetni tangens delta je bil precej višji pri ELKO z elektrolitoma D in E.

3.2. Anodne folije

Drugi najvažnejši sestavni del elektrolitskega kondenzatorja je anodna folija. Specializirani proizvajalci anodnih folij imajo že zelo širok izbor folij, naša naloga je izbrati za naš delovni elektrolit najustreznejšo.

Poleg izbire primernega tipa folije je zelo pomembno določiti ustrezno formirno napetost anodne folije za posamezen tip ELKO. Formirna napetost folije je tista napetost, do katere je bila le ta elektro-kemično obdelana pri proizvajalcu folij. Znano je, da se za ELKO, ki so primerni za uporabo v temperaturnem območju od -40°C do +85°C uporabljajo anodne folije z 1,3 krat večjo formirno napetostjo kot je nazivna napetost. Višja ko je temperatura uporabe ELKO, višja formirna napetost anodne folije je potrebna za isto nazivno napetost. Naši preizkusi so pokazali, da je za ELKO, ki se lahko uporabljajo pri +125°C, optimalno vzeti manj jedkano folijo in za eno kategorijo višjo formirno napetost kot za ELKO z možnostjo uporabe do +85°C. Druga možnost je uporabiti zelo jedkano folijo in za dve kategoriji višjo formirno napetost. Če ponazorimo s primerom: za ELKO RTH 330μF/10V lahko uporabimo folijo 2303/22V, katere specifična kapacitivnost je 40μF/cm^2 ali folijo 983/33V, katere specifična kapacitivnost je ravno tako 40μF/cm^2. Pri končni izbiri med eno in drugo folijo odloča cena, dimenzija ELKO in pa tudi možnost optimalne organizacije dela v tovarni.

V naslednji tabeli so zbrani rezultati življenjske dobe ELKO RTH 220μF/25V (25V, +125°C) v odvisnosti od vrste uporabljene anodne folije:

anoda	tan0(%)	-dC1(%)	tan1(%)	-dG1(%)
983/65V	6,5	12	13	16
1393/50V	6,9	11	8	16
983/50V	8,2	14	22	20
kriteriji	14	15	18,2	25

Specifične kapacitivnosti: 983/65V - 15 $\mu F/cm^2$
1393/50V - 14,8 $\mu F/cm^2$
983/50V - 22 $\mu F/cm^2$

tan0 - začetni tangens delta

tan1, -dC1 - tangens delta in sprememba kapacitivnosti po 1000 urah življenjske dobe

-dG1 - izguba teže elektrolita po 1000 urah življenjske dobe

Iz tabele je razvidno, da je posledica višje formirne napetosti anodne folije manjša sprememba kapacitivnosti in tangens delta ELKO tekom življenjske dobe. Jasno je razviden tudi enak vpliv manjše jedkanosti (manjše specifične kapacitivnosti) anodne folije.

V naslednji tabeli je prikazan vpliv anodne folije na življenjsko dobo visokovoltnih ELKO:

ELKO	anoda	tan0(%)	-dC1(%)	tan1(%)
RTH 10/350	991/520	4,7	5,9	5,2
RTH 10/250	991/520	4,7	5,0	4,9
RTH 10/250	991/385	5,6	15	10
kriteriji		10	10	13

Iz tabele je razvidno, da je potrebna določena minimalna formirna napetost za določeno nazivno napetost in zahtevano življenjsko dobo ELKO. Če je izbrana formirna napetost prenizka, se to najbolj izrazito odraža na prehitrem padcu kapacitivnosti. Če pa je formirna napetost nad optimalno, to bistveno ne podaljša življenjske dobe ELKO.

3.3. ELKO papir

Vsi visokotemperaturni nizkovoltni elektroliti, ki so se na naših preizkusih pokazali kot zadovoljivi in so ekološko sprejemljivi, vsebujejo kot topilo gama-butirolakton. Primerjalne začetne meritve ESR, tangens delta in impedance ELKO, impregniranih v glikolne elektrolite in tiste, ki vsebujejo kot topilo gama-butirolakton pa kažejo, da dobimo ob enaki upornosti obeh elektrolitov slabše rezultate pri gama-butirolaktonskih elektrolitih. Rešitev teh problemov so našli v japonski firmi NKK, kjer so razvili posebno vrsto papirja za gama-butirolaktonske elektrolite. V naslednji tabeli prikazujemo vpliv vrste uporabljenega papirja na začetne parametre ELKO. Ta vpliv je prikazan na primeru dveh elektrolitov, D in B, oba vsebujeta topilo gama-butirolakton.

ELKO	DEL	papir	tan(%) 100Hz	ESR (ohm) 100Hz	Z(ohm) 10KHz
RTH 3300/10V	D	NKK	7,0	0,038	0,033
		cel	11,5	0,063	0,052
RTH 3300/10V	B	NKK	5,2	0,028	0,024
		cel	7,5	0,042	0,035

NKK - poseben papir firme NKK, iz manile in sličnih vlaken

cel - običajno uporabljan celulozni papir

3.4. Inkapsulacija

Za zapiranje ELKO smo uporabili gumijasti čep. Preizkušali smo različne vrste gum od različnih proizvajalcev. Za preizkus smo izbrali naslednje gume: EPDM, butilna, mešanica EPDM in butila. Difuzijo sestavin elektrolita skozi čep smo zasledovali s tehtanjem ELKO in merjenjem njihovih parametrov med življenjsko dobo. S tehtanjem ELKO smo ugotavljali izgubo elektrolita. Tudi mi smo lahko potrdili že znano izkustveno pravilo, da se pri izgubi elektrolita za približno 25% ELKO že toliko izsuši, da njegovi parametri ne zadoščajo več postavljenim zahtevam.

V naslednji tabeli je prikazana razlika v difuziji sestavin elektrolita skozi čepe iz različnih materialov med breznapetostno življenjsko dobo.

ELKO	guma	dimenzija	izguba teže elektrolita (%)		
			500 ur	1000 ur	1500 ur
RTH 220/25V	E	10x21	16	39	50
	M		8	20	27
	B		4	11	14

E - EPDM guma

M - mešanica EPDM in butilne gume

Kot je razvidno iz gornje tabele, je difuzija elektrolita skozi butilno gumo najmanjša. Naši nadaljnji preizkusi so nam potrdili dejstvo, da je izparevanje elektrolita tudi

funkcija dimenzij čepka in kondenzatorja, kvalitete montaže ELKO in sestavin elektrolita.

3.5. Superponiran izmenični tok

Dovoljeno obremenljivost ELKO s superponiranim izmeničnim tokom smo deloma izmerili, deloma pa izračunali. V Iskrinem katalogu so podani za RTH in ATH ELKO tisti superponirani izmenični tokovi, ki segrejejo površino ELKO za 1°C pri temperaturi okolice +125°C.

Pri izračunu dovoljenega superponiranega izmeničnega toka (Irc) in njegove frekvenčne odvisnosti smo uporabili naslednjo formulo:

$$Irc = \frac{dT \cdot 2\pi v \cdot C \cdot K \cdot F}{\tan delta}$$

dT - temperaturna razlika med jedrom ELKO in okolice (°C)

v - frekvenca (Hz)

C - kapacitivnost ELKO (F)

F - površina ELKO (cm^2)

K - faktor

tan delta - izgubni kot (-)

3.6. Preizkusi življenjske dobe

Preizkus življenjske dobe ELKO je končni preizkus vseh sestavnih delov. Življenjsko dobo ELKO preizkušamo na maksimalni temperaturi, za katero je določen kondenzator narejen. Ločimo dva preizkusa in sicer preizkus pod obremenitvijo z nazivno enosmerno napetostjo in brez napetosti. Prvi preizkus je pomemben za delovanje ELKO, drugi pa za skladiščenje in mirovanje ELKO.

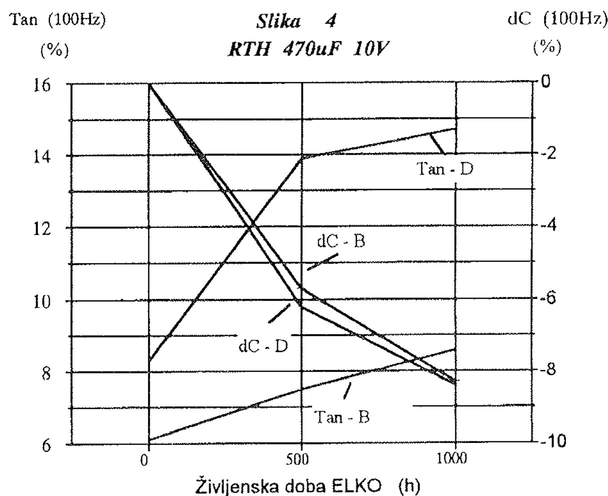
4. REZULTATI

1. Določili smo 6 elektrolitov (5 za nizkovoltno in 1 za visokovoltno območje), ki so primerni za impregnacijo 125°C-ELKO. Glavna razlika med ELKO, ki so impregnirani v navedene nizkovoltne elektrolite, je vidna v začetnem tan delta, impedanci in ESR ter spremembi teh parametrov med življenjsko dobo. Slika 4 prikazuje razliko v tangens delta in poteku življenjske dobe med ELKO z elektrolitoma B in D.

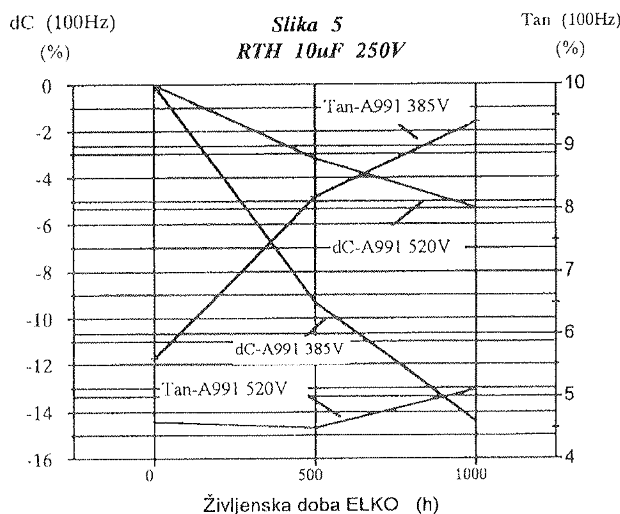
2. Določili smo optimalno vrsto anodne Iz folije in njeno optimalno formirno napetost za vsako posamezno nazivno napetost ELKO. Razlika v tangens delta in poteku življenjske dobe je prikazana v sliki 5.

3. Določili smo optimalno vrsto in množino papirja za vsako nazivno napetost posebej. Največji vpliv papirja je viden pri najnižji nazivni napetosti. V sliki 6 je prikazana odvisnost vpliva vrste papirja na začetni tan delta in na potek življenjske dobe.

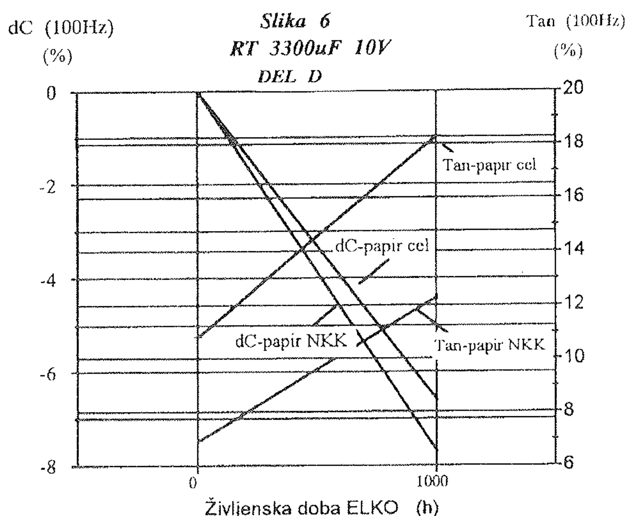
4. Primerjali smo dolžino življenjske dobe v odvisnosti od izvedbe ELKO. Ugotovili smo, da je ob veliki tehno-



Slika 4. RTH 470 μF 10V



Slika 5. RTH 10 μF 250 V



Slika 6. RT 3300 μF 10 V DEL D

loški in proizvodni disciplini možno napraviti radialni kondenzator z enako dolgo življenjsko dobo kot aksialnega. Problem izgube elektrolita med življenjsko dobo je lažje obvladljiv pri aksialni izvedbi kondenzatorja.

Dolžina življenjske dobe je zelo odvisna od konstrukcije ELKO, od uporabljene gume za čepek kondenzatorja in od kvalitete montaže.

5. Razvili smo kvalitetne visokotemperaturne ELKO: RTH in ATH, katerih temperaturno območje uporabe je od -40°C do +125°C, napetostno območje je od 10V do 350V, minimalna življenjska doba je 1000 ur, parametri po tej življenjski dobi ustrezajo standardu IEC 384-4 LL. Kvaliteta razvitih kondenzatorjev ustreza zahtevam v avtomobilski in vojaški elektroniki ter povsod tam, kjer so pri sicer nižji temperaturi okolice prisotni veliki superponirani izmenični tokovi (SMPS naprave).

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POLARIMETRIČNI TEMPERATURNI SENZOR: analiza polarizacijskega ločitvenega razmerja in dolžine senzorskega dela

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Ključne besede: fizika, optika, merjenje temperature, senzorji temperaturni polarimetrični, senzorji optični dvolomni, komponente polarizacijske, vodenje procesov industrijskih, senzorji z vlakni optičnimi, ER razmerje polarizacijsko ločitveno

Povzetek: Analizirali smo vpliv polarizacijskega ločitvenega razmerja vhodnega polarizatorja, koherenčnih lastnosti svetlobnega vira in dolžine senzorskega in dovodnega vlakna na polarimetrične meritve temperature. Iz rezultatov je razvidno, da je možno z uporabo polarizatorjev z nizkim polarizacijskim ločitvenim razmerjem in minimalno dolžino visoko dvolomnega optičnega vlakna ter nizko koherentnim virom svetlobe realizirati cenen polarimetrični termometer z omejeno občutljivostjo. Izveden je bil temperaturni polarimetrični senzor za absolutne meritve temperature, ki deluje v področju od 40°C do 60°C.

Polarimetric temperature sensor: extinction ratio and sensing length examination

Keywords: physics, optics, temperature measurements, polarimetric temperature sensors, birefringent fiber sensors, polarizing fiber sensors, polarizing components, industrial process control, optical fiber sensors, ER, extinction ratio

Abstract: Temperature is one of the most important parameters to be measured in industrial process control. The primary reason for interest in industrial fiber optic temperature sensors is their electromagnetic immunity and electrical passivity. This enables the use of fiber optic sensors in electromagnetically hostile and hazardous environments. During the last decade, many intrinsic optical fiber temperature sensors have been proposed using the Michelson or Mach-Zehnder configuration. However, those interferometers suffer low selectivity and require a well isolated and undisturbed reference arm that is very hard to produce. An alternative to the classic interferometry is a polarimetric sensor which uses the interference of two polarization eigenmodes in high birefringence fibers.
We theoretically and experimentally investigated the influences of the sensing and lead fiber length, the extinction ratio of the input polarizer and the coherence properties of the light source for polarimetric temperature measurements. We have shown that there is a possibility to construct a relatively simple and inexpensive fiber optic polarimetric thermometer for absolute temperature measurements by using a low ER polarizer and a low coherent source.
The proposed polarimeter does not exhibit high sensitivity However, it is easy to achieve a large unambiguous range with a resolution below 0.1°C, which satisfies most demands in many industrial and medical applications.

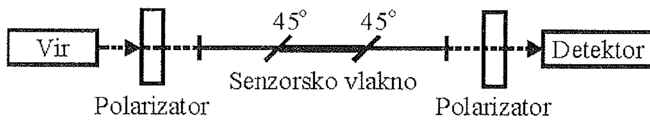
1 Uvod

Temperatura je ena izmed najpomembnejših merilnih veličin v procesni industriji. Poglavitni razlog, zaradi katerega nas zanimajo temperaturni senzorji, izvedeni z uporabo optičnih vlaken, je njihova elektromagnetna imunost in električna pasivnost. Optične vlakenske senzorje je mogoče uporabljati v elektromagnetno onesnaženih in eksplozivnih okoljih. V zadnjem desetletju se je pojavilo veliko število optičnih vlakenskih senzorjev z notranjim delovanjem, ki temeljijo na Michelsonovi ali Mach-Zehnderjevi konfiguraciji /1/. Problem omenjenih interferometrov je njihova nizka selektivnost, ki zahteva dobro izolirano in neobremenjeno referenčno vejo, kar je praktično zelo težko izvesti. Alternativo h klasičnim interferometrom ponujajo polarimetrični senzorji, pri katerih med sabo interferirata lastna polarizacijska rodova, ki se razširjata znotraj vlakna z ohranjanjem polarizacije /2,3,4,5/. Polarimetrični senzorji, ki temeljijo na pojavu dvolomnosti, so v splošnem preprostejši od tradicionalnih enorodovnih interferometričnih senzorjev. Kljub temu ostaja potreba po dokaj zahtevnem procesiranju signalov in uporabi dragih polarizacijskih komponent. Dodatna slabost interferomatričnih senzorjev je določitev absolutne temperature, saj je izhod iz interferometra periodična funkcija. Za rešitev tega problema so bile predlagane mnoge rešitve, kot npr. dvovalovna interferometrija ali interferometrija z uporabo "bele svetlobe" /6/, ki pa povečajo zahtevnost senzorja in s tem tudi ceno ter tako zmanjšajo področja uporabe. .

V mnogih industrijskih in biomedicinskih aplikacijah, kjer je podana zahteva po elektromagnetni imunosti in električni pasivnosti, je ponavadi zadostna temperaturna občutljivost 0.1 °C. V prispevku smo teoretično in eksperimentalno preverili vplive polarizacijskega ločitvenega razmerja vhodnega polarizatorja, koherenčnih lastnosti svetlobnega vira ter dolžine senzorskega in dovodnega vlakna na merilno območje in delovanje polarimetričnega termometra.

2 Teorija in simulacije

Sestava polarimetričnega senzorja z uporabo visoko dvolomnih optičnih vlaken je prikazana na sliki1. Senzorsko vlakno je z dovodnim in odvodnim vlaknom povezano z zlitimi spoji, tako da je kot med lastnimi osmi vlaken 45°.



Slika 1: Sestava polarimetričnega senzorja

2.1 Merjenje temperature

V visoko dvolomnem vlaknu se polarizacijska rodova LP_{01x} in LP_{01y} razširjata s fazno hitrostjo, ki je določena z lomnima količnikoma n_x in n_y. Razlika lomnih količnikov $\Delta n = n_x - n_y$ je določena z dvolomno dolžino $L_B = \lambda/\Delta n$. V primeru visoko dvolomnih vlaken z notranjimi stresnimi elementi (dvolomnost, ki je posledica stresnih elementov, je temperaturno odvisna) je temperaturna občutljivost podana s sledečim izrazom /4/:

$$\frac{1}{L_{senzor}}\frac{d(\Delta\phi)}{dT} = \frac{k}{L_{senzor}}\left[\frac{\Delta n}{n}\frac{dn}{dT} + \Delta n\frac{dL}{dT}\right] \quad (1)$$

pri tem je $\Delta\phi$ fazna zakasnitev, $k=2\pi/\lambda$ valovni vektor, L_{senzor} dolžina senzorskega vlakna in T merjena temperatura. Ker se dolžina senzorskega vlakna v primeru polarimetričnega senzorja spremeni enako za oba polarizacijska rodova, lahko drugi člen v enačbi (1) zanemarimo in (1) dobi obliko:

$$\frac{1}{L_{senzor}}\frac{d(\Delta\phi)}{dT} = \frac{k}{L_{senzor}}\left[\frac{\Delta n}{n}\frac{dn}{dT}\right] \quad (2)$$

2.2 Vpliv polarizacijskega ločitvenega razmerja, dovodnega vlakna in koherenčnih lastnosti vira

Da bi preverili vpliv dolžine dovodnega vlakna in koherenčnih lastnosti vira svetlobe, si oglejmo dva idealna primera: prvič, roda LP_{01x} in LP_{01y} sta na koncu dovodnega vlakna koherentna ter govorimo o koherentnem primeru in dugič, roda LP_{01x} in LP_{01y} na koncu dovodnega vlakna nista koherentna. V slednjem imamo opraviti z nekoherentnim primerom.

1. Koherentni primer

Za raziskavo vpliva polarizacijskih ločitvenih lastnosti vhodnega polarizatorja in dolžine senzorskega vlakna na polarimetrični termometer predpostavimo, da je polarizator glede na os dovodnega vlakna zasukan za kot θ. Izhodni polarizator (analizator) obravnavamo kot idealen polarizator.

Z uporabo Jonesove matrične notacije lahko zapišemo sledečo enačbo za polarimetrični termometer:

$$E_{izhod} = P_{izhod}\cdot T_{dovod}\cdot T_{45}\cdot T_{senzor}\cdot T_{45}\cdot T_{odvod}\cdot P_{vhod}\cdot E_{vhod}$$
$$I_{izhod} = \langle E_{izhod}E^{*}_{izhod}\rangle \quad (3)$$

kjer je E_{vhod} stolpični vektor vhodne električne poljske jakosti, P_{vhod} Jonesova matrika za vhodni polarizator, ki je glede na hitro os dovodnega dvolomnega vlakna zasukan za kot θ. P_{izhod} je Jonesova matrika, ki opisuje izhodni polarizator, T_{dovod} in T_{odvod} predstavljata dovodno in odvodno vlakno, T_{45} je matrični zapis za 45° spoj in T_{senzor} predstavlja senzorski del vlakna. Matrike za posamezne člene v enačbi (2) lahko zapišemo kot:

$$E_{vhod} = \begin{bmatrix}1\\1\end{bmatrix} \quad (4)$$

$$P_{vhod} = \begin{bmatrix}\cos^2\theta & \sin\theta\cos\theta\\ \sin\theta\cos\theta & \sin^2\theta\end{bmatrix} \quad (5)$$

$$T_{dovod} = \begin{bmatrix}\exp(i\phi_{x_in}) & 0\\ 0 & \exp(i\phi_{y_in})\end{bmatrix} \quad (6)$$

$$T_{45} = \begin{bmatrix}1 & \pm1\\ \mp1 & 1\end{bmatrix} \quad (7)$$

$$T_{senzor} = \begin{bmatrix}\exp(i\phi_{x}) & 0\\ 0 & \exp(i\phi_{y})\end{bmatrix} \quad (8)$$

$$T_{odvod} = \begin{bmatrix}\exp(i\phi_{x_out}) & 0\\ 0 & \exp(i\phi_{y_out})\end{bmatrix} \quad (9)$$

$$P_{izhod} = \begin{bmatrix}0 & 0\\ 0 & 1\end{bmatrix} \quad (10)$$

Z uporabo enačb (2)-(10) lahko zapišemo izraz za izhodno gostoto svetlobnega toka polarimetričnega termometra:

$$I_{izhod} = I_0\left[\underbrace{\frac{1}{2}(A^2+B^2)+\frac{1}{2}(B^2-A^2)\cos\phi}_{\text{senzorsko vlakno}} - \underbrace{4AB\sin\phi\sin\phi_1}_{\text{motnja dovoda}}\right] \quad (11)$$

kjer je

$\phi = 2\pi/\lambda\ \Delta n L_{senzor}$

$\phi_1 = 2\pi/\lambda\ \Delta n L_{dovod}$

$A = \sin^2\theta + \cos\theta\sin\theta$

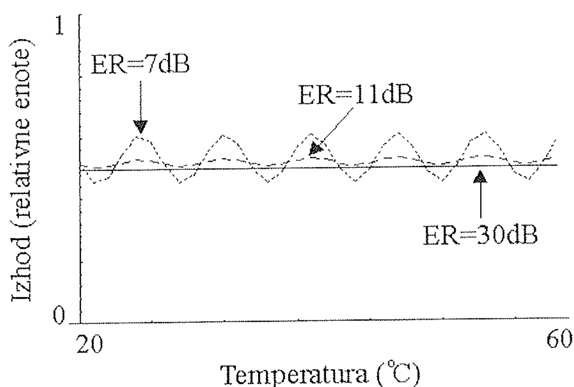
$B = \cos^2\theta + \cos\theta\sin\theta$

Izraz je v splošnem odvisen od vstopnih pogojev (kotni zamik θ in rezultirajoče polarizacijsko ločitveno razmerje vhodnega polarizatorja), dolžine senzorskega

vlakna L_{senzor} in dolžine dovodnega vlakna L_{dovod} v primeru neidealnega vzbujanja s polarizirano svetlobo. Polarizacijsko ločitveno razmerje polarizirane svetlobe v dovodnem visoko dvolomnem vlaknu je določeno z:

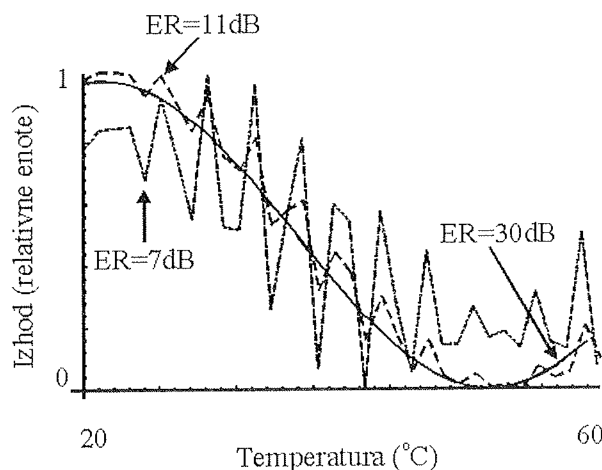
$$ER = 10\log\frac{\cos\theta}{\sin\theta} \qquad (12)$$

kjer je θ kotni zamik polarizatorja. Enačba (12) predstavlja gostoto svetlobnega toka na izhodu iz senzorskega sistema in je sestavljena iz dveh delov. Prvi del je odvisen samo od temperature senzorskega vlakna, medtem ko je drugi del odvisen od pogojev tako v senzorskem kot v dovodnem vlaknu (temperatura, vibracije, nateg, itd.). Zaradi tega lahko drug del obravnavamo kot motnjo dovoda, ki je odvisna od polarizacijskega ločitvenega razmerja ter je tako posledica neidealnih razmer vbujanja. Slika 2 prikazuje teoretično izračunan izhod iz polarimetra za konstantno temperaturo senzorskega dela in spremenljive pogoje v dovodnem vlaknu pri različnih polarizacijskih ločitvenih razmerjih. Slika 3 nadalje prikazuje teoretično dobljene



Slika 2: Teoretično izračunan izhod polarimetra v odvisnosti od temperature dovodnega vlakna za konstantno temperaturo senzorskega vlakna in spremenljiva polarizacijska ločitvena razmerja

izhodne karakteristike za primer, kadar hkrati spreminjamo temperaturo senzorskega in dovodnega vlakna pri različnih polarizacijskih ločitvenih razmerjih. Dovodno vlakno se obnaša kot dodatni senzorski element, s čimer se poveča merilna negotovost.

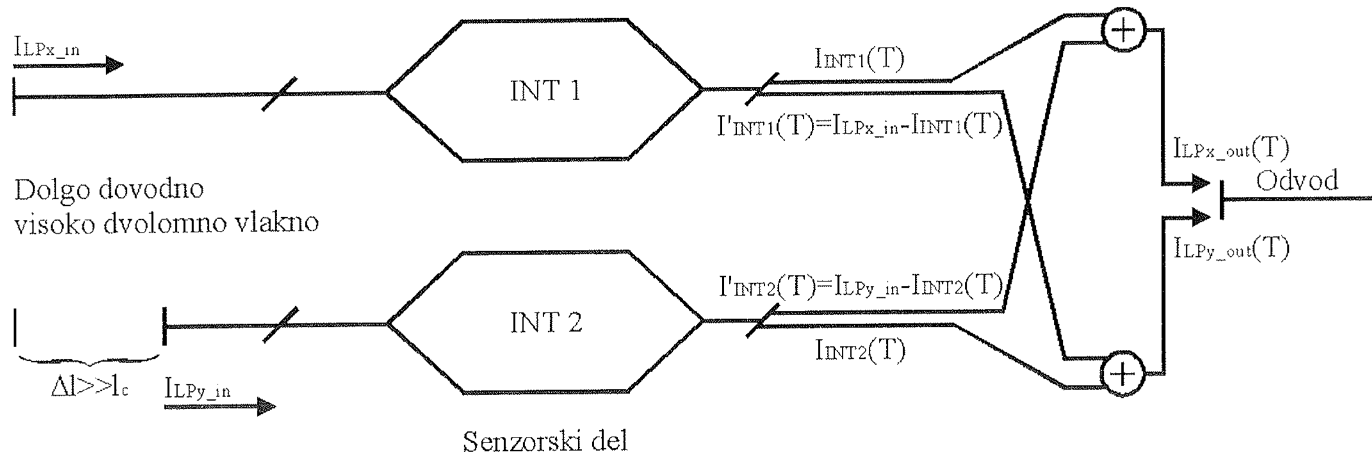


Slika 3: Teoretično določen izhod polarimetra za koherenten primer: hkratno spreminjanje temperature dovodnega in senzorskega vlakna za različna polarizacijska ločitvena razmerja vhodnega polarizatorja

2. Nekoherentni primer

Kadar polarizacijska rodova na koncu dovodnega vlakna nista koherentna, lahko interferometer razstavimo v dva idealna (neskončno polarizacijsko ločitveno razmerje) "vzajemno nekoherentna" interferometra, kot je prikazano na sliki 4.

Na prvem 45° spoju se zaradi obeh nekoherentnih rodov, ki se razširjata vzdolž dovodnega vlakna vzbudita oba polarizacijska rodova znotraj visoko dvolomnega senzorskega vlakna. Na drugem 45° spoju med seboj interferirata le tista rodova, ki sta bila koherentna



Slika 4: Model nekoherentnega polarimetra

na prvem spoju. Zaradi tega lahko merilni del predstavimo kot dva med seboj ločena interferometra. Optična moč, ki je sklopljena v vsakega od polarizacijsih rodov odvodnega vlakna, je tako vsota prispevkov posameznih interferometrov in jo lahko zapišemo kot:

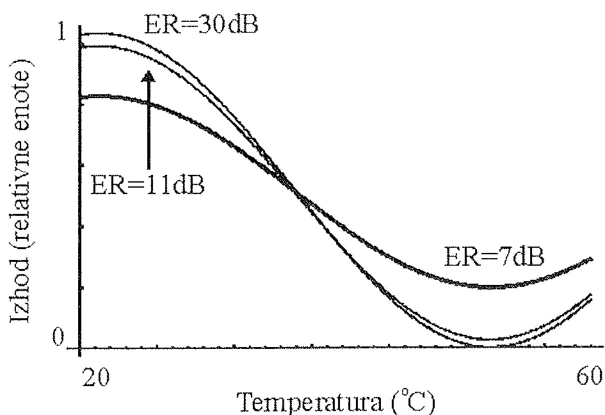
$$I_{LPx_izhod}(T) = I_{INT1}(T) + \left[I_{LPy_vhod} - I_{INT2}(T)\right]$$
$$I_{LPy_izhod}(T) = I_{INT2}(T) + \left[I_{LPx_vhod} - I_{INT1}(T)\right] \quad (14)$$

kjer sta $I_{LPx_izhod}(T)$ In $I_{LPy_izhod}(T)$ gostoti svetlobnega toka v glavnih oseh izhodnega vlakna. I_{INT1}, in I_{INT2} sta gostoti svetlobnega toka interference med polarizacijskima rodovoma v prvem in drugem razstavljenem interferometru. Njuna komplementarna izhoda sta enaka $I\check{Z}_{INT1}=I_{LPx_vhod}-I_{INT1}$ in $I\check{Z}_{INT2}=I_{LPy_vhod}-I_{INT2}$. I_{LPx_vhod} in I_{LPy_vhod} sta gostoti svetlobnega toka rodov vzdolž dovodnega vlakna.

Z uporabo enačb (14) in (12) lahko izhod iz polarimetra zapišemo kot:

$$I_{LPy_izhod} = I_{LPx_vhod} + \left(I_{LPy_vhod} - I_{LPx_vhod}\right)\left[\frac{1}{2} + \frac{1}{2}\cos\phi\right]$$
$$I_{LPx_izhod} = I_{LPy_vhod} + \left(I_{LPx_vhod} - I_{LPy_vhod}\right)\left[\frac{1}{2} + \frac{1}{2}\cos\phi\right] \quad (15)$$

Z uporabo izraza za izračun polarizacijskega ločitvenega razmerja ($ER=10\log(I_{Lpx_vhod}/I_{LPy_vhod})$ se enačba (15) preoblikuje v obliko:



Slika 5: Teoretično določen izhod polarimetra za nekoherenten primer: hkratno spreminjanje temperature dovodnega in senzorskega vlakna za različna polarizacijska ločitvena razmerja vhodnega polarizatorja

$$I_{LPy_izhod} = I_{LPy_vhod}\left[1 + \left(10^{-\frac{ER}{10}} - 1\right)\left[\frac{1}{2} + \frac{1}{2}\cos\phi\right]\right] \quad (16)$$
$$I_{LPx_izhod} = I_{LPx_vhod}\left[10^{-\frac{ER}{10}} + \left(1 - 10^{-\frac{ER}{10}}\right)\left[\frac{1}{2} + \frac{1}{2}\cos\phi\right]\right]$$

Iz enačbe (16) je razvidno, da je izhod polarimetra neodvisen od pogojev dovodnega vlakna, ne glede na polarizacijsko ločitveno razmerje. V primeru nekoherentnega delovanja vpliva zmanjšanje polarizacijskega ločitvenega razmerja vhodnega polarizatorja samo na vidljivost interferenčenega vzorca, ki se zmanjša (slika 5).

2.3 Teoretični zaključek

Ugotovimo lahko, da je za polarimetrični termometer potrebno uporabiti polarizator z velikim polarizacijskim ločitvenim razmerjem, ali pa zagotoviti, da postaneta vzbujena polarizacijska rodova v dovodnem vlaknu nekoherentna pred vstopom v senzorski del. To lahko dosežemo z uporabo dovolj dolgega kosa dovodnega vlakna. V simulacijah smo uporabljali idealen izhodni polarizator. Za odpravo vplivov odvodnega vlakna v primeru uporabe neidealnega izhodnega polarizatorja je potrebno upoštevati enake ukrepe kot za dovodno vlakno.

Minimalna dolžina dovodnega visoko dvolomnega vlakna, ki zagotavlja nekoherentnost med polarizacijskimi rodovi, je odvisna od koherenčnih lastnosti vira in jo lahko izrazimo s pomočjo koherenčne dolžine ℓ_c vira, dvolomne dolžine optičnega vlakna L_B in valovne dolžine vira λ:

$$L_{dovod} >> \frac{\ell_c \cdot L_B}{\lambda} \quad (17)$$

Dodatni pogoj, ki ga je potrebno izpolniti, je zadostna koherenčna dolžina vira, tako da polarizacijska rodova ne postaneta nekoherentna znotraj senzorskega dela:

$$\ell_c > \frac{\lambda \cdot L_{sensing}}{L_B} \quad (18)$$

Kadar uporabljamo polarizatorje z nizkim polarizacijskim ločitvenim razmerjem je potrebno izpolniti pogoja (17) in (18).

3 Eksperimentalni rezultati

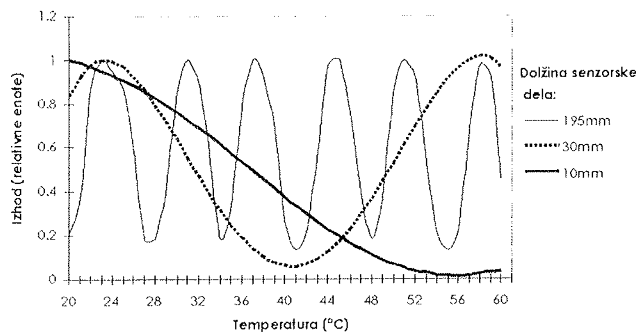
Da bi lahko izpolnili naš osnovni cilj, t.j. realizirati cenovno ugoden absolutni temperaturni polarimetrični senzor, je potrebno minimizirati število optičnih komponent. Realizacija tako zajema uporabo kratkih senzorskih vlaken, ki zagotavljajo neperiodičen izhodni signal in uporabo polarizatorjev z nizkim polarizacijskim ločitvenim razmerjem ali pravilnim sklopom med laser-

sko diodo in vlaknom z ohranjanjem polarizacije (zadostna polarizacijska ločitvena razmerja lahko dosežemo že s pravilnim sklapljanjem laserske diode in visoko dvolomnega vlakna). Kot primer smo realizirali polarimetrični merilnik temperature, ki omogoča absolutne meritve temperature v območju od 20°C do 60°C.

3.1 Absolutna meritev temperature

V splošnem je izhod polarimetra kosinusna funkcija z zelo majhnim področjem nedvoumnosti. Za dosego večjega področja nedvoumnosti in absolutnega načina merjenja z minimalnim procesiranjem signalov smo postopoma zmanjševali dolžino senzorskega visoko dvolomnega vlakna. Vsi eksperimentalni rezultati so bili doseženi z uporabo Fibercorovega visoko dvolomnega vlakna HB800, ki ima visoko stopnjo lastne dvolomnosti (L_B=0.8mm). Senzorsko vlakno je bilo z dovodnim in odvodnim spojeno s 45° zlitimi spoji. Eksperimentalni interferogrami za tri različne dolžine vlaken so prikazani na sliki 6. Iz interferogramov in enačbe (2) lahko določimo temperaturno občutljivost:

$$\frac{1}{L_{senzor}}\frac{d(\Delta\phi)}{dT} = 5{,}63\,\mathrm{radK^{-1}m^{-1}}$$

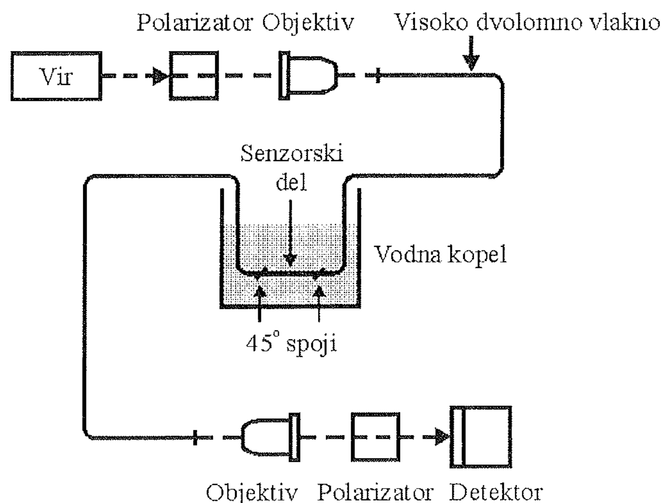


Slika 6: Eksperimentalni interferogrami za različne dolžine senzorskega vlakna

Iz rezulatov je razvidno, da povzroči dolžina senzorja približno 10 mm fazno zakasnitev $\pi/2$ preko celotnega merilnega področja (20°C do 60°C). Omenjen način zaznavanja izhodnega signala označimo kot kvadraturno detekcijo. V primerjavi z meritvami, kjer uporabimo daljše kose merilnega vlakna, smo zmanjšali občutljivost, razmerje med področjem merilne nedvoumnosti in ločljivosti pa je ostalo nespremenjeno.

3.2 Polarizacijsko ločitveno razmerje in dovodni šum

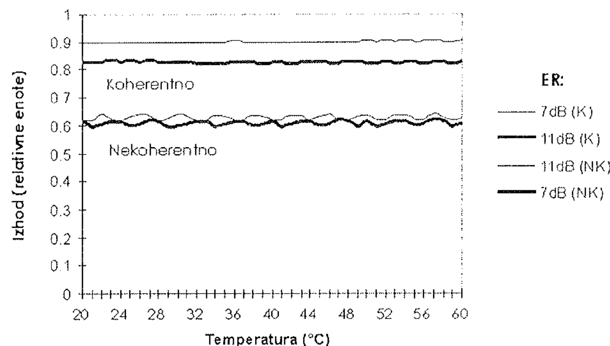
Eksperimentalno preverjanje vplivov polarizacijskega ločitvenega razmerja in dovodnega šuma je bilo izvedeno z uporabo sestava, ki je prikazan na sliki 7 (10mm senzorsko vlakno). V koherentnem primeru smo uporabljali lasersko diodo z valovno dolžino 850nm in koherenčno dolžino približno 1mm ($\Delta\lambda$=0.7nm) ter dovodno vlakno dolžine 1m. Za nekoherentni primer smo dolžino dovodnega vlakna povečali na 35m. Za različne kotne zamike vhodnega polarizatorja smo spreminjali temperaturo vodne kopeli od 20°C na 60°C ter pri tem opazovali izhod iz senzorja.



Slika 7: Eksperimentalni sestav polarimetričnega termometra

Slika 8 prikazuje tipičen izhod iz merilnega sistema, ko spreminjamo temperaturo približno 1m dovodnega vlakna, temperatura senzorskega vlakna pa ostaja nespremenjena. Na sliki sta prikazana tako koherentni in nekoherentni primer. Kadar uporabljamo polarizatorje z nizkim polarizacijskim ločitvenim razmerjem, opazimo v koherentnem primeru močan vpliv dovodnih vlaken na izhodno gostoto svetlobnega toka. V nekoherentnem primeru ostaja izhod iz senzorja nespremenjen tudi ob uporabi polarizatorjev z nizkim polarizacijskim ločitvenim razmerjem.

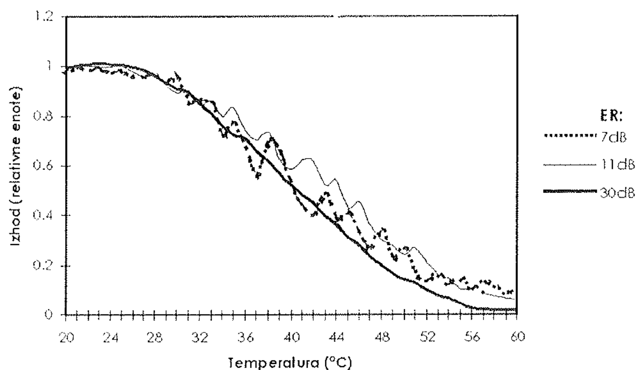
Sliki 9 in 10 prikazujeta temperaturno odvisnost izhodne gostote svetlobnega toka za koherentni in nekoherentni primer, kadar hkrati spreminjamo temperaturo dovodnega in senzorskega vlakna. V koherentnem primeru



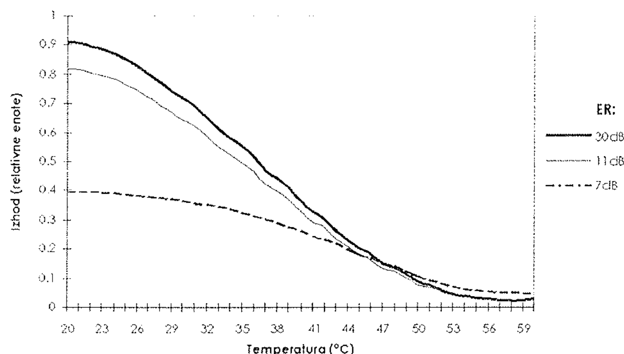
Slika 8: Eksperimentalno dobljen izhod polarimetra za konstantno temperaturo senzorskega vlakna in spremenljivo temperaturo dovodnega vlakna, pri različnih polarizacijskih ločitvenih razmerjih vhodnega polarizatorja

dobimo zelo šumen (kvazi periodičen) signal, še posebej, kadar uporabimo polarizatorje z nizkim polarizacijskim ločitvenim razmerjem. Zaradi tega koherentni primer ni uporaben za zastavljen način temperaturnega merjenja. V nekoherentnem primeru prikazanem na sliki 10 dobimo gladek in dobro definiran izhod preko celotnega merilnega področja. Za nižja polarizacijska ločitvena razmerja se zmanjša le vidljivost interferenčnega vzorca. Tudi v primeru izredno slabih polarizacijskih ločitvenih razmerij, okoli 7dB, dobimo še vedno uporabne rezultate. Kadar potrebujemo daljinsko delovanje senzorja, ga lahko povežemo s standardnimi telekomunikacijskimi vlakni. Pozornost pri sestavi je potrebno posvetiti predvsem zadostnemu delu visoko dvolomnega vlakna med polarizatorjem in senzorskim vlaknom, s katerim omogočimo nekoherentno delovanje.

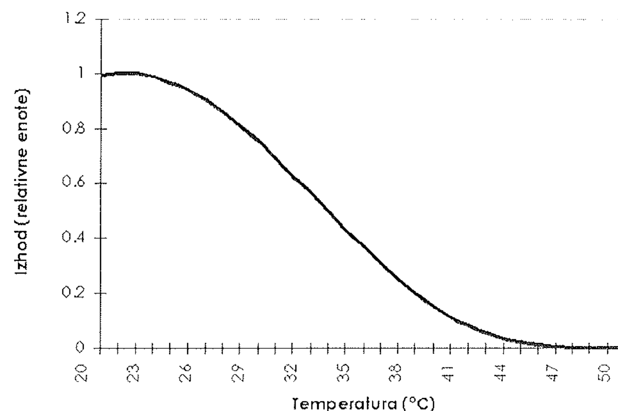
Na koncu smo delovanje preverili tudi z uporabo nekoherentnega vira svetlobe. V našem primeru je bila to svetleča dioda s koherenčno dolžino 5.7μm ($\Delta\lambda$=125nm). Da lahko polarizacijska rodova interferirata na koncu senzorskega vlakna, je bilo potrebno v primeru uporabe svetleče diode senzorsko vlakno skrajšati na 4mm. Dobljeni rezultat je prikazan na sliki 11. Tudi kadar uporabljamo frekvenčno širikopasoven vir, dobimo dobro vidljivost interferenčnega vzorca.



Slika 9: Eksperimentalno določen izhod polarimetra za koherenten primer: hkratno spreminjanje temperature dovodnega in senzorskega vlakna za različna polarizacijska ločitvena razmerja vhodnega polarizatorja



Slika 10: Eksperimentalno določen izhod polarimetra za nekoherenten primer: hkratno spreminjanje temperature dovodnega in senzorskega vlakna za različna polarizacijska ločitvena razmerja vhodnega polarizatorja



Slika 11: Eksperimentalno dobljena temperaturna odvisnost polarimetra ob uporabi svetleče diode

Dobljeni eksperimentalni rezultati se ujemajo s teoretičnimi napovedmi, ki smo jih podali v drugem razdelku.

4 Zaključek

Teoretično in eksperimentalno smo raziskali vpliv dolžine senzorskega in dovodnega vlakna, polarizacijskega ločitvenega razmerja vhodnega polarizatorja in koherenčnih lastnosti vira svetlobe. Pokazali smo, da lahko z uporabo polarizatorjev z nizkim polarizacijskim ločitvenim razmerjem in nizko koherenčnih virov sestavimo enostaven in cenen polarimetrični termometer za merjenje absolutnih temperatur.

Predstavljen polarimeter ne dosega izredno visokih občutljivosti, zato pa je mogoče v širokem področju nedvoumnosti doseči ločljivosti pod 0.1 °C, kar po navadi zadošča za večino industrijskih in medicinskih aplikacij.

Zahvala

Za vse koristne predloge in diskusije bi se radi zahvalili Dr. Kenny Weirju in Prof. Brian Culshawu.

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IZVEDBA NEREKURZIVNEGA DIGITALNEGA SITA S PROGRAMIRLJIVIM POLJEM LOGIČNIH VEZIJ V STRUKTURI PORAZDELJENE ARITMETIKE

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Ključne besede: FIR filtri digitalni s trajanjem omejenim odziva impulznega, FIR sita digitalna nerekurzivna, DSP procesiranje signalov digitalno, aritmetika porazdeljena, izvedbe praktične, FPGA vezja logična s poljem programirljivim, LCA vezja logična polj celičnih

Povzetek: V članku je opisana izvedba uniziverzalne strukture nerekurzivnega digitalnega sita s 15 koeficienti v porazdeljeni aritmetiki z LCA vezji firme Xilinx. Pri tem smo uporabili takšno strukturo, ki omogoča izračun izhodnega signala po klasičnem in po modificiranem postopku porazdeljene aritmetike. Z opisano aparaturno opremo smo pri izbranem nizkoprepustnem situ dosegli slabljenje 30 dB in frekvenco vzorčenja 333 kHz. Meritev amplitudnih frekvenčnih odzivov sita smo opravili z digitalnim generatorjem belega šuma na vhodu sita. Modificirana oblika porazdeljene aritmetike zagotavlja povečanje dinamičnega območja izhodnega signala.

The FIR Digital Filter Realization with the Field Programmable Gate Array in Distributed Arithmetic Structure

Keywords: FIR digital filters, finite-impulse response digital filters, DSP, digital signal processing, distributed arithmetic, practical implementations, FPGA, field programmable gate arrays, LCA circuits, logical cell arrays

Abstract: In this article the hardware realization of 15 tap general FIR digital filter in the distributed arithmetic structure with field programmable gate arrays is presented.
This hardware structure is suitable for the implementation of digital filters with arbitrary frequency response. The comparison between standard and modified distributed arithmetic structure is also presented and the increase of the dynamic range of the output signal for 6 dB with modified distributed arithmetic structure is shown. Digital filter consist of 12 bit analog to digital and 12 bit digital to analog converters, two Xilinx LCA circuits XC 3042 and 32k x16 bit EPROM capacity with access time of 100 ns. The response of implemented low pass filter with pass band frequency $f_p = 0.1 f_s$ and stop band frequency $f_s = 0.2 f_s$ is obtained as frequency sweep method and for comparison with FFT of the output signal when filter is exited with digital white noise signal in input.
In this complexity the attenuation of 30 dB and sample frequency f_s of 333 kHz is obtained. Because of 19 bit complexity of the arithmetic unit the quantization error of the output signal is less than 10^{-3}.

1. Uvod

Nerekurzivna digitalna sita so zaradi linearnega faznega odziva zelo zanimiva za področje digitalne obdelave signalov.

Pri aparaturni izvedbi digitalnih sit je pomembna izbira izvedbene oblike. Osnovni kriteriji, ki vplivajo na izbiro so: dobro ujemanje med izračunanimi in izmerjenimi rezultati, majhna aparaturna kompleksnost in velika hitrost delovanja.

Struktura, ki temelji na porazdeljeni aritmetiki in ROM pomnilniku, v katerem so zapisane vnaprej izračunane delne vsote koeficientov, se je pokazala primerna tudi pri aparaturnih izvedbah digitalnih sit /1/. Za izvedbe, ki smo jih doslej naredili s standardnimi integriranimi komponentami /2/, bomo odslej uporabili programirljiva polja logičnih vezij (FPGA, LCA vezja). Merilne rezultate amplitudnega in faznega odziva sita smo dobili s klasično merilno metodo in z uporabo hitre Fourierjeve transformacije izhodnega signala pri vzbujanju sita z belim šumom. Za ta namen smo uporabili lastni digitalni generator belega šuma /3/. Vhodne in izhodne vrednosti signalov pa smo zajemali z logičnim analizatorjem.

2. Nerekurzivno digitalno sito v strukturi porazdeljene aritmetike

S porazdeljeno aritmetiko je označen postopek izračuna skalarnega produkta dveh vektorjev na elementarnem bitnem nivoju brez uporabe običajnih množilnikov.

2.1. Klasična oblika porazdeljene aritmetike

Nerekurzivno digitalno sito je običajno podano s splošno konvolucijsko enačbo

$$y(k) = \sum_{n=0}^{N} h(n) \cdot x(k-n) \qquad (1)$$

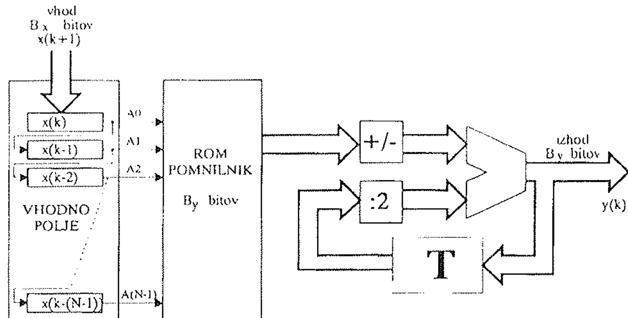
ki določa zvezo med vhodom *x(k)* in izhodom *y(k)*, pri tem *so s h(n)* označeni koeficienti impulznega odziva. Z upoštevanjem digitalne predstavitve vhodnega signala z B_x bitno besedo v dvojiški obliki, dobimo po krajši izpeljavi enostavnejši zapis določitve izhodne vrednosti y(k)

$$y(k) = \sum_{i=1}^{B_x-1} v_i(k) \cdot 2^{-i} - v_0(k) \qquad (2)$$

Pri tem so z v_i označene delne vsote koeficientov, ki jih izračunamo po enačbi

$$v_i(k) = \sum_{i=1}^{N-1} h(n) \cdot b_i(k-n) \qquad (3)$$

Pri uporabi konstantnih koeficientov digitalnega sita so $v_i(k)$ konstantne vrednosti in jih običajno zapišemo v pomnilnik vrste ROM. V (3) so z b_i označeni i-ti biti v vhodnem polju. Na sliki 1 je prikazana struktura nerekurzivnega digitalnega sita v klasični obliki porazdeljene aritmetike.



Slika 1: Struktura nerekurzivnega digitalnega sita v klasični obliki porazdeljene aritmetike

V tabeli 1 so za ilustracijo podane značilne delne vsote koeficientov za klasično obliko porazdeljene aritmetike.

Tabela 1: Značilne delne vsote koeficientov pri klasični obliki porazdeljene aritmetike

	naslovni vektor	delna vsota
0	0...000	0
1	0...001	h_0
2	0...010	h_1
3	0...011	h_0+h_1
4	0...100	h_2
.	.	.
.	.	.
2^{N-1}	1...111	$h_{N-1}+h_{N-2}+...h_0$

2.2. Nerekurzivno digitalno sito v strukturi modificirane oblike porazdeljene aritmetike

Pri dvojiškem zapisu vhodnega signala je v vhodnem polju z 1000...0 zapisana najmanjša (negativna) vrednost, z 0111...1 pa največja (pozitivna) binarna vrednost.

Modificirano obliko porazdeljene aritmetike dobimo, če pred vpisom v vhodno polje vhodni bipolarni signal pretvorimo v unipolarno obliko /4/. Tedaj izraz za izračun izhodnega signala v enačbi (2) preide v

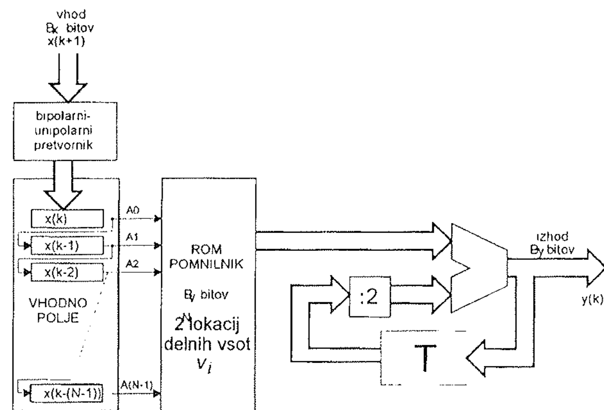
$$y(k) = y_m(k) = \sum_{i=0}^{B_x-1} v_{im}(k) \cdot 2^{-i} \qquad (4)$$

pri čemer so z $v_{im}(k)$ označene modificirane vrednosti delnih vsot koeficientov.

Zaradi spremenjene vrednosti vhodnega signala je potrebno v vhodnem polju delne vsote koeficientov simetrirati in normirati. Postopek simetriranja je odvisen od vrste frekvenčne karakteristike in ga izvedemo za vsako sito posebej. Značilne modificirane delne vsote koeficientov $v_{mi}(k)$ so prikazane v tabeli 2.

Tabela 2: Značilne delne vsote koeficientov pri modificirani obliki porazdeljene aritmetike

	naslovni vektor	modificirana delna vsota
0	0...000	$1/2(-h_0-h_1-h_2...-h_{N-1})$
1	0...001	$1/2(+h_0-h_1-h_2...-h_{N-1})$
2	0...010	$1/2(-h_0+h_1-h_2...-h_{N-1})$
3	0...011	$1/2(-h_0+h_1-h_2...-h_{N-1})$
4	0...100	$1/2(-h_0+h_1-h_2...-h_{N-1})$
.	.	.
.	.	.
2^{N-1}	1...111	$1/2(+h_0+h_1+h_2...+h_{N-1})$



Slika 2: Digitalno sito v modificirani obliki porazdeljene aritmetike

Novo modificirano strukturo nerekurzivnega digitalnega sita v porazdeljeni aritmetiki prikazuje slika 2.

Posebna prednost modificirane oblike je v povečani dinamiki izhodnega signala. Prisotna je tudi zmanjšana kompleksnost strukture, ki pa pri izvedbi z LCA elementi ni tako aktualna.

3. Xilinxova vezja družine XC3000 in razvojni paket XACT 5.0

Sito smo napravili s programirljivimi Xilinxovimi LCA vezji družine XC3000. Oglejmo si osnovne značilnosti LCA vezij in Xilinxovega razvojnega programskega paketa XACT 5.0.

3.1. Arhitektura LCA vezij

Arhitekturo LCA vezij v splošnem sestavljajo trije tipi programirljivih elementov:

Vhodno izhodni bloki (IOB) so razporejeni po obrobju LCA vezja in služijo za povezovanje z zunanjim svetom. Na vhodne priključke je možno programsko priključiti dvižne upore in določiti hitrost naraščanja izhodnega signala. Uporabimo jih lahko tudi kot tristanjski vmesnik ali pa kot zadrževalnik.

Konfiguracijski logični bloki (CLB) so osnovni gradniki LCA logičnih vezij. Vsak CLB vsebuje dva D flip flopa in logični kombinatorni del, s katerim je možno realizirati pet vhodno funkcijo z dvema različnima izhodoma.

Programirljivi povezovalni elementi so namenjeni za povezovanje posameznih elementov znotraj LCA strukture. Za različne časovne zahteve in načine povezovanja ločimo naslednje povezovalne elemente. Vzdolžne in navpične dolge povezovalne linije oblikujejo mrežo v LCA vezju. Namenjene so za signale, ki morajo prepotovati večje razdalje v strukturi in imeti minimalne časovne zakasnitve.

Neposredne povezave so povezave med posameznimi sosednjimi elementi znotraj LCA strukture. To so lahko povezave med konfiguracijskimi logičnimi bloki ali pa vhodno izhodnimi bloki.

Splošne povezave so mreža metalnih odsekov, ki ležijo horizontalno in vertikalno v prostoru. Skupaj s stikalnimi matrikami povezujejo elemente v LCA strukturi.

3.2. Inicializacija LCA vezij

Uporabljena LCA vezja temeljijo na SRAM tehnologiji. To pomeni, da jih je potrebno pred vsakim vklopom napajalne napetosti ponovno inicializirati. V notranjosti LCA vezja je logika, ki samodejno ob vklopu napajanja sproži inicializacijsko sekvenco. Inicializacijska vsebina je zapisana v klasičnem EPROM pomnilniku. Pri uporabi večih LCA vezij na tiskanem vezju je možno iz enega EPROM pomnilnika inicializirati več LCA naprav. Pri tem prva (glavna) naprava krmili inicializacijo ostalih naprav. Vse naprave pa začnejo delovati v uporabniškem načinu ob istem času, s tem pa je doseženo sinhrono delovanje in ni potrebe po dodatnih sinhronizacijskih linijah.

3.3. Razvojni paket XACT 5.0

Načrtovanje sita z razvojnim paketom XACT 5.0 ne poteka s primitivnimi elementi, ki so opisani v poglavju (3.1), ampak z v naprej pripravljenimi makroji. Xilinxov razvojni paket XACT 5.0 ima bogato knjižnico z makroji v obliki večbitnih števnikov, pomikalnih registrov, zadrževalnikov in seštevalnikov.

Z njim je bilo omogočeno enostavnejše in preglednejše načrtovanje vezij z vnaprej opisanimi makroji kot so seštevalniki, števci, registri in multipleksorji.

Razvojni paket XAKT 5.0 pa omogoča tudi uporabo X-blokov. Uporaba X-blokov podpira vektorski pristop načrtovanje posameznih struktur. Strukturo načrtamo z elementi iz knjižnice X-blokov. Širino strukture pa določimo kasneje, glede na zahteve aplikacije. Pri tem načrtovanju so dodatno upoštevane strukturne značilnosti posamezne družine, zato je učinkovitejši program za avtomatsko razmeščanje in povezovanje (APR) elementov. To pa doprinese tudi večji koncentraciji elementov znotraj LCA strukture in omogoča višje hitrosti delovanja vezij. Večino izhodnega LCA vezja smo načrtali z uporabo elementov iz knjižnice X-blokov.

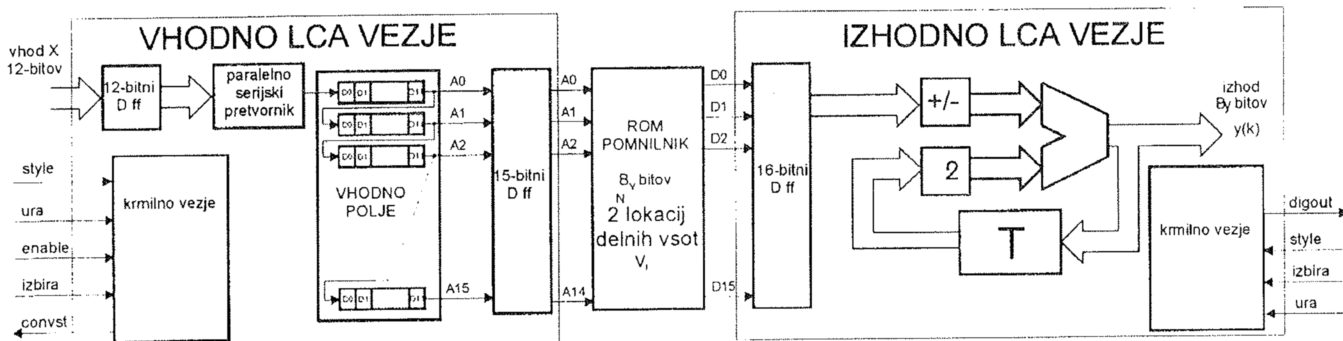
4. Izvedba

Digitalno sito smo izvedli z LCA vezji družine XC3000 /6/, ki so glede na velikost zadoščala našim potrebam. Za povezavo sita z okoljem smo predvideli dve možnosti glede na zahteve za praktično uporabo.

- Za povezavo sita z analognim okoljem smo uporabili 12-bitni AD pretvornik na vhodu in 12-bitni DA pretvornik na izhodu.
- Za povezavo z digitalnim okoljem pa smo uporabili kar 12-bitni digitalni vhod in izhod za neposredno priključitev digitalnega generatorja belega šuma na vhodu in logičnega analizatorja na izhodu.

V izvedbi smo zagotovili 12-bitno dolžino vhodno izhodne besede. Dolžina besede za zapis delnih vsot koeficientov v pomnilniku je 16-bitna, medtem, ko je dolžina besede v aritmetičnem delu sita 19-bitna.

Digitalno sito sestavljata dve LCA vezij XC3042 in pomnilnik vrste EROM. Pri digitalnem situ s 15 koeficienti potrebujemo pomnilnik s kapaciteto 32k besed. V vhodnem LCA vezju smo izvedli vhodno polje, v izhodnem LCA vezju pa aritmetični del strukture. Za izvedbo digitalnega sita v dveh LCA vezjih smo se odločili zaradi potrebnega števila logičnih konfiguracij-skih blokov in potrebnega števila vhodno izhodnih pri-ključkov. Tudi struktura porazdeljene aritmetike je takšna, da izvedba v dveh LCA vezjih ne zmanjša hitrosti in ne natančnosti izračuna izhodnega signala. Blokovna shema je prikazana na sliki 3.



Slika 3: Blokovna shema celotnega sita

4.1. Vhodno LCA vezje

Vhodno LCA vezje je prikazano na sliki 4. Vsebuje paralelno serijski pretvornik, vhodno polje in krmilno vezje. Vhodni zadrževalnik zajema vhodno besedo x(k) z vhodnega podatkovnega vodila s frekvenco vzorčenja 333 kHz. 12-bitni paralelno serijski pretvornik jo vpiše v vhodno polje. Vhodno polje je pomični register velikosti 180 bitov in je namenjeno za generiranje naslovnega vektorja za naslavljanje delnih vsot koeficientov, ki so zapisane v EPROM pomnilniku.

Krmilno vezje omogoča delovanje sita v glavnem ali pa pomožnem načinu. Način delovanja izbiramo z linijo IZBIRA. S kontrolno linijo STYLE pa izbiramo med klasično obliko porazdeljene aritmetike in med modificirano obliko porazdeljene aritmetike. Zasedenost vhodnega LCA vezja je bila po številu konfiguracijskih logičnih blokov 72%, po številu vhodno izhodnih blokov pa 34%.

4.2. Izhodno LCA vezje

V izhodnem LCA vezju smo izvedli aritmetični del digitalnega sita. Zaradi zmanjšanja vpliva kvantizacije na izračun izhodne besede y(k) in dovoljene prekoračitve vmesnih rezulatov preko absolutne vrednosti 1 smo uporabili 19-bitno širino strukture s seštevalnikom in zadrževalnim registrom. Aritmetični del je načrtan z elementi iz knjižnice X-blokov. Na sliki 5 je prikazana načrtana struktura izhodnega LCA vezja. V izhodnem LCA vezju je tudi krmilno vezje, ki je skoraj povsem identično s krmilnim vezjem v vhodnem LCA vezju. S tem smo dosegli sinhrono delovanje vhodnega in izhodnega LCA vezja. Zaradi takšnega načina delovanja ne potrebujemo linije za sinhronizacijo izhod-nega LCA vezja z vhodnim LCA vezjem. Izračunano izhodno vrednost y(k) pripeljemo ločeno na izhodno vodilo za 12-bitni digitalni izhod, ali pa neposredno na podatkovno vodilo D/A pretvornika.

Zasedenost izhodnega LCA vezja je bila po številu konfiguracijskih logičnih blokov 48%, po številu vhodno izhodnih blokov pa 50%. Shemo vezja kaže slika 5.

5. Rezultati

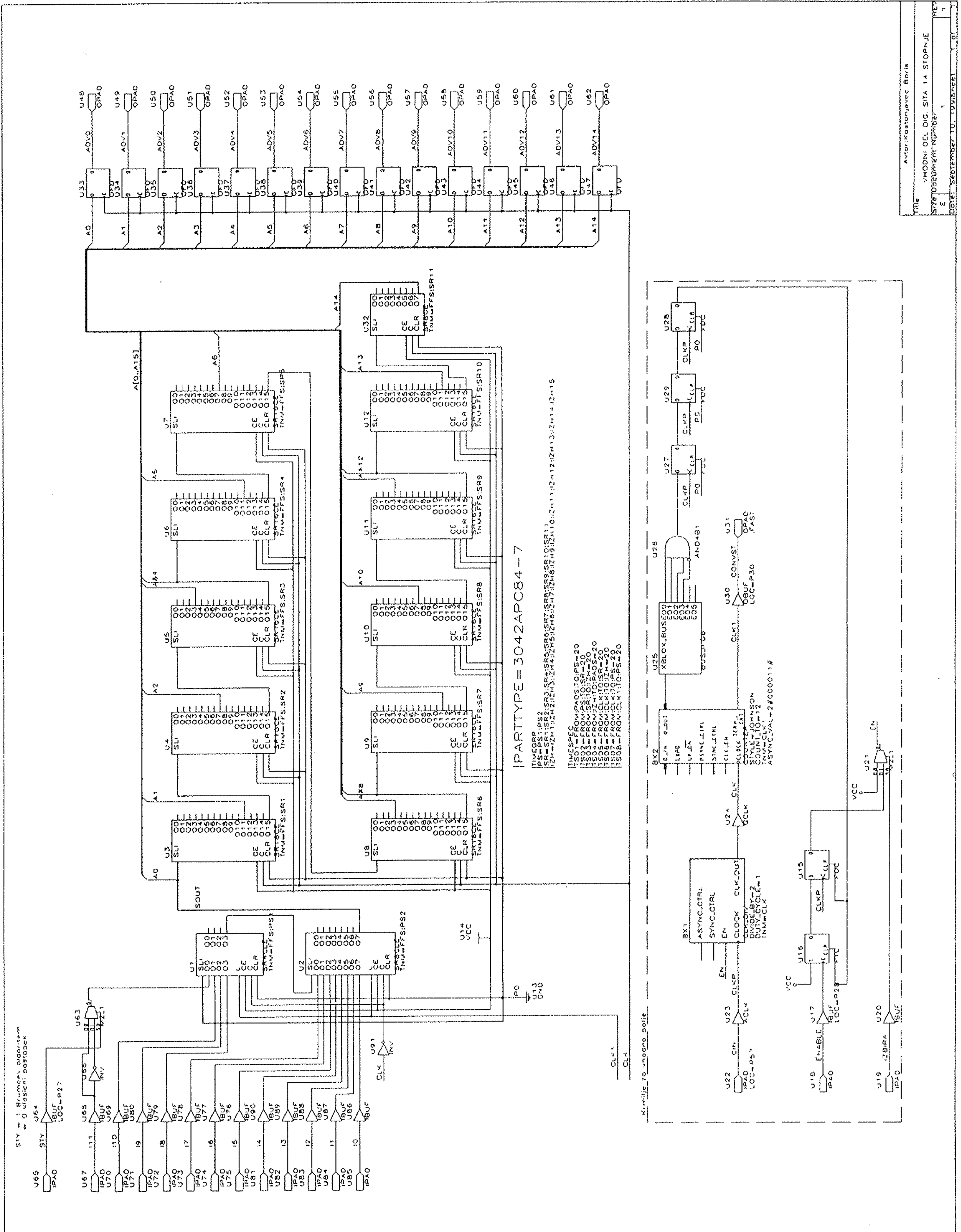
Univerzalna struktura opisanega digitalnega sita omogoča izvedbo poljubne oblike amplitudne frekvenčne karakteristike. Ogledali si bomo nizkoprepustno sito s 15 koeficienti, ki ima relativno prepustno frekvenco $f_P=0.1f_V$, in relalivno zaporno frekvenco $f_Z=0.2f_V$. Z f_V je oznalčena frekvenca vzorčenja. Koeficienti sita, ki določajo ta frekvenčni odziv sita, so zapisani v tabeli 3.

Tabela 3: Koeficienti nizkoprepustnega digitalnega sita

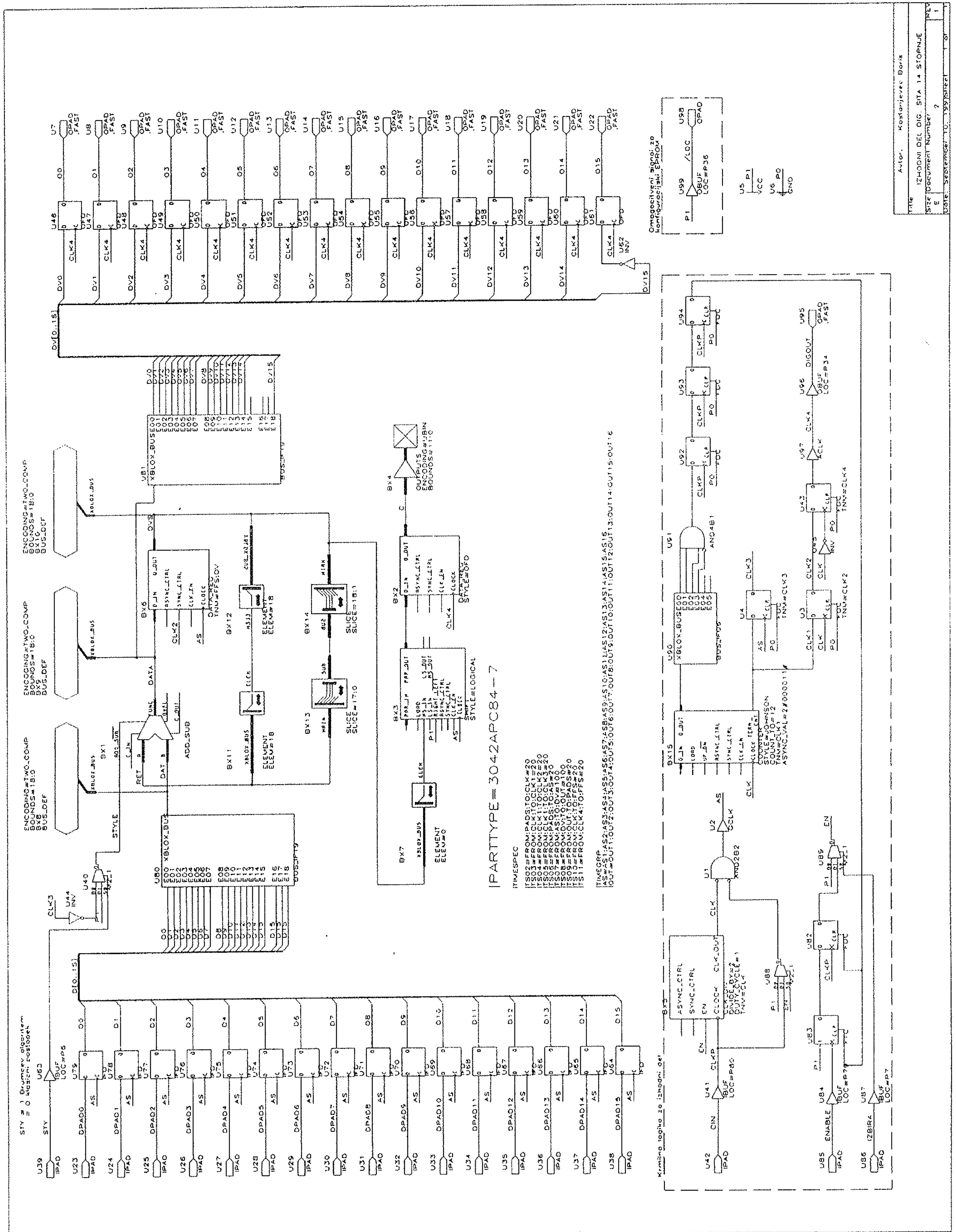
h(n)	nizkoprepustno sito $f_p = 0.1$; $f_z = 0.2$
h(0)=h(14)	1.326373E-02
h(1)=h(13)	-2.275006E-02
h(2)=h(12)	-4.475454E-02
h(3)=h(11)	-3.804951E-02
h(4)=h(10)	0.0271117
h(5)=h(9)	0.1419171
h(6)=h(8)	0.2543791
h(7)	0.3012954

5.1. Meritev amplitudnega odziva z analognim generatorjem spremenljive frekvence

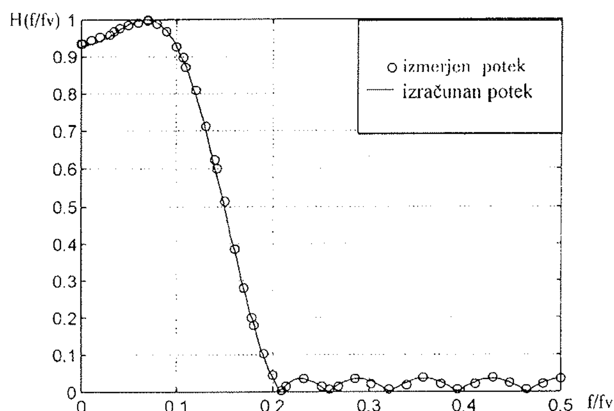
To je klasična merilna metoda za meritev amplitudnega frekvenčnega poteka. Na vhodu sita smo uporabili generator sinusnega signala spremenljive frekvence. Frekvenca vzorčenja je bila 333 kHz. Meritev smo opravili v pričakovanih točkah amplitudnega odziva. Na sliki 6 sta prikazana izračunani in izmerjeni amplitudni frekvenčni odziv v absolutnem merilu.



Slika 4: Vhodno LCA vezje z vhodnim poljem za generiranje naslovnega vektorja in krmilnim vezjem

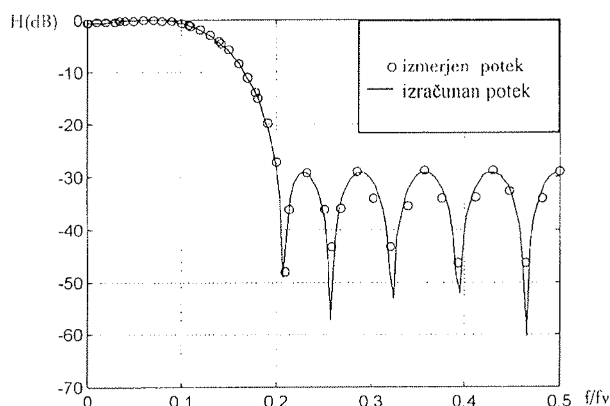


Slika 5: Izhodno LCA vezje z aritmetičnim delom strukture za izračun izhodne besede y(k)



Slika 6: Primerjava med izračunanim in izmerjenim amplitudnim odzivom digitalnega sita v absolutnem merilu za modificirano obliko digitalnega sita

Zaradi boljšega pogleda na razmere v zapornem področju frekvenčne karakteristike sta na sliki 7 prikazana izračunani in izmerjeni amplitudni odziv v logaritemskem merilu.

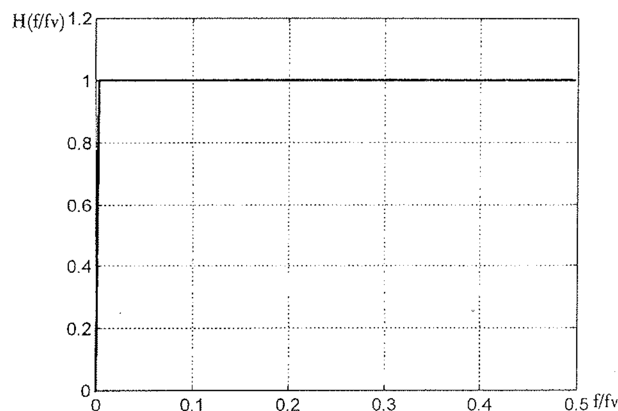


Slika 7: Amplitudni odziv digitalnega sita v logaritemskem merilu za modificirano obliko porazdeljene aritmetike

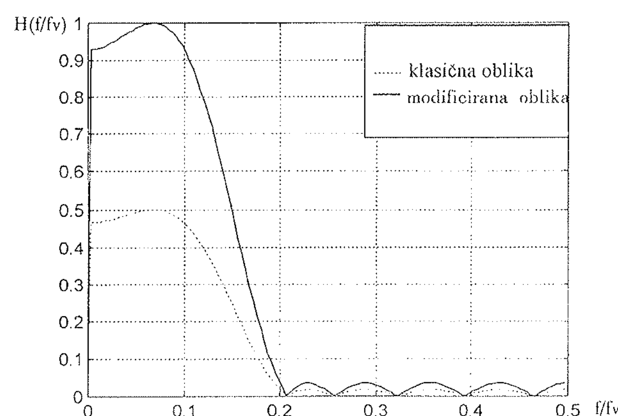
5.2. Meritev amplitudnega in faznega odziva z uporabo digitalnega generatorja belega šuma

Z uporabo digitalnega generatorja belega šuma na vhodu digitalnega sita dobimo odziv vezja na beli šum. Izhodne vrednosti y(k) smo zajemali z logičnim analizatorjem, dobljene podatke pa obdelali s programskim paketom Matlab /5/. S hitro Fourierjevo transformacijo dobimo praktično zvezni frekvenčni odziv.

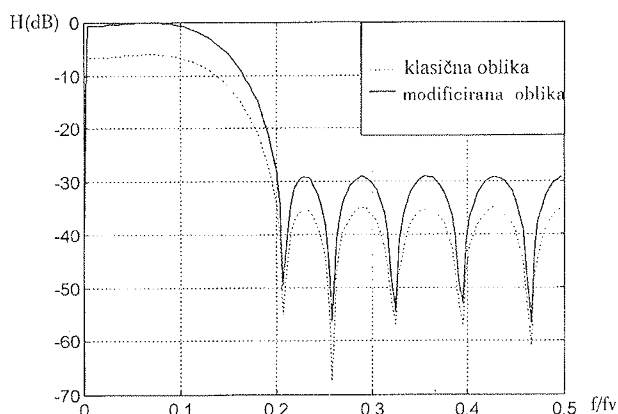
Ker smo meritve opravljali na situ s petnajstimi koeficienti, je za dovolj natančno meritev zadostoval beli šum z 256 naključnimi vzorci v periodi. Na sliki 8 je prikazan amplitudni spekter vhodnega belega šuma, ki smo ga pripeljali na vhod sita, na slikah 9 in 10 pa sta prikazana amplitudna odziva digitalnega sita v klasični in modificirani obliki porazdeljene aritmetike v absolutnem in logaritemskem merilu.



Slika 8: Frekvenčni spekter vhodnega signala



Slika 9: Primerjava amplitudnih odzivov digitalnega sita po klasičnem in modificiranem postopku

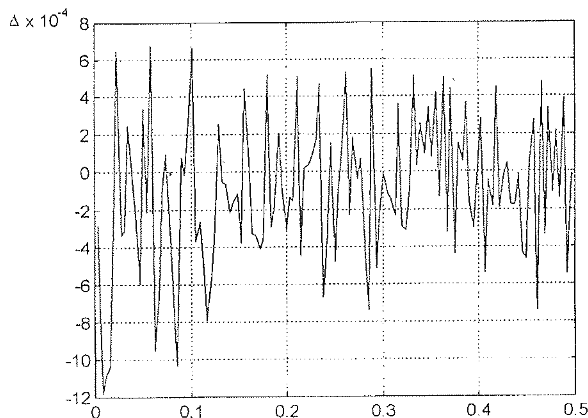


Slika 10: Primerjava amplitudnih odzivov digitalnega sita po klasičnem in modificiranem postopku

Čeprav dosežemo pri obeh strukturah isto vrednost slabljenja približno 30dB, pa je pri uporabi modificirane strukture porazdeljene aritmetike lepo vidno povečanje dinamičnega območja za 6dB.

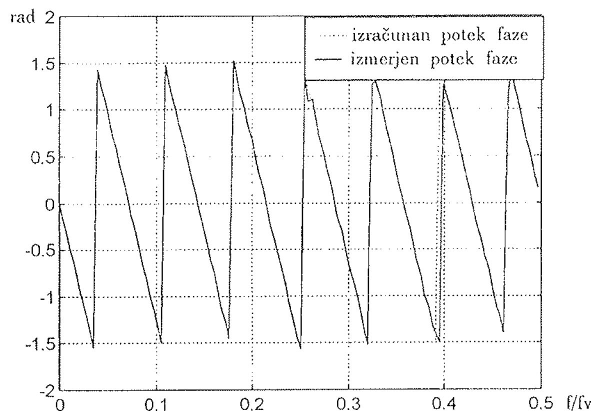
Izmerjeni rezultati amplitudnega odziva z uporabo digitalnega generatorja belega šuma se zelo dobro ujemajo

z izračunanimi vrednostmi. Na sliki 11 podajamo odstopanje izmerjenega amplitudnega odziva od izračunanega, ki je reda 10^{-3}. Odstopanje je podano za modificirano obliko digitalnega sita.



Slika 11: Odstopanje med izmerjenim in izračunanim amplitudnim odzivom digitalnega sita v modificirani obliki porazdeljene aritmetike

Z uporabo simetričnih koeficientov ima naše sito linearni potek faze v celotnem frekvenčnem področju. Potek faze se dobro ujema z izračunanim potekom. Potrebno je pa vedeti, da je bila pri izračunu poteka faze odpravljena zakasnitev $T=1/f_v= 3\mu s$, ki jo je vnašalo digitalno sito.



Slika 12: Potek faze pri modifcirani obliki digitalnega sita.

6. Zaključek

Prikazali smo, da omogočajo programirljiva polja logičnih vezij enostavno in uspešno izvedbo nerekurzivnih digitalnih sit, posebej, če sita izvedemo v strukturi porazdeljene aritmetike. S primerjavo med klasično in modificirano obliko smo pokazali, da dosežemo z modificirano obliko strukture porazdeljene aritmetike pri isti vrednosti slabljenja v zapornem frekvenčnem področju za 6 dB večje dinamično območje izhodnega signala.

Univerzalna struktura nerekurzivnega digitalnega sita je izvedena v dveh LCA vezjih XC3042. Pri izbiri vezij iz družine XC4000 bi zadostovalo tudi eno samo vezje. Pri 12-bitni kvantizaciji vhodnega in izhodnega signala, smo izbrali 16-bitni pomnilnik za zapis delnih vsot koeficientov ter 19-bitno aritmetično enoto. Pri takšni kompleksnosti vezja smo za nizko prepustno sito s petnajstimi koeficienti ter zahtevanimi parametri $f_p= 0.1f_v$ in $f_z=0.2f_v$ dosegli slabljenje 30dB. Frekvenca vzorčenja f_v je bila 333 kHz.

Frekvenčne odzive smo izmerili na dva načina:

- po klasičnem postopku merjenja amplitudnega in faznega odziva z generatorjem spremenljive frekvence sinusnega signala in
- meritev z uporabo digitalnega generatorja belega šuma na vhodu sita, pri čemer smo amplitudni in fazni odziv izračunali s hitro Fourierjevo transformacijo izhodnega signala. Izhodni signal smo zajeli z logičnim analizatorjem.

V primeru našega sita se rezultati lepo ujemajo.

7. Literatura

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PREDSTAVLJAMO PODJETJE Z NASLOVNICE
REPRESENT OF COMPANY FROM FRONT PAGE

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Instead of company presentation which has already been done several times in this Journal, we bring you some news and new AMS press releases.

Advance to new technologies

A new technology generation for the production of mixed analog/digital high performance ASICs was announced by Austria Mikro Systeme at press conference in Vienna:

The company has succeeded to progress into the field of "deep submicron" technology (structures smaller than 0.5 micron, about 1/100th of the diameter of a hair), which will be essential for the production of highly complex chip generations for the turn of the century. These will find application in new information technologies, multi-media, for the transmission of largest amounts of data, the integration of micro-mechanical components and in sensors (pressure, temperature, optical, magnetic, acceleration, etc.), airbags, medical electronics and mobile applications such as heart pace makers and robots.

This new superior technology can be characterized by highest switching speeds of transistors in the Pico second range. Several million different components are integrated in one chip with a minimum of power consumption; this chip generation achieves highest packing densities with enhanced features.

Through the introduction of "deep submicron" technologies a growing number of highly complex electronic systems on a single chip can be combined - the results: Increased functionality, reliability, savings in costs and space.

The miniature structures of the active devices, such as the transistors in **0.35 micron technology** are certainly smaller than the wave length of visible light (around 0.45 micron). This has necessitated the implementation of new methods, materials and equipment for the development and production of prototypes.

This technology has been accessible only for so-called "digital" standard products such as memories and microprocessors only and is now also available for mixed analog/digital circuits. The decisive break-through succeeded in the joint project together with leading semiconductor manufacturers in Europe under ESPRIT (European Strategic Projects in the Research of Information Technologies). This project is of strategic importance for Europe.

Together with the partners SGS-Thomson (France/Italy), GEC-Plessey (England), Matra-MHS (France), Mietec-Alcatel (Belgium), Philips (The Netherlands), Siemens (Germany) in SHAPE "Sub HAlf Micron Process for European Users" Austria Mikro Systeme has developed this new technology. The company was invited to partake because of its technological competence in the field of R & D and design of ASICs, the development and production of high performance analogue/digital ICs. Austria Mikro Systeme has chiefly contributed in this framework by developing highly complex process modules, transistor models and mixed analog/digital components.

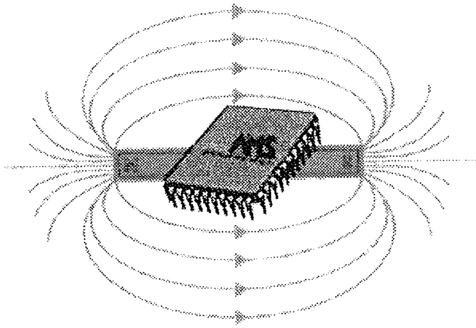
Advisor to the Minister, Dr. Heinrich Bodenseher, Ministry of Science and Transport: *"Through the participation in SHAPE together with leading European semiconductor manufacturers Austria Mikro Systeme can predominantly determine the development of the strategically significant semiconductor technology for the turn of the century. The European semiconductor industry - including Austria Mikro Systeme - can be ranked as the world's top class, among the USA and Japan".*

Market researchers as well as the media *(Semiconductor International, USA, 3/1997)* have rated Austria Mikro Systeme as prominent in the manufacture of mixed analog / digital circuits in Europe. Through the introduction of the new technology the company will continue to reinforce this position and expand it further world wide.

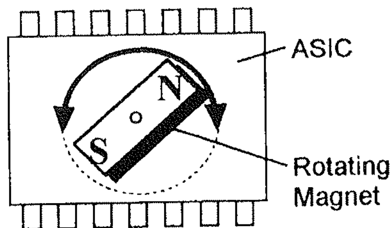
Singe-Chip Magnetosensor ASIC Macros for Absolute Angle Measurement

Austria Mikro Systeme announces the availability of CMOS mixed analog/digital ASIC macros which include on chip magnetosensors and detect magnetic fields produced by a low cost external magnet for calculating absolute angles from 0° to 360°.

Magnetosensor ICs can replace expensive optical encoders, potentiometers or mechanical switching systems determining angles. Applications include instrument panel (e.g. multi-position rotary switches) and step motor controls, steering wheel position indicators, electric motor torque control, industrial and robotics positioning and monitoring systems.



Robust angle measurement is ensured by signal processing that compensates for external fields and alterations in the magnetic field amplitude (e.g. due to temperature, mechanical stress, ageing, manufacturing tolerances). Analog as well as digital signal processing circuitry can be combined on the same chip to convert the sensor signals into an analog voltage or a digital bit word that corresponds to the absolute angle position. The chip measures the absolute angle of a rotating encoder magnet (N-S magnet or magnet pair) and very small magnets (~3 mm) with high rotation frequencies of >30,000 revolutions per minute. The sensor system block for angular measurement is self-contained and does not require additional external devices. Additional circuit blocks such as micro cores, digital interfaces or output drivers are integrated according to customer specification to form a complete ASIC system.



Advantages of these magnetic sensor ASIC systems are their adaptability to different magnetic encoders, insensitivity towards dust, dirt, moisture, oil films, their built-in compensation capabilities for external magnetic fields, self-test, self-diagnostic and self-trimming features, e.g. to compensate for system assembly tolerances.

New High Voltage 0.8 μm CMOS Processes

Austria Mikro Systeme and Thesys offer a new family of mixed signal CMOS processes, designated as "CXT, CXY and CXZ", suited for high voltage ASIC solutions for up to 50V.

The 0.8 micron double metal, single poly, basic process "CXT (CX08HA)" was primarily developed for ASICs incorporating complex digital parts with high speed and high density elements operating in a high voltage environment. The "CXY (CX08HD)" process is a double metal, double poly version for the integration of linear capacitances and "CXZ (CX08HI)" is a double metal, double poly, high resistive poly process for linear resistance applications requiring a minimum area.

A variety of high voltage devices is available in addition to the standard low voltage MOS Transistors: HV-NMOS, -PMOS, -DMOS-transistors, N junction FETS, isolated NPN bipolar transistors, isolated LV-NMOS Transistors etc.

High voltage and standard devices can be easily combined on the same ASIC through the new technology. Low power consumption, fast switching capabilities and **applicability to a wide range of automotive and industrial performance require-ments are further key benefits of this advanced process family**, being especially suited to withstand high voltage spikes which typically occur in such environments. Further applications include its use in fast high precision analogue circuits and in analogue front-ends for sensors and transducers.

Together with the proven 0.8 micron digital library the new 0.8 micron process family represents the ideal solution for high voltage ASICs.

Extended Foundry Services

To meet the increasing demand for customer ASIC designs to be completed and to be manufactured even more quickly, the Austria Mikro Systeme Group now offers extended foundry services at attractive pricing.

The advantages of the Group's foundry capabilities for the customer are:

- thorough design support with most comprehensive documentation and informal access to technical assistance
- most reliable device models
- an even wider choice of CMOS and BiCMOS process technologies to choose from: high voltage, low voltage, mixed signal and EEPROM processes from 0.6 to 1.2 micron
- more affordable sample and prototyping services
- shorter mask, fab and packaging cycles

The Group also provides unique multi-product wafer capabilities and multi-level mask services. By splitting wafer and mask costs among several projects, significant savings can be passed on to the customer.

All stages of manufacturing can be completed under one roof - R & D, design, mask lithography, wafer fabrication, assembly and test which allow for most competitive lead times for processing and highest quality. The products of the customer can be manufactured at any of the three locations of the Group:

- Thesys in Erfurt, Germany
- Austria Mikro Systeme in Austria, with more than one decade of focused customer support experience
- SAMES in Pretoria, South Africa.

Whatever the design resource, interface and experience of the customer the Group has the flexibility to quickly deliver the ASIC product the customer needs.

VESTI - NEWS

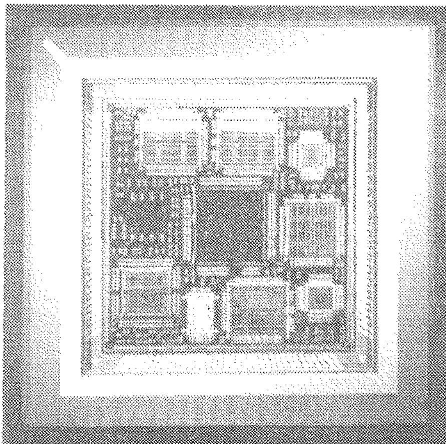
NEWS FROM IMEC

Pentium MCM packaged in PSGA

A Pentium MCM has been developed in MCM-D technology by a collaboration in the frame of EUROPRACTICE MCM. The MCM is intended as a processor subsystem in portable PC-system and embedded applications and is packaged in the new PSGA package.

The Pentium MCM contains a Mobile Pentium Processor (120/133 MHz), a Mobile Triton system controller, which provides PCI, cache and DRAM control, two data path chips for DRAM interface, 512 kb synchronous pipelined Burst 2nd level cache, Tag-SRAM, a clock driver and high-speed decoupling capacitors. Advantages are clear: integration of the system in an MCM not only reduces the size and weight of the system, but also the complexity of the overall design and of the PC board in particular. Power consumption and ringing is reduced thanks to the internal routing of all high-speed host bus signals.

The Pentium MCM is mounted in the thermally enhanced PSGA, a packaging technology developed jointly by IMEC and Siemens LTP Oostkamp (Belgium), and presented in our April 1997 Newsletter. This provides for low cost packaging of high pin-count devices.



Pentium MCM before assembling in the PSGA package. The substrate size is 32x32 mm. The chip is packaged in a 320 pins thermally enhanced PSGA o f 43x43 mm.

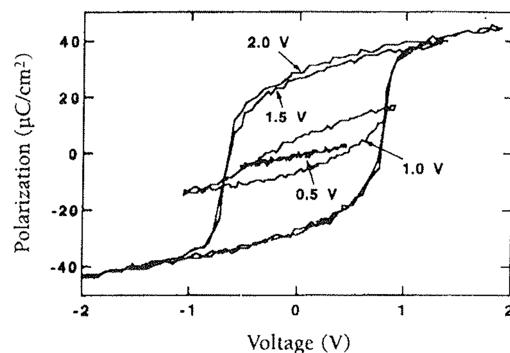
The chip has been mounted on a PC motherboard. First tests have been carried out successfully with Windows NT running and some benchmark programs at a clock frequency of 100 MHz.

Ultra-thin PZT ferroelectric capacitors enable low-voltage operation

A breakthrough in thickness scaling of PZT films

Lead-Zirconate-Titanate ($Pb_xTi_{1-x}O_3$) is a well known ferroelectric material and is one of the possible candidates for ferroelectric non-volatile memories. The remanent polarization Pr of PZT (20-40 μC/ cm^2) is much higher than that of its "rival" SBT material ($SrBi_2Ta_2O_9$) (P_r =10-15 μC/cm^2), resulting in a larger signal and enabling the fabrication of larger density memories. However, PZT ferroelectric capacitors require larger voltages to switch (3-5V) compared to SBT (1.5-3V). Therefore, SBT seemed to be preferable for low-voltage operation compatible with the scaled supply voltage for the high-density memories (1.2-2V for 1 Gbit DRAM), and also of interest for portable, battery-operated or RF-powered systems.

Recently however, IMEC succeeded in a major breakthrough in the fabrication technology of thin PZT films, enabling the deposition of down to 50 nm ultra-thin films retaining the same excellent hysteresis properties (P_r = 30 μC/cm^2) and high hysteresis loop rectangularity as thicker (200 nm) films (measured on Pt-electroded capacitors). Notwithstanding an increase of the coercive field for the thinner films, the coercive voltage was reduced to 0.76 V and fully saturated switching was obtained at 1.5 V for the 50 nm film.



Hysteresis behavior of PZT films.

IMEC launches new Industrial Affiliate Program (IIAP) on Integrated Ferroelectrics

IMEC recently started a new IIAP on integrated ferroelectrics to develop viable process technology for integration of ferroelectric thin-film devices with current submicron CMOS technology

Four different research modules in Integrated Ferroelectrics have been defined: materials, CMOS compatibility process integration, and characterization and testing.

Target companies include electronic chemicals suppliers, semiconductor equipment manufacturers involved in high-k oxide and ferroelectric deposition technology and IC manufacturers interested in ferroelectric applications and integration issues.

About five companies have already expressed their interest in joining this program. It is the intention to start the program during the third quarter of 1997.

Simple and efficient process for silicon solar cells

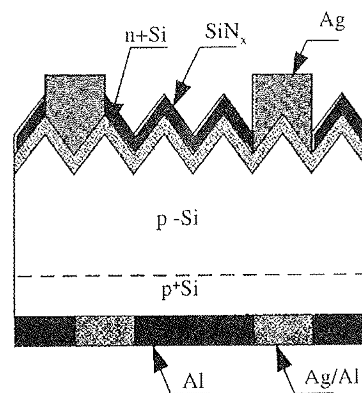
A recent study concerning the feasibility of a large production scenario of silicon solar cells (500 MWp/year) has indicated the importance of multicrystalline silicon. However, this necessitates an industrial solar cell process capable of producing high-efficient multicrystalline cells at low cost. IMEC has developed such a process based on firing the screen printed contacts through a PECVD deposited silicon nitride layer.

In order to reach high efficiencies on multicrystalline Si which suffers from intragrain and intergrain defects, the bulk of the material has to be passivated. Most high-efficient multicrystalline cells have received either a long hydrogenation treatment or a gettering step, or both. Neither of these has found a place in production lines due to their duration, thermal budget and/or the cost involved.

A process capable of achieving an excellent passivation of the surface and bulk of the cell in a very short time has been developed in IMEC. The total process sequence consists of only 6 steps: saw damage removal, surface texturization, emitter diffusion, SiNx deposition by direct Plasma Enhanced Chemical Vapour Deposition (PECVD), screen-printed metallization and parasitic junction removal. The crucial step is the contact firing.

This process has resulted in an absolute efficiency increase of 1 to 3% depending on the starting quality of the material compared to a classical process with TiO_x as ARC. The lower the material quality the higher the improvement will be from the "firing through SiN_x" process.

This simple process has led to efficiencies of 17.3% on monocrystalline and 15.8% on multicrystalline Si solar cells. A combination of the firing through the SiN_x process with mechanical grooving of the front surface to reduce the reflection in the case of multicrystalline cells (in collaboration with the University of Konstanz), has resulted in an efficiency of 16.4% on 100 cm^2 multicrystalline Si substrates.



Structure of screen-printed solar cell made by firing through SiN_x process.

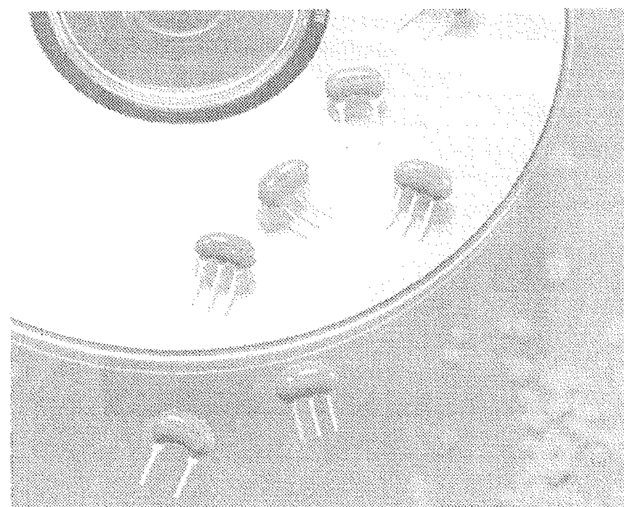
A lot of major industrial Si solar cell manufacturers have shown considerable interest in this process.

NEWS FROM MURATA

Tight tolerance resonators

Use this new ceramic resonator technology to reduce costs and replace quartz crystal oscillators in CAN-Bus systems, CD-ROM drivers, digital video discs, DVB settops and many other applications.

Murata's CSA□.□□MGN and CSA□.□□MGNA series use new technology. This improves the performance of well established families of resonators and



Comparison of Stabilities

Vibration mode	Status	Absolute best available tolerance	Deviation with Temperature		Ageing tolerance	Best total error available -40 to 85°C
			-40 to 85°C	-40 to 125°C		
MG	Current	±0,2%	±0,3%	±0,4%	±0,3%	±0,8%
	New	±0,1%	±0,2%	±0,25%	±0,1%	±0,4%

enables them to be used in applications previously only satisfied by quartz crystal performance.

The Car Area Network Bus is a good example of the way this product helps engineers. Systems can require overall clock stability as high as 0.4 %. This used to incur the cost and space of a crystal oscillator. As the table shows, this is now achievable with the much more economic ceramic resonator.

The current frequency range is 1.8 to 6.3 MHz with standard frequencies at 2.0, 2.45, 3.0, 3.58, 3.68, 4.0, 4.19, 4.91, 5.0 and 6.0 MHz. In due course the range will be extended to 12 MHz and the close tolerances will become available in the well known CSA□□.□□MX series.

Ageing over 10 years is a maximum of ±0,1 %. Resonant resistance is 30Ω maximum, insulation resistance is 5×10^8 Ω minimum at 10VDC and withstanding voltage is 100VDC for 5 seconds. The family is rated at 6VDC and 15 VAC(p-p).

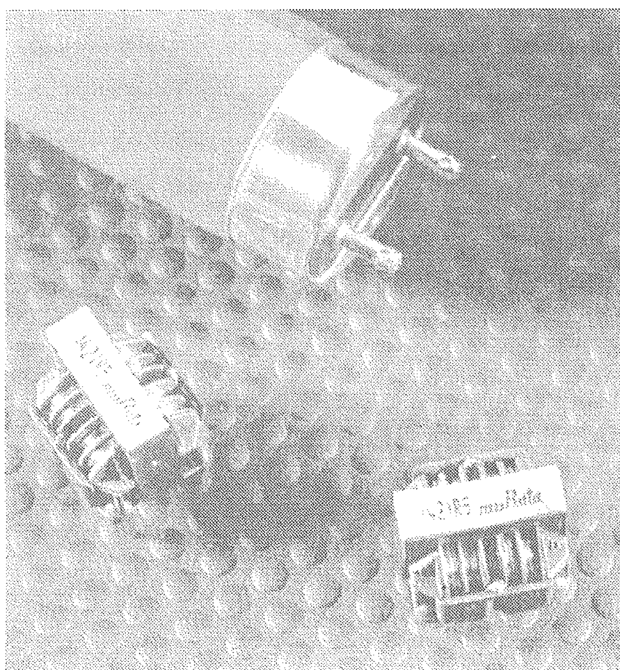
Most common cleaning methods are safe but Murata data defines limits for each which should never be exceeded. Mechanically the new family is identical to the CSA□.□□MG and is delivered in plastic bags containing 500 pieces or on tape in ammo-packs containing 1,500 pieces.

Samples are now available on request.

Compact choke coil suppresses differential and common mode noise

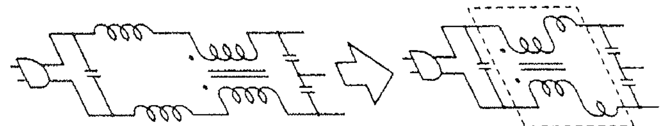
There are various ways of satisfying the harmonic current limitations of IEC1000-3 and EN60555-2. The most popular methods are active filter and oneconverter.

However, these cause further differential noise problems because of the active components employed. It is then necessary to use additional filtering components to suppress that noise.



Common mode choke coil
+
Differential mode choke coil

Hybrid choke coils is applied



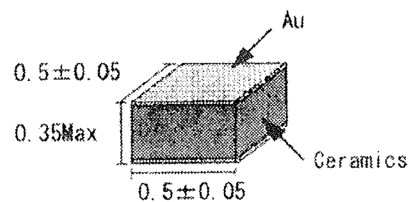
Murata's new, compact, high performance PLY11 choke coil has a dual function and solves both differential and common mode problems. This design reduces the number of components and minimises the space occupied by choke coils on the PCB. In addition general purpose common mode chokes, which are normally large to cover the lower frequencies, can very easily be replaced by the smaler and lighter PLY11.

The range offers common/differential mode inductances from 14mH/1mH to 0.45mH/0.05mH and can be used up to 250VAC. They are available in bulk packs.

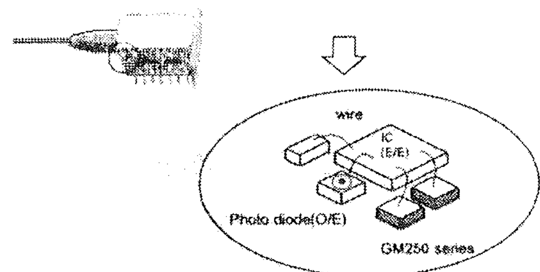
New high capacitance microwave MLCC

Murata introduces high value, sub-miniature vertical electrode micro-chip capacitors for die and wire bonding.

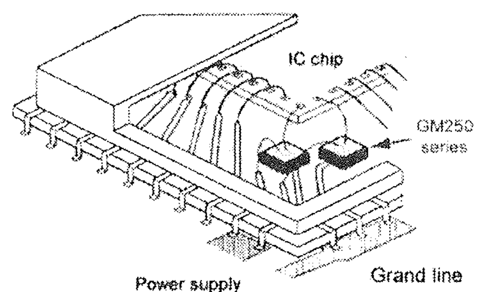
Dimension



1. Optical device for tele communication



2. IC package built-in

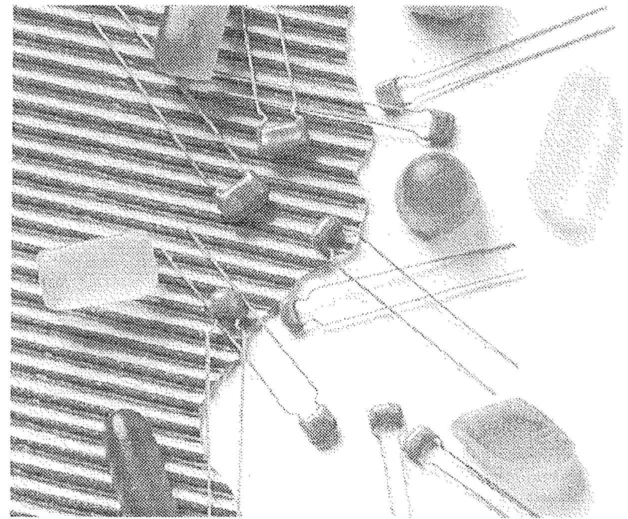


The Murata GM250 series of multi-layer ceramic capacitors provides higher values and better frequency characteristics than its predecessors. It is smaller and has electrodes on the upper and lower surfaces so that bonding processes can be employed.

The size reduction will enable users to mount the capacitors inside IC packages adjacent to bare chips as well as on substrates. Naturally reducing size improves the microwave performance.

Applications include bypassing in photo-receptors for optical telecommunications equipment, optical sensors and optical modules in general. Many uses will have an important effect on industry in the 21 st Century.

This product is in mass production now so talk to your regular Murata contact for details.



Replace single layer capacitors with advanced multilayer capacitors - use RPE (Y5V)

The very popular dielectric Y5V so far mainly used in Europe in SMD-Capacitors, is now available in Murata's radial leaded version - RPE.

Murata's factory in Bechhofen/Germany added the dielectric with Y5V characteristic to its product range to be able to offer an attractive leaded capacitor for general purpose use to customers in Europe. As the competitive market forces all set makers to search for possibilities to reduce costs, Murata recommends the use of Y5V characteristic for decoupling on by-passing circuits where X7R multilayer capacitors have been used in the past.

The Y5V characteristics allow a capacitance change of +22% to -82% within a temperature range of -30°C to +85°C. It is therefore suitable for all standard applications in the consumer, EDP or communications markets. As this RPE utilizes multilayer technology, it may also be used to replace single layer capacitors. With the addition of Y5V the newest ceramic material technology has now been introduced to the RPE standard series.

The following RPE items are now available:

Capacitance Value	Capacitance Tolerance	Temperature Characteristic	Rated Voltage	Lead Space	Murata P/N
100 nF	+22 - 82%	-30°C to 85°C	50 VDC	2.54 mm	RPE131Y5V104Z50
100 nF	+22 - 82%	-30°C to 85°C	50 VDC	5.08 mm	RPE132Y5V104Z50
100 nF	+22 - 82%	-30°C to 85°C	25 VDC	2.54 mm	RPE131Y5V104Z25
100 nF	+22 - 82%	-30°C to 85°C	25 VDC	5.08 mm	RPE132Y5V104Z25
1 μF	+22 - 82%	-30°C to 85°C	25 VDC	2.54 mm	RPE121Y5V105Z25
1 μF	+22 - 82%	-30°C to 85°C	25 VDC	5.08 mm	RPE122Y5V105Z25
1.5 μF	+22 - 82%	-30°C to 85°C	25 VDC	2.5 mm	RPE121Y5V155Z25
1.5 μF	+22 - 82%	-30°C to 85°C	25 VDC	5.08 mm	RPE122Y5V155Z25

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Thin Film Users Group Annual Symposium
CMP Users Group Annual Symposium

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04.11.-06.11.1997

Wescon/IC Expo

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09.11.- 11.11.1997

Microlitography Symposium, Interface 97

San Diego, CA, USA

Info.: +1 800 624 2486

11.11.-14.11.1997

Productronica 97

Munich, Germany

Info.: + 49 89 5107 275

12.11.-13.11.1997

Advanced Wafer Processing Series: Etch/Planarization

Sunnyvale, CA, USA

Info.: +1 602 515 9780

19.11.-20.11.1997

Photolitography Seminar

Sunnyvale, CA, USA

Info.: +1 602 515 4260

DECEMBER

01.12.-05.12.1997

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Boston, MA, USA

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03.12.-05.12.1997

SEMI Technology Symposium (STS 97)

Chiba, Japan

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07.12.-10.12.1997

43rd Annual IEEE International Electron Devices Meeting (IEDM)

Washington, D.C., USA

Info.: + 1 301 527 0900

08.12.-12.12.1997

Semiconductor Technology Seminar

Austin, TX, USA

Info.: + 1 650 941 8272

09.12.-10.12.1997

14th Annual Flat Information Displays Conference

Monterey, CA, USA

Info.: +1 408 448 4440

16.12.-20.12.1997

9th International Workshop on Physics of Semiconductor Devices

Delhi , India

Info.: fax 91/11 2913609

NAVODILA AVTORJEM

Informacije MIDEM je znanstveno-strokovno-društvena publikacija Strokovnega društva za mikroelektroniko, elektronske sestavne dele in materiale - MIDEM. Časopis objavlja prispevke domačih in tujih avtorjev, še posebej članov MIDEM, s področja mikroelektronike, elektronskih sestavnih delov in materialov, ki so lahko:

izvirni znanstveni članki, predhodna sporočila, pregledni članki, razprave z znanstvenih in strokovnih posvetovanj in strokovni članki.

Članki bodo recenzirani.

Časopis objavlja tudi novice iz stroke, vesti iz delovnih organizacij, inštitutov in fakultet, obvestila o akcijah društva MIDEM in njegovih članov ter druge relevantne prispevke.

Strokovni prispevki morajo biti pripravljeni na naslednji način

1. Naslov dela, imena in priimki avtorjev brez titul.
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3. Naslov dela v angleščini.
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