CAPACITOR-AREA AND POWER-CONSUMPTION OPTIMIZATION OF HIGH ORDER Δ - Σ MODULATORS

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Keywords: computer science, microelectronics, SP, Signal Processing, DELTA-SIGMA modulators, Δ - Σ modulators, noise reduction, area optimization, power consumption optimization, design

Abstract: A design methodology for the power consumption and capacitor area optimisation of high-order high-resolution single-bit switched-capacitor type Δ-Σ modulators is described. The main reasons for the power consumption are determined and appropriate steps for its reduction are proposed. The algorithm is coded in MATLAB and gives the unit capacitor size of each integrator stage for an arbitrary topology and the required specification of each opamp used in the integrator to achieve the required S/N ratio, minimize the power consumption and the silicon area and preserve matching accuracy. The 5th order modulator was built and the results prove the effectiveness of the approach.

Optimizacija moči in površine Δ-Σ modulatorjev visoke stopnje

Ključne besede: racunalništvo,mikroelektronika, SP obdelave signalov, DELTA-SIGMA modulatorji , Δ - Σ modulatorji, zmanjšanje šuma, optimiranje površine, optimiranje porabe energije, snovanje

Povzetek: V članku obravnavamo metodologijo načrtovanja eno in večbitnih S-C Δ-Σ modulatorjev, ki omogoča optimizacijo površine silicija in porabo moči. Prikazani so glavni razlogi za porabo moči in potrebni koraki za zmanjšanje. Algoritem smo realizirali v programu MATLAB. Rezultat je tabela kondenzatorjev in specifikacije ojačevalnikov vsake integracijske stopnje za poljubno topologijo modulatorja. Cilja optimizacije sta zmanjšanje površine polja kondenzatorjev ter porabe moči ob upoštevanju robnih pogojev: zahtevano razmerje S/N, točnost razmerij kondenzatorjev itd. Primer optimizacije modulatorja 5. reda dokazuje učinkovitost algoritma in metodologije.

1. INTRODUCTION

The power-consumption optimisation methodology for high-order high-resolution Δ-Σ S-C modulators is presented. The optimisation procedure tries to minimize the unit capacitances of the integrators in a loop filter in such a way that the noise requirements are fulfilled, area is minimized and matching accuracy is maintained.

The contribution of each noise source is dependent on the architecture, coefficients, capacitances and noise generated in the opamps. Usually this is calculated by using the linear model of the modulator /3/, which is adequate method if one is satisfied with approximate results. Since modulators are non-linear systems, linear model is not good enough and we need real non-linear time-domain simulation and optimisation. The kT/C noise simulation principle was presented in /5/ assuming the unit capacitor sizes are given. In this work the unit capacitor sizes are optimised in such a way that contributions to the total noise are approximately the same. At the same time the requirements for the opamps regarding 1/f and thermal noise as well as slew-rate are determined and can be used as specifications for the circuit design. The model of chopping and more realistic models for the opamps are added to the existing algorithm given in /5/. The algorithm is coded in MATLAB and is based on state-space description of an arbitrary topology S-C Δ-Σ modulator. The constraints are minimum possible noise and at the same time appropriate accuracy of the capacitor ratios which are the area and the technology dependent. To illustrate the methodology one example is given. It presents power consumption optimisation of the 5th-order single-loop ML-FT (multiple-loop feedback topology) with poles optimised for stability, having S/N ≥ 110dB. The improvement of the power efficiency and area of the modulator prove the correctness of the approach.

In section 2 the reasons for power consumption in an arbitrary S-C modulator are analysed and the algorithm for noise optimisation is presented. Since most of the power is consumed by the opamps (≥80%) driving the capacitive loads, they must be minimized, taking the area and matching of the capacitor ratio as a constraint. The algorithm also defines the required noise level of the opamps, while the design of the opamps is beyond the scope of this article and the algorithm. Short example illustrates the procedure and gives some additional information.

Section 3 briefly repeats the published state-space description of an arbitrary modulator with an additional noise model of the S-C stages and opamps and gives some optimisation results as a table of capacitances and noise requirements. In section 4 the conclusions are presented.

2. REASONS FOR POWER CONSUMPTION

The main reason for power consumption in any switched-capacitor-type modulator is the power needed by the opamps to drive capacitive loads and to maintain the required noise level. To simplify the description of the power-optimisation procedure, the 5th-order modulator is taken as an example, for which the power-optimisation results are presented at the end. The procedure works well for any S-C-type modulator. The system design considerations for the 5th-order modulator have been presented in an internal report /1/ (figure 1).

The coefficients are realised with appropriate capacitor ratios according to figure 3. The coefficient a_1 is given by $a_1 = \frac{C_{u_1}}{C_{I_1}}$. In reality, S-C integrators are fully differential to maintain good rejection against noise coming from the substrate and to gain 3dB in S/N ratio.

Most of the power in a modulator is consumed by the opamps, which must be capable of driving capacitive loads and have a sufficiently low noise to maintain the S/N ratio of the modulator. The power consumption of the transconductance amplifier, with its simplified AC model shown in figure 2 is proportional to the equation (1) /2/:

$$P \propto kTBw(DR)^2 \frac{V_{GS} - V_{TH}}{V_{DD}} \qquad (1)$$

Where: k is Boltzman's constant, T is the absolute temperature, DR is the dynamic range, Bw is the bandwidth, V_{GS}–V_{TH} is the gate-source over-drive voltage and V_{DD} is the supply voltage.

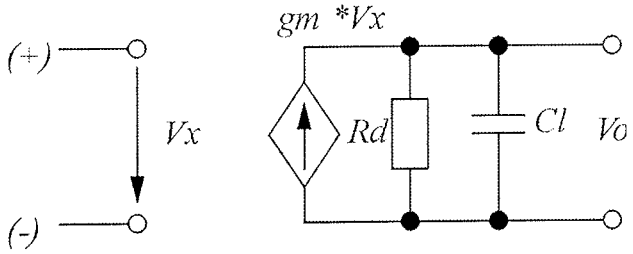

Figure 2: Simplified model of the opamp

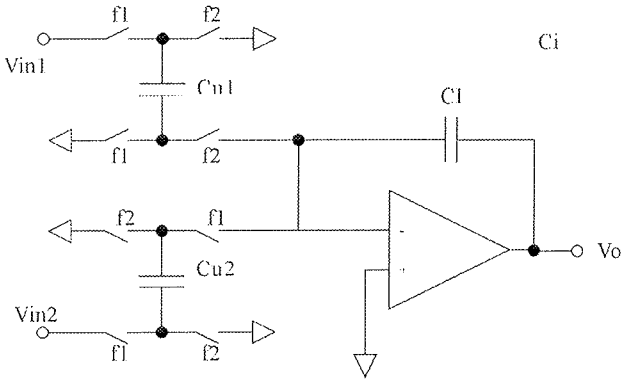

Figure 3: Single-ended S-C integrator

The capacitive loads of the opamps are defined by the coefficients of the loop-filter characteristics, stability constraints /1/ and by the thermal *kT/C* noise generated by the switched capacitors. For higher S/N-ratio requirements the noise must be smaller at the same supply voltage. This can be realised by increasing the unit (usually sampling) capacitance of the integrator; thus the capacitive load of the opamp is increased and more power is required to maintain the bandwidth (Bw). At the same time, for a larger S/N ratio a smaller thermal noise is required for the amplifier, which can only be realised by an increased current and/or increased area of the differential stage transistors. Fortunately only the first amplifier is critical for the low-pass modulator because all the other contributions are attenuated by **noise-transfer functions** of the loop filter.

The slew-rate must be larger than the maximum slope of the settling of v_{out} at maximum input signal to maintain linear settling behavior /3/. This requires the tail current of the differential stage to be greater than: $I_{tail} \geq S_r C_{load}$ /4/. If this limit is not respected the distortion and in-band noise will increase.

Chopping translates 1/f noise and the DC offset around multiples of the chopping frequency ($f_{ch} = f_s / 2$), which is later attenuated by a decimation filter together with shaped quantization noise. The only important parameter concerning 1/f noise is its corner frequency, usually between 10kHz and 100kHz, which in our case is out of the signal bandwidth after chopping.

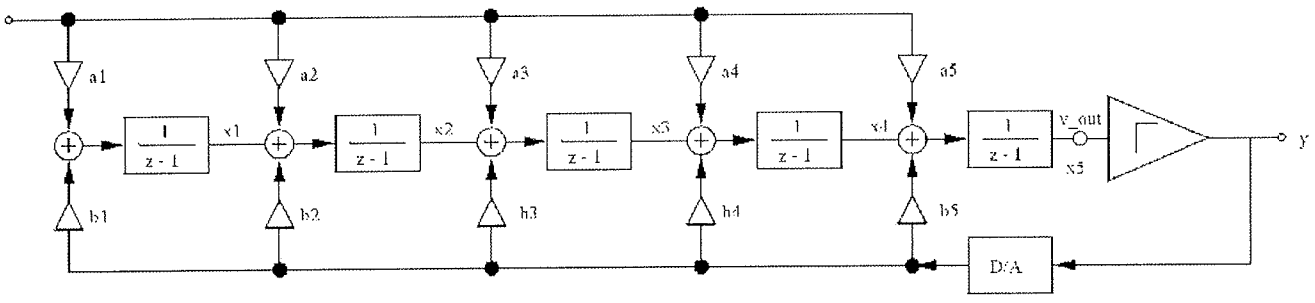

Figure 1: Simplified 5th-order modulator model

In any S-C circuit the coefficients are defined by capacitor ratios, and calculated from the loop-filter poles and zeroes. Each switched capacitor produces a noise power proportional to *kT/C*, where C is the capacitance, T is the absolute temperature and k is Boltzman's constant /4/. According to this model the noise power spectrum density is flat from 0 to fs/2. Every *kT/C* noise source contributes a certain amount of thermal noise which depends on the capacitance value and **noise-transfer functions** g_i. Different noise sources are uncorrelated, so noise contributions at the output of the loop filter can be added according to the equation (2). This is only possible for a simplified linear model of the whole modulator.

$$N_{loop}\left[\frac{W}{Hz}\right] = \frac{1}{f_N}\left[\sum_{i=1}^{i=M} N_{sc_i}\int_0^{f_N} g_{sc_i}^2(f)df + \sum_{j=1}^{j=N} N_{op_i}\int_0^{f_N} g_{op_j}^2(f)df\right] \quad (2)$$

Where: M is the number of S-C stages, N is the number of integrator stages, which is equal to the order of the loop filter, N_{sci} is the noise-power density of S-C stage i (independent of the frequency), N_{opi} is the noise-power density of the opamp j (independent of the frequency), $g_{sci}(f)$is the frequency-dependent **noise-transfer function** for each of the S-C stages, $g_{opj}(f)$ is the frequency dependent **noise-transfer function** for each opamp, N_{loop} is the noise-power density at the output of the loop filter and f_N is the Nyquist rate after decimation.

We can see that assuming uncorrelated noise sources the noise powers of the switched capacitor stages and opamps multiplied by the corresponding noise-transfer functions are added at the output of the loop filter. In addition to this the quantization noise power (which is assumed to be random) is also added. The summation is possible because at the beginning we assumed a linear model for the modulator, and so the theorem of superposition holds up to the output of the modulator. This simplified linear model is used just to get an insight into the behavior and is later replaced by a time-domain method.

1/f noise powers of all the integrator stages, except the first, are negligible because of the high-pass characteristics of the noise-transfer functions g_{opj} (figure 4).

Figure 5 shows AC noise-simulation results for the first opamp. Its thermal and 1/f noise components can be easily recognised. AC simulation results were taken as the input for the noise-generation procedure /5/ and then time-domain simulations were performed, including chopping by $f_s/2$. The 1/f noise component has been translated around $f_s/2$. The thermal noise at the output of the loop filter is composed of contributions from all S-C stages and opamps. The contributions are different for every S-C stage and opamp, and are dependent on the **noise-transfer functions** and the noise powers of the corresponding source; the total noise can be optimised by calculating appropriate capacitor sizes for the switched capacitors and the thermal noise of the opamps. The optimisation is achieved when the contributions at the output of the loop filter are the same.

Figure 6 shows the input-referred power-spectrum noise density of the first integrator: (a) with and (b) without chopping. It is thus possible to reduce capacitor sizes and noise requirements for the opamps, except for the first one. Unfortunately the unit capacitor size can not be made smaller than, for example, C_{unit}=0.3pF; the smallest dimension is constrained by the capacitor-ratio mismatch requirements, which are obtained from the stability and gain accuracy requirements of the modulator. The limit is a result of the synthesis procedure defined in /1/. The unit capacitor size of the first integrator must be bigger than $C_u \geq 15$pF to achieve the S/N ≥ 110dB at an oversampling ratio of D ≥ 256, taking into consideration all noise sources. The unit capacitor size in the following stages drops drastically (in the third and following stages the unit capacitor size is $C_u \geq 0.3$pF(see table on figure 9); the lower limit is calculated from the matching-accuracy parameters for a particular process and its requirements.

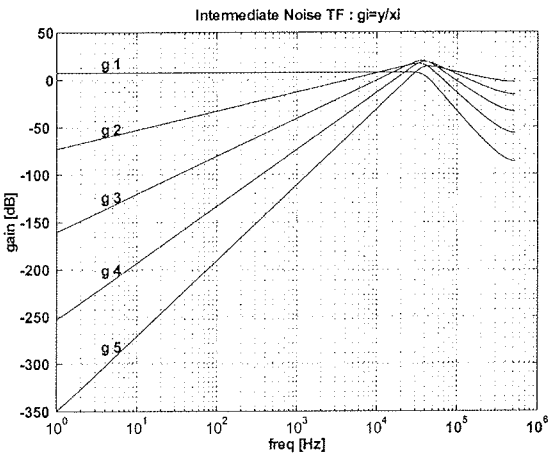

Figure 4: Noise transfer function of the 5th-order modulator

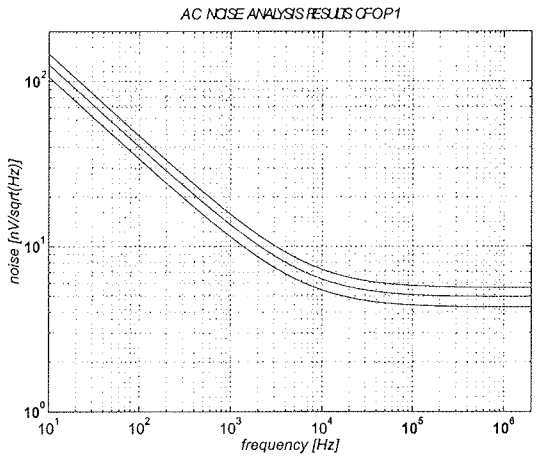

Figure 5: AC noise characteristics of the first opamp

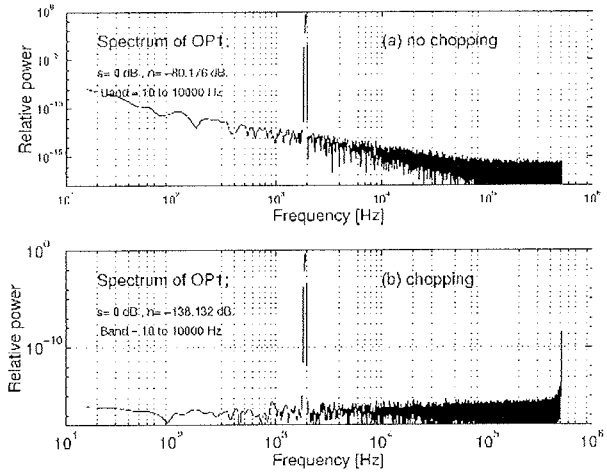

Figure 6: Spectrum at the output of the first integrator a) no chopping; b) with chopping

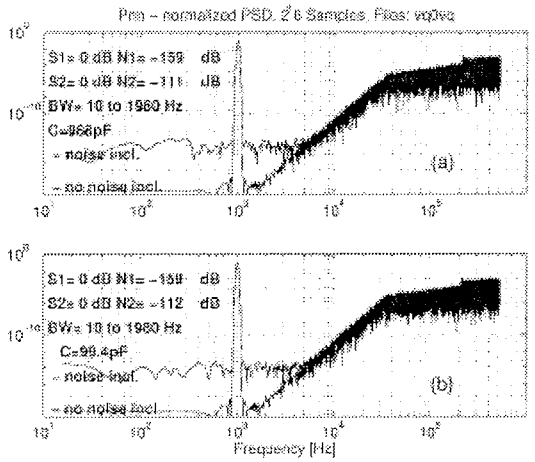

Figure 7: Spectrum of the bit-stream for 5th-order modulator a) no optimisation, no chopping; b) optimisation with chopping

Despite the fact that the loop filter is linear, the whole modulator is a highly non-linear device because of the comparator and 1 bit D/A converter. The quantization noise is assumed to be random but in reality it is not, and also the signal is not small as predicted by the AC small-signal-analysis method. For this reason the Monte-Carlo time-domain method is used in our simulations.

Figure 7 shows the noise simulation result for the 5th-order modulator: (a) before optimisation (without chopping) and (b) after optimisation (with chopping). The unit capacitor sizes and the thermal noise requirement for the opamps after optimisation if the S/N ratio of 110dB is required, are given in figure 9. By optimising capacitor sizes, the area of the capacitor arrays can be reduces by almost 10 times and the power consumption can be drastically reduced because the capacitive loads are lower, which is also shown on figure 8, which represents the layout of the realized modulator. It is evident that the area of the capacitor array is the biggest for the first integrator and than smaller for the second while the third and the following integrators have unit capacitor size of 0.3pF and thus need very small area.

Integ	Cu[pF]	ΣC[pF]	$V_n\left[\frac{nV}{\sqrt{Hz}}\right]$
1	15	66	≤9
2	1.2	24	≤85
3	0.3	4.4	≤1000
4	0.3	2.8	≤1000
5	0.3	2.0	≤1000

Figure 9: Table of capacitors before and after optimisation and opamp noise requirements

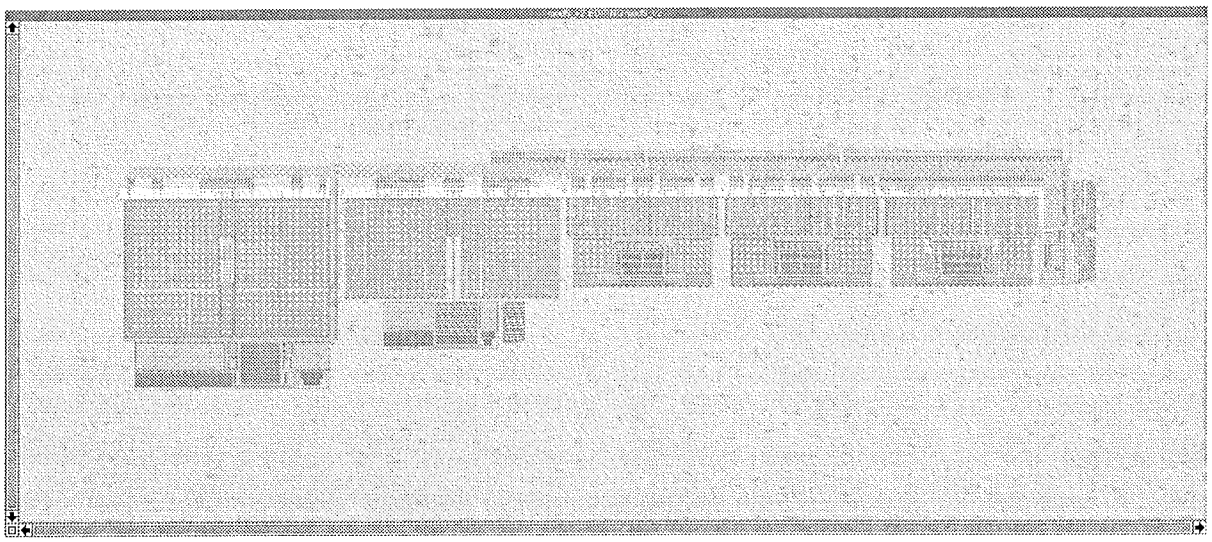

Figure 8: Layout of the realized 5th-order modulator

3. OPTIMIZATION ALGORITHM

The block diagram of a general Δ - Σ modulator is presented in figure 10, /3/. Its loop filter is generally an n^{th}-order FIR or IIR analog or sampled data filter. The behavior of the whole modulator is most generally and efficiently described by a combination of a linear time-domain multi-input single-output state-space description of the loop filter (state variables are outputs of the integrators) and of non-linear part, which describes single-bit or multi-bit quantizer (equation 3).

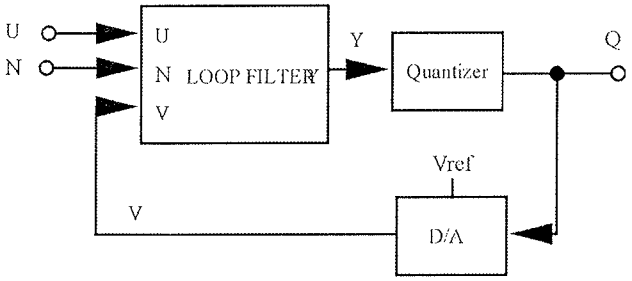

Figure 10: Block diagram of Δ-Σ modulator

$$x(n) = Ax(n-1) + Bv(n-1) + Nn(n-1)$$
$$y(n) = c^T x(n-1) + Dv(n-1)$$
$$v(n) = f_Q(y(n-1))V_{ref} \qquad (3)$$

The relation between the matrix elements and capacitors is defined for an arbitrary S-C loop filter in /5/. This model is improved by additional noise and linear and non-linear settling parameters. For convenience the simulation can be performed by turning on or off the chopping effects.
The optimisation algorithm gets its input data from the synthesis procedure. All the capacitor ratios are known, as is the architecture of the modulator. At the beginning the program assumes equal capacitors for all integrator stages. They are calculated from the S/N and oversampling-ratio requirements. The same thermal noise requirement for the opamps is taken as a basis. The time-domain Monte-Carlo simulation is then performed for each switched capacitor and each opamp in a modulator according to /5/. The contribution of each element is calculated in a band 0Hz to f_n and saved, then the capacitor sizes and the opamps' thermal noise parameters are adjusted according to these contributions in such a way that each noise source adds approximately the same contribution. The result is a table of unit capacitor sizes, the sum of all the capacitors for each integrator and the thermal noise requirements for the opamps. For our example the result is given in figure 9. We assumed that chopping of the first amplifier is performed, so the 1/f noise is translated around $f_s/2$ and later removed by the decimation filter. At the end a complete simulation of the modulator with optimised elements is performed. The result is presented in figure 7 (b).

4. CONCLUSIONS

A methodology for power-consumption optimisation for an S-C high order, high-resolution modulator is presented. The main reasons for power consumption are explained and a method to reduce the effects is proposed. An algorithm coded in MATLAB is developed and the results of an optimisation for a practical example of the 5^{th}-order single-bit Σ-Δ modulator are given. The required power consumptions of two modulators with equal architecture and different capacitors and opamps are compared. The power consumption for an optimised structure is reduced by more than 5 times compared to the non-optimised, while the capacitor array area is reduced by almost 10 times.

The advantage of the proposed algorithm is the speed and the effectiveness of the optimisation procedure and the possibility of performing the optimisation and the noise simulation in a reasonable time. It is only possible to use a simplified mathematical model for the circuits involved, which is the main limitation of the approach.

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