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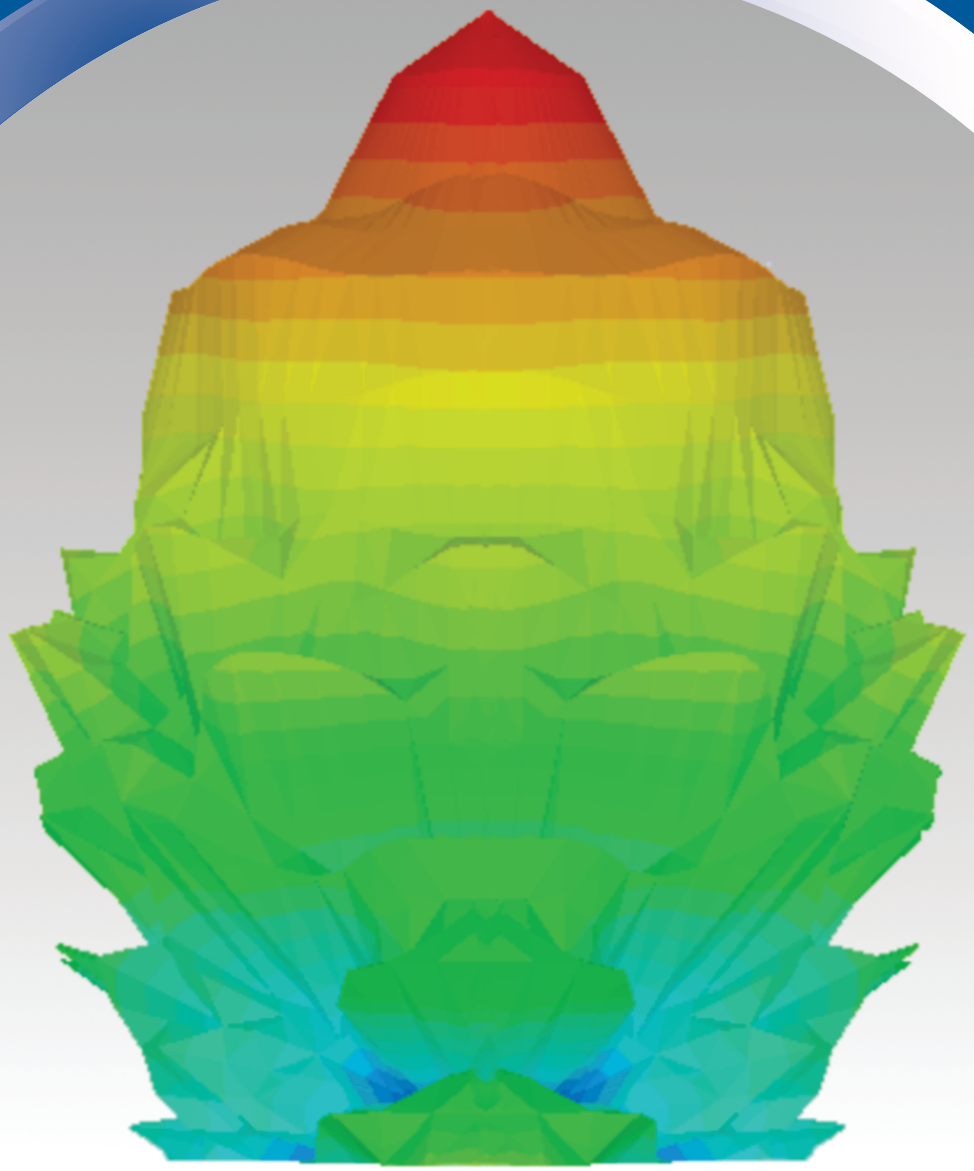

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Uredništvo Informacije MIDEM
MIDEM pri MIKROIKS
Stegne 11, 1521 Ljubljana, Slovenia
T. +386 (0)1 513 37 68
F. + 386 (0)1 513 37 71
E. info@midem-drustvo.si
www.midem-drustvo.si

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Coati Optimized Hybrid Neural Network for Efficient Network Slicing in 5 Generation Network

Ayya Dhurai Suceelal Sindhu[1], Chellappan Agees Kumar[2]

[1]Department of Electronics and Communication Engineering, Rajas Institute of Technology, Nagercoil, Tamil Nadu, India.
[2]Department of Electrical and Electronics Engineering, Arunachala College of Engineering for Women, Vellichanthai, India.

Abstract: Network slicing (NS) divides the physical network into many logical networks in order to support the variety of new applications with higher performance and flexibility needs. As a result of these applications, a massive amount of data has been generated with a huge number of mobile phones. Due to this, NS performance has been greatly impacted and extreme challenges have been created. To efficiently handle the challenges, this paper proposes a novel Optimal Network slice Classification Using Deep learning (ONE-CLOUD) technique, which integrates the Coati Optimization Algorithm (COA), GhostNet, and Gated Dilated Convolutional Neural Network (CNN). COA optimizes features such as user device type, packet loss ratio, and delay rate, employing GhostNet model, and Gated Dilated CNN for network slice classification. The proposed method classifies network slices into enhanced Mobile BroadBand (eMBB), Ultra-Reliable and Low-Latency Communications (URLLC), and massive Machine-Type Communications (mMTC). The effectiveness of the suggested approach has been evaluated using the 5G-SliciNdd dataset, utilizing evaluation criteria like accuracy, precision, recall, sensitivity, specificity, throughput, and reduced latency. The overall accuracy of the proposed method is 5.78%, 2.78% and 4.70% higher than the existing DQN-E2E, DRL, and AAA techniques respectively.

Keywords: Network Slicing; Deep learning; GhostNet; Gated Dilated CNN; Coati Optimization.

Coatijevo optimizirano hibridno nevronsko omrežje za učinkovito rezanje omrežja v omrežju petih generacij

Izvleček: Razrez omrežja (NS) razdeli fizično omrežje na več logičnih omrežij, da bi podprl različne nove aplikacije z večjo zmogljivostjo in prilagodljivostjo. Zaradi teh aplikacij se je z velikim številom mobilnih telefonov ustvarila ogromna količina podatkov. To je močno vplivalo na zmogljivost omrežja NS in povzročilo izjemne izzive. Za učinkovito obvladovanje teh izzivov članek predlaga novo tehniko optimalne klasifikacije omrežnih rezin z uporabo globokega učenja (ONE-CLOUD), ki združuje algoritem COA (Coati Optimization Algorithm), GhostNet in gated dilated konvolucijsko nevronsko mrežo (CNN). COA optimizira lastnosti, kot so vrsta uporabniške naprave, stopnja izgube paketov in stopnja zamude, pri čemer uporablja model GhostNet in Gated Dilated CNN za klasifikacijo omrežnih rezin. Predlagana metoda razvršča omrežne rezine v izboljšano mobilno širokopasovno omrežje (eMBB), izjemno zanesljive komunikacije z nizko zakasnitvijo (URLLC) in množične komunikacije strojnega tipa (mMTC). Učinkovitost predlaganega pristopa je bila ocenjena z uporabo podatkovne zbirke 5G-SliciNdd, pri čemer so bila uporabljena merila za ocenjevanje, kot so natančnost, točnost, priklic, občutljivost, specifičnost, prepustnost in zmanjšana zakasnitev. Skupna natančnost predlagane metode je za 5,78 %, 2,78 % in 4,70 % višja od obstoječih tehnik DQN-E2E, DRL in AAA.

Ključne besede: Rezanje omrežja; globoko učenje; GhostNet; Gated Dilated CNN; Coati optimizacija.

** Corresponding Author's e-mail: ageeskumar12@outlook.com*

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1 Introduction

Network slicing is an innovative architype for building system services that 5G networks have promoted with the growth of Software-Defined Networking (SDN) and Network Function Virtualization (NFV) [1]. 5G systems face immense demand due to mobile tech growth and app diversity. They must bolster Quality of Service (QoS) for multiple sectors like virtual reality, augmented reality, and remote healthcare, necessitating unprecedented advancement [2,3].

In 5G systems, NS defines autonomous, cohesive networks composed of a blend of dedicated and communal resource instances, including system equipment, radio spectrum, and VNF [4]. 5G system is designed to be a versatile, multi-service infrastructure that accommodates a diverse range of services, including eMBB, URLLC, and mMTC [5]. One of the utilization cases for future 5G, low-inactivity correspondence, is supposed to be upheld by MEC, a basic 5G improvement innovation [6]. It brings far-off systems administration, storage, and public distributed computing capacities nearer to the edge of the organization [7].

A network slice contains different organization components, for example, the terminal, access organization, center organization, and transport organization, which can be used by numerous administrators [8]. Unique in relation to other network slices, a network slice has devoted or potentially shared assets [9]. Portable network slice administrators will deliver diverse network slices bundled into one product for business clients with varying requirements, including a single network slice type catering to different verticals [10,11].

To effectively establish and manage network slices that meet QoS requirements amid changing conditions, handling extensive data swiftly proves challenging for humans [12,13]. The automatic method for managing network slices is critical because manual slice assignment is inefficient when dealing with the vast amount of data and dynamic conditions in 5G networks. Automatic classification enhances resource allocation by quickly adjusting to changing user demands and network conditions, thereby ensuring optimal performance without the delay and potential human error associated with custom manual assignments. It also supports the scalability required to manage the complexity and diversity of modern 5G applications, such as VR, AR, and remote healthcare. To address this issue a novel Optimal Network slice Classification Using Deep learning (ONE-CLOUD) technique, has been suggested. The main contributions are as follows:

- Packet loss ratio, delay rate, speed, device type, slice type, user bandwidth, and other attributes are gathered initially from the various users or devices in the 5G network.
- After collecting these features, Coati Optimization Algorithm (COA) is employed to select features from the collected attributes. Subsequently, the selected features are output in the form of optimal weighted features.
- The NS prediction is achieved by hybridizing GhostNet and Gated Dilated CNN through the AND operation, using the newly extracted weight optimized features. The output categorizes the network slices into three types: eMBB, mMTC, and URLLC.

The remainder of the research is described as follows: Section II examines the study using the literature as a guide. Section III thoroughly explains the suggested system. Section IV shows the result and discussion, whereas Section V shows the conclusion.

2 Literature survey

Several studies have utilized several techniques to NS in recent years. The following section covers a few of the current evaluation approaches along with their disadvantages are as follows:

In 2020, Li, T., et al., [14] suggested an E2E system slicing source distribution system that operates in multi-slice and multi-service scenarios, based on Deep Q-Networks (DQN). This system dynamically allocates resources to optimize by considering both the fundamental system slices and the radio access network slices. To the access side's ideal allocation approach, the typical access rate is enlarged by 9% for slices with delay limitations and by 5% for slices with rate constraints. In 2021, He, Y., et al., [15] recommended a multi-chain 5G NS facility value computation model to ascertain the characteristics of the NS service quality. The Cosi protocol features lower traffic consumption and a steady calculation cost as compared to other protocols. Ultimately, the practicality and effectiveness of the multi-chain 5G NS facility value computation architecture is demonstrated by security analysis and experimental outcomes.

In 2022, Suh, K., et al., [16] suggested a deep reinforcement learning (DRL)-based NS method to determine the source provision strategy that maximizes long-term amount in B5G systems while meeting QoS standards. The suggested method is shown to be efficient in addressing the coexistence of use cases in B5G environments and optimizing long-term throughput by numerical findings. In 2023, Dangi, R. and Lalwani, P., [17] suggested a successful hybrid learning algorithm-based network-slicing technique to enhance QoS and

maximize NS, the results produced by the suggested model are contrasted with those of current deep learning, machine learning, and optimization methods. It proves that the suggested model performed better than the others and identified the right network slices to provide top-notch services.

In 2023, Hu, Y., et al., [18] recommended neural network-based carrying technique. This paper provides a power 5G slicing service carrying mechanism based on neural networks. Through simulation verification, proved that the properties of electric power services are retrieved, classified, matched, and compliant with the 5G power NS. In 2023, Botez, R., et al., [19] suggested a modified A* algorithm Targeting services with low or extremely low latency requirements, it offers a better way to NS in 5G backhaul networks. According to experimental data, the suggested technique improves processing time by an order of magnitude. These outcomes show how well our method works in 5G backhaul networks to achieve URLLC. In 2024, Gomes, R., et al., [20] suggested the Artificial Algae Algorithm (AAA) as a 5G-specific NS solution for the VNE problem. The runtime presentation of AAA is independent of the number of simulated nodes this results in execution times that are up to ten times faster than DE and PSO when taking into account 30 nodes. The suggested method using AAA demonstrated an improvement of more than 60% in an implementation time that was ten epochs faster.

The aforementioned techniques have a number of issues with NS, including low accuracy, high Latency. To overcome these challenges a novel ONE-CLOUD technique has been proposed and discussed in next section.

3 Optimal network slice classification using deep learning

In this section, a novel Optimal Network slice Classification Using Deep learning (ONE-CLOUD) technique has been proposed to optimize resource utilization, and enhance the flexibility and efficiency of 5G and beyond networks. Initially, various attributes like bandwidth, device type, speed, slice type, packet loss ratio, and delay rate are gathered from different devices or users in the 5G network. These features undergo COA for selection, resulting in optimal weighted features. GhostNet is hy-

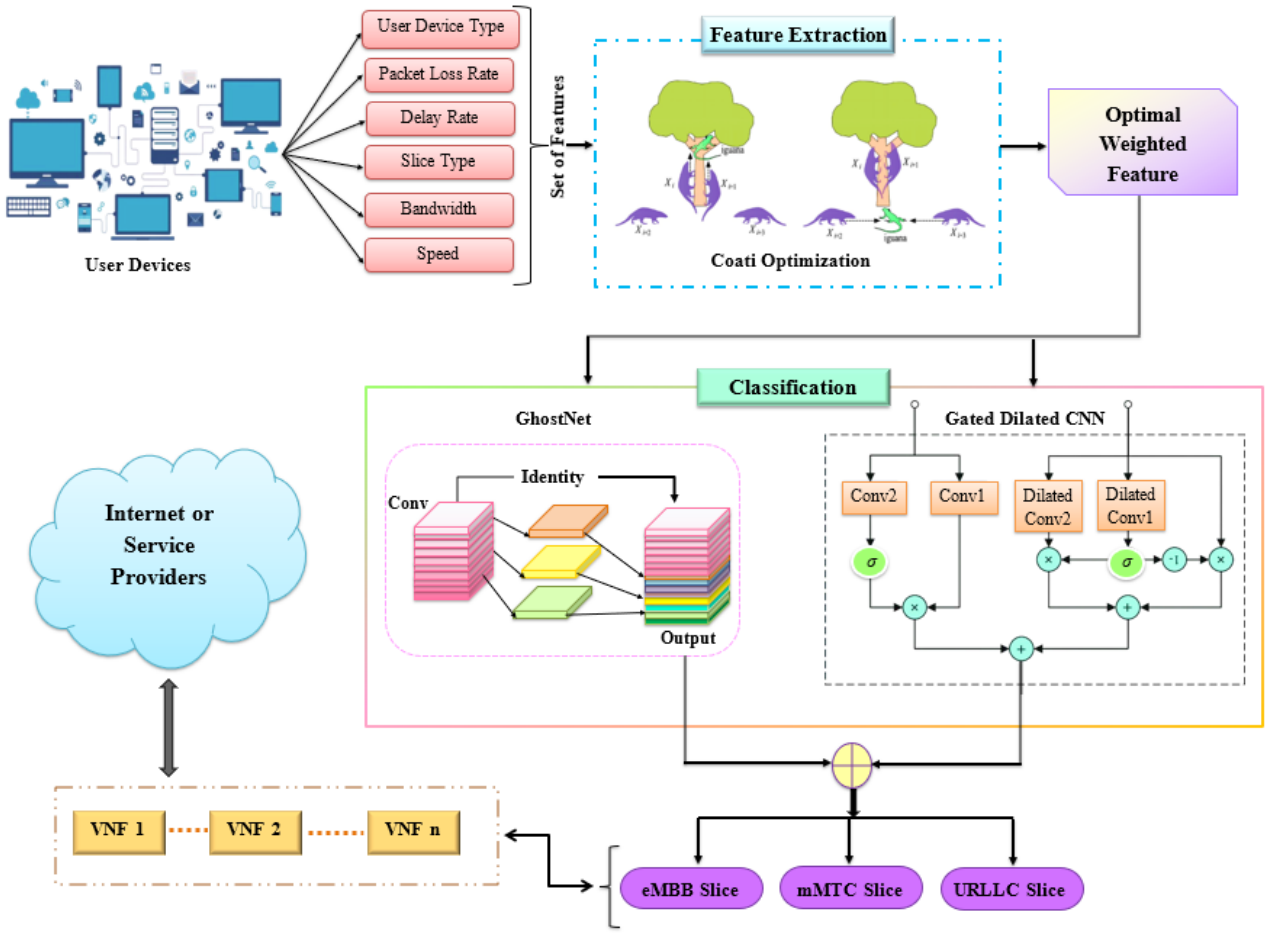


Figure 1: Overall workflow of Proposed ONE-CLOUD Method

bridized with Gated Dilated CNN using the AND operation to predict NS, leveraging the newly optimized features. The output classifies network slices into three types: eMBB, mMTC, and URLLC. The overall proposed ONE-CLOUD's workflow is depicted in Figure 1.

3.1 Feature extraction

In NS, feature extraction is the process of locating and obtaining pertinent data or attributes from the collection of features linked to each slice.

3.1.1 Feature Extraction

The COA [21] is a recently developed bioinspired optimization technique influenced by the natural behavior of coatis, presents a novel approach for feature extraction in NS. COA is based on the essential idea of imitating two important coatis' behaviors: (i) chasing and fighting iguanas and (ii) running away from predators. The COA is considered the most suitable technique for network slicing feature extraction since its bioinspired mechanisms mimic coatis' hunting and evasion behaviours. These behaviours enable more effective exploration and exploitation of the solution space. The COA is especially well-suited for challenges like network slicing, which demands for dynamic adaptability to changing conditions and limits, as it has proven to perform well in balancing global search capability and local search precision. When compared to other optimization algorithms like particle Swarm Optimization (PSO) and Cuckoo Search Optimization (CSO), COA's dual strategy allows for a more thorough exploration of potential solutions and reduces the probability of getting trapped in local optima. This COA behaviour facilitates more efficient resource distribution in complicated 5G scenarios. Performance measures like latency and throughput are improved by COA's ability to manage high-dimensional features such as device type, packet loss, and delay rates in network slicing of 5G. Because the mentioned algorithms might not provide the same balance between exploration and exploitation needed for network slice optimization, this helps in our decision to choose the COA algorithm. The coatis's original location in the hunt space is determined at random using Eqn. (1) at the initial stage of the COA implementation.

$$Z_j : Z_{ij} = LW_i + k \cdot \left(UP_i - LW_i\right), j = 1, 2, \ldots, m, \quad i = 1, 2, \ldots, n \tag{1}$$

where m is the amount of coatis, n is the amount of choice variables, k is a chance actual amount in the interlude 0,1, Z_j is the location of the jth coati in hunt space, and LW_i and UP_i are the inferior and superior bounds of the jth choice variable, correspondingly. The subsequent medium Z, known as the population matrix, is used to numerically depict the inhabitants in the COA which is given in Eqn (2)

$$Z = \begin{bmatrix} Z_1 \\ \vdots \\ Z_j \\ \vdots \\ Z_m \end{bmatrix}_{m \times n} = \begin{bmatrix} z_{1,1} & \cdots & z_{1,j} & \cdots & z_{1,m} \\ \vdots & \ddots & \vdots & \iddots & \vdots \\ z_{j,1} & \cdots & z_{j,i} & \cdots & z_{j,m} \\ \vdots & \iddots & \vdots & \ddots & \vdots \\ z_{m,1} & \cdots & z_{m,j} & \cdots & z_{m,n} \end{bmatrix}_{m \times n} \tag{2}$$

Two of coatis's natural activities are modeled in order to update coatis's position (feature solutions) in the COA. Among these behaviors are: i) The method used by coatis to attack iguanas and ii) The coatis' method of avoiding predators. Consequently, there are two steps to the updating of the COA population.

Phase 1: Strategy for hunting and attacking iguanas (exploration phase)

The first phase updates the coati population by simulating their iguana-attacking strategy. Some climb trees to scare iguanas, while others wait below. Half climb trees, and the rest wait for the iguana to drop. The mathematical simulation of the climbing coatis' location is expressed by Eqn. (3).

$$Z_j^{po1} : z_{ji}^{po1} = z_{ji} + k \cdot \left(Ig_i - I \cdot z_{j,i}\right), \quad for\, i = 1, 2, \ldots, \frac{m}{2} and\ j = 1, 2, \ldots, m. \tag{3}$$

Following its release to the ground, the iguana is placed arbitrarily throughout the search area. Eqn (4), (5).is used to approximate the random position that causes coatis on the pounded to transfer in the hunt space.

$$Ig^C : Ig_i^c = LW_i + k \cdot \left(UP_i - LW_i\right), i = 1, 2, \ldots., n \tag{4}$$

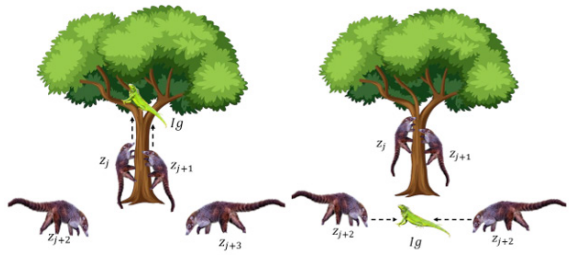
If each coati's new position increases the value of the objective function, it is permitted for the update process; if not, the coati stays in its previous place. Eqn (6) determines the simulated values of j = 1, 2, ... m, to which this update condition is applicable.

$$Z_j^{po1} : z_{j.i}^{po1} = \begin{cases} z_{j.i} + k \cdot \left(Ig_i - I \cdot z_{j,i}\right), E_{Ig^C} < E_j \\ z_{j.i} + k \cdot \left(z_{ji} - Ig_i^c\right), for\ j = \frac{m}{2} + 1, \frac{m}{2} + \ldots, m\ and\ i = 1, 2, \ldots n \end{cases} \tag{5}$$

$$z_j = \begin{cases} Z_j^{po1}, E_j^{po1} < E_j \\ z_j, \ else \end{cases} \quad (6)$$

where k is an arbitrary real number in the range [0, 1], *Jg* stands for the iguana's location in the hunt area, Z_j^{po1} is the original location estimated for the jth coati, $z_{j.i}^{po1}$ is its ith dimension, and E_j^{po1} is its neutral role worth. Jg_i is its ith measurement; Figure 2 shows the coati optimization algorithm's initial phase.

Figure 2: Coati Optimization Algorithm's initial phase: (a) Half of the coatis attacking the tree-dwelling iguana, and (b) the remaining coatis hunting the fallen iguana



Phase 2: The procedure of running away from an assailant (the exploitation stage)

The second phase updates coatis' search space position by modeling their natural behavior when facing predators. When attacked, coatis escape, strategically moving to a safe spot near their current position, showcasing COA's effective local search exploitation ability. To replicate this behavior, a random position is generated near each coati's location using Eqns. (7) and (8).

$$LW_i^{loc} = \frac{LW_i}{d}, UP_j^{loc} = \frac{UP_i}{d}, where\, d = 1, 2, \ldots, D \quad (7)$$

$$Z_j^{po2} : z_{j.i}^{po2} = z_{j.i} + (1 - 2k) \cdot \left(LW_i^{loc} + k \cdot \left(UP_i^{loc} - LW_i^{loc} \right) \right) \quad (8)$$

The recently computed position is deemed suitable if it enhances the objective function value, a condition simulated by employing Eqn. (9).

$$z_j = \begin{cases} Z_j^{po2}, E_j^{po2} < E_j \\ z_j, \ else \end{cases} \quad (9)$$

Here, Z_j^{po2} is the original location determined for the ith coati using another stage of COA; $z_{j.i}^{po1}$ is its ith dimension; E_j^{po2} is its impartial role value; k is a chance amount within the break [0, 1]; COA to help categorise the weight function, and optimal weight features are the output from the feature extraction process. The description of various features used in NS is given in Table 1.

Table 1: Overall summary of various features used in network slicing

Features	Feature Description
User device type	Properties describe characters and parts of a device
Packet loss rate	Percentage of packet vanish with respect to packet transmitted
Bandwidth	Fastest transfer of information rate possible with an internet connection
Delay rate	The time frame before an event occurs
Speed	Dimensions of location variation

3.2 Network slicing with the commitment of ghostnet and gated dilated CNN

Network slicing employs GhostNet and Gated Dilated CNN for efficient classification, enhancing performance and optimizing resource allocation in diverse network environments. The proposed technique combines the GhostNet and Gated Dilated CNN in network slicing, which addresses the challenges in classification, especially in handling large and distinct data from 5G network slices.

3.2.1 GhostNet Model

The fundamental unit of GhostNet is a stack of Ghost bottlenecks, of which the Ghost modules are the building hunks. The primary layer is a standard convolutional layer with 16 filters, followed by a series of Ghost bottlenecks with increasingly more channels. Using a convolutional layer and global average pooling, the feature maps are ultimately transformed into a feature vector for the final classification. The Optimal weighted features are given as input to the GhostNet. It is suitable for classifying network slices where resource constraints are common and its input is an optimal weighted feature. The convolution operation in a Ghost Module is given in Eqn (10):

$$q_i = \sum_{j \in I_i} v_j y_j \quad (10)$$

Here *p* be the input to the Ghost Module, and q be the output, *i* indexes the output channels, S_j is the set of indices corresponding to the output channels, V_j is the weight associated with input channel y_i and y_i is the input feature map. The Ghost Module introduces a ghost set G_i of randomly selected indices from the set I_i, and the convolution operation is given in Eqn (11)

$$q_i = \sum_{i \in G_i} v_j p_j \tag{11}$$

The ghost set G_i is dynamically sampled during each forward pass, leading to parameter-efficient training. With reference to intrinsic feature maps, $X' \in \mathbb{R}^{b' \times v' \times n}$ can be generated by Eqn (12), $j' \grave{o} \mathbb{R}^{e \times r \times r \times n}$ is the convolutional filters. Nevertheless, as Eqn (13) illustrates, partial convolutional operations are performed, and the remaining feature maps are produced via a linear operation.

$$X' = Y^* j' + b \tag{12}$$

$$X_{j,i} = \theta_{j,i}\left(X_j^{'}\right), \forall_j = 1,\ldots,n, i = 1,\ldots,h, \tag{13}$$

Where, $X_j^{'}$ is the j-th inherent feature map in X', $\theta_{j,i}$ the direct process for generating the i-th ghost feature map $X_{j,i}$. The outputs from all the ghost branches are aggregated to obtain the final output Q which is given in Eqn (14).

$$Q = \sum_{j=1}^{M} Z_j \tag{14}$$

Where, is the total number of ghost breaches. As an improvement, we used the AND operation to optimize the weight function after receiving the output Q from GhostNet. GhostNet model is highly efficient in extracting features from high-dimensional data with fewer parameters, making it suitable for real-time and resource-constrained environments such as 5G networks. GhostNet's ability to generate additional feature maps through simple linear transformations helps in reducing the computational burden while retaining critical information for classifying network slices (eMBB, mMTC, URLLC). Utilizing fewer convolutional operations ensures that the model is lightweight, making it ideal for environments with limited computational power.

3.2.2 Gated dilated CNN model

Gated Dilated Convolutional Neural Networks are a type of DL architecture that combines the concepts of dilated convolutions and gated units to capture long-range dependencies in input data. Dilated convolution that introduces gaps between the weights. Eqn (15) provides the expression for the dilated convolution operation on a 1D sequence.

$$\left(a \times f\right)\left(j\right) = \sum_{s=1}^{S} a\left(j + dr \cdot s\right) \cdot f\left(s\right) \tag{15}$$

where indicates the convolution process, is the dilation rate, is the filter size, is the filter or kernal, and is the input sequence. Two gates are used in the gating mechanism: the reset gate (rg) and the update gate (ug). Eqn (16) & (17) is used to calculate the update gate (z) and reset gate (r) using sigmoid activation functions.

$$ug = \mu\left(V_{ug} \times \left[a, h_{s-1}\right]\right) \tag{16}$$

$$rg = \mu\left(V_{rg} \times \left[a, h_{s-1}\right]\right) \tag{17}$$

The Contender concealed state (is then figured using reset gate, which is given in the Eqn (18). Finally, the actual concealed state (is figured Using the update gate to combine the candidate hidden state with the current hidden state, which is given in Eqn (19)

$$\widetilde{h_s} = \tan h\left(V_h \times \left[rg \odot h_{s-1}, a\right]\right) \tag{18}$$

$$h_s = \left(1 - ug\right) \odot h_{s-1} + ug \odot h_s \tag{19}$$

Here, V_{ug} , V_{rg} , and V_h are weight matrices, is the sigmoid activation function, $\odot$ indicates multiplication of elements, and tanh is the hyperbolic tangent activation function. If L describes the output of the last layer before the softmax activation, the final output (O_p) can be computed as in Eqn (20)

$$O_p = softmax\left(L\right) \tag{20}$$

Finally, the output of two models is merged by AND operation and classifies the NS types into 3 classes such as eMBB, mMTC and URLLC. The Gated Dilated CNN is integrated to capture long-range dependencies in the data. 5G networks often generate complex temporal sequences, and traditional CNNs may fail to exploit these patterns fully. The dilated convolutions in the Gated Dilated CNN allow the model to handle long-range dependencies efficiently by expanding the receptive field without increasing the number of parameters. This mechanism is particularly effective in classifying diverse network slices, as it captures both short-term and long-term dependencies in the data, which is crucial for optimizing network performance in real time. By combining GhostNet and Gated Dilated CNN through the AND operation, the proposed ONE-CLOUD technique ensures optimal feature extraction and classification, addressing both the computational efficiency and the complexity of network slicing classification.

4 Results and discussion

The proposed ONE-CLOUD technique's simulation outcomes are obtainable in this section to assess the

efficiency of the proposed technique. Performance scrutiny and execution of the suggested 5G NS were conducted in MATLAB.

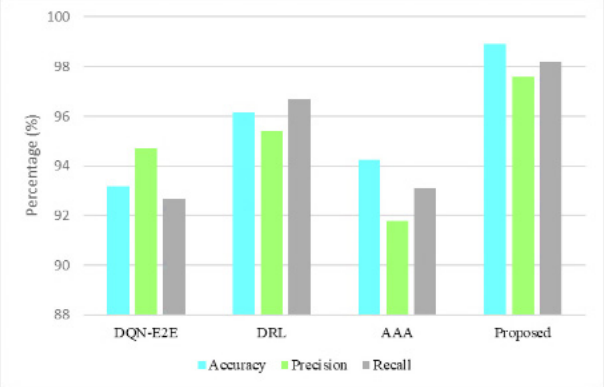


Figure 3: Overall Performance comparison in terms of accuracy, precision, and recall

The effectiveness of the technique was assessed using the 5G-SliciNdd dataset. The dataset used in this work has been split into training, validation, and testing sets, which has been divided into 80%, 10%, and 10% of the entire dataset. The dataset split has been done randomly which ensures that each class is represented proportionally in each subset to prevent class imbalance. The training set has been used to train the network, validation set has been used to fine tune the hyperparameters of the network, and the test set is used to test the network and its performance in NS. With this splitting, we can ensure that the network can reduce overfitting of training data which results in generalization. Additionally, the separate test set will help in evaluating the generalizability and robustness of proposed ONE-CLOUD technique. This ensures that the results state the actual performance of the network on test data.

The proposed ONE-CLOUD model's effectiveness is contrasted with DQN-E2E [14], DRL [16], and AAA [20] in terms F1-score, accuracy, sensitivity, specificity, precision, throughput and latency. In Figure 3, a comprehensive evaluation of overall performance is presented, comparing accuracy, precision, and recall of NS against existing DQN-E2E, DRL, and AAA techniques. The assessment provides insights into how effectively the proposed ONE-CLOUD NS approach performs in comparison to established methods. This comparison aids in gauging the efficacy of NS in comparison to existing techniques.

Figures 4(a) and 4(b) show the training and test data sets, as well as the accuracy and loss curves. The Accuracy Curve in Subfigure (a) shows how the model's correctness upsurges on both the training and authentication sets during the course of training epochs. Both

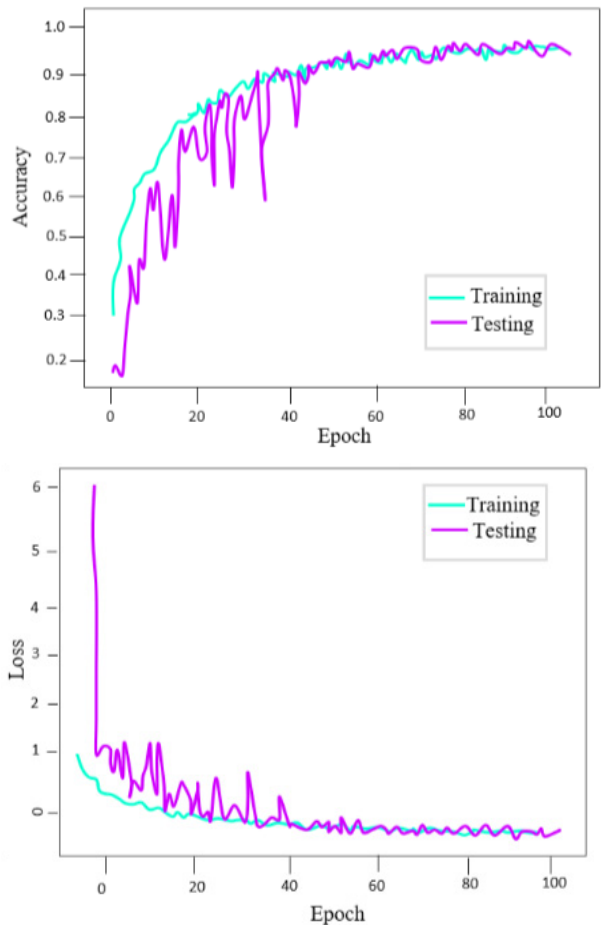


Figure 4: (a) Accuracy Curve; (b) Loss Curve

training and validation losses tend to be downward, according to the Loss Curve in Subfigure (b).

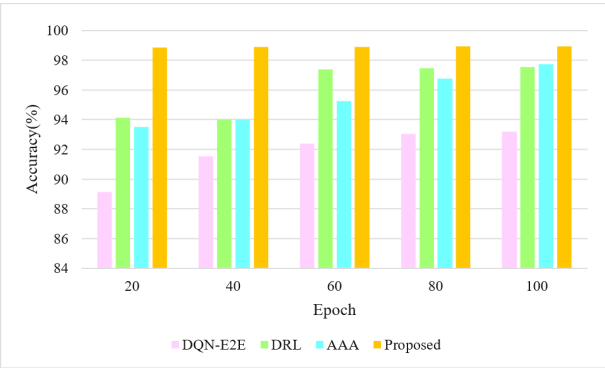


Figure 5: Comparison in terms of accuracy

Figure 5 illustrates a focused comparison in terms of accuracy with 100 epochs between the proposed ONE-CLOUD technique and existing DQN-E2E, DRL, and AAA methods.

The graph offers a visual representation of how well the new approach performs in terms of correctness

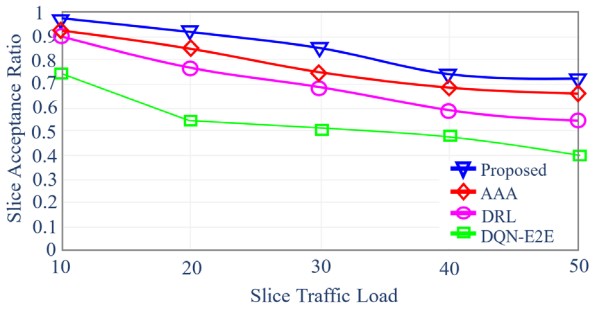


Figure 6: Slice acceptance ratio with variable slice traffic load

compared to established techniques. Comparing the accuracy of the suggested ONE-CLOUD method to the current DQN-E2E, DRL, and AAA procedures, it is 5.78%, 2.78%, and 4.70% higher.

In Figure 6, the slice receiving ratio is presented alongside variable slice traffic loads, linking the presentation of the proposed ONE-CLOUD technique with existing DQN-E2E, DRL, and AAA methods. This figure allows for an assessment of how well the proposed method adapts to varying levels of network demand compared to established techniques.

Figure 7: Revenue-to-cost ratio with variable slice traffic load

Figure 7 illustrates the revenue-to-cost ratio in relation to mutable share traffic loads for both the existing DQN-E2E, DRL, and AAA methods and the proposed ONE-CLOUD technique for NS. A higher revenue-to-cost ratio indicates improved cost-effectiveness, highlighting the potential benefits of implementing the proposed NS method in comparison to the conventional system

Figure 8 presents a comparative analysis of sensitivity and specificity between the existing system and the proposed ONE-CLOUD method for NS. The specificity and sensitivity of the proposed ONE-CLOUD method are 3.90%, 9.25%, 12.44% and 5.02%, 4.18%, 6.27% greater than the existing AAA, DRL and DQN-E2E techniques respectively.

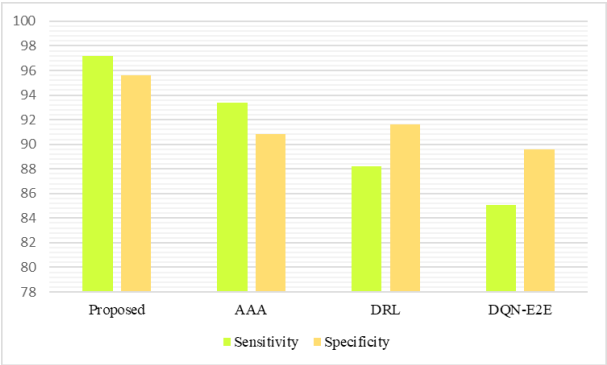


Figure 8: Comparison in terms of sensitivity and specificity

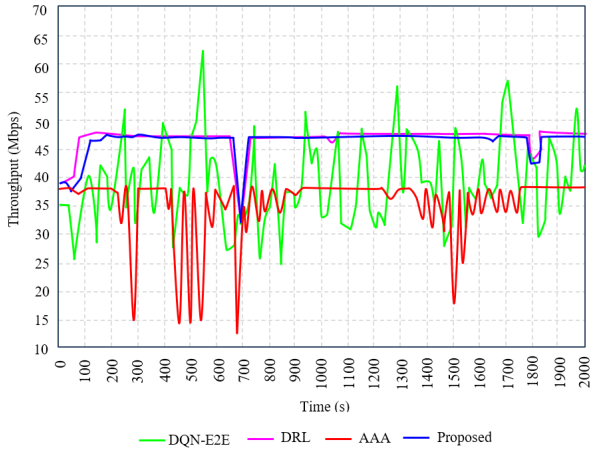


Figure 9: Comparison in terms of throughput

Figure 9 presents a comparison of throughput between the existing AAA, DRL and DQN-E2E techniques and the proposed ONE-CLOUD method for NS. This graph enables an assessment of how the proposed NS method performs in terms of data transmission efficacy associated to the existing system, providing valuable insights into the potential improvements in throughput offered by the proposed ONE-CLOUD approach.

Figure 10 illustrates a latency comparison between the proposed ONE-CLOUD method and existing AAA, DRL and DQN-E2E techniques. The proposed method dem-

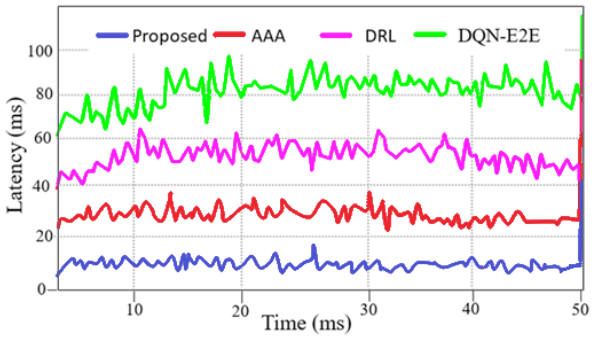


Figure 10: Comparison in terms of latency

onstrates superior latency performance compared to current methods. This comparison offers valued visions into the effectiveness and efficiency of the proposed NS approach, showcasing its potential to minimize communication delays.

5 Conclusion

In this paper, a novel Optimal NEtwork slice CLassificatiOn Using Deep learning (ONE-CLOUD) technique has been proposed to optimize resource utilization, and enhance the flexibility and efficiency of 5G and beyond networks. The COA-based feature extraction optimizes device attributes. These features enhance GhostNet and Gated Dilated CNN models, combined via AND operation, boosting accuracy in classifying eMBB, mMTC, and URLLC network slices. The evaluation of the proposed ONE-CLOUD method, conducted using the 5G-SliciNdd dataset. The proposed ONE-CLOUD method outperforms existing techniques, in terms of precision, accuracy, latency, sensitivity, specificity, throughput, and recall. The overall accuracy of the proposed ONE-CLOUD method is 5.78%, 2.78% and 4.70% higher than the existing DQN-E2E, DRL, and AAA techniques respectively. Future work could explore the scalability and applicability of the proposed technique in large-scale network environments, as well as its adaptability to emerging communication technologies beyond the scope of 5G.

6 Acknowledgments

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7 Conflict of interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

8 References

1. A.A. Barakabitze, A. Ahmad, R. Mijumbi, A. Hines, "5G network slicing using SDN and NFV: A survey of taxonomy, architectures and future challenges," Comput. Networks, vol. 167, pp. 106984, 2020, https://doi.org/10.1016/j.comnet.2019.106984.
2. A. Ahilan, M.A. Rejula, S.N.Kumar, and B.M. Kumar, "Virtual Reality Sensor Based IoT Embedded System for Stress Diagnosis," IEEE Sensors Journal. 2023.
3. S. Zafar, N. Iftekhar, A.Yadav, A. Ahilan, S.N. Kumar, and A. Jeyam, "An IoT method for telemedicine: Lossless medical image compression using local adaptive blocks," IEEE Sensors Journal, vol. 22, no. 15, pp.15345-15352, 2022.
4. Dr. S. Reeba Rex, Dr. T. Pravin Rose, S. Amudaria, "Real Time Remote Monitoring Via Horse Head Optimization Deep Learning NetworK," International Journal of Data Science and Artificial Intelligence, vol. 02, no.02, pp. 42-47, 2024.
5. A. Karimidehkordi, "Multi-Service Radio Resource Management for 5G Networks". 2019.
6. P. Mor, S.B. Bajaj, "Enabling Technologies and Architecture for 5G-Enabled IoT," Blockchain for 5G-Enabled IoT: The new wave for Industrial Automation, pp. 223-259, 2021, https://doi.org/10.1007/978-3-030-67490-8_9.
7. W. Yu, F. Liang, X. He, W.G. Hatcher, C. Lu, J. Lin, X. Yang, "A survey on the edge computing for the Internet of Things," IEEE access, vol. 6, pp. 6900-6919, 2017. https://doi.org/10.1109/ACCESS.2017.2778504.
8. X. Zhou, R. Li, T. Chen, H. Zhang, "Network slicing as a service: enabling enterprises' own software-defined cellular networks," IEEE Commun. Mag., vol. 54, no. 7, pp. 146-153, 2016, https://doi.org/10.1109/MCOM.2016.7509393.
9. R. Li, Z. Zhao, X. Zhou, G. Ding, Y. Chen, Z. Wang, H. Zhang, "Intelligent 5G: When cellular networks meet artificial intelligence," IEEE Wireless Commun.., vol. 24, no. 5, pp.175-183, 2017. https://doi.org/10.1109/MWC.2017.1600304WC.
10. P. Govender, "Dynamic quality of service enabled network slicing for fifth generation core network (Doctoral dissertation, University of Johannesburg)". 2023.
11. T. Irshad, "Design and implementation of a testbed for network slicing". 2018.
12. F. Firouzi, B. Farahani, and A. Marinšek, "The convergence and interplay of edge, fog, and cloud in the AI-driven Internet of Things (IoT)," Inf. Syst., vol. 107, pp.101840, 2022, https://doi.org/10.1016/j.is.2021.101840.
13. M. El Rajab, L. Yang, A. "Shami, Zero-touch networks: Towards next-generation network automation," Computer Networks, pp.110294, 2024, https://doi.org/10.1016/j.comnet.2024.110294.
14. T. Li, X. Zhu, and X. Liu, "An end-to-end network slicing algorithm based on deep Q-learning for 5G network," IEEE Access, vol. 8, pp. 122229-122240, 2020, https://doi.org/10.1109/ACCESS.2020.3006502.

15. Y. He, C. Zhang, B. Wu, Y. Yang, K. Xiao, H. Li, "Cross-chain trusted service quality computing scheme for multi-chain model-based 5g network slicing slam," IEEE Internet Things J. 2021. https://doi.org/10.1109/JIOT.2021.3132388
16. K. Suh, S. Kim, Y. Ahn, S. Kim, H. Ju, and B. Shim, "Deep reinforcement learning-based network slicing for beyond 5G," IEEE Access, vol. 10, pp.7384-7395, 2022, https://doi.org/10.1109/ACCESS.2022.3141789.
17. R. Dangi, P. Lalwani, "Harris Hawks optimization-based hybrid deep learning model for efficient network slicing in 5G network," Cluster Comput., pp.1-15, 2023, https://doi.org/10.1007/s10586-022-03960-1.
18. Y. Hu, L. Gong, X. Li, H. Li, R. Zhang, R. Gu, "A Carrying Method for 5G Network Slicing in Smart Grid Communication Services Based on Neural Network," Future Internet, vol. 15, no. 7, pp.247, 2023, https://doi.org/10.3390/fi15070247.
19. R. Botez, A.G. Pasca, A.T. Sferle, I.A. Ivanciu, V. Dobrota, "Efficient Network Slicing with SDN and Heuristic Algorithm for Low Latency Services in 5G/B5G Networks," Sens., vol. 23, no. 13, pp.6053, 2023, https://doi.org/10.3390/s23136053.
20. R. Gomes, D. Vieira, M.B. Pereira, M.F. de Castro, "Artificial algae optimization for Virtual Network Embedding problems in 5G network slicing scenarios," Expert Syst. Appl., vol. 239, pp.122436, 2024, https://doi.org/10.1016/j.eswa.2023.122436.
21. M. Dehghani, Z. Montazeri, E. Trojovská, and P. Trojovský, "Coati Optimization Algorithm: A new bio-inspired metaheuristic algorithm for solving optimization problems," Knowledge-Based Systems, vol. 259, pp.110011, 2023. ž https://doi.org/10.1016/j.knosys.2022.110011

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Design and Efficiency Enhancement of Polar Encoder Based on Universal Logic Gates Utilizing QCA Technology

Liu Dongdong, Ji Tiantian*

School of Computer and Information Engineering, Fuyang Normal University, Fuyang, China

Abstract: Nano-scale circuit designs can be implemented using a transistor-free method called Quantum-dot Cellular Automata (QCA). QCA circuits are denser, quicker, and need less energy than the commonly used transistor-based technologies. In QCA technology, like in many other technologies, it is crucial to send and receive information securely. The QCA-based polar encoder circuit is one of the circuits that makes this possible. There are some drawbacks to the polar encoders circuit in QCA technology, and a strong design with high speed and low cell count is also strongly required. This paper presents three new and largely used circuits for QCA-based polar encoders. The G2 (2-bit) design is a single-layer structure with 16 cells only and a total area of 0.02 μm2, while its delay is 0.5 clock cycles. A suggested G4 design would be 121 cells, requiring a total size of 0.16 μm2 with a delay of 1.50 clock cycles. The G8 design has a delay of 3.5 clock cycles at a total size of 0.8 μm2 with 564 cells. All designs are simulated using QCADesigner. The tests and the simulations prove the supremacy of the proposed circuits over the best previous circuits in terms of speed, number of cells, and space used for implementation.

Keywords: Polar Encoder, Quantum-Dot, Cellular Automata, QCADesigner, Nano Communication. Nano Electronic.

Oblikovanje in povečanje učinkovitosti polarnega dekodirnika na osnovi univerzalnih logičnih vrat z uporabo tehnologije QCA

Izvleček: Zasnove vezij v nanometrskem merilu je mogoče izvesti z metodo brez tranzistorjev, imenovano kvantni celični avtomati (QCA). Vezja QCA so gostejša, hitrejša in potrebujejo manj energije kot običajno uporabljene tehnologije, ki temeljijo na tranzistorjih. Pri tehnologiji QCA je tako kot pri številnih drugih tehnologijah ključnega pomena varno pošiljanje in sprejemanje informacij. Polarno kodirno vezje, ki temelji na QCA, je eno od vezij, ki to omogoča. Vezje polarnih kodirnikov v QCA-tehnologiji ima nekaj pomanjkljivosti ter potrebuje močno zasnovo z visoko hitrostjo in majhnim številom celic. V tem članku so predstavljena tri nova in večinoma uporabljena vezja za polarne kodirnike, ki temeljijo na QCA. Zasnova G2 (2-bitna) je enoplastna struktura s 16 celicami in skupno površino 0,02 μm2, njena zakasnitev pa je 0,5 takta. Predlagana zasnova G4 bi imela 121 celic, za kar bi potrebovali skupno površino 0,16 μm2 , zakasnitev pa bi bila 1,50 takta. Zasnova G8 ima zakasnitev 3,5 takta pri skupni velikosti 0,8 μm2 in 564 celicami. Vse zasnove so simulirane s programom QCADesigner. Testi in simulacije dokazujejo premoč predlaganih vezij nad najboljšimi predhodnimi vezji glede hitrosti, števila celic in prostora, porabljenega za izvedbo.

Ključne besede: polarni kodirnik, kvantne točke, mobilni avtomat, QCADesigner, nano povezljivost, nanoelektronski

** Corresponding Author's e-mail: cheenxf@163.com*

1 Introduction

Broadly, research has been the hallmark of years gone by in finding a proper alternative to transistor-based technologies [1-3]. Because transistor-based technologies have reached their physical limit, they result in many pathologies, such as short-channel effects,

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design variance, and heat. One of the most promising alternatives is Quantum-dot Cellular Automata (*QCA*) technology [4, 5]. These are due to the remarkable features and benefits of QCA, such as rapid switch speed, operation frequency in the terahertz rate, high device density, and low power dissipation [6, 7]. It is because of the fantastic characteristics and advantages of QCA, including its rapid switch speed, terahertz operating frequency, extremely high device density, and very low power dissipation [7, 8]. A number of different implementations, including atoms, molecules, and semiconductors that have been studied based on electrostatic interactions, have been proposed to replicate bistable and local QCA paradigm interactions. In addition, several experimental gadgets have been built and successfully tested [9]. Due to the novelty of this technology, many researchers have presented different designs for different circuits, such as encoder circuits, adders, calculating units, subtractors, and polar code circuits [10]. Polar codes significantly reduce block error probability, with an asymptotic error exponent upper bound. However, the number of studies on polar encoders is rare, and there is a need to design faster circuits with fewer cells and optimal space consumption [11]. Polar encoders are relatively new, having been first introduced in *2009* by *E. Arikan [12]*. A polar encoder is one that has *K* inputs and *N* outputs (*N,K*). Its fundamental premise is channel polarization to separate the noiseless channel from the noisy channels [12].

In QCA technology, the role of a polar encoder has not been taken so serious, and there was a need to present new circuits that realize the issue of a polar encoder as a critical aspect of this technology [13]. Ensuring reliable data transmission and securing the information of the users are very crucial. This demands presenting the function of a polar encoder in this technology. QCA technology will be able to increase its potential in establishing a safe transfer of data so that the important information of the users can be protected by highlighting the design of new circuits and appreciating the worth of this topic. A polar encoder is to be designed in order to meet the growing demand of reliable data transmission and strong protection of information in QCA technology. It means that with respect to QCA technology, there are problems in the polar encoder circuit, data transfer, and reliable information protection; apparently, what is demanded is sturdy designs at fast speeds and few cells. In such a paper, the authors have proposed low-cell QCA-based polar encoder circuit architecture at the nano-scale level. The designs are simple, adaptable, and realized in a single layer. The primary structural component of the circuit is the majority gate. The suggested circuits are built and tested using *QCADesigner-E*, a program for modeling QCA circuits. The important contributions are as follows:

I. Offering the designs of single layer *2-bit, 4-bit, and 8-bit* polar encoders in QCA;
II. Assessing the size, latency, cell counts, and logic gate counts of suggested circuits;
III. Evaluating the quantum cost and energy dissipation of suggested circuits.

As a result, a novel polar encoder circuit design and implementation were given in the current research. Section 2 gives an overview of earlier efforts as well as the history of QCA. Section 3 presents the suggested polar encoder circuit's design, implementation, and simulation results. Section 4 provides comparison and evaluation charts and tables for significant QCA parameters, and Section 5 presents this article's conclusions.

2 Backgrounds and related work

2.1 Preliminaries for QCA

Recently, nano-designs have gotten much attention in many fields [14-16]. QCA provides a new idea in nano-scale. The most fundamental unit of a QCA component is a cell. In a cell, there are two free electrons and four free quantum dots. Two free electrons are allowed to travel freely amongst the four quantum dots and, through electrostatic interaction, can achieve two stable states [17]. The binary *"1"* and binary *"0"* can be represented by the two stable states. Figure 1 depicts the fundamental components of the QCA technology [18]. Normal cells and rotated cells are two categories of QCA cells. The 2 stable states of QCA cells are shown in Figure 1 (a).). Each cell in a mathematical sense can be described by polarization *P*, whereby (Here *p1, p2, p3, and p4* will be the probabilities of the electron across the dots.):

$$p = \frac{(p1 + p3) - (p2 + p4)}{(p1 + p2 + p3 + p4)} \quad (1)$$

Figure 1 (b) shows a three-input majority gate, and Figure 1 (c) depicts an inverter [11]. The inverter can reverse an input signal, whereas the 3-input majority gate can produce an output based on majority rules [19]. We are aware of four different QCA models. There are numerous theories for each of the four schemes. Both magnetic and molecular QCA cells can operate steadily at room temperature [20]. The majority gate is regarded as the basic logic gate in QCA, defined by the function:

$$\text{Majority}(Input_1, Input_2, Input_3) = (Input_1 \times Input_2) + (Input_1 \times Input_3) + (Input_2 \times Input_3) \quad (2)$$

This function provides the majority value of between inputs $Input_1$, $Input_2$, and $Input_3$. The inverter is a simple gate that makes an inversion of the input state:

$$Inverter\ (IN) = (\overline{Out}) \quad (3)$$

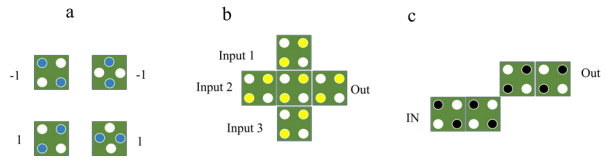

Figure 1: QCA Assemblies; (a) primary cells, (b) majority gate, (c) inverter gate.

The architecture of the QCA circuit heavily relies on the QCA clock mechanism. First off, it supplies the required power to QCA circuits [21]. Second, it aids in data transmission pipelining. In QCA, there are four clock zones (*Zones 0-3*), each of which is driven by a four-phase clock signal [22]. Each clock zone has one of four phase states, including *Switch, Hold, Release, and Relax*, using ($\pi/2$) phase-shifted signals. The *Switch* state marks the start of computation, whereas the *Hold* state maintains polarization. The QCA cell is ready for the following computation during the *Release and Relax* stages [17].

2.1 Related works

In this section, important encoder circuits in QCA technology are examined.

Salimzadeh, et al. [23] proposed the design and implementation of a fault-tolerant priority encoder. In this study, a fault-tolerant priority encoder was designed, with a primary focus on providing a new fault-tolerant majority gate. Simulations were conducted using the QCADesigner software *V. 2.0.3*, revealing improved performance of the proposed structure. The problem with this method is the use of many cells and its low speed.

Also, Safoev, et al. [24] proposed a QCA-based priority encoder using the Toffoli gate. In the paper, it is suggested that a reversible priority encoder be designed, which has played a key role in addressing encoding and decoding processes. This research pays attention to QCA technology as a new technology for implementing reversible priority encoder circuits. This paper presents a new architecture for a reversible encoder. A low-cost design for the Toffoli gate is presented to facilitate the implementation of the proposed reversible encoder circuit. The circuit has been tested with the QCADesigner simulation tool. The result shows it to have a correct operation. However, the problem in this circuit is using the Toffoli gate since this gate is an old gate with a low speed for generating the output.

Das and De [25] provided a QCA-based circuit for a polar encoder. Using a bottom-up approach, they designed a QCA-based polar encoder circuit that consumes low power at the nano-scale level. They also explored the impact of stuck-at-fault errors on generating valid polar codes and proposed test vectors to ensure proper circuit implementation. Notably, the proposed circuit boasts low energy dissipation, fast circuit latency, and a small device area. The results confirmed the circuit's accuracy. However, this design suffers from inadequate performance and excessive cell usage.

Finally, Ahmed, et al. [26] proposed a design of a QCA-based cost-efficient polar encoder. The use of polar encoders in secure communication was discussed extensively in this article, leading to the creation of a polar encoder utilizing QCA technology. This encoder had an area of *0.1944* μm^2 on one layer and contained *600* cells. The total area for implementing this circuit was *0.7225* μm^2. Due to the large number of cells, and also very high hardware implementation space, this design cannot be used practically, and the unavailability of easy access to the inputs and outputs is one of the important limitations of this circuit.

3 Polar encoder design

The polar encoder represents a variety of fault correction codes in communication systems that increase the reliability of data transmission. These codes are of great importance and a must due to their tremendous superiority in transferring data without faults and their performance superiority compared with other methods. In the polar encoder method of data encryption, information is divided into several blocks that are then mapped to a set of binary symbols. This set of symbols then combines the data with varying levels of confidence [27]. Finally, the data is transmitted through communication channels, and after receiving the information, the receiver extracts and sorts the data using a polar decoder. These codes increase speed, reduce complexity, and provide better security in public communication channels. In general, it can be supposed that polar encoders and decoders are very promising solutions for safe communications at the nano level and in complex circuits, and with new designs, their use will increase.

Figure 2 shows the schematic or block diagram of a polar decoder and encoder for communication at the nano level. The schematic diagram includes various sections such as input and output values, communication channel, polar decoder section, and polar encoder section. In this schematic, to create a polar encoder, several *GN* bits are selected as information input, and the rest of the inputs remain fixed. The frozen bits can

be assigned a value of either *"1" or "0"*, but usually, they are fixed at *"0"*.

A straightforward recursive rule defines G_N. G_2 is created initially, then G_4 is formed by concatenating G_2 units, and G_8 is constructed by concatenating G_2 and G_4 units. To construct G_2N, N copies of G_2 and two copies of G_N are utilized. The *XOR* gate is the fundamental building block of polar encoder structures, specifically G_2, G_4, and G_8. G_2 requires only one *XOR* gate to produce the output, which has two inputs and two outputs. Table 1 presents the truth table for this gate. The design of G_2 in QCA is shown in Figure 3, and it is created and simulated in the *QCADesigner* tool. The design is a single-layer structure with only *16* cells and a total area of *0.02 μm²*, and it has a latency of *0.5 clock cycles*.

Table 1: The truth table for QCA-based G2 circuit

I_1	I_2	O_1	O_2
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	1

The implemented G_2 circuit is used to create the G_4 circuit and this circuit is shown in Figure 4. This circuit uses 121 quantum cells in an area of 0.16 μm² and has a latency of 1.50 clock cycles. It is also worth mentioning that this circuit has *4 inputs* and *4 outputs*. As shown in Figure 5, the G_8 circuit has *8 inputs and 8 outputs* and is implemented by combining *4, G2* circuits and *2, G4* circuits. Also, according to Figure 6, the G_8 circuit is designed and implemented in one layer based on QCA technology and has accessible and convenient inputs and outputs. With a total of *564* cells, the proposed design occupies a total area of *0.8* μm² and has a latency of *3.5 clock cycles*.

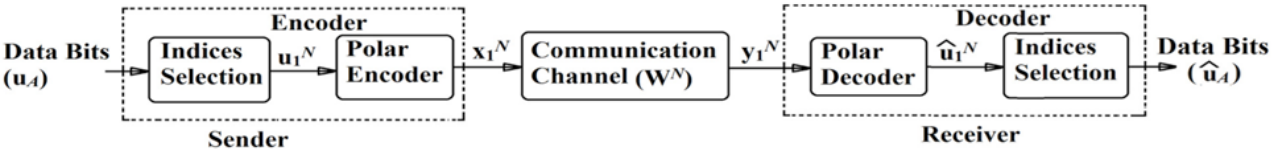

Figure 2: Data communication with Polar encoder [26]

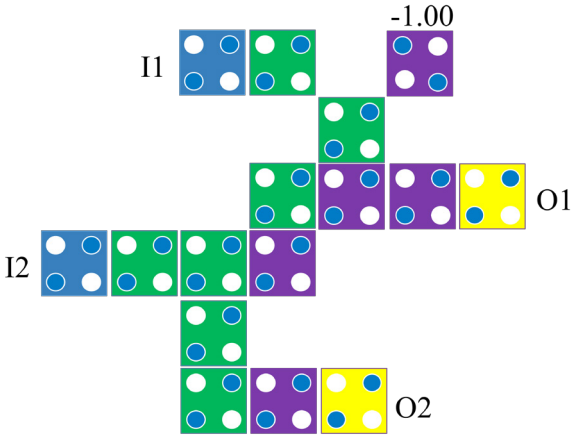

Figure 3: The proposed QCA design for the G_2 circuit

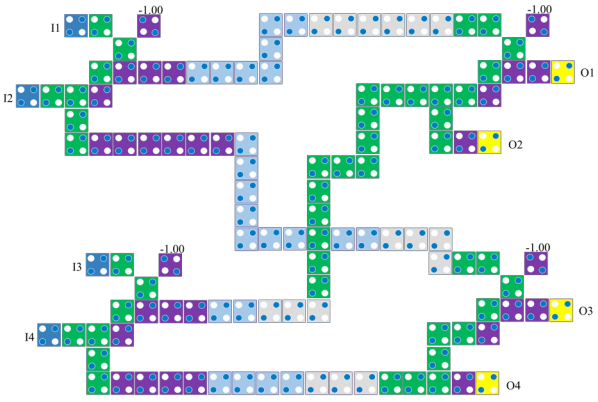

Figure 4: The proposed QCA-based G_4 circuit

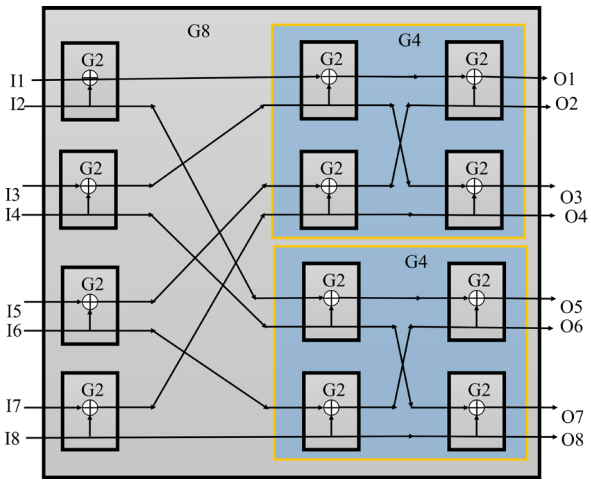

Figure 5: The applied G_8 block diagram

The (*8,4*) polar encoder has the same structure as G_8, but I_1, I_2, I_3, *and* I_5 are held at logic *"0"* as frozen bits. Figure 7 illustrates the QCA layout for this structure, and its performance parameters are identical to those of the G_8 structure. Consequently, this configuration includes four information bits (I_4, I_6, I_7, *and* I_8) and eight output bits. The design consists of a total of *560* cells, occupies an area of *0.8 μm²*, and has a latency of *3.5 clock cycles*.

The G_2 polar encoder circuit with QCA uses the least number of cells implementing a *XOR* gate that is necessary in

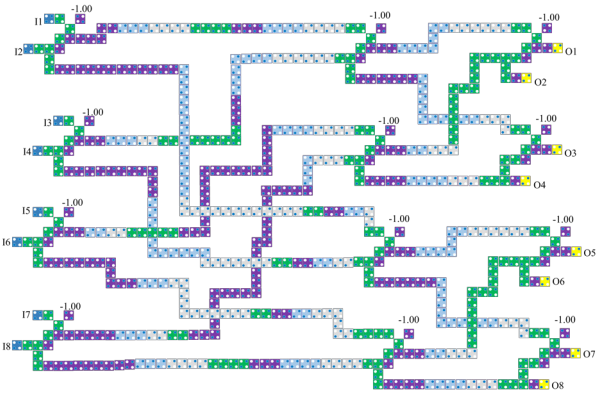

Figure 6: The proposed QCA implementation of G_8

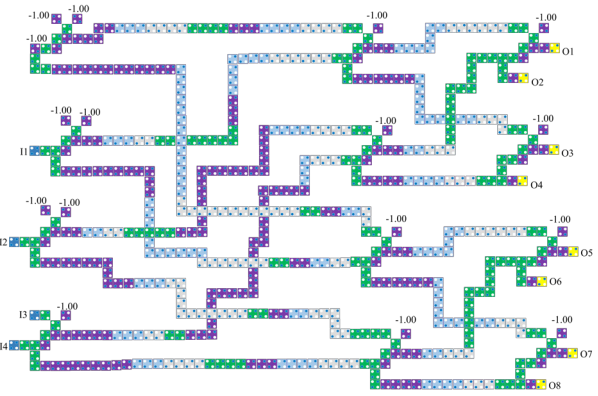

Figure 7: The proposed QCA implementation of the proposed (8, 4) polar encoder

encoding operations. The output of the G_2 polar encoder circuit can thus be expressed for this *XOR* gate as:

$$XOR(I_1,1_2)=I_1 \oplus I_2 \quad (4)$$

The G_4 *and* G_8 circuits are cascaded from the basic G_2 units. For the output in case of G_4, it can be given by:

$$G_4(I_1, I_2, I_3, \text{and } I_4) = XOR(XOR(I_1,1_2), XOR(I_3,1_4)) \quad (5)$$

The G_8 circuit extends this approach, with four G_2 circuits and two G_4 circuits:

$$G_8(I_1, I_2, I_3, I_4, I_5, I_6, I_7, \text{and } I_8) = \\ = XOR(G_4(I_1, I_2, I_3, \text{and } I_4), G4(I_5, I_6, I_7, \text{and } I_8)) \quad (6)$$

4 Discussions

The coherence vector and bistable vector characteristics are utilized in the simulation using the QCADesigner [18]. As described in [4], the simulation considers various parameters for coherence vector-based analysis:

1. Cell height and width: 18nm
2. Operating temperature: *1 K*
3. Relaxation time: *1.00e-015* s
4. Time step: *1.00e-016* s
5. Total simulation time: *7.00e-011* s
6. High clock: *9.80e-22J*
7. Low clock: *3.80e-23J*
8. The clock's amplitude factor: *2.0000*
9. Permittivity relative: *12.900*
10. The impact radius: *80 nm*
11. Layer separation: *11.5 nm*

Figure 8 displays the simulation waveform, which enables effortless verification of the structure's functionality. Take, for instance, the scenario where I_1 has a value of *0* and I_2 has a value of 1. Under these conditions, the outputs will be $O_1 = 1$ *and* $O_2 = 1$, with a delay of *0.5 clock cycles*. This outcome can be cross-checked with the information in Table 1. The simulation waveform facilitates the equal ease of verification of all input and output combinations.

Figure 9 illustrates the simulation waveform, which can be used to examine the simulation results. Suppose inputs I_1, I_2, I_3, *and* I_4 have values of 1, *0, 0, and 1*, respectively. In that case, the outputs will be $O_1 = 0$, $O_2 = 1$, $O_3 = 1$, *and* $O_4 = 1$. The same combination of outputs can be seen in the simulation waveform depicted in Figure 9. The output is generated with a latency of 1.*5 clock cycles*. All the input and output combinations can be validated similarly using the simulation waveform.

Figures 10 and 11 depict simulation waveforms for the proposed G_8 and polar encoder, respectively. The simulation results include all possible inputs for both the execution circuit and the expected output, demonstrating the circuits' accuracy. Likewise, by examining the simulation waveform, all input and output combinations are confirmed.

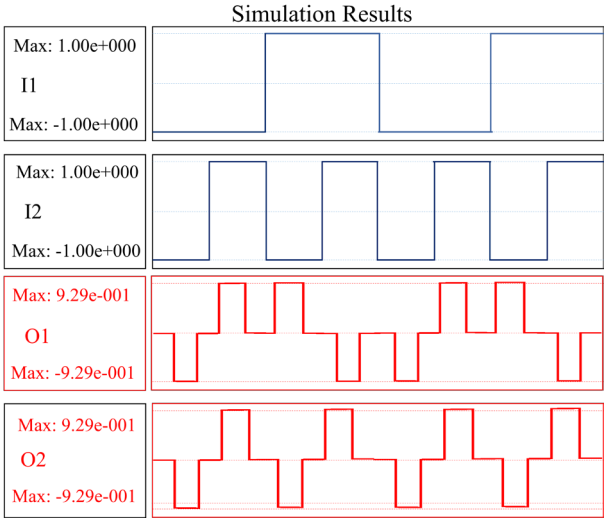

Figure 8: The simulation results of G_2 design

Table 2 provides a complete comparison of the proposed circuits and the best previous circuits in terms of cell count, area, and delay. The G_2 circuit of the new implementation has 16 cells with an area of 0.02 μm² and produces the final output after 0.5 clock cycles. Also, the G4 circuit of the new implementation has 121 cells with an area of 0.16 μm² and produces the final output after 1.5 clock cycles. It should be noted that the G8 circuit has 564 cells with an area of 0.8 μm² and produces the final output after 3.5 clock cycles. Finally, the (8,4) polar encoder circuit has 560 quantum cells and is implemented in the space of 0.8 μm2. According to the values of Table 2 and also the complete Figure 12, it can be seen that the circuits provided in all compared cases have provided the best performance and results.

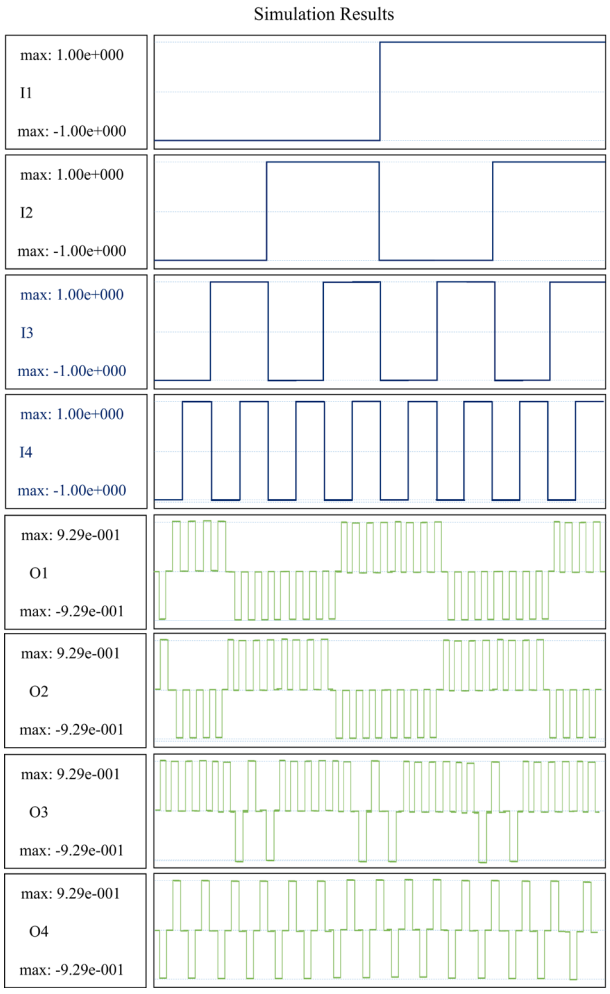

Figure 9: The simulation results of G_4 design

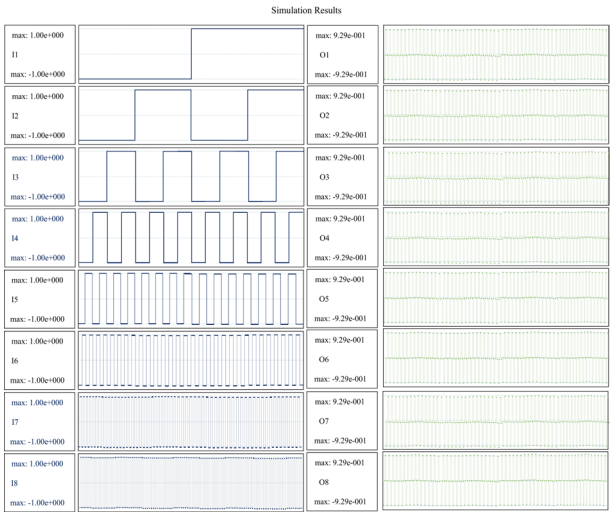

Figure 10: The simulation results for QCA-based G_8 circuit

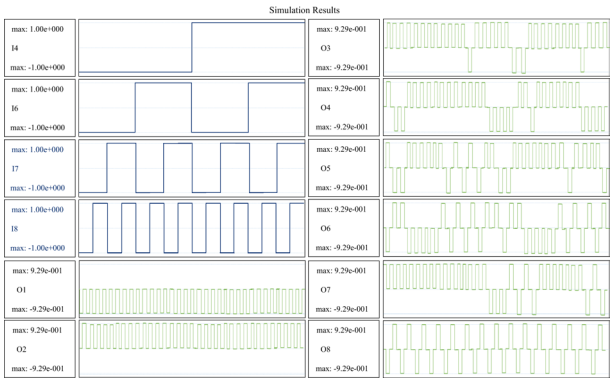

Figure 11: The simulation outcomes of QCA-based polar encoder

Table 2: Comparison between the proposed design and other state-of-the-arts

Designs	Area (μm²)	Cells	Latency
Proposed G_2	0.02	16	0.5
Proposed G_4	0.16	121	1.5
Proposed G_8	0.8	564	3.5
Proposed G $(_{8,4})$	0.8	560	3.5
Ahmed, et al. [26] G_2	0.016	21	0.5
Ahmed, et al. [26] G_4	0.132	133	1.75
Ahmed, et al. [26] G_8	0.7225	600	3.75
Ahmed, et al. [26] $(_{8,4})$	0.7255	600	3.75
Das and De [25] G_2	0.077	69	1.25
Das and De [25] G_{45}	0.456	322	3.25
Das and De [25] G_8	1.915	1188	6.25
Das and De [25] $(_{8,4})$	1.915	1188	6.25

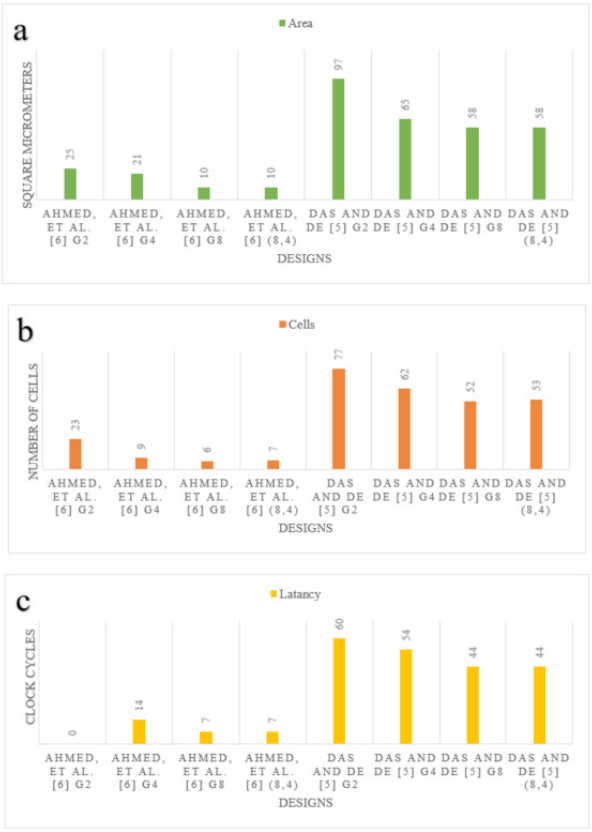

Figure 12: Chart of percentage improvement and comparison of QCA-based polar designs. (a) area, (b) number of cells, and (c) delay.

5 Conclusion

Emerging nanotechnology, known as *QCA,* has several noteworthy benefits, including reduced power dissipation, increased circuit density, and quicker speed. This technology offers increased component density, faster processing, and less latency with reduced power consumption. As a result, QCA technology is a wise option for nano-scale computing. It has also been determined that QCA is suitable for constructing various nano-communication devices and circuits. An essential and integral component of the QCA logic circuit family is communication. However, for producing secure communications, the polar encoding circuit is quite popular and frequently utilized. This circuit can improve data transmission efficiency and accuracy, opening up new possibilities for environmental monitoring and medical engineering applications. As a result, circuits for *2, 4, and 8* polar encoders have been devised and implemented in the paper. Only *16* cells, covering *0.02 μm²*, and a delay of 0.5 clock cycles were utilized in the G2 circuit; *121* cells, covering *0.16 μm²*, and a latency of *1.50 clock cycles* were employed in the G4 circuit. In addition, the suggested G_8 circuit has a delay of *3.5 clock cycles*, *564* cells, and an area of *0.8 μm²*. Lastly, the *0.8 μm²* size, *3.5 clock cycle* delay, and *560* cells were employed in the suggested (*8,4*) polar encoder design. QCADesigner *version 2.0.3* software was used to implement these new circuits and compare them to the best existing circuits. The results showed the superiority of the circuits presented in cell count, area, and latency compared to the most recent circuits. Future works utilizing the concepts provided here might involve implementing bigger, more bit-intensive circuits through the use of QCA-based polar encoders and decoders, as well as more optimum circuit construction.

Data Availability: *The article contains all the data.*

Conflict of interest: *No conflict of interest is found amongst the authors.*

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7 References

1. C. Constantinescu, "Trends and challenges in VLSI circuit reliability," *IEEE micro,* vol. 23, no. 4, pp. 14-19, 2003, https://doi.org/10.1109/MM.2003.1225959.
2. A. Yan *et al.*, "Nonvolatile latch designs with node-upset tolerance and recovery using magnetic tunnel junctions and CMOS," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* 2023.
3. A. Yan *et al.*, "Two double-node-upset-hardened flip-flop designs for high-performance applications," *IEEE Transactions on Emerging Topics in Computing,* 2023.
4. W. Li *et al.*, "Charge States, Triple Points, and Quadruple Points in an InAs Nanowire Triple Quantum Dot Revealed by an Integrated Charge Sensor," *Advanced Quantum Technologies,* p. 2200158, 2023, https://doi.org/10.1002/qute.202200158.
5. A. Yan *et al.*, "Designs of BCD adder based on excess-3 code in quantum-dot cellular automata," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 70, no. 6, pp. 2256-2260, 2023.
6. M. T. Bohr and I. A. Young, "CMOS scaling trends and beyond," *IEEE Micro,* vol. 37, no. 6, pp. 20-29, 2017, https://doi.org/10.1109/MM.2017.4241347.

7 S.-S. Ahmadpour *et al.*, "Design and implementation of a nano-scale high-speed multiplier for signal processing applications," *Nano Communication Networks,* vol. 41, p. 100523, 2024.

8. S. F. Naz, S. Riyaz, and V. K. Sharma, "A Review of QCA Nanotechnology as an Alternate to CMOS," *Current Nanoscience,* vol. 18, no. 1, pp. 18-30, 2022, https://doi.org/10.2174/1573413717666210301111822.

9. Y. Li, D. Sang, M. Li, X. Li, T. Wang, and B. O. Mohammed, "A New Quantum-Based Building Block for Designing a Nano-Circuit with Lower Complexity," *Informacije MIDEM,* vol. 53, no. 2, pp. 57-64, 2023, https://doi.org/10.33180/10.33180/InfMIDEM2023.201.

10. Y. Wang and S. Faghani, "A New Efficient Nanodesign of Composite Gate Based on Quantum Dot Cellular Automata," *Nano,* p. 2250103, 2022, https://doi.org/10.1142/S179329202250103X.

11 H. Wu, S. Jiang, N. J. Navimipour, and S. Seyedi, "Quantum-based serial-parallel multiplier circuit using an efficient nano-scale serial adder," *Informacije MIDEM,* vol. 54, no. 2, 2024.

12. E. Arikan, "Channel polarization: A method for constructing capacity-achieving codes for symmetric binary-input memoryless channels," *IEEE Transactions on information Theory,* vol. 55, no. 7, pp. 3051-3073, 2009, https://doi.org/10.1109/TIT.2009.2021379.

13. J. Timler and C. S. Lent, "Power gain and dissipation in quantum-dot cellular automata," *journal of applied physics,* vol. 91, no. 2, pp. 823-831, 2002, https://doi.org/10.1063/1.1421217.

14. J. Kang *et al.*, "Parallel nanosheet arrays for industrial oxygen production," *Journal of the American Chemical Society,* vol. 145, no. 46, pp. 25143-25149, 2023.

15. H. Zhang *et al.*, "Recent advances in nanofiber-based flexible transparent electrodes," *International Journal of Extreme Manufacturing,* vol. 5, no. 3, p. 032005, 2023.

16. H. Li *et al.*, "Flexible transparent electromagnetic interference shielding films with silver mesh fabricated using electric-field-driven microscale 3D printing," *Optics & Laser Technology,* vol. 148, p. 107717, 2022.

17. M. Raj, L. Gopalakrishnan, and S. B. Ko, "Reliable SRAM using NAND-NOR gate in beyond-CMOS QCA technology," *IET Computers & Digital Techniques,* vol. 15, no. 3, pp. 202-213, 2021, https://doi.org/10.1049/cdt2.12012.

18. S. Seyedi and B. Pourghebleh, "A new design for 4-bit RCA using quantum cellular automata technology," *Optical and Quantum Electronics,* vol. 55, no. 1, p. 11, 2023.

19. D. T. Stephen, H. P. Nautrup, J. Bermejo-Vega, J. Eisert, and R. Raussendorf, "Subsystem symmetries, quantum cellular automata, and computational phases of quantum matter," *Quantum,* vol. 3, p. 142, 2019, https://doi.org/10.22331/q-2019-05-20-142.

20. S. Seyedi, B. Pourghebleh, and N. Jafari Navimipour, "A new coplanar design of a 4-bit ripple carry adder based on quantum-dot cellular automata technology," *IET Circuits, Devices & Systems,* vol. 16, no. 1, pp. 64-70, 2022, https://doi.org/10.1049/cds2.12083.

21. S. S. Gu *et al.*, "Characterization of a Triple Quantum Dot via an On-chip Microwave Resonator," *Advanced Quantum Technologies,* vol. 5, no. 2, p. 2100104, 2022, https://doi.org/10.1002/qute.202100104.

22. T. Farrelly, "A review of quantum cellular automata," *Quantum,* vol. 4, p. 368, 2020, https://doi.org/10.22331/q-2020-11-30-368.

23. F. Salimzadeh, E. Safarpoor, and S. R. Heikalabad, "Designing and implementing a fault-tolerant priority encoder in QCA nanotechnology," *ECS Journal of Solid State Science and Technology,* vol. 10, no. 6, p. 063004, 2021, https://doi.org/10.1149/2162-8777/ac0118.

24. N. Safoev, G. Abdukhalil, and K. A. Abdisalomovich, "QCA based Priority Encoder using Toffoli gate," in *2020 IEEE 14th International Conference on Application of Information and Communication Technologies (AICT)*, 2020: IEEE, pp. 1-4, https://doi.org/10.1109/AICT50176.2020.9368637.

25. J. C. Das and D. De, "QCA based design of Polar encoder circuit for nano communication network," *Nano communication networks,* vol. 18, pp. 82-92, 2018, https://doi.org/10.1016/j.nancom.2018.08.004.

26. S. Ahmed, S. F. Naz, and S. M. Bhat, "Design of quantum-dot cellular automata technology based cost-efficient polar encoder for nanocommunication systems," *International Journal of Communication Systems,* vol. 33, no. 18, p. e4630, 2020, https://doi.org/10.1002/dac.4630.

27. X. Che, B. Ip, and Z. Yan, "Field test of multi-hop image sensing network prototype on a city-wide scale," *Digital Communications and Networks,* vol. 5, no. 2, pp. 131-137, 2019, https://doi.org/10.1016/j.dcan.2017.07.002.

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Introducing EIS Circuit Elements in SPICE Simulator Environment

Matevž Kunaver

Faculty of Electrical Engineering, University of Ljubljana, Ljubljana, Slovenia

Abstract: This study introduces hypothetical circuit elements, specifically the Constant Phase Element (CPE) and Zeroth-Order Approximation of a RC Circuit (ZARC), into the SPICE circuit simulation environment to enhance Electrochemical Impedance Spectroscopy (EIS) analysis. EIS, a critical method for understanding electrochemical processes in fields such as fuel cell analysis, corrosion studies, and biomaterials, relies on fitting measured impedance curves to Equivalent Electrical Circuit (EEC) models. However, existing approaches require expert knowledge and significant mathematical effort, limiting automation. By integrating CPE and ZARC into SPICE, this work bridges the gap between EIS analysis and advanced automatic circuit design methodologies, enabling efficient model selection and parameter determination. Experimental results demonstrate the accuracy of the implemented elements through a series of case studies, evaluated using Sheppard's criteria function. This integration marks a significant step toward automated EIS model fitting and optimization, with potential implications for advancing electrochemical and materials research.

Keywords: Electrochemical Impedance Spectroscopy, Circuit Simulators, Hypothetical Circuit Elements, Equivalent Electronic Circuits

Vpeljava elemementov EIS v SPICE simlator vezij

Izvleček: Ta študija uvaja hipotetične vezne elemente, specifično konstantnofazni element (CPE) in ničelni red približka RC vezja (ZARC), v simulacijsko okolje SPICE za izboljšanje analize elektrokemijske impedančne spektroskopije (EIS). EIS, ključna metoda za razumevanje elektrokemijskih procesov na področjih, kot so analiza gorivnih celic, študije korozije in biomateriali, temelji na ujemanju izmerjenih impedančnih krivulj z modeli ekvivalentnih električnih vezij (EEC). Obstoječi pristopi zahtevajo strokovno znanje in znatno matematično delo, kar omejuje avtomatizacijo. Z integracijo CPE in ZARC v SPICE to delo premošča vrzel med analizo EIS in naprednimi metodologijami samodejne zasnove vezij, kar omogoča učinkovito izbiro modelov in določanje parametrov. Eksperimentalni rezultati potrjujejo natančnost implementiranih elementov skozi serijo študij primerov, ocenjenih s pomočjo Sheppardove funkcije kriterijev. Ta integracija predstavlja pomemben korak proti avtomatiziranemu prilagajanju in optimizaciji modelov EIS, z možnimi vplivi na napredek raziskav na področju elektrokemije in materialov.

Ključne besede: Elektrokemična Impedančna Spektroskopija, Simulatorji Vezij, Hipotetični Elementi Vezja, Ekvivalentna Električna vezja

** Corresponding Author's e-mail: matevz.kunaver@fe.uni-lj.si*

1 Introduction

With the rapid growth of electrical storage, electric vehicles, advanced materials and other technological advancements there is also an increasing demand for methods that can offer a quick insight into any ongoing process or material to quickly detect and prevent possible incidents. One of such methods is Electrochemical Impedance Spectroscopy (EIS) which can be used for fuel cell analysis (in order to detect if a fuel cell is starting to deteriorate), corrosion science (analyzing and simulating effects of corrosion on various metals), Bio medics and process control.

The key technique in EIS is measuring the Impedance response and then fitting the resulting curve to a known Equivalent Electrical Circuit (EEC) model. This approach requires some guesswork as the researcher must select one of the known EEC models based on experience and try to fit the model's impedance curve to that obtained during EIS measurement. Each EEC model corresponds to one of the processes encountered in the field (so one model for a perfectly working fuel cell, one for a deteriorating fuel cell, one for a cell with corrosion on connectors etc.). If the model represents a good fit for the measured data, we can assume

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that we are dealing with the process described with the selected model.

The two major disadvantages of this fitting approach are that it relies on expert knowledge, since only a seasoned observer can reliably select the most appropriate EEC when seeing the measured impedance curve and that the approach also requires a lot of mathematical work to fit the EEC circuit element values to the measured data.

The field of automatic analog circuit design on the other hand offers several methods that could be used to automate this procedure and reduce the required level of expertise. Several advanced techniques could potentially also determine the correct values of EEC elements. All these techniques, however, face a problem – EEC circuits consist of several circuit elements (Constant Phase Element, ZARC) which do not exist in circuit simulators used by these approaches. These elements don't have a direct physical equivalent in a circuit and are mostly represented by their transfer function. For the purposes of this article we will refer to these elements as hypothetical circuit elements to discern from those already implemented in circuit simulators.

The aim of the research presented in this article is to correct this by introducing these hypothetical elements into SPICE circuit simulator and thus enabling future research into combining automatic circuit design techniques with the EEC circuits obtained from EIS.

2 Current state of EIS

Current EIS techniques rely on a combination of Circuit Description Code (CDC) [1], circuit model selection and mathematical modelling techniques such as the Levenberg–Marquardt Algorithm.

2.1 Electrochemical impedance spectroscopy

Electrochemical Impedance Spectroscopy (EIS) is a powerful analytical technique used to study the electrical properties of materials and electrochemical systems. By applying a small alternating current (AC) signal over a range of frequencies to an electrochemical system and measuring the resulting voltage response, EIS provides insights into the impedance characteristics of the system. This technique is invaluable for characterizing the complex behavior of electrochemical reactions, interfaces, and materials. EIS is particularly useful in understanding processes in fuel cells, batteries, corrosion studies, and other electrochemical devices.

In the context of fuel cells, EIS is employed to analyze the performance and degradation mechanisms of these energy conversion devices. By applying EIS to fuel cells, researchers can evaluate the impedance at different frequencies to identify various components of the cell's resistance, including ohmic resistance, charge transfer resistance, and mass transport resistance. This allows for a deeper understanding of the fuel cell's efficiency, degradation, and overall performance, facilitating improvements in design and operation.

2.2 Equivalent electric circuits and circuit description code

The core of EIS consists of selecting a known circuit and seeing if it is possible to match its impedance curve to measured data.

These circuits are often described using the Circuit Description Code (CDC) which describes circuits using their elements (resistor as R, capacitor as C etc.) and parenthesis to describe their relation [1]. A CDC without parenthesis would describe all elements being in series. Parenthesis denotes elements that are parallel to each other.

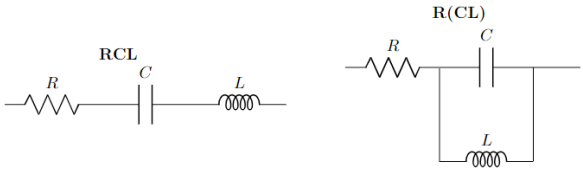

Figure 1: CDC example for a simple serial circuit (left) and a circuit with parallel elements(right)

Each EEC is therefore described with the appropriate CDC code. Once selected it offers a mathematical model to be fitted to the input curve. In the case of a RCL circuit the fitter would have to determine the correct resistance (R), capacitance (C) and inductance (L) of the circuit. One should note that for the purpose of this article, we did not add any additional noise (Gaussian or any other model) since we were aiming to create a circuit model that is a perfect fit to the mathematical model of our hypothetical elements.

2.3 Notable EEC components and their usage in modelling

While there are many different components used in EEC two of them tend to stand out and are used frequently in fuel cell analysis.

2.3.1 Constant phase element (CPE)

The CPE element [2] is used for modelling several simple chemical processes in fuel cells such as porous elec-

trodes, the effect of surface roughness of electrodes, etc.

CPE therefore simulates non-ideal capacitive behavior and deviations from standard capacitance. The mathematical model of the element is given by equation 1:

$$Z_{\mathrm{CPE}}(\omega) = \frac{1}{Q(j\omega)^n} \tag{1}$$

where Q is the CPE constant, ω is the angular frequency and n the CPE exponent (-1 < n ≤ 1), which describes the deviation from ideal capacitive behavior. A CPE element with n=1, would therefore have the same frequency response as an ordinary Capacitor. One should note that with fuel cells the value of n is usually between 0.5 and 1. At 0.5 the CPE becomes the Warburg element that is often used to study diffusion. In CDC the CPE element is denoted with the symbol **Q**.

2.3.2 Zeroth-order approximation of a RC circuit (ZARC)
The ZARC element [3] is used for simulating impedance response with multiple RC-like behaviors and complex impedance spectra. The impedance model of this element is given by equation 2:

$$Z_{\mathrm{ZARC}}(\omega) = \frac{R}{1 + RQ(j\omega)^n} \tag{2}$$

where R is the resistance, Q is the CPE constant, ω is the angular frequency and n is the order of approximation, usually between 0.5 and 1, same as with CPE element. In CDC the ZARC element is represented by **(RQ)**. [4]

2.4 Mathematical modelling

Current EIS techniques [5] work by first performing a frequency sweep of the selected process (circuit element, fuel cell or electrode) and measuring its impedance. Once the impedance is known the user must select the EEC model that he/she thinks would fit best.

Once the model is selected, the user must also select the estimated starting values of each element in the EEC model (resistance, CPE constants, orders of approximation…). These are then used with the selected mathematical approach to determine the best fit possible for the selected model and the exact element values at the same time. If the chosen values are not appropriate, the procedure still converges to the correct result but requires more iterations to do so. It can also lead to procedure getting stuck in a local minimum and producing incorrect results. This is a common issue in EIS data fitting, which is why it is desired for the starting values to be close to the optimal values.

Examples of such techniques are reflective Newton type method [6] and Levenberg-Marquardt algorithm [5].

2.5 Sheppard's criteria function

Once the mathematical approximation is complete the results are compared with the original impedance curve using the selected criteria function. Since this is a curve fitting problem there are many possible criteria functions such as RMSE, MSE and R-square. In the field of EIS however it has been estimated that the Sheppard's criteria function [7] [1] performs best for the measured impedance data, especially since it features an additional weight [8] to compensate the difference between imaginary and real data axis. We therefore opted to use this function in our research.

The criteria function is calculated using equations 3 and 4:

$$Shp = \sum \left(w_i \left(Re\left(Z_i^{math}\right) - Re\left(Z_i^{model}\right)\right)^2 + w_i \left(Im\left(Z_i^{math}\right) - Im\left(Z_i^{model}\right)\right)^2 \right) \tag{3}$$

$$w_i = \frac{1}{Re\left(Z_i^{math}\right)^2 + Im\left(Z_i^{math}\right)^2} \tag{4}$$

where w_i represents the weight calculated from the input impedance data, Z_i^{math} represents the impedance of the mathematical model (our target) calculated at the i-th frequency point and Z_i^{model} the measured impedance of our SPICE circuit at the same frequency point.

One should note that in cases of real measurements, the Z_i^{math} gets replaced with $Z_i^{measured}$.

The result of the criteria function indicates the goodness of the fit with lower values indicating a better fit. In the event of a perfect fit the result would thus be zero.

2.6 Our alternative approach

The above techniques rely heavily on the user's expertise and experience in addition to requiring a lot of input from him/her (the EEC model and its estimates).

In the field of circuit designs there are a lot of tools that offer a certain level of automatization for circuit design and could potentially be used to help in this example [9] [10] [11] [12]. Such techniques can be based on genetical programming [13], evolutionary computation with a pre-selected element layout [14] or even gram-

matical evolution [13] [15] [16] where one can create completely new circuits from the given electrical components.

The only problem is that all such techniques require access to circuit elements which in case of EIS is not possible since CPE and ZARC do not yet exist in most circuit simulators. The only known implementations are approximations using a long chain of RC elements as shown by Lopez [3]. Our aim is to create a single compact element that matches the mathematical model exactly.

We therefore decided to implement and evaluate these elements in the SPICE circuit simulator with the aim of developing an automatic EIS model selection algorithm in the future. This required rewriting some of the SPICE models and exhaustive testing.

2.7 Challenges with implementation of hypothetical elements in circuit simulators

Due to the non-integer exponent of $j\omega$ the transfer functions of CPE and ZARC cannot be modeled with circuit elements like resistors, capacitors, and inductors. The fractional exponent also complicates the simulation of such devices in the time domain where the usual approach is to use convolution with the impulse response of the device. The impulse response can be obtained via inverse Fourier transformation of the device's transfer function. Fortunately, impedance calculations are performed in the frequency domain where the evaluation of CPE and ZARC involves only simple algebraic manipulations of complex numbers.

The internal API of SPICE makes it possible to separately describe the behavior of an element for the time domain and for the frequency domain. The model developer is responsible for making sure these two descriptions are consistent with each other. If one does not intend to simulate a device in time domain, it is sufficient to provide the description of a device for frequency domain only.

Because CPE, ZARC, and all the EIS equivalent circuits are linear the time domain description of CPE and ZARC can be reduced to that of a simple resistor. This description is used only in the computation of the operating point. Because the circuit is linear the linearizations of the elements which are used in the frequency domain analysis do not depend on the operating point. The operating point computation cannot be skipped thus one has to make sure the simulator computes some operating point that does not even have to reflect any physically meaningful behavior.

Modeling a device in frequency domain involves the computation of its admittance matrix. For CPE and ZARC this matrix reduces to a single element. Its value can be computed by evaluating the inverse of the element's impedance at the frequency provided by the simulator.

3 Adding new elements to SPICE

Our aim was therefore to take the elements required by EIS (CPE and ZARC) and implement them in the circuit simulator of our choosing (SPICE). We also considered alternatives such as Verilog-A [17] but found that we could not use to correctly model the element in the frequency domain.

We have also performed a series of evaluations where we compared the mathematical model (i.e. the ideal) with the results given by the simulator elements. Ideally, they should be as close as possible. In order to remain impartial, we used the same evaluation technique as is used in measuring the fit between the curve and the mathematical model in EIS – the Sheppard's criteria function.

3.1 SPICE

Developed in the late 1970s at the University of California, Berkeley, SPICE (Simulation Program with Integrated Circuit Emphasis) [18] provides a comprehensive environment for modeling and simulation of the behavior of analog and digital circuits.

At its core, SPICE simulates the electrical behavior of circuits by solving the nonlinear differential equations that describe the circuit components and their interactions. It models the various elements of a circuit, such as resistors, capacitors, inductors, diodes, transistors, and operational amplifiers, using mathematical equations that represent their behavior.

One of SPICE's primary functions is to perform a DC operating point analysis, which calculates the steady-state voltages and currents in the circuit. This analysis is essential for understanding the circuit's behavior under constant input conditions. Additionally, SPICE can conduct AC analysis to determine the circuit's response to small-signal variations across a range of frequencies, providing insights into frequency response, gain, and stability.

SPICE has become a cornerstone of electronic design and analysis due to its ability to accurately predict cir-

cuit behavior before physical prototypes are built. This capability significantly reduces development time and costs by allowing engineers to test and optimize their designs virtually.

In addition to traditional circuit simulation, SPICE has been integrated into mixed-signal simulation environments that combine analog and digital circuit analysis. This integration allows for comprehensive testing of systems that involve both types of circuits, such as those found in modern microprocessors and digital communication systems.

In research, SPICE facilitates the exploration of new circuit designs, materials, and technologies. Researchers use the simulator to model innovative concepts, test hypotheses, and validate theoretical predictions. This capability accelerates the development of cutting-edge technologies and advances the field of electronics.

3.2 Implementation of CPE and ZARC in SPICE

Adding a new device to the SPICE simulator is a tedious process. Fortunately, XSPICE extensions provide a simple mechanism for adding new elements to SPICE. We used Spice Opus [19] [20] which is based on the original SPICE3 source code with added XSPICE extensions. Spice Opus makes it possible to describe an element by using the XSPICE API. The description is compiled into a dynamic library which is loaded by the simulator at runtime.

In XSPICE one describes the behavior of an element in the frequency domain by specifying the real and the imaginary parts of the transfer functions between element's terminal voltages and branch currents. Because both CPE and ZARC have only two terminals and one branch a single transfer function must be defined. For CPE the transfer function at a given frequency *f* is

$$H = Q\left(2\pi f\right)^n cos\left(n\pi/2\right) + iQ\left(2\pi f\right)^n sin\left(n\pi/2\right) \quad (5)$$

Similarly, for ZARC we have

$$H = R^{-1}\left(1+\Omega cos\left(n\pi/2\right)\right) + iR^{-1}\Omega sin\left(n\pi/2\right) \quad (6)$$

where $\Omega = \left(2\pi f\tau\right)^n$ and *i* is the imaginary unit.

The element description is provided in two files. One specifies the element's interface (terminals and parameters). The other specifies its inner workings. The latter one is written in an extension of the C programming language. Both files are preprocessed by the XSPICE's model compiler (cmpp) upon which the resulting files are compiled with a C compiler and linked into a dynamic library.

For each candidate circuit PyOpus [21] generates the circuit's netlist comprising its topology and parameter values. The netlist also contains the commands the simulator must execute to produce the circuit's response. After the netlist is created PyOpus invokes the Spice Opus simulator which loads the netlist (Figure 2). The dynamic library with the CPE/ZARC model is loaded into the simulator with the corresponding simulator command (cmload) which is followed by the analysis command. The results are written into a SPICE RAW file from which they are loaded by PyOpus for impedance extraction and cost function computation.

3.3 Simulation and Evaluation

The aim of our experiments was to match the theoretical (i.e. mathematical) circuit elements as closely as possible with simulated circuit elements in SPICE. We first used the mathematical impedance model to create the baseline impedance curve and compared it with the SPICE simulation results.

3.3.1 Input Data – Mathematical Model

For all our experiments we used the mathematical impedance model of the selected circuit. We used the models described by equations 1 and 2 computed at given points in the selected frequency range.
For some of the case studies we also added some Gaussian noise to the calculated impedance curve to see if it would have any effect on the final evaluation.

3.3.2 Output Data – SPICE simulation

Our SPICE simulations used a simple circuit for measuring the desired impedance curve.

The system measured the voltage values at both ends of the subcircuit and then calculated the resulting impedance. We used the AC analysis with a frequency sweep from 10^{-2}Hz to 10^{5}Hz which is the usual range used in EIS measurements.

Our experiment consisted of two circuit files – one for the main circuit (as shown on figure 1) and the other for the element setup we wanted to measure. This enabled us to perform a whole series of experiments by simply swapping out the subcircuit files.

3.3.3 Evaluation

Since we wanted to be able to compare our results to those presented in other EIS articles, we used the same metric that is used by them – Sheppard's criteria function (see 2.5). The only difference is that we compared the impedance curve gained from the mathematical

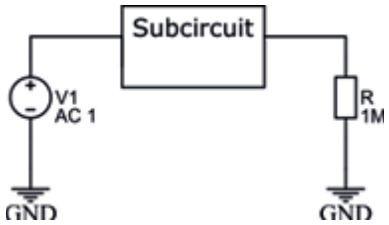

Figure 1: Measuring circuit setup

model (using equations (1) and (2)) with the impedance values obtained from the SPICE simulator. Everything else remained the same – the lower the number the better our SPICE model matched the theoretical mathematical model of the EEC element.

3.3.4 Experiment flow

The main aim of our experiments was to prove that our circuit model matches the theoretical model of each element. Instead of first calculating the model impedance values for each frequency of interest and then comparing the result with the curve obtained from the SPICE element we made a slight modification.

We first ran the SPICE simulation and collected both the impedance values, and the exact frequencies used by the simulator. We then used these points in the mathematical model to ensure a fair comparison.

Lastly, we used the Sheppard's criteria function to get the result.

4 Case studies

We tested three circuits that commonly occur in EIS articles – a single CPE element, a single ZARC element and two serial ZARC elements, combined with a resistor. The last circuit is also often used in Fuel cell EEC. For each circuit, we first calculated the values of the mathematical models using equations 1 and 2. We then created an equivalent subcircuit netlist, ran the SPICE simulation and extracted the impedance measurements. Both the model and the measurements were then used in our final evaluation using the Sheppard's criteria function. One should note that at this stage we used only mathematical models as input since we had to verify the fit of new circuit elements.

4.1 Single CPE element (Q)

The single CPE element had the CPE constant set to 0.01 and the n value to 0.8 with no additional elements in the circuit. As can be seen in figure 2 the model and simulation were a perfect match, with a Sheppard value of $7.1*10^{-13}$.

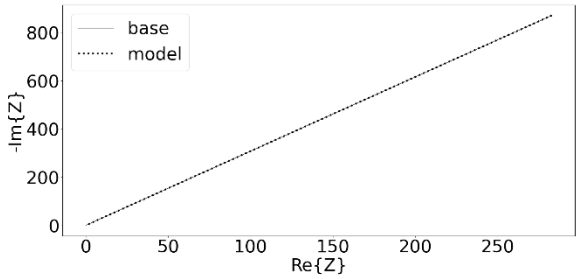

Figure 2: Single CPE

4.2 Sigle ZARC element (RQ)

For the single ZARC element we used resistance value of 50Ω, CPE constant 0.01 and n value of 0.7 and again added no additional elements to the subcircuit. The resulting Sheppard value was $7.09*10^{-13}$ with the model and simulation data shown in figure 3.

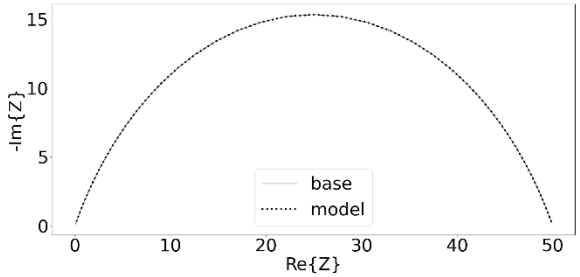

Figure 3: Single Zarc

4.3 Two parallel ZARC elements (R(QR)(QR))

This was by far the most important experiment since there are a lot of cases where fuel cell measurements result in the "double hill" curve which indicates that there should be two ZARC elements involved. The EIS model adds an additional serial resistor, so we adjusted our subcircuit accordingly.

The first evaluation featured ZARC elements with similar characteristics and is shown in figure 4. The circuit featured a serial resistor of 10Ω, first ZARC with (R=50 Ω, CPE constant = 0.01 and n = 0.7) and the second with (R=50 Ω, CPE constant = 0.0001 and n = 0.7). The resulting criteria function value was $2.17*10^{-12}$ which again show a good fit.

It is however rare to have ZARC elements that are so evenly matched, which is why we performed another evaluation and adjusted the second ZARC element to (R=50 Ω, CPE constant = 0.01 and n = 0.45). The resulting fit is shown in figure 5. The value of the criteria function was $2.54*10^{-12}$ which means that the fit remains good despite a noticeable difference from the original curve shown in figure 4.

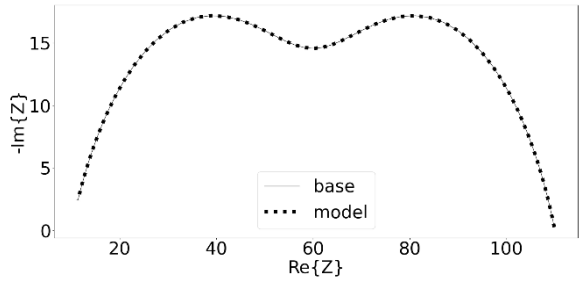

Figure 4: Double Zarc Model

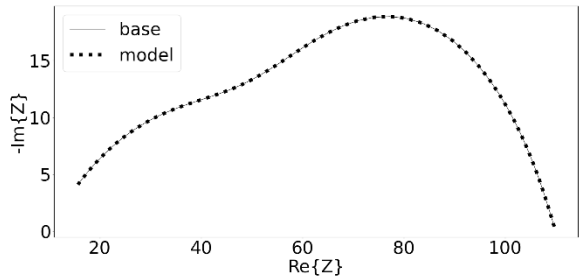

Figure 5: Two ZARC with dissimilar characteristics

5 Conclusions and future work

The results presented in this work show that we have successfully implemented two theoretical circuit elements (CPE and ZARC) in the SPICE circuit simulator. This is one of the first known implementations of such elements in SPICE.

This implementation allows a completely new approach to EIS impedance fitting since we can now experiment with automatic circuit design techniques which were previously inaccessible in the field of EIS. It also does not impact the performance of SPICE since we only added additional models to its circuit elements library.

For our future work we plan on trying to modify our existing evolutionary methods [16] [22] to include the new elements and try to select the correct EEC model based on the input impedance curve. Should this prove successful we can also attempt to correctly determine the circuit element values using circuit optimization techniques [23].

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7 Conflicts of interest

The authors declare no conflict of interest.
The founding sponsors had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, and in the decision to publish the results.

8 References

1. B. A. Boukamp, "A Nonlinear Least Squares Fit procedure for analysis of immittance data of electrochemical systems," *Solid State Ionics,* vol. 20, pp. 31-44, 1986, https://doi.org/10.1016/0167-2738(86)90031-7.
2. S. Kochowski and K. Nitsch, "Description of the frequency behaviour of metal–SiO2–GaAs structure characteristics by electrical equivalent circuit with constant phase element," *Thin Solid Films,* vol. 415, pp. 133-137, 2002, https://doi.org/10.1016/S0040-6090(02)00506-0.
3. J. A. López-Villanueva, P. Rodríguez-Iturriaga, L. Parrilla and S. Rodríguez-Bolívar, "A compact model of the ZARC for circuit simulators in the frequency and time domains," *AEU - International Journal of Electronics and Communications,* vol. 153, p. 154293, 2022, https://doi.org/10.1016/j.aeue.2022.154293.
4. B. Hirschorn, M. E. Orazem, B. Tribollet, V. Vivier, I. Frateur and M. Musiani, "Determination of effective capacitance and film thickness from constant-phase-element parameters," *Electrochimica Acta,* vol. 55, pp. 6218-6227, 2010.
5. M. Žic, V. Subotić, S. Pereverzyev and I. Fajfar, "Solving CNLS problems using Levenberg-Marquardt algorithm: A new fitting strategy combining limits and a symbolic Jacobian matrix," *Journal of Electroanalytical Chemistry,* vol. 866, p. 114171, 2020, https://doi.org/10.1016/j.jelechem.2020.114171.
6. T. F. Coleman and Y. Li, "An Interior Trust Region Approach for Nonlinear Minimization Subject to Bounds," *SIAM Journal on Optimization,* vol. 6, pp. 418-445, 1996, https://doi.org/10.1137/0806023.
7. R. J. Sheppard, B. P. Jordan and E. H. Grant, "Least squares analysis of complex data with applications to permittivity measurements," *Journal of Physics D: Applied Physics,* vol. 3, p. 1759, November 1970, https://dx.doi.org/10.1088/0022-3727/3/11/326.
8. P. Zoltowski, "The error function for fitting of models to immittance data," *Journal of Electroanalyti-*

cal Chemistry and Interfacial Electrochemistry, vol. 178, pp. 11-19, 1984; https://doi.org/10.1016/S0022-0728(84)80019-4.
9. Z. Gan, Z. Yang, T. Shang, T. Yu and M. Jiang, "Automated synthesis of passive analog filters using graph representation," *Expert Systems with Applications,* vol. 37, no. 3, pp. 1887-1898, 2010, https://doi.org/10.1016/j.eswa.2009.07.013.
10. G. Gielen and R. Rutenbar, Computer-aided design of analog and mixed-signal integrated circuits, New York: John Wiley & Sons, 2002, https://doi.org/10.1109/5.899053.
11. G. Györök, "Crossbar network for automatic analog circuit synthesis," in *2014 IEEE 12th International Symposium on Applied Machine Intelligence and Informatics (SAMI)*, 2014, https://doi.org/10.1109/SAMI.2014.6822419.
12. R. Zebulum, M. Pacheco and M. Vellasco, "Comparison of different evolutionary methodologies applied to electronic filter design," in *IEEE International Conference on Evolutionary Computation Proceedings*, 1998, https://doi.org/10.1109/ICEC.1998.699812.
13. J. R. Koza, I. F. H. Bennett, D. Andre, M. A. Keane and F. Dunlap, "Automated Synthesis of Analog Electrical Circuits by Means of Genetic Programming," *Trans. Evol. Comp,* vol. 1, pp. 109-128, Jul 1997, http://dx.doi.org/10.1109/4235.687879.
14. Ž. Rojec, Á. Bűrmen and I. Fajfar, «Analog circuit topology synthesis by means of evolutionary computation,» *Engineering Applications of Artificial Intelligence,* vol. 80, pp. 48-65, 2019, https://doi.org/10.1016/j.engappai.2019.01.012.
15. J. R. Koza, Genetic Programming: On the Programming of Computers by Means of Natural Selection, Cambridge, MA: MIT Press, 1992.
16. M. Kunaver, "Grammatical evolution-based analog circuit synthesis," *Informacije MIDEM,* vol. 49, p. 229–240, 2019, https://doi.org/10.33180/InfMIDEM2019.405.
17. A. Bürmen, T. Tuma, I. Fajfar, J. Puhan, Ž. Rojec, M. Kunaver and S. Tomažič, "Free software support for compact modelling with Verilog-A," *Informacije MIDEM,* vol. 54, 2024; https://doi.org/10.33180/InfMIDEM2024.404.
18. L. W. Nagel and D. O. Pederson, "SPICE (Simulation Program with Integrated Circuit Emphasis)," 1973.
19. T. Tuma and A. Burmen, Circuit Simulation with SPICE OPUS: Theory and Practice, 1st ed., Birkhäuser Basel, 2009, https://doi.org/10.1007/978-0-8176-4867-1.
20. "Spice Opus," Faculty of Electrical Engineering, Ljubljana, [Online]. Available: https://www.spiceopus.si/. [Accessed 11 12 2024].
21. A. Bűrmen, J. Puhan, J. Olenšek, G. Cijan and T. Tuma, "PyOPUS - Simulation, Optimization, and Design," EDA Laboratory, Faculty of Electrical Engineering, University of Ljubljana, 2016.
22. Ž. Rojec, «Towards smaller single-point failure-resilient analog circuits by use of a genetic algorithm,» *Informacije MIDEM : časopis za mikroelektroniko, elektronske sestavne dele in materiale,* vol. 53, p. 103–117, 2023.
23. Á. Bűrmen, T. Tuma and I. Fajfar, «A combined simplex-trust-region method for analog circuit optimization,» *Journal of circuits, systems, and computers,* vol. 17, pp. 123-140, 2008, http://dx.doi.org/10.1142/S0218126608004125.
24. T. H. Wan, M. Saccoccio, C. Chen and F. Ciucci, "Influence of the Discretization Methods on the Distribution of Relaxation Times Deconvolution: Implementing Radial Basis Functions with DRTtools," *Electrochimica Acta,* vol. 184, pp. 483-499, 2015, https://doi.org/10.1016/j.electacta.2015.09.097.

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Development of an Improved Zinc Oxide Thin Film Transistor for Next-Generation Smartphone Display Technologies

Anindya Bose[1], Sayori Biswas[2], and Sarthak Sengupta[3]

[1]Electronics Engineering Division, 6th Generation of Computing, London, United Kingdom
[2]Department of Electronics Engineering, Jadavpur University, Kolkata, India
[3]School of Digital Health, IIHMR University, Jaipur, India

Abstract: The study aims to create a portable and highly efficient Zinc Oxide (ZnO) Thin Film Transistor (TFT) on a single crystal Silicon substrate, followed by necessary electrical characterizations. The research explores relevant studies from around the world. The TFT has garnered attention worldwide due to its potential application in flat panel displays. The electrical and optoelectronic properties of ZnO-based TFT have also attracted significant interest. The figure of merit of a TFT is strongly influenced by crucial parameters such as on/off current ratio and field-dependent mobility, both of which are dependent on Transistor geometry, the crystallinity of the active layer, and the quality of the interface (such as semiconductor-insulator interface or metal-semiconductor interface). The growth and processing conditions of different layers impact these variables as well. The study presents the development of a low-powered and efficient bottom gate ZnO TFT on a p-type single-crystal Silicon substrate for next-generation laptop and mobile display segments. In this context, RF magnetron sputtering was used to create a bottom-gate ZnO-based Thin-film Transistor (ZnO-TFT) at room temperature. The ZnO-TFT operates in depletion mode with a threshold voltage of -1.2 V and exhibits a drain current on/off current ratio of 2 x 10^8. Maximum saturation mobility of 48 cm^2/V-sec was recorded at VGS=24.1 V and VDS=10 V. This research study can be an opportunity for future researchers working in flexible smart panel display driving circuits.

Keywords: Zinc Oxide, Maskless Lithography, RF Magnetron sputtering, Thin Film Transistor, Future display driver element.

Razvoj izboljšanega tankoplastnega tranzistorja iz cinkovega oksida za naslednje generacije tehnologij za predvajanje na pametnih telefonih

Izvleček: Cilj študije je ustvariti prenosni in visoko učinkovit tankoplastni tranzistor iz cinkovega oksida (ZnO) na monokristalni silicijevi podlagi, čemur sledijo potrebne električne karakterizacije. V raziskavi so preučene ustrezne študije z vsega sveta. TFT je po vsem svetu pritegnil pozornost zaradi možnosti uporabe v ploskih zaslonih. Električne in optoelektronske lastnosti TFT na osnovi ZnO so prav tako pritegnile veliko zanimanja. Na kakovost TFT močno vplivajo ključni parametri, kot sta razmerje med vklopnim in izklopnim tokom ter od polja odvisna gibljivost, ki sta odvisna od geometrije tranzistorja, kristaliničnosti aktivne plasti in kakovosti vmesnika (kot je vmesnik polprevodnik-izolator ali vmesnik kovina-polprevodnik). Na te spremenljivke vplivajo tudi pogoji rasti in obdelave različnih plasti. Študija predstavlja razvoj nizkozmogljivega in učinkovitega TFT z vrati iz ZnO na p-tipu monokristalne silicijeve podlage za naslednjo generacijo prenosnih računalnikov in mobilnih zaslonov. Pri tem je bilo z magnetronskim brizganjem RF uporabljeno za izdelavo tankoplastnega tranzistorja na osnovi ZnO (ZnO-TFT) z vrati pri sobni temperaturi. ZnO TFT deluje v načinu ponora z napetostjo praga -1,2 V in izkazuje razmerje vklopnega/izklopnega toka 2 x 10^8. Največja nasičena gibljivost 48 cm^2/Vs je bila zabeležena pri VGS = 24,1 V in VDS = 10 V. Ta raziskava je lahko priložnost za prihodnje raziskovalce, ki se ukvarjajo s pogonskimi vezji prilagodljivih pametnih panelnih zaslonov.

Ključne besede: Cinkov oksid, litografija brez maske, RF magnetronsko brizganje, tankoplastni tranzistor, element gonilnika zaslona prihodnosti.

** Corresponding Author's e-mail: anindya.nitdgp@gmail.com*

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1 Introduction

A conventional technology extensively utilized in new-generation flat-panel displays, laptops, desktop computers, smartphones, video gaming systems, and personal digital assistants is thin-film transistor (TFT) technology. Due to this technology, flat screens with ever-larger dimensions are now possible, revolutionizing video systems: The most common substrates being used nowadays for the production of TFT-enabled liquid crystal display (TFT-LCD) have a diagonal dimension of 164 inches. It took a long time for their fabrication technique to advance to the point where it could be utilized in production, even though it has a history that is almost as old as CMOS technology [1]. There are three sides to the advancement and development of TFT technology: the enhancement of the semiconductor layer, the stability of the manufacturing process for large-scale production, and the advancement of process machinery to create ever-larger devices. The first factor was primarily what initially slowed down the massive development of this technology. TFT-LCDs have used this technology since it first appeared. However, some other applications have been critically reviewed over the past 20 years in diverse areas like X-ray detection [2, 3], microelectronic devices-enabled memory [4, 5], chemical sensing [6], and bio-chemical sensing [7]. The last field has seen a significant contribution from organic thin film transistors (OTFTs) [8].

The display industry makes extensive use of TFTs as specific devices for data available in pixel display. TFTs also hold promise for flexible 3D ICs and large-area integrated circuit applications. A type of flat panel display also known as Active Matrix LCD was made possible by TFT technology, which is majorly considered the main building block behind the display unit of laptop computers. Flat panel displays are increasingly being used in place of cathode ray tube (CRT) screens in desktop computer systems. Recent advancements in the mobility and stability of amorphous silicon, along with the higher manufacturing costs of polysilicon, have heightened interest in oxide semiconductors such as ZnO and indium gallium zinc oxide (IGZO). Although some special designs of ZnO-TFT with field-dependent saturation mobility higher than 100 cm^2/Vs have already been reported [9] and the manufacturing process of such devices greatly used pulsed laser deposition (PLD) technique, which could restrict their use in large-area and low-cost applications. RF Sputtering is a desirable deposition technique for the high-volume manufacturers of oxide semiconductor devices, particularly ZnO, in contrast to PLD.

In this study, we have demonstrated an efficient TFT device structure that utilizes an RF-sputtered zinc oxide (ZnO) film as the active layer. The ZnO TFT, which has a channel width of 60 nm, was fabricated on a single-sided polished p-type <100> crystal-oriented silicon die with dimensions of 2 cm x 2 cm. This device exhibits a high on/off drain current ratio of approximately 2 x 10^8 and a field-dependent saturation mobility of 48 cm^2/Vs.

A bottom gate TFT is developed where ZnO plays the pivotal role of the active channel layer. A thin layer of Silicon dioxide (SiO_2) provides an isolation between the p-type Silicon substrate and the conducting ZnO channel. Source and drain metallic contacts are applied on the top of the conductive ZnO layer. The gate contact terminal of the Transistor lies on the top of the Silicon layer through which the modulation of charge carrier concentration takes place inside the ZnO channel. TFTs are a special class of Field Effect Transistor that consumes current in the microampere range which is a hundred times smaller than a conventional silicon MOSFET. It is also important that the size of the TFT is much smaller than the conventional silicon MOSFET.

2 Literature review

A review of the literature was collected to explore relevant research articles. TFTs are essentially MOSFET transistors, and the first TFT was made in 1962, around two years after the first MOSFET [10]. The first TFT-LCD was demonstrated in 1973, establishing the primary course for TFT technology research and development [11]. The manufacture of TFTs and MOSFETs does not share the same challenges. This distinction explains why TFT-LCDs took more than 20 years to become commercially viable. The process steps are where the fundamental distinction between CMOS and TFT technology exists.

While TFT technology just requires deposition, CMOS technology also includes the steps of implantation and layered growth from the substrate. This has significant ramifications for the source, drain, and channel's crystalline quality: the carrier mobility in CMOS is unquestionably better than in sin TFTs because of the crystallinity preservation with the implantation approach, whereas deposition only yields amorphous layers. TFT technology, on the other hand, has a significant advantage over CMOS technology in that since just a deposition procedure is required, transistors may be made on virtually any substrate, including transparent materials like glass and plastic. That is why technology has always been chosen for the creation of LCD screens.

A CdSe TFT was introduced in 1973 [12, 13] after the CdS TFT, which was the first, was introduced. The car-

rier mobility of both was above 40 cm^2/Vs, which was fairly good mobility. However, the application to LCDs never became commercially viable due to challenges in the fabrication process, such as the stability of the semiconductor quality on a broad surface followed by the reliability issues of the devices.

Due to the invention of hydrogenated amorphous silicon (a-Si:H) at the beginning of the 1980s, which significantly enhanced the stability and properties of TFTs, this technology underwent a significant advancement, enabling the production of active matrix (AM) LCDs, and in 1989 the first TFT-LCD was commercialized. Due to the advancement of other materials, the semiconducting layer was then improved. A significant step in further enhancing the properties of TFTs was the creation of transparent oxide semiconductors, such as IGZO. Due to the high carrier mobility and the creation of transparent transistors, the LCDs' aperture ratio increased while power consumption was further decreased [14]. Some other groups also reported potential TFTs with high K gate dielectrics [15, 16, 25, 28] and in both cases, the performance of the device was found to be remarkably good in terms of its mobility and on/off current ratio.

Another element of technological growth is product dimensions. The diagonal measurement of the first TFT-LCD to be commercialized was 10.4 inches. The 10th generation of mother glass, which corresponds to glass substrates as large as 2850 mm by 3050 mm, is now being used in TFT-LCD manufacturing facilities (164 in.). The 11th generation of mother glass, measuring 3200 mm by 3600 mm (189 in.), is now being developed and ought to be put into use soon. Companies like SHARP, LG, Samsung, and Innolux, among others, have been working hard to develop stable processes on large-scale substrates and to make progressively huge equipment for the deposition, lithography, etching, and testing of even larger substrates. LCD panels are the principal device that uses TFTs. TFTs are nevertheless frequently utilized as sensors in X-ray detectors. In numerous sensing applications, TFT devices are also used.

Resistive pressure sensors are among the most used physical sensors and were created for TFT touch panels. Since the start of the 2010s, businesses like LG Display, AUO, and JDI have started producing them [12]. OLED and pressure sensor layers have been incorporated into the TFT array substrate. In the latter, pressure is converted into an electrical signal that is then sent to TFTs, which modulate and operate the OLED. A soft polymer containing conductive particles or a pressure-sensitive rubber with resistance that varies with pressure, such as poly (methyl methacrylate) (PMMA), can be used as the pressure sensor [13]. For example, when TFTs are made on a flexible substrate utilizing organic TFTs (OTFT), this application of e-skin technology for physical sensors has attracted a lot of interest from the robotics community [17]. In addition to that the application of TFTs was also found in the field of uncooled infrared sensor arrays for thermal, pollution management, or watching over semiconductor wafers while they're being processed [18, 19].

Recent advancements in electronic device design emphasize power efficiency, scalability, and stability across various applications, including IoT and biomedical devices. For instance, a novel Sense Amplifier-Based Flip-Flop (SAFF) demonstrated robust performance under wide voltage and temperature variations, showcasing significant power and area efficiency for IoT applications [20]. Similarly, a high-performance frequency divider utilizing advanced CMOS technology achieved reduced delay and improved precision, making it suitable for biomedical applications [21]. These studies highlight the importance of innovative methodologies to enhance device efficiency, scalability, and applicability. Building on these principles, this research employs advanced nanofabrication techniques, including RF magnetron sputtering, to develop a ZnO TFT with a high on/off current ratio and superior field-dependent mobility, offering a low power solution for next-generation laptop and smartphone displays.

3 Theory and analysis

The semiconductor industry has experienced tremendous expansion as a result of the dependence of daily life on its products. Achieving progress necessitates the creation of ever more compact devices that are also faster, more adaptable, more efficient, and less expensive. To fulfill the demands of the expanding semiconductor industry, new technologies and materials have been developed in response to this demand. One of the newest and busiest fields of study is nanotechnology, which produces items with very small particles and unique features. Thin-film technology, which enables the deposition of extremely thin layers of semiconductor material on a supporting substrate (from a few nanometers down to the angstrom level), is crucial in this regard. Due to surface and quantum confinement effects, the resultant material has unprecedented mechanical, chemical, optical, and electrical properties after being shrunk to the nanometer scale. ZnO is an attractive material because of its superior electronic and optoelectronic properties. ZnO is excellent for a variety of devices because of its direct and wide band gap (i.e., 3.4 eV) nature along with large

exciton binding energy [22]. In the tetrahedral geometry of the crystal lattice, each Zn atom is surrounded by four O atoms, while each O atom is also surrounded by four Zn atoms. Rock salt, zinc blende, and wurtzite are the three crystal forms that ZnO can take. ZnO exists in wurtzite form at ambient temperatures [23]. The growth of ZnO on a cubic substrate can produce a stable zinc blende phase [24, 25, 26]. The lattice parameters for the wurtzite structure are equal, between 3.2475 and 3.5201 angstrom, and between 5.2042 and 5.2075 angstrom. Strong ionic characteristics are seen in the link between Zn and O in the crystal lattice. ZnO is thus categorized as a compound that falls between an ionic and a covalent kind [23].

In this context, a necessary initiative is taken towards the fabrication and characterization of an efficient ZnO-based TFT structure with bottom gate arrangement. Fabrication of a TFT is a complex process and it occupies a lot of steps starting from mask layout design to the development of the end device on a single side polished <100> crystalline silicon wafer.

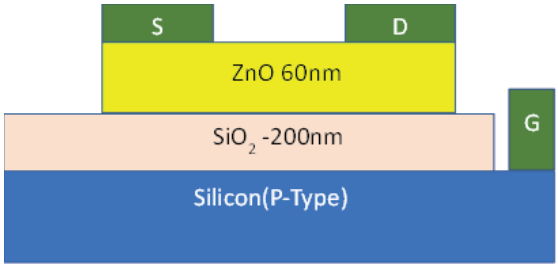

Figure 1: Structure of proposed ZnO TFT

In Figure 1, a two-dimensional design of a TFT is proposed where ZnO is the active layer. The Transistor will be developed on a p-type single crystal <100> silicon substrate. Source, Drain, and Gate metal contacts are made up of aluminium. Figure 2 represents the layout design of the ZnO TFT with a *W/L* ratio of 75/25. The light blue region represents the ZnO layer, and the pink-colored region represents the source and drains metal contacts respectively, and the dark blue region placed at the right side represents the bottom gate metal contact. One might find it confusing to compare Figure 2 with Figure 1. However, the process involved a blanket deposition of SiO_2 on top of the silicon wafer. Following this, a square section was completely etched away from the SiO_2 using UV photolithography, indicated by the shaded dark blue area. Later the bottom gate aluminium contact was deposited in that region.

In Figures 3 and 4, a step-by-step process fabrication method is given. Contamination is a big problem in the nanofabrication process so to minimize the effect of contamination a cleaning is a must for a fresh new

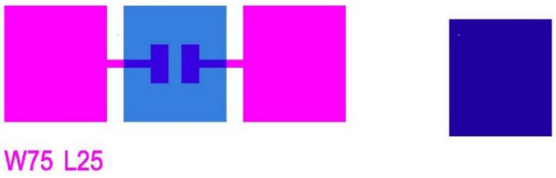

Figure 2: Mask Layout Design of a ZnO TFT in Clewin Software

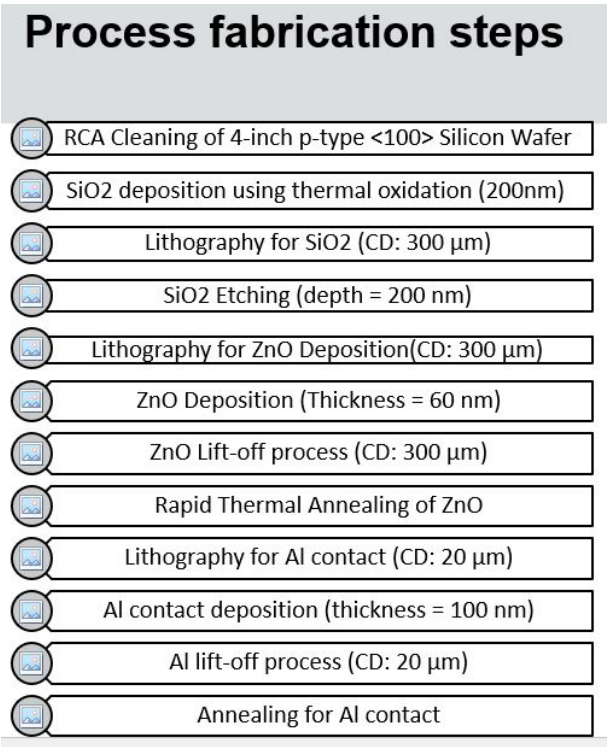

Figure 3: Process fabrication steps

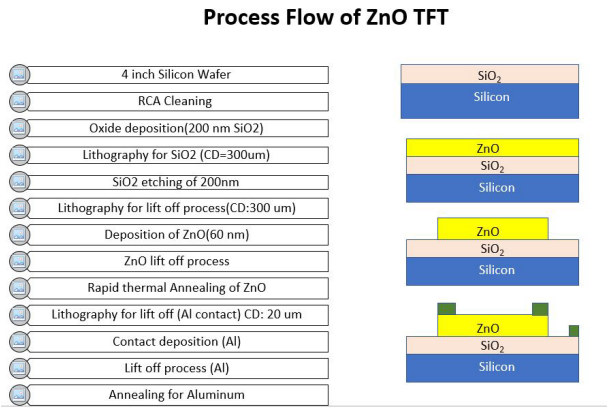

Figure 4: Complete process flow chart of ZnO TFT with tentative step-by-step design

wafer. It is highly recommended to clean the silicon wafer before doing any process. Therefore, an RCA (Radio Corporation of America) cleaning was performed followed by a dilute HF dip just before the thermal oxidation process.

RCA Cleaning: The RCA cleaning is a three-stage cleaning process and in the first stage the wafer is immersed in a mixture containing Deionized water, NH_4OH, and H_2O_2 in a ratio of 5:1:1. The solution temperature is kept constant at 75 °C during the cleaning process. Similarly, the second stage of RCA cleaning was done at 75 °C with the following quantities present in the mixture (Deionized water and H_2O_2 and HCl) in the ratio of 6:1:1. The total duration of the first and second stages of cleaning is around 20 mins (i.e., 10 mins for each stage). The first stage of RCA is used to remove the inorganic oxides from the wafer surface and the second stage of RCA is used to remove metallic and ionic contaminants from the wafer surface. After the RCA process, one has to clean the wafer using a solution containing a dilute Hydrofluoric Acid (i.e., a mixture of HF and wafer in a ratio of 1:50) for 30 s. Silicon tends to react naturally with atmospheric oxygen and in this process, a thin layer of native oxide develops on the surface of the silicon wafer. A dilute Hydrofluoric Acid (HF) dip completely removes the native oxides from the wafer surface.

Thermal Oxidation: Once after the cleaning process, the wafer should be taken to the thermal oxidation chamber without further delay. Dry oxidation is then performed inside the oxidation chamber at a temperature of 1100 °C where silicon reacts with oxygen and a thin oxide (SiO_2) layer of 200 nm is formed at the surface of the wafer. The process duration was around four hours.

Maskless Lithography: The lithography process used in this study was performed with the Heidelberg µPG 501, a direct laser writing tool that operates at a UV wavelength of 365 nm. This mask-less lithography method enables precise patterning of photoresist-coated substrates by directly writing the desired features without the need for traditional photomasks. This approach offers enhanced flexibility and accuracy, especially for prototype fabrication.

A maskless UV photolithography is then performed for the selective etching of the thermal SiO_2 layer from the top of the wafer. A UV light source of 365nm wavelength was projected on the photoresist coated wafer surface in Figure 2. Laser/LED writing is a photolithography process that uses a laser beam or LED to create the required patterns on the photoresist (direct writing). The Mask Writer's unique feature is its ability to generate patterns directly on any substrate using photolithographic principles, with or without the aid of a traditional mask plate. Mask writers are primarily used to create photolithographic mask reticles and masks up to 5 inches in size for the Heidelberg uPG 501 system. AZ5214 type positive tone photoresist was used during this process. A positive tone photoresist is an organic compound found in the solid form (i.e., a thick substance) and upon UV exposure the exposed area becomes softer. That part can be removed by using the proper developer solvent. 22 s of development of the wafer in a solution containing MF26A (i.e., usually used for the development of positive photoresist-coated silicon wafers) gave the desired output and it was thoroughly confirmed during a microscopic inspection.

Wet Chemical Etching: Just after the photolithography process, the wafer was taken to the Chemical Wet etch bay to execute a SiO_2 chemical etch process to remove the SiO_2 from the selective areas where the photoresist is not present. A buffered oxide etchant solution was used to etch the 200 nm thin SiO_2. A wet etchant called buffered oxide etchant (BOE) is utilized in microfabrication. Its main application is to etch SiO_2 or silicon nitride thin films (Si_3N_4). BOE contains a combination of Hydrofluoric acid (HF) and a buffering agent like ammonium fluoride (NH_4F) whose work is to supply the fluorine ion into the solution and to maintain the uniformity in etch rate. The optimized etch rate of the BOE solution was found to be 71 nm/minute after testing. The Silicon wafer was dipped into the mixture for the desired time duration to etch the thermal oxide completely from the selective area.

Deposition of ZnO: After the completion of the SiO_2 etching process, the substrate was sent for optical lithography since a lithography process must be performed before the deposition of the transparent ZnO layer through RF (Radio Frequency) magnetron sputtering. The lithography process for ZnO is the same as discussed before. The minimum feature size was found to be 300 µm.

One of the methods for depositing thin films that are most frequently employed is sputtering. The substance from which a film is created or a plate with the materials to be deposited serves as the target. The target often called the cathode, is connected to the negative terminal of a DC (Direct Current) or RF power supply. It typically receives several kilovolts of electricity. The substrate that is exposed to the cathode may be grounded, electrically floating, biased either positively or negatively, heated, chilled, or any combination of these. After the chamber has been emptied, a gas (typically argon) is added and used as the medium to start and sustain a discharge. Typically, gas pressures range from a few to 100 mtorr. It is seen that current flows and a film condense on the substrate after a visible light discharge has been maintained between the electrodes. Of course, there is no current flow and no film deposition in a vacuum. Positive ions from the discharge interact with the cathode plate under a microscope and use momentum transfer to eject neutral

target atoms. These atoms enter the discharge region, travel through it, and then eventually deposit on the developing film. In addition, the target emits radiation (X-rays and photons) as well as other particles (secondary electrons, desorbed gases, and negative ions).

The RF magnetron sputtering involves a thermal process where the sample is heated up to 100 °C using a halogen lamp. The ZnO deposition was done by RF magnetron sputtering through rotation mode. The rotation mode was chosen to achieve good uniformity of ZnO deposition throughout the desired area.

ZnO Lift-off Process: After the deposition process, the ZnO-containing wafer was immediately transferred to the wet chemical bay for a lift-off process. It is noted that during photolithography a positive photoresist was coated all over the wafer or sample and only the area exposed to UV rays doesn't contain any photoresist after the development. Inside the RF Magnetron sputtering chamber, the ZnO was deposited all over the wafer and it is expected that ZnO to be present only at the place where it faces a SiO_2. In the lift-off process firstly, the wafer is dipped into an acetone solution, and therefore applying extra acetone to the top of the wafer with a high velocity. During this process, there was a peel-off of the Photoresist which was present underneath ZnO. ZnO was also eliminated from the wafer surface along with the photoresist. Only that part of ZnO will be stacked to the wafer which faces the underneath SiO_2 layer. The process is very complex and it requires continuous microscope inspection but during microscope inspection, the wafer must be transferred into an IPA (Isopropyl Alcohol) solution because the volatile nature of acetone damages the microscope objective. The wafer can only be taken out from the chemical bay when a 100% elimination of the undesired ZnO layer is observed during microscope inspection.

Rapid Thermal Annealing: A Rapid Thermal Process was done to establish a bonding between ZnO and Underneath SiO_2 just after the lift-off process. RTP (Rapid Thermal Processing) technology rapidly heats silicon wafers to high temperatures, reaching up to 1100 °C in just a few seconds. However, to avoid dislocations and wafer breakage brought on by thermal shock, wafer temperatures must be gradually lowered during cooling. Available gases include N_2, Ar, O_2, and H_2. It can be used for Annealing Contact Alloying, Rapid Thermal Oxidation (RTO), Rapid Thermal Nitridation (RTN), Densification and Crystallization, Silicidation, etc.

After all this process there was a need for aluminium contact deposition at the source, drain, and gate terminal. The photo-lithography process was repeated followed by aluminium deposition and lift-off which have already been explained. The minimum feature size of the aluminium mask was found to be 20 µm. All the Photolithography steps included in this fabrication process were done inside a class 100 cleanroom under yellow light ambient so that the unnecessary polymerization of Chemical Photoresist can be avoided.

Deposition of Aluminium: An Aluminium layer of 100 nm thickness was deposited using the electron beam evaporation method and the rotation mode of deposition was preferred in our case because of better uniformity during deposition. The metal is heated in the electron-beam evaporation process so that it can be deposited. Thin films are achieved through a controlled deposition. Solid sources are capable of deposition of metals and dielectrics. The substance is held in a water-cooled crucible and subjected to the electron beam, which causes it to evaporate and condense on the wafers/samples. The deposition is homogenous because of the planetary substrate rotation system. For substrate heating, radiant heaters are offered. There is also an option for ion etching, ion-assisted deposition, and ion co-deposition. During the deposition process, a pressure of 2×10^{-7} torr must be maintained. To reduce source atom collisions with background material atoms, a high vacuum is required.

Aluminium Lift-off Process: The aluminium (Al) lift-off process was done exactly in a similar way that has already been discussed in the case of ZnO lift-off, ZnO is exchanged by aluminium in this case.

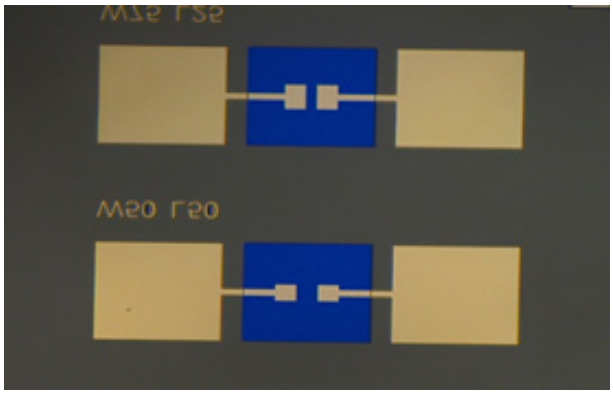

Figure 5: A single crystal silicon die containing two ZnO TFT

Figures 5 and Figure 6 were captured just after the successful aluminium lift-off process, the transparent blue area in Figure 5 and Figure 6 refers to ZnO and the aluminium contact looks like a golden-shaded area.

Forming Gas Annealing: The device was subjected to a 15-minute forming gas annealing process at 400 °C in an environment with a 9:1 ratio of nitrogen and hydrogen before being allowed to leave the clean room facility.

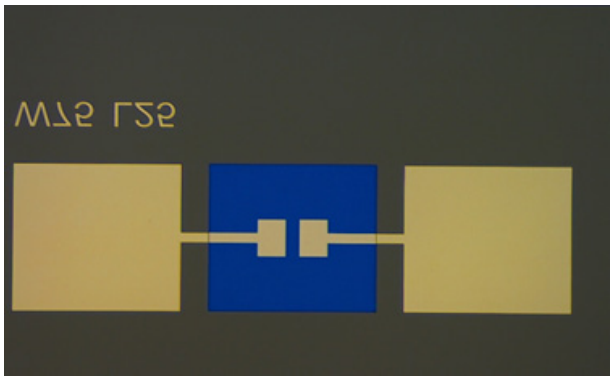

Figure 6: Zoomed view of a single TFT with a *W/L* ratio of 75/25

4 Result and discussion

TFT belongs to the family of new generation portable Field Effect Transistors. Like all our conventional Field Effect Transistors, it requires a thorough electrical characterization to be proven efficient in next-generation mobile smartphone display technologies. The choice of active material always plays the most significant role in deciding the ultimate performance of the fabricated transistor in our case, which is ZnO.

In this context, a bottom gate ZnO TFT is fabricated on a single crystal silicon die under a centralized contamination-free Clean Room Facility, and after its development, it is mounted on a Printed Circuit Board for proper electrical characterization. The final output wires are connected to the relevant PCB electrical contacts designated as Source, Drain, and Gates, respectively, to connect with the external Electrical probe station for characterization. All necessary transistor terminals, such as Source, Drain, Gate, and others, are wire bonded with the PCB electrical contacts.

A wafer level electrical characterization system also known as a DC Probe Station (PM5, Agilent Device Analyzer B1500A with pulsed source of 5 MHz) was used to perform the IV and CV measurements for the specific TFT. The characterization system's fundamental characteristics include superior IV measurement performance: measuring resolution of 0.1 fA/0.5 µV, Measurement features for the HV-SPGUs include direct control, arbitrary linear waveform generating GUI, single and multi-channel sweep, time sampling, list sweep, quasi-static CV (using the SMUs), a 10 ns pulsed I-V solution is available for characterizing samples, and an integrated capacitance module supports CV measurements between 1 kHz and 5 MHz.

ZnO TFT's transfer characteristics and output characteristics are shown in Figures 7 and 8, respectively, and an on/off current ratio that was derived from Figure 7 was found to be in the order of 2 x 10^8. At V_{DS} = 10 V and V_{GS} = 20 V, the highest drain current was determined to be 1 x 10^{-3} A, while the minimum drain current was determined to be 0.5 x 10^{-11} A at V_{DS} = 10 V and V_{GS} = −1.2 V. Calculating the on/off current ratio was done using the data presented above. The Transfer Characteristics plot, however, makes it abundantly evident that our manufactured ZnO TFT is a depletion-type Field Effect Transistor with a negative threshold voltage.

Figure 9 explains a functional relationship between the device mobility and the applied gate to source voltage. The mobility of the transistor is an extraordinarily important parameter for describing the optimal performance of the resulting device on-chip. A very high magnitude of field-dependent mobility is the reason for the presence of a polycrystalline ZnO channel layer between SiO_2 and metallic contact. With increasing V_{GS}, the ratio of free carrier to fixed charge at the grain boundaries increases in proportion to the charge density of induced free carrier, resulting in a reduction of the potential barrier at the grain boundaries. A maximum saturation mobility of 48 cm^2/Vs was recorded at V_{GS} = 24.1 V and V_{DS} = 10 V. Some of the studies [28, 29, 31] were done in the past on ZnO nanostructures to prove their worth for potential high-speed device applications but this research clearly shows the novelty of ZnO TFT in terms of speed and power consumption. Furthermore, the magnitude of field-dependent mobility was compared with much recent literature shown in Table 1 to conclude the superiority of this device.

Figure 10 shows the Capacitance-Voltage characteristics for a wide range of frequencies, from 1 kHz to 1 MHz. According to the plot at 1 kHz, the accumulation zone is shown by the left-hand region of V_{GS} = −5V, the depletion zone is indicated by the region between −5 V and −1.2 V, and the strong inversion region by the region immediately to the right of V_{GS} = −1.2 V. The observed value of gate oxide capacitance at the frequency of 1 kHz was found to be 28.5 pF from the CV characteristics plot. It is discovered that the estimated value of V_{TH} from the CV measurement curve is −1.2 V. Figure 9 shows a clear example of the shift in threshold voltage towards the negative x-axis that interferes with the depletion-type operation of the TFT. At the point where the applied Gate voltage is larger than −1.2 V, a strong inversion effect causes the n-channel to be formed from the p-type silicon substrate.

When a very high frequency (1 MHz) is reached, a differential change in capacitor voltage has no impact on the inversion layer charge. The differential change in

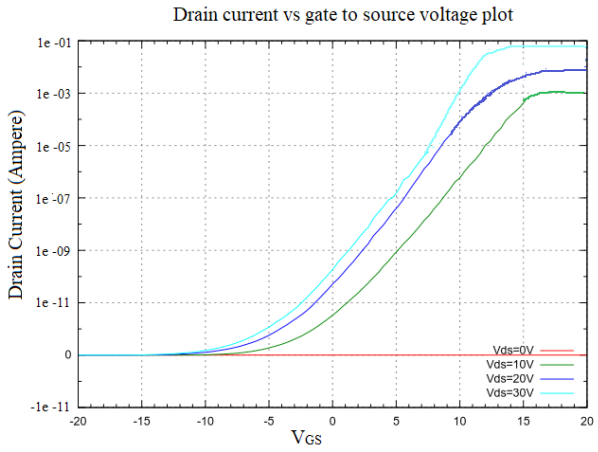

Figure 7: Drain current vs Gate to Source voltage plot of ZnO TFT

charge carrier occurs at the meal as well as the space charge region of the p-type semiconductor substrate. Therefore, the capacitance achieves a minimum value. The frequency dependence of the Capacitance-Gate Voltage plot can be visualized in Figure 10.

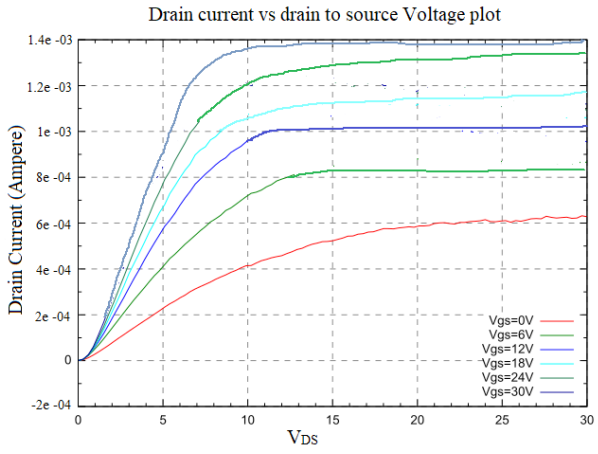

Figure 8: Drain current vs Drain to Source voltage plot

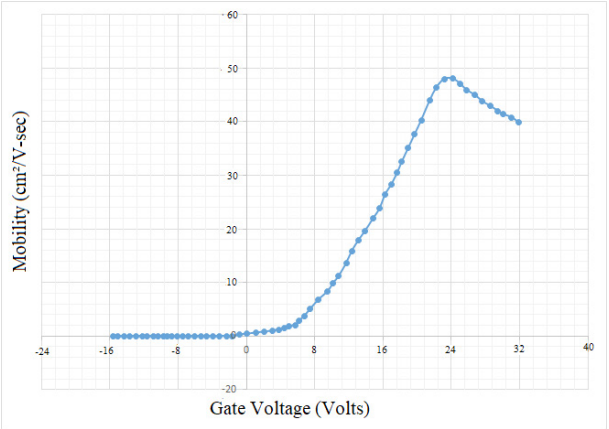

Figure 9: Field-dependent mobility plot

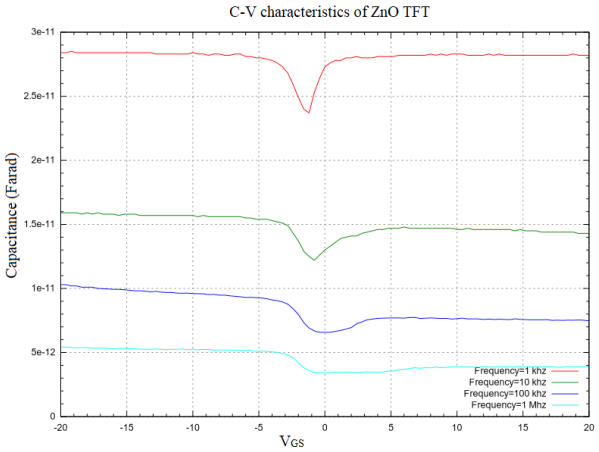

Figure 10: CV characteristics plot of ZnO TFT

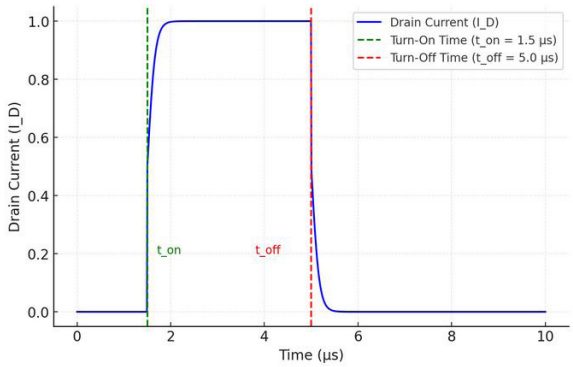

Figure 11: Transient response of ZnO TFT

To measure the transient response of a ZnO TFT fabricated on a single-crystal silicon (100) substrate, a Source Measure Unit (SMU), such as the Keithley 2460, is typically used. The SMU applies a pulsed gate voltage (V_G) to switch the device between its ON and OFF states, while a constant drain voltage (V_D = 10 V) is applied, and the normalized drain current (I_D) is monitored as a function of time. The transient response curve in Figure 11, showing I_D versus time, provides critical metrics: the turn-on time (t_{on}), defined as the time for I_D to reach 90% of its steady-state value when V_G transitions from OFF to ON, and the turn-off time (t_{off}), the time for I_D to drop to 10% of its steady-state value when V_G transitions from ON to OFF. The fabricated ZnO TFTs, known for high carrier mobility, typically exhibit t_{on} = 1.5 µs and t_{off} = 5 µs. This setup and analysis highlight the device's suitability for high-speed electronic applications.

The off current in the ZnO-TFT was measured at V_{DS} = 10 V, and V_{GS} = −1.2 V these values correspond to the depletion mode, ensuring the device operates at its minimum drain current ($I_{DS,off}$), which aligns with the threshold voltage (V_{TH}) experimentally determined from the capacitance-voltage (C-V) characteristics. The choice of these bias values allows for an accurate on/

off current ratio calculation, as V_{TH} at −1.2 V, represents the onset of the depletion zone, consistent with the transfer characteristics. The threshold voltage (V_{TH}) was determined by analyzing the C-V curves, which delineated the transition between the depletion and inversion regimes. This analysis confirmed the negative V_{TH} observed in the transfer characteristics.

Sub-threshold conduction is a critical aspect of the ZnO-TFT, particularly for applications in energy-efficient display technologies where minimizing power consumption is essential. In the fabricated device, the sub-threshold leakage current, measured as the minimum drain current ($I_{DS,\ min}$) at V_{GS} = −1.8 V, is approximately 0.0001663×10^{-11} A with a calculated sub-threshold slope of 0.075 V/Decade using two sets of values (V_{GS} = −1.2 V, I_D = 0.5 x 10^{-11} A) and (V_{GS} = −1.8, I_D = 0.0001663 x 10^{-11}A) putting into to relation mentioned in equation (1) shown below,

$$s = \left[\frac{\partial \ln I_{Ds}}{\partial V_{Gs}} \right]^{-1} \quad (1)$$

This value indicates that sub-threshold conduction is minimal, highlighting the effective gate control over the channel in the depletion mode. A low sub-threshold leakage current reduces standby power consumption, making the device well-suited for portable and low-power applications such as next-generation displays. The implications of sub-threshold conduction are closely tied to the sub-threshold slope, which determines the voltage required for an order-of-magnitude increase in current. The reported low leakage current suggests efficient control in the sub-threshold regime. Including this discussion and potentially calculating the sub-threshold slope based on experimental data would strengthen the analysis of the ZnO-TFT's suitability for display applications.

Repeated measurements were conducted for key parameters, including mobility and on/off current ratios to ensure data reliability. The mobility of the ZnO TFT was measured with a maximum uncertainty of ±1.2 cm^2/Vs, derived from variations in multiple measurements. Similarly, the on/off current ratio was determined with an error margin of ±5%, calculated based on fluctuations in the recorded drain current under consistent conditions. These measurements were performed using an Agilent Device Analyzer B1500A with a pulsed source of 5 MHz, which has a resolution of 0.1 fA/0.5 μV for current and voltage measurements, ensuring high precision. The reported data represent the mean values obtained from at least five measurements, with the standard deviations used to estimate the error margins.

ZnO is typically found to have an n-type structure. This n-type is caused by structural point defects (vacancies and interstitials) and extended defects (threading/planar dislocations). The n-type conductivity of the ZnO lattice is due to oxygen vacancies. The pre-existence of n-type nature creates an n channel in the ZnO thin film structure, resulting in electrical conduction at V_{GS} less than 0 volt and compels the TFT to be operated in the depletion mode.

Table 1: Different types of ZnO TFTs with their on/off current ratio and saturation mobility values

Different types of ZnO TFTs	Associated on/off current ratio and Saturation mobility values
Transparent ZnO thin-film transistor fabricated by rf magnetron sputtering [32]	on/off current ratio = 10^6 saturation mobility = 2 cm^2/V-s
Stable ZnO thin film transistors by fast open-air atomic layer deposition [33]	on/off current ratio = 10^8 saturation mobility = 10 cm^2/V-s
Improving the Gate Stability of ZnO Thin-Film Transistors with Aluminium Oxide Dielectric Layers [34]	on/off current ratio = 1.45 x 10^3 saturation mobility = 0.24 cm^2/V-s
Investigation on doping dependency of solution-processed Ga-doped ZnO thin film Transistor [35]	on/off current ratio = 4.17 x 10^6 saturation mobility = 1.63 cm^2/V-s
Fully flexible solution-deposited ZnO thin-film transistors	on/off current ratio = 10^6 Saturation Mobility = 0.35 cm^2/V-s
Characteristics of ALD-ZnO Thin Film Transistor Using H_2O and H_2O_2 as Oxygen Sources [37]	on/off current ratio = 2 x 10^7 saturation mobility = 10.7 cm^2/V-s
Effects of yttrium doping on the electrical performances and stability of ZnO thin-film transistors [38]	on/off current ratio = 10^7 saturation mobility = 9.8 cm^2/V-s
Controllable Doping and Passivation of ZnO Thin Films by Surface Chemistry Modification to Design Low-cost and High-performance Thin Film Transistors [39]	on/off current ratio = 10^5 saturation mobility = 0.117 cm^2/V-s
Impact of electrode materials on the performance of amorphous IGZO thin-film transistors [40]	on/off current ratio = 10^7 to 10^8 saturation mobility = 24 to 50 cm^2/V-s

Table 1 gives a survey of all potential ZnO-based TFTs along with their on/off current ratios and saturation mobility values. Both of these parameters are extremely crucial to determine the performance of a TFT. In

this context, the fabricated ZnO TFT on a p-type single crystal Silicon substrate not only exhibits an extremely high value of on/off current but also exhibits a remarkable magnitude of field-dependent saturation mobility that was never reported before which implies a largely improved operating speed of the Transistor at the on-state condition.

The fabricated ZnO TFT has been compared against amorphous silicon (a-Si) TFTs and IGZO TFTs, the most commonly used technologies in display applications that ZnO TFTs aim to replace. Amorphous silicon TFTs, known for their low field-effect mobility (0.1–1 cm^2/Vs) [1], dominate low-cost display applications but are limited by slower response times. IGZO TFTs, with their significantly higher mobility (10–20 cm^2/Vs) and excellent uniformity and stability, are more suited for high-end displays [14], [37]. In contrast, the fabricated ZnO TFT demonstrates a remarkable field-effect mobility of 48 cm^2/Vs, significantly surpassing both a-Si and IGZO technologies. Furthermore, it exhibits a high on/off current ratio of 2×10^8, outperforming many reported IGZO devices [37]. ZnO TFTs can also be fabricated using cost-effective methods such as RF magnetron sputtering at room temperature [32], combining the performance advantages of IGZO TFTs with the scalability and affordability of a-Si TFTs.

A comparative analysis with IGZO TFTs studied by Tappertzhofen et al., 2022, further underscores the competitive performance of the ZnO TFT. While IGZO TFTs in Tappertzhofen's study achieved saturation mobilities ranging from 24 to 50 cm^2/Vs and on/off ratios up to 10^8, depending on the electrode materials (Pt, W, or Ti) [40], the ZnO TFT from our study matches these benchmarks with a saturation mobility of 48 cm^2/Vs and an on/off ratio of 2×10^8. Importantly, our research emphasizes low-cost fabrication using RF magnetron sputtering and Al electrodes, whereas Tappertzhofen et al. focused on optimizing IGZO TFTs with advanced electrode materials to enhance performance. Both studies highlight their devices' potential for high-resolution and flexible display applications. The ZnO TFT stands out for its balance of excellent performance and cost-effective manufacturing, making it a strong candidate for next-generation display technologies.

An experiment was conducted on the depletion-type ZnO TFT with an initial threshold voltage V_{TH} of −1.2 V to study the effects of Negative Bias Stress (NBS). A gate voltage V_{GS} of −6 V was applied for stress durations of 10,000 s (2.8 hours) and 24 hours. The results showed a shift in threshold voltage ΔV_{TH} of approximately −0.4 V for the shorter stress duration, resulting in a final threshold voltage $V_{TH,\,final}$ of −1.6 V. For the extended stress duration of 24 hours, the ΔV_{TH} increased to −0.9 V, yielding a final $V_{TH,\,final}$ of −2.1 V. These observations confirm that the shift is attributed to charge trapping at the ZnO/dielectric interface and defect generation within the channel or dielectric layer, highlighting the device's stability under prolonged negative bias stress. This ensures the reliability of the fabricated ZnO TFT for smartphone display applications.

The term "improved" in the title is justified by the significant advancements demonstrated in this study. The fabricated ZnO Thin Film Transistor (TFT) exhibits an exceptionally high on/off current ratio of 2×10^8 and a maximum field-dependent saturation mobility of 48 cm^2/Vs, outperforming many previously reported ZnO-based TFTs (refer to Table 1 of the manuscript). These parameters highlight superior switching behavior and enhanced operational speed. Additionally, the use of RF magnetron sputtering at room temperature ensures a cost-effective and scalable fabrication process compared to more expensive techniques like PLD, making it suitable for mass production. The bottom-gate structure developed on a p-type single-crystal silicon substrate ensures high device quality and compatibility. These improvements position the ZnO TFT as a promising candidate for next-generation display technologies, addressing the demand for high-performance, low-power, and flexible devices, particularly in advanced laptop and smartphone displays.

The ZnO TFT fabrication process described in this study demonstrates significant potential for large-area display applications due to its scalability and cost-effectiveness. The use of RF magnetron sputtering ensures uniform ZnO deposition across extensive surfaces, which is critical for achieving consistency and reliability on large substrates, such as Gen 10 or Gen 11 mother glass commonly used in the display industry. Maskless UV photolithography, employed in this work, eliminates the need for expensive masks, enabling flexible and direct patterning over large areas. This approach can be scaled using industry-standard step-and-repeat or digital lithography techniques, further enhancing its applicability for mass production. The modular fabrication steps—such as SiO_2 etching, ZnO deposition, and Al metallization—can be easily adapted to automated processes and advanced systems like roll-to-roll sputtering for high-throughput manufacturing. Additionally, RF sputtering, a cost-effective alternative to methods like PLD, makes the process economically viable for industrial-scale production. Future work will focus on demonstrating the fabrication of large-area TFT arrays on substrates like flexible polymers, optimizing throughput and uniformity, and validating performance, yield, and scalability for flat-panel display applications.

5 Conclusion

This study demonstrated the successful development of a highly efficient ZnO-based Thin Film Transistor (TFT) fabricated using RF magnetron sputtering on a single-crystal silicon substrate. The device exhibited exceptional performance metrics, including an on/off current ratio of 2×10^8 and a maximum saturation mobility of 48 cm^2/Vs. All fabrication and characterization processes were conducted in a controlled cleanroom environment, maintaining a temperature of (24±3) °C and a relative humidity of 30–55%. These results establish the ZnO TFT as a strong candidate for next-generation smartphone and laptop displays, combining high operational speed, low power consumption, and scalability for large-area manufacturing. Furthermore, the cost-effective fabrication process using maskless photolithography and RF sputtering ensures its practical applicability for mass production.

Future research can explore further optimization of the ZnO TFT structure for flexible substrates, aiming to enhance mechanical durability while maintaining electrical performance. Such advancements could expand its potential applications, including foldable and wearable display technologies.

6 Conflicts of interest

The authors declare no conflict of interest.

7 References

1. Kuo Y., "Thin film transistor technology—Past, present, and future", *The Electrochemical Society Interface*. Vol. 22 No. 1, 2013, pp. 55-61.
2. Kasap S.O and Rowlands J.A., "Review X-ray photoconductors and stabilized a-Se for direct conversion digital flat-panel X-ray image-detectors", *Journal of Materials Science: Materials in Electronics*, Vol. 11, 2000, pp. 179-198.
3. Moy J.P., "Large area X-ray detectors based on amorphous silicon technology", *Thin Solid Films*, Vol. 337 No 1-2, 1999, pp. 213-221.
4. Kuo Y and Norminanda H., "Nonvolatile hydrogenated-amorphous-silicon thin-film-transistor memory devices", *Appl. Phys. Lett.* 89, 173503, 2006.
5. Yang J, Bahrami A., Ding X, Lehmann S, Kruse N, He S, Wang B, Hantusch M, Nielsch K., "Characteristics of ALD-ZnO Thin Film Transistor Using H_2O and H_2O_2 as Oxygen Sources", *Advanced Materials Interfaces*, Vol. 9 No 15, 2022, pp. 1-9.
6. Liao F, Chen C and Subramanian V., "Organic TFTs as gas sensors for electronic nose applications", *Sensors and Actuators B: Chemical*, Vol. 107 No. 2, 2005, pp. 849-855.
7. Estrela P and Migliorato P., "Chemical and biological sensors using polycrystalline silicon TFTs", *Journal of Materials Chemistry*, Vol. 17, 2007, pp. 219-224.
8. Elkington D, Cooling N, Belcher W, Dastoor PC and Zhou X., "Organic Thin-Film Transistor (OTFT)-Based Sensors", *MDPI Electronics*, Vol. 3, 2014, pp. 234-254.
9. Bayraktaroglu B, Leedy K and Neidhard R., "Microwave ZnO Thin-Film Transistors", *IEEE Electron Device Letters*, Vol. 29 No 9, 2008, pp. 1024-1026.
10. Weimer PK 1962 The TFT A New Thin-Film Transistor *IEEE Proceedings of the IRE*, Vol. 50 No 2, pp. 1462-1469.
11. Brody TP, Asars JA and Dixon GD, "A 6 × 6 inch 20 lines-per-inch liquid-crystal display panel", *IEEE Transactions on Electron Devices,* Vol. 20 No 11, 1973, pp. 995-1001.
12. Walker G, "A review of technologies for sensing contact location on the surface of a display", *Journal of the Society for Information Display*, Vol. 20 No 8, 2014, pp. 413-440.
13. Wang C, Hwang D, Yu Z, Takei K, Park J, Chen T, Ma B and Javey A., "User interactive electronic skin for instantaneous pressure visualization", *Nature Materials*, Vol. 12 No 10, 2013, pp.899-904.
14. Matsuno T 2012 Sharp *Information* 104, 13.
15. Ramesh L, Moparthi S, Tiwari PK, Samoju VR and Saramekala GK., " Investigation of the Electrical Properties of Double-Gate Dual-Active-Layer (DG-DAL) Thin-Film Transistor (TFT) with $HfO_2|La_2O_3|HfO_2$ (HLH) Sandwich Gate Dielectrics", *Semiconductors*, Vol. 54 No 10, 2020, pp. 1290–1295.
16. Gogoi P., "Thermally deposited Ag-doped CdS thin film transistors with high-k rare-earth oxide Nd_2O_3 as gate dielectric", *Semiconductors*, Vo. 47 No 3, 2013, pp. 341–344.
17. Sekitani T, Zschieschang U, Klauk H and Someya T., "Flexible organic transistors and circuits with extreme bending stability", *Nature Materials*, Vol. 9, 2010, pp. 1015-1022.
18. Dong L, Yue R, Liu L and Xia S., "Design and fabrication of single-chip a-Si TFT-based uncooled infrared sensors", *Sensors and Actuators A: Physical*, Vol. 116 No 2, 2004, pp. 257-263.
19. Dong L, Yue R and Liu L., "Fabrication and characterization of integrated uncooled infrared sensor arrays using a-Si thin-film transistors as active elements", *Journal of Microelectromechanical Systems*, Vol. 14 No 5, 2005, pp. 1167-1177.

20. P. Teotia and O. A. Shah, "Power and Area Efficient Sense Amplifier Based Flip Flop with Wide Voltage and Temperature Upholding for Portable IoT Applications," *Informacije MIDEM*, vol. 53, no. 1, pp. 39–48, 2023. https://doi.org/10.33180/InfMIDEM2023.104.
21. S. Grewal and O. A. Shah, "Design and Analysis of High Performance Frequency Divider in 32 nm CMOS Technology for Biomedical Applications," International Journal of Online and Biomedical Engineering (iJOE), vol. 19, no. 7, pp. 69–87, 2023. https://doi.org/10.3991/ijoe.v19i07.39145.
22. Janotti A and Van de Walle CG, "Fundamentals of zinc oxide as a semiconductor", *Reports on Progress in Physics*, Vol. 72 No 12, 2009, pp. 1-29.
23. Özgür Ü, Alivov YI, Liu C, Teke A, Reshchikov MA, Doğan S, Avrutin V, Cho SJ and Morkoç H., "A comprehensive review of ZnO materials and devices", *Journal of Applied Physics*. Vol. 98 No 4, 2005, pp. 1-104.
24. Morkoç H and Özgür U 2009 Zinc Oxide: Fundamentals, Materials and Device Technology *Wiley-VCH Verlag GmbH and Co KGaA*, Weinheim, Germany.
25. Kim SK, Jeong SY and Cho CR., "Structural reconstruction of hexagonal to cubic ZnO films on Pt/Ti/SiO_2/Si substrate by annealing", *Applied Physics Letters*. Vol. 82 No 4, 2003, pp. 562-564.
26. Ashrafi ABMA, Ueta A, Avramescu A, Kumano H, Suemune I, Ok YW and Seong TY., "Growth and characterization of hypothetical zinc-blende ZnO films on GaAs (001) substrates with ZnS buffer layers", *Applied Physics Letters*, Vol. 76 No 5, 2000, pp. 550-552.
27. Saha, J. K., Bukke, R. N., Mude, N. N., and Jang, J., "Significant improvement of spray pyrolyzed ZnO thin film by precursor optimization for high mobility thin film transistors", *Scientific Reports*, Vol. 10 No 1, 2020, pp. 1-11.
28. Mori I, Sato Y, Ooishi Y and Ono K., "Improvement of motion blur for IPS-Pro LCD TVs driven by 180 Hz impulsive driving", *in Proc. 14th IDW*, Sappro, Japan, 2007, pp. 79–82.
29. Jagadish C and Pearton S., "Zinc Oxide Bulk, Thin Films and Nanostructures processing, Properties and Applications", *Eds. Amsterdam, The Netherlands: Elsevier*, 2007, pp. 415–442.
30. Kandpal K, Gupta N, Singh J and Shekhar C., "On the Threshold Voltage and Performance of ZnO-Based Thin-Film Transistors with a ZrO_2 Gate Dielectric", *Journal of Electronic Materials*, Vol. 49, 2020, pp. 3156–3164.
31. Liu L, Mei Z, Tang A, Azarov A, Kuznetsov A, Xue QK and Du X., " Oxygen vacancies: The origin of n-type conductivity in ZnO", *Physical Review B*, Vol. 93 No 23, 2016, pp. 1-6.
32. Carcia PF, McLean RS, Reilly MH and Nunes G., "Transparent ZnO thin-film transistor fabricated by rf magnetron sputtering", *Applied Physics Letters*, Vol. 82 No 7, 2003, pp. 1117-1119.
33. Levy DH, Freeman D, Nelson SF, Cowdery-Corvan PJ and Irving LM., "Stable ZnO thin film transistors by fast open-air atomic layer deposition", *Applied Physics Letters*, Vol. 92 No 19, 2008, pp. 1-3.
34. Oh MS, Lee K, Song JH, Lee BH, Sung MM, Hwang DK and Im S., " Improving the Gate Stability of ZnO Thin-Film Transistors with Aluminum Oxide Dielectric Layers", *Journal of The Electrochemical Society*, Vol. 155 No 12, 2008, pp. 1009-1014.
35. Park WJ, Shin HS, Ahn BD, Kim GH, Lee SM, Kim KH and Kim HJ., "Investigation on doping dependency of solution-processed Ga-doped ZnO thin film Transistor", *Applied Physics Letters*, Vol. 93 No 8, 2008, pp. 1-3.
36. Song K, Noh J, Jun T, Jung Y, Kang HY and Moon J., "Fully flexible solution-deposited ZnO thin-film transistors", *Advanced Materials*, Vol. 22 No 38, 2010, pp. 4308-4312.
37. Yang CM, Wang JC, Chiang TW, Lin YT, Juan TW, Chen TC, Shih MY, Lue CE and Lai CS 2013 Nano-IGZO layer for EGFET in pH sensing characteristics *Proc. Nanoelectronics Conf. INEC'2013*, 2013 480.
38. Abliz A, Xu L, Wan D, Duan H, Wang J, Wang C, Liu C., "Effects of Yttrium Doping on the Electrical Performances and Stability of ZnO Thin-Film Transistors", *Applied Surface Science*, Vol. 475, 2018, pp. 565-570.
39. Kim D, Kun Woo H, Min Lee Y, Kim Y, Choi JH and Ju Oh S., "Controllable Doping and Passivation of ZnO Thin Films by Surface Chemistry Modification to Design Low-cost and High-performance Thin Film Transistors",*Applied Surface Science,* Vol. 509, 2020, pp. 1-7.
40. C. Tappertzhofen, K. Kaul, T. Marschner, and T. Mikolajick, "Impact of electrode materials on the performance of amorphous IGZO thin-film transistors," *MRS Bulletin*, vol. 47, no. 4, pp. 1–8, Apr. 2022, https://doi.org/10.1557/s43580-022-00298-z.

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Dual Band Reflectarray for Transmitter/Receiver Ground Station Drone Tracking Applications

Viwin Singh Yobuamalan[1], Ramesh Subramaniam[2], Sweetline Shamini Sureshkumar[3], and Chitra Sivathanu[4]

[1,2]Department of Electronics and Communication Engineering, SRM Valliammai Engineering College, Chennai, Tamil Nadu, India.
[3]Department of Electronics and Communication Engineering, Sri Sai Ram Institute of Technology, Chennai, Tamil Nadu, India.
[4]Department of Electronics and Communication Engineering, Rajalakshmi Engineering College, Chennai, Tamil Nadu, India.

Abstract: A dual-band, single-layer reflect array offering high gain has been developed for dual-polarized drone tracking applications. The reflect array unit comprises two center-notched spiral structures aligned orthogonally and is separated by an independent notch-perfect rectangle element. Based on the reflect array unit design, a single layer 7 x 7 array, totally 49 elements for Horizontally Linearly Polarized (HLP) Ku-band transmission (12.4 – 14.8 GHz) and 49 elements for Vertically Linearly Polarized (VLP) X-band reception (10.7 – 12 GHz is designed with the phase changes of over 75°. This phase changes is obtained by adjusting the length of the notched spiral patch within the unit cell. Two distinct horn sources has been implemented to energize the orthogonal ports, supplying separate linear polarization for each frequency band. The efficiency is about 18.2 to 22% across different frequency bands, underscoring the array's suitability for Drone Tracking applications. From the performance measures, it is found that the proposed dual-band reflect array is more suitable for drone ground station tracking applications. Additionally, this proposed structure minimizes design complexity and meets specifications of a low profile antenna with a simple structure and reduced weight.

Keywords: Dual-band, Reflect array, orthogonally linear polarization, single reflecting layer, Low Profile

Dvopasovni odsevni niz za oddajnik/sprejemnik zemeljske postaje za sledenje dronov

Izvleček: Razvit je bil dvopasovni enoslojni odbojni niz z visokim ojačenjem za dvo-polarizirane aplikacije sledenja dronov. Enota odbojnega polja je sestavljena iz dveh spiralnih struktur s središčnim zarezovanjem, ki sta pravokotno poravnani, ločuje ju neodvisni pravokotni element s popolnim zarezovanjem. Na podlagi zasnove enote odbojnega polja je zasnovano enoslojno polje 7 x 7, ki ima 49 elementov za oddajanje v pasu Ku (12,4-14,8 GHz) in 49 elementov za sprejemanje v pasu X (10,7-12 GHz) z vertikalno linearno polarizacijo (VLP) s faznimi spremembami nad 75°. Te spremembe faze se dosežejo s prilagajanjem dolžine spiralne zaplate z zarezami v enoti celice. Za napajanje ortogonalnih vrat sta bila uporabljena dva različna rogova, ki zagotavljata ločeno linearno polarizacijo za vsak frekvenčni pas. Učinkovitost je približno 18,2 do 22 % v različnih frekvenčnih pasovih, kar poudarja primernost polja za aplikacije sledenja dronov. Iz meritev učinkovitosti je razvidno, da je predlagano dvopasovno odbojno polje primernejše za aplikacije sledenja zemeljskih postaj dronov. Poleg tega ta predlagana struktura zmanjšuje zapletenost zasnove in izpolnjuje specifikacije nizkoprofilne antene z enostavno strukturo in manjšo maso.

Ključne besede: Dvopasovno, odbojni niz, ortogonalno linearna polarizacija, en odbojni sloj, nizek profil

** Corresponding Author's e-mail: viwinsingh3@gmail.com*

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1 Introduction

The transmit and receive (Tx/Rx) communication in Drone Tracking Applications has garnered significant interest due to its ability to double the spectrum efficiency. To achieve this, high transmit-receive (Tx/Rx) isolation at the antenna layer is required, which helps reduce the complexity and cost in wireless communication systems. Hence, several Tx/Rx antennas like co-polarized shared aperture scheme with high isolation have been developed. However, extending these co-polarized designs to large-scale arrays can be complex.

Reflect array antennas known for their high gain and simple feeding mechanisms have been formulated. It typically have narrow bandwidths, but modifying the f/D ratio and aperture size can increase it by about 10% [1-2]. To make the aperture smaller and reduce cross polarization, the elements of the RA are fine-tuned using a multilayered RAs. Although these are more constructive but leads to misalignment errors [3].

Multilayer reflect arrays can enhance bandwidth by over 15%, though they are challenging to design, expensive to fabricate, and heavier than single-layer structures. To allow system frequencies to share the same aperture in a single layer, they need to be widely separated [4]. Thus, Multi-resonant single-layer elements achieve phase variation at two distinct bands by varying patch length. Three interconnected dipoles in a single layer achieve various polarizations, but wide spacing may lead to impractically large inner element spacing and narrow element patterns [5]. A design of a wide band single layer reflect array antenna using a new broadband cell is proposed [6, 7]. Single-layer dual-band circularly polarized reflect arrays combine devices operating on different frequency bands, though with relatively high side-lobe levels and cross-polarization due to high-frequency components [8]. Designs like a single reflecting layer with curved double cross elements cater to dual-band linearly polarized operation. Dielectric layers with phase delay lines and circular patches with slots are used for X-band and K-band operation. Additionally, designs using square rings with slots and parallel dipoles in a single layer demonstrate phase shift and operation in two distinct frequency bands. Circular patches added to ring structures with a single dielectric layer offer dual-band capabilities. A dual-frequency reflect array with three layers of patches of differing sizes is described, although it incurs significant processing costs due to structural complexity [9-14]. However, multilayer reflect array antennas restrict transmission phase, diminishing overall performance. Profile reduction can be achieved by reducing the number of layers, resulting in low-profile structures with high radiation efficiency and simple designs [15-18].

Dual-band reflect arrays often use two layers, making them more complex and expensive to produce. They also become heavier, which is not ideal for many uses. Single-layer elements are better because they are cheaper, lighter and easier to make [19-23]. So, this work focused on single layer elements Dual Band Reflect Array for Tx/Rx Ground Station Drone Tracking Applications.

2 Antenna design

Thus, a formulated basic single-layer microstrip element is shown in Figure 1a.

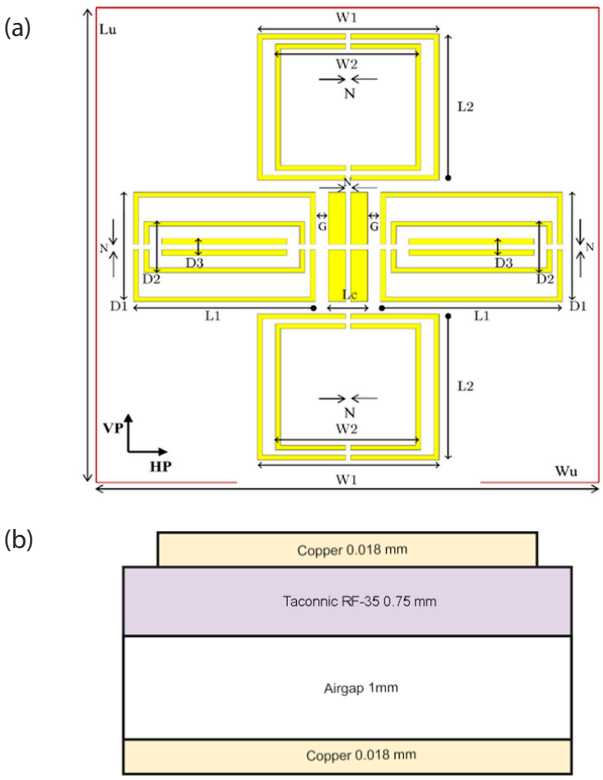


Figure 1: Geometry of unit cell in mm (a) top view b) side view

The radiating patches of the unit element module are in the shape of rectangular spirals. The rectangular spiral patches are evenly spaced relative to the origin and perpendicular to the axis of the unit cell. The horizontal centre notched spiral loop element is accountable for the horizontal linear polarized reflect array, while the vertical centre notched spiral loop element is accountable for the vertical linear polarized reflect array.

The notched rectangle element is positioned in the middle between the dual elements for polarization diversity between the operating bands and to decrease cross polarization. Horizontal and vertical elements

are positioned orthogonally and independently. This single-layer component eliminates a number of design flaws that were present in the previous designs [24-26]. In this design, there are no spatial restrictions on the elements, and they are all independent of one another.

By introducing a notch in the centre of a spiral structure, perfect orthogonal linear polarization at two frequencies can be supported. The reflect array structure is very simple and easy to fabricate, and it provides a high degree of polarization diversity. By varying the horizontal spiral loop length L1 achieved nearly 75° phase shift similarly the vertical spiral loop length L2 achieved nearly 78° phase shift. The dual element changing their length provides the smooth phase response independently.

2.1 Design and study of unit cell

The unit cells are etched on a standard Taconic RF 35 substrate, which has a dielectric constant of 3.55 and a thickness of 0.76 mm. The ground plane for transmitting and receiving frequencies is a conventional copper plane. The floquet port is used to model the unit cell structures, and a periodic boundary condition is established. A comprehensive wave analysis is then performed using the incident plane that is normal to the unit cell axis. The unit cell for transmitter frequencies is built for linear horizontal polarization. Similarly, the receiver is designed for linear vertical polarization. The unit cell performance is critical in determining the radiation performance of the planned array. To reduce phase errors, a phase range of 360 degrees or greater is required. Obtaining a smooth linear phase versus length response is also critical. The width L1 is changed to achieve a wide phase range for the transmit band's centre frequency. The width L2 is changed to obtain a large phase range for the receiver band's centre frequency [27].

2.1.1 Phase ranges for transmit band and receive band

The required phase shift at each element in flat reflect array unit cell is obtained from [1],

$$\varphi_R = K_0\left(d_i - \left(x_i cos\varphi_b + y_i\, sin\varphi_b\right) sin\,\theta_b\right) \qquad (1)$$

where, K_0 = propagation constant in vacuum, d_i = distance from phase center of the horn feed to the individual cell, (x_i, y_i) = the co-ordinates of element i. (φ_b, θ_b) = beam azimuth and elevation angle from the source.

Varying the length changes the impedance and therefore the refection phase-shift is changed. To verify this, the reflected phase versus length response for the center frequency is examined for polarization modes and is shown in figure 2a and 2b.

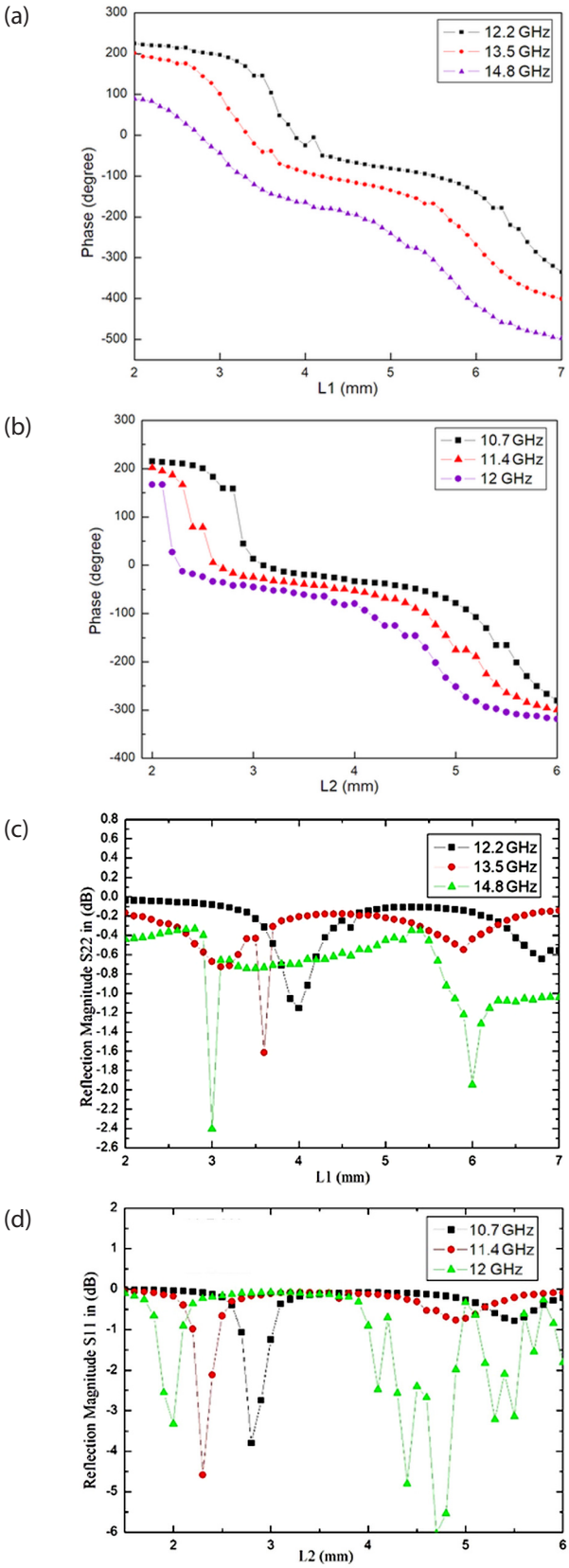


Figure 2: Reflection phase and magnitude of unit cell (a) Reflection Phase Ku-band. (b) Reflection Phase X-band. (c) Reflection magnitude Ku-band. (d) Reflection magnitude X-band.

Here, Ansoft HFSS simulation software, which provides master-slave boundaries and Floquet Ports to model repeating structures has been utilised. By changing the length, a phase shift and a change in the magnitude of the reflection field can be achieved, as shown in Figure 2.

A parametric sweep from 2 mm to 7 mm for L1 revealed a comprehensive reflected phase range exceeding 360 degrees for transmitter center frequencies, as shown in Figure 2(a) within CST MWS environment, configured for horizontal polarization (mode 2). However, in mode 1 (vertical polarization), the reflected phase range was limited to approximately 30 degrees (-140 to -170).

For reception frequencies, it's crucial that the reflecting element operates solely in linear vertical polarization, as confirmed by design findings. Remarkably, across all center frequencies in mode 1, an expansive phase range exceeding 360 degrees was observed, meeting vertical polarization requirements. Conversely, in mode 2, intentionally inferior performance was noted. Illustrated in Figure 2(B), the phase response for L2 values from 1 to 4 mm emphasizes the unit cell's exclusive operability in vertical polarization mode for receiver functionality, where it dominates in mode 1 and exhibits submissiveness in mode 2 within the complementary configuration.

The simulation results in Figures 2a and 2b show that the new unit cell has a wide linear phase range, about 500° and 300°, for the frequencies studied in the Ku and X bands. The graphs reveal that the phase response is similar at nearby frequencies. This feature can enhance the bandwidth in both frequency bands. So it can considered that all the elements are normally illuminated.

As shown in Figures 2a and 2b, when L increases, the reflection phase curve becomes more linear and the phase range also increases. Additionally, the reflection magnitude changes as the length varies.

Figure 3 shows the current distribution. Even though strong currents are generated on the resonator, the loss

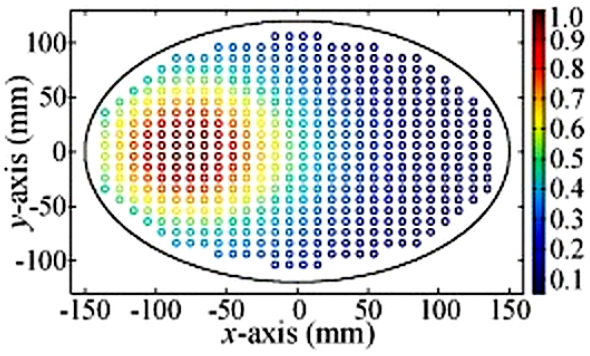


Figure 3: Current distribution

remains low because the copper has good conductivity and the substrate has almost no loss tangent. Since the loss is very small, it doesn't need to be considered in the design of the refractory antenna.

To improve scanning gain, this design keeps the positions of the feeding horns fixed. The Tx and Rx beams in the boresight direction are mainly set by the elements lined up with the feeding horns. Figure 4 shows the calculated radiation patterns based on the array factor and element pattern.

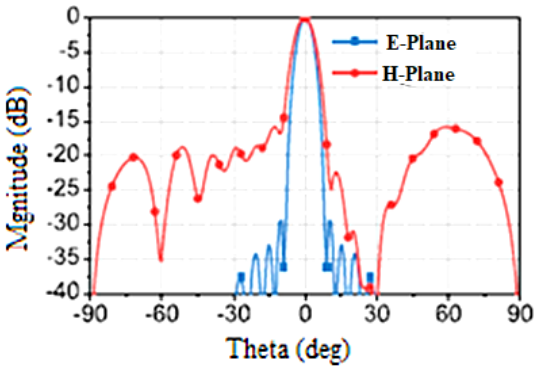


Figure 4: Radiation Patterns

The array can produce broadside radiations in both main planes. The E-plane has normal radiation, but the side lobes in the H-plane are quite strong. This indicates that the phase distribution of the other half of the array (along the positive x-axis) can impact the H-plane's radiation performance (side lobes). To reduce these side lobes, a phase distribution optimization scheme is introduced. Thus, the optimised design parameters of the proposed antenna is depicted in Table 1.

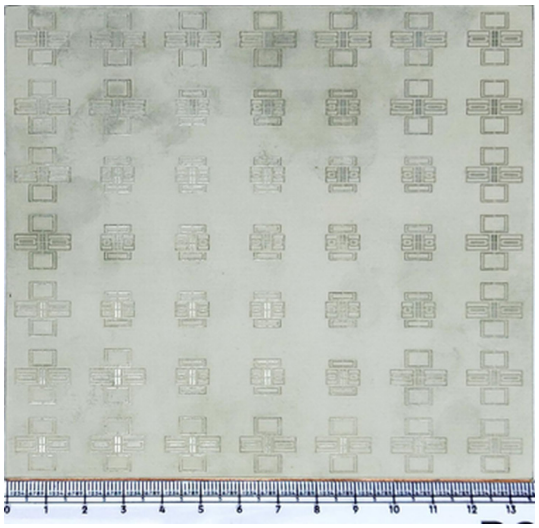
Table 1: Parameter value of the design

Parameter	Value (mm)
N	0.2
Lc	1.5
T	0.76
Tg	1
W1	7.5
W2	7
D1	7
D2	4.5
D3	1.25
Wu	19.3
Lu	19.3
G	1

Where,
N - Centered notch size (in both horizontal and vertical)
Lc -independent center notched rectangle element length,
T - Substrate thickness,

Tg -Air gap thickness,
W1 and W2 - vertical element width,
D1 and D2 - horizontal element width,
Wu and Lu - unit cell length and width.
L1 and L2 - varying horizontal and vertical spiral length for phase responses.

(a)



(b)

(c)

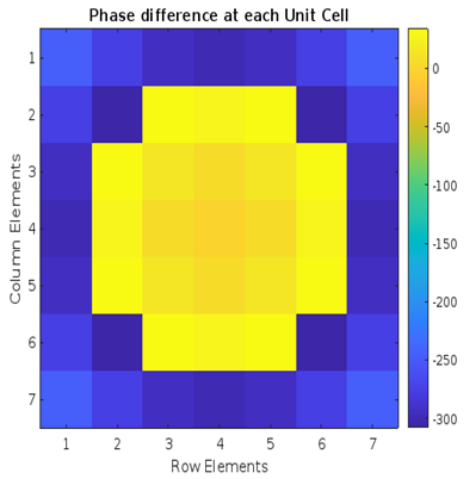


Figure 5: Fabricated single layer reflect-array antenna (a) Top View (b) Bottom view (c) Phase distribution diagram

3 Results and discussion

The unit cell elements were used to create a 7 × 7 array, resulting in a single layer that measures 135.66 mm by 135.66 mm. This array was made on a standard Taconic RF-35 lossy substrate, which has a dielectric constant of 3.55 and a thickness of 0.76 mm, with a loss tangent of 0.0018. The elements of the array were etched onto the substrate. There is a 1 mm thin air gap layer between the substrate and the ground plane to allow for wide bandwidth. The required phase for each individual element, based on its position, is listed in Table 2 is calculated using Equation (1).

The array is simulated with the CST MWS time domain solver, with the normalized impedance set to 50 ohms before simulation. Radiation properties including main lobe level, main lobe beam width, and side lobe levels were examined. Figure 5 shows the fabricated single layer reflect-array antenna.

Figure 6 shows the measurement setup. A 7×7 element reflect array was placed at a distance from the feed horn, following the ratio f/D = 1. The feed horn was connected to a standard WR34 coaxial to waveguide adapter. The reflect array was tilted at 20° with a spacer and all these components were accumulated in a dielectric frame.

The source center feed comprises a pyramidal horn antenna with an F/D ratio set to 0.8. A full wave analysis was conducted for all six frequencies. The array was modeled using a waveguide port.

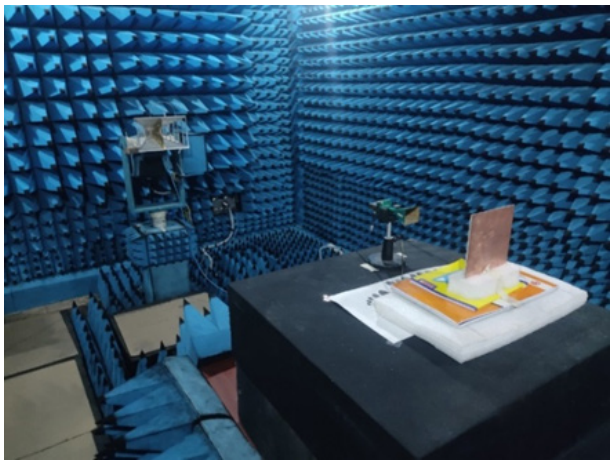


Figure 6: Measurement setup for the proposed reflect array antenna.

Figure 7 compares the measured and simulated gain radiation patterns. The measured and simulated patterns match well, although the measured gain is slightly lower than the simulated gain. These differences might be due to process errors and dielectric losses.

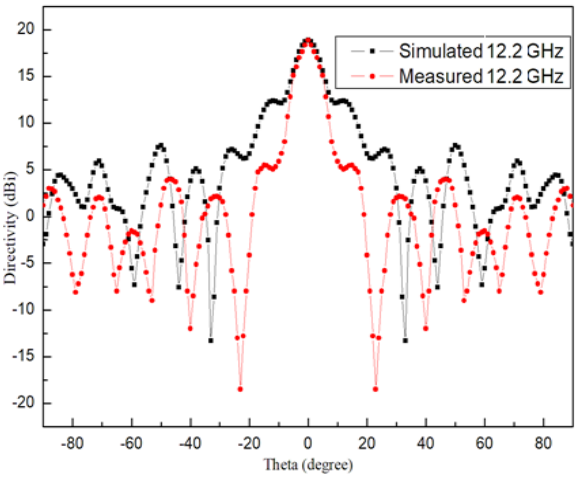
The results show that the fabrication process is effective. The transmission and reception efficiency of the reflect array antenna are 18% and 22%, respectively.

Figure 8 shows a comparison of the relative magnitudes of the simulated and measured patterns at different frequencies.

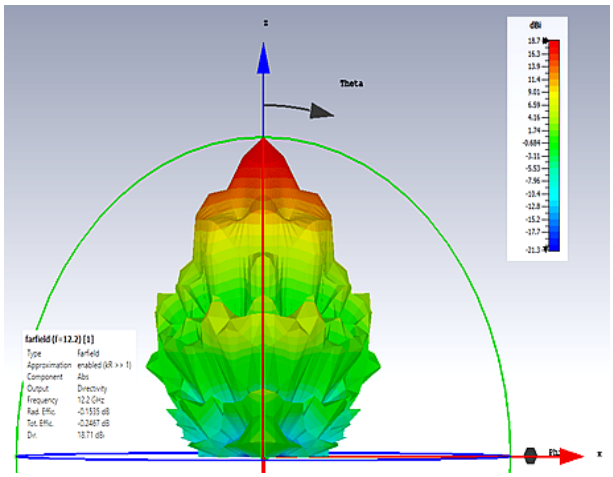
Figure 9 shows the measured S11 of the reflect array antenna. The S11 is below -14 dB in the frequency range from 10 GHz to 12.5 GHz.

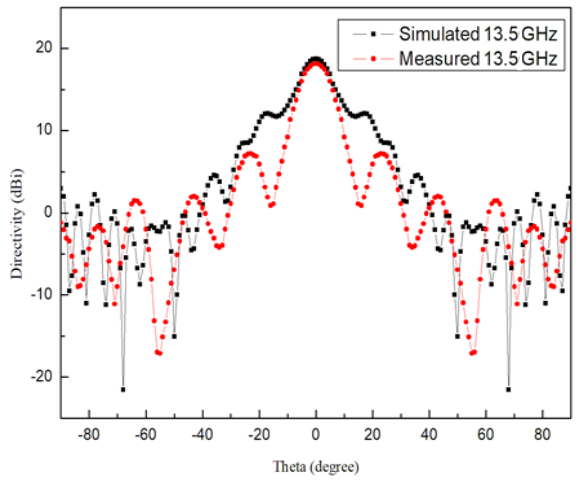
These findings suggest that the developed prototype demonstrator exhibits good electrical performance and shows potential for applications in drone systems. For performance comparisons, Table 3 lists recently reported designs of single-layer dual-band antennas.

Table 3 shows a comparison of the fabricated reflect array with existing reflect array antennas. The results show that horn centre feed blockage reduces effi-



(a)





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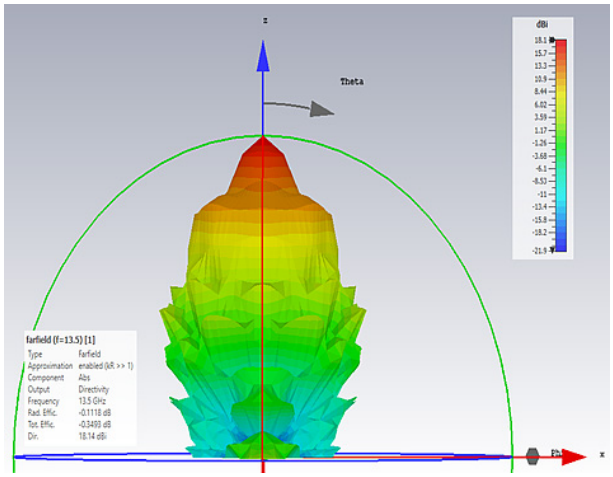

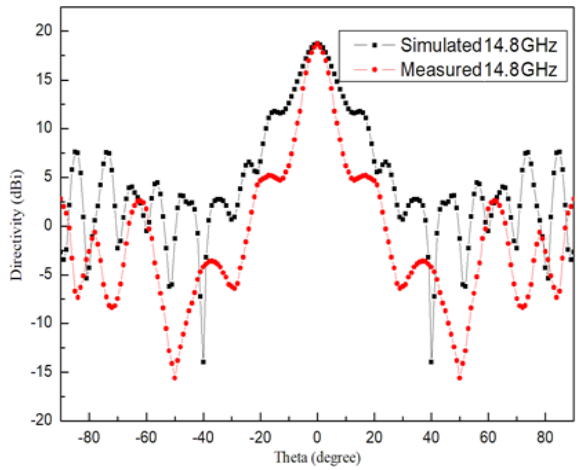

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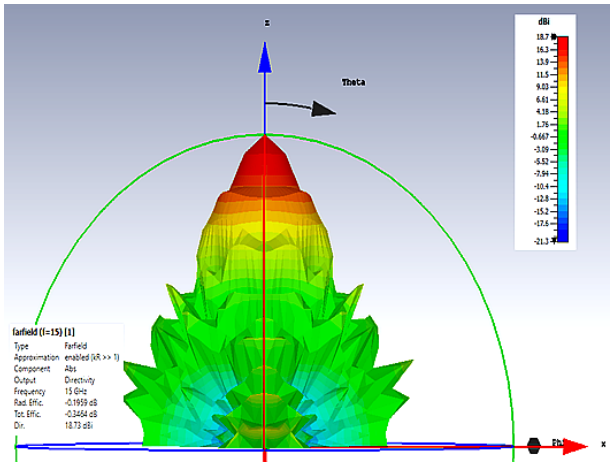

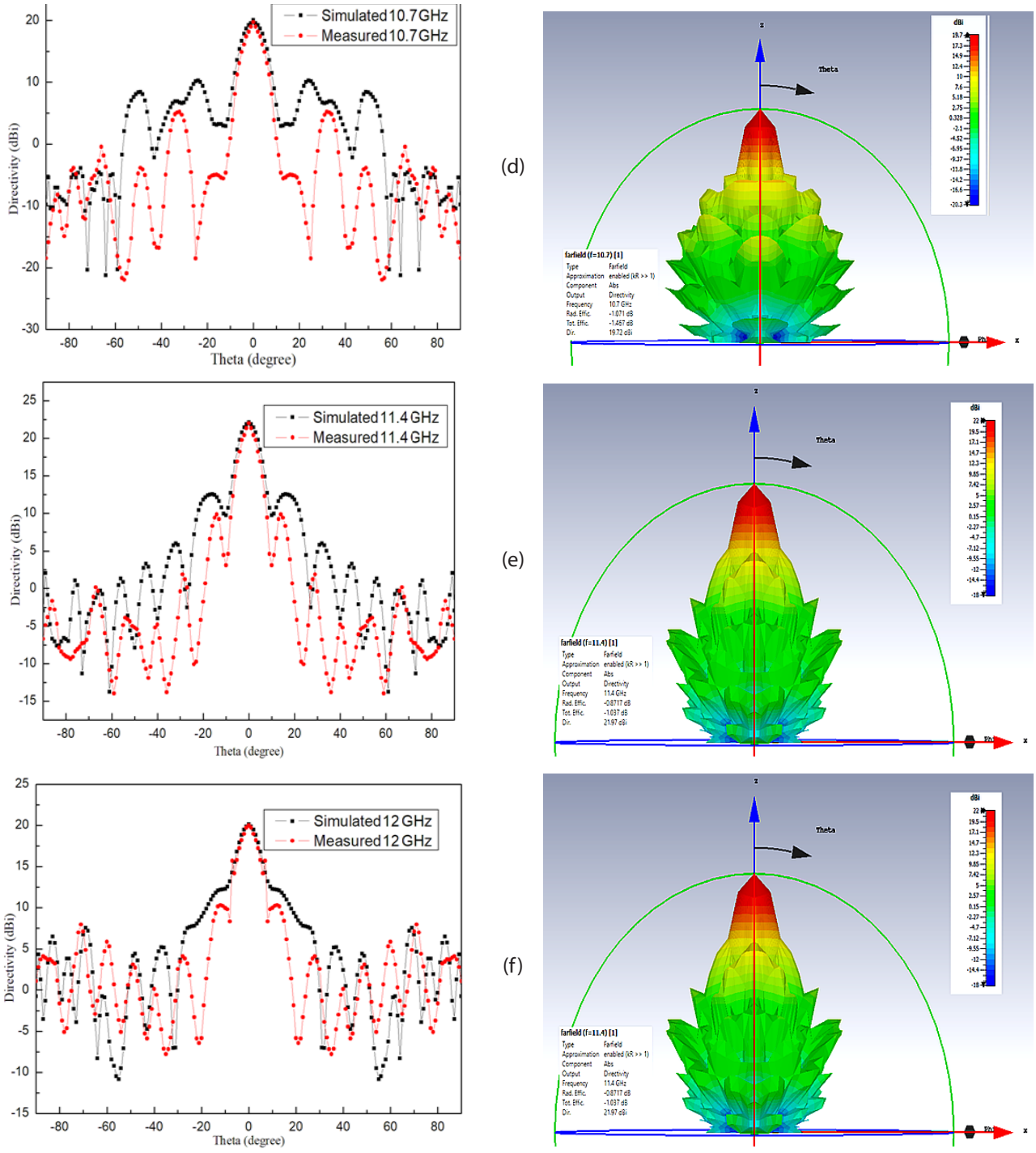

Figure 7: Simulated and tested reflect-array co-polarization radiation pattern comparison and 3D radiation pattern of transmitter bands (a) 12.2 GHz (b) 13.5 GHz (c) 14.8 GHz, receiver bands (d) 10.7 GHz (e) 11.4 GHz (f) 12 GHz

ciency. When the number of elements and aperture size of the tested reflect array antenna are compared, the higher gain is achieved. Furthermore, the ability to tune the phase of two bands independently simplifies dual band independent pattern isolation shaping at the transmitter and receiver.

4 Conclusion

This work developed a highly efficient 7 × 7 single-layer reflect array antenna with dual linear polarized modes designed for two distinct frequency bands. The incorporation of independent rectangular spirals for each band, along with strategically positioned notched square shapes within the unit cells, ensures effective

isolation between the dual elements. This proposed unit cell design presents a promising solution for various applications, including long-range communication for drone ground stations, tracker antennas, radar systems, and CubeSat satellite communication prototype unitcell, owing to its simplicity and compactness. This simulations have yielded impressive gains, with values ranging from 18.2 to 22 dBi across different frequency bands, underscoring the array's suitability for high-gain applications.

Table 2: Amount of phase shift (Degrees) required at each element position in 7 × 7 array and (L1/L2) normalized values (mm)

-146.6° (L1=5.95 mm / L2=4.47 mm)	157.32° (6 / 4.55)	122.6° (6.06 / 4.57)	110.83° (6.07 / 4.6)	122.6° (6.06 / 4.57)	157.32° (6 / 4.55)	-146.6° (5.95 / 4.47)
157.32° (6 / 4.55)	98.97° (6.15 / 4.58)	62.72° (3.62/ 2.54)	50.41° (3.65 / 2.55)	62.72° (3.62/ 2.54)	98.97° (6.15 / 4.58)	157.32° (6 / 4.55)
122.6° (6.06 / 4.57)	62.72° (3.62/ 2.54)	25.45° (3.67 / 2.58)	12.79° (3.68 / 2.6)	25.45° (3.67 / 2.58)	62.72° (3.62/ 2.54)	122.6° (6.06 / 4.57)
110.83° (6.07 / 4.6)	50.41° (3.65 / 2.55)	12.79° (3.68 / 2.6)	0° (3.7 / 2.62)	12.79° (3.68 / 2.6)	50.41° (3.65 / 2.55)	110.83° (6.07 / 4.6)
122.6° (6.06 / 4.57)	62.72° (3.62/ 2.54)	25.45° (3.67 / 2.58)	12.79° (3.68 / 2.6)	25.45° (3.67 / 2.58)	62.72° (3.62/ 2.54)	122.6° (6.06 / 4.57)
157.32° (6 / 4.55)	98.97° (6.15 / 4.58)	62.72° (3.62/ 2.54)	50.41° (3.65 / 2.55)	62.72° (3.62/ 2.54)	98.97° (6.15 / 4.58)	157.32° (6 / 4.55)
-146.6° (5.95 / 4.47)	157.32° (6 / 4.55)	122.6° (6.06 / 4.57)	110.83° (6.07 / 4.6)	122.6° (6.06 / 4.57)	157.32° (6 / 4.55)	-146.6° (5.95 / 4.47)

Table 3: Comparison of the tested reflect array with existing reflect array antenna

Ref.	Freq. (GHz)	No. of Substrate Layer	Elements Phase Range (degree)	Gain (dBi)	AE (%)	Polarization	Feed Type	Element Type
5	10/22	Single + Airgap	360 / 360	23/ 30	41/ 42	Dual LP	Center feed	Independent element with space limit
7	20/ 30	Single	More than 360	36/ 38	66.5/ 50	CP	Offset feed	Not an independent element
9	X/ K	Single + Airgap	400 / 500	26/ 29	47/25	Dual CP	Offset Feed	Not an independent with circular shape
10	X/ Ku	Single	530/ 780	23/ 25	46/33	CP	Center Feed	Independent elements with space limits. Outer border element gives space resistance.
11	X / Ku	Single	550 / 600	28 / 31	50 / 51	Dual LP	Center Feed	Independent elements. Dual elements varying length in both Horizontal and Vertical
12	X / K	Single + Airgap	400 / 400	27 / 31	63 / 42	Orthogonal LP	Center feed	Not an independent with circular shape
13	Ka / W	Dual	500/ 500	44 / 49	NA	LP	Offset feed	Independent elements situated in different layers
16	13.5 / 22	Three + Two Airgap	400 / 400	22 / 26	33 / 27	Dual LP	Center feed	Independent elements situated in different layers
Proposed work	10.7, 11.4, 12 / 12.2, 13.5, 14.8	Single + Air Gap	750 / 780	19.72, 22, 19.99 /18.87, 18.14, 18.73	47.8 / 21.3	Dual Orthogonal LP	Center Feed	Independent elements with band diversity. Not affect each other.

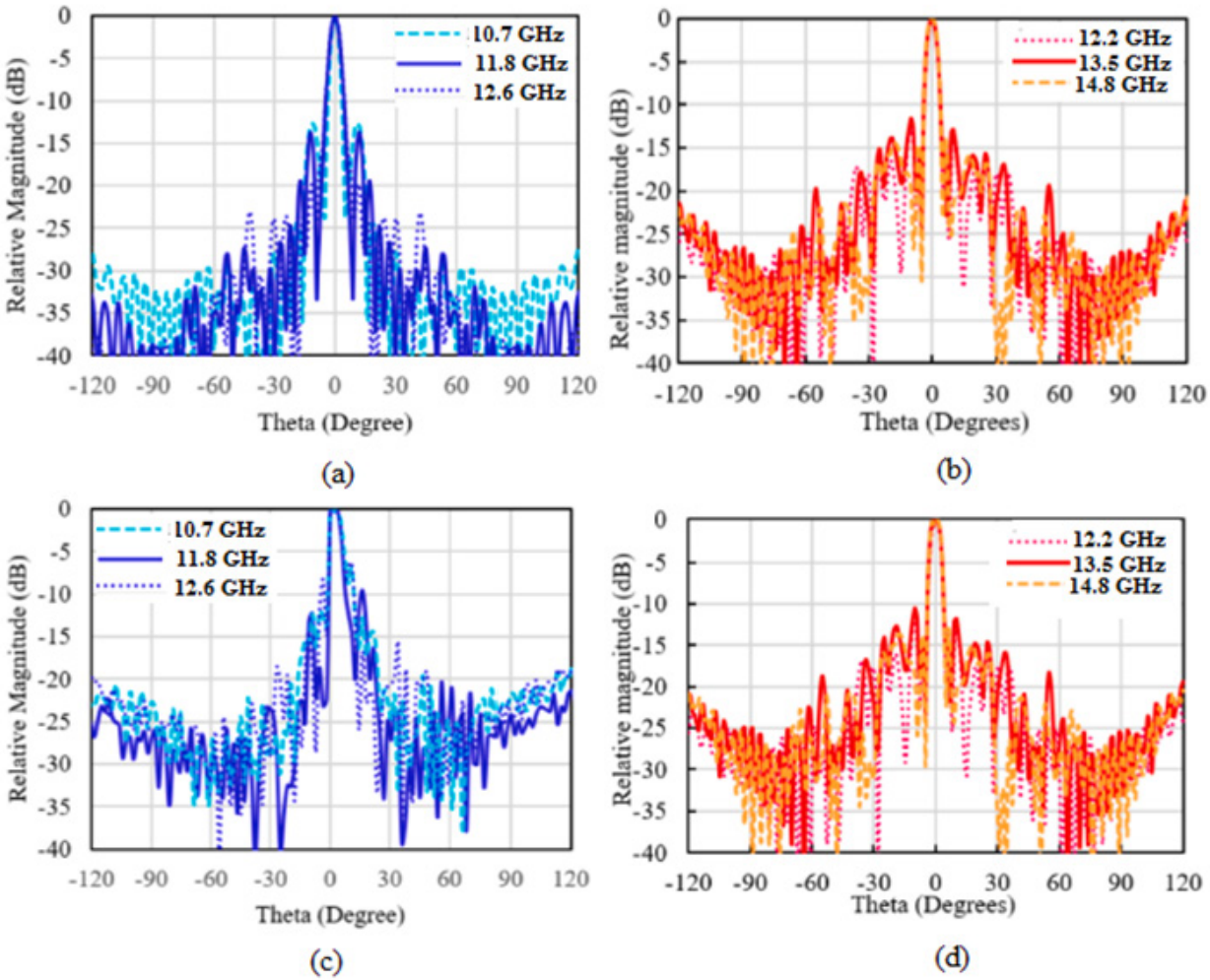

Figure 8: (a) Simulated H pattern at Receiver Band, (b) Simulated E pattern at Tx, (c) Measured H pattern at Rx, (d) Measured E pattern at Tx.

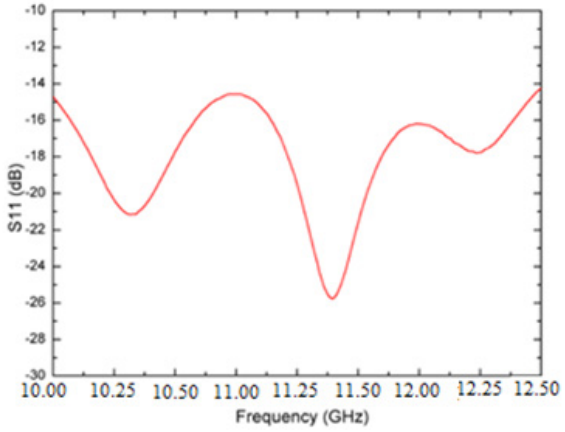

Figure 9: Measured S11 of the reflect array antenna

5 Conflicts of interest

The authors declare that they have no conflicts of interest to report regarding the present study.

6 Acknowledgment

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7 References

1. Imaz-Lueje, B., Prado, D.R., Arrebola, M. and Pino, M.R., 2020. Reflectarray antennas: A smart solution for new generation satellite mega-constellations in space communications. Scientific Reports, 10(1), p.21554. https://www.nature.com/articles/s41598-020-78501-0
2. Narayanasamy, K., Mohammed, G.N.A., Savarimuthu, K., Sivasamy, R. and Kanagasabai, M., 2020. A comprehensive analysis on the state-of-the-art developments in reflectarray, transmitarray, and

transmit-reflectarray antennas. International Journal of RF and Microwave Computer-Aided Engineering, 30(9), e22272. https://doi.org/10.1002/mmce.22272.
3. Prado, D.R., Arrebola, M., Pino, M.R. and Goussetis, G., 2020. Contoured-beam dual-band dual-linear polarized reflectarray design using a multiobjective multistage optimization. IEEE Transactions on antennas and propagation, 68(11), pp.7682-7687. https://doi.org/10.1109/tap.2020.2993014.
4. Han, C., Zhang, Y. and Yang, Q., 2017. Single-layer dual-band dual-linear-polarization reflectarray antenna with different beams for each band. Progress in Electromagnetics Research C, 73,65-73. https://doi.org/10.1109/tap.2016.2639023
5. Phua, Y.N., Lim, E.H. and Chung, B.K., 2020. Design of a single-layer broadband reflectarray using circular microstrip patch loaded with two unequal slots. AEU-International Journal of Electronics and Communications, 124, 153341. https://doi.org/10.1016/j.aeue.2020.153341.
6. Li, X. and Yang, L., 2020. Single-layer dual-band wide band-ratio reflectarray with orthogonal linear polarization. IEEE Access, 8, 93586-93593. https://doi.org/10.1109/ACCESS.2020.2986040.
7. Miklavčič, P. and Batagelj, B., 2024. A New Sum-Channel Radiating Element for a Patch-Monopole Monopulse Feed. Electronics, 13(16),p.3187. https://doi.org/10.3390/electronics13163187
8. Narayanasamy, K., Mohammed, G.N.A. and Arunkumar, S., 2024. A bandwidth-enhanced orthogonally polarized dual band reflectarray antenna. AEU-International Journal of Electronics and Communications, 176, 155155. https://doi.org/10.1016/j.aeue.2024.155155.
9. Elahi, M., Jeong, T., Yang, Y., Lee, K.Y. and Hwang, K.C., 2023. A wideband reflectarray antenna for satellite application with low cross-polarization. Applied Sciences, 13(7), p.4545. https://doi.org/10.3390/app13074545.
10. Ünaldı, S., Bodur, H., Cimen, S. and Çakır, G., 2020. RCS reduction of reflectarray using new variable size FSS method. AEU-International Journal of Electronics and Communications, 117, p.153098. https://doi.org/10.1016/j.aeue.2020.153098.
11. Tariq, S., Naseer, N., Iftikhar, A., Shafique, M.F., Nasir, J., Dahri, M.H., Fida, A. and Saka, B., 2023. Direct printable X-band low profile broadband reflectarray antenna using copper foils. AEU-International Journal of Electronics and Communications, 171, 154901. https://doi.org/10.1016/j.aeue.2023.154901.
12. Farooq, U., Iftikhar, A., Najam, A.I., Khan, S.A. and Shafique, M.F., 2023. An optically transparent dual-band frequency selective surface for polarization independent RF shielding. Optics Communications, 546, 129824. https://doi.org/10.1016/j.optcom.2023.129824.
13. Hashemi, S., Yahaghi, A. and Mohajeri, F., 2021. An optimization-based design of a wideband, polarization-independent reflectarray antenna at terahertz frequencies. Photonics and Nanostructures-Fundamentals and Applications, 45, p.100918. https://doi.org/10.1016/j.photonics.2021.100918.
14. Li, J., Mao, L. and Zhang, T., 2023. FSS sandwiched dual-frequency reflectarray for mobile communication applications. Electronics, 12(4), p.897. https://doi.org/10.3390/electronics12040897.
15. Song, W., Cai, Y., Xue, Q., Guo, N., Liu, K., Li, S., Wang, J. and Ding, H., 2022. X/Ku dual-band single-layer reflectarray antenna. Microwave and Optical Technology Letters, 64(9), pp.1621-1626. https://doi.org/10.1002/mop.33313.
16. qMalfajani, R.S. and Arand, B.A., 2017. Dual-band orthogonally polarized single-layer reflectarray antenna. IEEE Transactions on Antennas and Propagation, 65(11), pp.6145-6150. https://doi.org/10.1109/TAP.2017.2754459
17. Naseri P, Riel M, Demers Y, Hum SV. A dual-band dual-circularly polarized reflectarray for K/Ka-band space applications. IEEE Trans Antennas Propag. 2020; 68(6): 4627-4637. https://doi.org/10.1109/TAP.2020.2972650.
18. You, B.Q., Liu, Y.X., Zhou, J.H. and Chou, H.T., 2012. Numerical synthesis of dual-band reflectarray antenna for optimum near-field radiation. IEEE Antennas and Wireless Propagation Letters, 11, 760-762. https://doi.org/10.1109/LAWP.2012.2204229.
19. Dahri, M.H., Jamaluddin, M.H., Seman, F.C., Abbasi, M.I., Sallehuddin, N.F., I. Ashyap, A.Y. and Kamarudin, M.R., 2020. Aspects of efficiency enhancement in reflectarrays with analytical investigation and accurate measurement. Electronics, 9(11), p.1887. https://doi.org/10.3390/electronics9111887.
20. Encinar, J.A. and Zornoza, J.A., 2003. Broadband design of three-layer printed reflectarrays. IEEE Transactions on Antennas and Propagation, 51(7), pp.1662-1664. https://doi.org/0.1109/TAP.2003.813611
21. Ma, B., Lu, F., Zhi, G., Xue, X., Zhao, X., Ma, C., Fan, Y. and Yang, M., 2021. Development of an X-band reflectarray antenna for satellite communications. Scientific Reports, 11(1), p.6530. https://doi.org/10.1038/s41598-021-85132-6
22. Deng, R., Xu, S., Yang, F. and Li, M., 2017. Design of a low-cost single-layer X/Ku dual-band metal-only reflectarray antenna. IEEE Antennas and Wireless Propagation Letters, 16, pp.2106-2109. https://doi.org/10.1109/LAWP.2017.2698099

23. Yang, S., Yan, Z., Li, X. and Cai, M., 2022. Dual-band dual-polarized transmitarray with independent control of polarization at each band. International Journal of RF and Microwave Computer-Aided Engineering, 32(2), p.e22957. https://doi.org/10.1002/mmce.22957.
24. Abdelrahman, A.H., Elsherbeni, A.Z. and Yang, F., 2013. Transmission phase limit of multilayer frequency-selective surfaces for transmitarray designs. IEEE Transactions on Antennas and Propagation, 62(2), pp.690-697. https://doi.org/10.1109/TAP.2013.2289313
25. Raaza, A., Ramesh, S., Jerritta, S. and Rajendran, V., 2019. Circularly polarized circular slit planar antenna for vehicular satellite applications. The Applied Computational Electromagnetics Society Journal (ACES), pp.1340-1345. https://www.researchgate.net/publication/336319294_Circulary_Polarized_Circular_Slit_ Planar_Antenna_for_ Vehicular_Satellite_Applications
26. Abishek, E., Subramaniam, R., Ramanujam, P. and Esakkimuthu, M., 2023. Low-profile Circularly Polarized Conformal Antenna Array with Side Lobe Suppression for Vehicular SATCOM Applications. The Applied Computational Electromagnetics Society Journal (ACES), pp.439-447. https://doi.org/10.13052/2023.ACES.J.380608.
27. Hrovat, A., Kandus, G., Kuhar, U., Kelmendi, A. and Vilhar, A., 2016. A Ka-band satellite beacon receiver for propagation experiment. Informacije MIDEM, 46(1), pp.13-23.

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An efficient Spotted Hyena Optimizer based Multi-user Detection for Polar Encoder

Biju George George Alexander[1], Ablin Rajathurai[2], Albert Raj Anthonymuthu[3]

[1]Department of Electronics and Communication Engineering, Stella Mary's College of Engineering, Aruthenganvilai, Tamil Nadu, India
[2]Department of Electronics and Communication Engineering, Arunachala College of Engineering for Women, Manavilai, Tamil Nadu, India
[3]Department of Electronics and Communication Engineering, DMI Engineering College, Aralvaimozhi, Tamil Nadu, India

Abstract: Polar codes are among the most efficient types of error correction coding. Currently, these codes are employed in 5G communication networks and are the leading contender for 6G. Symmetry is significant in coding and decoding techniques for polar codes. However, some algorithms have high latency, and low throughput but suffer from high computational complexity. To overcome these issue a novel efficient Spotted Hyena Optimizer based Multi-User Detection for Polar Encoder (SHO-MUD) has been proposed for enhancing the throughput and reduce the latency. To increase spectrum, throughput, and energy efficiency, the SHO-MUD technique that has been suggested combines a polar encoder (PE) multiplexed with OFDMA with parity check polar coding (PCPC). PCPC-PE uses a system-configurable transmission rate to increase diversity gain and coding process dependability. To achieve optimum resource use over several data blocks, users are scheduled using the Spotted Hyena Optimizer (SHO) approach in conjunction with the MPA. The SHO scheduling efficiently allocates and schedules resources, resulting in a throughput gain of 0.6 bits per second. The suggested system provides user fairness by assuring an equal throughput of 1.55 bits/sec for all users.

Keywords: Polar Encoder; Multi-User Detection; Message Passing Algorithm: Spotted Hyena Optimizer; parity check polar coding

Učinkovito zaznavanje več uporabnikov za polarni kodirnik na osnovi Spotted Hyena optimizatorja

Izvleček: Polarne kode so ena najučinkovitejših vrst kodiranja za popravljanje napak. Trenutno se te kode uporabljajo v komunikacijskih omrežjih 5G in so glavni kandidat za 6G. Pri tehnikah kodiranja in dekodiranja polarnih kod je pomembna simetrija. Nekateri algoritmi imajo visoko latenco in nizko prepustnost, vendar trpijo zaradi visoke računske zapletenosti. Za odpravo teh težav je bil predlagan nov učinkovit optimizator Spotted Hyena za zaznavanje več uporabnikov (SHO-MUD) za povečanje prepustnosti in zmanjšanje zakasnitve. Za povečanje spektra, prepustnosti in energetske učinkovitosti predlagana tehnika SHO-MUD združuje polarni kodirnik (PE), ki je multipleksno povezan z OFDMA s polarnim kodiranjem za preverjanje paritete (PCPC). PCPC-PE uporablja sistemsko nastavljivo prenosno hitrost za povečanje raznolikosti in zanesljivosti procesa kodiranja. Za doseganje optimalne uporabe virov v več podatkovnih blokih se uporabniki načrtujejo z uporabo pristopa Spotted Hyena Optimizer (SHO) v povezavi z MPA. Načrtovanje SHO učinkovito razporeja in načrtuje vire, kar omogoča povečanje prepustnosti za 0,6 bita na sekundo. Predlagani sistem zagotavlja pravičnost uporabnikov z zagotavljanjem enake prepustnosti 1,55 bitov/s za vse uporabnike.

Ključne besede: Polarni kodirnik; zaznava več uporabnikov; algoritem za posredovanje sporočil: Spotted Hyena; polarno kodiranje s preverjanjem paritete

** Corresponding Author's e-mail: biju04@gmail.com*

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1 Introduction

Polar codes (PC) have garnered significant interest for their capacity to accomplish successive cancellation (SC) decoding and symmetric capacity on binary-input discrete memoryless channels. [1, 2]. After properly combining the input bits of several copies of the channel in a parallel concatenation scheme, the bit-channels present different reliabilities [3]. Asymptotically, as the number of copies goes to infinity, a fraction of the bit-channels becomes noiseless, while the remaining bit channels are rendered useless [4,5]. Encoding amounts to sending the data bits through the good bit-channels and the so-called frozen bits (usually zeros) through the bad bit-channels [6,7].

Polar codes are intended to separate bit channels into the most and least reliable categories [8]. The least trustworthy channels are considered frozen, meaning they record zero values while creating code words. The most reliable channels are utilized to move information bits [9]. The way the polar codes are constructed determines how reliable the bit sequence is. There exist methods for generating convolutional polar codes [11], even if the majority of studies employ the traditional block structure given in [10]. Furthermore, polar codes are joined with other codes to create a concatenated code, which boosts productivity. A cyclic redundancy check (CRC) is therefore computed before to polar encoding in 5G NR, which significantly enhances transmission noise immunity. [12,13].

In 5G communication model, PC play a crucial role in several aspects, primarily in ensuring reliable and efficient data transmission over wireless channels. PC are utilized as the channel coding scheme in the control channels of the 5G New Radio (NR) standard [14]. These control channels are responsible for transmitting critical signaling information such as synchronization signals, system information, and scheduling assignments [15]. By employing polar codes, 5G systems can achieve high reliability and efficiency in transmitting these control signals, even in challenging wireless environments.

The reliability order of bit-channels is not universal since it is determined by channel circumstances and code length. Several approaches for designing frozen sets on the fly with little complexity have been offered. The major contribution of the work has been followed by

- The proposed approach combines parity check polar coding (PCPC) with a polar encoder (PE) and OFDMA multiplexing to improve spectral, throughput, and energy efficiency.
- PCPC-PE to enhance the coding process reliability and diversity gain by employing a flexible transmission rate on the system.
- To ensure proper resource utilization of multiple data blocks, the users are scheduled by implementing the Spotted Hyena Optimizer (SHO) technique along with the MPA.

The remaining portion of the work has been followed by, section 1 illustrates the introduction, section 2 represents the literature review, Section 3 illustrates the proposed model, Section 4 describes the findings from the experiment, and Section 5 depicts the conclusion of the work.

2 Literature review

In 2021 Krasser, F.G., et al., [16] provided a unique and effective test bench and implementation for a small PC using an Intel DE10-Standard Development Kit for a System on Chip Field Programmable Gate Array (SoC FPGA). An 11% boost in throughput over a reference implementation for short PC is achieved by adopting fully-unrolled encoder and decoder architectures, which also result in high throughputs while consuming very little energy.

In 2023 Zhai, Y., et al., [17] Developed a polar code generation approach for the underwater acoustic channel that significantly decreases complexity while meeting the necessity for practical UWC. The suggested construction method and scheme also effectively ensures data transmission reliability, as demonstrated by lake-trial results under two different channel conditions.

In 2024 Pillet, C., et al., [18] describe a low-latency decoding strategy for shorter PC based on automorphism groups. The automorphism group of shorter polar codes, generated by two known shortening patterns, is shown to be finite but not empty, allowing for reduced polar code decoding with the Automorphism Ensemble (AE). Extensive simulation results for shorter polar codes using AE are shown and compared to the SC-List (SCL) approach. Shorter polar codes under AE have a block-error rate that matches or surpasses SCL while lowering decoding latency.

In 2023 Shreshtha, A. and Sarangi, S.R., [19] recommends an innovative way for appropriately using PC encoders in a 5G base station. Additionally, we offer a collection of novel resource allocation algorithms and assess their efficacy against similar methods in the literature in order to intelligently allocate user data packets across available compute nodes. Using our suggested optimization approaches, we save 17% on a 5G base station. Simultaneously, we may enhance performance by 24% over a typical base station.

In 2019 Sharma, A. and Salim, M., [20] focused on channel coding schemes, specifically for URLLC use cases in 5G New Radio (5G-NR), and analyzing the performance of polar codes for the same. Polar codes are examined using a variety of performance settings for short block lengths and low code rates, as required for the URLLC scenario. The extremely reliable polar code's exceptional error correction performance, along with its low computational complexity and decoding delay, makes it a viable candidate in the URLLC channel coding competition.

In 2021 Liao, Y., et al., [21] proposed a novel polar-code generation approach that avoids the need to sift and select bit channels depending on dependability. It is proved that using this strategy to optimize polar-code synthesis for the SCL decoder is equivalent to maximizing the anticipated benefit of traversing a maze. The simulation findings reveal that typical polar-code architectures built for successive cancellation decoders are no longer ideal for SCL decoding in terms of frame error rate.

In 2020 Xu, W., et al., [22] suggested deep learning (DL) techniques to optimising polar belief propagation (BP) decoding and concatenated LDPC-polar codes. Numerical simulations reveal that there is no performance difference between 2-D OMS and accurate BP at varied code lengths.

In 2022 Tseng, S.M., [23] employing LSTM for Polar code decoding with Markov Gaussian memory impulse noise channels. The proposed LSTM-based approach has a one-third bit error probability when compared to typical SC/BP/SCL decoding algorithms for Markov Gaussian channels. It is also 5–12 times faster in execution time and decoding delay.

In 2019 Wen, C., et al., [24] presented a technique that combines convolutional neural networks (CNN) and classic Belief Propagation (BP) decoding. We model the proposed method's performance using 4QAM and BPSK modulation. The traditional real-valued CNN approach is extended to complex-valued ones using a QAM modulation method that is detailed. The findings indicate that lowering anticipated noise increases bit error rate (BER) performance.

In 2023 Hebbar, S.A., et al., [25] provide a novel CurRIculum-based Sequential neural decoder for Polar coding (CRISP). The recommended curriculum is critical in increasing CRISP accuracy, as seen by comparisons to other curricula. To the best of our knowledge, CRISP is the first data-driven decoder for PAC codes, and it works almost optimally on the PAC (32,16) code.

3 Proposed methodology

In this paper a novel efficient Spotted Hyena Optimizer based Multi-User Detection for Polar Encoder (SHO-MUD) has been proposed for enhancing the throughput and reduce the latency

Polar codes

Erdal Arıkan (Arikan, 2009) developed polar codes, the first deterministic code architecture that achieves Shannon capacity with minimal encoding and decoding complexity. This section introduces PC and gives inspiration for our technique.

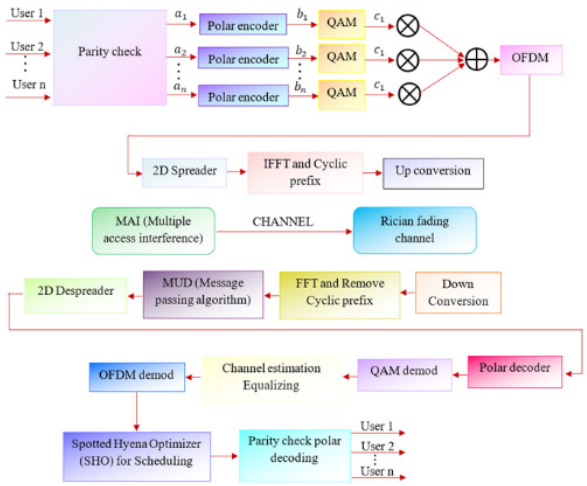

Figure 1: Proposed Methodology

3.1 Polar encoding

One linear block coding scheme, PC, encodes by modifying linear codes into systematic codes and decodes in a range of scenarios with little to no complexity. The use of a PCPC determines the system's dependability utilized a Polarization Weight (PW) evaluation and enhances BER performance. The following equations describe the coding system for linear transformations over the field F.

$$U_0^{a-1} = b_o^{k-1} G_1 \tag{1}$$

Where U_0^{a-1} represents the code word, b_o^{k-1} represents the message word, and G_1 represents the generator matrix using eqn 1

$$b_o^{k-1} = b_o^{k-1} Y, b_o^{k-1} Y_u \tag{2}$$

The first part of $b_o^{k-1} Y$ includes user information provided by to enable a free interchange between each transmission cycle.

$$b_o^{k-1}Y = b_o^{k-1_j} : j \in Y \tag{3}$$

The number of digits that are considered frozen at the start of the decoding process is provided in the second section and is shown by

$$b_o^{k-1}Y_u = b_o^{k-1_j} : j \in Y_u \tag{4}$$

Combine the equation 3,4, and 5 will written by

$$U_0^{a-1} = b_o^{k-1}YG_{1Y} + b_o^{k-1}Y_uG_{1Yu} \tag{5}$$

where, G_{1Y} and G_{1Yb} illustrates the sub-matrices of G_1 with row indices Y and Y_u. The non-systematic encoder is the name given to this kind of mapping. By appropriately selecting the set Y's size, the coding rate may be adjusted.

$$U_0^{a-1} = b_o^{k-1}YG_{1YX} + b_o^{k-1}Y_uG_{1Y_{c'}} \tag{6}$$

$$U_0^{a-1} = b_o^{k-1}YG_{1YX_u} + b_o^{k-1}Y_uG_{1Y_uX_{u'}} \tag{7}$$

$$M = 2^m \tag{8}$$

The generator matrices PC with block size m is given as

$$G = H^{\otimes m} \tag{9}$$

where, $H = \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix}$ illustrates the Kernel, and $\otimes$ denotes the Kronecker power.

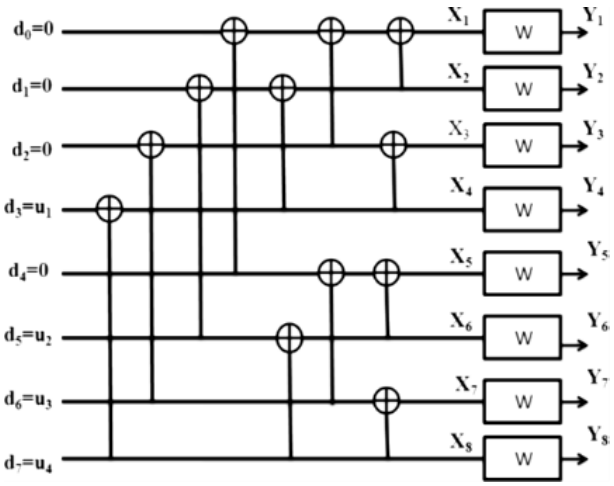

Figure 2: Polar codes encoder

Figure 2. depicts a model for PC encoding operation with (*N, K, C*^{C}) and encoding decoding complexity. *O*(*NlogN*)

3.1.1 2D Spreader

The 2D spreader receives the output from the SCMA encoder after that. Two-dimensional OFDM distribution allows for frequency reuse and frequency variation in a cellular environment. By allocating a portion of subcarriers to every receiver, OFCDM may provide multiple-access. Additionally, there is an increase in throughput along with temporal and frequency diversity. The provided symbol may be distributed using codes {+1, −1, +1, −1} in the time domain and {+1, −1} in the frequency domain. Effective transmission across a multipath fading channel is made possible by the 2D spreader.

3.1.2 IFFT and Cyclic prefix

Symbols that are sent are directed to the IFFT block, which performs 2D spreading and converts the frequency domain vector signal into a time domain signals. Guard intervals help prevent fading from many paths. The 2D spread data streams are fed into the IFFT block in the following manner to provide the orthogonality of subcarriers:

$$k(t) = \sum_{c=-\infty}^{\infty}\sum_{v=0}^{V-1} l_{c,v} Rect(t - mT) e^{j2\pi c/T} \tag{10}$$

Where $l_{c,v}$ represents the cth transmitted symbol in the vth subcarrier. Prior to transmission to the base station, the signal is up-converted.

3.1.3 Multi-User Detection (MUD) via Message passing Algorithm

MUDs are used on the receiving end to separate user data from non-orthogonal overlapping data. The number of data layer collisions on each resource piece is decreased by the sparseness of the polar codewords. Multiple Access Interference (MAI) is the main factor affecting MUD performance. The best performing but most difficult approach for handling MAI is the optimal maximal a posteriori algorithm (MAP). A straightforward technique is needed to improve MAP performance. The serial MPA is an efficient method for scheduling in ascending order on the receiving side. The serial MPA algorithm's convergence rate varies with scheduling, though. Consequently, an IWO-based MPA detection system is presented to improve its performance, which creates a path between the resource node and user node for an appropriate scheduling order.

3.2 Polar decoding

A technique for deciphering communications in polar codes is called polar decoding. PC are a kind of error-correcting codes that express data using polar coordi-

nates. Polar decoding involves converting the received signal's polar coordinates to Cartesian coordinates before applying a typical decoding method to decode it. Applications for polar decoding are numerous and include data storage and wireless communication.

3.2.1 Rician fading channel

The Rician fading version is another statistical variant that implies that the sign consists of a resilient LOS element and a random component. The LOS element is a linear channel with regular amplitude and segment that connects the transmitter and receiver.

$$P = \frac{u^2}{2\sigma^2} \tag{11}$$

$P = \frac{u^2}{2\sigma^2}$ described as the scale parameter andRatio of power contributions from line-of-sight paths to other multipaths.

The second scaling factor for the distribution is Ω, which represents the total power from both pathways.

$$\Omega = u^2 + 2\sigma^2 \tag{12}$$

$\Omega = u^2 + 2\sigma^2$ described as the total power obtained across all routes. The received signal amplitude (rather than the received signal strength) is then distributed using the following parameters in rice distribution (RD). The function of probability density is

$$u^2 = \frac{P}{1+P}\Omega \tag{13}$$

$$\sigma^2 = \frac{\Omega}{2(1+P)} \tag{14}$$

$$f(a \mid u, \sigma) = \frac{a}{\sigma^2} exp\left(\frac{-\left(a^2+u^2\right)}{2\sigma^2}\right) I_0\left(\frac{au}{\sigma^2}\right) \tag{15}$$

This leads to the following probability density function:

$$f(a) = \frac{2(P+1)a}{\Omega} \exp\left(-P - \frac{(P+1)a^2}{\Omega}\right) I_0\left(2\sqrt{\frac{P(P+1)}{\Omega}}a\right) \tag{16}$$

I n this case, I_0 is the first-kind modified Bessel function of order zero at 0th order.

3.3 Spotted hyena optimizer (SHO)

The behavior of the spotted hyena, particularly its social relationships with other animals, served as inspiration for the SHO. The spotted, striped, brown, and aardwolf are the four recognized hyena species; they differ in size, behavior, and nutrition. Out of the three hyena species, the spotted hyena is the most proficient predator. Spotted hyena females live in clans or groups.

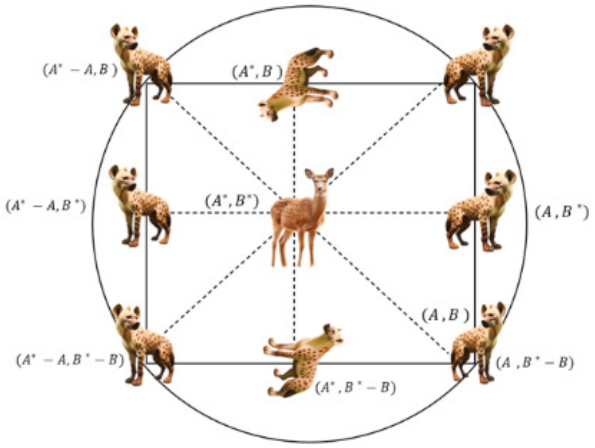

Figure 3: Position vectors in two dimensions of spotted hyena

To create SHO, the hunting tactics and social dynamics of the spotted hyena are computationally constructed. The four stages of SHO include encircling, hunting, attacking prey, and searching. Spotted hyena's position vectors in 2d are given in figure 3.

3.3.1 Encircling

In SHO, hyenas try to place themselves as close to the prey as possible, leading the group to that location. The optimal position is now approximated to be the location of the prey. Once they locate their meal, hyenas circle around it. First, the best member of the population is recognized, and others modify their views accordingly. The encircling mechanism is modeled by equation (17).

$$\overrightarrow{Di_{hy}} = \left|\vec{A} \cdot \overrightarrow{Po_{py}}(y) - \overrightarrow{Po}(y)\right| \tag{17}$$

$$\overrightarrow{Po}(y+1) = \overrightarrow{Po_{py}}(y) - \vec{F} \cdot \overrightarrow{Di_{hy}} \tag{18}$$

Equation (2) defines parameter Dt as the distance between a hyena and the prey's position. $\overrightarrow{Po}(y+1)$ denotes the hyena's newfangled location in the current repetition. The current iteration is denoted by y in Equations (18) and (19), The algorithm iteration is y, and hyenas use this equation to gauge the distance to their prey, surrounded by specific mechanisms. Equations (20) and (21) calculate vector coefficients $\vec{A}$ and $\vec{F}$, using position vectors and element-wise multiplication.

$$\vec{A} = 2 \cdot \overrightarrow{qb_1} \tag{19}$$

$$\vec{F} = 2\vec{d} \cdot \overrightarrow{qb_2} - \vec{d} \tag{20}$$

$$\vec{d} = 5 - \left(IT \times \left(\frac{5}{max_{IT}} \right) \right) \tag{21}$$

Equation (5) shows that $\overrightarrow{qb_1}$ and $\overrightarrow{qb_2}$ are random vectors in the interval (0, 1), and that h drops linearly from 5 to 0 during the iteration time. The maximum number of iterations is indicated by the max_{IT} option. An increased number of iterations is necessary to increase efficiency.

3.3.2 Hunting

Hyenas are mostly gregarious animals that hunt in packs and are adept at locating prey. In order to statistically explain hyena behavior, it is thought that the optimal search factor is an ideal component that knows the position of the prey. In order to identify the top search agent, other search agents' band together and update the best results they have found which are given in equation (22), (23) and (24).

$$\overrightarrow{Di_{hy}} = \left| \vec{A} \cdot \overrightarrow{Po_{hy}} - \overrightarrow{Po_k} \right| \tag{22}$$

$$\overrightarrow{Po_k} = \overrightarrow{Po_{hy}} - \vec{F}\,\overrightarrow{Di_{hy}} \tag{23}$$

$$\overrightarrow{C_{hy}} = \overrightarrow{Po_k} + \overrightarrow{Po_{k+1}} + \ldots + \overrightarrow{Po_{k+M}} \tag{24}$$

The first hyena's ideal location is determined by the constraint $\overrightarrow{Po_{hy}}$, whereas the other hyenas' location is indicated by $\overrightarrow{Po_k}$. Equation (10) is used to calculate the number of hyenas, which is displayed in Parameter M.

$$M = count_{ns}\left(\overrightarrow{Po_{hy}} + \overrightarrow{Po_{hy+1}} + \overrightarrow{Po_{hy+2}}, \ldots.., \left(\overrightarrow{Po_{hy}} + \vec{N} \right) \right) \tag{25}$$

The *ns* parameter in Equation (25) specifies the total number of solutions as well as all feasible solutions., where $\vec{N}$ is a random vector in the interval (0.5,1). The parameter $\overrightarrow{C_{hy}}$ represents a set of the ideal solution's number M.

3.3.3 Attacking Prey

The worth of the path h_y is decreased with the purpose of creating a mathematical model for the target attack. The vector h can have its value reduced from 5 to 0 during an iteration by reducing the change in the vector F. The pack of untainted hyenas is forced to outbreak the target if the value of F is |F| < 1, Which is given in equation (26).

$$\overrightarrow{Po}(y+1) = \frac{\overrightarrow{C_{hy}}}{M} \tag{26}$$

The ideal position is saved and updated by $\overrightarrow{Po}(y+1)$ in Equation (26), and The best agent's position determines how the other search agents are positioned.

3.3.4 Searching for prey

This method depends on modifications to the vector $\vec{F}$ that enable hunting (random search). The arbitrary numbers that force the search engine to depart from a reference hyena and are greater than or less than −1 are represented by $\vec{F}$. When compared to the non-random search phase, the random search phase computes a search agent's location based on the search agent's selection at random rather than using the current best search agent. The SHO may conduct a global search thanks to this mechanism and |F| > 1. Both of these factors highlight random search.

4 Materials and Methods

In this section evaluates and compares the performance of the proposed SHO-MUD. The experimental arrangement executed on PC with Windows 11, 13 generation Intel (R) Core (TM) is 1335U 1.30 GH2.

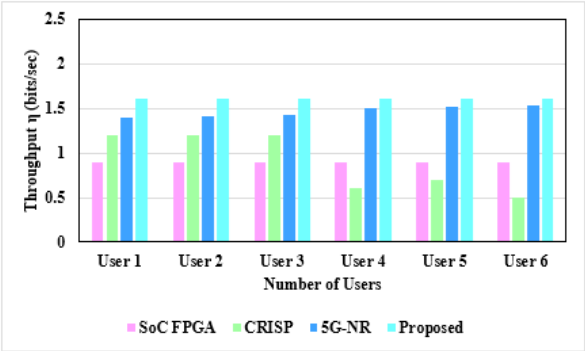

Figure 4: Number of user vs Throughput

Figure 4 depicts the analysis of throughput for each user. In this scenario, the suggested throughput results are compared to benchmark methodologies such as SoC FPGA [16], CRISP [25], and 5G-NR [20]. The SHO scheduling efficiently allocates and schedules resources, resulting in a throughput gain of 0.6 bits per second. The suggested system provides user fairness by assuring an equal throughput of 1.55 bits/sec for all users. The overall Energy Efficiency of the proposed SHO-MUD method is 1.6%. The throughput of the proposed model 1.34%, 1.36%, and 0.9% better than SoC FPGA, CRISP and 5G-NR respectively.

Figure 5 shows the variance in outage probability over the Rician fading distribution. The projected outage probability is calculated depending on the number

of interfering signals. The proposed method is 19% whereas, existing SoC FPGA has 18.6%, CRISP has 48.7% and 5G-NR has 51.23% respectively.

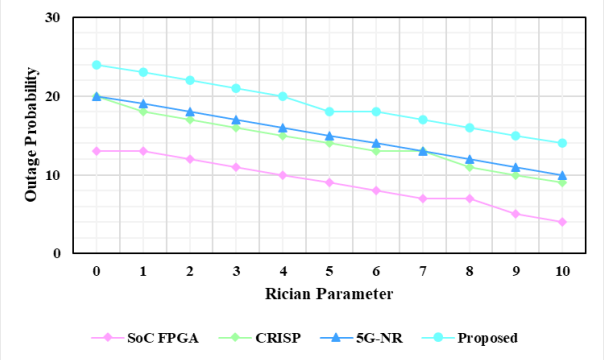

Figure 5: Rician Fading Distribution Outage Probability

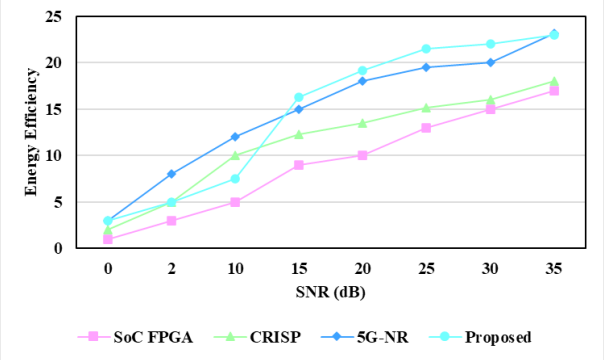

Figure 6: Energy Efficiency

Fig. 6, all techniques show an increase in energy efficiency as SNR increases. The suggested technique outperforms the existing SoC FPGA [16], CRISP [25], and 5G-NR [20] approaches in terms of EE. The average Energy Efficiency of the proposed SHO-MUD method is 31.1%. The BER of the proposed model 0.52%, 0.58%, and 0.89% better than SoC FPGA, CRISP and 5G-NR respectively.

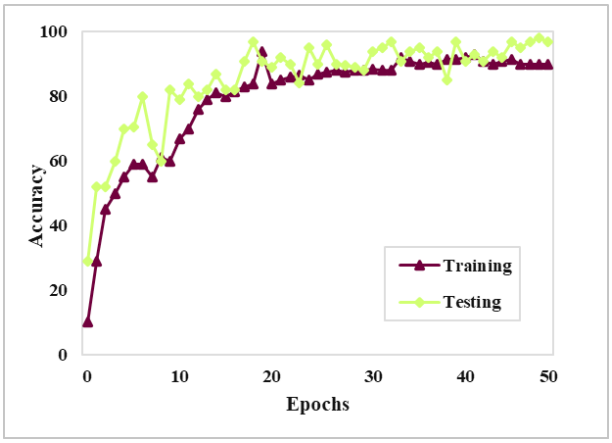

Figure 7: Performance based on training and testing sets

Figure 7(a,b) shows the horizontal axis as the number of times epoch. One epoch, out of all the examples, had one forward pass and one retrograde pass. The variation in accuracy and loss with increasing epochs is seen in Figure 7(a,b).

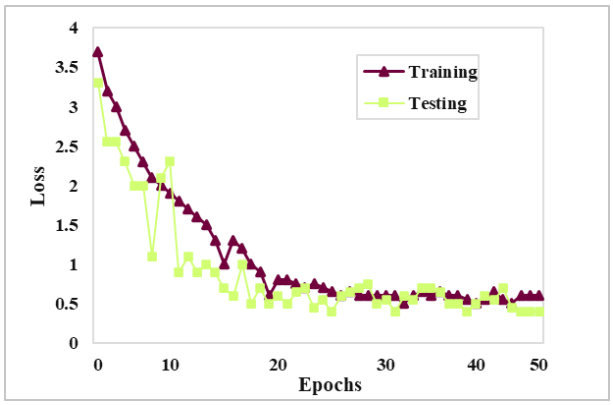

Figure 8: Normalized latency and computational complexity

Figure 8 displays the computational complexity and latency values of the suggested design with N = 32, 768, which are correspondingly normalized by the recommended values. When the decoding converges and the amount of parallelism grows, each point displays a normalized value. In comparison to the suggested decoding, the proposed decoding flexibility reduces delay at the expense of computational complexity.

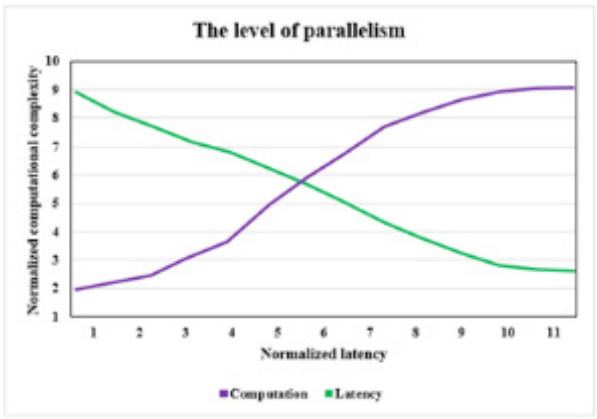

Figure 9: Convergence of iterations vs identification accuracy

Figure 9 illustrates the convergence of the pro-posed and the basic technique. It is evident from the graphic that the suggested strategy outperforms previous approaches in terms of identification accuracy. With a 90.71% accuracy the proposed method performs better the existing techniques such as SoC FPGA has 5.02%, CRISP has 4.96% and 5G-NR has 3.44% respectively.

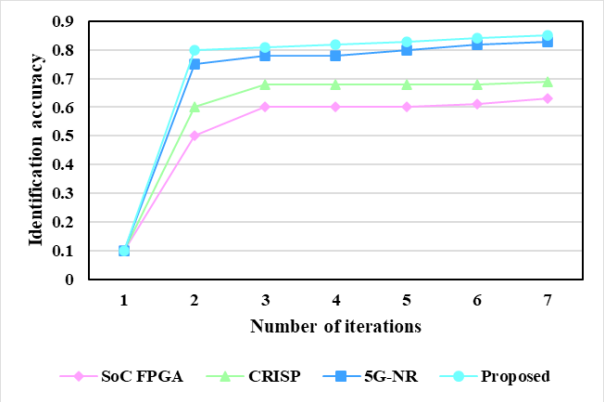

Figure 10: Number of iterations vs BER

Figure 10 displays a comparison of the detection scheme's convergence behavior. When compared to the current serial and parallel MPA approaches, the suggested scheme exhibits a greater rate of convergence after at least two rounds. The average BER of the proposed method is 7%. The BER of the proposed model 5.02%, 4.96%, and 3.44% lower than SoC FPGA, CRISP and 5G-NR respectively.

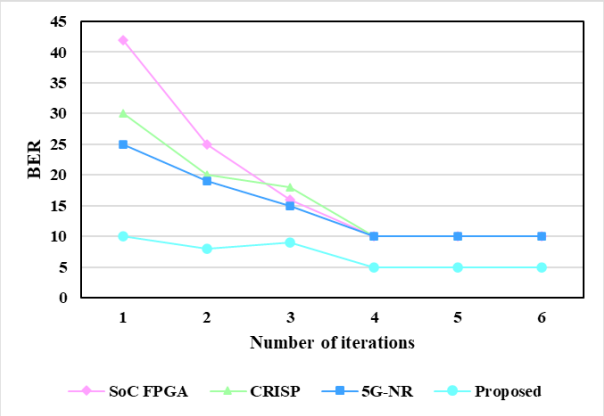

Figure 11: Target distribution for SNR = 4dB

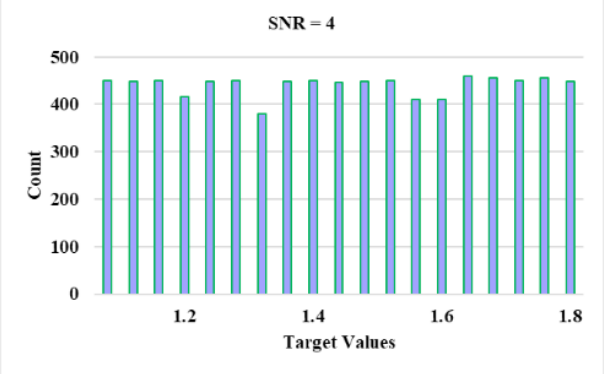

Figure 12: Target distribution for SNR= -8 dB

Fig. 11 displays the values' histogram at two distinct SNR levels, namely SNR=4 dB The target distribution for SNR = -8 dB is displayed in Figure 12. Every SNR received its own file, which was made. As a result, building models for various SNR levels is made simpler. Furthermore, a larger random collection of SNR values has been generated, which may be utilized to train a global model that can forecast for any SNR value.

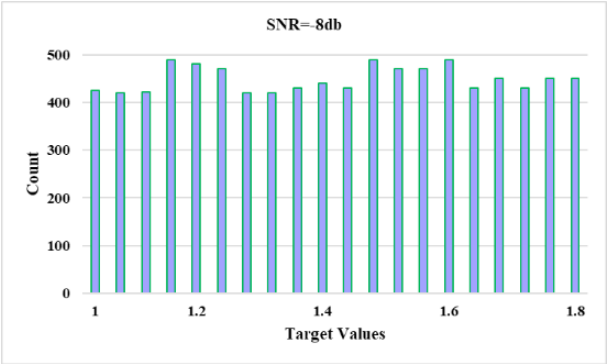

Figure 13: Comparison analysis of existing deep learning models

The accuracy obtained by ResNet, Alex Net, DenseNet, and suggested is 90.34%, 94.39%, 89.92%, and 99.5%, respectively, as Figure 13 illustrates. The suggested specificities of 91.19%, 89.98%, 90.18%, and 99.7% were attained by ResNet, Alex Net, and DenseNet. ResNet, Alex Net, and DenseNet yielded the following recommended precision values: 89.58%, 93.87%, 91.49%, and 94.29%. ResNet, Alex Net, and DenseNet yielded the following projected recall percentages: 93.51%, 89.59%, 92.87%, and 95.18%. ResNet, Alex Net, and DenseNet provide the F1 score, which is 90.31%, 89.98%, 87.89%, and 95.34%, respectively. The accuracy rate of the suggested is greater than that of the models in use at the moment.

5 Conclusions

In this section a novel efficient Spotted Hyena Optimizer based Multi-User Detection for Polar Encoder (SHO-MUD) has been proposed for enhancing the throughput and reduce the latency. Using a SHO-based MUD method, the suggested technique lowers complexity and increases convergence rate in terms of iterations. It also lowers the Bit Error Rate (BER) and achieves improved throughput and energy efficiency, respectively. The SHO scheduling effectively schedules and distributes the resources, increasing throughput by 0.6 bits/sec. By guaranteeing an equal throughput of 1.55 bits/sec for every user, the suggested technique accomplishes user fairness. The EE of the proposed method is17%, 18%, 23.2%, and 23% better than existing techniques. Future research aims to assess how well the

suggested generalized rapid decoding applies to real-world multi-kernel codes.

6 Acknowledgments

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7 Conflict of interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

8 References

1. J. Wang, and C. Ling, "Polar sampler: A novel Bernoulli sampler using polar codes with application to integer Gaussian sampling," *Designs, Codes Cryptogr.* vol. 91, no. 5, pp. 1779-1811, 2023. http://dx.doi.org/10.1007/s10623-022-01164-7
2. K. B. Priya Iyer, S. Ramesh, J. Sathiamoorthy, & A. Ahilan, "Tetra Optimization Based Hybrid Parameters for OFDM Modulated Wireless Sensor Network", *IETE J. Res.*, vol. 70, no. 5, pp. 4509–4522, 2023, https://doi.org/10.1080/03772063.2023.2225471
3. C.J. Pang, "Resource-constrained Coding for Communication and Computation Applications (Doctoral dissertation)". 2023. http://dx.doi.org/10.1007/978-3-642-20520-0_6
4. M. Prabhu, B. Muthu Kumar & A. Ahilan, Slime Mould Algorithm based Fuzzy Linear CFO Estimation in Wireless Sensor Networks. IETE J. Res., 1-11 (2023). https://doi.org/10.1080/03772063.2023.2194279
5. K. Niu, P. Zhang, J. Dai, Z. Si, and C. Dong, "A golden decade of polar codes: From basic principle to 5G applications," *China Commun.* vol. 20, no. 2, pp. 94-121, 2023. http://dx.doi.org/10.23919/jcc.2023.02.015
6. Y. Deng, S. Wu, J. You, J. Jiao, N. Zhang, and Q. Zhang, "Optimizing age of information in Polar coded status update system," *IEEE Internet Things J.* 2023. http://dx.doi.org/10.1109/jiot.2023.3290644
7. H. Hematkhah, Y. Kavian, and E. Namjoo, "PoCH: automatic HDL code generator tool for Polar channel coding decoders in multimedia communication systems," *Multimedia Tools Appl.* vol. 82, no. 24, pp. 36739-36768, 2023. http://dx.doi.org/10.1007/s11042-023-14507-w
8. M. Fletcher, E. Paulz, D. Ridge, and A.J. Michaels, "Low-Latency Wireless Network Extension for Industrial Internet of Things," *Sens.* vol. 24, no. 7, pp. 2113, 2024. http://dx.doi.org/10.3390/s24072113
9. A. Alashqar, J. Alkasassbeh, R. Mesleh, and A. Al-Qaisi, "SDR implementation and real-time performance evaluation of 5G channel coding techniques," *AEU Int. J. Electron. Commun.* vol. 170, pp. 154852, 2023. http://dx.doi.org/10.1016/j.aeue.2023.154852
10. K. Pelekanakis, P. Paglierani, A. Alvarez, and J. Alves, "Comparison of error correction codes via optimal channel replay of high north underwater acoustic channels," *Comput. Network.* 110270, 2024. http://dx.doi.org/10.1016/j.comnet.2024.110270
11. D. Yang, Y. Mao, and X. Liu, "Judgement of error frames using frozen bits and its applications in decoding of polar codes," *IET Commun.* vol. 17, no. 14, pp. 1760-1772, 2023. http://dx.doi.org/10.1049/cmu2.12651
12. T. Jiang, Y. Liu, L. Xiao, W. Liu, and G. Liu, "PCC polar codes for future wireless communications: Potential applications and design guidelines," *IEEE Wireless Commun.* 2023. http://dx.doi.org/10.1109/mwc.017.2200586
13. S. Lydia, Y.K. Gultom, S. Alam, I. Surjati, A. Alkina, A. Mekhtiyev, Y. Neshina, T. Serikov, P. Madi, K. Sansyzbay, and A. Yurchenko, "Polar Code Performance Analysis for High-Speed Wireless Data Communication System," *Journal of Theoretical and Applied Information Technology*, vol. 100, no. 05, 2022. http://dx.doi.org/10.21883/tpl.2022.08.55116.19200
14. M. Maksimovi, and M. Forcan, "Application of 5G channel coding techniques in smart grid: LDPC vs. polar coding for command messaging," *In 7th International Conference on Electronics, Telecommunications, Computing, Automatics and Nuclear Engineering-IcETRAN,* pp. 8-10, 2020. http://dx.doi.org/10.1016/j.segan.2021.100495
15. N.A. Mohammed, A.M. Mansoor, R.B. Ahmad, and S.R.B. Azzuhri, "Deployment of polar codes for mission-critical machine-type communication over wireless networks," arXiv preprint arXiv:2110.02938. 2021. http://dx.doi.org/10.32604/cmc.2022.020462
16. F.G. Krasser, M.C. Liberatori, L. Coppolillo, L. Arnone, and J.C. Moreira, "Fast and efficient FPGA implementation of Polar Codes and SoC test bench," *Microprocess, Microsyst.* vol. 84, pp. 104264, 2021. http://dx.doi.org/10.1016/j.micpro.2021.104264

17. Y. Zhai, J. Li, H. Feng, and F. Hong, "Application research of polar coded OFDM underwater acoustic communications," *EURASIP J. Wireless Commun. Networking,* vol. 2023, no. 1, pp. 26, 2023. http://dx.doi.org/10.1186/s13638-023-02236-5
18. C. Pillet, I. Sagitov, V. Bioglio, and P. "Giard Shortened Polar Codes under Automorphism Ensemble Decoding," IEEE Commun. Lett. 2024. http://dx.doi.org/10.1109/lcomm.2024.3365091
19. A. Shreshtha, and S. R. Sarangi, "Efficiently Using Polar Codes in 5G Base Stations to Enhance Rural Connectivity." arXiv preprint arXiv:2306.15476. 2023. http://dx.doi.org/10.1063/pt.5.028530
20. A. Sharma, and M. Salim, "Polar code appropriateness for ultra-reliable and low-latency use cases of 5G systems," *Int. J. Networked Distrib. Comput.* vol. 7, no. 3, pp. 93-99, 2019. http://dx.doi.org/10.2991/ijndc.k.190702.005
21. Y. Liao, S.A. Hashemi, J.M. Cioffi, and A. Goldsmith, "Construction of polar codes with reinforcement learning," *IEEE Trans. Commun.* vol. 70, no. 1, pp. 185-198, 2021. http://dx.doi.org/10.1109/tcomm.2021.3120274
22. W. Xu, X. Ta, Y. Be'ery, Y.L. Ueng, Y. Huang, X. You, and C. Zhang, "Deep learning-aided belief propagation decoder for polar codes," *IEEE J. Emerging Sel. Top. Circuits Syst.* vol. 10, no. 2, pp. 189-203, 2020. http://dx.doi.org/10.1109/jetcas.2020.2995962
23. S.M. Tseng, W.C. Hsu, and F. Tseng, "Deep learning-based decoding for polar codes in Markov Gaussian memory impulse noise channels," *Wireless Pers. Commun*. vol. 122, no. 1, 737-753, 2022. http://dx.doi.org/10.1007/s11277-021-08923-0
24. C. Wen, J. Xiong, L. Gui, Z. Shi, and Y. Wang, "A novel decoding scheme for polar code using convolutional neural network," *In 2019 IEEE International Symposium on Broadband Multimedia Systems and Broadcasting (BMSB),* pp. 1-5, 2019. IEEE. http://dx.doi.org/10.1109/bmsb47279.2019.8971888
25. S. A. Hebbar, V.V. Nadkarni, A.V. Makkuva, S. Bhat, S. Oh, and P. Viswanath, "CRISP: Curriculum based Sequential neural decoders for Polar code family," *In International Conference on Machine Learning,* pp. 12823-12845, 2023. PMLR. http://dx.doi.org/10.1109/isit50566.2022.9834589

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