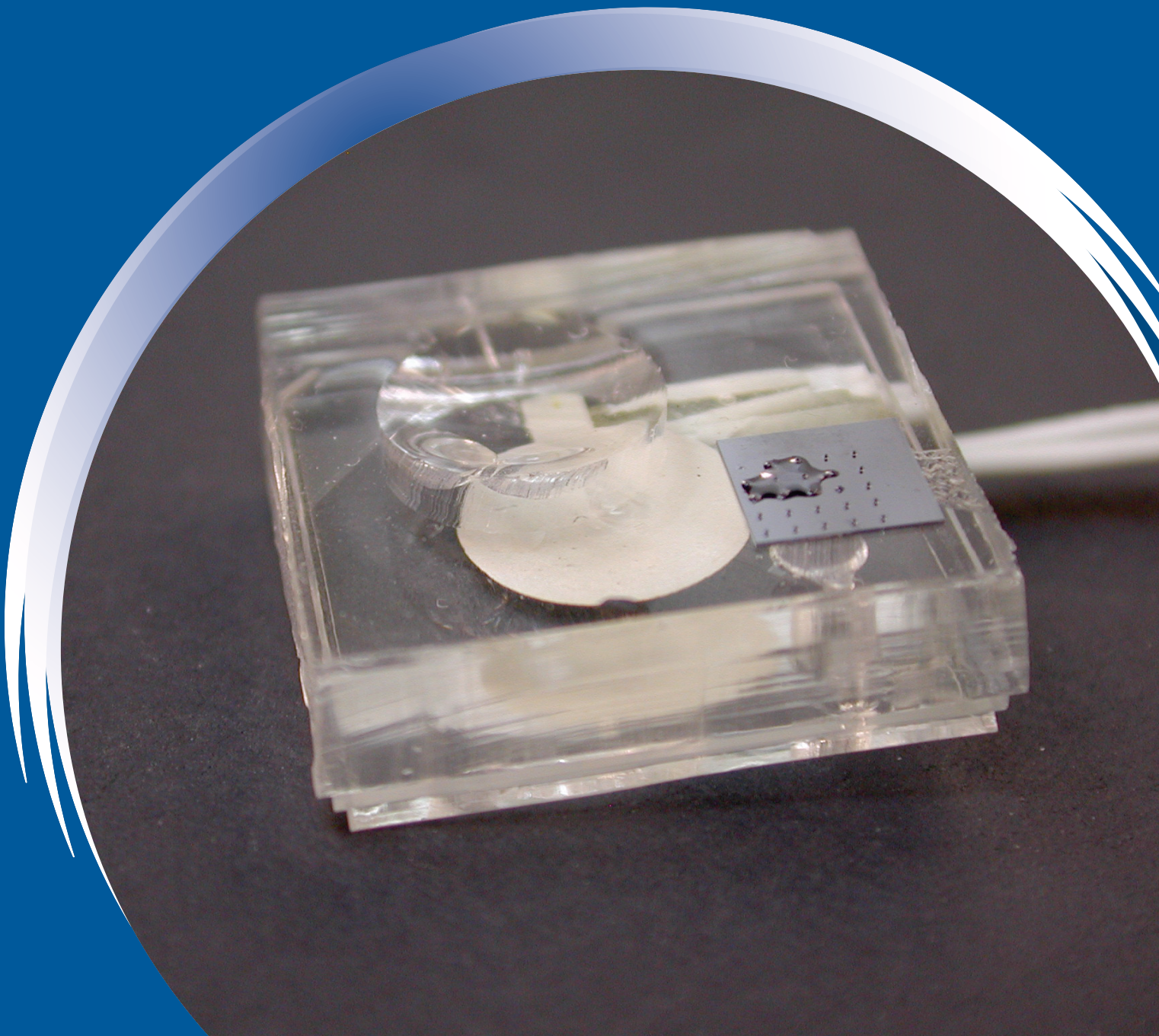
ISSN 0352-9045

Informacije MIDEM

Journal of Microelectronics, Electronic Components and Materials
Vol. 51, No. 1(2021), March 2021

Revija za mikroelektroniko, elektronske sestavne dele in materiale
letnik 51, številka 1(2021), Marec 2021



UDK 621.3:(53+54+621+66)(05)(497.1)=00 ISSN 0352-9045

Informacije MIDEM *1-2021*

Journal of Microelectronics, Electronic Components and Materials

VOLUME 51, NO. 1(177), LJUBLJANA, MARCH 2021 | LETNIK 51, NO. 1(177), LJUBLJANA, MAREC 2021

Published quarterly (March, June, September, December) by Society for Microelectronics, Electronic Components and Materials - MIDEM.

Headquarters | Naslov uredništva
Uredništvo Informacije MIDEM
MIDEM pri MIKROIKS
Stegne 11, 1521 Ljubljana, Slovenia
T. +386 (0)1 513 37 68
F. + 386 (0)1 513 37 71
E. info@midem-drustvo.si
www.midem-drustvo.si

Annual subscription rate is 160 EUR, separate issue is 40 EUR. MIDEM members and Society sponsors receive current issues for free. Scientific Council for Technical Sciences of Slovenian Research Agency has recognized Informacije MIDEM as scientific Journal for microelectronics, electronic components and materials. Publishing of the Journal is cofinanced by Slovenian Research Agency and by Society sponsors. Scientific and professional papers published in the journal are indexed and abstracted in COBISS and INSPEC databases. The Journal is indexed by ISI® for Sci Search®, Research Alert® and Material Science Citation Index™. |
Letna naročnina je 160 EUR, cena posamezne številke pa 40 EUR. Člani in sponzorji MIDEM prejemajo posamezne številke brezplačno. Znanstveni svet za tehnične vede je podal pozitivno mnenje o reviji kot znanstveno-strokovni reviji za mikroelektroniko, elektronske sestavne dele in materiale. Izdajo revije sofinancirajo ARRS in sponzorji društva. Znanstveno-strokovne prispevke objavljene v Informacijah MIDEM zajemamo v podatkovne baze COBISS in INSPEC. Prispevke iz revije zajema ISI® v naslednje svoje produkte: Sci Search®, Research Alert® in Materials Science Citation Index™.

Design | Oblikovanje: Snežana Madić Lešnik; Printed by | tisk: Biro M, Ljubljana; Circulation | Naklada: 1000 issues | izvodov; Slovenia Taxe Percue | Poštnina plačana pri pošti 1102 Ljubljana

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
vol. 51, No. 1(2021)

Content | Vsebina

Review scientific papers — Pregledni znanstveni članki

Original scientific papers — Izvirni znanstveni članki

Editorial | Uvodnik

Dear reader,

Another year is around, a special year that we will all remember. It was a year of covid-19 that continues to affect our lives and limit our freedom. For our journal it was a year of celebration, since we published the 50th volume. Thanks to open access all papers are accessible in WoS, Scopus or DOAJ by a single mouse click. We sincerely hope that the open-access papers will help us in wider dissemination and larger readership.

In 2020 we received more than 150 manuscripts, out of which only 16 have been accepted for publication so far, while 45 were out of scope and 75 manuscripts were rejected. The success rate remains low (close to 10% in 2020) primarily because we receive many manuscripts that do not meet the quality and originality that we aim at. Citation metrics with JCR IF-2019=0.340, SNIP-2019=0.353 and CiteScore-2019=0,90 is an important performance indicator. In 2020 we published 24 original scientific papers and I sincerely thank all reviewers and Editorial Board Members for their valuable contribution to the journal.

As a part of your success in science and engineering we commit ourselves to continue serving you and look forward to receiving your future manuscript(s) on our submission page (http://ojs.midem-drustvo.si/).

Stay safe and healthy!

Prof. Marko Topič
Editor-in-Chief

31 March 2021

Review scientific paper
https://doi.org/10.33180/InfMIDEM2021.101

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 51, No. 1(2021), 3 – 23

Microfluidics: a review

Borut Pečar, Drago Resnik, Matej Možek, Danilo Vrtačnik

University of Ljubljana, Faculty of Electrical Engineering, Laboratory of Microsensor Structures and Electronics, Ljubljana, Slovenia

Abstract: Microfluidics technologies have become a powerful tool in life science research laboratories over the past three decades. This review discusses three important segments of the field from origins and current status to future prospective: a) materials and microfabrication technologies from the field, b) research and development of essential microfluidic components and c) integration of components into complex microfluidic systems that will, according to some forecasts, play a key role in improving the quality of life for future generations. The most sophisticated microfluidic systems developed by now are Point-of-Care systems, that are based on Lab-on-Chip technologies. As these subfields are very extensive and go beyond the scope of this review, some carefully chosen additional review papers are provided.

Keywords: microfluidics; materials; technologies; micropumps; flowmeters; microneedles; fuel steam reformers; microdosing systems; LOC; POC

Mikrofluidika: pregled področja

Izvleček: Mikrofluidne tehnologije so v zadnjih treh desetletjih postale nepogrešljivo orodje sodobne znanosti. Pregledni članek pokriva tri pomembne segmente področja: a) materiale in tehnologije za izdelavo mikrofluidnih naprav, b) raziskave in razvoj osnovnih mikrofluidnih komponent in c) integracijo komponent v kompleksne mikrofluidne sisteme, ki bodo po napovedi mnogih imeli ključno vlogo pri zagotavljanju višje kakovosti življenja prihodnjih generacij. Med najnaprednejše mikrofluidne sisteme uvrščamo sisteme za hitro analizo na samem mestu odvzema vzorca, ki temeljijo na tehnologijah »laboratorija na čipu«. Ker področja teh sistemov presegajo obseg tega dela, smo podali nekaj dodatnih skrbno izbranih preglednih člankov s področij.

Ključne besede: Mikrofluidika; materiali; tehnologije; mikročrpalke; merilniki pretoka; mikroigle; mikroprocesorji goriva; mikrodozirni sistemi; LOC; POC

* *Corresponding Author's e-mail: borut.pecar@fe.uni-lj.si*

1 Introduction

Since Richard Feynman's thought-provoking 1959 speech "There's Plenty of Room at the Bottom", humanity has witnessed the most rapid technology development in its history—the miniaturization of devices [1]. Microelectronics was one of the most significant enabling technology of the last century. Until recently, the development of miniaturized transducer and fluidic devices lagged behind this miniaturization trend in microelectronics. In the late 1970s, silicon technology was extended to 3-D machining of mechanical microdevices, which later came to be known as microelectromechanical systems (MEMS) [2]. The development of microvalves, micropumps and microflow sensors in the late 1980s dominated the early stage of microfluidics. Since then, microfluidics is rapidly emerging as a breakthrough technology that finds applications in diverse fields ranging from biology, chemistry, pharmacy, biomedicine to information technology and optics [3].

Microfluidics can be defined as the science and technology of manipulating small amount of fluids in channels with dimensions of tens to hundreds of micrometers [4]. Due to their small scale, microfluidic devices have advantages over conventional devices. Among the advantageous properties are, large surface area to volume ratio, which lowers the diffusional distances dramatically and very low reagent consumption [4]. Consequently, they can enhance the reaction efficiency, reduce the analysis time, simplify procedures and provide highly portable systems [5]. Furthermore, they can be easy to use, cheap to fabricate and disposable [6].

The purpose of this review is to give a broad overview of the field, summarizing recent advances in materials and microfabrication technologies in relation to the field, addressing the essential microfluidic components and outlining the integration of components into wide variety of miniature-sophisticated systems capable of performing even the most demanding tasks. The remainder of the review paper is organized as follows:

Section 2 covers relevant materials and technologies for microfluidic applications. Correspondingly, silicon, glass and polymer materials will be addressed. Focus will be on precedent research activities in the field of reactive and deep reactive ion etching of silicon, dry and wet etching of glass and polymers micromachining. Since most microfluidic devices require bonding of substrates with additional functional layers to create enclosed volumes, various bonding processes such as silicon-silicon, silicon-glass and thermoplastic–polydimethylsiloxane bonding will be reviewed.

Section 3 is devoted to microfluidic components. First, an overview of micropumps, microvalves and microactuators will be given. Regarding micropump integration into modern polydimethylsiloxane (PDMS) microfluidic systems that require miniaturization and autonomy, focus in this subsection will be on PDMS elastomeric micropumps, especially on microthrottle pumps and peristaltic micropumps. Moreover, additional micropump functionalities such as bidirectional pumping and low pulsating flow will be discussed. Second, flowmeters for microfluidic applications will be outlined. Various flowmeter measurement principles and reported functional devices will be summarized. Focus will be on thermal mass microflowmeters, which have been fabricated on a wide variety of substrates. Here, past efforts which led to improvements of flowmeters sensitivity and response time, will be reviewed. Third, heaters, coolers and temperature sensors for microfluidic platforms will be addressed. Temperature is a critical parameter in managing many physical, chemical and biological microfluidic applications therefore many interesting approaches to this issue have been proposed. Fourth, overview of microneedles will be made. The microneedles are essential in microfluidic systems for transdermal drug delivery applications. They have been made from various materials using different fabrication processes and were applied using many approaches to enhance the drug delivery through the skin.

Section 4 deals with microfluidic systems, where microfluidic components discussed in Section 3 are integrated and functionally interconnected into advanced microfluidic platforms. Such systems can execute even the most demanding tasks required by the modern science. Here, several most representative microfluidics systems will be addressed, starting with micro fuel reformers, more specific with methanol steam reformers, which convert methanol solution into a hydrogen rich gas needed for fuel cells to generate electricity. Many different approaches related to this field and which have been reported in the last sixteen years and greatly improved conversing efficiency, will be reviewed. Temperature control and fuel supply for micro fuel reformers will be also addressed from the microfluidic aspect. Next, microdosing systems for drug delivery, which typically comprises several integrated microfluidic components such as micropumps, microfluidic channels, reservoirs and microneedle arrays, will be suggested. In this subsection, innovative bubble-type, shape memory alloy and other non-mechanical microdosing systems will also be tackled. At the end of the Section 4, Lab-on-Chip (LOC) and Point-of-Care (POC) systems, which are the most sophisticated microfluidic systems developed by now, will be described. As these subfields are very extensive and go beyond the scope of this review, we will provide some additional carefully chosen review papers in conjunction with foodborne pathogens detection, drug development, stem cell analysis, cardiovascular disease prevention, infectious disease diagnostics etc. Few examples of successful transformations of LOC technologies into actual POC devices will follow. Our conclusions are drawn in the final Section 5.

2 Materials and technologies for microfluidic applications

Microfluidic devices originate from microelectronics fabrication sector [7]. Silicon has been most frequently used as the base substrate material for fabrication of microfluidic devices in the past. However, silicon substrate is relatively expensive and optically opaque at certain wavelengths, limiting its applications in optical detection. To combat these shortcomings, glass and polymer materials have been introduced into microfluidic devices [7]. Polymer materials in microfluidics include polymethylmethacrylate (PMMA), polystyrene (PS), polycarbonate (PC), polyethylene terephthalate (PET), polyethylene (PE) and PDMS. Amongst these polymer materials, PDMS has been one of the most widely used materials for fabricating microfluidic devices due to its flexibility in moulding and stamping, optical transparency and biocompatibility [8].

The literature on microfabrication techniques for microfluidic applications shows a variety of approaches. Silicon microfabrication is a process that involves the removal of silicon material using wet chemical or dry plasma etching processes such as reactive ion etch-

ing (RIE) or deep reactive ion etching (DRIE) in order to create 3-D silicon or non-silicon microstructures for microfluidic devices [9]. An excellent overview of techniques involved in advanced microfabrication of silicon was written by Resnik et al. [10]. RIE has limitations in producing deep vertical silicon structures and is more often used for etching thin inorganic and organic layers. To overcome these limitations, Vrtačnik et al. [11] studied and optimized RIE of deep silicon microchannels for microfluidic applications. Optimal set of etching parameters resulted in high silicon etching rate (2 µm/min), good anisotropy close to 90°, lateral undercut less than 6% and surface roughness of less than 1 µm.

DRIE process was first introduced by Bosch in the mid-nineties and commercialized by several equipment manufactures. DRIE is capable of forming vertically smooth sidewalls at high etch rate (>10 µm min^{-1}) [12]. An improved DRIE process for ultra high aspect ratio silicon trenches with reduced undercut was reported by Owen et al. [13]. By ramping process pressure, etch power and switching time, authors were able to produce 5.7 µm trenches with an aspect ratio of 70. Giang et al. [14] reported microfabrication of shallow concave pits or deep spherical cavities in PDMS using DRIE silicon molds. Effect of DRIE process parameters on the surface morphology and mechanical performance of silicon structures were studied by Chen et al. [15]. Authors designed and performed a set of experiments to fully characterize surface morphology and mechanical behavior of silicon samples produced with different DRIE operating conditions. Similarly, Vrtačnik et al. [16] performed optimization of Bosch process for DRIE silicon microstructures. After optimization, directional Si etching resulted in etch rate of 3.0 µm min^{-1}, profile angle close to 90°, roughness of sidewalls less than 150 nm and aspect ratio higher than 10 (see test pillar structures in Fig. 1).

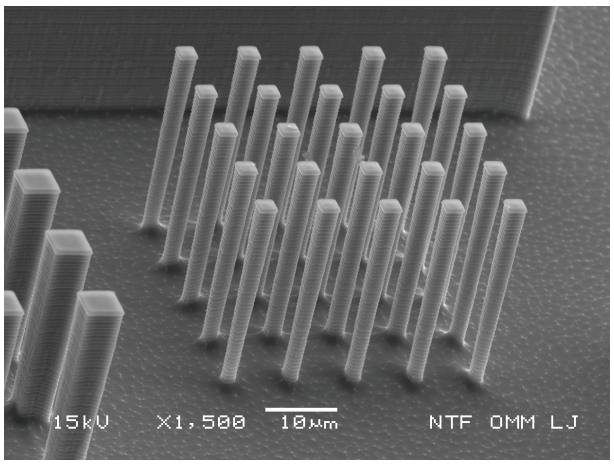


Figure 1: SEM image of test Si pillar structures fabricated by optimized DRIE etching. Source: Vrtačnik et al. [16].

For glass microfabrication, three major groups of techniques are used: mechanical treatment, dry and wet etching. Mechanical treatments include traditional drilling, ultrasonic drilling, electrochemical discharge and powder blasting. The dry etching technique of Pyrex glass using SF_6 was reported by Li et al. [17]. Authors fabricated small through holes in Pyrex glass wafers intended for electrical feed-throughs. The disadvantage of glass etching by DRIE was relatively low etching rate, which extended etching time to 10 hours. Wet etching of glass is the most common method and was reported by Stjernström and Roeraade [18]. In this work, capillary electrophoretic chips were fabricated in glass using photoresist as the mask layer. Excellent review on wet etching of glass for microfluidics was given by Iliescu [19].

For polymers micromachining, soft lithography [20], hot embossing [21], injection molding [22], casting [23], laser micromachining [24] and milling [25] are the most commonly applied.

Most microfluidic devices require bonding of substrates to create enclosed volumes for fluid handling. Therefore, various bonding processes have been developed in the last thirty years to mutually bond silicon, glass and polymer layers. Direct silicon wafer-to-wafer bonding without the use of intermediate adhesive layer was employed by Thompson et al. [26]. To heat silicon wafers above 1000 °C before they were brought into contact, electromagnetic induction was applied. Typical power consumption was in the range of 900 to 1300 W for silicon wafers with the diameter values between 75 and 100 mm. Low temperature direct bonding of silicon and silicon dioxide by surface activation method was investigated by Takagi et al. [27]. Neutralized high-energy Ar beam etching (FAB 110, Atom Tech, UK) was used to create a clean surface which had strong bonding ability. The specimens were brought in contact and bonded in vacuum. Modified process for low temperature direct silicon bonding was reported by Quenzer and Benecke [28]. After a hydrophilic pretreatment, a diluted solution of sodium silicate in water was spun onto one of the two surfaces and the two wafers were brought into contact. Resnik et al. [29,30] studied direct bonding of (111) and (100) oriented silicon wafers performed in the range of temperatures from 80 to 400 °C in nitrogen, oxygen and low vacuum atmosphere. Authors found that bond strengthening in nitrogen ambient exhibited about 25% higher tensile strength compared to bonding performed in vacuum or oxygen.

The combination of glass and silicon is a common choice for fabrication of microfluidic systems. Glass can be bonded to silicon with fusion bonding process or anodic bonding process. Fusion bonding process

as applied by Xiao et al. [31] comprises thorough silicon wafers cleaning during which Si–O–Si bonds of the native oxide on the silicon surface.The Si–O–Si bonds on the glass surface are cleaved by the attack of OH^- and H^+ ions. The new Si–OH groups on wafer surfaces are formed after the silicon and glass wafers are put together face to face in a clean room at room temperature. Resnik et al. [32,33] focused on issues accompanied with defect free anodic bonding of multilayer glass-Si-glass microfluidic structures. Pyrex 7740 and Borofloat 33 glass wafers were bonded to bare Si and Si/SiO2 terminated structures in the temperature range 350-400 °C in the air ambient under applied anodic voltages between 800-1200 V. Authors concluded that appropriate configuration of bonding electrodes was mandatory to avoid debonding effects in multilayer bonding process.

Thermoplastic–polydimethylsiloxane assemblies in the field of microfluidics gained popularity in the last ten years [34]. Many strategies for plastic–PDMS bonding have been previously reported, such as sol–gel coating approach, chemical gluing approach and organofunctional silanes approach [35, 36]. First approach requires a multiple coating procedures as well as a complex technology. Second approach creates chemically robust amine–epoxy bonds at the interface at room temperature, however, two silane-coupling reagents are required and both surfaces had to be oxidized prior to chemical modification. Third approach requires only one coupling agent. In this approach, the most widely used organofunctional silane is 3-amino propyltriethoxysilane (APTES), aminosilane frequently employed in covalent bonding of organic films to metal oxides [37]. Pečar et al. [38] studied, optimized and applied two room-temperature bonding processes for thermoplastic - PDMS polymer covalent bonding based on organofunctional silanes APTES and amine-PDMS linker (Fig. 2).

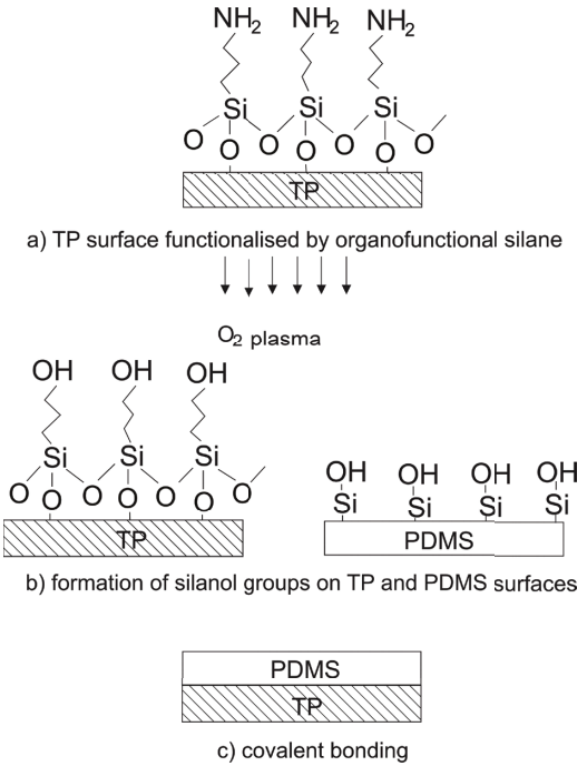


Figure 2: Process flow for thermoplastic (TP)-PDMS covalent bonding via organofunctional silanes e.g. APTES or amine-PDMS linker. Formation of Si–OH groups on both surfaces is provoked by oxygen plasma. Covalent bond is established when both surfaces are brought in contact. Source: Pečar et al. [38].

Both bonding processes were applied on piezoelectric micropumps where glass substrate was replaced by thermoplastic substrate. Water initiated the hydrolysis of covalent bonds established via the modified APTES bonding process while micropumps employing amine-PDMS linker exhibited no deterioration in their performance after eight weeks of continuous operation.

3 Microfluidic components

3.1 Micropumps

The most often encountered components in microfluidic systems are micropumps [39]. They are incorporated into the system separately as discrete components or integrated into the microfluidic platform. Division of micropumps based on Krutzch classification [40] is shown in Fig.3.

Micropumps employing displacement principle exert pressure forces on the working fluid through one or more moving boundaries, while the onesemploying dynamic principle add energy to the working fluid in a manner that increases either its momentum or its pressure. First, reciprocating micropumps require valves for its operation. Passive valves operate based on the pressure gradient, while active valves require outside actuation. In 1988, van Linte et al. [41] introduced diaphragm passive check valve. Seven years latter, Carrozza et al. reported ball valve [42]. Each ball valve consisted of a cylindrical chamber connected to a hemispherical chamber, which contained a mobile ball. First cantilever flap was reported by Koch et al. in 1998 [43]. For this flap, deep boron diffusion together with KOH etching was employed. Recently, Pečar et al. [44] proposed venous-valves micropump with valves that mimic the operation of biological venous valves. Next, reciprocating micropumps require an actuator to perform pumping function. For this purpose, piezo-

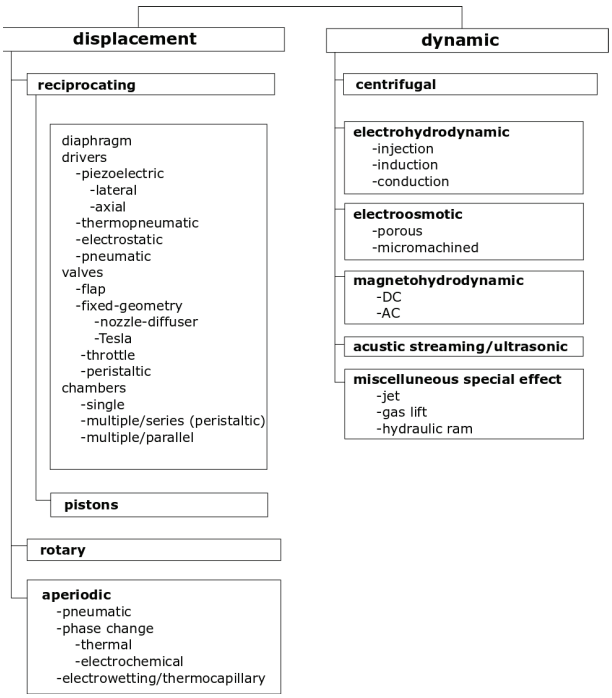


Figure 3: Division of micropumps based on Krutzch classification [40] where throttle and peristaltic pumps were additionally assigned to "valves" category.

electric, electrostatic, electromagnetic, shape memory alloy and pneumatic or thermopneumatic actuators have been applied. Piezoelectric actuation with lead zirconate titanate (PZT) has been widely utilized for micropump actuation due to small size, low power consumption, absence of electromagnetic interference and relatively low fabrication costs [45]. An effective method for reducing the excitation signal amplitudes in piezoelectric micropumps might be the use of highly efficient piezoelectric materials. The microcylinder pumps employing piezoelectric actuators based on relaxor-ferroelectric $0.57Pb(Sc_{1/2}Nb_{1/2})O_3–0.43PbTiO_3$ (PSN–43PT) was reported by Pečar et al. [46]. The performance results indicate that PSN–43PT is a promising material for high performance portable, wearable, or implantable micropump applications, where operation amplitude has to be kept low for reasons of safety and smaller plus more economic driver circuits.

A special subgroup of displacement micropumps are pumps without check valves (fixed geometry, throttle, peristaltic). Rectifying effect is accomplished (a) by geometrically asymmetric channels or structures such as diffusers [47], Tesla valves [48] or oscillating sharp-edge structures [49] shown in Fig. 4, (b) by principle of peristaltics or (c) by use of throttle rectifying elements.

Over the last decade, PDMS has become virtually the default material for forming microfluidic devices due to its simplicity of casting and bonding to the glass

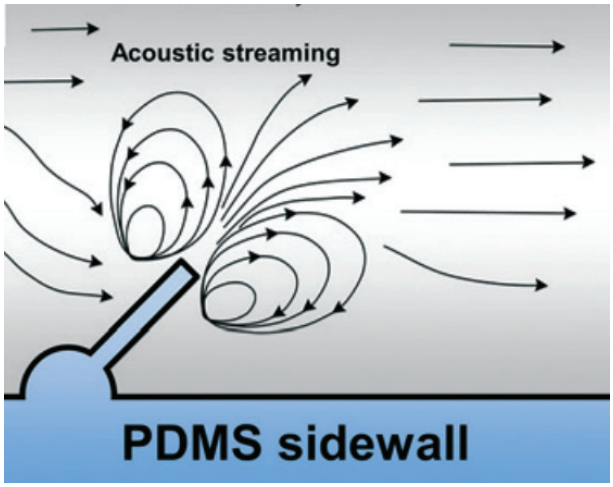


Figure 4: Acoustic streaming phenomenon around the tip of a tilted oscillating sharp-edge structure in acoustofluidic pumping device actuated by piezoelectric transducer. Source: Huang et al. [49].

substrate [50]. Regarding micropump integration into modern PDMS microfluidic systems that are required to be miniature and autonomous, micropumps fabricated on PDMS elastomer are considered as the most appropriate. Incorporation of PDMS micropumps into microfluidic systems can be found widely in the recent literature. Wang et al. [51] proposed a check valve micropump for implantable drug delivery application. A magnetic nanoparticle-PDMS composite membrane is actuated in a magnetic field to release a drug. For the same application, Gadad et al. [52] reported a dual-chamber valveless PDMS micropump. It produced 1.7 ml min^{-1} of water flowrate at excitation frequency of 14.8 Hz. Kawun et all. [53] reported a thin PDMS nozzle/diffuser micropump for biomedical applications. The pump comprised a cast PDMS body, a spin coated PDMS membrane and commercial silicone tubing, all bonded together with PDMS. The pump produced a peak flowrate of 135 µl min^{-1} and a maximum backpressure of 2.5 mbar at excitation frequency of 12 Hz and duty cycle of 25%. Chien et al. [54] proposed a ball valve PDMS/PC micropump on LOC microfluidic devices. It comprised a pair of ball valves implemented by confining a micro-ball within nozzle. Micropump exhibited maximum flowrate of 389 ml min^{-1} and a maximum backpressure of 41.5 mbar.

Regarding advanced microfluidic systems that require additional pumping capabilities and functionalities, several solutions were recently proposed. In 2018, Ye et al. [55] reported a PDMS check valve improvement for piezoelectric PDMS pumps. Authors achieved a considerable increase in the micropump flowrate performance by adding a blocking edge over conventional polydimethylsiloxane (PDMS) check valve. Generally, micropumps drive the fluid in only one direction. How-

ever, bidirectional capability is an important feature in the development of chemical analysis especially in the fluid handling application such as mixing, circulation and metering [56]. For instance, in a chemical analysis, to mix two chemical compounds, a single directional flow micropump needs an additional active rotational mechanism to create turbulent flow in mixing process. With the bidirectional flow functionality, the microfluidic system can be made in more efficient and compact structure, which merits from reducing the chemical analysis time and complexity. Recently, a research group from Malysia [57] reported a PDMS bidirectional flow dual-chamber micropump for LOC applications. Authors implemented a dispersing depth between the microchannel chamber and inlet/outlet channel in order to achieve a bidirectional flow.

For microfluidic systems where steady, low pulsating flow is required, a PDMS micropump system with additional PDMS fluidic capacitor was proposed [58]. Two single pneumatic micropumps connected in parallel exhibited maximum flowrate of 496 µl min^{-1}. It was shown, that the PDMS structure with its elastic mechanical properties smoothened pulsating flow with a smoothing factor of 0.6. In addition, Gidde and Pawar [59] addressed PDMS material properties and their influence on PDMS micropumps performance.

One sub-group of micropumps that does not employ check-valves are peristaltic micropumps. Conventional piezoelectric peristaltic micropumps comprise a series of sequentially actuated segments that deform fluidic channel on the principle of peristalsis to induce a net flow. The first piezoelectric peristaltic micropump with three piezoelectric actuators was reported by Smits in 1990 [60]. In 2003, Berg et al. [61] reported first peristaltic micropump with two piezoelectric actuators. Here, an established mechanical traveling wave was induced by a proper signal phasing of two actuation sequences. Such provoked flow-rates were comparable to three-stage peristaltic micropumps. A two-stage micropump was patented in 2010 (U.S. 20100059127 A1). A first piezoelectric peristaltic micropump with a single piezoelectric actuator was reported by Pečar et al. [62]. The fabricated prototypes featured high water / air flowrate performance (up to 0.24 ml min^{-1}/up to 0.84 ml min^{-1}) and backpressure performance (up to 360 mbar/up to 80 mbar). Furthermore, bubble tolerance and self-priming capability have been proved, together with valve regime of operation that enables sealing of the fluidic path when appropriate dc voltage was applied.

Another sub-group of micropumps that does not employ check-valves are throttle micropumps [63]. Their main advantage is high tolerance to clogging caused by mechanical particles or aggregates in the pumping medium, omitting the need for filters, which introduce significant pressure drop and increase system complexity. Furthermore, incomplete closing of rectifying elements (throttling) prevents damage to sensitive biological samples. Compared to peristaltic micropumps, microthrottle pumps exhibit superior backpressure and flowrate performance. A novel design of a strip-type microthrottle pump with a rectangular actuator geometry was proposed by Pečar et al. [64], with more efficient chip surface consumption compared to existing micropumps with circular actuators. Measured characteristics proved expected micropump operation, achieving maximal flow-rate 0.43 mL min^{-1} and maximal backpressure 12.4 kPa at 300 V excitation. In 2014, Pečar et al. [65] introduced a novel concept of microthrottle pump, named "microcylinder pump". Improved version of microcylinder pump was embedded in professional housing (see Fig. 5). Novel concept offers numerous advantages over conventional microthrottle design including self-priming ability, high level of bubble tolerance, inhibition of the cavitation occurrence and valve regime of operation.

3.2 Flowmeters

Flowmeters are prerequisite for proper operation of a wide range of microfluidics devices. Four measurement principles are frequently employed in these devices, namely thermal dilution in a flow stream, transit time measurement of a tracer injected into the flow, pressure difference measurement across a restriction and force measurement on an element placed in the stream [66].

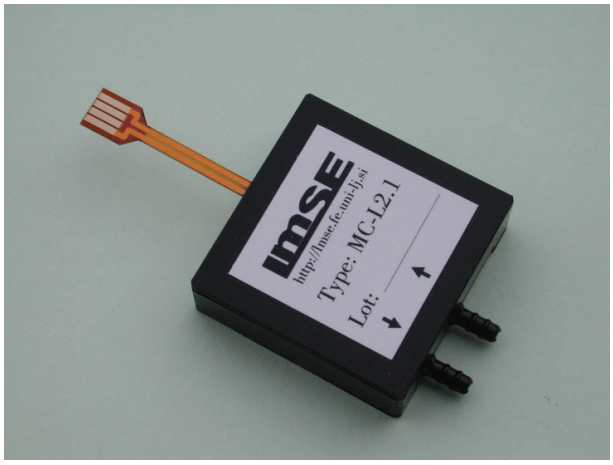


Figure 5: Piezoelectric microcylinder pump in a professional housing.

Wang et al. [67] demonstrated an electrolytic-bubble-based approach. Authors measured pressure difference (and thus flow rate) in real time by simultaneously generating two gas bubbles electrochemically along a

channel. Nezhard et al. [68] fabricated PDMS microcantilever flow sensor suitable for integration in LOC. The author's attention was focused on a high aspect ratio microcantilever, which was fabricated using a multilayer PDMS fabrication process. The device was capable of measuring flowrates as low as 35 $\mu L\ min^{-1}$. Amnache et al. [69] reported microflowmeter for moderate flowrates of gases based on a differential pressure measurement. It consisted of a microfabricated silicon–glass rectangular micro-orifice plate and two pressure sensors. Richter et al. [70] studied microflowmeter based on the micromachined electrohydrodynamic injection pump. Method is based on the measurement of the ion transit time between two grids. Another unique approach was demonstrated by Accoto et al. [71]. Their PDMS microflowmeter for closed-loop management of biological samples detected the streaming potential associated with the liquid flow by means of interface between polymeric surfaces and polar liquids and yielded a linear response. Nie et al. [72] reported microflowmeter which operated in the range of 30–250 nl min^{-1} for water. The principle was based on determining the evaporation rate of the liquid via reading the number of wetted pore array structures in a microfluidic system, through which continuous evaporation took place.

Thermal detection principles are widely used for air and gas flow sensors. An excellent state-of-the-art review in the field of thermal mass flowmeters was given by van Oudheusden [73] with the references therein. Typically, thermal mass flowmeter comprises a heating element which creates a local temperature increase and sensing elements that aim to measure the distortion in the temperature profile along the channel as induced by the fluid flow [74]. Several Si-based thermal flow sensors are currently available for measuring gas and liquid flowrates [75-77]. To enhance the device sensitivity and to improve corresponding response time, heat dissipation to the substrate should be minimized [78]. Due to the high thermal conductivity of the silicon substrate, various schemes have been implemented in order to achieve the thermal isolation of the sensing elements, such as freestanding structures, vacuum cavities and formation of porous silicon, or thin silicon nitride membranes [78]. Baek et al. [79] reported a vacuum-isolated thermal microflowmeter for *in vivo* drug delivery. Flowmeter used an arsenic-doped polysilicon heater/sensor, supported on dielectric membrane over the flow channel. Heater/sensor was capped by a vacuum-sealed microchamber to minimize heating of the surrounding structure and maximize heating efficiency.

To provide highly effective thermal isolation of the heating/sensing elements without the need for above-mentioned thermal insulation approaches and additional MEMS fabrication processes, attempts have been made to substitute silicon substrate with organic materials such as epoxy-based negative photoresist SU8 [79], polyimide [80, 81], Kapton® [82] and parylene [83]. Pečar et al. [84] proposed thermal microflowmeter for microfluidic applications where a PDMS elastomer was employed as heat insulative substrate between heater/sensor elements (Fig. 6). Device is suitable for integration on common microfluidic platform with additional PDMS fluidic components.

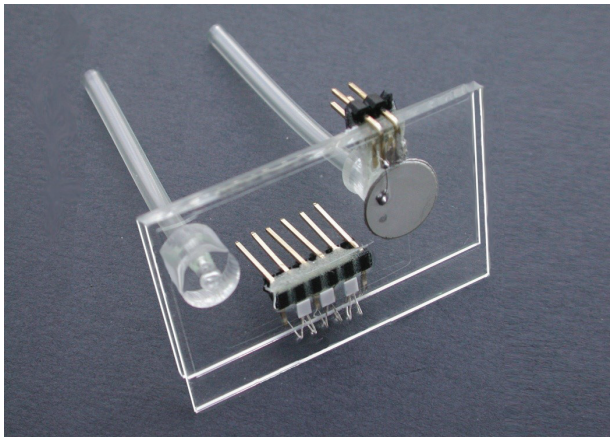


Figure 6: Thermal microflowmeter for microfluidic applications and piezoelectric micropump on common substrate by Pečar et al. [84]. PDMS elastomer is employed as heat insulative substrate between heater/sensor elements.

3.3 Heaters, coolers and temperature sensors for microfluidic platforms

Modern microfluidic systems require integration of multiple functions within a compact platform. One of such functionalities is the control of temperature, either in terms of profile or accessible range [85]. The temperature is a critical parameter in managing many physical, chemical and biological microfluidic applications such as Polymerase Chain Reaction (PCR), Electrophoresis (TGF), digital microfluidics, mixing and protein crystallization. The most commonly employed heating or cooling technologies exploit Peltier element, microwaves, pre-heated liquids, integrated wires or lasers, chemical reactions and Joule heating.

Matsu et al. [86] reported application of temperature gradient concentrator in a PDMS/glass hybrid microfluidic chip. By the combination of a temperature gradient along a microchannel using two Peltie elements, an applied electric field, and a buffer with a temperature-dependent ionic strength, Oregon Green 488 carboxylic acid was concentrated approximately 30 times as high as the initial concentration. Kempitiya et al. [87] explored the potential of microwave heating for appli-

cations requiring parallel deoxyribonucleic acid (DNA) amplification platforms. For this purpose, authors delivered microwave power at 6 GHz to the chamber via copper transmission line in a microstrip configuration. Temperatures up to 72 °C were achieved with less than 400 mW power consumption. An approach by using preheated and precooled liquids to generate a linear temperature gradient across a series of samples was employed by Mao et al. [88]. The three channel device (see Fig. 7) comprises a sandwich of glass and PDMS layers. Hot and cold fluids were introduced through the brass tubing using standard water bath circulators. The advantages of optical heating with laser are absence of the electric connections and the heating locations are more controllable comparing to the resistive electrodes. Optical approach was employed by Zhang et al. [89]. They used continuous wave laser induced heat to substitute microvalves and micropumps in microfluidic platform. Authors demonstrated effective blocking of microfluidic channels and bi directional pumping of fluid at a flow rate of 7.2–28.8 µl h^{-1}.

The interesting approach to heating and cooling in microfluidics, especially in PCR, was proposed by Guijt et al. [90]. In that work, chemical and physical processes were employed to locally regulate temperature. Cooling and heating of the microchannel was achieved by evaporation of acetone (endothermic process) and by dissolution of concentrated sulfuric acid in water (exothermic process), respectively.

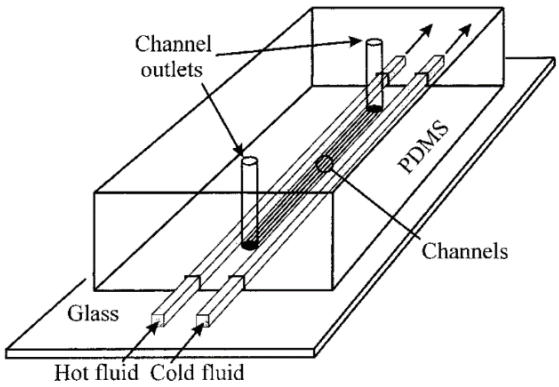


Figure 7: Three-channel device using preheated and precooled liquids by Mao et al. [88]. Reprinted with permission from [88]. Copyright (2019) American Chemical Society.

Regarding Joule heating, Mavraki et al. [91] reported low cost microfluidic device with integrated microheaters on a thin flexible polymeric substrate suitable to perform DNA amplification on a chip. The heating/sensing elements were formed on the Cu layer on the Pyralux substrate. Electrical measurements proved the functionality of the microheaters both as temperature sensors and thermal elements. Selva et al. [92] demonstrated Joule heating with electrical resistors that were fabricated by evaporating chromium (15 nm) and gold (150 nm) on the glass wafer. By applying improved optimization algorithms, the shape of resistors was optimized to generate high-temperature gradients with a linear temperature profile. Hserh et al. [93] proposed a new approach to increase the temperature uniformity inside a microthermal cycler, especially for PCR, by using new array-type microheaters with active compensation units. In this study, platinum was used as material for the microheaters and the temperature sensors. Resnik et al. [94] reported thin film Ti/Pt heaters and integrated temperature sensors on a Si microfluidic platform (Fig. 8). Heaters and sensors were fabricated by the combination of DC sputtering, lift-off process and thermal annealing of the deposited layers. Heater was able to provide vaporization of input liquid between 120 and 150 ◦C. Integrated Pt temperature sensors exhibited a typical TCR of 2200 ± 100 ppm/°C when annealed at 700 °C and proved stable during the prolonged operation.

3.4 Microneedle arrays

Microneedles are essential in microfluidic systems for drug delivery application. They are used for delivering drug through the transdermal route and for overcoming the limitations of conventional drug delivery approaches [95].

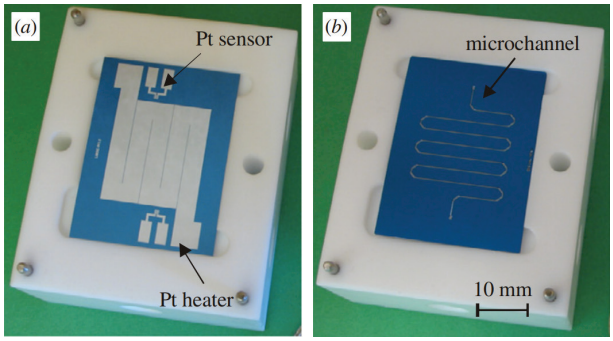


Figure 8: fabricated microfluidic platform with the meandered microchannel on the rear side (left) and a Ti/Pt heater and sensors on the front side (right) in PTFE housing.

Microneedles differ in design and composition. Currently, four distinct types of microneedles exist [96]: (a) solid microneedles often used to pretreat the skin prior to the administration of bioactives; (b) drug-coated solid microneedles for drug dissolution in the skin; (c) hollow microneedles for drug injections; and (d) dissolving microneedles prepared from a polymer in which the drug or vaccine is embedded in the polymer matrix for the controlled or rapid release in the skin. In the early

period microneedles used for drug delivery were made from silicon wafers through deep reactive ion etching and photolithography [97, 98]. Chen et al. [99] and Lin and Pisano [100] reported silicon microneedles with biodegradable tips and 6 mm-long silicon microneedles for localized chemical analysis, respectively. In the last fifteen years, various titanium [101], stainless steel [102], glass, ceramics [103] and polymeric [104-106] microneedles were introduced.

Since the diffusion of substances through the skin layers is a gradual process, microneedles systems use various approaches to enhance the drug delivery through the skin. Common methods practice electroporation, iontophoresis, sonophoresis [107], use of chemical enhancers [108], high velocity jet injection, ablation, tape stripping, vibratory, or impact assisted approaches [109]. Resnik et al. [110] reported investigation of skin penetration efficacy by a silicon microneedle array. When impact assisted penetration of microneedle array was applied instead of incremental increase of applied force, a significant impedance reduction of up to 50% on animal skin and 95% on human skin was obtained, which was a strong evidence of successful skin penetration.

Several publications have appeared in recent years documenting many successful microneedle arrays applications. In recent study, Deng et al. [111] for the first time evaluated the ability of solid silicon microneedle array for punching holes to deliver cholesterol-modified housekeeping gene (GAPDH) siRNA to the mouse ear. Such development of siRNA therapies has significant potential for the treatment of skin conditions (alopecia, allergic skin diseases, hyperpigmentation, psoriasis, skin cancer, pachyonychia congenital) caused by aberrant gene expression. In 2020, Kim et al. [112] delivered coronaviruses-S1 subunit vaccines by dissolving microneedle array. MERS-S1 subunit vaccines elicited strong and long-lasting antigen-specific antibody responses in mice, implyingthat it is a promising immunization strategy against coronavirus infection. For diabetic patients, insulin delivery using hollow microneedle array is very desirable. In experimental study of in vivo insulin delivery conducted by Resnik et al. [113], two types of fast-acting insulin were used to provide evidence of efficient delivery by hollow microneedle array to a human subject (Fig. 9). Results of *in vivo* insulin delivery proved successful infusion of fast-acting insulin as shown by blood analyses. Recently, a new cell transplantation method to inject donor cells into tissues to treat certain diseases using an array of ultrathin microneedles was reported by Iliescu et al. [114]. Here, an array of silicon microneedles was successfully employed to inject fluorescently labeled Mardin–Darby canine kidney cells into rat liver tissue.

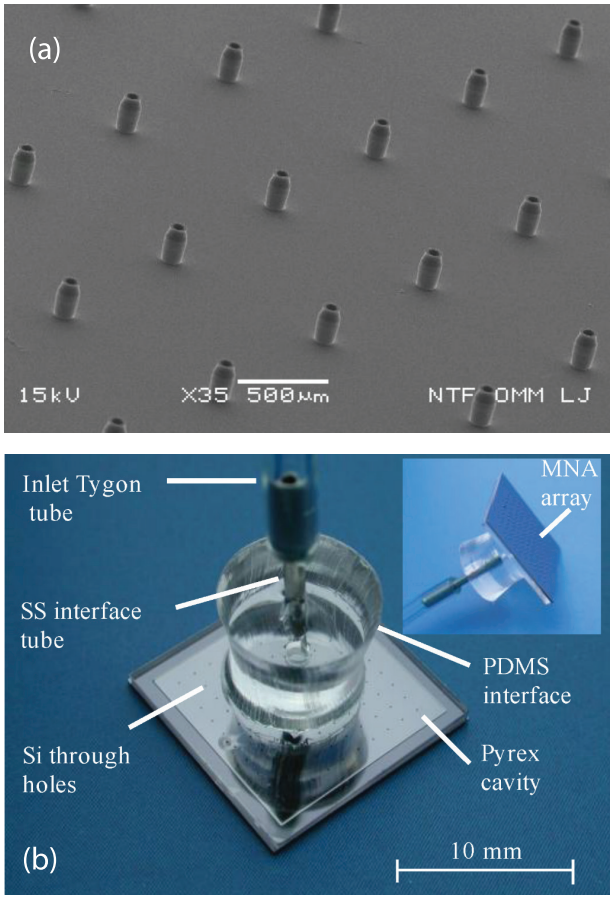


Figure 9: SEM image of hollow Si microneedles array fabricated by DRIE etching (a) and assembled microinjection device with 100 microneedles (b) view from the rear side, showing fluidic connection, distribution cavity and through holes. Source: Resnik et al. [113].

4 Microfluidic systems

4.1 Micro fuel reformers

With the rapid advancement in technology, everyday application of electronic devices such as laptops, cell phones, music players and other portable devices has become inevitable. Li-ion batteries are good options for providing the required energy for such devices. However, they require time-consuming recharging and are generally difficult to be recycled [115]. In contrast, liquid hydrocarbon fuels contains enormous energy per volume and weight compared to the best existing batteries, refueling is more convenient than recharging and recyclable fuel cartridges are more environmentally friendly. From the above reasons, various approaches were proposed to convert liquid hydrocarbon fuels to electrical power at micro-scale, such as using miniature gas turbine generators, fuel cells, thermo electric generators, a thermophotovoltaic generator and a thermi-

onic generator [116]. Among them, a miniature hydrogen fuel cell system combined with a microfluidic fuel reformer seems one of promising candidates to power mobile devices. Microfluidics technologies enabled fabrication of catalyst coated microchannels with large surface area to volume ratio, which greatly increased fuel conversion efficiency. Methanol is one of the best choices for the hydrogen production since it is a liquid at room temperature and can be easily stored in small cartridges premixed with water.

In 2004, Pacific Northwest National Laboratory developed a micro integrated methanol reformer, which was equipped with a microcombustor, an evaporator and a CO methanizer [117]. It was small enough for portable electronics but limited to 3.55 ml min^{-1} hydrogen production. Kamura et al. [118] reported a miniaturized methanol reformer with $Cu/ZnO/Al_2O_3$ catalyst-based microreactor shown in Fig. 10. The microreactor (25 × 17 × 1.3 mm^3) was constructed from glass and silicon substrates. The use of the high-performance catalyst allowed for higher hydrogen production rates than using a commercial Cu/ZnO catalyst. The microreactor was demonstrated to be capable maintaining a hydrogen production rate suitable for powering 1 W-class devices.

Hsueh et al. [119] presented a numerical investigation of the transport phenomena and performance of a plate methanol steam micro-reformer with serpentine flow field as a function of wall temperature, fuel ratio and Reynolds number. Jeong et al. [120] studied hydrogen production by steam reforming of methanol over Cu/Zn-based catalysts. Among the catalysts tested, $Cu/ZnO/ZrO_2/Al_2O_3$ exhibited the highest methanol conversion and the lowest CO concentration in the outlet gas.

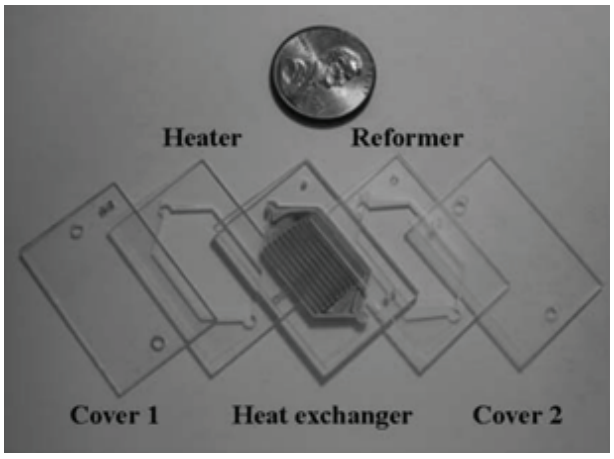


Figure 10: Individual glass wafers of MEMS methanol reformer heated by decomposition of hydrogen peroxide. Source: Kim et al. [121].

Kim et al. [121] proposed micro methanol reformer with a heat source. The micro system consists of the methanol steam-reforming reactor, the hydrogen peroxide catalytic decomposition reactor and a heat exchanger between the two reactors. Catalyst loaded supports were inserted in the cavity made on the glass wafer. The total hydrogen production rate was 23.5 ml min^{-1}. This amount of hydrogen can produce 1.5 W of power on a typical proton-exchange membrane fuel cells.

To improve the energy conversion of a micro-channel reactor, Mei et al. [122] proposed and fabricated an innovative microchannel catalyst support with a microporous surface. Results showed that the microchannel catalyst support with micro-porous and non-porous surfaces had a hydrogen production rate of 18.07 ml min-1 and 9.65 m min-1, respectively at 573 K under the inlet flowrate of 30 µl min-1. Huang et al. [123] studied the fractal channel pattern design and the gradient catalyst layer in relation to their effects on the performance of a methanol micro steam reformer. Compared to a uniform catalyst layer, the fractal design effectively increased the conversion ratio by 8.5% and decrease CO by 11% when the inlet liquid flow rate was fixed at 1.0 cc min-1. Recently, Sarafraz et al. [124] conducted series of experiments for the hydrogen production via steam reforming of methanol with Cu–SiO2 porous catalyst coated on the internal walls of a micro-reactor with parallel micropassages. Wang et al. [125] proposed a partial oxidation methanol micro reformer with finger-shaped channels for low operating temperature and high conversing efficiency. Micro reformer supplied hydrogen to fuel cells by generating 2.23 J min-1 for 80% H2 utilization and 60% fuel cell efficiency at 2 ml min-1 of supplied reactant gas.

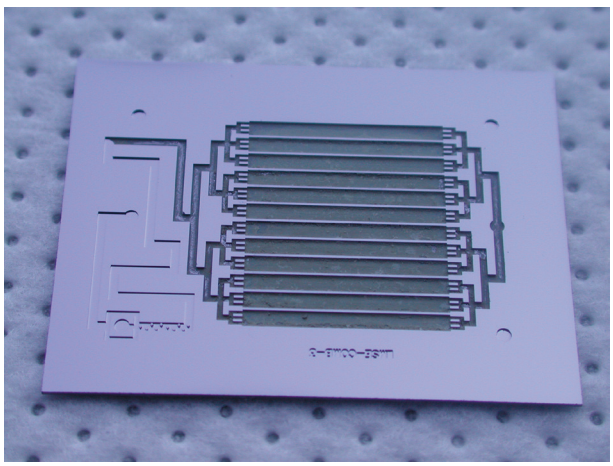


Figure 11: Si based micro catalytic methanol–oxygen combustor with thin film nanostructured Pt/CeO_2 catalyst in microchannels.

To maintain the required reactions taking place in micro reformer unit, a micro combustor is commonly

employed. The most convenient approach is to utilize the same energy source (methanol) for steam reforming process and for catalytic combustion. In this case the methanol–air or methanol–oxygen mixture should be provided for combusting process. Correspondingly, Resnik et al. [126] studied Si based micro catalytic methanol–oxygen combustor with thin film nanostructured Pt/CeO_2 catalyst (Fig. 11). The goal of the study was to reduce the catalyst load and to maximize the catalyst effectiveness through better mass transfer by implementing of the new high performance mesoporous Pt/CeO_2 catalyst with multiple layer deposition method and by the proposed micro combustor design.

For proper operation of methanol fuel microreactor, precise temperature control and uninterrupted fuel supply is mandatory. Temperature control of methanol fuel microreactor for hydrogen production was reported by Peruško et al. [127]. The temperature control was achieved by on-off control with an adjustable hysteresis. The heater actuation circuit comprised a boost converter, controlled by pulse width modulated signal from the microcontroller. The output of the boost converter was applied to the platinum (Pt) heater in the microreactor evaporation stage. To pump the fuel into microreformer, a fuel supply system is required. Pečar et al. [128] proposed a low cost, energy efficient flow-generator for hydrogen production in microreactors. The proposed approach is energy efficient and suitable for implementation into a compact hybrid device, small enough to fit on microreactor housing.

4.2 Micro dosing systems for drug delivery

A typical microdosing system comprises micropump, microsensor, microfluidic channel, reservoir and electronics. It is mainly aimed at serious chronic diseases, such as diabetes, melancholia, malignant lymphoma, etc., or abrupt life threats, such as heart attack, stroke, septicaemia etc. [129]. With the automatic dosing system, the patients are protected from sudden death or irregular/incorrect taking medicine. Microdosing systems are fabricated using bio-compatibile materials such as poly methyl methacrylate, poly-pimethylsiloxane, SU-8 photo resist, or parylene C [129].

Bubble-type and other non-mechanical microdosing systems need no physical actuation components but its effectiveness, due to long time delay and slow response, are much devalued [129]. Bohm et el. [130] proposed a closed-loop controlled micromachined dosing system for accurate manipulation of liquids in microsystems down to the nanoliter range via expanding electrochemically generated gas bubbles. Another solution was described by Reynaerts et al. [131]. An implantable drug-delivery system based on shape memory alloy micro-actuation was based on a precisely controlled discontinuous release from a pressurized reservoir by using a shape memory actuated microwave system. One dose can be controlled with accuracy up to 5 µl. However, shape memory alloys dosing systems suffer from a relatively low flowrate and insufficient bio-compatibility [129]. A microdosing device comprising a dosing chamber, dispensing opening and vibration unit was patented by Koerner et al. [132]. Vibration unit was connected to at least one boundary surface of the dosing chamber. Consequently, boundary surface oscillated for the purpose of a dispensing operation. A plastic micro drug delivery system was successfully demonstrated by Ianchulev et al. [133], utilizing the principle of osmosis without any electrical power consumption. The system had an osmotic microactuator and a polydimethylsiloxane (PDMS) microfluidic cover compartment consisting of a reservoir, a microfluidic channel and a delivery port. Induced osmotic pressure could extend up to 25 MPa to overcome possible blockages caused by cells or tissues during drug delivery operations. Than et al. [134] reported a strategy using an eye patch equipped with an array of detachable microneedles. Microneedles penetrated the ocular surface tissue, and served as implanted microreservoirs for controlled drug delivery. System comprised micro-seized membrane in sealed microfluidic reservoir, piezoelectric microcylinder pump and array of hollow Si microneedles. Biocompatible components were covalently bonded to each other to form a compact wearable system. Complete emptying of 590 µl sealed reservoir needed suction pressure of less than 50 millibars which minimized power consumption that is crucial for long device autonomy.

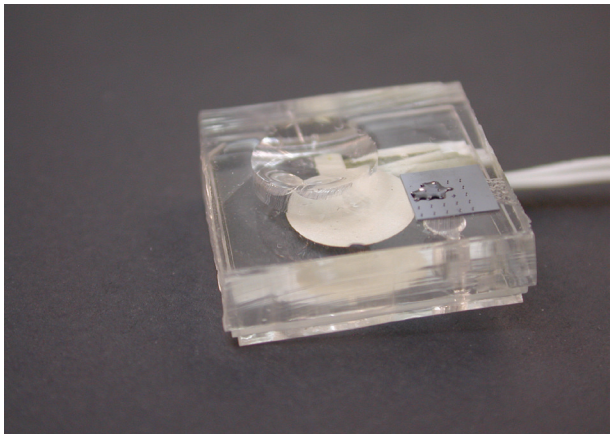


Figure 12: Wearable integrated microdosing system for transdermal drug delivery by Vrtačnik et al. [136,137].

Kabata et al. [135] fabricated insulin pump using the volume change of hydrogen bubbles and conducted experiments using rats. To monitor the blood glu-

cose level, a glucose sensor was employed. Recently, Vrtačnik et al. [136, 137] proposed and patented wearable integrated microdosing system with a microneedle array for transdermal drug delivery (Fig. 12).

4.3 Lab-on-Chip and Point-of-Care systems

One of the main objectives of microfluidic technologies is to provide a total solution, from sample input to display of the analyzed results [138]. Complete analytical protocols, from sample pretreatment through to sample and reagent manipulation, separation, reaction and detection can be performed automatically on well-designed and integrated miniaturized devices such as LOC systems. LOC devices are a subset of MEMS devices and often indicated by "Micro Total Analysis Systems" (μTAS) as well [139]. LOC devices comprise microchannels, integrated pumps, electrodes, valves, sensors and electronics to perform required tasks [140]. The term "Lab on Chip" was probably first used [141] by Moser et al. from Technical University Vienna [142] to describe the miniaturized thin film glutamate and glutamine biosensors developed by them. Research on LOC focuses on several applications including human diagnostics, DNA analysis and synthesis of chemicals [140]. The miniaturization of biochemical operations normally handled in a laboratory has numerous advantages, such as cost efficiency, parallelization, ergonomics, diagnostic speed and sensitivity.

LOC systems offer advantages for pathogen, toxin and virus detection. A review by Yoon et al. [143] summarized the requirements of LOCs for foodborne pathogens detection and gave an overview on immunoassay and PCR-based LOC biosensors. A review by Weigl et al. [144] highlights LOCs for drug development, advances in LOC technology for flow-injection analysis, electrokinesis, cell manipulation, proteomics, sample preconditioning, immunoassays, electrospray ionization mass spectrometry, and polymerase chain reaction. Overview on LOC technologies for stem cell analysis was presented by Ertl et al. [145]. Authors focused on the advantages of the microfluidic devices to overcome most of the challenges associated with stem cell identification, expansion and differentiation. Por et al. [146] focused on the latest developments in environmental LOC monitoring devices and provided future perspectives to overcome the challenges using printing technologies. Wu et al. [147] made a short review on LOC platforms for detection of cardiovascular disease and cancer biomarkers. Ai et al. [148] summarized recent progress in LOCs for pharmaceutical analysis and pharmacological/toxicological tests. Authors gave insight into the challenges and possible breakthrough of Pharm-LOCs development.

POC diagnostic systems are instruments that can rapidly provide in vitro diagnostic results by non-trained personnel at a patient site, in the physician's office, in the field, at home, in an ambulance, or in a hospital [149]. There has been a growing need to provide diagnostic results at the point of care, for prompt treatment of acute diseases such as acute myocardial infarction and for home-care diagnostics such as diabetes monitoring. In many ways, the features of microfluidics and LOC technologies are a natural fit for POC diagnostics devices [150]. Bringing the LOC technology to life through POC devices is a challenging task. So far, there have been only a few successes in the transformation of LOC technology to the actual POC devices with a real life application [151]. A review of POC diagnostic systems using microfluidic LOC technologies was recently given by Sia at al.[152]. This review covers advances in POC technologies, commercially available POC diagnostic systems and microfluidic LOC technologies. Park et al. [153] summarized advances in microfluidic PCR for POC infectious disease diagnostics. In this review, authors discussed practical issues and perspectives related to implementing microfluidic PCR technologies into infectious disease diagnostics. Further on, in recent years, paper-based microfluidics has emerged as a multiplexable POC platform [154]. Paper-based microfluidics is considered a low-cost, lightweight, and disposable technology [155]. A review on paper-based microfluidic POC diagnostic devices was given by Yetisen et al. [156], covering fabrication of paper-based microfluidic devices, functionalization of microfluidic components and quantitative readouts via handheld devices and camera phones.

Examples of successful transformations of the LOC technologies into an actual POC devices are encouraging. Ahn et al. [157] demonstrated a disposable plastic biochip incorporating smart passive microfluidics with embedded on-chip power sources and integrated biosensor array for applications in clinical diagnostics and POC testing. Neuzil et al. [158] demonstrated a high performance polymerase chain reaction system in portable LOC for POC. Sun et al. [159] designed, fabricated, and tested miniature 96 sample ELISA-LOC for immunological detection of Staphylococcal Enterotoxin B. Their simple POC system is useful for carrying out various immunological assays and other complex medical assays without a laboratory. Upaassana et al. [160] reported highly sensitive LOC immunoassay for protein biomarker that causes lung inflammation (see Fig. 13). Authors drastically reduced analysis time to about 30 min as opposed to hours in conventional methods. Recently, several authors demonstrated an integrated POC solution for noninvasive diagnosis and therapy monitoring of heart failure patients [161]. KardiaPOC™ is an easy to use portable device with a disposable LOC

for the rapid, accurate, non-invasive and simultaneous quantitative assessment of four heart failure related biomarkers from saliva samples.

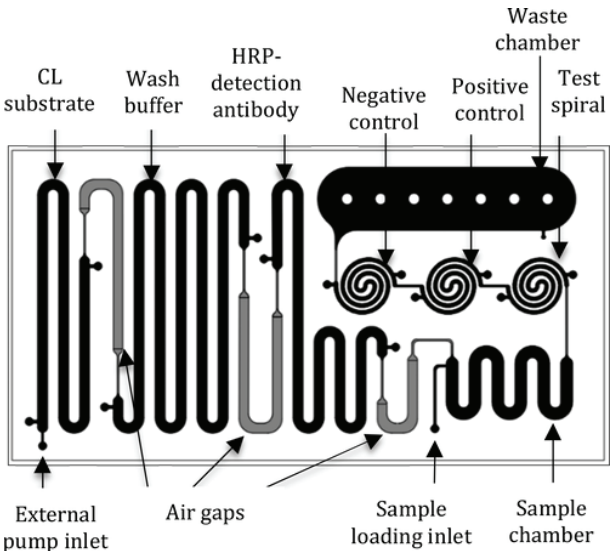


Figure 13: Schematic diagram of the highly sensitive LOC for POC immunoassay for protein biomarker that causes lung inflammation by Upaassana et al. [160]. On-chip reservoirs store assay reagents. Air gaps isolate reagents and prevent mixing while in storage and during the assay. Reprinted with permission from [160]. Copyright (2019) American Chemical Society.

5 Conclusions: Future perspective of the field

The field of microfluidics has grown into a mature technology capable of producing the most complex microfluidics systems that push the boundaries of today's scientific and technological advances. Many challenges still lie ahead, but the main challenge remains how to translate a wide variety of successful microfluidic concepts from laboratory prototypes to robust end-user products in order to be more accessible. Many fabrication processes currently employed in laboratory environment, including manually performed PDMS soft lithography techniques, are inappropriate for mass production of microfluidic devices due to speed and cost concerns. There is a need to overcome these limitations in the future. Advances in bioinspired smart materials are leading to next-generation fabrication technologies for microfluidic devices such as 4-D printing, which adds a time dimension to the conventional 3-D printing and offer the capability to control size, shape and structure post-manufacture [162]. With the continuous development of novel fabrication technologies including 4-D printing, it is expected that the future microfluidic devices, will be less expensive, more integrated, more customizable and will incorporate a higher level of quality control [163]. Given the current state of the field, we can expect that future advances, particularly in POC systems, will have a transformative impact on the global health care system, which will improve the quality of life especially for elder people and people in developing countries [164]. Some exciting futuristic aspects for the field of microfluidics was given by Tian et al. [165] as follows:

»Microfluidics will provide autonomous distributed monitors for public health and surveillance for biothreats. The aging population will use health kits to provide preventive medicine. Medical checkups will be performed daily. Healthcare costs will be reduced due to the availability of microfluidics instruments. Chronic disease patients will possess home diagnostics systems and high risk patients (e.g. post surgical) will enjoy the comfort of being at home knowing that LOC devices will be monitoring risks of infection, blood clots, etc. Microfluidic devices will increase the efficacy and safety of medical treatments by assisting in the prescription and administration of drugs. Artificial cells, synthetic hybrid biomolecules and synthetic biomaterials will require the development of sophisticated microfluidic platforms down to the true nanometer scale dimensions.«

6 Acknowledgments

The authors would like to thank the Slovenian Research Agency/ARRS and the Ministry of Education, Science, Culture and Sport for their support of this work (Grant No P2-0244).

7 Conflict of Interest

The authors declare no conflict of interest.

8 Permission statement

The authors declare they have permission from the rightsholders to re-use the material.

9 References

1. R. P. Feynman, "There's plenty of room at the bottom", Journal of Microelectromechanical Systems,

Vol. 1, Issue 1 , pp. 60-66, Mar 1992, https://doi.org/10.1109/84.128057.
2. K. E. Petersen, "Silicon as a mechanical material", Proc.IEEE, Vol. 70, No. 5, pp. 420-457, 1982, https://doi.org/10.1109/PROC.1982.12331.
3. P. S. Dittrich and A. Manz, "Lab-on-a-chip: microfluidics in drug discovery," Nat Rev Drug Discov, vol. 5, no. 3, pp. 210–218, Mar. 2006, https://doi.org/10.1038/nrd1985.
4. N. T. Nguyen and S. T. Wereley, "Fundamentals and applications of microfluidics," Artech House. Boston, MA, USA: Inc, 2006
5. S. Lai, S. Wang, J. Luo, L. J. Lee, S.-T. Yang, and M. J. Madou, "Design of a Compact Disk-like Microfluidic Platform for Enzyme-Linked Immunosorbent Assay," Anal. Chem., vol. 76, no. 7, pp. 1832–1837, Apr. 2004, https://doi.org/10.1021/ac0348322.
6. A. M. Streets and Y. Huang, "Chip in a lab: Microfluidics for next generation life science research," Biomicrofluidics, vol. 7, no. 1, p. 011302, Jan. 2013, https://doi.org/10.1063/1.4789751.
7. K. F. Lei, "Chapter 1. Materials and Fabrication Techniques for Nano- and Microfluidic Devices," Royal Society of Chemistry, pp. 1–28.
8. M. P. Wolf, G. B. Salieb-Beugelaar, and P. Hunziker, "PDMS with designer functionalities—Properties, modifications strategies, and applications," Progress in Polymer Science, vol. 83, pp. 97–134, Aug. 2018, https://doi.org/10.1016/j.progpolymsci.2018.06.001.
9. M. Elwenspoek and H. V. Jansen, "Cambridge studies in semiconductor physics and microelectronic engineering: Silicon micromachining series number 7," Cambridge, England: Cambridge University Press, 2004.
10. D. Resnik, U. Aljančič, D. Vrtačnik, M. Cvar, and S. Amon, "Mikroobdelava silicija," Vakuumist, vol. 1, no. let 18, pp. 4–11, 1998.
11. D. Vrtačnik et al. "RIE of deep silicon microchannels for microfluidic applications," Proceedings, 44th International Conference MIDEM, September 2008.
12. M. Tilli, "Silicon wafers preparation and properties," in Handbook of Silicon Based MEMS Materials and Technologies, Elsevier, 2020, pp. 93–110, https://doi.org/10.1016/b978-0-12-817786-0.00004-9
13. K. J. Owen, B. VanDerElzen, R. L. Peterson, and K. Najafi, "High aspect ratio deep silicon etching," presented at the 2012 IEEE 25th International Conference on Micro Electro Mechanical Systems (MEMS), Jan. 2012, https://doi.org/10.1109/memsys.2012.6170138.
14. U.-B. T. Giang, D. Lee, M. R. King, and L. A. DeLouise, "Microfabrication of cavities in polydimethylsiloxane using DRIE silicon molds," Lab Chip, vol. 7, no. 12, p. 1660, 2007, https://doi.org/10.1039/b714742b.
15. Kuo-Shen Chen, A. A. Ayon, Xin Zhang, and S. M. Spearing, "Effect of process parameters on the surface morphology and mechanical performance of silicon structures after deep reactive ion etching (DRIE)," J. Microelectromech. Syst., vol. 11, no. 3, pp. 264–275, Jun. 2002, https://doi.org/10.1109/jmems.2002.1007405.
16. D. Vrtačnik et al. "Optimization of DRIE silicon microstructures with Bosch process," Proceedings, 47th International Conference MIDEM, september 2011.
17. X. Li, T. Abe, Y. Liu, and M. Esashi, "Fabrication of high-density electrical feed-throughs by deep-reactive-ion etching of Pyrex glass," J. Microelectromech. Syst., vol. 11, no. 6, pp. 625–630, Dec. 2002, https://doi.org/10.1109/jmems.2002.805211.
18. M. Stjernström and J. Roeraade, "Method for fabrication of microfluidic systems in glass," J. Micromech. Microeng., vol. 8, no. 1, pp. 33–38, Mar. 1998, https://doi.org/10.1088/0960-1317/8/1/006.
19. C. Iliescu, "Microfluidics in glass: technologies and applications," Informacije MIDEM, 2006, 36(4), 204, http://www.dlib.si/details/URN:NBN:SI:doc-U408KBPW.
20. Y. Xia and G. M. Whitesides, "SOFT LITHOGRAPHY," Annu. Rev. Mater. Sci., vol. 28, no. 1, pp. 153–184, Aug. 1998, https://doi.org/10.1146/annurev.matsci.28.1.153.
21. V. N. Goral, Y.-C. Hsieh, O. N. Petzold, R. A. Faris, and P. K. Yuen, "Hot embossing of plastic microfluidic devices using poly(dimethylsiloxane) molds," J. Micromech. Microeng., vol. 21, no. 1, p. 017002, Dec. 2010, https://doi.org/10.1088/0960-1317/21/1/017002.
22. M. Matteucci, T. L. Christiansen, S. Tanzi, P. F. Østergaard, S. T. Larsen, and R. Taboryski, "Fabrication and characterization of injection molded multi level nano and microfluidic systems," Microelectronic Engineering, vol. 111, pp. 294–298, Nov. 2013, https://doi.org/10.1016/j.mee.2013.01.060.
23. P. Sethu, "Cast epoxy-based microfluidic systems and their application in biotechnology," Sensors and Actuators B: Chemical, vol. 98, no. 2–3, pp. 337–346, Mar. 2004, https://doi.org/10.1016/j.snb.2003.09.036.
24. P. P. Shiu, G. K. Knopf, M. Ostojic, and S. Nikumb, "Rapid fabrication of tooling for microfluidic devices via laser micromachining and hot embossing," J. Micromech. Microeng., vol. 18, no. 2, p. 025012, Jan. 2008, https://doi.org/10.1088/0960-1317/18/2/025012.

25. V. Shukla, S. N. Akhtar, S. K. Subbu, and J. Ramkumar, "Fabrication of Complex Micro Channels by Micro Electric Discharge Milling (μ-ED Milling)," presented at the ASME 2013 International Mechanical Engineering Congress and Exposition, Nov. 2013, https://doi.org/10.1115/imece2013-64031.
26. K. Thompson, Y. B. Gianchandani, J. Booske, and R. F. Cooper, "Direct silicon-silicon bonding by electromagnetic induction heating," J. Microelectromech. Syst., vol. 11, no. 4, pp. 285–292, Aug. 2002, https://doi.org/10.1109/jmems.2002.800929.
27. H. Takagi, R. Maeda, T. R. Chung, and T. Suga, "Low-temperature direct bonding of silicon and silicon dioxide by the surface activation method," Sensors and Actuators A: Physical, vol. 70, no. 1–2, pp. 164–170, Oct. 1998, https://doi.org/10.1016/s0924-4247(98)00128-9.
28. H. J. Quenzer and W. Benecke, "Low-temperature silicon wafer bonding," Sensors and Actuators A: Physical, vol. 32, no. 1–3, pp. 340–344, Apr. 1992, https://doi.org/10.1016/0924-4247(92)80009-r.
29. D. Resnik, D. Vrtačnik, U. Aljančič, and S. Amon, "Study of low-temperature direct bonding of (111) and (100) silicon wafers under various ambient and surface conditions," Sensors and Actuators A: Physical, vol. 80, no. 1, pp. 68–76, Mar. 2000, https://doi.org/10.1016/s0924-4247(99)00299-x.
30. D. Resnik, D. Vrtačnik, U. Aljančič, and S. Amon, "Study of low-temperature direct bonding of (111) and (100) silicon wafers under various ambient and surface conditions," Sensors and Actuators A: Physical, vol. 80, no. 1, pp. 68–76, Mar. 2000, https://doi.org/10.1016/s0924-4247(99)00299-x.
31. Z.-X. Xiao, G.-Y. Wu, Z.-H. Li, G.-B. Zhang, Y.-L. Hao, and Y.-Y. Wang, "Silicon–glass wafer bonding with silicon hydrophilic fusion bonding technology," Sensors and Actuators A: Physical, vol. 72, no. 1, pp. 46–48, Jan. 1999, https://doi.org/10.1016/s0924-4247(98)00197-6.
32. D. Resnik, U. Aljancic, D. Vrtacnik, M. Mozek, B. Pecar, and S. Amon, "Microfluidic platforms realized by micromachining and anodic bonding of Si and glass substrates," presented at the 2012 International Caribbean Conference on Devices, Circuits and Systems (ICCDCS), Mar. 2012, https://doi.org/10.1109/iccdcs.2012.6188939.
33. D. Resnik, M. Možek, T. Dolžan, S. Amon and D. Vrtačnik, "Spajanje podlag silicij-steklo z anodnim bondiranjem, "Vakuumist, 2012, 3(32), pp. 4-11.
34. C.-W. Tsao, "Polymer Microfluidics: Simple, Low-Cost Fabrication Process Bridging Academic Lab Research to Commercialized Production," Micromachines, vol. 7, no. 12, p. 225, Dec. 2016, https://doi.org/10.3390/mi7120225.
35. Y. Suzuki, M. Yamada, and M. Seki, "Sol–gel based fabrication of hybrid microfluidic devices composed of PDMS and thermoplastic substrates," Sensors and Actuators B: Chemical, vol. 148, no. 1, pp. 323–329, Jun. 2010, https://doi.org/10.1016/j.snb.2010.04.018.
36. C.-W. Tsao and D. L. DeVoe, "Bonding of thermoplastic polymer microfluidics," Microfluid Nanofluid, vol. 6, no. 1, pp. 1–16, Nov. 2008, https://doi.org/10.1007/s10404-008-0361-x.
37. K. S. Lee and R. J. Ram, "Plastic–PDMS bonding for high pressure hydrolytically stable active microfluidics," Lab Chip, vol. 9, no. 11, p. 1618, 2009, https://doi.org/10.1039/b820924c.
38. B. Pečar, M. Možek, and D. Vrtačnik, "Ther-moplastic-PDMS polymer covalent bonding for microfluidic applications,"Informacije MIDEM, 2017, vol. 47, no. 3, pp. 147–154.
39. J. P. Conde et al., "Lab-on-chip systems for integrated bioanalyses," Essays in Biochemistry, vol. 60, no. 1, pp. 121–131, Jun. 2016, https://doi.org/10.1042/ebc20150013.
40. W. C. Krutzsch and P. Cooper, "Introduction: classification and selection of pumps," Pump Handbook, 2001.
41. H. T. G. van Lintel, F. C. M. van De Pol, and S. Bouwstra, "A piezoelectric micropump based on micromachining of silicon," Sensors and Actuators, vol. 15, no. 2, pp. 153–167, Oct. 1988, https://doi.org/10.1016/0250-6874(88)87005-7.
42. M. C. Carrozza, N. Croce, B. Magnani, and P. Dario, "A piezoelectric-driven stereolithography-fabricated micropump," J. Micromech. Microeng., vol. 5, no. 2, pp. 177–179, Jun. 1995, https://doi.org/10.1088/0960-1317/5/2/032.
43. M. Koch, N. Harris, A. G. R. Evans, N. M. White, and A. Brunnschweiler, "A novel micromachined pump based on thick-film piezoelectric actuation," Sensors and Actuators A: Physical, vol. 70, no. 1–2, pp. 98–103, Oct. 1998, https://doi.org/10.1016/s0924-4247(98)00120-4.
44. B. Pečar, M. Možek, and D. Vrtačnik, "Piezoelektrična mikročrpalka z ventiloma, ki posnemata delovanje bioloških venskih zaklopk," patent SI 25227 (A), 2017-12-29. Ljubljana: Urad RS za intelektualno lastnino, 2017
45. R. Ardito, E. Bertarelli, A. Corigliano, and G. Gafforelli, "On the application of piezolaminated composites to diaphragm micropumps," Composite Structures, vol. 99, pp. 231–240, May 2013, https://doi.org/10.1016/j.compstruct.2012.11.041
46. B. Pečar et al., "Microcylinder pump employing 0. 57 Pb (Sc1/2Nb1/2) O3–0. 43 PbTiO3 piezoelectric actuator,"Journal of Optoelectronics and Advanced Materials, 2017, vol. 19, pp. 617–622.

47. B Pečar et al., "Silicon piezoelectric vaveless micropumps", MIT & SLIM, 2011 : proceedings of the 11th International Conference on Management of Innovative Technologies & 2nd International Conference
48. Z. Jin, Z. Gao, M. Chen, and J. Qian, "Parametric study on Tesla valve with reverse flow for hydrogen decompression," International Journal of Hydrogen Energy, vol. 43, no. 18, pp. 8888–8896, May 2018, https://doi.org/10.1016/j.ijhydene.2018.03.014.
49. P.-H. Huang et al., "A reliable and programmable acoustofluidic pump powered by oscillating sharp-edge structures," Lab Chip, vol. 14, no. 22, pp. 4319–4323, 2014, https://doi.org/10.1039/c4lc00806e.
50. M. Tanyeri and S. Tay, "Viable cell culture in PDMS-based microfluidic devices," in Methods in Cell Biology, Elsevier, 2018, pp. 3–33, https://doi.org/10.1016/bs.mcb.2018.09.007.
51. C. Wang, J. Kim, and J. Park, "Micro check valve integrated magnetically actuated micropump for implantable drug delivery," presented at the 2017 19th International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS), Jun. 2017, https://doi.org/10.1109/transducers.2017.7994396
52. N. Gadad et al., "Fabrication and development of magnetically actuated PDMS micropump for drug delivery," IOP Conf. Ser.: Mater. Sci. Eng., vol. 376, p. 012128, Jun. 2018, https://doi.org/10.1088/1757-899x/376/1/012128
53. P. Kawun, S. Leahy, and Y. Lai, "A thin PDMS nozzle/diffuser micropump for biomedical applications," Sensors and Actuators A: Physical, vol. 249, pp. 149–154, Oct. 2016, https://doi.org/10.1016/j.sna.2016.08.032.
54. H.-L. Chien and Y.-C. Lee, "A ball valve micro-pump based on axially symmetrical nozzle fabricated by excimer laser micromachining technology," Int. J. Precis. Eng. Manuf., vol. 18, no. 10, pp. 1315–1320, Oct. 2017, https://doi.org/10.1007/s12541-017-0156-7.
55. Y. Ye, J. Chen, Y. J. Ren, and Z. H. Feng, "Valve improvement for high flow rate piezoelectric pump with PDMS film valves," Sensors and Actuators A: Physical, vol. 283, pp. 245–253, Nov. 2018, https://doi.org/10.1016/j.sna.2018.09.064.
56. A. Mashayek, C. P. Caulfield, and W. R. Peltier, "Role of overturns in optimal mixing in stratified mixing layers," J. Fluid Mech., vol. 826, pp. 522–552, Aug. 2017, https://doi.org/10.1017/jfm.2017.374.
57. M. Rusli, P. S. Chee, R. Arsat, K. X. Lau, and P. L. Leow, "Electromagnetic actuation dual-chamber bidirectional flow micropump," Sensors and Actuators A: Physical, vol. 282, pp. 17–27, Oct. 2018, https://doi.org/10.1016/j.sna.2018.08.047.
58. A. T. Al-Halhouli, S. Demming, A. Dietzel, and S. Büttgenbach, "Design, Fabrication, and Characterization of a Continuous Flow Micropump System," Journal of Thermal Science and Engineering Applications, vol. 8, no. 2, Dec. 2015, https://doi.org/10.1115/1.4031922.
59. R. R. Gidde and P. M. Pawar, "On effect of viscoelastic characteristics of polymers on performance of micropump," Advances in Mechanical Engineering, vol. 9, no. 2, p. 168781401769121, Feb. 2017, https://doi.org/10.1177/1687814017691211.
60. J. G. Smits, "Piezoelectric micropump with three valves working peristaltically," Sensors and Actuators A: Physical, vol. 21, no. 1–3, pp. 203–206, Feb. 1990, https://doi.org/10.1016/0924-4247(90)85039-7.
61. J. M. Berg, R. Anderson, M. Anaya, B. Lahlouh, M. Holtz, and T. Dallas, "A two-stage discrete peristaltic micropump," Sensors and Actuators A: Physical, vol. 104, no. 1, pp. 6–10, Mar. 2003, https://doi.org/10.1016/s0924-4247(02)00434-x.
62. B. Pečar, D. Križaj, D. Vrtačnik, D. Resnik, T. Dolžan, and M. Možek, "Piezoelectric peristaltic micropump with a single actuator," J. Micromech. Microeng., vol. 24, no. 10, p. 105010, Sep. 2014, https://doi.org/10.1088/0960-1317/24/10/105010
63. M. J. Davies, I. D. Johnston, C. K. L. Tan, and M. C. Tracey, "Whole blood pumping with a microthrottle pump," Biomicrofluidics, vol. 4, no. 4, p. 044112, Dec. 2010, https://doi.org/10.1063/1.3528327.
64. B. Pečar et al., "A Strip-Type Microthrottle Pump: Modeling, Design and Fabrication," Sensors, vol. 13, no. 3, pp. 3092–3108, Mar. 2013, https://doi.org/10.3390/s130303092.
65. B. Pečar et al., "Piezoelektrična mikrocilindrska črpalka," SI 24234 A, 2014-05-30. Ljubljana: Urad RS za intelektualno lastnino, 2014. 13 str., P 201300185 2013-07-05
66. P. Gravesen, J. Branebjerg, and O. S. Jensen, "Microfluidics-a review," Journal of microme-chanics and microengineering, 1993, vol. 3, no. 4, p. 168, https://doi.org/10.3390/s130303092.
67. J. Wang, M. Sullivan and S. Z. Hua, "Electro-lytic-bubble-based flow sensor for microfluidic systems," J Microelectromech Syst, 2007, vol. 16, no. 5, pp. 1087–1094, https://doi.org/10.1109/jmems.2007.906078
68. A. S. Nezhad, M. Ghanbari, C. G. Agudelo, M. Packirisamy, R. B. Bhat, and A. Geitmann, "PDMS Microcantilever-Based Flow Sensor Integration for Lab-on-a-Chip," IEEE Sensors J., vol. 13, no. 2, pp. 601–609, Feb. 2013, https://doi.org/10.1109/jsen.2012.2223667.

69. A. Amnache, M. Omri, and L. G. Fréchette, "A silicon rectangular micro-orifice for gas flow measurement at moderate Reynolds numbers: design, fabrication and flow analyses," Microfluid Nanofluid, vol. 22, no. 6, May 2018, https://doi.org/10.1007/s10404-018-2077-x.
70. A. Richter, K. A. Hofmann, A. Plettner, and H. Sandmaier, "The electrohydrodynamic micro flow meter," presented at the TRANSDUCERS '91: 1991 International Conference on Solid-State Sensors and Actuators. Digest of Technical Papers, https://doi.org/10.1109/sensor.1991.149042.
71. D. Accoto et al., "A micro flow-meter for closed-loop management of biological samples," presented at the 2005 IEEE Engineering in Medicine and Biology 27th Annual Conference, 2005, https://doi.org/10.1109/iembs.2005.1615614.
72. C. Nie, A. J. H. Frijns, R. Mandamparambil, M. A. G. Zevenbergen, and J. M. J. den Toonder, "An evaporation based digital microflow meter," J. Micromech. Microeng., vol. 25, no. 11, p. 115008, Sep. 2015, https://doi.org/10.1088/0960-1317/25/11/115008
73. B. W. van Oudheusden, "Silicon thermal flow sensors," Sensors and Actuators A: Physical, vol. 30, no. 1–2, pp. 5–26, Jan. 1992, https://doi.org/10.1016/0924-4247(92)80192-6.
74. A. Petropoulos and G. Kaltsas, "Study and Evaluation of a PCB-MEMS Liquid Microflow Sensor," Sensors, vol. 10, no. 10, pp. 8981–9001, Oct. 2010, https://doi.org/10.3390/s101008981.
75. Y. Valizadeh Yaghmourali, N. Ahmadi, and E. Abbaspour-sani, "A thermal-calorimetric gas flow meter with improved isolating feature," Microsyst Technol, vol. 23, no. 6, pp. 1927–1936, Mar. 2016, https://doi.org/10.1007/s00542-016-2915-2.
76. W. Ke, M. Liu, T. Li, and Y. Wang, "MEMS thermal gas flow sensor with self-test function," J. Micromech. Microeng., vol. 29, no. 12, p. 125009, Oct. 2019, https://doi.org/10.1088/1361-6439/ab4aef.
77. W. Kang, H.-M. Choi, and Y.-M. Choi, "Development of MEMS-based thermal mass flow sensors for high sensitivity and wide flow rate range," J Mech Sci Technol, vol. 32, no. 9, pp. 4237–4243, Sep. 2018, https://doi.org/10.1007/s12206-018-0822-4.
78. G. Kaltsas et al., "A novel microfabrication technology on organic substrates – application to a thermal flow sensor," J. Phys.: Conf. Ser., vol. 92, p. 012046, Dec. 2007, https://doi.org/10.1088/1742-6596/92/1/012046.
79. Y. Li, K. Baek, M. Gulari, D. Lin, and K. D. Wise, "A Vacuum-Isolated Thermal Microflowmeter for In-Vivo Drug Delivery," presented at the IEEE Sensors, 2005., https://doi.org/10.1109/icsens.2005.1597787.
80. P. Liu, R. Zhu, and R. Que, "A Flexible Flow Sensor System and Its Characteristics for Fluid Mechanics Measurements," Sensors, vol. 9, no. 12, pp. 9533–9543, Nov. 2009, https://doi.org/10.3390/s91209533.
81.]R. Ahrens and K. Schlote-Holubek, "A micro flow sensor from a polymer for gases and liquids," J. Micromech. Microeng., vol. 19, no. 7, p. 074006, Jun. 2009, https://doi.org/10.1088/0960-1317/19/7/074006.
82. C. Li, P.-M. Wu, J. Han, and C. H. Ahn, "A flexible polymer tube lab-chip integrated with microsensors for smart microcatheter," Biomed Microdevices, vol. 10, no. 5, pp. 671–679, May 2008, https://doi.org/10.1007/s10544-008-9178-3.
83. J. T. W. Kuo, L.-Y. Chang, P.-Y. Li, T. Hoang, and E. Meng, "A microfluidic platform with integrated flow sensing for focal chemical stimulation of cells and tissue," Sensors and Actuators B: Chemical, vol. 152, no. 2, pp. 267–276, Mar. 2011, https://doi.org/10.1016/j.snb.2010.12.019.
84. B. Pečar et al., "Microflowmeter for microfluidics applications, " Conference proceedings, 52nd International Conference MIDEM, September 28 - 30 2016, pp. 122-126.
85. V. Miralles, A. Huerre, F. Malloggi, and M.-C. Jullien, "A Review of Heating and Temperature Control in Microfluidic Systems: Techniques and Applications," Diagnostics, vol. 3, no. 1, pp. 33–67, Jan. 2013, https://doi.org/10.3390/diagnostics3010033.
86. T. Matsui, J. Franzke, A. Manz, and D. Janasek, "Temperature gradient focusing in a PDMS/glass hybrid microfluidic chip," Electrophoresis, vol. 28, no. 24, pp. 4606–4611, Dec. 2007, https://doi.org/10.1002/elps.200700272.
87. A. Kempitiya, D. A. Borca-Tasciuc, H. S. Mohamed, and M. M. Hella, "Localized microwave heating in microwells for parallel DNA amplification applications," Appl. Phys. Lett., vol. 94, no. 6, p. 064106, Feb. 2009, https://doi.org/10.1063/1.3078273.
88. H. Mao, T. Yang, and P. S. Cremer, "A Microfluidic Device with a Linear Temperature Gradient for Parallel and Combinatorial Measurements," J. Am. Chem. Soc., vol. 124, no. 16, pp. 4432–4435, Apr. 2002, https://doi.org/10.1021/ja017625x.
89. K. Zhang, A. Jian, X. Zhang, Y. Wang, Z. Li, and H. Tam, "Laser-induced thermal bubbles for microfluidic applications," Lab Chip, vol. 11, no. 7, p. 1389, 2011, https://doi.org/10.1039/c0lc00520g.
90. R. M. Guijt, A. Dodge, G. W. K. van Dedem, N. F. de Rooij, and E. Verpoorte, "Chemical and physical processes for integrated temperature control in

microfluidic devices," Lab Chip, vol. 3, no. 1, p. 1, 2003, https://doi.org/10.1039/b210629a.
91. E. Mavraki, D. Moschou, G. Kokkoris, N. Vourdas, S. Chatzandroulis, and A. Tserepi, "A continuous flow µPCR device with integrated microheaters on a flexible polyimide substrate," Procedia Engineering, vol. 25, pp. 1245–1248, 2011, https://doi.org/10.1016/j.proeng.2011.12.307.
92. B. Selva, J. Marchalot, and M.-C. Jullien, "An optimized resistor pattern for temperature gradient control in microfluidics," J. Micromech. Microeng., vol. 19, no. 6, p. 065002, May 2009, https://doi.org/10.1088/0960-1317/19/6/065002.
93. T.-M. Hsieh, C.-H. Luo, F.-C. Huang, J.-H. Wang, L.-J. Chien, and G.-B. Lee, "Enhancement of thermal uniformity for a microthermal cycler and its application for polymerase chain reaction☆," Sensors and Actuators B: Chemical, vol. 130, no. 2, pp. 848–856, Mar. 2008, https://doi.org/10.1016/j.snb.2007.10.063.
94. D. Resnik, D. Vrtačnik, M. Možek, B. Pečar, and S. Amon, "Experimental study of heat-treated thin film Ti/Pt heater and temperature sensor properties on a Si microfluidic platform," J. Micromech. Microeng., vol. 21, no. 2, p. 025025, Jan. 2011, https://doi.org/10.1088/0960-1317/21/2/025025.
95. E. Larrañeta, R. E. M. Lutton, A. D. Woolfson, and R. F. Donnelly, "Microneedle arrays as transdermal and intradermal drug delivery systems: Materials science, manufacture and commercial development," Materials Science and Engineering: R: Reports, vol. 104, pp. 1–32, Jun. 2016, https://doi.org/10.1016/j.mser.2016.03.001.
96. Y.-C. Kim, J.-H. Park, and M. R. Prausnitz, "Microneedles for drug and vaccine delivery," Advanced Drug Delivery Reviews, vol. 64, no. 14, pp. 1547–1568, Nov. 2012, https://doi.org/10.1016/j.addr.2012.04.005.
97. W. H. Smart and K. Subramanian, "The Use of Silicon Microfabrication Technology in Painless Blood Glucose Monitoring," Diabetes Technol. Ther., vol. 2, no. 4, pp. 549–559, Dec. 2000, https://doi.org/10.1089/15209150050501961.
98. H. J. G. E. Gardeniers et al., "Silicon micromachined hollow microneedles for transdermal liquid transport," J. Microelectromech. Syst., vol. 12, no. 6, pp. 855–862, Dec. 2003, https://doi.org/10.1109/jmems.2003.820293.
99. B. Chen, J. Wei, F. E. H. Tay, Y. T. Wong, and C. Iliescu, "Silicon microneedle array with biodegradable tips for transdermal drug delivery," Microsyst Technol, vol. 14, no. 7, pp. 1015–1019, Jan. 2008, https://doi.org/10.1007/s00542-007-0530-y.
100. Liwei Lin and A. P. Pisano, "Silicon-processed microneedles," J. Microelectromech. Syst., vol. 8, no. 1, pp. 78–84, Mar. 1999, https://doi.org/10.1109/84.749406.
101. W. Martanto, J. S. Moore, T. Couse, and M. R. Prausnitz, "Mechanism of fluid infusion during microneedle insertion and retraction," Journal of Controlled Release, vol. 112, no. 3, pp. 357–361, May 2006, https://doi.org/10.1016/j.jconrel.2006.02.017.
102. S. Doddaballapur, "Microneedling with dermaroller," J Cutan Aesthet Surg, vol. 2, no. 2, p. 110, 2009, https://doi.org/10.4103/0974-2077.58529.
103. L. Wei-Ze et al., "Super-short solid silicon microneedles for transdermal drug delivery applications," International Journal of Pharmaceutics, vol. 389, no. 1–2, pp. 122–129, Apr. 2010, https://doi.org/10.1016/j.ijpharm.2010.01.024.
104. M. A. L. Teo, C. Shearwood, K. C. Ng, J. Lu, and S. Moochhala, "In Vitro and In Vivo Characterization of MEMS Microneedles," Biomed Microdevices, vol. 7, no. 1, pp. 47–52, Mar. 2005, https://doi.org/10.1007/s10544-005-6171-y.
105. S. P. Davis, W. Martanto, M. G. Allen, and M. R. Prausnitz, "Hollow Metal Microneedles for Insulin Delivery to Diabetic Rats," IEEE Trans. Biomed. Eng., vol. 52, no. 5, pp. 909–915, May 2005, https://doi.org/10.1109/tbme.2005.845240.
106. J.-H. Park, M. G. Allen, and M. R. Prausnitz, "Polymer Microneedles for Controlled-Release Drug Delivery," Pharm Res, vol. 23, no. 5, pp. 1008–1019, May 2006, https://doi.org/10.1007/s11095-006-0028-9.
107. S. H. Bariya, M. C. Gohel, T. A. Mehta, and O. P. Sharma, "Microneedles: an emerging transdermal drug delivery system," Journal of Pharmacy and Pharmacology, vol. 64, no. 1, pp. 11–29, Nov. 2011, https://doi.org/10.1111/j.2042-7158.2011.01369.x
108. P. Karande, A. Jain, and S. Mitragotri, "Relationships between skin's electrical impedance and permeability in the presence of chemical enhancers," Journal of Controlled Release, vol. 110, no. 2, pp. 307–313, Jan. 2006, https://doi.org/10.1016/j.jconrel.2005.10.012.
109. M. R. Prausnitz and R. Langer, "Transdermal drug delivery," Nat Biotechnol, vol. 26, no. 11, pp. 1261–1268, Nov. 2008, https://doi.org/10.1038/nbt.1504.
110. D. Resnik et al., "Characterization of skin penetration efficacy by Au-coated Si microneedle array electrode," Sensors and Actuators A: Physical, vol. 232, pp. 299–309, Aug. 2015, https://doi.org/10.1016/j.sna.2015.05.020.
111. Deng et al., "Transdermal Delivery of siRNA through Microneedle Array," Sci Rep, vol. 6, no. 1, Feb. 2016, https://doi.org/10.1038/srep21422.

112. E. Kim et al., "Microneedle array delivered recombinant coronavirus vaccines: Immunogenicity and rapid translational development," EBioMedicine, vol. 55, p. 102743, May 2020, https://doi.org/10.1016/j.ebiom.2020.102743.
113. D. Resnik et al., "In Vivo Experimental Study of Noninvasive Insulin Microinjection through Hollow Si Microneedle Array," Micromachines, vol. 9, no. 1, p. 40, Jan. 2018, https://doi.org/10.3390/mi9010040.
114. F. S. Iliescu, J. C. M. Teo, D. Vrtacnik, H. Taylor, and C. Iliescu, "Cell therapy using an array of ultrathin hollow microneedles," Microsyst Technol, vol. 24, no. 7, pp. 2905–2912, Nov. 2017, https://doi.org/10.1007/s00542-017-3631-2.
115. Z. Li, A. Khajepour, and J. Song, "A comprehensive review of the key technologies for pure electric vehicles," Energy, vol. 182, pp. 824–839, Sep. 2019, https://doi.org/10.1016/j.energy.2019.06.077.
116. S. Tanaka, K.-S. Chang, K.-B. Min, D. Satoh, K. Yoshida, and M. Esashi, "MEMS-based components of a miniature fuel cell/fuel reformer system," Chemical Engineering Journal, vol. 101, no. 1–3, pp. 143–149, Aug. 2004, https://doi.org/10.1016/j.cej.2004.01.017.
117. J. D. Holladay, E. O. Jones, R. A. Dagle, G. G. Xia, C. Cao, and Y. Wang, "High efficiency and low carbon monoxide micro-scale methanol processors," Journal of Power Sources, vol. 131, no. 1–2, pp. 69–72, May 2004, https://doi.org/10.1016/j.jpowsour.2004.01.003.
118. Y. Kawamura, N. Ogura, T. Yamamoto, and A. Igarashi, "A miniaturized methanol reformer with Si-based microreactor for a small PEMFC," Chemical Engineering Science, vol. 61, no. 4, pp. 1092–1101, Feb. 2006, https://doi.org/10.1016/j.ces.2005.08.014.
119. C.-Y. Hsueh, H.-S. Chu, W.-M. Yan, and C.-H. Chen, "Transport phenomena and performance of a plate methanol steam micro-reformer with serpentine flow field design," Applied Energy, vol. 87, no. 10, pp. 3137–3147, Oct. 2010, https://doi.org/10.1016/j.apenergy.2010.02.027.
120. H. Jeong, K. I. Kim, T. H. Kim, C. H. Ko, H. C. Park, and I. K. Song, "Hydrogen production by steam reforming of methanol in a micro-channel reactor coated with Cu/ZnO/ZrO2/Al2O3 catalyst," Journal of Power Sources, vol. 159, no. 2, pp. 1296–1299, Sep. 2006, https://doi.org/10.1016/j.jpowsour.2005.11.095.
121. T. Kim, J. S. Hwang, and S. Kwon, "A MEMS methanol reformer heated by decomposition of hydrogen peroxide," Lab Chip, vol. 7, no. 7, p. 835, 2007, https://doi.org/10.1039/b700040e.
122. D. Mei, Y. Feng, M. Qian, and Z. Chen, "An innovative micro-channel catalyst support with a micro-porous surface for hydrogen production via methanol steam reforming," International Journal of Hydrogen Energy, vol. 41, no. 4, pp. 2268–2277, Jan. 2016, https://doi.org/10.1016/j.ijhydene.2015.12.044.
123. Y.-X. Huang, J.-Y. Jang, and C.-H. Cheng, "Fractal channel design in a micro methanol steam reformer," International Journal of Hydrogen Energy, vol. 39, no. 5, pp. 1998–2007, Feb. 2014, https://doi.org/10.1016/j.ijhydene.2013.11.088.
124. M. M. Sarafraz, M. R. Safaei, M. Goodarzi, and M. Arjomandi, "Reforming of methanol with steam in a micro-reactor with Cu–SiO2 porous catalyst," International Journal of Hydrogen Energy, vol. 44, no. 36, pp. 19628–19639, Jul. 2019, https://doi.org/10.1016/j.ijhydene.2019.05.215.
125. H.-S. Wang, K.-Y. Huang, Y.-J. Huang, Y.-C. Su, and F.-G. Tseng, "A low-temperature partial-oxidation-methanol micro reformer with high fuel conversion rate and hydrogen production yield," Applied Energy, vol. 138, pp. 21–30, Jan. 2015, https://doi.org/10.1016/j.apenergy.2014.10.033.
126. D. Resnik, S. Hočevar, J. Batista, D. Vrtačnik, M. Možek, and S. Amon, "Si based methanol catalytic micro combustor for integrated steam reformer applications," Sensors and Actuators A: Physical, vol. 180, pp. 127–136, Jun. 2012, https://doi.org/10.1016/j.sna.2012.04.029.
127. D. Peruško et al., "Temperature control of methanol fuel microreactor for hydrogen production,"Proceedings of the 34th International Convention MIPRO (pp. 141-144), 2011, pp. 141–144.
128. B. Pečar et al., "Microflow-generator for fuel-cell methanol hydrogen microreactor," 33rd International Convention MIPRO , IEEE, 2010, pp. 110–115.
129. C. Tsai and C.-Y. Sue, "Review of MEMS-based drug delivery and dosing systems," Sensors and Actuators A: Physical, vol. 134, no. 2, pp. 555–564, Mar. 2007, https://doi.org/10.1016/j.sna.2006.06.014.
130. S. Böhm, B. Timmer, W. Olthuis, and P. Bergveld, "A closed-loop controlled electrochemically actuated micro-dosing system," J. Micromech. Microeng., vol. 10, no. 4, pp. 498–504, Oct. 2000, https://doi.org/10.1088/0960-1317/10/4/303.
131. D. Reynaerts, J. Peirs, and H. Van Brussel, "An implantable drug-delivery system based on shape memory alloy micro-actuation," Sensors and Actuators A: Physical, vol. 61, no. 1–3, pp. 455–462, Jun. 1997, https://doi.org/10.1016/s0924-4247(97)80305-6.
132. J. Koerner, M. Helmlinger and H. Schuerle (2009). U.S. Patent No. 7,584,903. Washington, DC: U.S. Patent and Trademark Office.

133. Y.-C. Su and L. Lin, "A Water-Powered Micro Drug Delivery System," J. Microelectromech. Syst., vol. 13, no. 1, pp. 75–82, Feb. 2004, https://doi.org/10.1109/jmems.2003.823215.
134. A. Than et al., "Self-implantable double-layered micro-drug-reservoirs for efficient and controlled ocular drug delivery," Nat Commun, vol. 9, no. 1, Nov. 2018, https://doi.org/10.1038/s41467-018-06981-w.
135. A. Kabata, H. Suzuki, Y. Kishigami, and M. Haga, "Micro System for Injection of Insulin and Monitoring of Glucose Concentration," presented at the IEEE Sensors, 2005, https://doi.org/10.1109/icsens.2005.1597663.
136. D. Vrtačnik et al. "Micro-sized PDMS membranes in sealed microfluidic reservoirs, " in Conference proceedings 2016. 52nd International Conference MIDEM, September 28 - 30 2016, Ankaran, Slovenia.
137. D. Vrtačnik et al. "Nosljiv integrirani mikrodozirni sistem s poljem silicijevih mikroigel za transdermalni vnos zdravil, " patent SI24564 (A), 2015-06-30. Ljubljana: Urad RS za intelektualno lastnino, 2015.
138. K. F. Lei, "Chapter 1. Materials and Fabrication Techniques for Nano- and Microfluidic Devices," in Microfluidics in Detection Science, Royal Society of Chemistry, pp. 1–28.
139. M. Barbooti, Ed., "Environmental Applications of Instrumental Chemical Analysis." Apple Academic Press, Apr. 15, 2015, https://doi.org/10.1201/b18376.
140. "Microfluidics innovation center,"Elveflow.com, 31-Jul-2019. [Online]. Available: https://www.elveflow.com. [Accessed: 12-Mar-2021].
141. J. Sengupta and C. M. Hussain, "Graphene and its derivatives for Analytical Lab on Chip platforms," TrAC Trends in Analytical Chemistry, vol. 114, pp. 326–337, May 2019, https://doi.org/10.1016/j.trac.2019.03.015.
142. I. Moser et al., "Miniaturized Thin Film Glutamate and Glutamine Biosensors," in Biosensors '94, Elsevier, 1994, p. 170, https://doi.org/10.1016/b978-1-85617-242-4.50137-3
143. J.-Y. Yoon and B. Kim, "Lab-on-a-Chip Pathogen Sensors for Food Safety," Sensors, vol. 12, no. 8, pp. 10713–10741, Aug. 2012, https://doi.org/10.3390/s120810713.
144. B. H. Weigl, R. L. Bardell, and C. R. Cabrera, "Lab-on-a-chip for drug development," Advanced Drug Delivery Reviews, vol. 55, no. 3, pp. 349–377, Feb. 2003, https://doi.org/10.1016/s0169-409x(02)00223-5.
145. P. Ertl, D. Sticker, V. Charwat, C. Kasper, and G. Lepperdinger, "Lab-on-a-chip technologies for stem cell analysis," Trends in Biotechnology, vol. 32, no. 5, pp. 245–253, May 2014, https://doi.org/10.1016/j.tibtech.2014.03.004.
146. R. Pol, F. Céspedes, D. Gabriel, and M. Baeza, "Microfluidic lab-on-a-chip platforms for environmental monitoring," TrAC Trends in Analytical Chemistry, vol. 95, pp. 62–68, Oct. 2017, https://doi.org/10.1016/j.trac.2017.08.001.
147. J. Wu, M. Dong, S. Santos, C. Rigatto, Y. Liu, and F. Lin, "Lab-on-a-Chip Platforms for Detection of Cardiovascular Disease and Cancer Biomarkers," Sensors, vol. 17, no. 12, p. 2934, Dec. 2017, https://doi.org/10.3390/s17122934.
148. Y. Ai, F. Zhang, C. Wang, R. Xie, and Q. Liang, "Recent progress in lab-on-a-chip for pharmaceutical analysis and pharmacological/toxicological test," TrAC Trends in Analytical Chemistry, vol. 117, pp. 215–230, Aug. 2019, https://doi.org/10.1016/j.trac.2019.06.026.
149. W. Jung, J. Han, J.-W. Choi, and C. H. Ahn, "Point-of-care testing (POCT) diagnostic systems using microfluidic lab-on-a-chip technologies," Microelectronic Engineering, vol. 132, pp. 46–57, Jan. 2015, https://doi.org/10.1016/j.mee.2014.09.024.
150. S. K. Sia and L. J. Kricka, "Microfluidics and point-of-care testing," Lab Chip, vol. 8, no. 12, p. 1982, 2008, https://doi.org/10.1039/b817915h.
151. T. Nguyen, S. Zoëga Andreasen, A. Wolff, and D. Duong Bang, "From Lab on a Chip to Point of Care Devices: The Role of Open Source Microcontrollers," Micromachines, vol. 9, no. 8, p. 403, Aug. 2018, https://doi.org/10.3390/mi9080403.
152. S. K. Sia and L. J. Kricka, "Microfluidics and point-of-care testing," Lab Chip, vol. 8, no. 12, p. 1982, 2008, https://doi.org/10.1039/b817915h.
153. S. Park, Y. Zhang, S. Lin, T.-H. Wang, and S. Yang, "Advances in microfluidic PCR for point-of-care infectious disease diagnostics," Biotechnology Advances, vol. 29, no. 6, pp. 830–839, Nov. 2011, https://doi.org/10.1016/j.biotechadv.2011.06.017
154. B. J. Toley et al., "Multidimensional Paper Networks: A New Generation of Low-Cost Pump-Free Microfluidic Devices," J Indian Inst Sci, vol. 98, no. 2, pp. 103–136, May 2018, https://doi.org/10.1007/s41745-018-0077-1.
155. A. Böhm and M. Biesalski, "Paper-based microfluidic devices: A complex low-cost material in high-tech applications," MRS Bull., vol. 42, no. 05, pp. 356–364, May 2017, https://doi.org/10.1557/mrs.2017.92.
156. A. K. Yetisen, M. S. Akram, and C. R. Lowe, "Paper-based microfluidic point-of-care diagnostic de-

vices," Lab Chip, vol. 13, no. 12, p. 2210, 2013, https://doi.org/10.1039/c3lc50169h.
157. C. H. Ahn et al., "Disposable Smart Lab on a Chip for Point-of-Care Clinical Diagnostics," Proc. IEEE, vol. 92, no. 1, pp. 154–173, Jan. 2004, https://doi.org/10.1109/jproc.2003.820548.
158. P. Neuzil, J. Pipper, and T. M. Hsieh, "Disposable real-time microPCR device: lab-on-a-chip at a low cost," Mol. BioSyst., vol. 2, no. 6–7, p. 292, 2006, https://doi.org/10.1039/b605957k.
159. S. Sun, M. Yang, Y. Kostov, and A. Rasooly, "ELISA-LOC: lab-on-a-chip for enzyme-linked immunodetection," Lab Chip, vol. 10, no. 16, p. 2093, 2010, https://doi.org/10.1039/c003994b.
160. V. T. Upaassana et al., "Highly Sensitive Lab on a Chip (LOC) Immunoassay for Early Diagnosis of Respiratory Disease Caused by Respirable Crystalline Silica (RCS)," Anal. Chem., May 2019, https://doi.org/10.1021/acs.analchem.9b00582.
161. E. E. Tripoliti et al., "KardiaTool: An Integrated POC Solution for Non-invasive Diagnosis and Therapy Monitoring of Heart Failure Patients," presented at the 2018 40th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC), Jul. 2018, https://doi.org/10.1109/embc.2018.8513298.
162. X. Hou et al., "Erratum: Interplay between materials and microfluidics," Nat Rev Mater, vol. 2, no. 5, May 2017, https://doi.org/10.1038/natrevmats.2017.28.
163. A. Bohr, S. Colombo, and H. Jensen, "Future of microfluidics in research and in the market," in Microfluidics for Pharmaceutical Applications, Elsevier, 2019, pp. 425–465.
164. R. Lo, "Microfluidics technology: future prospects for molecular diagnostics," AHCT, vol. Volume 3, pp. 3–17, Feb. 2017, doi: 10.2147/ahct.s94024.
165. W.-C. Tian and E. Finehout, "Current and Future Trends in Microfluidics within Biotechnology Research," in Microfluidics for Biological Applications, Springer US, pp. 385–411.

Arrived: 04. 12. 2021
Accepted: 19. 03. 2021

Review scientific paper
https://doi.org/10.33180/InfMIDEM2021.102

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 51, No. 1(2021), 25 – 48

Nanotechnology and Nanoscience – From Past Breakthroughs to Future Prospects

Jernej Štremfelj, Franc Smole

University of Ljubljana, Faculty of Electrical Engineering, Ljubljana, Slovenia

Abstract: Nanoscience and nanotechnology are already improving our lives in numerous ways. The aim of this paper is to give an insight into the vast array of their potential future uses, as well as current applications, and present the major breakthroughs, which made their development possible. A special section is reserved for the development in the field of microelectronics, which is facing numerous challenges due to the downsizing of devices to the nanometre level. Current situation in microelectronics industry and predictions for the next few years are presented. Furthermore, the use of nanotechnology and future prospects in the fields of medicine, energetics, environmental protection and transport are described. A significant part of this paper is devoted to the field of electronics and information technology, where some potential nanotechnological solutions for the challenges of microelectronics are implied. The use of carbon nanotubes in logic circuits and memory applications is presented. The basic principle of single-electron transistor is also described. Basic concepts of the use of spintronics in magnetoresistive random access memory (MRAM) structures are explained. Memristor is also presented as an important future prospect. In the last part, the investments in nanotechnology and nanoscience under the funding programmes of European Union are presented, followed by some predictions of these fields' future development. However, the review paper focuses only on positive effects of the use of nanotechnology, and thus does not discuss its possible negative impact on public health and environment.

Keywords: nanotechnology; nanoscience; microelectronics; carbon nanotubes; quantum dots

Nanotehnologija in nanoznanost – od preteklih dosežkov do obetov za prihodnost

Izvleček: Nanoznanost in nanotehnologija že izboljšujeta naše življenje na različne načine. Namen članka je podati vpogled v širok nabor potencialnih področij njune uporabe tako v današnjem času, kot tudi v prihodnosti in predstaviti pomembnejša odkritja, ki so omogočila razvoj tega področja. Posebno poglavje je namenjeno razvoju na področju mikroelektronike, ki se zaradi manjšanja dimenzij na nanometrski nivo sooča s številnimi izzivi. Predstavljena je trenutna situacija v mikroelektronski industriji in obeti za naslednjih nekaj let. V nadaljevanju je predstavljena uporaba nanotehnologije in obeti za prihodnost na področjih medicine, energetike, varovanja okolja in transporta. Pomemben del članka je namenjen področju elektronike in informacijskih tehnologij, kjer so predstavljene nekatere potencialne nanotehnološke rešitve za izzive mikroelektronike. Predstavljena je uporabnost ogljikovih nanocevk v logičnih vezjih in pomnilniških strukturah. Razloženo je osnovno delovanje enoelektronskega tranzistorja. Podani so koncepti uporabe spintronike v pomnilniških strukturah MRAM (magnetoresistive random access memory), kot pomemben obet za prihodnost pa je predstavljen tudi memristor. V zadnjem delu so navedena sredstva, ki jih Evropska Unija v okviru svojih programov financiranja namenja za razvoj nanotehnologije in nanoznanosti. Navedenih je tudi nekaj napovedi glede razvoja opisanih področij v prihodnosti. V članku so predstavljeni le pozitivni vplivi uporabe nanotehnologije, medtem ko analiza morebitnih negativnih vplivov na okolje in zdravje ljudi ni vključena.

Ključne besede: nanotehnologija; nanoznanost; mikroelektronika; ogljikove nanocevke; kvantne pike

** Corresponding Author's e-mail: js8675@student.uni-lj.si*

1 Introduction

Nanotechnology focuses on developing materials, structures and systems by manipulating matter on the 1-100 nm scale [1], [2]. However, the final objective does not necessarily have to be nanodimensional. It is of most importance that new properties, which occur

at the nanometre scale are being taken advantage of [1]. The role of nanoscience is to pave the way for nanotechnology by studying those phenomena [2]. The fact is that the nanometre world behaves a little differently as one would expect based on one's visible and also micrometre world experience. Physical, mechanical, chemical, electrical and numerous other properties of particles are being completely changed as quantum effects begin to rule their behaviour [1], [3]. Those effects are studied by an important branch of modern physics, called quantum mechanics, which was developed after the year 1900 [1].

One of the fascinating results of quantum effects at the nanoscale is that the particle properties are changing with its dimensions. Therefore, material properties can be fine-tuned by changing the size of the particles. Thus, they can for example be labelled with fluorescent colours, which is useful for their identification [3].

An interesting example, which illustrates those unique properties is gold. A metal, which typically has a distinctive yellow colour, occurs as red or purple at the nanoscopic scale (Fig. 1). The reason for this phenomenon is that the movement of electrons is confined at the nanoscale dimensions, which gives golden nanoparticles a different light response, compared to bigger particles. Their small dimensions and special optical properties make them increasingly useful in medicine. They are being accumulated selectively in cancer cells, which allows precise laser destruction of tumour, without harming healthy cells [3].

Figure 1: Light response of gold nanoparticles with different diameters. Reprinted with modification (cropping) from [4]. Copyright 2016-2020 Phornano Holding GmbH.

Another quantum effect that is completely contradictory with the laws of classical physics is quantum tunnelling through a potential barrier [3], [1]. In 1981, a scanning tunnelling microscope was invented on its basis and brought a Nobel Prize in physics to its inventors [5], [6].

All of the aforesaid examples certainly give us an explanation why developers in many completely different areas of modern technology strive for miniaturisation. A simple thought experiment, which is depicted in Fig. 2, leads to additional arguments. Let us imagine a 1 cm^3 cube. Its surface area is therefore 6 cm^2. If we divide it into 1000 smaller cubes with 1 mm^3 volume, we get a total surface area of 6000 mm^2 or 60 cm^2. If we continue with this procedure to the nanometre scale, we get 10^{21} cubes with volume of 1 nm^3 and surface area of 6 nm^2 each. By adding their surface areas, we get an astonishing value of 6 km^2. Therefore, smaller particles have exceptionally large active surface area compared to their volume. Consequentially, there is more area for contact between particles, which increases their reactivity [3].

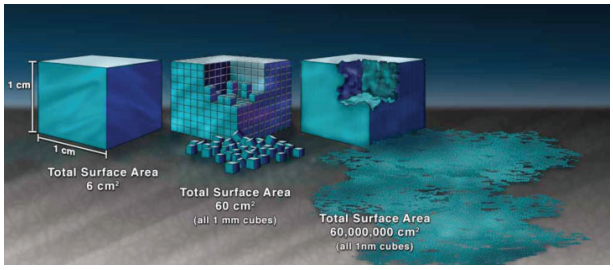


Figure 2: Increase in total surface area, achieved by diminishing particle size. Reprinted from [3]. Licensed under CC BY 3.0 license.

2 Microelectronics

However, when speaking about decreasing dimensions, especially electronic engineers firstly think about the famous Moore's law. Most electronic devices are downsizing especially due to their better functionality and compactness, and not because of fascinating nanodimensional phenomena. In addition, the devices are becoming cheaper with more chips being made on one silicon wafer. This development is made possible by downscaling of the basic components of integrated circuits – the transistors. The discovery of this element can be counted as the beginning of the microelectronic industry. This achievement was accomplished in 1947 in Bell Laboratories by William Shockley, John Bardeen and Walter H. Brattein, who were awarded Nobel Prize in physics, nine years later [1], [7].

Although the first transistor was a point-contact transistor (Fig. 3), it represented a basis for the development of the first germanium bipolar transistor, based on two pn-junctions, which was conceived in year 1948 by Shockley and fabricated in 1950. Four years

Figure 3: First transistor. Reprinted from [8]. Copyright 2020 Nokia.

later, Gordon Teal from Texas Instruments made the first silicon version [9]. Next big breakthrough happened in year 1958, when Jack Kilby realised integration of elements on the same germanium substrate (Fig. 4.c). In 1959, Robert Noyce integrated also the connections, this time on a silicon substrate, and therefore laid the foundations for integrated circuit development [10]. In the same year, Dawon Kahng and Martin John Attala made the first metal-oxide semiconductor field-effect transistor (MOSFET) by growing a silicon dioxide (SiO_2) layer on silicon wafer (Fig. 4.b) [11]. This was the first compact transistor, whose structure made possible the miniaturisation to the dimensions, used in today's complementary metal-oxide semiconductor (CMOS) integrated circuits [12]. The mentioned inventions are presented in Table 1 in chronological order. Two of them are also depicted in Fig. 4, which shows the progress in the design principles of electronic components and integrated circuits through years.

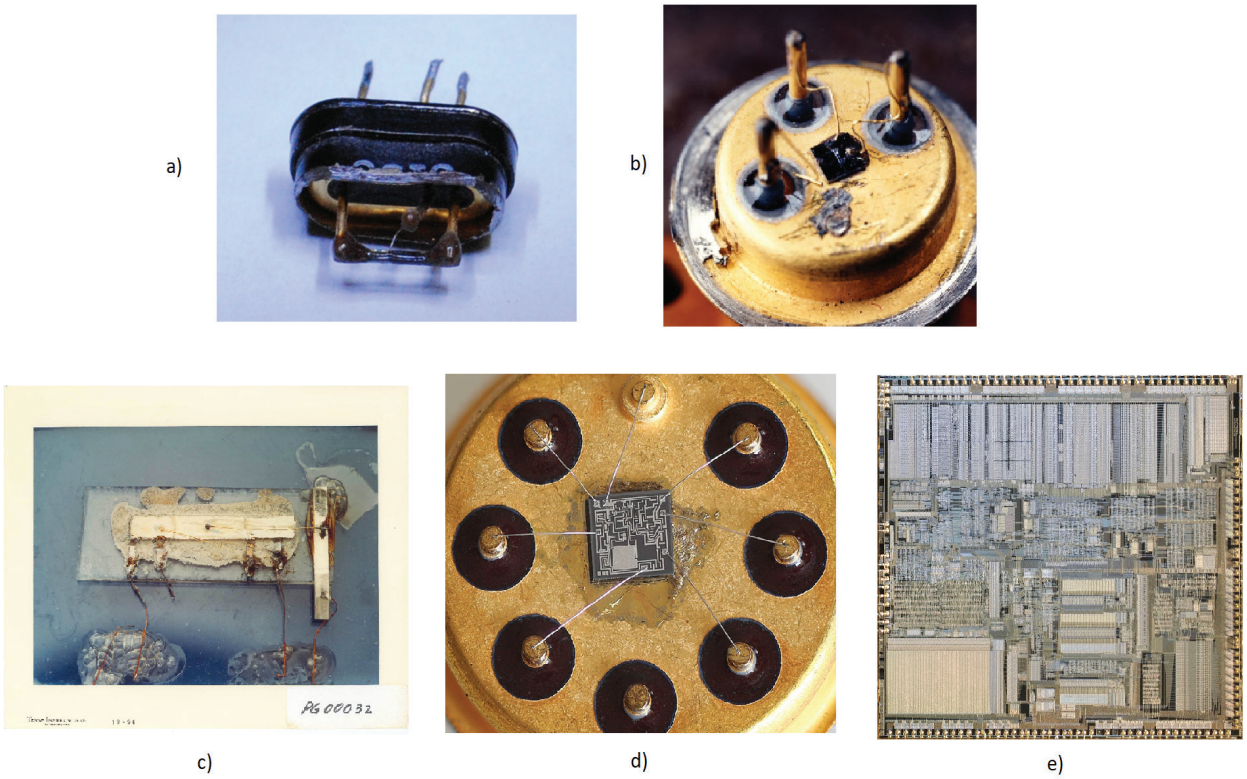


Figure 4: a) Silicon NPN grown-junction bipolar transistor of type ST2010, manufactured in 1961. Reprinted with modification (cropping) from [13]. Licenced under CC BY-SA 3.0. Author: David Forbes; **b)** First MOSFET, fabricated in Bell Laboratories in 1959. Reprinted from [14]. Copyright 2021 Nokia; **c)** First integrated circuit, fabricated in Fairchild Semiconductor in 1959. Reprinted from [15]; **d)** uA741 operational amplifier, made by Fairchild Semiconductor in 1969. Reprinted with modification (cropping) from [16]. Licenced under CC BY-SA 4.0. Author: Jay Philippbar; **e)** Die image of Intel A80386DX-20 32-bit microprocessor, introduced in 1987. The integrated circuit consisted of 275000 transistors [17]. Reprinted from [18]. Licenced under CC BY-SA 3.0.

Table 1: Important inventions, which made possible the development of microelectronics industry

Inventor	Year	Discovery
W. Shockley, J. Bardeen, W. H. Brattein	1947	First transistor
W. Shockley, G. Teal, M. Sparks	1950	First germanium bipolar transistor
G. Teal	1954	First silicon bipolar transistor
J. Kilby	1958	Integration of elements on germanium substrate
R. Noyce	1959	Integration of elements and connections on silicon substrate
D. Kahng, M. J. Attala	1959	First MOSFET

In 1965, Gordon E. Moore predicted that the number of components per integrated circuit would double every year in his article for the journal »Electronics« [19]. In 1975, he modified his assumption a bit, and predicted doubling approximately every two years [20]. 45 years later, we can conclude that his predictions were correct, which can be observed in Fig. 5. Achieving predicted miniaturisation became the driving force of microelectronics development.

In the middle of the 1980s, the minimal gate length of the MOSFET reached 1 µm, whereas at the turn of the millennium the typical dimensions were already at around 150 nm [21]. In 2005, the 65 nm technology was introduced, five years later the main manufacturers already produced chips in the 32 nm technology [1]. At this point, it is necessary to stress that inconsistencies between technology node names and actual transistor dimensions occurred through the years. The dimensions, stated in technology node name, are a consequence of International Technology Roadmap for Semiconductors (ITRS) [22] and its successor International Roadmap for Devices and Systems (IRDS) guidelines [23], which predict the development in this field for the next fifteen years. Until the mid-1990s, the technology node dimensions were consistent with the gate length of MOSFETs [24], while today they do not correspond to any of actual dimensions, but only reflect the general technology progress [25]. That being the case, the Intel's 250 nm technology transistors had gate length of 200 nm, while its 180 nm technology transistors from a year later only 130 nm. The trend of more aggressive gate length scaling lasted to the year 2007, when Intel reached the gate length of 25 nm with its 45 nm technology node. At that time, the gate length downscaling stalled for few years [26]. Miniaturisation to such small dimensions brought numerous disadvantages, which more than ten years ago indicated that CMOS technology would not be able to achieve further progress only

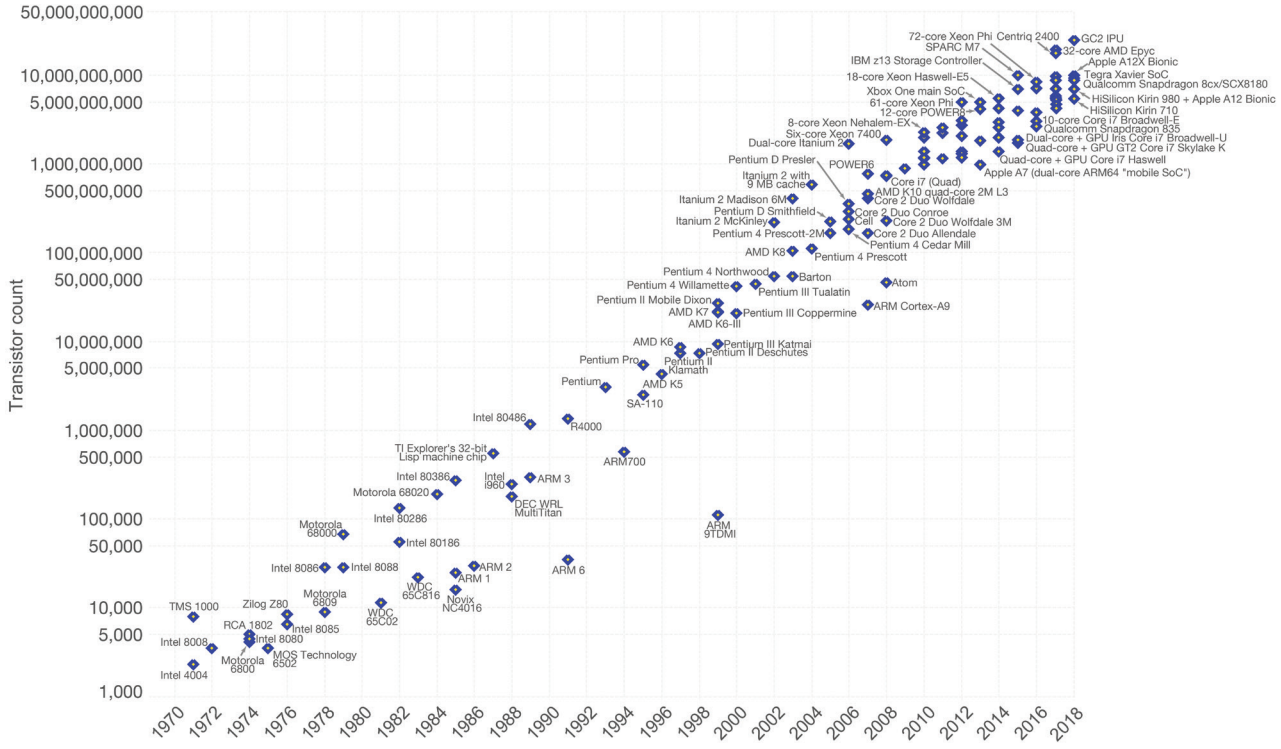


Figure 5: Number of transistors per integrated circuit between years 1971 and 2018. Reprinted with modification (cropping) from [29]. Licensed under CC-BY-SA 4.0 license. Author: Max Roser

by downsizing planar transistors. The MOSFET channel dimensions had decreased to such an extent that the voltage applied between the drain and the source began to cause significant subthreshold leakage, which increased static power consumption in CMOS circuits. As a solution, the first three-dimensional (3D) MOSFET – fin field-effect transistor (FinFET) entered mass production in 2011, within the 22 nm technology node [27].

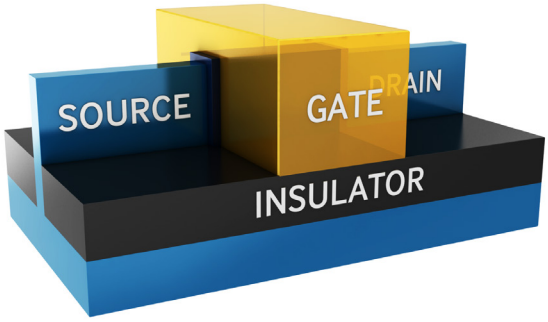


Figure 6: Visualisation of FinFET. Reprinted from [28]. Copyright 2010-2020 Samsung.

In this type of transistor, depicted in Fig. 6, the channel is vertically raised above the substrate and surrounded with the gate on three sides, which limits the mentioned current leakage. However, FinFET also has its disadvantages. By planar transistors, the channel width can be flexibly determined in order to achieve the desired current capabilities. Higher width-to-length ratio results in higher transistor current at certain gate-to-source voltage in the saturation region. It also brings higher transconductance of the transistor, which gives higher ratio between changes in drain current and gate-to-source voltage. By FinFET, the effective channel width cannot be so unrestrictedly set. It is equivalent to

$$2 \cdot h_{fin} + w_{fin} \tag{1}$$

where h_{fin} denotes the channel height and w_{fin} represents the channel width. The height is limited with manufacturing process, while changing the width-to-height ratio is undesirable due to the worsening of characteristics. That issue was solved by developing FinFET with multiple fin structures [1]. This version of FinFET is also being used in the latest 5 nm technology [30], whose mass production was started by Taiwan Semiconductor Manufacturing Company (TSMC) and Samsung in 2020 [31].

Nevertheless, the way for the mass production is paved by prior research and development, which at the same time give us a look into the future prospects. On that basis, it is assumed that FinFET is soon going to be replaced with new solutions. The developers found additional room for improvement in the fact that FinFET's bottom side was still connected to the body of the silicon, which meant that the subthreshold leakage could be further reduced. The idea was realised by the development of a transistor with the gate surrounding the channel on all sides – gate all-around field-effect transistor (GAAFET) [27].

The result of GAAFET development was firstly a transistor with the channel region in the shape of a very narrow nanowire. However, the small channel dimensions did not provide sufficient currents and consequentially switching speeds, which was soon solved by stacking nanowires on the top of each other (Fig. 7 – GAAFET). Unfortunately, this approach also brought several limitations. Similar as by FinFET, the stack's height was limited. Furthermore, additional nanowires increased the device's capacitance and thus slowed the transistor's switching speed. Another downside was the complex manufacturing of very narrow nanowires, which could lead to structure irregularities [27].

The discussed problems were diminished by developing a transistor with nanosheets (Fig. 7 – MBCFET), which is, according to Samsung, going to be used in the 3 nm technology, whose mass production is predicted to begin in the next years [32]. This is an improved version of the aforementioned GAAFET, with stacked thin sheets of silicon instead of nanowires. Thus, the effective channel width is increased, while the leakage current is still limited. Moreover, the variable sheet width enables the channel width flexibility, which is not the case by FinFET [27].

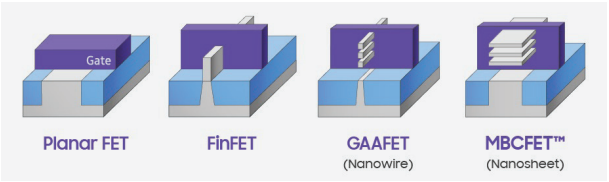


Figure 7: Evolution of Samsung's field-effect transistors. Reprinted from [33]. Copyright 2010-2020 Samsung.

With all the described improvements, the validity of the Moore's law, whose end has been foreseen by many, certainly extended for at least a decade. Nonetheless, all mentioned solutions are still based on the elementary version of silicon MOSFET, where the photolithography with all its limitations remains the main technological process. The main problem regarding photolithography is that at the nanoscale dimensions, the diffraction of light causes significant random manufacturing variations, which can result in unpredictable behaviour of elements [1]. Nevertheless, we are witnessing a fast development also in this field.

In the second half of 2019, the extreme ultraviolet lithography (EUVL) at 13,5 nm wavelength succeeded the deep ultraviolet lithography using excimer argon fluoride (ArF) laser at 193 nm wavelength, in mass production of some 7 nm technology integrated circuits [34], [1]. Despite the promising predictions of using even shorter wavelengths, which could be made possible by the development of beyond extreme ultraviolet lithography (BEUVL) [35], it is quite probable that downscaling, using only lithography processes will soon come to an end.

Another issue, brought by small dimensions of integrated circuits and high transistor density, is cooling. One of its consequences is the stall of the processor frequency, which has not significantly improved for approximately a decade and remains below 4 GHz in most cases. A potential solution for the near future is in using other, more efficient semiconductor materials as silicon, for example indium-gallium arsenide (InGaAs) [27].

Regardless of all foregoing solutions, it is inevitable that electronics industry is going to face essential changes in the future. It will be necessary to find alternatives to the CMOS technology, which are most likely going to be based on the aforementioned nanodimensional phenomena. Downscaling brought the dimensions almost to the atomic level and consequently gave us a completely different perspective of future technological development. New approaches to the mentioned problems, using new materials are being researched. Many studies already focus on the self-assembly of nanostructures on the atomic level [1].

3 Atoms

The idea of manipulating single atoms stirred already the imagination of ancient Greek philosophers. In the fifth century before Christ, philosophers Democritus and Leucippus, who were also the founders of the Greek philosophical school of atomism [36], stated that everything was composed of *atomos* (Greek word for "unbreakable"), which were indivisible. They claimed that those particles were solid and homogenous but varied in size, shape and weight. Between them, there was only empty space. Later on, their ideas came in for criticism and disapproval from other philosophers and were also considered atheistic by Christians [37].

Scientific establishing of the atomic theory began in the 17. century, when British scientist Robert Boyle proved the inverse relationship between the pressure of a gas and its volume, which is known as Boyle's law. The pressure in a container of gas is a consequence of the atoms' collisions with the container walls, which are more significant at a smaller volume of container. At the end of the 18. century, a French chemist Joseph Louis Proust empirically discovered that the ratio between different elements in a chemical compound always remains the same, without being affected by the way of its preparation, which is consistent with the Democritus' concept of indivisibility. His theory was later expanded by John Dalton, who figured out that the molecules consisted of fixed number of different atoms and therefore laid the foundations for the modern atomic theory [37].

In the 19. century, the question arose, what are the atoms composed of. Joseph John Thomson was one of the scientists, who tried to answer it. He experimented with a closed glass tube with almost no air inside. With high voltage applied across two metal electrodes in it, he produced a visible ray and found out that the ray deflected in presence of electric or magnetic field. On the basis of the deflection and magnetic field measurements, he concluded that the particles in this ray were significantly lighter than atoms. In addition, he observed that they were attracted by positive charge and repelled by negative, which indicated their negative charge. He got similar results when using electrodes of other metals, which lead him to a conclusion, that these particles were present in all atoms [38]. Therefore, he showed that the atoms were not indivisible and proved the existence of electrons [39]. In 1904, he proposed a model of atom, depicted on Fig. 8.a, where the electrons were embedded in positively charged mass, making the atom electrically neutral. Next important breakthrough in studying electrons' properties was achieved in 1909 by Robert Andrews Millikan, who found out the value of charge and mass of a single electron. However, the form of the atoms, especially the positively charged part, was still not properly explained [38].

The inaccuracy of by then proposed atom models was proved by Ernest Rutherford in 1911, even though he initially tried to confirm their correctness. He, Hans Geiger and Ernest Madsen conducted an experiment where they directed a beam of positively charged alpha particles to thin gold foil and observed their deflection. Assuming the Thomson's model, which implied distribution of positive charge over the entire atom, was correct, they expected little or no deflection of particles. However, whereas most of the particles really passed through the foil without any deflection, some of them were significantly diverted. On that basis, Rutherford concluded that most of the atom's volume consisted of empty space, whereas at the centre of atom, there was a small, positively charged nucleus. He proposed a new model of atom, depicted on Fig. 8.b, with the electrons orbiting around the nucleus [38], [39]. Later, he discovered that all elements' nuclei contained hydro-

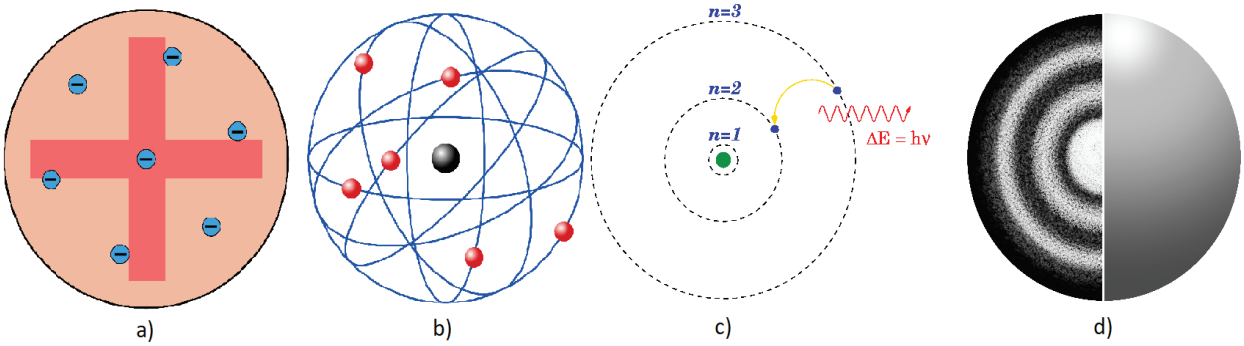


Figure 8: a) Thomson's atomic model, called also "The plum pudding model". Reprinted from [40]. Licenced under CC BY-SA 4.0.; **b)** Rutherford's atomic model. Reprinted from [41]. Licenced under CC BY-SA 3.0.; **c)** Bohr's atomic model. Reprinted from [42]. Licenced under CC BY-SA 3.0.; **d)** Schrödinger's atomic model, called also "The quantum mechanical model" or "Wave model". Reprinted from [43]. Licenced under Pixabay License.

gen nuclei – positively charged subatomic particles. He named them protons [38].

In 1913, Niels Bohr found out that the movement of the electrons in orbits with arbitrary radii, as proposed in Rutherford's model, was unstable. According to the classical physics, electrons would emit electromagnetic radiation when orbiting and consequently lose energy. Therefore, their orbits' radii would diminish, so they would spiral towards the nucleus. Based on the findings of Max Planck and Albert Einstein, who postulated that the energy of radiation could have only discrete values, Bohr stated that the angular momentum of the electron was also quantised. Due to the quantisation, the orbits had fixed radii and energies. In order to jump to another orbit, the electron had to emit or absorb the energy equal to the difference of two orbits' energies [44]. The Bohr's model of atom is depicted on Fig. 8.c.

However, the Bohr's theory did not prove to be entirely correct. His model was based on the hydrogen atom, and could not explain the emitted spectrum of atoms with more electrons. Even hydrogen's spectrum was not adequately explained with Bohr's energy levels. Its individual spectral lines proved to be divided into more, closely spaced ones, which showed the existence of additional energy states [44], [45].

In the early 1920s, the scientists started to develop a theory, where the matter was assumed to have both particle and wave characteristics. In 1923, Louis Victor de Broglie stated that the electrons should also be considered that way [44].

In 1926, Erwin Schrödinger developed an equation, which represented the foundation of the quantum mechanics. It described the form of wave functions, whose values at a given point of time and space gave the information about the probability of the particle, being at that point. He applied and also successfully solved it for the hydrogen atom [46], [47]. Therefore, he proposed the quantum mechanical model of atom (Fig. 8.d), where the electrons were treated as waves. Instead of the exact location of an electron, only the probability of the electron, being in a given region could be determined [48]. The Schrödinger's model of atom is still accepted as the most accurate one [39].

Nevertheless, the structure of atomic nucleus was not yet entirely understood. It was known that it contained protons, but its mass indicated the existence of additional building blocks [49]. In 1932, James Chadwick observed the reaction between alpha particles and beryllium atoms. Neutrally charged particles with approximate mass of proton were emitted. These particles were named neutrons [50]. This finding also explained the existence of isotopes – chemically indistinguishable atoms with different atomic masses, discovered by Frederick Soddy about twenty years before. The isotopes of a same element have different number of neutrons and consequentially different atomic masses, whereas their chemical properties remain the same, because of the same number of protons [38], [51].

Another quantum phenomenon that is important for understanding the atom's structure is the electron spin. It was experimentally discovered by Otto Stern and Walther Gerlach in 1922. They directed a beam of electrically neutral silver atoms through an inhomogeneous magnetic field. On the basis of the classical physics and the assumption that the electrons would act as magnetic dipoles, they expected that the atoms would be deflected in different directions, based on the magnetic dipole moments' orientations, giving a random and continuous distribution on the screen. However, the atoms were deflected only in two directions. That result clearly indicated that electrons could exhibit only two possible, antiparallel orientations, which could not

be explained by classical physics. The reason for that result was in the electron spin, which could have two possible values. Up and down [48], [1].

Three years after the abovementioned experiment, Wolfgang Ernst Pauli discovered that only two electrons could be located in the same orbital or energy level. In addition, they had to have the opposite spin. Hence, the electrons repel each other not only because of the charge, but also due to the parallel spins [1].

Another interesting empirical discovery was made by Friedrich Hund, who found out that the electrons in ground state always occupy the maximum number of empty orbitals. Therefore, if more energetically equivalent orbitals are available, they occupy the empty ones, rather than join an electron in a half-occupied orbital. Such arrangement of electrons is more stable [1].

Since that time, our understanding of the atomic world improved even more. However, the described transition from classical mechanics to quantum mechanics, which crucially influenced the atomic theory, represents one of the most important advances in the history of physics. All the mentioned findings made many achievements of the nanotechnology possible. The electron spins can for example be used as qubits in quantum computing. The electron and also nuclear spin of phosphorus donor in silicon proved highly appropriate for such use [52], [53], [54].

4 A half century of nanotechnology

The outstanding potential of the abovementioned possibilities fascinated an American physicist Richard Feynman in the 1950s. His prophetic speech »There's Plenty of Room at the Bottom«, which he held at the annual banquet of the American Physical Society in 1959, could be counted as the beginning of the history of nanotechnology. Therein, he pointed out that the technology process miniaturisation to the atomic level was completely realisable according to the laws of physics and predicted that future technology was going to be based on rearranging the atoms as desired. He talked about the bottom-up approach, which represented an alternative to the top-down approach, which has been driving the miniaturisation in the field of microelectronics, according to the Moore's law, for many more years. Feynman motivated the audience with numerous challenges, like for example writing the entire Encyclopaedia Britannica on a pinhead, or making an electrical motor, smaller than 0.256 cm^3 and also offered a pair of 1000 $ prizes. Some of the challenges were already realised in months after the speech, which made it clear that his predictions were going to come true even sooner than he expected [37].

The term »nanotechnology« was first used in 1974 by a Japanese scientist Norio Taniguchi in a paper about the technological concepts on the nanometre level. He stated that atoms and molecules with the dimensions of 0.1-0.2 nm are the smallest particles in the processing of materials. In addition, he defined the separation, consolidation and deformation of materials by single atoms or molecules as a main part of the nanotechnology [55].

A very important breakthrough in further nanotechnology and nanoscience development was achieved in 1981 by the scientists of the company International Business Machines (IBM) Zürich, who invented the aforementioned scanning tunnelling microscope [5]. Five years later, the atomic force microscope was invented in the same company and became the most important tool for observing and manipulating material on the atomic level [56]. In the following years, the increasingly efficient computing systems enabled progressively demanding simulations, which, alongside with the experimental work, lead to fast development. In 1989, another scientific team from IBM managed to align 35 atoms of xenon in the form of letters »IBM« (Fig. 9) [57].

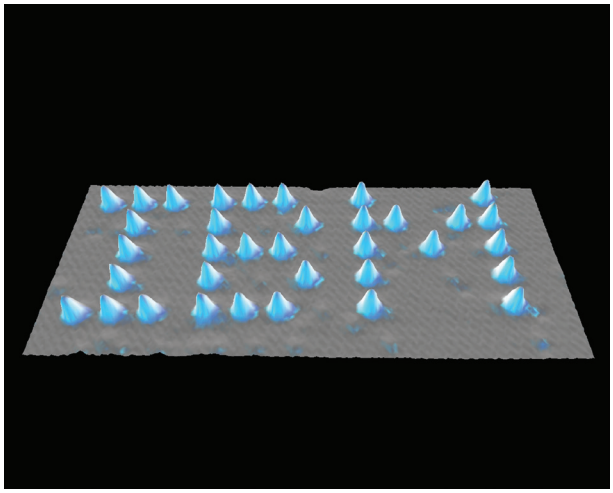


Figure 9: Thirty-five xenon atoms, arranged in the form of "IBM". Image originally created by IBM Corporation.

Another very important discovery had been made four years before by scientists Robert F. Curl, Harold W. Kroto and Richard E. Smalley, who discovered the carbon allotrope – buckminsterfullerene (C_{60}) [58]. As a consequence, special structures of fullerene – the carbon nanotubes (CNTs) were discovered in 1991 [59].

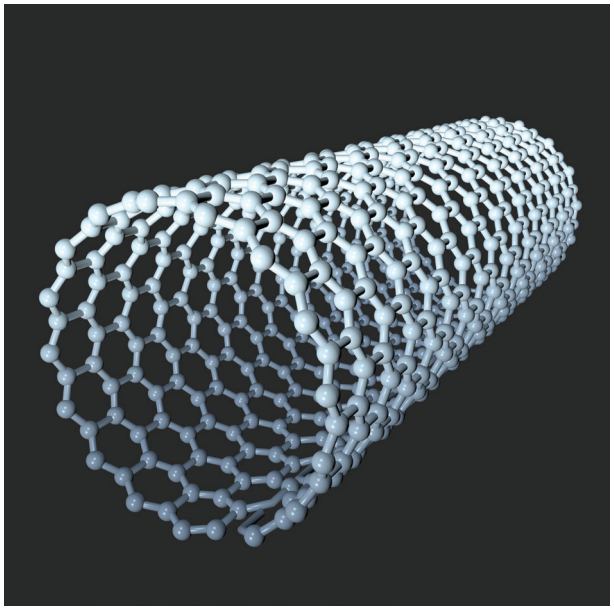


Figure 10: Visualisation of a CNT. Reprinted from [60]. Copyright 2000-2020 Dreamstime.

A structure of a CNT can be imagined as a graphene sheet, rolled into a hollow cylinder, as shown in Fig. 10. The carbon atoms are connected by sigma (σ) bonds, which are the strongest type of covalent chemical bonds. This makes CNTs the strongest fibres. Topological defects in their structure, like pentagons and heptagons, embedded in the hexagonal lattice, enable their termination, as well as formation of joints and toroidal or spiral shaped nanotubes. In addition to the mechanical ones, they also have outstanding electrical, chemical, optical, magnetic and thermal properties. Their diameter varies between 0.4 nm and 3 nm for single-wall CNTs or up to 100 nm for outer walls of multi-wall CNTs. They can be metallic or semiconducting. Researches have shown their potential as sensors, actuators, batteries, fuel cells, capacitors and field-emission devices, which makes them one of the most promising materials in the field of nanotechnology [1].

The studies of semiconductor nanocrystals also lead to the development of quantum dots [61]. These are small, in most cases semiconductor structures, with the dimensions that are comparable or smaller than the Fermi wavelength, which is around a nanometre for metals and few dozen nanometres for semiconductors. Therefore, the movement of electrons is restricted in all three dimensions, which results in discrete energy states of electrons that completely change the material properties (Fig. 11) [1].

What is more, the small dimensions bring higher reactivity to the material, because of more atoms on the surface, which can interact with the environment.

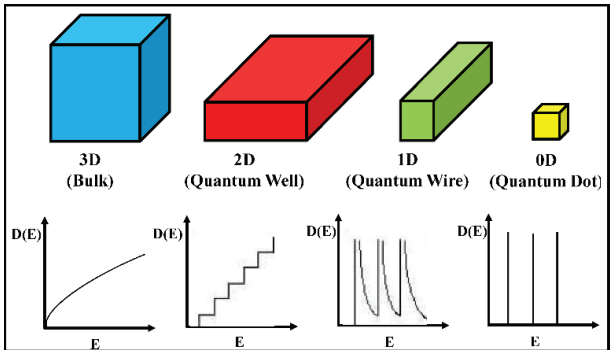


Figure 11: Diagram of density of states for different forms of semiconductors. Discrete energy states can be observed in case of quantum dots. Reprinted from [62]. Licensed under CC BY-NC-SA 3.0 license.

Quantum dots can be used as charge islands in the circuits based on the Coulomb blockade [1]. Additionally, their exceptional optical properties make them potentially useful in lasers, photodetectors [63], displays [64], solar cells [65] and also as biological markers. The return of excited electrons to the ground state produces light emission. Therefore, by making sure that for example a semiconductor quantum dot stops on a cancer cell and is appropriately illuminated, a tumour can be detected [1].

In the 1990s, the progress of nanotechnology continued at an increasingly high rate. In 1992, nanostructured catalytic materials MCM-41 and MCM-48 were discovered. They are still being heavily used in refining crude oil and also in medicine [66], [67].

Seven years later, Lee and Ho from American university Cornell managed to assemble molecules of Cu(CO), Fe(CO), $Cu(CO)_2$ and $Fe(CO)_2$ from individual iron (Fe) and copper (Cu) atoms and carbon oxide (CO) molecules, by using a scanning tunnelling microscope [68].

In the same year, Chad Mirkin invented dip-pen nanolithography and so introduced one of the alternatives to the before described photolithography. As the name suggests, the material is deposited on the surface by an atomic force microscope tip, similarly as by writing with a pen on the paper (Fig. 12) [69]. Therefore, a mask is not necessary, which is a crucial benefit [1].

In the following years, nanotechnological solutions started to make their way to commercial products. Scratch-resistant car bumpers, antibacterial socks, faster-recharging batteries, electronic devices with improved displays and similar products began to appear. The scientific achievements in this field were also increasingly frequent [67].

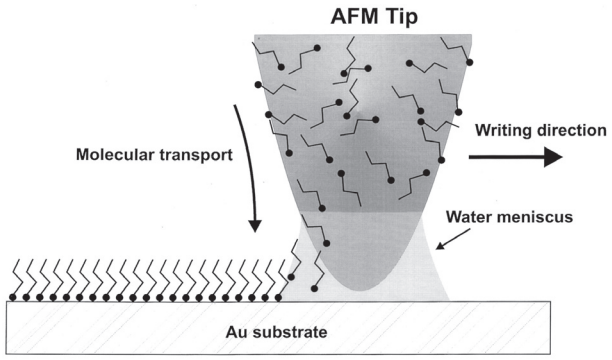


Figure 12: Writing principle of dip-pen nanolithography. From [69]. Reprinted with permission from AAAS.

In 2003, the scientists at Rice University developed gold nanoshells, which at the right dimensions absorb near-infrared light and can therefore be used for discovery, diagnosis and also treatment of breast cancer [70], [67].

Two years later, Barish, Rothemund and Winfree from the California Institute of Technology made deoxyribonucleic (DNA) crystals that perform operations of copying and counting by self-assembling and hence demonstrated the potential of algorithmic self-assembly for being used in creating complex nanoscale patterns [71]. Self-assembly of smaller components into larger and more complex ones due to intermolecular forces, similar as in nature, became one of the most promising fields of research in nanotechnology [1]. In 2010, Seeman and his team from New York University made a 3D self-assembling DNA structure, whose construction can be programmed by putting small cohesive sequences on ends of the patterns [72].

Another unique achievement was made by IBM in the same year. Using a nanometre-sized silicon tip, they created a 3D relief world map with the dimensions of 22 µm by 11 µm in two minutes and twenty-three seconds [73], [74]. Considering the fact that bottom-up approach is in general slower than its top-down counterpart, achieving such manufacturing speed is very important. Thus, this achievement confirmed the great potential of such technological procedures.

During the described development, most of the leading industrial countries established the organisations committed to the progress of nanotechnology, where study of nanodimensional material properties in order to develop new processes and appliances, which in the end also bring economic results, remains the main research objective. Moreover, the education in this field and the awareness of the nanotechnology's impact on public health and security are becoming increasingly important [75], [76], [77], [78].

5 Nanotechnology and nanoscience today and tomorrow

Nowadays, nanotechnology is a part of our lives, which is reflected on many different areas. Alongside with nanoscience, it plays a key role in the development and revolutionary improvements in electronics, information technology, medicine, energetics, transport, environmental remediation and generally our everyday life. The expectations of future development are also very promising [79].

5.1 Everyday life

Numerous commercial products for everyday use, which are based on the use of nanomaterials are already available. Thin nanoparticle films on glasses, windows, computer screens and other surfaces make those surfaces water and dust repellent, anti-reflective, ultraviolet or infrared light-resistant, scratch-resistant or even electrically conductive [79]. Smart textiles with many nanosensors, which react to the stimuli from the environment and the human body are being developed [80], [81]. Nanoparticles are being added to the materials for tennis rackets, bicycles, helmets and car parts and are therefore making them lighter, stronger and more flexible. Nanostructures are also used in degreasers, stain removers and air purifiers. Another field of their use is personal care. Nanoparticles of titanium dioxide (TiO_2) and zinc oxide (ZnO) have been used in sunscreens for years [79], [82].

5.2 Medicine

Nanotechnology is being increasingly used in modern medicine. Its contribution to the new solutions for disease prevention, diagnosis and treatment is of great importance. It is enabling the development of better diagnostic tools, which are crucial for early disease diagnoses, which increase the probability of successful treatment [79]. A promising example are the already mentioned gold nanoparticles with their unique physical properties, which can be used as probes for detection of specific nucleic acids sequences [83] and are also applicable to the most sophisticated photothermal cancer therapy methods [84]. In addition, they can serve as a tool for cancer imaging [85], [86]. Nanotechnology also has an enormous potential for treatment and diagnosis of atherosclerosis. High density lipoprotein (HDL) mimicking nanoparticles have been designed and are expected to have similar properties to native HDL, also known as »good cholesterol«, which removes cholesterol from atherosclerotic plaques [87]. Nanotechnology is also enabling the establishment of more effective drug delivery methods for the treatment

of ophthalmological, pulmonary and cardiovascular diseases along with cancer therapy, where nanoscale delivery carriers are targeted directly to the cancer cell, improving the treatment efficiency and reducing side effects [88]. Bone and nerve tissue engineering also represent promising fields of research. It is possible to compose nanomaterials which are able to mimic the architecture of natural bone [89]. Nanoparticles have been also applied to many virus detection methods. A promising technique has recently been reported to detect severe acute respiratory syndrome coronavirus 2 (SARS-CoV-2), which causes coronavirus disease 19 (COVID-19). They are also suitable for targeted vaccine delivery to mucosal and alveolar structures [90], which could serve as an alternative to parenteral vaccine administration [91].

5.3 Energetics

Nanotechnology is changing the field of traditional, as well as alternative energy sources. Numerous solutions for low loss energy generation and distribution with less of a negative environmental impact are being researched [79].

Nanocatalysts are improving the efficiency of many conversion processes in petroleum processing industries [92]. Moreover, car fuel consumption can be reduced by adding metallic nanoparticles to fuel, which ensure more efficient combustion [93]. Already described CNTs have proved effective as a low-temperature adsorbents for carbon dioxide (CO_2) capture from power plant flue gas [94]. CNT fibres also have a future potential to be used in electrical wiring. By controlled assembly of CNTs, material with excellent electrical conductivity could be produced [95]. In addition, improved materials for wind turbine blades are also being developed using CNTs, which enable production of more durable and more efficient blades [96]. Nanotechnology is utilised also in the new photovoltaic solutions, where perovskite solar cells with their high efficiency and low cost represent a promising future prospect. They can also be utilised in tandem solar cells (Fig. 13), which possess a higher power conversion efficiency potential than single-junction solar cells [97]. Different principles, including the utility of colloidal quantum dots are also being developed for thermoelectric generators, which can be used in converting waste heat into electrical power [98].

5.4 Environmental protection

In addition to the mentioned energy efficiency improvements, nanotechnology also offers other possibilities, which can lead to better environmental protection. Advancements are being achieved in detecting and removing the contaminants from different substances [79].

Water purification is one of the most common examples where nanomaterials can be utilised, improving existing remediation technologies [100]. Another example is water desalination with a single-layer molybdenum disulphide (MoS_2) nanopore, which can effectively reject ions, allowing water flux that is two to five orders of magnitude greater comparing to other known nanoporous membranes [101]. Nanotechnology based techniques, using nanoscale zero-valent iron, CNTs and other nanomaterials are being developed for oil removal, which can contribute to future improvements of oil spill remediation [102]. Toxic gases in the ambient air can also be removed, exploiting adsorption properties of CNTs and gold nanoparticles [100]. CNTs can also be utilised in biosensors with fast responses and high sensitivity due to their electrical conductivity, which is highly dependent on the concentration of certain gas molecules [1]. Fig. 14 depicts a FET-based CNT sensor structure.

5.5 Transport

Nanotechnology offers various possibilities for improving the existing technologies for automotive industry. With its capability to preserve lighter and stronger

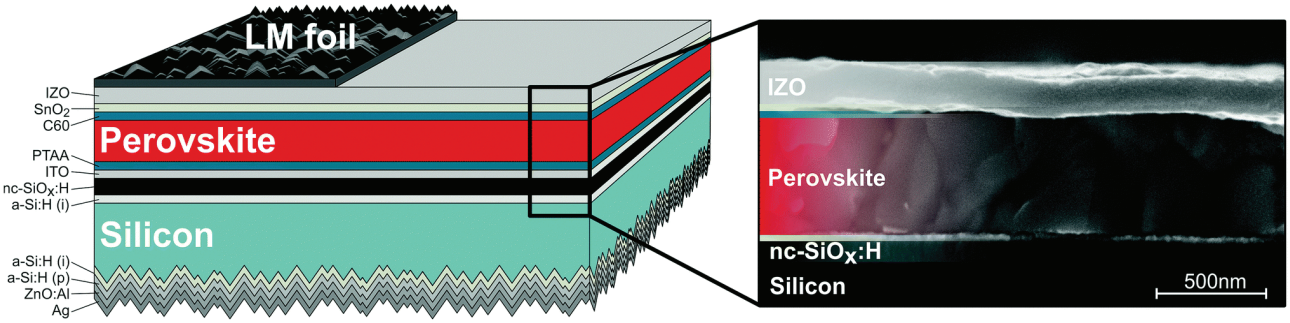


Figure 13: Structure of a perovskite-silicon tandem solar cell. Reprinted from [99]. Licensed under CC BY-NC 3.0 license.

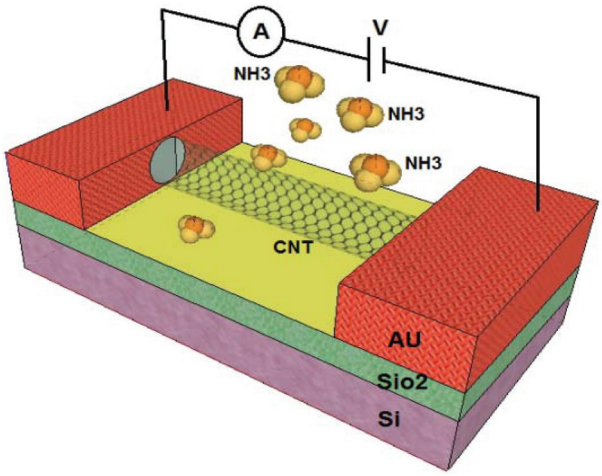


Figure 14: CNT gas sensor. Reprinted with modification (cropping) from [103]. Licensed under CC BY 3.0 license.

body parts and therefore enhance safety and fuel efficiency, it can be incorporated in various parts of the vehicle. Coating with nanoparticles can improve the durability of paint and make it more scratch-resistant. In addition, ultra-thin hydrophobic layers of aluminium oxide on the mirrors significantly reduce the light reflection. Moreover, nanoparticles of aluminium oxide can improve the tire durability when added to the rubber composite. Aluminium nanomaterials also have the potential to reduce friction of the engine cylinder walls, and therefore improve the engine efficiency [104]. Nano-composite materials are also very promising in the field of aviation. CNT reinforced polymer (CNRP) can be incorporated in airframes, as an alternative to conventional aluminium. Study of O'Donnell and Smith [105] showed, that a decrease in airframe structural mass of 10,07% on average, as a consequence of using CNRP, resulted in decreased fuel consumption of 11,2%. Composite materials, reinforced with CNTs could also reduce icing effects [104]. Furthermore, nanotechnology also enables the progress in materials used for maritime transport. A study was made, where material with nanostructured titanium dioxide (TiO_2) polymer coating proved to have higher corrosion resistance in seawater [106].

Alongside with all abovementioned improvements and future prospects, the transport engineering is also predicted to utilize nanotechnological solutions in future [107]. Nanostructure modification of materials should enhance their performance [108]. Nanoparticles represent one of the key technologies available for self-healing asphalt pavement design [109]. Highly sensitive nanosensors could also be embedded in concrete and asphalt materials and therefore be used for the monitoring of road infrastructures [110].

5.6 Electronics and information technology

As already described, an astonishing progress has been made in electronics during the last fifty years. However, the miniaturisation has also brought many aforementioned issues, which do not allow further development of CMOS technology only by downscaling planar silicon MOSFETs. Consequently, new approaches are being developed by using different materials, where the special nanodimensional characteristics play a significant role. Despite the fact that silicon technology is still far from being replaced, the breakthroughs in nanotechnology clearly indicate that the development in the field of electronics is not going to stagnate soon [1].

5.6.1 Carbon nanotubes

As much as in other fields, CNTs also represent a promising prospect in electronics. Similar as in the silicon technology, the p-type and n-type nanotube together form an element with semiconducting properties. Likewise, a structure with the properties similar to those of heterojunction diode can be formed using a p-type semiconductor nanotube and a metal nanotube. If such a structure is placed on a silicon dioxide substrate with a gate contact, an element, similar to the junction field effect transistor (JFET) is formed. First experimental versions of CNT field effect transistors (CNTFET) were introduced in 1998. Metal contacts were placed on the layer of oxide, which was deposited on the silicon gate. Then, a CNT, which served as a channel, was grown between the metal electrodes by chemical vapour deposition (Fig. 15). Researches have shown that by increasing gate voltage, the Schottky-barrier on the metal-nanotube junctions is being decreased, thus increasing the current [1].

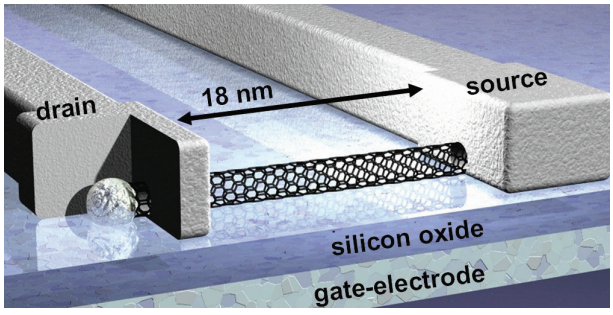


Figure 15: Structure of CNTFET with a channel length of 18 nm, constructed by Infineon in 2004. Reprinted from [111]. Copyright 1999 - 2020 Infineon Technologies AG.

The design of CNTFET electrical circuits is quite similar to conventional technologies. The capability of creating both p-type and n-type nanotubes enables the design of CMOS-like circuits, identical to those in the silicon technology, which are known to be the most energy ef-

ficient. Extraordinary properties of CNTs represent the main advantage of CNTFETs over conventional MOSFETs. Clock frequencies up to 1 THz could be reached in the future due to their high carrier mobility [1]. With their energy efficiency and extremely small dimensions, those transistors represent one of the most perspective candidates for the successor of silicon-based technology. Nevertheless, the development of such transistors is facing numerous problems. Firstly, it is impossible to synthesise only semiconducting nanotubes. To achieve that, the diameter and chirality of CNTs would have to be precisely controlled. Thus, every CNT synthesis results in a certain percentage of metallic CNTs, whose conductance cannot be sufficiently modulated by the gate of CNTFET. Secondly, CNTs bundle together into random structures during wafer fabrication, which results in CNTFET failure. Thirdly, the conventional CMOS technology demands the fabrication of transistors with precisely controlled and tuneable properties, which is a severe issue by CNTFETs [112]. In 2013, Shulaker et al. in [113] demonstrated a miniature one-bit computer, made from 178 CNTFETs, whereas in 2019 they introduced a 16-bit microprocessor, comprising more than 14000 CNTFETs. During its development, they evolved new techniques of circuit design for significantly decreasing the effect of metallic CNTs. Moreover, they developed an efficient process for removing undesirable CNT bundles on the wafer, using special adhesive promoters and solvents [112]. They predict that CNTs in combination with the silicon-based technology could become a part of the integrated circuits production in few years [114].

The CNTs are also very promising in the field of data storage. Nano random access memory (NRAM) structures, whose cells comprise of hundreds of CNTs, positioned between two electrodes, are being developed. Depending on the voltage on the electrodes, nanotubes connect or disconnect from each other (Fig. 16), which reflects in changed resistance, representing a logical one or zero. One of the main advantages of NRAM is the non-volatility of CNTs, caused by molecular binding forces, which keep them connected or separated without any voltage applied. NRAM is projected to retain data for more than 300 years at 300 °C. Furthermore, by stacking the layers of memory cells on top of each other, very high data storage density could be achieved in the future [115].

CNTs can also be utilised as light sources in optoelectronics. Under certain circumstances, electrons and holes can enter the CNT simultaneously from the opposite sides. When they meet, a recombination occurs, where the electron jumps from the conduction to the valence band, releasing the energy in the form of light. Another promising future area of usage are the ultra-

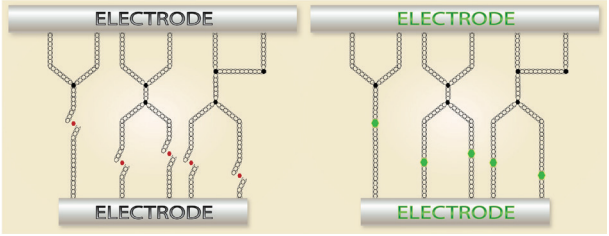


Figure 16: Working principle of NRAM. Data is stored by connecting or disconnecting CNTs between the electrodes. Reprinted with modification (cropping) from [116]. Copyright 2020 Nantero.com.

thin computer screens, which are based on the field electron emission of the CNTs and are expected to be very energy efficient with better brightness and longer life span [1].

5.6.2 Quantum dots

Quantum dots also possess many potential applications in electronics. Besides of those using the light emission of electron, which returns to the ground state, there are also other possibilities for their utilization. Quantum dot is a part of single-electron transistor. That is a structure, where the electrons are tunnelling between either source or drain and the quantum dot in between. The amount of energy needed for the tunnelling to take place is tuned by the third electrode – the gate, which is capacitively coupled to the quantum dot island (Fig. 17) [117].

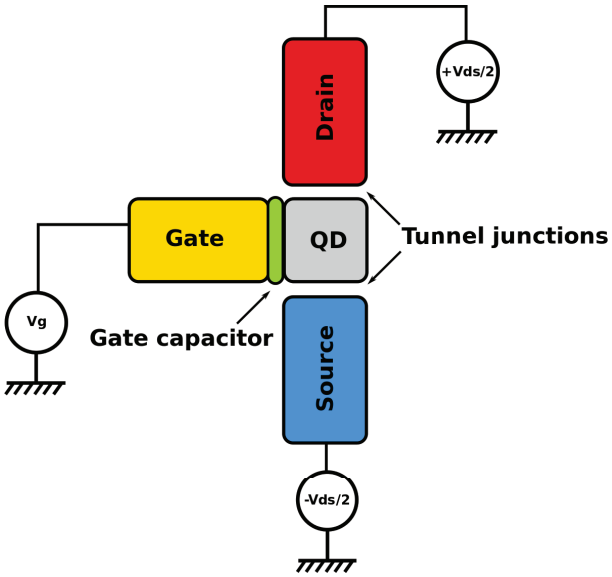


Figure 17: Schematic visualisation of a single-electron transistor. Reprinted from [118]. Visualisation is in the public domain.

Tunnelling of the electrons, which results in electrical current, is due to the Coulomb blockade possible only when appropriate combination of voltages is applied

to the gate terminal and between drain and source electrodes (Fig. 18). Thus, the switching operation of the transistor is enabled at very low power consumption, which represents a potential for the future of logical circuits. Coulomb blockade can be observed only at small enough dimensions, which result in small capacitances between the quantum dot and the source or drain electrode. In this case, when the potential difference between for example the source and quantum dot is too small, the tunnelling is not possible due to negative change in energy, stored in electric field between the electrodes, which would occur by the transfer of an electron. However, this is valid only at temperature of 0 K. At higher temperatures, the Coulomb blockade is observable when the mentioned change in energy is larger than the thermal energy. Therefore, at room temperature, a quantum dot must be in size of few nanometres at most [1].

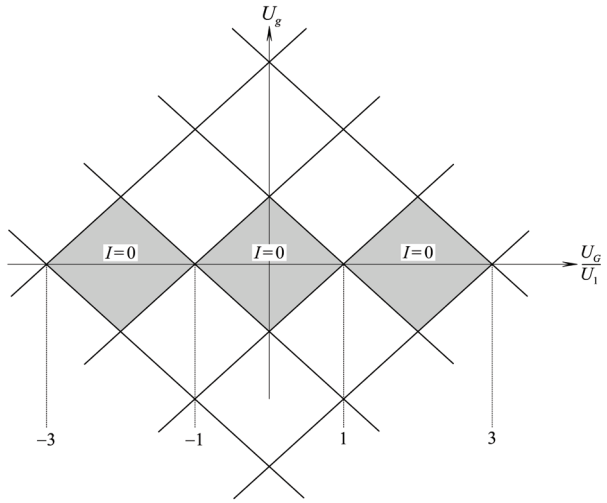


Figure 18: Stability diagram of single electron transistor. Shadowed areas depict the combinations of voltages, where tunnelling is not possible. U_g represents drain-to-source voltage, whereas U_G represents gate voltage. U_1 equals to $\frac{q}{2C_G}$, where q denotes elementary charge and C_G is the capacitance between gate electrode and quantum dot. When U_G equals to odd multiples of U_1, the Coulomb blockade does not exist [1].

Apart from the challenges, associated with manufacturing the quantum dots in so small dimensions, the effect of random background charge also represents a problem. Impurities with trapped charge in the insulating oxide can lead to logic errors in the single-electron logic circuits or their unreliable operation. What is more, the transfer characteristics of single-electron transistor have more peaks and thus more voltages where tunnelling can occur. Consequently, the potential single-electron logic circuits are going to be sensitive to noise and voltage drift [1]. However, the features of single-electron transistors make them usable in supersensitive electrometers, infrared radiation detectors and also memory devices [119].

5.6.3 Spintronics

Another field, which offers promising possibilities for advancement, especially in data storage technologies, is spintronics. That is a fairly new discipline, which deals with manipulation of the electron's spin in order to code, store, transfer and process the information. By using the spin of electron instead of its charge, many improvements could be made in the field of electronics [1]. One of the most promising applications of the principles of spintronics is magnetoresistive random access memory (MRAM), based on the magnetoresistance effect, where the resistance of material, in this case a ferromagnetic, is being changed in the presence of magnetic field [120]. The ability of movement of electrons in a ferromagnetic material depends on their spin orientation in relation to the material magnetisation. Electrons with spin orientation parallel to the magnetisation move unlimitedly, in contrary to the electrons with antiparallel spin orientation, who thus feel higher resistance [1]. Utilizing this property, a spin valve was designed, which served as a basis for the first storage element in MRAM. It consisted of two ferromagnetic layers with a non-magnetic conductive layer in between. One of the ferromagnetic layers had an antiferromagnetic layer in its proximity, which made it fairly insensitive to the applied magnetic field. This ferromagnetic layer was therefore called "pinned" or "fixed" layer, while the other one was "free", because its magnetisation could be changed. Therefore, a parallel or antiparallel magnetisation of layers could be achieved [120]. By parallel magnetisation, electrons with particular spin orientation felt low resistance in both layers, whereas the other ones felt high resistance

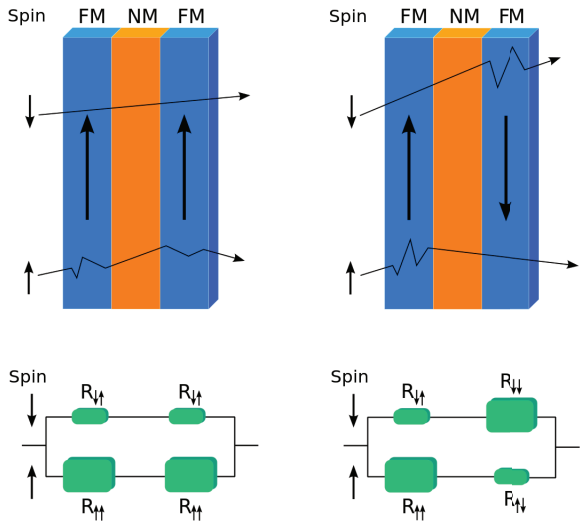


Figure 19: Resistive model of spin valve. Reprinted from [121]. Licensed under CC BY-SA 3.0 license.

in both layers. By antiparallel magnetisation, electrons of each spin orientation felt high resistance in one of the layers. With the current of both groups of electrons being independent of each other, the equivalent resistance was higher by antiparallel magnetisation, as depicted in Fig. 19. Hence, data could be stored by affecting the free layer magnetisation [1].

A big breakthrough was made in the late 1980s, when the spin valve based structures were discovered, whose resistance changed for up to 80% due to the applied magnetic field. This was called giant magnetoresistance (GMR) [1]. However, the practical GMR, which could be used in MRAM has remained too low to produce a sufficient voltage difference between the high and low resistance states [120]. As an improvement, the magnetic tunnel junction (MTJ) structures, using tunnel magnetoresistance (TMR), were developed. TMR structures are similar to GMR, except they have a very thin insulator film between the ferromagnetic layers instead of a non-magnetic layer. Therefore, the electrons can tunnel through the insulating film, where the probability of tunnelling is higher by parallel magnetisation, resulting in lower resistance. The values of the resistance change based on TMR have already achieved 100-200% in MRAM devices, which produces a significant voltage difference between logic states.

The basic principle of writing in MRAM is based on applying a magnetic field to appropriate cell, which switches the magnetisation in free layer. MRAM architecture consists of word and bit lines, which are orthogonal to each other (Fig. 20). The magnetic field is strong enough to alter the magnetisation in a data cell only when the current flows through both corresponding lines, which allows the addressing of each cell separately [1], [120].

However, at smaller cell dimensions, higher switching field and consequently higher current is necessary, which limits the scalability of field-assisted MRAM to about 90 nm. As a solution, spin transfer torque (STT) MRAM was introduced, where the switching of magnetisation was induced by a current, flowing through the device (Fig. 21). If the magnetisation needs to be switched from antiparallel to parallel, the electrons are sent from a pinned layer to free layer. In the pinned layer, the electrons with a spin in the opposite direction to magnetisation get scattered and the others pass to the free layer. There, the spin angular momentum exerts a torque on the magnetisation, resulting in its switching to parallel direction. In order to achieve switching from parallel to antiparallel magnetisation, the current must flow in the opposite direction. In this case, the electrons flow from the free to pinned layer. The electrons with spin orientation antiparallel to magnetisation get scattered back to the free layer, where they cause a switch to antiparallel magnetisation. STT MRAM allows scaling to smaller dimensions than MRAM with magnetic field-based writing [120].

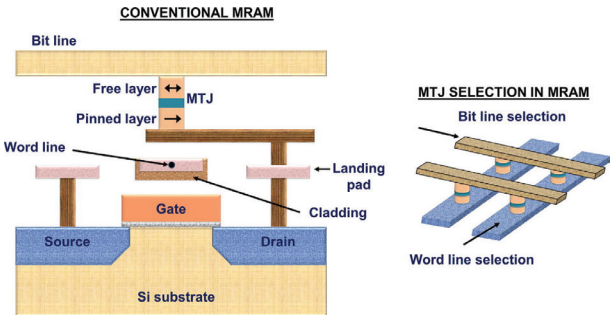


Figure 20: Schematic representation of conventional MRAM architecture, where magnetisation of free layer is set by applying sufficient magnetic field to the cell. To achieve that, current must flow through both corresponding word line and bit line. Reprinted from [120]. Licensed under CC BY-NC-ND 4.0 license.

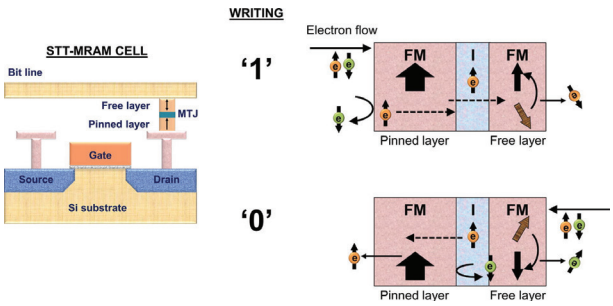


Figure 21: STT MRAM cell and its writing principle. Reprinted from [120]. Licensed under CC BY-NC-ND 4.0 license.

One of the main advantages of MRAM in general is its non-volatility, which is achieved by retentivity of ferromagnetic materials. Nevertheless, to achieve long lasting data retention, sufficient thermal stability of MTJ must be provided. By the in-plane MTJs, where the magnetisation of ferromagnetic layers is in the film plane (Fig. 22), this is hardly achievable for the cells with diameter less than 60 nm. Therefore, the MTJs with perpendicular magnetisation (pMTJ) are being increasingly researched [120]. Moreover, the critical switching current density, at which the magnetisation direction in free layer is rotated by the STT effect, can be considerably reduced, using pMTJ [122]. Thus, MRAMs with perpendicular magnetisation are considered to replace in-plane ones in the near future [120].

With all the mentioned attributes, STT MRAM is considered as a perfect candidate for future memory applications. However, the issue of a relatively high switching

current and consequently high energy consumption will have to be solved in order to launch MRAM successfully into the computer memory market [123].

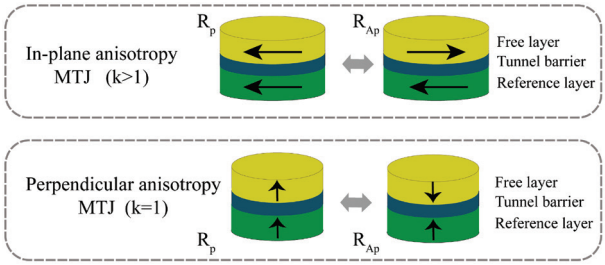


Figure 22: MTJ with in-plane and perpendicular magnetisation, where *k* represents width-to-length ratio of MTJ. By in-plane magnetisation, MTJs must have elliptical shape in order to prevent the formation of vortex magnetisation in the films, which is another downside of in-plane MTJs regarding scalability [120]. Reprinted with modification (cropping) from [124]. Licensed under CC BY 4.0 license.

5.6.4 Memristor

When talking about the potential future data storage solutions, it is appropriate to mention memristor. This is an element, which was theoretically described in the 1970s by Leon Chua and in its essence represents a relation between the electric charge and magnetic flux. Chua came to a conclusion that memristor therefore represents the fourth fundamental component of electrical circuits, alongside with the capacitor, resistor and inductor. The main property of memristor is that its resistance is being changed by the current, which flows through it. It is very important that this resistance retains its value after the current is shut down, which means that memristor can be used as a non-volatile memory device, whose high or low resistance represents one bit of information [1].

Physical realisation of memristor had not taken place until 2008, when the company Hewlett Packard (HP) introduced an element with allegedly memristive properties. It was made of a thin layer of titanium dioxide (TiO_2), embedded between two platinum (Pt) electrodes. A part of TiO_2 layer was oxygen deficient and therefore acted as an electrically conductive doped semiconductor due to the oxygen vacancies, which acted as dopants. The other part was not conductive. With external voltage applied, positively charged vacancies moved in the direction of electric field. When the vacancies drifted towards the opposite Pt electrode, the conductive channels were created at some point, switching the device on. When they drifted away, the channels were dispersed and the electronic barrier was recovered, switching the device off [125], [1]. Described memristive effects are highly dependent on the device's dimensions. They are remarkably more significant at the nanometre scale, which explains the fact that memristor was not physically realised before the immense progress in the field of nanotechnology [1]. The discussions are common, whether the mentioned realisation actually is a memristor, as described by Leon Chua, or it just exhibits some similar characteristics. Despite the fact that both the justification of memristor as the fourth fundamental electrical component and the actual realisation of theoretically proposed memristive properties are on shaky grounds, the memristor certainly represents a big promise in data storage, logic circuits and neural networks [1].

Several different types of memristive devices have been proposed so far, for example redox-based, ferroelectric, multiferroic and spin-based memristors [126]. In 2017, Samardžić et al. presented a multiferroic multilayer memristor, composed of $BaTiO_3/NiFe_2O_4/BaTiO_3$ thin films, deposited on platinised silicon wafers by spin-coating. Bottom electrode was therefore platinum, whereas the upper one was golden. The investigated memristor proved to have typical current-voltage characteristics in the form of pinched hysteresis loop, which was symmetric and repeatable for the voltage amplitudes of ±10 V. Two conducting mechanisms were identified. Fowler-Nordheim tunnelling for the applied voltages above 5 V and thermionic emission for lower voltages and higher temperatures [126]. In 2019, Lu et al. demonstrated purely electronic memristors, fabricated from amorphous silicon, doped with oxygen or nitrogen and embedded between metal electrodes. Such memristive devices could be easily integrated into conventional silicon technology, which is one of their main advantages [127]. Memristors have also found their way to biological computing. In 2020, Fu et al. presented a diffusive memristor, made of protein nanowires of the bacterium Geobacter sulfurreducens, functioning at low, biological voltages (40-100 mV) [128]. Diffusive memristors spontaneously relax back to non-conductive state, after the bias voltage for switching to conductive state is removed [129]. Hence, they enable emulations in short and long-term memory synapses, artificial neurons and neural networks [128], [129]. The artificial neuron, constructed with diffusive protein-nanowire memristors achieved similar temporal integration as biological neurons [128].

Various ways of memristors' utilisation have been introduced in the past few years. Memristor crossbar arrays with potential applications in non-volatile memory, logic circuits and neuromorphic computing systems have been proposed and realised [130]. Two nanometre feature size memristor crossbar arrays with a single-layer density comparable to information density achieved with state-of-the-art flash memory devices were re-

alised in 2018. Such structures represent a promising solution for power efficient information storage and processing [131]. Multi-bit memristive devices, which possess more than two distinctive resistance states, have also been proposed. In 2015, a microscale TiO_2 based memristor with silver and indium tin oxide electrodes was made and proved to have quantised conductance steps that were integer multiples of elementary conductance [132]. Two years later, memory cells with up to 6.5 bits information storage and long-lasting data retention have been developed [133]. Memristors with large number of conducting states could be very useful in artificial neural networks. Several researches have been made in this field. Graphene based non-volatile memristive synapses were introduced recently, with more than 16 arbitrarily programmable conductance states [134].

5.7 Funding of nanotechnology

Nanotechnology and nanoscience are becoming increasingly important driving forces for the modern world's development. It is estimated that governments worldwide invested over $67 billion in nanotechnology research between years 2000 and 2015. They also represent a significant part of European Union's (EU) research funding programmes. Under the Seventh Framework Programme (FP7), €2.56 billion was devoted for the projects in the fields of nanotechnology and nanoscience between years 2007 and 2011, mostly coming through the "Nanosciences, Nanotechnologies, Materials & new Production Technologies (NMP)" scheme [135]. Between 2014 and September of 2020, €56.4 billion was earmarked for the projects of Horizon 2020, EU research and innovation funding programme [136]. Under that programme, an estimated total budget of €1.77 billion was devoted only for the programme part "Nanotechnologies, Advanced Materials, Biotechnology and Advanced Manufacturing and Processing" between years 2018 and 2020 [137]. There are also other initiatives in the field of nanotechnology, funded under the same programme. One of them is Graphene Flagship with planned budget of €1 billion, which was initiated in 2013 and is still in progress [138]. The same budget is predicted for the Quantum Technologies Flagship initiative, which started in 2018 and supports quantum technologies research in Europe [139]. The funding of these initiatives will be continued by the programme Horizon Europe, which will span from 2021 to 2027 and have a budget of around €100 billion [140]. It is therefore reasonable to expect that the research in the fields of nanoscience and nanotechnologies is going to be increasingly funded by the EU in future.

5.8 A look to the future

With such financial support, we can expect an immense progress in these fields in next years. New solutions will have to be found in order to continue the development of the electronics' industry, according to the Moore's law. CNTFETs certainly have a potential to succeed the silicon based technology. However, the complete transition to CNTFETs is not likely to happen in the near future, due to the many manufacturing difficulties. We will more probably face gradual changes, in the form of incorporating CNTs as parts of the silicon based circuits, which could already happen in the present decade [114]. Nevertheless, the silicon transistors with nanosheets are yet to come into mass production in the next technology nodes, which implies that silicon will not be replaced very soon. In addition, it is more likely that it will be succeeded by more efficient, for example III-V semiconductors, before the CNTs play a significant role [27]. Most probably, the future electronic circuits will firstly be designed using combinations of mentioned materials.

Besides new materials and transistor types, different design and manufacturing principles could also contribute to the progress in the field of electronics. An interesting example is wafer-scale processing, where the whole silicon wafer is used for production of a single chip. This approach can be useful in designing high-performance computers, which execute computationally demanding tasks, like training deep artificial neural networks. A very large number of processor cores and memory units can therefore be integrated on a single chip, which significantly increases communication bandwidth and decreases processing times [141]. In 2019, a computer systems company Cerebras introduced a chip, measuring 46.255 mm^2, with more than 1.2 trillion transistors and 400,000 cores, using TSMC's 16 nm fabrication technology [142], [143]. In 2020, they announced a second generation of the chip, which comprised 850,000 artificial intelligence optimised cores and 2.6 trillion transistors, using TSMC's 7 nm technology [144].

Another field, which will importantly benefit from the progress of the nanotechnology is medicine. Promising methods are being developed for early diagnosing of different diseases, including certain types of cancer and diabetes, by detecting biomarkers in human breath [135], [145]. Furthermore, graphene quantum dots have shown the potential to treat the Parkinson's as well as Alzheimer's disease, which could change the life of millions of people in the future [146], [147], [148]. Targeted drug delivery with the use of nanoparticles is also a promising field, which will provide less invasive treatment, especially for cancer patients [135]. One of

the most perspective areas of nanotechnology in general, the self-assembly of structures, will also affect the field of medicine, in terms of self-repair mechanisms. Methods are being developed, where the nanostructured scaffolds are used to direct the growth of cardiac, bone and skin tissues [135].

Self-assembly will certainly represent a future revolution in many areas of technology. Assembling of molecules in particular structure without external intervention is an essential tool, which makes the bottom-up fabrication possible. It will enable the development of CNT based electronic devices and also be increasingly used in energy and environmental remediation applications. Low cost and highly efficient perovskite solar cells with self-assembled monolayers are already being developed, contributing to the progress of this perspective solar technology [149].

6 Conclusions

Considering all the above, it is clear that nanotechnology and nanoscience are going to affect our lives in the future. In this review paper, only positive effects of this field are presented. However, numerous questions are being set about the negative impacts of nanotechnology on health and also about its ethics. Although some hesitations may really be unjustified and only appear due to the fear of the unknown, which is a part of human nature, these questions will have to be addressed and resolved before the wider use. Nevertheless, despite the fact that this field of science is relatively new and the mankind's coexistence with it is still in its beginnings, it definitely has a bright future, possessing a great potential to improve our and our descendants' lives.

7 Conflict of interest

The authors declare no conflict of interest.

8 References

1. F. Smole, *Nanoelektronika*, 1. Ljubljana: Založba FE in FRI, 2014.
2. S. Bayda, M. Adeel, T. Tuccinardi, M. Cordani, and F. Rizzolio, "The history of nanoscience and nanotechnology: From chemical-physical applications to nanomedicine," *Molecules*, vol. 25, no. 1. MDPI AG, p. 112, 2019, https://doi.org/10.3390/molecules25010112.
3. "What's So Special about the Nanoscale? | nano.gov." https://www.nano.gov/nanotech-101/special (accessed Nov. 29, 2020).
4. "Nano Gold | 4cast web-tool | PHORNANO Holding GmbH." https://www.phornano.com/4ngold (accessed Nov. 29, 2020).
5. G. Binnig and H. Rohrer, "Scanning tunneling microscopy from birth to adolescence," *Rev. Mod. Phys.*, vol. 59, no. 3, pp. 615–625, 1987, https://doi.org/10.1103/RevModPhys.59.615.
6. "The Nobel Prize in Physics 1986." https://www.nobelprize.org/prizes/physics/1986/summary/ (accessed Nov. 29, 2020).
7. "The Nobel Prize in Physics 1956 - NobelPrize.org." https://www.nobelprize.org/prizes/physics/1956/summary/ (accessed Nov. 29, 2020).
8. "Nokia Bell-Labs Timeline." https://www.bell-labs.com/timeline/#/1940/1/open/ (accessed Dec. 22, 2020).
9. M. Riordan, "The lost history of the transistor," *IEEE Spectr.*, vol. 41, no. 5, pp. 44–49, 2003, https://doi.org/10.1109/MSPEC.2004.1296014.
10. J. S. C. Kilby, "Turning potential into realities: The invention of the integrated circuit (Nobel lecture)," *ChemPhysChem*, vol. 2, no. 8–9. Wiley-VCH Verlag, pp. 482–489, Aug. 17, 2001, https://doi.org/10.1002/1439-7641(20010917)2:8/9<482::aid-cphc482>3.0.co;2-y.
11. R. K. Basset, *To the Digital Age: Research Labs, Start-up Companies and the Rise of MOS Technology (Johns Hopkins Studies in the History of Technology)*. Baltimore: Johns Hopkins University Press, 2002.
12. S. L. Moskowitz, *Advanced Materials Innovation: Managing Global Technology in the 21st century*. John Wiley & Sons, 2016.
13. "File:Grown-junction NPN transistor type ST2010.png - Wikimedia Commons." https://commons.wikimedia.org/wiki/File:Grown-junction_NPN_transistor_type_ST2010.png (accessed Feb. 27, 2021).
14. "Nokia Bell-Labs Timeline." https://www.bell-labs.com/timeline/#/1950/1/open/ (accessed Feb. 27, 2021).
15. "Jack Kilby's Integrated Circuit | National Museum of American History." https://americanhistory.si.edu/collections/search/object/nmah_689592 (accessed Feb. 27, 2021).
16. "File:Fairchild uA741 opamp 6920.jpg - Wikimedia Commons." https://commons.wikimedia.org/wiki/File:Fairchild_uA741_opamp_6920.jpg (accessed Feb. 27, 2021).
17. "Intel A80386DX-20." https://www.cpu-world.com/CPUs/80386/Intel-A80386DX-20.html (accessed Feb. 27, 2021).
18. "File:Intel A80386DX-20 CPU Die Image.jpg - Wikimedia Commons." https://commons.wikimedia.

org/wiki/File:Intel_A80386DX-20_CPU_Die_Image.jpg (accessed Feb. 27, 2021).
19. G. E. Moore, "Cramming more components onto integrated circuits. In: Electronics," *Electronics*, 1965, [Online]. Available: https://www.cs.csub.edu/~melissa/cs350-f15/notes/Doc/gordon_moore_1965_article.pdf.
20. G. E. Moore, "Progress in digital integrated electronics," *Electron devices meeting*. 1975, [Online]. Available: http://ai.eecs.umich.edu/people/conway/VLSI/BackgroundContext/SMErpt/AppB.pdf.
21. B. Knehr, J. Lewis, and C. Morse, "Developmental History of main-line Intel CPUs," 2002. [Online]. Available: https://users.cs.jmu.edu/abzugcx/Public/Student-Produced-Term-Projects/Computer-Organization-2002-SPRING/Intel-CPUs-by-Clint-Morse-Jeff-Lewis-Brian-Knehr-2002-SPR.doc.
22. "International Technology Roadmap for Semiconductors - ITRS 2.0 Home Page." http://www.itrs2.net/ (accessed Nov. 29, 2020).
23. "The International Roadmap for Devices, International Roadmap for Devices and Systems; 2017 Edition; More Moore," 2018. Accessed: Nov. 29, 2020. [Online]. Available: https://irds.ieee.org/images/files/pdf/2017/2017IRDS_MM.pdf.
24. "The National Technology Roadmap for Semiconductors," 1994. Accessed: Nov. 29, 2020. [Online]. Available: http://www.rennes.supelec.fr/ren/perso/gtourneu/enseignement/roadmap94.pdf.
25. H. S. P. Wong *et al.*, "A Density Metric for Semiconductor Technology [Point of View]," *Proceedings of the IEEE*, vol. 108, no. 4. Institute of Electrical and Electronics Engineers Inc., pp. 478–482, Apr. 01, 2020, https://doi.org/10.1109/JPROC.2020.2981715.
26. "Process Technology History - Intel - WikiChip." https://en.wikichip.org/wiki/intel/process (accessed Nov. 29, 2020).
27. P. Ye, T. Ernst, and M. V. Khare, "The last silicon transistor: Nanosheet devices could be the final evolutionary step for Moore's Law," *IEEE Spectr.*, vol. 56, no. 8, pp. 30–35, Aug. 2019, https://doi.org/10.1109/MSPEC.2019.8784120.
28. "Samsung Electronics on Track for 10nm FinFET Process Technology Production Ramp-up – Samsung Global Newsroom." https://news.samsung.com/global/samsung-electronics-on-track-for-10nm-finfet-process-technology-production-ramp-up (accessed Dec. 22, 2020).
29. "File: Moore's Law Transistor Count 1971-2018.png - Wikimedia Commons." https://commons.wikimedia.org/wiki/File:Moore%27s_Law_Transistor_Count_1971-2018.png (accessed Dec. 27, 2020).
30. Y. Ding *et al.*, "A Device Design for 5 nm Logic FinFET Technology," *J. Microelectron. Manuf.*, vol. 3, no. 1, pp. 1–8, 2019, https://doi.org/10.33079/jomm.20030105.
31. A. Artashyan, "Samsung Electronics Has Already Begun Mass Production Of 5nm Chips." https://www.gizchina.com/2020/07/30/samsung-electronics-has-already-begun-mass-production-of-5nm-chips/ (accessed Nov. 29, 2020).
32. I. Cutress, "Samsung Announces 3nm GAA MBCFET PDK, Version 0.1." https://www.anandtech.com/show/14333/samsung-announces-3nm-gaa-mbcfet-pdk-version-01 (accessed Nov. 29, 2020).
33. "Samsung Electronics' Leadership in Advanced Foundry Technology Showcased with Latest Silicon Innovations and Ecosystem Platform – Samsung Global Newsroom." https://news.samsung.com/global/samsung-electronics-leadership-in-advanced-foundry-technology-showcased-with-latest-silicon-innovations-and-ecosystem-platform (accessed Dec. 22, 2020).
34. "Q2 2019 Taiwan Semiconductor Manufacturing Co Ltd EarningsCall (Edited transcript)." Thomson Reuters, Jul. , Accessed: Nov. 29, 2020. [Online]. Available: https://www.tsmc.com/uploadfile/ir/quarterly/2019/2NQYt/E/TSMC 2Q19 transcript.pdf.
35. N. Mojarad, J. Gobrecht, and Y. Ekinci, "Beyond EUV lithography: A comparative study of efficient photoresists' performance," *Sci. Rep.*, vol. 5, no. 1, pp. 1–7, Mar. 2015, https://doi.org/10.1038/srep09235.
36. A. A. Long, *The Cambridge Companion to Early Greek Philosophy (Cambridge Companions to Philosophy)*. Cambridge University Press, 1999.
37. B. Rogers, J. Adams, and S. Pennathur, *Nanotechnology: Understanding Small Systems, Third Edition*, 3rd ed. CRC Press, 2015.
38. "2.1: A History of Atomic Theory - Chemistry LibreTexts." https://chem.libretexts.org/Courses/Oregon_Institute_of_Technology/OIT%3A_CHE_201_-_General_Chemistry_I_(Anthony_and_Clark)/Unit_2%3A_The_Structure_of_the_Atom/2.1%3A_A_History_of_Atomic_Theory (accessed Feb. 23, 2021).
39. "The History of the Atom – Theories and Models – Compound Interest." https://www.compoundchem.com/2016/10/13/atomicmodels/ (accessed Feb. 23, 2021).
40. "File:Plum pudding model.svg - Wikimedia Commons." https://commons.wikimedia.org/wiki/File:Plum_pudding_model.svg (accessed Feb. 25, 2021).
41. "File:Rutherford atom.svg - Wikimedia Commons." https://commons.wikimedia.org/wiki/File:Rutherford_atom.svg (accessed Feb. 26, 2021).

42. "File:Bohr atom model.png - Wikimedia Commons." https://commons.wikimedia.org/wiki/File:Bohr_atom_model.png (accessed Feb. 26, 2021).
43. "Atom Model Schrödinger - Free image on Pixabay." https://pixabay.com/illustrations/atom-model-schrödinger-atomic-5000565/ (accessed Feb. 26, 2021).
44. "Atom - Bohr's shell model | Britannica." https://www.britannica.com/science/atom/Bohrs-shell-model (accessed Feb. 24, 2021).
45. T. W. Hansch, A. L. Schawlow, and G. W. Series, "The Spectrum of Atomic Hydrogen," *Sci. Am.*, vol. 240, no. 3, pp. 94–111, 1979, Accessed: Mar. 29, 2021. [Online]. Available: https://www.jstor.org/stable/24965154.
46. "Schrodinger equation | Explanation & Facts | Britannica." https://www.britannica.com/science/Schrodinger-equation (accessed Feb. 25, 2021).
47. "Wave function | Definition & Facts | Britannica." https://www.britannica.com/science/wave-function (accessed Feb. 25, 2021).
48. "The quantum mechanical model of the atom (article) | Khan Academy." https://www.khanacademy.org/science/physics/quantum-physics/quantum-numbers-and-orbitals/a/the-quantum-mechanical-model-of-the-atom (accessed Feb. 25, 2021).
49. "Atom - The laws of quantum mechanics | Britannica." https://www.britannica.com/science/atom/The-laws-of-quantum-mechanics (accessed Feb. 25, 2021).
50. "Development of the Atomic Theory." http://www.abcte.org/files/previews/chemistry/s1_p6.html (accessed Feb. 25, 2021).
51. "Frederick Soddy - Facts - NobelPrize.org." https://www.nobelprize.org/prizes/chemistry/1921/soddy/facts/ (accessed Feb. 25, 2021).
52. "Donor spin qubit in silicon | Fundamental Quantum Technologies Laboratory." https://www.fqt.unsw.edu.au/research/donor-spin-qubit-in-silicon (accessed Feb. 25, 2021).
53. J. J. Pla *et al.*, "A single-atom electron spin qubit in silicon," *Nature*, vol. 489, no. 7417, pp. 541–544, Sep. 2012, https://doi.org/10.1038/nature11449.
54. J. J. Pla *et al.*, "High-fidelity readout and control of a nuclear spin qubit in silicon," *Nature*, vol. 496, no. 7445, pp. 334–338, Apr. 2013, https://doi.org/10.1038/nature12011.
55. N. Taniguchi, "On the Basic concept of Nanotechnology," *Proceeding ICPE*, 1974.
56. G. Binnig, C. F. Quate, and C. Gerber, "Atomic force microscope," *Phys. Rev. Lett.*, vol. 56, no. 9, pp. 930–933, Mar. 1986, https://doi.org/10.1103/PhysRevLett.56.930.
57. D. M. Eigler and E. K. Schweizer, "Positioning single atoms with a scanning tunnelling microscope," *Nature*, vol. 344, no. 6266, pp. 524–526, Apr. 1990, https://doi.org/10.1038/344524a0.
58. H. W. Kroto, J. R. Heath, S. C. O'Brien, R. F. Curl, and R. E. Smalley, "C60: Buckminsterfullerene," *Nature*, vol. 318, pp. 162–163, 1985, https://doi.org/10.1038/318162a0.
59. S. Iijima, "Helical microtubules of graphitic carbon," *Nature*, vol. 354, pp. 56–58, 1991, https://doi.org/10.1038/354056a0.
60. "Carbon Nanotube stock illustration. Illustration of colour - 43175001." https://www.dreamstime.com/stock-illustration-carbon-nanotube-illustration-nanotechnology-scene-computer-artwork-image43175001 (accessed Dec. 22, 2020).
61. A. I. Ekimov, A. L. Efros, and A. A. Onushchenko, "Quantum size effect in semiconductor microcrystals," *Solid State Commun.*, vol. 56, no. 11, pp. 921–924, 1985, https://doi.org/10.1016/S0038-1098(85)80025-9.
62. S. Kailasa, K.-H. Cheng, and H.-F. Wu, "Semiconductor Nanomaterials-Based Fluorescence Spectroscopic and Matrix-Assisted Laser Desorption/Ionization (MALDI) Mass Spectrometric Approaches to Proteome Analysis," *Materials (Basel).*, vol. 6, no. 12, pp. 5763–5795, Dec. 2013, https://doi.org/10.3390/ma6125763.
63. C. Livache *et al.*, "A colloidal quantum dot infrared photodetector and its use for intraband detection," *Nat. Commun.*, vol. 10, 2019, https://doi.org/10.1038/s41467-019-10170-8.
64. Z. Liu *et al.*, "Micro-light-emitting diodes with quantum dots in display technology," *Light Sci. Appl.*, vol. 9, 2020, https://doi.org/10.1038/s41377-020-0268-1.
65. A. J. Nozik, "Quantum dot solar cells," in *Physica E: Low-Dimensional Systems and Nanostructures*, Apr. 2002, vol. 14, no. 1–2, pp. 115–120, https://doi.org/10.1016/S1386-9477(02)00374-0.
66. C. T. Kresge, J. C. Vartuli, W. J. Roth, and M. E. Leonowicz, "The discovery of ExxonMobil's M41S family of mesoporous molecular sieves," in *Studies in Surface Science and Catalysis*, Jan. 2004, vol. 148, pp. 53–72, https://doi.org/10.1016/s0167-2991(04)80193-9.
67. "Nanotechnology Timeline | nano.gov." https://www.nano.gov/timeline (accessed Nov. 29, 2020).
68. H. Lee and W. Ho, "Structural determination by single-molecule vibrational spectroscopy and microscopy: Contrast between copper and iron carbonyls," *Phys. Rev. B - Condens. Matter Mater. Phys.*, vol. 61, no. 24, pp. R16347–R16350, Jun. 2000, https://doi.org/10.1103/PhysRevB.61.R16347.
69. R. D. Piner, J. Zhu, F. Xu, S. Hong, and C. A. Mirkin, "'Dip-pen' nanolithography," *Science (80-.).*, vol.

283, no. 5402, pp. 661–663, Jan. 1999, https://doi.org/10.1126/science.283.5402.661.
70. L. R. Hirsch, J. B. Jackson, A. Lee, N. J. Halas, and J. L. West, "A whole blood immunoassay using gold nanoshells," *Anal. Chem.*, vol. 75, no. 10, pp. 2377–2381, May 2003, https://doi.org/10.1021/ac0262210.
71. R. D. Barish, P. W. K. Rothemund, and E. Winfree, "Two computational primitives for algorithmic self-assembly: Copying and counting," *Nano Lett.*, vol. 5, no. 12, pp. 2586–2592, Dec. 2005, https://doi.org/10.1021/nl052038l.
72. N. C. Seeman, "Nanomaterials Based on DNA," *Annu. Rev. Biochem.*, vol. 79, pp. 65–87, 2010, https://doi.org/10.1146/annurev-biochem-060308-102244
73. A. W. Knoll *et al.*, "Probe-based 3-D nanolithography using self-amplified depolymerization polymers," *Adv. Mater.*, vol. 22, no. 31, pp. 3361–3365, 2010, https://doi.org/10.1002/adma.200904386.
74. "IBM Creates Nano-sized 3D Map of Earth in Less Than 3 Minutes!" https://singularityhub.com/2010/04/28/ibm-creates-nano-sized-3d-map-of-earth-in-less-than-3-minutes-video/ (accessed Nov. 29, 2020).
75. "2014 National Nanotechnology Initiative Strategic Plan," 2014. Accessed: Nov. 29, 2020. [Online]. Available: www.whitehouse.gov/administration/eop/ostp/nstc.
76. "Progress Review on the Coordinated Implementation of the National Nanotechnology Initiative 2011, Environmental, Health and Safety Research Strategy," 2011. Accessed: Nov. 29, 2020. [Online]. Available: www.nano.gov.
77. "Nanoscience and nanotechnologies: opportunities and uncertainties," 2004. Accessed: Nov. 29, 2020. [Online]. Available: https://royalsociety.org/~/media/Royal_Society_Content/policy/publications/2004/9693.pdf.
78. "Towards a European Strategy for Nanotechnology," 2004. Accessed: Nov. 29, 2020. [Online]. Available: https://ec.europa.eu/research/industrial_technologies/pdf/policy/nano_com_en_new.pdf.
79. "Benefits and Applications | nano.gov." https://www.nano.gov/you/nanotechnology-benefits (accessed Nov. 29, 2020).
80. L. Van Langenhove, C. Hertleer, P. Westbroek, and J. Priniotakis, "Textile sensors for healthcare," in *Smart textiles for medicine and healthcare: Materials, systems and applications*, Elsevier Ltd, 2007, pp. 106–122. https://doi.org/10.1533/9781845692933.1.106
81. A. Hatamie *et al.*, "Review—Textile Based Chemical and Physical Sensors for Healthcare Monitoring," *J. Electrochem. Soc.*, vol. 167, no. 3, p. 037546, Jan. 2020, https://doi.org/10.1149/1945-7111/ab6827.
82. P. J. Lu, S. C. Huang, Y. P. Chen, L. C. Chiueh, and D. Y. C. Shih, "Analysis of titanium dioxide and zinc oxide nanoparticles in cosmetics," *J. Food Drug Anal.*, vol. 23, no. 3, pp. 587–594, Sep. 2015, https://doi.org/10.1016/j.jfda.2015.02.009.
83. C. S. Thaxton, D. G. Georganopoulou, and C. A. Mirkin, "Gold nanoparticle probes for the detection of nucleic acid targets," *Clinica Chimica Acta*, vol. 363, no. 1–2. Elsevier, pp. 120–126, Jan. 01, 2006, https://doi.org/10.1016/j.cccn.2005.05.042.
84. J. B. Vines, J. H. Yoon, N. E. Ryu, D. J. Lim, and H. Park, "Gold nanoparticles for photothermal cancer therapy," *Frontiers in Chemistry*, vol. 7, no. APR. Frontiers Media S.A., p. 167, 2019, https://doi.org/10.3389/fchem.2019.00167.
85. A. Meola, J. Rao, N. Chaudhary, M. Sharma, and S. D. Chang, "Gold nanoparticles for brain tumor imaging: A systematic review," *Frontiers in Neurology*, vol. 9, no. MAY. Frontiers Media S.A., May 14, 2018, https://doi.org/10.3389/fneur.2018.00328.
86. S. Bagheri *et al.*, "Using gold nanoparticles in diagnosis and treatment of melanoma cancer," *Artificial Cells, Nanomedicine and Biotechnology*, vol. 46, no. sup1. Taylor and Francis Ltd., pp. 462–471, Oct. 31, 2018, https://doi.org/10.1080/21691401.2018.1430585.
87. J. Chen, X. Zhang, R. Millican, J. E. Creutzmann, S. Martin, and H. W. Jun, "High density lipoprotein mimicking nanoparticles for atherosclerosis," *Nano Convergence*, vol. 7, no. 1. Korea Nano Technology Research Society, Dec. 01, 2020, https://doi.org/10.1186/s40580-019-0214-1.
88. F. U. Din *et al.*, "Effective use of nanocarriers as drug delivery systems for the treatment of selected tumors," *International Journal of Nanomedicine*, vol. 12. Dove Medical Press Ltd., pp. 7291–7309, Oct. 05, 2017, https://doi.org/10.2147/IJN.S146315.
89. M. Griffin, D. Kalaskar, A. Seifalian, and P. Butler, "An update on the Application of Nanotechnology in Bone Tissue Engineering," *Open Orthop. J.*, vol. 10, no. 1, pp. 836–848, Jan. 2017, https://doi.org/10.2174/1874325001610010836.
90. R. Medhi, P. Srinoi, N. Ngo, H. V. Tran, and T. R. Lee, "Nanoparticle-Based Strategies to Combat COVID-19," *ACS Applied Nano Materials*, vol. 3, no. 9. American Chemical Society, pp. 8557–8580, Sep. 25, 2020, https://doi.org/10.1021/acsanm.0c01978.
91. M. Hellfritzsch and R. Scherließ, "Mucosal vaccination via the respiratory tract," *Pharmaceutics*, vol. 11, no. 8. MDPI AG, Aug. 01, 2019, https://doi.org/10.3390/pharmaceutics11080375.

92. U. J. Etim, P. Bai, and Z. Yan, "Nanotechnology Applications in Petroleum Refining," in *Saleh T. (eds) Nanotechnology in Oil and Gas Industries. Topics in Mining, Metallurgy and Materials Engineering*, Springer, Cham, 2018, pp. 37–65. https://doi.org/10.1007/978-3-319-60630-9_2
93. H. Soukht Saraee, S. Jafarmadar, H. Taghavifar, and S. J. Ashrafi, "Reduction of emissions and fuel consumption in a compression ignition engine using nanoparticles," *Int. J. Environ. Sci. Technol.*, vol. 12, no. 7, pp. 2245–2252, Jul. 2015, https://doi.org/10.1007/s13762-015-0759-4.
94. F. Su, C. Lu, W. Cnen, H. Bai, and J. F. Hwang, "Capture of CO2 from flue gas via multiwalled carbon nanotubes," *Sci. Total Environ.*, vol. 407, no. 8, pp. 3017–3023, Apr. 2009, https://doi.org/10.1016/j.scitotenv.2009.01.007.
95. A. Lekawa-Raus, J. Patmore, L. Kurzepa, J. Bulmer, and K. Koziol, "Electrical properties of carbon nanotube based fibers and their future use in electrical wiring," *Adv. Funct. Mater.*, vol. 24, no. 24, pp. 3661–3682, Jun. 2014, https://doi.org/10.1002/adfm.201303716.
96. S. Boncel, A. Kolanowska, A. W. Kuziel, and I. Krzyżewska, "Carbon Nanotube Wind Turbine Blades: How Far Are We Today from Laboratory Tests to Industrial Implementation?," *ACS Appl. Nano Mater.*, vol. 1, no. 12, pp. 6542–6555, Dec. 2018, https://doi.org/10.1021/acsanm.8b01824.
97. M. Jošt, L. Kegelmann, L. Korte, and S. Albrecht, "Monolithic Perovskite Tandem Solar Cells: A Review of the Present Status and Advanced Characterization Methods Toward 30% Efficiency," *Advanced Energy Materials*, vol. 10, no. 26. Wiley-VCH Verlag, Jul. 01, 2020, https://doi.org/10.1002/aenm.201904102.
98. M. I. Nugraha *et al.*, "Low-Temperature-Processed Colloidal Quantum Dots as Building Blocks for Thermoelectrics," *Adv. Energy Mater.*, vol. 9, no. 13, p. 1803049, Apr. 2019, https://doi.org/10.1002/aenm.201803049.
99. M. Jošt *et al.*, "Textured interfaces in monolithic perovskite/silicon tandem solar cells: advanced light management for improved efficiency and energy yield," *Energy Environ. Sci*, vol. 11, p. 3511, 2018, https://doi.org/10.1039/c8ee02469c.
100. I. S. Yunus, Harwin, A. Kurniawan, D. Adityawarman, and A. Indarto, "Nanotechnologies in water and air pollution treatment," *Environ. Technol. Rev.*, vol. 1, no. 1, pp. 136–148, Nov. 2012, https://doi.org/10.1080/21622515.2012.733966.
101. M. Heiranian, A. B. Farimani, and N. R. Aluru, "Water desalination with a single-layer MoS 2 nanopore," *Nat. Commun.*, vol. 6, 2015, https://doi.org/10.1038/ncomms9616.
102. B. I. Kharisov, H. V. R. Dias, and O. V. Kharissova, "Nanotechnology-based remediation of petroleum impurities from water," *J. Pet. Sci. Eng.*, vol. 122, pp. 705–718, Aug. 2014, https://doi.org/10.1016/j.petrol.2014.09.013.
103. E. Akbari *et al.*, "Analytical calculation of sensing parameters on carbon nanotube based gas sensors," *Sensors (Switzerland)*, vol. 14, no. 3, pp. 5502–5515, Mar. 2014, https://doi.org/10.3390/s140305502.
104. M. Shafique and X. Luo, "Nanotechnology in transportation vehicles: An overview of its applications, environmental, health and safety concerns," *Materials*, vol. 12, no. 15. MDPI AG, Aug. 01, 2019, https://doi.org/10.3390/ma12152493.
105. S. E. O and D. B. Smith, "Potential Impact of Carbon Nanotube Reinforced Polymer Composite on Commercial Heavy Aircraft," 2004. Accessed: Nov. 29, 2020. [Online]. Available: https://apps.dtic.mil/sti/pdfs/AD1106874.pdf.
106. L. Mardare and L. Benea, "Development of Anticorrosive Polymer Nanocomposite Coating for Corrosion Protection in Marine Environment," in *IOP Conference Series: Materials Science and Engineering*, Jun. 2017, vol. 209, no. 1, p. 47, https://doi.org/10.1088/1757-899X/209/1/012056.
107. I. Ahmed, N. Ahmad, I. Mehmood, I. U. Haq, M. Hassan, and M. U. A. Khan, "Applications of Nanotechnology in Transportation Engineering," in *Advanced Research on Nanotechnology for Civil Engineering Applications*, IGI Global, 2016, pp. 180–207. https://doi.org/10.4018/978-1-5225-0344-6.ch006
108. W. Zhu, P. J. M. Bartos, and A. Porro, "Application of nanotechnology in construction," *Mater. Struct.*, vol. 37, no. 9, pp. 649–658, Nov. 2004, https://doi.org/10.1007/bf02483294.
109. A. Tabaković and E. Schlangen, "Self-healing technology for asphalt pavements," in *Advances in Polymer Science*, vol. 273, Springer New York LLC, 2016, pp. 285–306. https://doi.org/10.1007/12_2015_335
110. M. Barriera, S. Pouget, B. Lebental, and J. Van Rompu, "In situ pavement monitoring: A review," *Infrastructures*, vol. 5, no. 2. MDPI Multidisciplinary Digital Publishing Institute, 2020, https://doi.org/10.3390/infrastructures5020018.
111. "Infineon Unveils World`s Smallest Nanotube Transistor - Infineon Technologies." https://www.infineon.com/cms/en/about-infineon/press/market-news/2004/132191.html (accessed Dec. 22, 2020).

112. G. Hills *et al.*, "Modern microprocessor built from complementary carbon nanotube transistors," *Nature*, vol. 572, pp. 595–602, 2019, https://doi.org/10.1038/s41586-019-1493-8.
113. M. M. Shulaker *et al.*, "Carbon nanotube computer," *Nature*, vol. 501, no. 7468, pp. 526–530, Sep. 2013, https://doi.org/10.1038/nature12502.
114. E. Gibney, "Biggest carbon-nanotube chip yet says 'Hello, World!'" *Nature*, 2019, https://doi.org/10.1038/d41586-019-02576-7.
115. B. Gervasi, "Will Carbon Nanotube Memory Replace DRAM?," *IEEE Micro*, vol. 39, no. 2, pp. 45–51, 2019, https://doi.org/10.1109/MM.2019.2897560.
116. "Image Gallery - Nantero.com." http://nantero.com/newsroom/press-image-gallery/#lightbox/5/ (accessed Dec. 22, 2020).
117. M. Devoret and C. Glattli, "Single-electron transistors," *Phys. World*, vol. 11, no. 9, pp. 29–33, Sep. 1998, https://doi.org/10.1088/2058-7058/11/9/26.
118. "File:Set schematic.svg - Wikimedia Commons." https://commons.wikimedia.org/wiki/File:Set_schematic.svg (accessed Nov. 29, 2020).
119. O. Kumar and M. Kaur, "Single Electron Transistor: Applications & Problems," *Int. J. VLSI Des. Commun. Syst.*, vol. 1, no. 4, pp. 24–29, Dec. 2010, https://doi.org/10.5121/vlsic.2010.1403.
120. S. Bhatti, R. Sbiaa, A. Hirohata, H. Ohno, S. Fukami, and S. N. Piramanayagam, "Spintronics based random access memory: a review," *Materials Today*, vol. 20, no. 9. Elsevier B.V., pp. 530–548, Nov. 01, 2017, https://doi.org/10.1016/j.mattod.2017.07.007.
121. "File:Spin-valve GMR.svg - Wikimedia Commons." https://commons.wikimedia.org/wiki/File:Spin-valve_GMR.svg (accessed Nov. 29, 2020).
122. J. G. Webster, S. Z. Peng, Y. Zhang, M. X. Wang, Y. G. Zhang, and W. Zhao, "Magnetic Tunnel Junctions for Spintronics: Principles and Applications," in *Wiley Encyclopedia of Electrical and Electronics Engineering*, John Wiley & Sons, Inc., 2014, pp. 1–16. https://doi.org/10.1002/047134608X.W8231
123. V. Sverdlov, J. Weinbub, and S. Selberherr, "Spintronics as a Non-Volatile Complement to Modern Microelectronics," *Inf. MIDEM*, vol. 47, no. 4, pp. 195–210, 2017.
124. M. Wang, Y. Zhang, X. Zhao, and W. Zhao, "Tunnel Junction with Perpendicular Magnetic Anisotropy: Status and Challenges," *Micromachines*, vol. 6, no. 8, pp. 1023–1045, 2015, https://doi.org/10.3390/mi6081023.
125. J. J. Yang, M. D. Pickett, X. Li, D. A. A. Ohlberg, D. R. Stewart, and R. S. Williams, "Memristive switching mechanism for metal/oxide/metal nanodevices," *Nat. Nanotechnol.*, vol. 3, no. 7, pp. 429–433, 2008, https://doi.org/10.1038/nnano.2008.160.
126. N. Samardzic, B. Bajac, V. V Srdic, and G. M. Stojanovic, "Conduction Mechanisms in Multiferroic Multilayer BaTiO3/NiFe2O4/BaTiO3 Memristors," *J. Electron. Mater.*, vol. 46, no. 10, pp. 5492–5496, 2017, https://doi.org/10.1007/s11664-017-5618-2.
127. Y. Lu, A. Alvarez, C. H. Kao, J. S. Bow, S. Y. Chen, and I. W. Chen, "An electronic silicon-based memristor with a high switching uniformity," *Nat. Electron.*, vol. 2, no. 2, pp. 66–74, Feb. 2019, https://doi.org/10.1038/s41928-019-0204-7.
128. T. Fu *et al.*, "Bioinspired bio-voltage memristors," *Nat. Commun.*, vol. 11, no. 1, pp. 1–10, 2020, https://doi.org/10.1038/s41467-020-15759-y.
129. Z. Wang *et al.*, "Memristors with diffusive dynamics as synaptic emulators for neuromorphic computing," *Nat. Mater.*, vol. 16, no. 1, pp. 101–108, Jan. 2017, https://doi.org/10.1038/nmat4756.
130. L. Shi, G. Zheng, B. Tian, B. Dkhil, and C. Duan, "Research progress on solutions to the sneak path issue in memristor crossbar arrays," *Nanoscale Advances*, vol. 2, no. 5. Royal Society of Chemistry, pp. 1811–1827, May 01, 2020, https://doi.org/10.1039/d0na00100g.
131. S. Pi *et al.*, "Memristor crossbar arrays with 6-nm half-pitch and 2-nm critical dimension," *Nat. Nanotechnol.*, vol. 14, pp. 35–39, 2019, https://doi.org/10.1038/s41565-018-0302-0.
132. N. Samardžić, M. Mionić, B. Dakić, H. Hofmann, S. Dautović, and G. Stojanović, "Analysis of quantized electrical characteristics of microscale TiO2 ink-jet printed memristor," *IEEE Trans. Electron Devices*, vol. 62, no. 6, pp. 1898–1904, Jun. 2015, https://doi.org/10.1109/TED.2015.2421283.
133. S. Stathopoulos *et al.*, "Multibit memory operation of metal-oxide Bi-layer memristors," *Sci. Rep.*, vol. 7, 2017, https://doi.org/10.1038/s41598-017-17785-1.
134. T. F. Schranghamer, A. Oberoi, and S. Das, "Graphene memristive synapses for high precision neuromorphic computing," *Nat. Commun.*, vol. 11, 2020, https://doi.org/10.1038/s41467-020-19203-z.
135. "Nanotechnology: the invisible giant tackling Europe's future challenges." 2013, Accessed: Mar. 01, 2021. [Online]. Available: https://ec.europa.eu/research/industrial_technologies/pdf/nanotechnology_en.pdf.
136. M. Kadunc and N. Bruno, "Keeping our eyes on the Horizon; Monitoring flash series: a Horizon 2020 monitoring report," 2020. https://doi.org/10.2777/303024.

137. "Horizon 2020; Nanotechnologies, Advanced Materials, Biotechnology and Advanced Manufacturing and Processing; Work Programme 2018-2020," 2020. Accessed: Mar. 01, 2021. [Online]. Available: https://ec.europa.eu/research/participants/data/ref/h2020/wp/2018-2020/main/h2020-wp1820-leit-nmp_en.pdf.
138. "Graphene research, innovation and collaboration | Graphene Flagship." https://graphene-flagship.eu/ (accessed Mar. 01, 2021).
139. "Quantum Technology | The future is Quantum." https://qt.eu/ (accessed Mar. 01, 2021).
140. "EU budget: Commission proposes most ambitious Research and Innovation programme yet." 2018, [Online]. Available: https://ec.europa.eu/commission/presscorner/detail/en/IP_18_4041.
141. R. Schreiber, "Wafer-Scale Processors: The Time Has Come - Cerebras," 2019. https://cerebras.net/wafer-scale-processors-the-time-has-come/ (accessed Apr. 01, 2021).
142. B. Solca, "Cerebras breaks trillion transistor count with chip larger than an iPad - NotebookCheck.net News," 2019. https://www.notebookcheck.net/Cerebras-breaks-trillion-transistor-count-with-chip-larger-than-an-iPad.431193.0.html (accessed Apr. 01, 2021).
143. "Home - Cerebras." https://cerebras.net/ (accessed Apr. 01, 2021).
144. R. Thubron, "Cerebras reveals details of the world's largest chip: 2.6 trillion transistors, 850,000 cores | TechSpot," 2020. https://www.techspot.com/news/86427-cerebras-reveals-details-world-largest-chip-26-trillion.html (accessed Apr. 01, 2021).
145. N. Nasiri and C. Clarke, "Nanostructured Chemiresistive Gas Sensors for Medical Applications," *Sensors*, vol. 19, no. 3, p. 462, Jan. 2019, https://doi.org/10.3390/s19030462.
146. C. Wilson, "Quantum dots in brain could treat Parkinson's disease," *New Sci.*, no. 3186, 2018.
147. D. Kim *et al.*, "Graphene quantum dots prevent α-synucleinopathy in Parkinson's disease," *Nat. Nanotechnol.*, vol. 13, no. 9, pp. 812–818, Sep. 2018, https://doi.org/10.1038/s41565-018-0179-y.
148. Y. Liu, L. P. Xu, W. Dai, H. Dong, Y. Wen, and X. Zhang, "Graphene quantum dots for the inhibition of β amyloid aggregation," *Nanoscale*, vol. 7, no. 45, pp. 19060–19065, Dec. 2015, https://doi.org/10.1039/c5nr06282a.
149. A. Al-Ashouri *et al.*, "Conformal monolayer contacts with lossless interfaces for perovskite single junction and monolithic tandem solar cells," *Energy Environ. Sci.*, vol. 12, no. 11, pp. 3356–3369, Nov. 2019, https://doi.org/10.1039/c9ee02268f.

Arrived: 29. 12. 2020
Accepted: 07. 04. 2021

Original scientific paper
https://doi.org/10.33180/InfMIDEM2021.103

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 51, No. 1(2021), 49 – 61

Multi-Port Memory Design in Quantum Cellular Automata Using Logical Crossing

Kamaraj Arunachalam[1], Marichamy Perumalsamy[2], Abirami Ramasamy[1]

[1]Mepco Schlenk Engineering College, Department of ECE, Sivakasi
[2]P.S.R Engineering College, Department of ECE, Sivakasi.

Abstract: Memory and its data communication play a vital role in deciding the performance of a Processor. In order to obtain a high performance computing machine, memory access has to be equally faster. In this paper, Dual port memory with Set/Reset is designed using Majority Voter in Quantum-dot Cellular Automata (QCA). Dual port memory consists of basic functional blocks such as 2 to 4 decoder, Control Logic Block (CLB), Address Checker Block (ACB), Memory Cell (MC), Data Router block and Input/Output block. These functional units are constructed using the 3-input majority voters. QCA is one of the recent technologies for the design of nanometer level digital components. The functionality of Dual Port Memory has been simulated and verified in QCADesigner 2.0.3. A novel crossover method called Logical Crossing is utilized to improve the area of the proposed design. The logical crossing does the data transmission with the support of proper Clock zone assignment. The logical crossing based QCA layouts are optimized in terms of area and number of cell counts. It is observed that 29.81%, 18.27%, 8.32%, 11.57% and 3.69% are the percentage of improvement in the number of cells in Decoder, ACB, CLB, Data Router and Memory Cell respectively. Also, 25.71%, 16.83%, 8.62%, 4.74% and 3.73% of improvement is achieved in the area for Decoder, ACB, CLB, Data Router and Memory Cell respectively. In addition to that the proposed Dual port memory using logical crossing attains improvement in the area by 8.26%; that is made possible due to the 8.65% reduction in the number of cells required for its construction. Moreover, the quantum circuits of the RAM are obtained using the RCViewer+ tool. The quantum cost, constant inputs, the number of gates, garbage output and total cost are estimated as 285, 67, 57, 50 and 516 respectively.

Keywords: Dual Port memory; Logical Crossing; Number of Cells; Total Cost

Večvhodni spominski dizajn kvantnih celičnih avtomatov z uporabo logičnega križanja

Izvleček: Učinkovitost procesorja je odvisna od spomina in podatkovne komunikacije. Članek opisuje dvovhodni spomin s set/reset z uporabo večinskega volivca v kvantnem celičnem avtomatu (QCA). Dvovhodni spomin je sestavljen iz osnovnih funkcijskih blokov, kot so: 2-4 dekoder, controlni logični blok (CLB),blok preverjanja naslovov (ACB), spomiska celica (MC), podatkovni usmerjevalni blok in vhodno izhodni blok. Te funkcionalne enote s zgrajene z uporabo trovhodnih večinskih volilcev. Funkcionalnost je bila simulirana in preverjena v QCADesigner 2.0.3. Uporabljena je nova metoda logičnega križanja, ki opravlja prenos podatkov s podporo pravilne ure. Izboljšave v številu celic v dekoderju, ACB, CLB, usmerjevalniku in spomiski celici zanšajo 29.81%, 18.27%, 8.32%, 11.57% in 3.69% in izboljšavi v površini dekoderja, ACB, CLB, usmerjevalnika in spomiske celice v višini 25.71%, 16.83%, 8.62%, 4.74% in 3.73%. Skupna površina je manjša za 8.26%. Kvantna vezja RAM so narejena v RCViever+ orodju.

Ključne besede: dvovhodni spomin; logično križanje; število celic; strošek

** Corresponding Author's e-mail: kamarajvlsi@gmail.com*

1 Introduction

In a processor, the memory plays a critical role in deciding the performance of computation. The main characteristics of RAM are Reliability, Availability and Maintainability. The computation speed depends upon the design of memory architecture and the speed of communication. The communication speed indirectly depends on the architectural design of memory. The improvement in architectural design increases the performance of the system.

In CMOS (Complementary Metal Oxide Semiconductor), the memory architecture has nearly reached its saturation point. There comes a need for technological improvement at this moment, which can be achieved through the realization of digital structures in nanometer quantum cellular automata (QCA) [1]. QCA is a fast, ultra-low power and provides high packing density compared to other emerging nanotechnologies [1]. Further, the performance of the QCA can be enhanced by incorporating novel architectures. Generally, coplanar (single layer) and multilayer crossing is adopted in QCA wiring. However, usage of Multilayer architecture consumes less area and exhibits higher performance compared to coplanar wiring [2]. Logical Crossing is a new kind of wire crossing that exhibits a better performance than its predecessors. [3].

Two kinds of memory architectures can be realized in QCA. They are (1) line based and (2) loop based memory. In line-based memory, the four QCA clocking signals are used for storing the values in the cell; whereas the loop-based structure maintains the data using feedback in the circuit [1, 4]. The line-based method is very simple, but the reliability is questionable. While the loop-based method has better reliability and it is realized using multiplexer logic and latches [5].

The remaining parts of the paper are organized as follows; Section 2 explains the definitions of performance measures. Section 3 discusses the outcomes of the RAM related literature reviews. Section 4 deals with the novel logical crossing for interconnections in QCA. Section 5 elaborates on the proposed RAM design and its QCA realization. The simulation results obtained are discussed in Section 6. Finally, the paper is concluded with suggestions for future research.

2 Preliminaries performance metrics

2.1 Quantum Cost

The Quantum Cost of a circuit is defined as the total number of elementary quantum gates (primitive gates) that are needed to realize a given function [6]. The quantum cost of reversible preliminary gates such as Feynman, Toffoli and Fredkin gates are 1, 5 and 5 respectively [6].

2.2 Garbage Output

Garbage Output is defined as the number of unused outputs of the reversible circuit. Based on the requirement, these outputs are introduced to maintain the property of reversibility in the circuit [7].

2.3 Constant Input

Constant Input is a predefined input (Logic '0' or '1') in order to obtain the desired output function from the reversible gate. The input is kept constant at either '0' or '1' during the entire computation.

2.4 Logical Calculations

It is defined as the number of NOT (γ), AND (β) and XOR (α) operations that are required to obtain a desirable output function in reversible logic [8]. It indicates the hardware complexity of the circuit.

2.5 Number of Gates

It is the total number of gates required to realize the desired function. It is measured from the circuit's input to its output.

2.6 Total Cost

It is a sum of the Quantum Cost, Constant Input, Garbage output and Number of Gates.

2.7 QCA

Due to the increasing growth of electronic tools, parameters such as speed, area, processing power, energy consumption and density in the design of these tools are highly important [9]. In this regard, new technologies and designs are always being presented to resolve the disadvantages and make necessary improvements. One of the proposed technologies that try to advance in the digital electronics industry is quantum cellular automata (QCA) nanotechnology. This technology, which progresses constantly, has higher speed, density; also consumes far lower area and energy compared to the existing technologies [10].

In QCA technology, there can be two types of cells, which are 45°and 90°cells. A QCA cell contains four quantum dots that are located in the square corners. The electrons occupy the two corners of the QCA cell diagonally. A QCA wire can be designed simply by placing QCA cells next to each other. The length of the QCA wires should not be high since it leads to signal drop and can cause trouble in the circuit operation. Once the polarization of a QCA cell is fixed, the encoded binary information is transferred to the adjacent cells [11].

The three input majority gate and inverters are the basic structures of QCA circuits. Designing this gate is difficult in other technologies, but in this technology, the five QCA cells are arranged in a way to generate the majority gate. According to the structure and equation

of three input majority gate, it is observed that the AND and OR gates can be constructed based on two inputs by inserting a fixed value into one of the three input cells (logical one for OR and logical zero for AND) [12].

2.8 QCA Clocking

Every QCA based circuit requires a clocking mechanism for synchronization, flow control management, and provision of power to stimulate a circuit. This synchronization process is performed through QCA Clocking [13] as shown in Fig.1. The clocking of QCA can be accomplished by controlling the potential barriers between adjacent quantum dots.

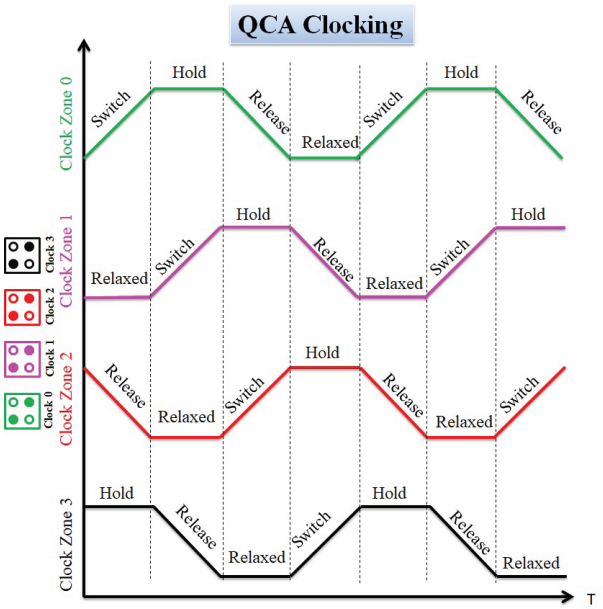


Figure 1: QCA Clocking (4 Clock Zones)

In QCA, the data flow path is based on the path along which the clocking phase increases [14]. It must be noticed that clocking phases should increase in turn unless the circuit does not function as expected. The control of data flow is one of the specific characteristics of QCA. This inherent characteristic helps designers in developing more optimized novel structures for digital circuits [15].

3 Related works in RAM

Timing of the clocking zones requires two additional clocks to implement a four step process for reading/writing data to the memory in line based parallel memory [16]. The parallel hybrid memory architecture reduces the area and latency. The area, number of interconnection and latency can be improved by proper QCA layout [17].

Various kinds of RAM architectures are presented and their performances are analyzed in terms of number of cells, area, number of clocks and cell delay as shown in Table 1. Then the best and worst-case performances are identified based on the latency and area of the presented layout design [5]. Set/Reset signals are introduced in the recent RAM cell designs. The inclusion of Set/Reset does not increase the number of gates [18], but the number of gates is reduced in [19] through optimum realization. The number of QCA cells increases when the RAM layout is realized using regular clock zones with Latches (D or SR), but it reduces the clock latency [20]. The number of QCA cells, area, the number of gates and latency of RAM are reduced with the usage of 3-input and 5-input majority gate [19] in the architecture. Also, the removal of coplanar wires (crossover) [20, 21] and the effective layout arrangement of QCA cells make it a robust and noise free design [18, 19].

Initially, single port RAM is designed using SR/D Latch with Loop-based concept in QCA. The performance is improved by incorporating the 5-input majority gate and efficient layout design. But, the present-day processors are expecting RAM with multiple ports and high capacity. So recently, a 4×4 RAM is designed with two ports using majority voters in QCA [22, 23]. The major objective of this RAM design is to avoid cross-

Table 1: Comparison of RAM Designs present in the Literatures

RAM Design	Crossover	No. of Ports	Latch	Basic Building Blocks	Set / Reset	Number of Gates	Number of Clock Cells	Area (μm^2)	Latency
1×4 [21]	Coplanar (Loop Based)	Single Port Memory Cell	D	3-input Majority Voter & not Gate	No	8 (6+2)	158	0.16	2
1×1 [20]			SR		No	8 (6+2)	144	0.18	1
			D			6 (5+1)	132	0.21	1
1×1 [18]	No Crossover		D FF		Yes	8 (6+2)	109	0.13	1.75
1×1 [19]			D	5-input Majority Voter	Yes	4	88	0.08	1.5
4×4 [22]		Dual Port Memory Cell	-	3-input Majority Voter	Yes	6	40	0.048	0.75
4×4 [23]	Multilayer		-		Yes	-	-	-	-

ings in the entire layout [22]. But, multilayer crossing is adopted in [23] to reduce the number of cells and area.

3.1 Limitations of the existing design

From the above analysis of the existing RAM designs, the following observations are made,

- Single port memory is designed with or without crossover in [19-21].
- No array type architecture is presented so far except in [22, 23].
- Coplanar and multilayer crossings are used in [20, 21 and 23].
- In order to overcome the limitations of the existing designs, a Multiport 4×4 RAM is proposed in this paper, which is being realized in the QCA layout using Logical Crossing.

4 Logical crossing

Two major wire crossing techniques are popularly used in QCA data transmission: coplanar and multilayer. Each of them has its own advantages and disadvantages as shown in Table 2 [3, 24].

In order to combine the advantages of both methods, a new wire crossing technique is introduced in [3] named Logical Crossing. In logical crossing, the data are transmitted to adjacent cells by operating them with clock signals shifted in phase by 180º clock phase. When two cells are in locked and locking stages, the Coulomb repulsion between them makes the data transmission possible. In other clock zones, the data transmission does not occur. The detailed clock zone information for data transfer in QCA is shown in Table 3.

Hence the cells in the hold and relax phase can cross each other without polarization effect. The diagrammatical view of data transmission in coplanar, multilayer and logical crossing are shown in Fig.2 and their corresponding QCA simulation waveforms are shown in Fig. 3. It is observed that the Logical Crossing uses Clock Zone 0 & 2 to pass Input A & B and Clock Zone 1 & 3 to transfer Input A & C to output.

The logical crossing method is used to construct XOR function [3], 2×1 multiplexer [25], Full Adder [26] and complex logical functions [24]. The incorporation of logical crossing in all these references reduces the number of cells and area in the QCA layout.

5 Proposed dual port RAM design

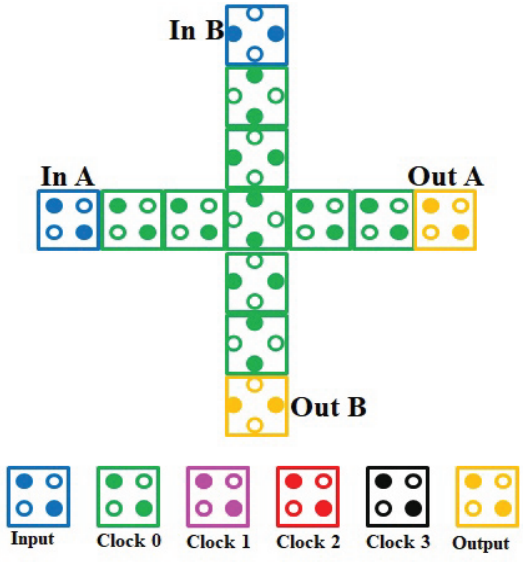
In dual port memory, a user can access two memory locations at a time. A data conflict may occur when two users access (among them at least one is write opera-

Table 2: Comparison of Wire Crossing Methods

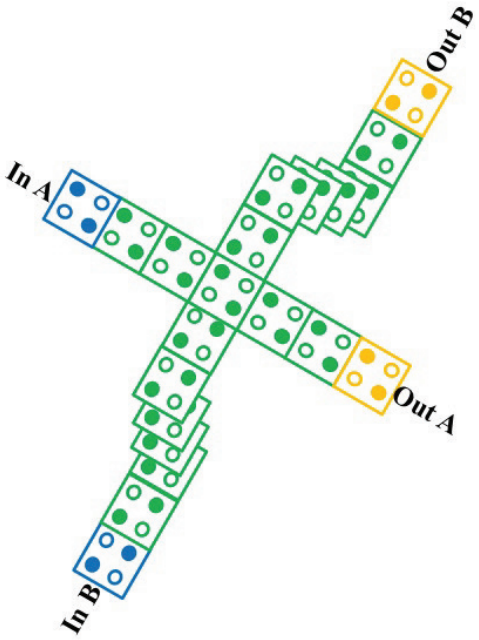
Wire crossing technique	Advantages	Disadvantages
Coplanar	1. Single Layer. 2. Lower number of cells. 3. No additional layers and cells. 4. No noise interference.	1. Need additional space between (45º deg.) cells. 2. Decreased energy separation between the ground state and the first excited state. 3. Performance decreases (high operating temperature, resistance to entropy and switching time).
Multilayer	1. No need to rotate the cells. 2. Good energy transformation. 3. Good performance (fast switching and high entropy).	1. Noise problem between intersection cells in the crossover area. 2. Number of layers, crossover and vertical cells are increased.

Table 3: Data Transfer in QCA

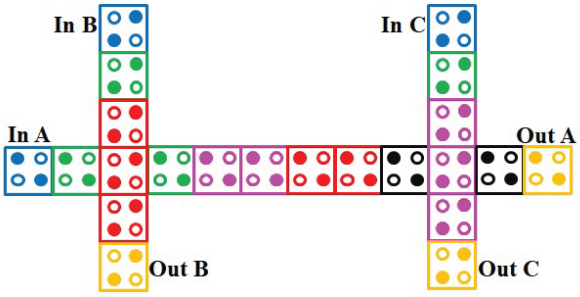
Clock Zones	State of Cells	Action & Data Transmission
Two adjacent clock cells (Clock Zone 1 & 3, Clock 2 & 4)	Locked and Locking stages pair.	Coulomb repulsion. Data transmission is performed within two cells.
Other Clock Zones Pairs	Locked and Relaxing stages.	Data transmission does not operate between two cells.
	Locking and Relaxed stages.	
	Locking and Relaxing Stages.	
	Locked and Relaxed stages pair.	Coulomb repulsion. Data transmission is not performed without any interference.



a. Coplanar Crossing



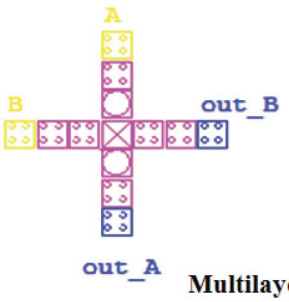
b. Multilayer Crossing

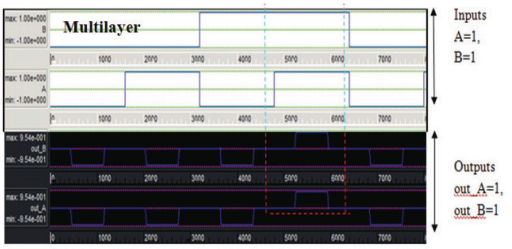


c. Logical Crossing

Figure 2: Wire Crossing Methods in QCA

a)





b)

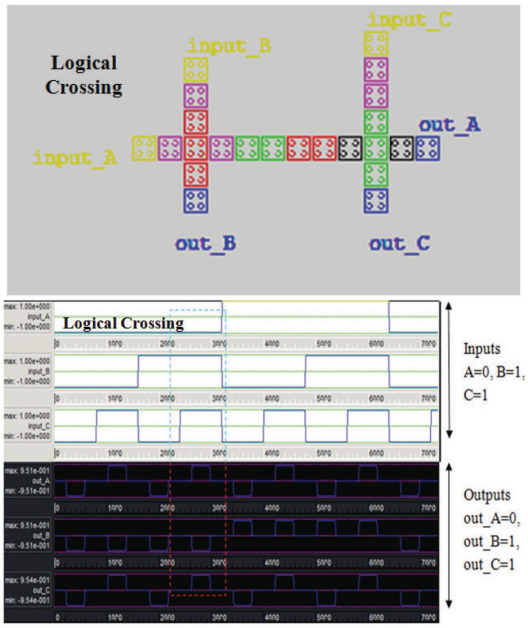


Figure 3: Simulation of Wire Crossing Methods in QCA, a) Multilayer Crossing and b) Logical Crossing.

tion) the same location at same time. The data conflicts can be avoided if one of the ports signal is stalled by delaying it. But this demands for additional buffers in QCA to introduce delay. So, to overcome this problem a priority-based dual port memory architecture is proposed. Fig.4. shows the proposed architecture..

Dual port memory architecture consists of decoder block, Address Checker Block (ACB), Control Logic Block (CLB), Data Router Block (DRB), Macro Memory Cell (MC) as shown in Fig. 5 (a to e). The decoder provides the address to the two ports (Port A and Port B). ACB checks the address of the two ports (i.e. to check whether the address of the two ports is the same). CLB

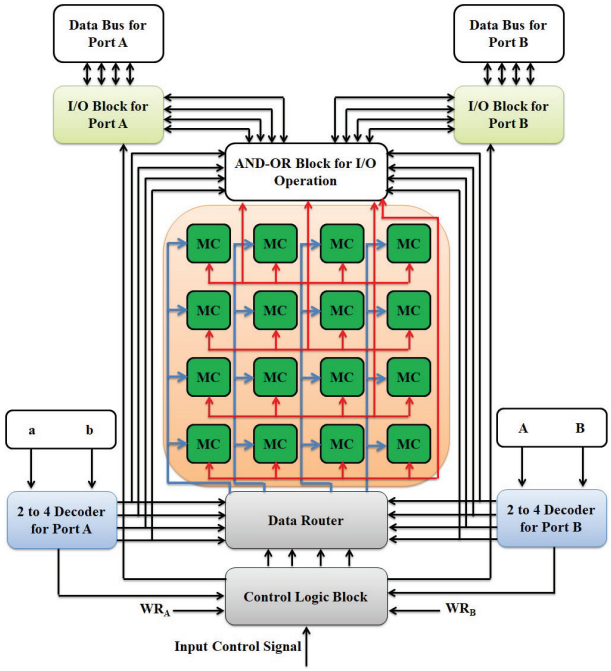


Figure 4: Block diagram of priority based Dual Port Memory.

generates the priority for the two ports, if Port A has higher priority, it accesses that memory cell first; followed by Port B. DRB provides the write/read operation (Data Route) to the two ports. Memory cell stores the single bit and it performs write/read operations.

5.1 Decoder

In dual port memory, two memory cells are selected at the same time for write/read operation. So, two decoders are used to generate the addresses for both the ports as shown in Fig.5a. The decoders are used to generate a 'row select' signal for addressing an appropriate memory array which is shown in Table 4.

Table 4: Truth Table of Decoder

A	B	A'B'	A'B	AB'	AB
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

5.2 Address Checker Block (ACB)

The addresses of the two decoders are compared to check whether they are similar or not. If the output of Address Checker Block (ACB) as shown in Fig.5b, X is '1' then addresses of the ports are same. Table 5 shows the operational output of ACB, where D_{iR} and D_{iL} represent the right and left decoder outputs respectively. If D_{0R} and

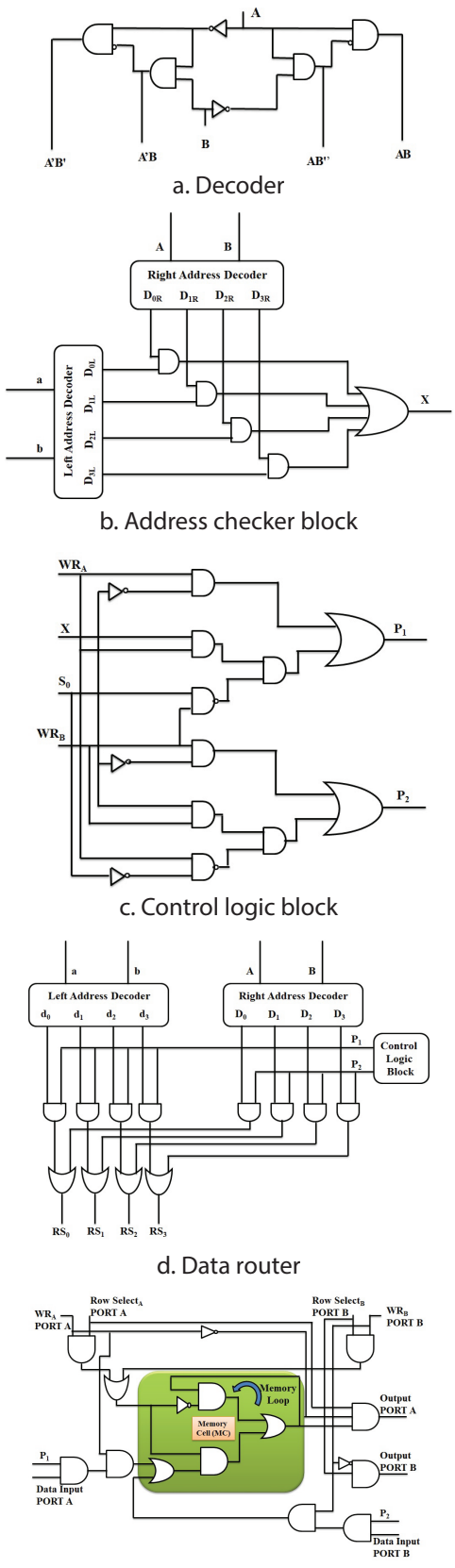


Figure 5: Block diagram of individual modules of Dual Port Memory a) Decoder b) Address Checker Block c) Control Logic Block d) Data Router and e) Memory cell.

D_{0L} have logic '1' the output is logic '1'. Similarly, all inputs logic is performed. The ACB works on a priority basis.

Table 5: Truth Table of ACB

D0R	D1R	D2R	D3R	D0L	D1L	D2L	D3L	X
1	X	X	X	1	X	X	X	1
X	1	X	X	X	1	X	X	1
X	X	1	X	X	X	1	X	1
X	X	X	1	X	X	X	1	1
0	0	0	0	0	0	0	0	0

5.3 Control Logic Block (CLB)

The control logic block (CLB) has inputs of Data Router signals of two ports and a control input. CLB produces the priorities as well as the Data Router for both ports. If the addresses are different, no conflict occurs at all. So, after the ACB block, if the addresses are unmatched, the control logic block simply passes the same Data Router data for both ports as supplied to the input lines of this block. For the same addresses, outputs will be chosen based on the control input (S_0) as per Table 6.

Table 6: Truth table for CLB priority calculation

Inputs						Outputs	
S0	Address Port A	Address Port B	WR_A	WR_B	X	P_1	P_2
0	01	01	0	0	1	0	0
0	01	01	0	1	1	0	1
0	01	01	1	0	1	1	0
0	01	01	1	1	1	1	1
1	10	10	0	0	1	0	0
1	10	10	0	1	1	0	1
1	10	10	1	0	1	1	0
1	10	10	1	1	1	1	1
0	10	11	0	0	0	0	0
0	10	11	0	1	0	0	1
0	10	11	1	0	0	1	0
0	10	11	1	1	0	1	1
1	10	11	0	0	0	0	0
1	10	11	0	1	0	0	1
1	10	11	1	0	0	1	0
1	10	11	1	1	0	1	1

If the addresses are same and X is logic '1', S_0 is the conflict resolver, WR_A and WR_B have logic '0' then the priority outputs P_1 and P_2 are logic '0'. The priority and the port for write/read A/B is selected based on the address port and WR signal. In order to remove the conflicts, the conflict resolve factor (0 or 1) is used. When the same memory location is selected for both ports with at least one operation is write operation, then the priority of the two ports must be different. These priorities also work as the final write/read signals as shown in the following equations 1 to 4.

B_1 and B_2 can be defined by the following functions.

$$B_1 = XWR_A\left(S_0WR_B\right)' \quad (1)$$

$$B_2 = XWR_B\left(S_0'WR_A\right)' \quad (2)$$

Therefore, conflict resolver functions as the write/read signals which satisfies all the following conditions (access of the same or different memory location),

$$P_1 = X'WR_A + XWR_A\left(S_0WR_B\right)' = X'WR_A + B_1 \quad (3)$$

$$P_2 = X'WR_B + XWR_B\left(S_0'WR_A\right)' = X'WR_B + B_2 \quad (4)$$

Where, P_1, P_2 are the priority of port A and port B respectively.

5.4 Data Router

Priority generated in the CLB is used as the Data Router for ports A & B. At any point of time, one row is selected for port A/port B, for the intended operation. Hence, the Data Router and the address lines have to be combined as shown in Fig.5d. In Table 7, d_i is the left address decoder while D_i is the right address decoder, P_i is Port A/B and RS_i is memory array i for write/read operation. If the same memory location is selected for both the ports, then the write/read signal of the prior port is selected. Output signals RS_1, RS_2, RS_3, and RS_4 are the Data Router signals for four rows.

5.5 Memory Cell

The memory architecture used in [27, 28] is modified according to dual port mode as shown in Fig. 5e. The

Table 7: Truth table for Data Router

a	b	d_3	d_2	d_1	d_0	A	B	D_3	D_2	D_1	D_0	P_1	P_2	RS_0	RS_1	RS_2	RS_3
0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	0	0	0
0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	1	0	0
1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	0	1	0
1	1	1	0	0	0	1	1	1	0	0	0	1	1	0	0	0	1

Table 8: Truth table of memory cell for Dual port memory

P_1	P_2	Data input		WR_A	RS_A	WR_B	RS_B	Output A	Output B
		Port A	Port B						
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	1	0	1	1	1
0	0	1	1	1	0	1	0	0	0
0	0	1	1	1	1	1	1	0	0
0	1	0	0	0	0	0	0	0	0
0	1	0	0	0	1	0	1	1	1
0	1	1	1	1	0	1	0	0	0
0	1	1	1	1	1	1	1	0	0
1	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	1	1	1
1	0	1	1	1	0	1	0	0	0
1	0	1	1	1	1	1	1	0	0
1	1	0	0	0	0	0	0	0	0
1	1	0	0	0	1	0	1	1	1
1	1	1	1	1	0	1	0	0	0
1	1	1	1	1	1	1	1	0	0

stored data are constantly updated inside the memory loop until both the write/read and row select wires of the same port are enabled. If the row select is enabled and the write/read is logic '0', then the current memory value inside the loop is forwarded to the output. The data input of the prior port is considered as the input line of the memory cell. In Table 8, WR_i and RS_i are the write and the read operation of Port A and B, respectively.

5.6 I/O Operation

There are individual data inputs for each port. The selected input port data are forwarded to the Memory cell or data are transferred to the output port based on the CLB control signals. The operation is performed using AND-OR combinational logic.

6 Results and discussions

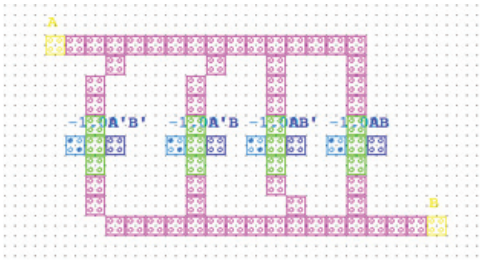
The above discussed dual port memory components are realized in quantum cellular automata (QCA) using logical crossing as shown in Fig.6 (a to e). It shows the QCA realization of Decoder, ACB, CLB, Data Router and Memory cell using Logical crossing based crossover. QCADesigner 2.0.3 [29] is used for this QCA layout design. The simulation waveforms of the individual modules of the RAM are shown in Fig.7. The simulation waveforms confirm the functional verification of the proposed RAM design. In Fig.7, the sample input and output simulation waveforms are shown, in which, for each module, one of the possible inputs and outputs is highlighted on the waveform and its logical value is represented on the right side.

Table 9: Comparison of Memory Cell implementation in QCA

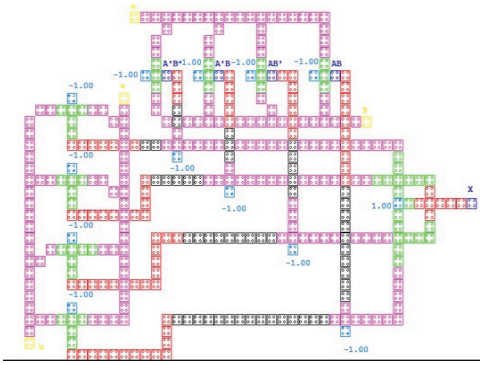
S. No.	Memory Cell References	Number of Cells
1.	[21]	158
2.	[20] with D Latch	132
3.	[18]	109
4.	[20] with SR Latch	100
5.	[19]	88
6.	Proposed	77

The QCA layout of individual modules of dual port RAM is realized using the logical crossing. The AND, OR and NOT are the basic logic units of the functional blocks of RAM. These logic units are constructed using 3-input majority voter and they are incorporated to build the decoder, ACB, CLB, Data Router and Memory cell. The interconnections between them are introduced by logical crossing, which has a positive impact on the performance measures.

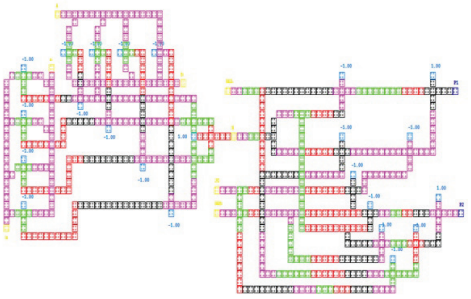
In [18-20], memory cell structure alone is implemented in QCA using multilayer/coplanar architecture. In [20], the inherent QCA capability is used to derive the Latch function. From Table 9, it is observed that the logical crossing in memory cell design reduces the required number of cells. When observing the logical crossing realization in Table 10, the inverter realization has 20%



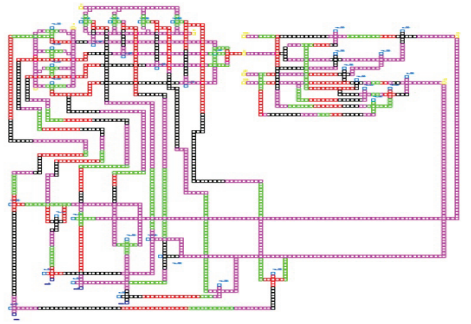
a. 2 to 4 Decoder



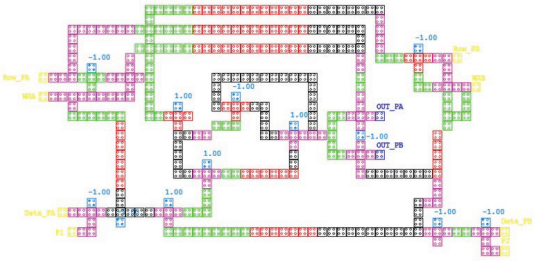
b. Address checker block



c. Control logic block



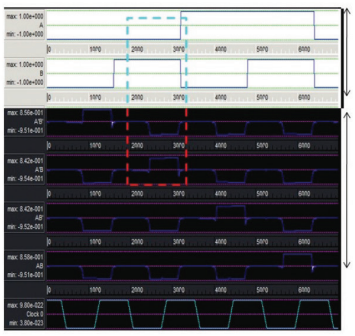
d. Data router



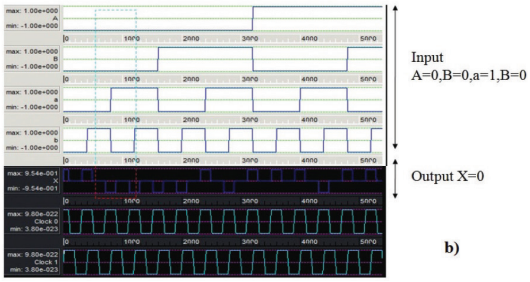
e. Memory Cell

Figure 6: QCA Realization of Dual port memory blocks

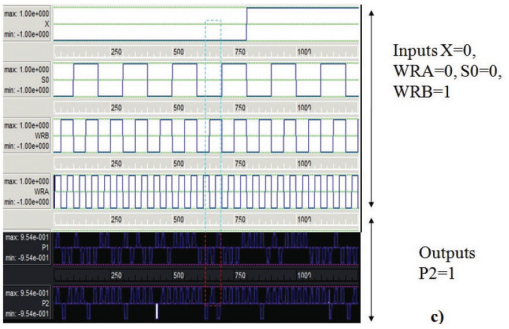
a)



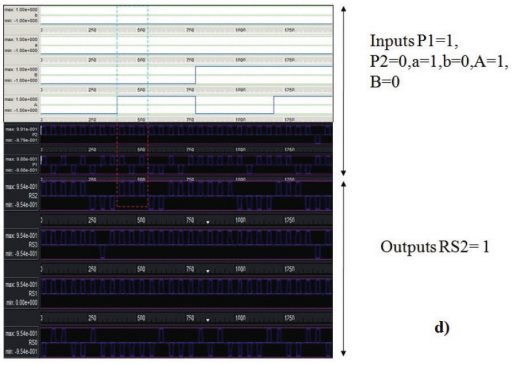
b)



c)



d)



e)

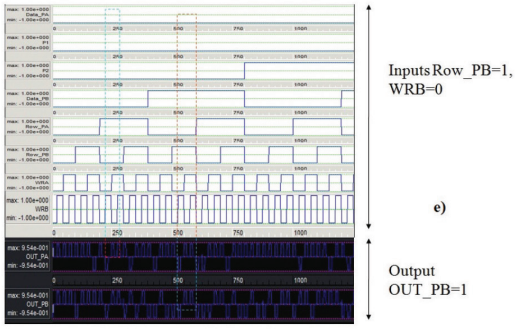


Figure 7: QCA Simulation of Dual Port RAM a) Decoder b) Address Checker Block and c) Control Logic Block d) Data Router and e) Memory cell.

Table 10: Comparison of Dual Port Memory

Components of RAM	Type and Number of functional units	Existing [22]			Proposed (Logical Crossing)			% of Improvement w.r.t. [22]		
		Number of Cells	Wires	Total	Number of Cells	Wires	Total	Number of Cells	Wires	Total
AND	-	5	0	5	5	0	5	0	0	0
OR	-	5	0	5	5	0	5	0	0	0
NOT		5	0	5	4	0	4	20	0	20
Decoder	4 AND, 2 NOT	30	74	104	28	45	73	6.67	39.19	29.81
ACB	2 Decoders, 4 AND, 1 OR	233	194	427	171	178	349	26.61	8.25	18.27
CLB	8 AND, 2 OR	477	328	805	421	317	738	11.74	3.35	8.32
Data Router Signal	2 Decoders, 1 CLB, 2 ACB, 8 AND, 2 OR	1917	530	2447	1676	488	2164	12.57	7.92	11.57
Memory Cell (MC)	3 NOT, 10 AND, 3 OR	80	300	380	77	290	367	3.75	3.33	3.42
4×4 MC	16 MC	1520	650	2170	1468	622	2090	3.42	4.31	3.69
Complete architecture	2 Decoders, Data Router, 4×4 MC, CLB, ACB	13620	11892	25512	12882	10423	23305	5.42	12.35	8.65

Table 11: Area comparison of Dual Port Memory

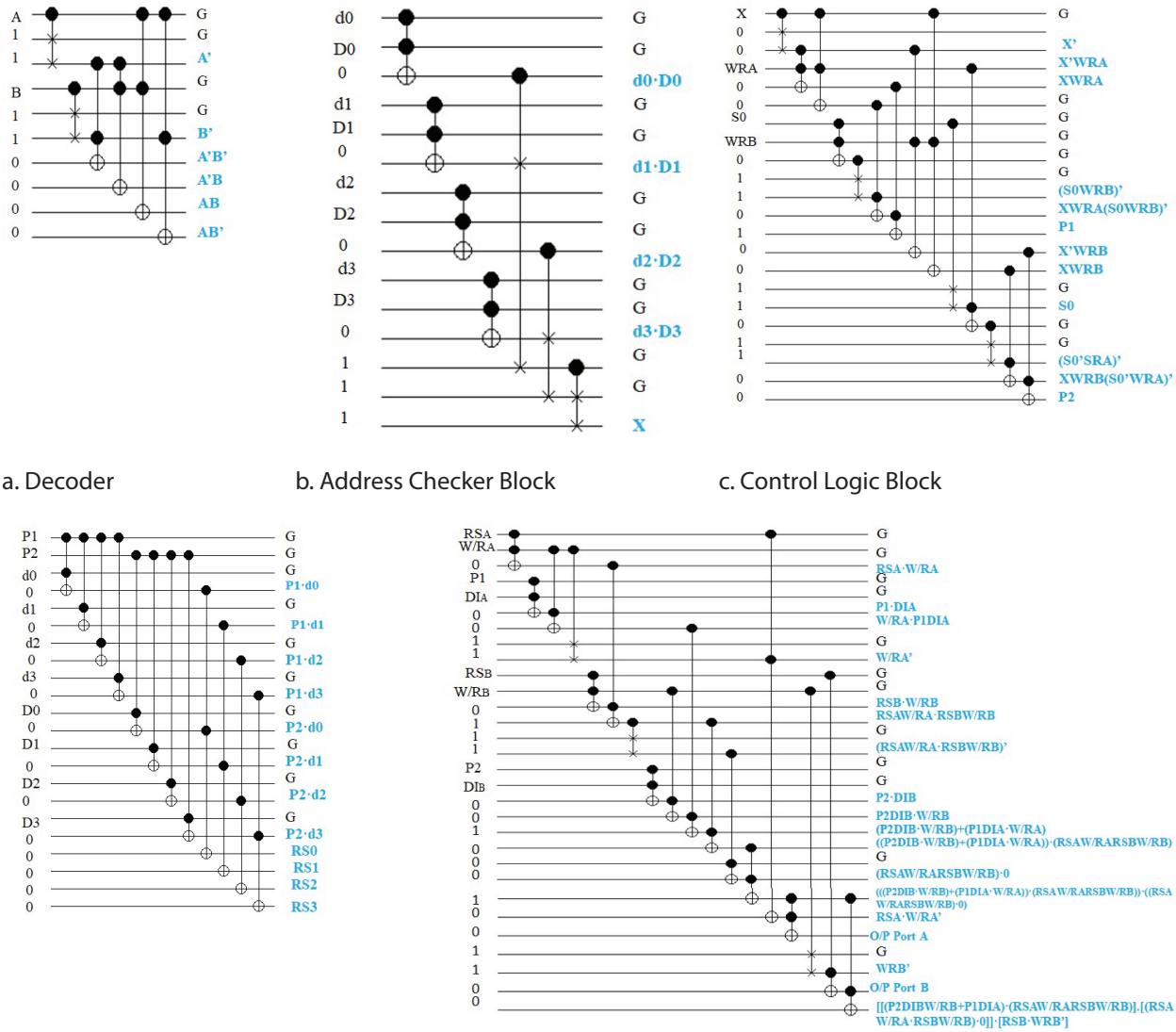
Modules of Dual Port Memory	Area occupied by		%of improvement w.r.t. [22]
	Existing layout [22]	Proposed (Logical crossing)	
2:4 Decoder	0.14	0.104	25.71%
Address checker block	1.01	0.84	16.83%
Control logic block	2.32	2.12	8.62%
Data Router	2.74	2.61	4.74%
Memory cell	0.51	0.491	3.73%
Total	6.72	6.165	8.26%

area reduction. In the decoder, the number of cells needed for providing interconnections is reduced by 39%. The decoder area is reduced by 29.81% compared to existing designs. The area reduction in the decoder

Table 12: Performance of Dual Port RAM

Modules of Dual Port Memory	Number of Primitive Gates		Quantum Cost	Constant Input	Number of Gates	Garbage Output	Logical Calculations	Total Cost
	Toffoli	Fredkin						
2:4 Decoder	4	2	30	8	6	4	$4\alpha+2\beta+4\gamma$	54
ACB	4	3	35	7	7	12	$4\alpha+3\beta+4\gamma$	68
CLB	10	4	70	18	14	12	$10\alpha+4\beta+10\gamma$	128
Data Router	12	-	60	12	12	10	$12\beta+12\gamma$	106
Memory cell	15	3	90	22	18	12	$10\alpha+4\beta+10\gamma$	160
Total	45	12	285	67	57	50	$28\alpha+27\beta+50\gamma$	516

Where α is XOR, β is AND, γ is NOT gate functions



a. Decoder b. Address Checker Block c. Control Logic Block

d. Data Router e. Memory Cell

Figure 8: Quantum Equivalent Circuit of Dual Port RAM

is mostly due to the results of the area reduction of the ACB (up to 18.27%). Similarly, the control logic block has an 8.32% smaller area due to logical crossing. The AND and OR gates are the only logical elements in CLB, where the area is not reduced with logical crossing. Hence, the area reduction was possible only in the interconnections for CLB. Data router is a combination of CLB and ACB (for which the area is already reduced). This has a positive effect on the construction of data router resulting in area reduction up to 11.27%. The number of cells required for wire connections in the proposed methodology has been reduced significantly.

The realization of memory cell leads to a small area reduction of 3.42%. The area occupied by the 4×4 memory array is reduced by 3.69%. The complete architecture of the RAM is obtained by combining all the individual modules, which results in a 12.35% area reduction compared to the existing designs due to the use of the logical crossing. Hence, the overall area reduction of 8.65% is achieved for RAM. Upon summarizing the obtained results, the functional units are integrated together to construct the 4×4 Dual Port RAM. In addition to that, it is observed from Table 11 that the reduction of number of cells in the RAM layout has been up to 8.26%.

The quantum circuit of the functional modules of RAM is obtained from Toffoli-Fredkin Code (.tfc) using RCViewer+ software [30]. In Fig.8, logic '1' and '0' denote the constant inputs and 'G' refers to garbage output. Here, Toffoli and Fredkin primitive gates are used to construct the RAM and their quantum cost is 5 [6]. The quantum cost of RAM is the sum of the quantum cost of the primitive gates used in the circuit. The quantum

cost, constant input, number of gates and garbage output are listed in Table 12.

From Table 12, the total cost of RAM is 516, which is the sum of quantum cost (285), number of constant inputs (67), number of gates (57) and number of garbage outputs (50). The number of logical calculations show the hardware complexity of the circuits.

7 Conclusion and future work

Quantum Cellular Automata is a low-power technology compared to present-day CMOS technology. In this paper, various functional blocks of Dual port memory such as 2 to 4 decoder, Control Logic Block (CLB), Address checker block (ACB), Data Router block and 4×4 memory cell block are designed using majority voters. The design unit consists of basic logic gates such as AND, OR, Inverter and connecting wires. All the functional modules are realized in the QCA layout with Logical Crossing. In Logical crossing method, the alternate clock signals are used to control the flow of data transmission rather than orientation and multiple layers for crossover. It has a positive impact on the cell count and reduces the area.

In comparison to the best published results from recent literature, it is worth mentioning that the number of cells is reduced by 29.81% (Decoder), 18.27% (ACB), 8.32% (CLB), 11.57% (Data Router) and 3.69% (Memory Cell) in the proposed work. Also, the area of the aforementioned blocks is reduced by 25.71%, 16.83%, 8.62%, 4.74% and 3.73%, respectively. In addition to that, the proposed logical crossing based complete Dual port memory achieves an improvement of 8.26% in area and 8.65% in number of cells. Moreover, the quantum cost, the number of constant inputs, the number of gates, the number of garbage output and the total cost are 285, 67, 57, 50 and 516 respectively. The work can be extended towards adding Asynchronous/Synchronous Set/Reset abilities to the dual port memory with increased memory array size.

8 Conflict of interest

The Authors of this Manuscript do not have any Conflict of Interest (COI) in publishing this paper.

9 References

1. Milad Bagherian Khosroshahy, Mohammad Hossein Moaiyeri, Keivan Navi and Nader Bagherzadeh, "An energy and cost efficient majority-based RAM cell in quantum-dot cellular automata", *Results in Physics*, Vol.7, pp.3543–3551, 2017, https://doi.org/10.1016/j.rinp.2017.08.067.
2. Weiqiang Liu, Maire O'Neill and Earl E. Swartzlander Jr, "Design of Semiconductor QCA Systems", *Artech House Publisher*, ISBN: ISBN-13: 978-1608076871, 2014.
3. Sang-Ho Shin, Jun-Cheol Jeon and Kee-Young Yoo, "Design of Wire-Crossing Technique Based on Difference of Cell State in Quantum-Dot Cellular Automata", *International Journal of Control and Automation*, Vol.7, No.4, pp.153-164, 2014, https://doi.org/10.14257/ijca.2014.7.4.14.
4. Marco Ottavi, Vamsi Vankamamidi, Fabrizio Lombardi and Salvatore Pontarelli, "Novel memory designs for QCA implementation", *Proceedings of 5th IEEE Conference on Nanotechnology*, pp. 1-4, 2005, https://doi.org/10.1109/nano.2005.1500822.
5. Javad Chaharlang and Mohammad Mosleh, "An Overview on RAM Memories in QCA Technology", Majlesi Journal of Electrical Engineering, Vol. 11, No. 2, pp.9-17, 2017, http://mjee.org/index/index.php/ee/article/view/2068.
6. Majid Mohammadi and Mohammad Eshghi, "On figures of merit in reversible and quantum logic designs", *Quantum Information Processing*, vol. 8, no.4, pp.297–318, 2009, https://link.springer.com/article/10.1007/s11128-009-0106-0.
7. Md. Mazder Rahman, Anindita Banerjee, Gerhard W. Dueck, and Anirban Pathak, "Quantum Gates to Reduce the Quantum Cost of Reversible Circuit", *41st IEEE International Symposium on Multiple-Valued Logic*, pp.86-92., 2011, https://doi.org/10.1109/ ISMVL.2011.56.
8. Xuemei Qi, Fulong Chen, Kaizhong Zuo, Liangmin Guo, Yonglong Luo, and Min Hu, "Design of fast fault tolerant reversible signed multiplier", *International Journal of the Physical Sciences,* vol. 7(17), pp. 2506 – 2514, 2012, https://doi.org/10.5897/ijps12.213.
9. K.Navi, A.Roohi and S.Sayedsalehi, "Designing reconfigurable Quantum-Dot Cellular Automata logic circuits", *Journal of Computer Theoretical Nanoscience,* pp. 1–10, 2013, https://doi.org/10.1166/jctn.2013.2819.
10. Reza Binaei and Mohammad Gholami, "Design of novel D flip-flops with set and reset abilities in quantum-dot cellular automata nanotechnology", *Computers and Electrical Engineering*, pp. 935-937, February 2019, https://doi.org/10.1016/j.compeleceng.2019.02.002.
11. C.S. Lent, P.D. Tougaw and W. Porod, "Quantum cellular automata: the physics of computing with arrays of quantum dot molecules", Proceedings Workshop on Physics and Computation. Phy-

sComp 94, pp. 5–13, 1994, https://doi.org/10.1109/phycmp.1994.363705.
12. J.Han, E.R.Boykin, H.Chen, J.Liang and J.A.B. Fortes, "On the reliability of computational structures using majority logic", *IEEE Transactions on Nanotechnology*, vol.10, no.5, pp. 99–112, 2011, https://doi.org/10.1109/tnano.2011.2111460.
13. M. Ottavi, S. Pontarelli, V. Vankamamidi, A. Salsano and F. Lombardi, "QCA memory with parallel read/serial write: design and analysis", *IEEE Proceedings - Circuits Devices and Systems*, pp. 292-294, July 2006, https://doi.org/10.1049/ip-cds:20050094.
14. B.Taskin, Bo Hong, "Dual-Phase Line-Based QCA Memory Design", *Sixth IEEE Conference on Nanotechnology*, 2006, https://doi.org/10.1109/nano.2006.247635.
15. V. Vankamamidi, M. Ottavi and F. Lombardi, "Two-dimensional schemes for clocking/timing of QCA circuits", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 27, no.1, pp. 34–43, 2008, https://doi.org/10.1109/tcad.2007.907020.
16. Vamsi Vankamamidi, Marco Ottavi, and Fabrizio Lombardi, "A Line-Based Parallel Memory for QCA Implementation", *IEEE Transactions on Nanotechnology*, vol.4, pp. 6, November 2005, https://doi.org/10.1109/tnano.2005.858589.
17. M. Ottavi, S. Pontarelli, V. Vankamamidi, A. Salsano and F. Lombardi, "QCA memory with parallel read/serial write: design and analysis", *IEEE Proceedings - Circuits Devices and Systems*, pp. 292-294, July 2006, https://doi.org/10.1049/ip-cds:20050094.
18. S. Hashemi and K. Navi, "New robust QCA D flip flop and memory structures", *Microelectronics Journal,* Vol. 43, pp. 929–940 (Elsevier), 2012, https://doi.org/10.1016/j.mejo.2012.10.007.
19. Shaahin Angizi, Soheil Sarmadi, SamiraSayedsalehi and Keivan Navi, "Design and evaluation of new majority gate-based RAM cell in quantum-dot cellular automata", *Microelectronics Journal*, Vol. 46, pp. 43–51, 2015. https://doi.org/10.1016/j.mejo.2014.10.003.
20. M.A. Dehkordi, A. Shahini Shamsabadi, B. Shahgholi Ghahfarokhi and A. Vafaei, "Novel RAM cell designs based on inherent capabilities of quantum-dot cellular automata", *Microelectronics Journal*, Vol. 42, pp. 701–708, 2011, https://dl.acm.org/doi/10.1016/j.mejo.2011.02.006.
21. K. Walus, A. Vetteth, G. A. Jullien and V.S. Dimitrov, "RAM design using quantum- dot cellular automata", *Technical Proceedings of the Nanotechnology Conference and Trade Show*, Vol.2, pp. 160–163, 2003, https://pdfs.semanticscholar.org/55af/927bbe5bab620efc1d56e8ce895aed520c61.pdf.
22. Kunal Das, Arindam Sadhu, Debashis De and Jadav Chandra Das, "Design and simulation of priority based dual port memory in quantum dot cellular automata", *Microprocessors and Microsystems*, Vol.69, pp.118–137, 2019, https://doi.org/10.1016/j.micpro.2019.06.004.
23. A. Chandrasekaran, K. Senthil Kumar, N. Vishnu kumar mani, S. Tilak Raaj and K. Suryaprakash, "Efficient Design of Control Logic Block in Dual Port Memory", *International Journal of Recent Technology and Engineering*, Vol.8, No.6, 2020, https://doi.org/10.1016/j.micpro.2019.06.004.
24. Shaahin Angizi, Esam Alkaldy, Nader Bagherzadeh and Keivan Navi, "Novel Robust Single Layer Wire Crossing Approach for Exclusive OR Sum of Products Logic Design with Quantum-Dot Cellular Automata", *Journal of Low Power Electronics*, Vol. 10, pp.259–271, 2014, https://doi.org/10.1166/jolpe.2014.1320.
25. Shadi Sheikhfaal, "A QCA Layout Design Methodology Part I", 2018, arXiv:1801.09807.
26. Md. Abdullah-Al-Shafi and Ali Newaz Bahar, "An Architecture of 2-Dimensional 4-Dot 2-Electron QCA Full Adder and Subtractor with Energy Dissipation Study", *Active and Passive Electronic Components, Hindawi*, pp.1-10, 2018. https://doi.org/10.1155/2018/5062960.
27. A.Kamaraj, P.Marichamy, J.Senthil Kumar, S.Selva Nidhyananthan and C.Kalyana Sundaram, "Design of Space-Efficient Nano Router in Reversible Logic with Multilayer Architecture", *Design and Testing of Reversible Logic, Springer,* pp. 233-250, 2019, https://doi.org/10.1007/978-981-13-8821-7_13.
28. A.Kamaraj and P.Marichamy, "Area Optimized Nano-Metric Level Dual Port Memory Design In QCA", *Journal of Adv Research in Dynamical & Control Systems*, Vol. 11, No.07, 2019, https://www.jardcs.org/abstract.php?id=2997. https://waluslab.ece.ubc.ca/qcadesigner/ http://webhome.cs.uvic.ca/~dmaslov/.

Arrived: 06. 04. 2020
Accepted: 29. 01. 2021

Original scientific paper
https://doi.org/10.33180/InfMIDEM2021.104

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 51, No. 1(2021), 63 – 71

A Low-Voltage Current Mirror for Transconductance Amplifiers

Hamdi Ercan[1], Sezai Alper Tekin[2]

[1]Erciyes University, Department of Avionics, Kayseri, Turkey
[2]Erciyes University, Department of Industrial Design Engineering, Kayseri, Turkey

Abstract: In this study, a low-voltage current mirror to use in differential pairs as an active load is introduced. The proposed current mirror which can operate at ±0.5 V has high output impedance and low input impedance. The proposed structure employs the principle of voltage level-shifting for PMOS transistors. The voltage level-shifting operation has been achieved by using the bulk voltage at this structure. Spice simulations also justify this current mirror's outstanding performance with a bandwidth of 11 GHz using an external capacitor at an input current of 200 µA.

Keywords: PMOS level shifter; low-voltage; current mirror; current-mode; differential pair; bulk voltage

Nizkonapetostno tokovno zrcalo za transkonduktančne ojačevalnike

Izvleček: Članek predstavlja nizkonapetostno zrcalo za uporabo kot aktivno breme v diferencialnih parih. Predlagano zrcalo obratuje pri napetosti ±0.5 V in ima visoko vhodno nizko izhodno impedanco. Struktura uporablja princip premikanja napetostnega nivoja pri PMOS tranzistorjih. Odlična učinkovitost je bila pokazana tudi s SPICE simulacijami pri pasovni širini 11 GHz, z uporabo zunanjega kondenzatorja pri vhodnem toku 200 µA.

Ključne besede: PMOS premikanja nivoja; nizka napetost; tokovno zrcalo; tokovni način; diferencialen par

** Corresponding Author's e-mail: hamdiercan@erciyes.edu.tr;*

1 Introduction

Nowadays, integrated circuit design has concentrated on a circuit with low-voltage operation, low-power dissipation, wide bandwidth and minimum area requirements. A growing need has emerged associated with low-voltage analog circuit design. The demand for circuits operating at low voltage has increased due to the need for low power dissipation. The low-voltage and low-power designs have increased operation time between the battery recharging cycle and have utilized a smaller or lighter-weight battery. Numerous low voltage applications have been proposed earlier [1,2]. Considering several technologies such as bipolar junction transistor (BJT), metal-oxide-semiconductor (MOS) and bipolar complementary MOS (BiCMOS), the CMOS technology has played a crucial role in the development of low power circuit for diverse applications.

The current mirror has been known as a circuit having two terminals whose output current is independent of the output voltage and depends only on the input current. These circuits copying the current carry out a significant function for active elements such as Op-Amp, OTA, current conveyor etc. The low-voltage current mirror has been used in a lot of active elements designed with low-power. The performance parameters of current mirrors like active elements parameters contain linearity, power dissipation, minimum supply voltage requirement, input and output resistance in these applications. At the same time, many active elements include differential pairs designed using PMOS current mirror as an active load [3-6]. The low-voltage operation of the active elements has been restricted because these current mirrors have high input voltage. A low voltage level shifter-based current mirror has been presented in Ref. [7] for current sensor application. Ac-

cording to this study, the bandwidth of the circuit was a few tens of MHz. Though this current mirror can be used in low voltage design, the level shifter approach has been designed using only the NMOS current mirror. The threshold voltage of the PMOS transistor is always higher than that of the NMOS. Thus, the circuit presented in Ref. [7] cannot be obtained using a PMOS transistor. However, this case has been resolved by using the proposed circuit.

In the present study, a low-voltage PMOS current mirror employing voltage level-shifting principle has been introduced. The voltage level-shifting operation has been achieved by using bulk voltage in this structure. The circuit utilizes a voltage level shifter at the input port to achieve the high input voltage swing capability. Thus, it can operate with low power supply voltage and low input /low output voltage requirements. Additionally, the proposed structure as an active load has been used in the transconductance amplifier.

2 Conventional PMOS current mirror

A conventional PMOS current mirror (CM) circuit is shown in Figure 1. Transistor M_1 has been used as a diode and the input current copied to output has been compelled to pump by the input voltage.

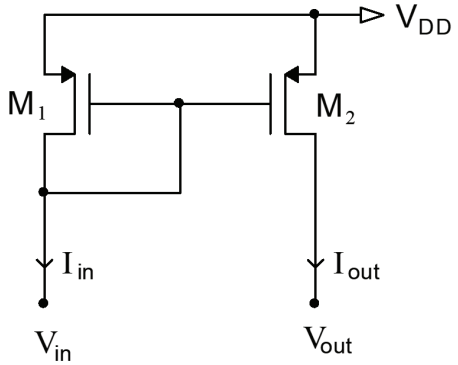


Figure 1: A conventional PMOS current mirror.

Transistor M_1 shown in Figure 1, operates in saturation mode. Besides, the input impedance of the CM depends on the transconductance (g_m) of the M_1. The input voltage of the circuit can be written as below:

$$V_{in} = V_{DD} - \sqrt{\frac{2I_{in}}{k_p\left(\frac{W_1}{L_1}\right)}} - V_{THP} \tag{1}$$

where $k_p = \mu_p C_{ox}$ is the conduction factor, V_{THP} is the threshold voltage for PMOS transistor, V_{DD} represents the supply voltage. Also, W and L are the effective transistor width and length. The output voltage requirement of the CM can be given as

$$V_{out,max} \approx V_{DD} - V_{DS2,sat} \tag{2}$$

where $V_{DS,sat}$ is drain-to-source voltage for relevant transistors in the saturation region. One of the drawbacks of the conventional PMOS CM is that input voltage is always greater than the threshold voltage, being a crucial parameter for low-voltage application. The other disadvantage is the low output impedance. Therefore, using this structure is inconvenient in the low voltage. By using the proposed approach, these challenges have been met.

3 PMOS level-shifter current mirror

Figure 2 indicates the PMOS level-shifted current mirror (PMOS LSCM) circuit for low-voltage applications [8]. Transistors M_1 and M_2 are operated in the saturated region ($V_{SD} > V_{SG} - V_{THP}$) in this circuit. Where V_{SD} and V_{SG} are the source-drain voltage and the source-gate voltage for M_1 and M_2, respectively. Additionally, V_{THP} is the threshold voltage for M_1 and M_2. Nevertheless, the most convenient mode is the operation of M_3 in sub-threshold region ($V_{GS3} < V_{THN}$). Where V_{GS3} is the gate-source voltage for M_3 and V_{THN} is the threshold voltage for M_3. Also, M_1 operates in sub-threshold region for low input currents and saturation region for high input currents [9,10].

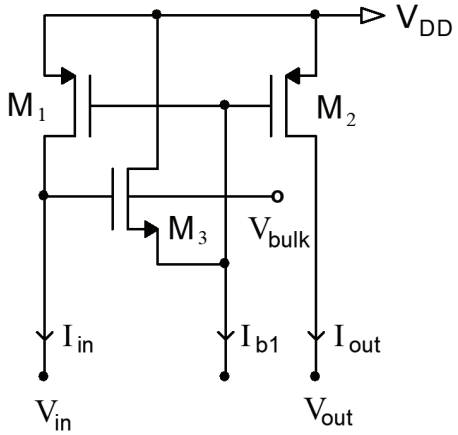


Figure 2: PMOS level-shifter current mirror.

Threshold voltage can be defined by [11]

$$V_{THN} = V_{THO} + \gamma\left(\sqrt{2|\varphi_F| - V_{BS}} - \sqrt{2|\varphi_F|}\right) \tag{3}$$

where V_{THN} is the threshold voltage for M_3, V_{THO} is the zero-V_{BS} value of the threshold voltage, ϕ_F is the surface

inversion potential of silicon, γ is the body effect parameter and V_{BS} (V_{bulk}-V_S) is the bulk-source voltage. V_{BS} represents the bulk-source voltage for M_3. As shown in Figure 2, transistor M_3 has been used for shifting the voltage level at the drain terminal of M_1. The high value of the biasing current forces M_3 to operate in the saturation region. According to these results, the relation between the voltages can be written as below

$$V_{in} = V_{DD} - \left(V_{SG1} - V_{GS3}\right) \tag{4}$$

where V_{SG1} and V_{GS3} are the gate-to-source voltage of the relevant transistors. The equations describing the operation in saturation and sub-threshold regions, respectively are

$$I_{D1} = \frac{1}{2} k_p \frac{W_1}{L_1} \left(V_{SG1} - V_{THP}\right)^2 \tag{5.a}$$

$$I_{D3} = I_{D03} \frac{W_3}{L_3} \exp\left(\frac{V_{GS3} - V_{THN}}{nU_T}\right) \tag{5.b}$$

where I_{D1} and I_{D3} are the drain currents of transistors M_1 and M_3, respectively. Besides, $k_p = \mu_n C_{ox}$ is the transconductance parameter of the PMOS transistor, U_T is the thermal voltage and I_{D03} is the saturation current. Also, I_{D03} and *n* are the process- dependent constants. From Equation (5), the V_{SG1} and V_{GS3} can be obtained as

$$V_{SG1} = \sqrt{\frac{2I_{in}}{k_p \left(W_1 / L_1\right)}} + V_{THP} \tag{6.a}$$

$$V_{GS3} = nU_T \left| \ln\left(\frac{I_{b1}}{I_{D03}} \frac{L_3}{W_3}\right) \right| + V_{THN} \tag{6.b}$$

The input voltage of LSCM can be written as below

$$V_{in} = V_{DD} - \sqrt{\frac{2I_{in}}{k_p \left(\frac{W_1}{L_1}\right)}} + nU_T \left| \ln\left(\frac{I_{b1}}{I_{D03}} \frac{L_3}{W_3}\right) \right| - \left|V_{THP}\right| + V_{THN} \tag{7}$$

by using Equations (5) and (6). For low voltage operation, $V_{THN} > |V_{THP}|$ and $I_{in} > I_{b1}$ is required. This condition related to threshold voltages is arranged when the bulk-source voltage of the M3 is negative value using the bulk voltage (V_{bulk}) as shown in Equation (3).

The output voltage necessity for the proposed PMOS LSCM is given by

$$V_{out,max} \approx V_{DD} - V_{DS2,sat} \tag{8}$$

4 Proposed low-voltage PMOS current mirror structure

The low-voltage PMOS current mirror (LVCM) structure is shown in Figure 3.

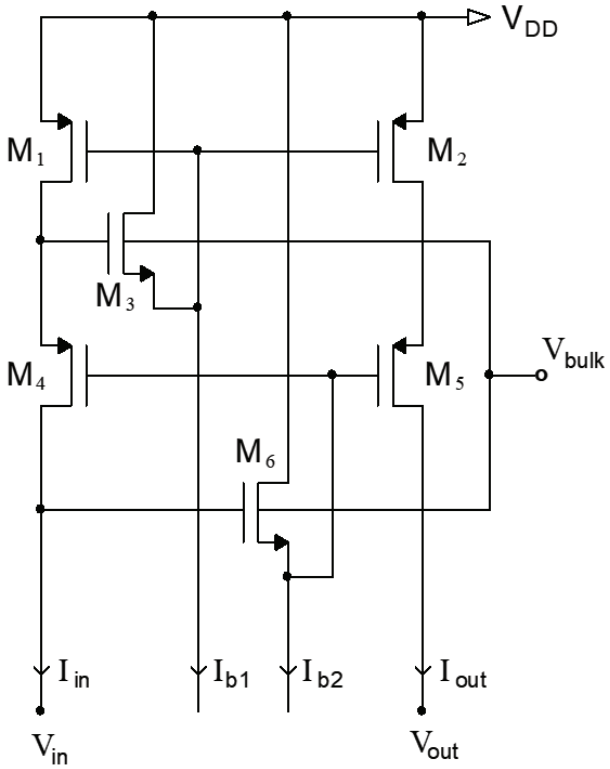


Figure 3: Low-voltage PMOS current mirror.

The input voltage for the proposed CM is given by

$$V_{in} = V_{DD} - \left[\left(V_{SG1} + V_{SG4}\right) + \left(V_{GS3} + V_{GS6}\right)\right] \tag{9}$$

From Equation (3), it can be seen that the threshold voltage can be increased by using the bulk-source voltage for M_3 and M_6. Hence, it should be indicated that this condition for the PMOS transistor can achieve level-shifting operation. If Figure 3 is analyzed, it can be seen that $V_{SG1} > V_{GS3}$ and $V_{SG4} > V_{GS6}$ because there is a relationship between voltages as $V_{THN} > V_{THP}$. This condition is arranged when the bulk-source voltage of the M_5 and M_6 is negative value as seen in Equation (3). Also, the input voltage of the CM shown in Figure 3 can be written as

$$V_{in} = V_{DD} - \sqrt{\frac{2I_{in}}{k_p \left(\frac{W_1}{L_1}\right)}} - \sqrt{\frac{2I_{in}}{k_p \left(W_4 / L_4\right)}} + nU_T \left| \ln\left(\frac{I_{b1} I_{b2}}{I_{D03} I_{D06}} \frac{L_3 L_6}{W_3 W_6}\right) \right| - 2\left|V_{THP}\right| + 2V_{THN} \tag{10}$$

where $k_p = \mu_n C_{ox}$ is the transconductance parameter of the PMOS transistor, U_T is the thermal voltage and I_{D03}, I_{D06} is the saturation current. Also, I_{D03}, I_{D06} and *n* are the process- dependent constants. The maximum output voltage requirement for the proposed CM is given by

$$V_{out,max} \approx V_{DD} - (V_{DS2,sat} + V_{DS5,sat}) \tag{11}$$

Input and output impedances of the proposed circuit can be defined as

$$R_{in} \approx \frac{g_{m1} + g_{m4}}{g_{m1} g_{m4}} \tag{12.a}$$

$$R_{out} \approx \frac{g_{m5}}{g_{ds2} g_{ds5}} \tag{12.b}$$

The proposed LVCM is shown in Figure 4. The transistors M_7 and M_8 have been added for biasing.

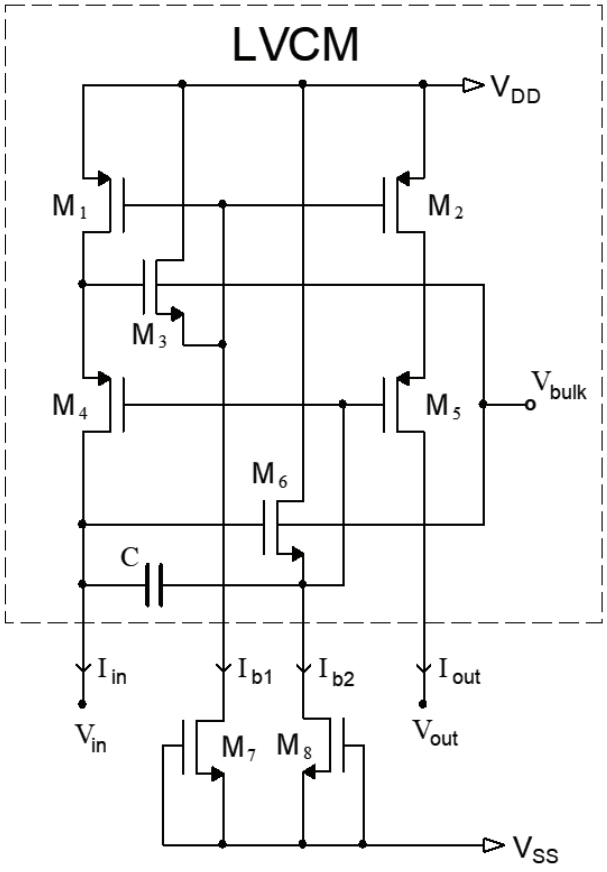


Figure 4: Enhanced low-voltage PMOS current mirror.

If the M_3 and M_6 are considered identical, the biasing current I_{b1} can be given as

$$I_{b1} = I_{D07} \frac{W_7}{L_7} \exp\left(\frac{-V_{THN}}{nU_T}\right) \tag{13}$$

I_{D07} is the saturation current. Also, I_{D07} and *n* are the process-dependent constants. I_{b2} can be defined as similar to I_{b1}. It can be seen that these currents are always low. Thus, the M_3 and M_6 operate in the sub-threshold region. Also, using an external capacitance (C) shown in Figure 4 decreases effective input capacitance.

Figure 5 (a) indicates the conventional transconductance amplifier circuit. Figure 5 (b) indicates the proposed transconductance amplifier circuit for use in low voltage applications.

The drain resistance as a load is used in the transconductance amplifier. Replacing the drain resistance with a current mirror as an active load results in much higher voltage gain [11]. The proposed LVCM as an active load can be used in the transconductance amplifier shown in Figure 5 (b). Transconductance can be expressed as

$$G_m = \frac{I_0}{V_1 - V_2} \cong \sqrt{I_B k_n \frac{W}{L}} \tag{14}$$

Here, it can be determined as $G_m \approx g_m = g_{m9} = g_{m10}$. Where V_1, V_2 are the input voltages, I_0 is the output current, g_{m9} and g_{m10} are the transconductances of transistors M_9 and M_{10}, respectively. W/L is the aspect ratio of the transistors using for differential pair. The bulk for differential pair is connected to drain in Figure 5 (b). Body bias is used to dynamically adjust the threshold voltage (V_{TH}) of a CMOS transistor. The polarity of the body bias for M_9 and M_{10} is positive values. This situation causes a decrease in the value of V_{TH} for M_9 and M_{10}. The bulk-connected structure is suitable for low voltage applications. Also, the current I_B is the biasing current for the differential pair. A low-voltage transconductance amplifier has been used in many active elements designed with low-power such as Op-Amp, OTA and current conveyor [1-4]. Thus, these active elements have gained operating capability at the low-voltage by using the proposed circuit.

5 Simulation results

The current mirror circuits (Figs. 1, 2, and 4) were simulated for TSMC 0.13 µm technology. The aspect ratios of the transistors are given in Table 1.

Table 1: The aspect ratio of the transistors.

Transistor	M1–M4	M5, M6	M7, M8	M9, M10	M11, M12
W/L (µm)	30/0.26	20/0.26	0.26/0.26	2/1	40/0.26

All the circuit operations have been simulated for the supply voltage ±0.5 V. Currents I_{b1} and I_{b2} are selected

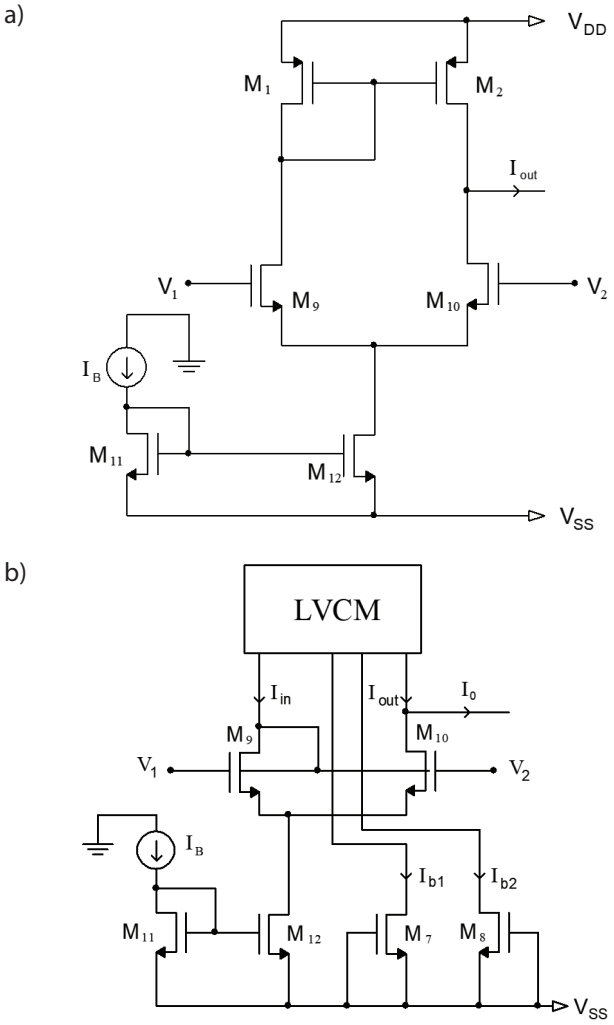


Figure 5: Transconductance amplifiers a) conventional, b) proposed.

as 20 nA. Also, V_{bulk} is equal to -0.5V (V_{SS}). Comparison of current/voltage characteristics of the current mirrors is illustrated in Figure 6. V_{in} is the input voltage for LVCM is shown in Figure 3. The value of V_{in} is taken as 0 V. The I / V characteristic shown in Figure 6 is obtained by changing the supply voltage between 0 mV and 600 mV.

It is clearly shown that the supply voltage of the proposed LVCM requires the lowest value of the supply voltage compared to any other structures. Therefore, the proposed circuit is suitable for low voltage applications. The current transfer characteristic exhibits linear behavior as depicted in Figure 7. However, deviation from linearity occurs for larger value of currents.

The percentage gain error (I_{out} / I_{in}) of the proposed circuit is approximately 0.3 % for I_{in}=200 µA as displayed in Figure 8. Whereas, the percentage gain error (I_{out} / I_{in}) of the PMOS LSCM and conventional CM are 0.6 % and 0.9 % for I_{in}=200 µA, respectively.

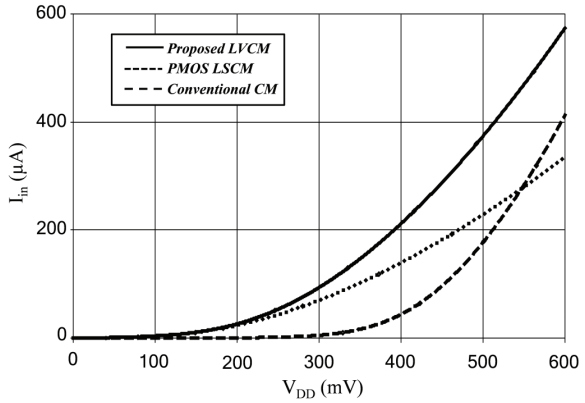


Figure 6: Comparison of I / V characteristics of various CMs.

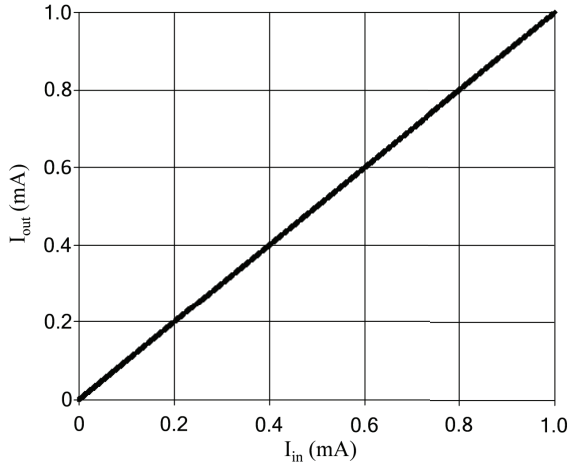


Figure 7: Current transfer characteristics of proposed LVCM.

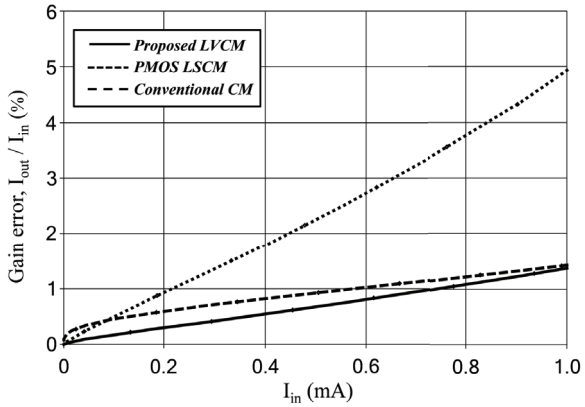


Figure 8: Current tracking errors of various CMs.

The I-V characteristics of the proposed LVCM at different input currents are illustrated in Figure 9. The output current swing of the LVCM is almost independent on V_{DD} for low output current values. The value of V_{out}

is taken as 0 V (V_{out} = 0 V). Considering the output current of the proposed LVCM it can be operated at 0.5 V as shown in Figure 9.

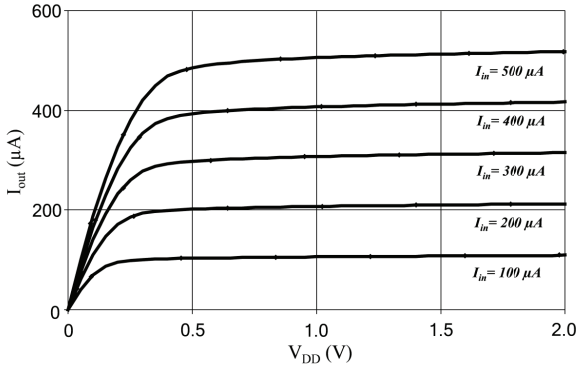


Figure 9: I-V characteristics of the proposed LVCM.

The frequency responses of the current mirrors are indicated in Figure 10.

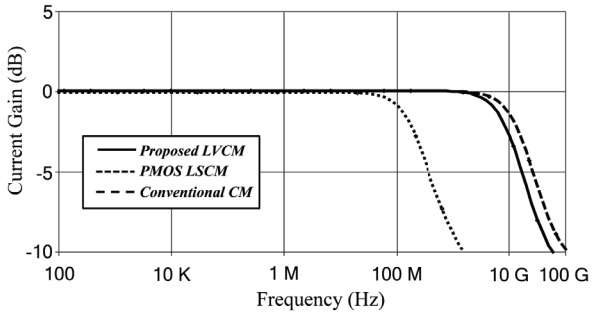


Figure 10: Comparison of the bandwidth of various CMs.

There is an improvement in the bandwidth when a capacitance (C) is used and the bandwidth is found to be 11 GHz. It is shown that the bandwidth reduces to 5 GHz when the C is not used in the design. It is seen that as the capacity value increases, the bandwidth increases. Also, the capacitance (C) has a value of 100 pF. The bandwidth of the PMOS LSCM and conventional CM are 0.24 GHz and 17.2 GHz, respectively.

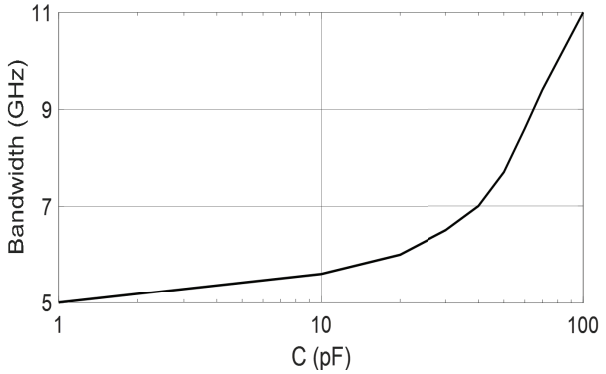


Figure 11: Variation of the bandwidth with external capacitor

The capacitance (C) has a value of 100 pF for 11 GHz shown in Figure 11. As the capacitance value decreases, the bandwidth decreases. The bandwidth can be sacrificed to obtain the lower value of capacitance.
The temperature effect on gain-bandwidth performance of the LVCM is depicted in Figure 12.

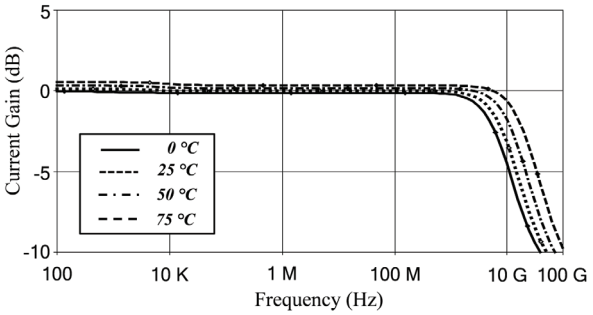


Figure 12: The temperature effect on Gain-Bandwidth performance of the LVCM.

The current gain is about equal to 0.35 dB for 75 °C as shown in Figure 12. Although higher temperature increases the gain of the LVCM the increase is tolerable. The LVCM exhibits temperature-dependent bandwidth characteristics depending on transistors M_3 and M_6 operates in sub-threshold region as shown in Figure 3. The Monte Carlo analysis which is repeated for 30 times is illustrated in Figure 13.

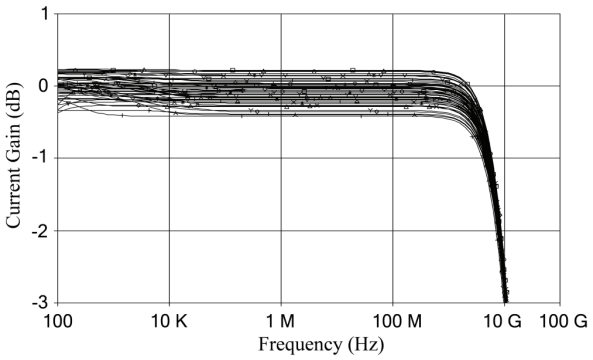


Figure 13: Monte Carlo analysis for Current Gain.

Figure 13 justifies that current gain value has still stable under 20 % random variations in threshold voltages of the transistors. Figure 13 indicates the good performance of the proposed circuit versus mismatches.

Performance comparison of the aforementioned current mirrors is depicted in Table 2.

Table 2: Performance comparison of the CMs.

Parameter	PMOS CM	Level Shifter CM	Proposed LVCM
Power dissipation (μW)	177	67.7	56.6
3 dB BW, I_{out} / I_{in} (GHz)	17.2	0.24	11
V_{in} (mV)	512	470	392
R_{in} (KΩ)	2.56	2.35	1.96
R_{out} (KΩ)	69.5	99.3	130
Gain error, I_{out} / I_{in} (%)	0.9	0.6	0.3
for supply voltage = ±0.5 V and input current I_{in} = 200 μA			

When the performance parameters of the CMs are investigated, it is clearly shown that the proposed structure has a lot of advantages compared with the others. Significantly, the proposed circuit's input resistance is much lower than the others, and it is seen that the suggested LVCM's low input voltage is one of the critical advantages. Also, the gain error belonging to currents (I_{out} / I_{in}) of the proposed circuit is reasonable compared to the other circuits.

The low-voltage transconductance amplifier used the LVCM and the conventional transconductance amplifier is shown in Figure 5. These circuits were simulated for TSMC 0.13 μm technology. The aspect ratios of the transistors are given in Table 1.

The relation between input difference voltage and output current of the transconductance amplifiers is depicted in Figure 14. Also, the supply voltage has been chosen as ±0.5 V for both amplifiers. The value of I_B shown in Figure 5 is chosen as 50 μA.

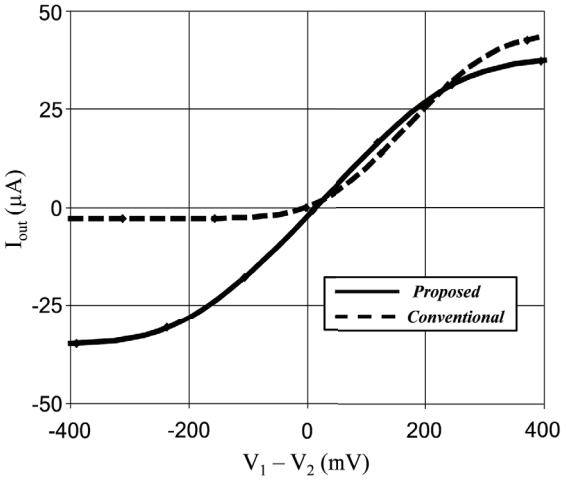


Figure 14: I / V characteristic of the transconductance amplifiers (input difference voltage versus output current)

Conventional transconductance amplifier has not exhibited good performance at low voltage. The circuit has not strictly operated at ±0.5 V for the negative values of the output current. It is shown that the proposed circuit is more suitable than the other circuit for low voltage applications. However, a conventional transconductance amplifier can only be operated on minimum supply voltage with ±0.65 V, while the proposed circuit can be employed for lower voltage.

Figure 15 indicates the power consumptions of the proposed and conventional transconductance amplifiers for different biasing currents (I_B).

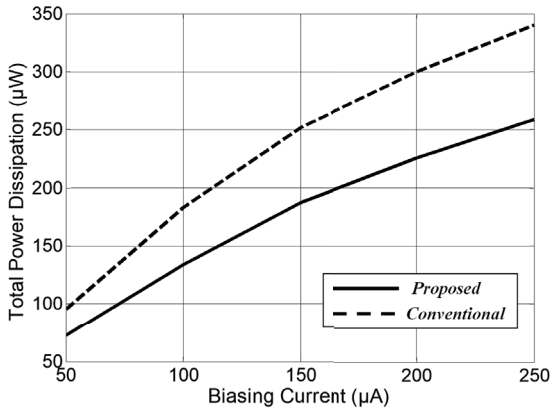


Figure 15: Total power dissipation versus biasing currents for circuits.

As seen in Figure 15, the presented circuit consumes lower power than the conventional circuit for diverse biasing currents. The proposed circuit consumes 70 μW for 50 μA of biasing current. Hence, the suggested circuit is suitable for low-power applications.

The frequency performance of the transconductance amplifiers is illustrated in Figure 16.

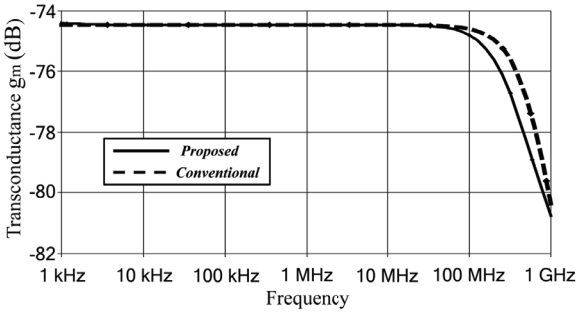


Figure 16: The frequency response of the transconductance amplifiers.

Frequency responses of the transconductance (g_m) value for the proposed and conventional circuits are indicated in Figure 16, which gives a bandwidth (-3dB) of 398.8 MHz and 581.1 MHz, respectively.

The total harmonic distortion (THD) is evaluated for input voltage with different amplitudes for a biasing current of 50 µA, as shown in Figure 17.

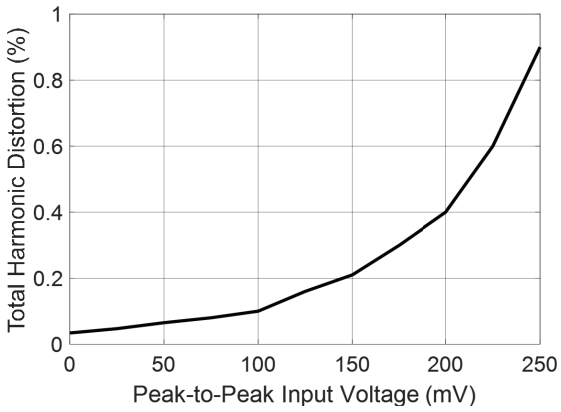


Figure 17: THD (%) versus input voltage (at a frequency of 1 MHz) for the proposed circuit.

The fundamental frequency (1st harmonic) has been specified and THD has been calculated via the PSpice program. The third harmonic provides the most important contribution to the total harmonic distortion of the circuit. The THD has a value of about 0.94% for 250 mV_{P-P}. It is shown that THD obtained according to the different peak-to-peak input voltages are reasonable values.

6 Conclusion

A low-voltage current mirror circuit employing the voltage level-shifting principle is demonstrated for use in differential pair as an active load. The proposed current mirror operates at ±0.5 V and its bandwidth is about 11 GHz. Also, it consumes 56.6 µW power. The proposed circuit exhibits better performance than the other CMs called PMOS CM and level shifter CM. It is undeniable that the simulation results confirm the validity of the theory and demonstrate the usage of the LVCM in electronic applications. Also, the proposed transconductance amplifier using LVCM has been compared to the conventional one. The proposed transconductance amplifier's bandwidth is about 581.1 MHz. It consumes 70 µW power. Finally, such a current mirror is appropriate for low-voltage applications, resulting in increasing threshold voltage. Hereafter, the suggested PMOS current mirror would be operated even at lower supply voltages if the threshold voltages could be decreased.

7 Conflict of interest

The authors declare no conflict of interest.

8 References

1. S. Chatterjee, Y. Tsividis, and P. Kinget, "Ultra-low voltage analog integrated circuits," *IEICE Trans. Electron.*, vol. E89-C, no. 6, pp.673–680, 2006, https://www.doi.org/10.1093/ietele/e89-c.6.673.
2. S.A. Tekin, H. Ercan, and M. Alçı, "Novel low voltage CMOS current controlled floating resistor usingdifferential pair," Radioengineering, vol. 22, no. 2, pp. 428-433, 2013, https://dx.doi.org/10.13164/re
3. H. Ercan, "A linear current-controlled floating negative resistor," *Informacije MIDEM Journal of Microelectronics*, Electronic Components and Materials, vol.43, no.4, pp.222–227, 2013.
4. S.A. Tekin, "Voltage summing current conveyor (VSCC) for oscillator and summing amplifier applications," *Informacije MIDEM Journal of Microelectronics*, Electronic Components and Materials, vol. 44, no. 2, pp. 159–167, 2014.
5. K. K. Abdalla, D. R. Bhaskar and R. Senani, "A review of the evolution of current-mode circuits and techniques and various modern analog circuit building blocks," *Nature & Science*, vol. 10, no. 10, pp. 1–13, 2012, https://www.doi.org/ 10.7537/marsnsj101012.01
6. K. Monfaredi, H. Faraji Baghtash, "An Extremely Low-Voltage and High-Compliance Current Mirror" *Circuits Syst Signal Process*, vol. 39, pp. 30–53, 2020, https://doi.org/10.1007/s00034-019-01175-1.
7. J. Ramirez-Angulo, "Low voltage current mirrors for built-in current sensors*", IEEE International Symposium on Circuits and Systems ISCAS '94*, vol. 5, 1994, pp .673–680, https://www.doi.org/ 10.1109/ISCAS.1994.409429.
8. H. Ercan, S.A. Tekin, and M. Alçı, "Low-voltage low-power multifunction current-controlled conveyor," *International Journal of Electronics*, vol. 102, no. 3, pp. 444–461, 2015, https://doi.org/10.1080/00207217.2014.897382.
9. S.S. Rajput, and S.S. Jamuar, "A current mirror for low voltage, high performance analog circuits," *Analog Integrated Circuits and Signal Processing*, vol. 36, no. 3, pp.221–233, 2003, https://doi.org/10.1023/A:1024718421282.

10. S. Yan, and E. Sanchez-Sinencio. "Low voltage analog circuit design techniques: A tutorial," *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, vol.83, no.2, pp. 179–196, 2000.
11. A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, Revised Edition, Oxford University Press, New York, 2007.

Arrived: 11. 01. 2021
Accepted: 01. 04. 2021

Original scientific paper
https://doi.org/10.33180/InfMIDEM2021.105

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 51, No. 1(2021), 73 – 84

Effect of Dipole Position and Orientation on Light Extraction for Red OLEDs on Periodically Corrugated Substrate - FEM Simulations Study

Milan Kovačič

University of Ljubljana, Faculty of Electrical Engineering, Ljubljana, Slovenia

Abstract: One of the main efficiency-limiting factors for organic light-emitting diodes (OLEDs) is poor light extraction, which typically reaches only 20% (in best cases up to 30%) in flat standard devices. Optical modeling and simulations play an important role in improving light extraction and optimizing outcoupling efficiency. Using FEM modeling approach, the effect of dipole positions and orientations for red OLEDs on periodically corrugated substrate is evaluated and used to enhance the outcoupling efficiency. It is shown that with only 3 carefully selected dipole positions, the outcoupling efficiency over the whole area can be predicted with very reasonable accuracy, which greatly reduces the number of simulations required. The presented modelling approach is used for optimization of the sine texture as a substrate corrugation structure. OLEDs with optimized simulated texture show a relative improvement of light outcoupling from the thin film stack to the substrate by more than 25% compared to the flat plane devices.

Keywords: OLED; outcoupling; finite element method; optical modelling

Vpliv Pozicije in Orientacije Dipola na Izstop Svetlobe Rdečih OLED na Periodično Teksturiranem Substratu – FEM Simulacijska Obravnava

Izvleček: Eden izmed glavnih dejavnikov, ki omejujejo učinkovitost organskih svetlečih diod (OLED), je nizka stopnja učinkovitosti izstopa svetlobe, ki pri standardnih napravah dosega le okoli 20% (v najboljših primerih pa do 30%). Optično modeliranje in simulacije igrajo pomembno vlogo pri izboljšanju izstopa svetlobe in optimizaciji optičnega izkoristka. Z uporabo FEM modeliranja se ovrednoti učinek položaja in usmeritve dipolov za rdečo OLED na periodično teksturiranem substratu, ki se uporablja za povečanje učinkovitosti izstopa svetlobe. Pokaže se, da je mogoče s samo 3 skrbno izbranimi položaji dipola, z dobro natančnostjo napovedati učinkovitost izstopa na celotnem območju, kar močno zmanjša število zahtevanih simulacij. Predstavljeni FEM pristop se uporabi za optimizacijo sinusne teksture kot strukture teksturiranega substrata. OLED z optimizirano simulirano teksturo kažejo relativno več kot 25% izboljšanje učinkovitosti izstopa svetlobe iz tankoplastne strukture v substrat v primerjavi s ploščatimi napravami.

Ključne besede: OLED; izstop svetlobe; metoda končnih elementov; optično modeliranje

** Corresponding Author's e-mail: milan.kovacic@fe.uni-lj.si*

1 Introduction

Organic light-emitting diodes (OLEDs) have in recent years achieved a commercial widespread in display technology, especially in mobile and television displays. OLEDs are also very promising for general indoor and outdoor lighting, due to low cost, high efficiency, and high color quality. OLEDs can be fabricated as a large area sources on rigid or flexible substrates, can be made transparent for application on windows, all of which is important in lighting and architecture design [1]–[5]. OLEDs based on phosphorescent [6] and more recently on thermally activated delayed fluorescence

emitters [7], [8] have already achieved internal efficiencies close to 100%. On the other hand, highest *EQE*s for typical flat plane devices reaches only 20-30%, which is due to high optical losses resulting in poor light outcoupling efficiency [9].

Optical losses in OLEDs can be divided into three main groups. First are substrate losses due to total internal reflection (TIR) on the substrate/air interface, where light gets captured inside the thick substrate. Second are waveguide losses, that happen due to TIR at organic (transparent contact)/substrate interface, where light gets waveguided and eventually absorbed. Third part are losses due to coupling of light to surface plasmon polaritons (SPP) at organic/metallic interfaces. Minor losses are also due to parasitic absorption in layers [10]. There has been a lot of research and proposed solutions to improve the light outcoupling, see for example recent reviews [11], [12]. Especially on reducing the substrate losses, highly efficient solutions already exist, like attaching a half-sphere, different microtexturing [13]–[17] and others [18], [19]. On the other hand, solutions to waveguide and SPP losses exists, like micro-lens arrays [20], introducing scattering particles [21], corrugations [22], [23] and others [24], [25], but remain less researched and non-optimized. This is mainly because internal solutions are more challenging to fabricate and to integrate with OLED thin film stack, without having negative impact on electrical efficiency [26]. With this in mind, optical modelling and simulations play an important role in improving outcoupling efficiency, to predict optimal solutions prior to complicated fabrication process, to test only most promising ones. Simulations of light emission from thin film stacks with internal outcoupling solutions (e.g. texturization, corrugations, scattering particles) requires more advanced modelling approaches, compared to flat-plane devices.

In this paper, finite element method (FEM [27]) optical modelling is utilized to research effects of a corrugated substrate, which introduces internal textures in the OLED device structure itself. The aim is improved outcoupling of light into the substrate. In particular the focus is on investigation of different positions and orientations of emitting dipoles on outcoupling efficiency for red OLED on periodically corrugated substrate. FEM modelling approach, describing main considerations when simulating OLEDs, is explained. Presented model is used to analyze how number and position of simulated dipoles affect the simulated outcoupling accuracy. In addition, it is shown that in the analyzed cases already 3 specifically positioned dipoles in the simulation domain are sufficient to get good prediction of trends for outcoupling efficiency. Moreover, outcoupling efficiency and outcoupling trends of differently oriented dipoles for different positions on corrugated substrate are evaluated.

2 OLED Modelling

The outcoupling of light in OLEDs, which is the focus of this paper, can be presented by combined opto-electrical parameter called external quantum efficiency (*EQE*), which defines the ratio between the number of photons reaching the far field as useful light to the number of injected charge carriers. *EQE* is calculated using equation (1), where γ is electrical efficiency defined as ratio between the number of radiative recombination in emission layer and the number of injected charge carriers, $s_{\mathrm{el}}(\lambda)$ is normalized electroluminescent spectrum of emission material, $\eta_{\mathrm{out}}(\lambda)$ is outcoupling efficiency of generated light into far field and $\eta^{*}_{\mathrm{rad,e}}(\lambda)$ is effective radiative efficiency.

$$EQE = \gamma \int_{\lambda} s_{\mathrm{el}}(\lambda)\ \eta^{*}_{\mathrm{rad,e}}(\lambda)\ \eta_{\mathrm{out}}(\lambda)\ \mathrm{d}\lambda \tag{1}$$

where

$$\eta^{*}_{\mathrm{rad,e}}(\lambda) = \frac{\eta_{\mathrm{rad,e}}\ F(\lambda)}{1 - \eta_{\mathrm{rad,e}} + \eta_{\mathrm{rad,e}}\ F(\lambda)} \tag{2}$$

$\eta^{*}_{\mathrm{rad,e}}(\lambda)$ determines the ratio between radiative and non-radiative recombination. $\eta_{\mathrm{rad,e}}$ is the intrinsic radiative efficiency of the emitter and $F(\lambda)$ is the Purcell factor, defined as a ratio between total emitted light at the source location and total emitted light in infinitive homogeneous medium. Using optical simulations, also employed in this work, wavelength dependent outcoupling efficiency of generated light $\eta_{\mathrm{out}}(\lambda)$ and wavelength dependent Purcell factor $F(\lambda)$ are calculated, and with these and by using equations (1) and (2), *EQE* as a primary optical data can be calculated.

2.1 Modelling of light in thin film OLED stack

In OLEDs light is generated in the emission layer (EML) inside a thin film structure (e.g., see thin film structure used in this paper – Figure 1(a)) by electroluminescence emission of emitter material molecules. As sizes of these molecules are much smaller (few nanometers) than emission light wavelength (visible light), these can be treated as differently oriented point dipole sources [28]. The dipoles have specific predefined emission spectrum (determined by the molecule type) and angular intensity distribution and polarization of light according to the orientation in the layered system. Dipoles can in general have any arbitrarily orientation

which can be represented by three perpendicular dipole components, two horizontally (*x-y*) and one vertically (*z*) oriented according to the selected global coordinate system. In case of flat plane OLEDs, orientation of dipoles in the plane of layered system (*x-y*) plays no direct role on outcoupling efficiency itself (it can affect angular distribution of light) and is in most cases treated as isotopically oriented [29], thus only ratio between vertical and horizontal dipoles is considered. To describe general orientation of all emitting dipoles in the system, an anisotropy coefficient a is introduced, which is defined as the ratio between the vertical dipole component towards all three dipole components. Anisotropy coefficient $a = 1/3$ meaning isotropic orientation of dipoles, while $a < 1/3$ indicates preferential horizontal orientation of dipoles and $a > 1/3$, preferential orientation of vertical dipoles.

Simulation of flat plane devices can be quickly and efficiently done by decomposing the dipole emission into set of plane waves which are then transferred through the thin film stack by using transfer matrix method (TMM). In case of large external corrugations or other textures, TMM can be coupled with geometrical optics for complete device simulations [16], [17].

On the other hand, modelling and simulation of nanotextured, corrugated or by introducing other disruption in horizontal directions (e.g., scattering particles) requires more advanced approach.

For the modelling of nanostructured thin-film structure we use 3D optical simulator COMSOL Multiphysics [30], which is based on a finite element method. We choose FEM due to advantages over other methods (RCWA FDTD) due to possibility of better discretization with higher order approximation of field inside the element, fairly straightforward definition of material properties (dielectrics and metals) and boundary conditions (e.g. absorbing, symmetry), ability to handle complex 3-D geometry and especially delivery of steady-state solutions in frequency (wavelength) instead of time domain (e.g. FDTD).

Using FEM, an arbitrarily oriented dipole source can be placed anywhere inside the structure and its steady state can be simulated. As each dipole need to be treated as individual source in laterally large structure (incoherent relation between different dipoles), there is a problem how to set the boundary conditions of simulation domain to avoid coherent connections between different dipoles. This presents one of the main challenges in rigorous simulations of OLEDs, requiring special modelling approaches to be taken. For example, regular periodicity boundary conditions that significantly reduce the simulation domain to a single unit cell or less, cannot be used here, as imply coherent connections between sources in periodically repeated unit cells. One solution would be to put a single dipole source in a laterally large structure with dimensions large enough to take into account all effects taking place far away from the source with multiple simulations for each different dipole position and orientation [31]. Main drawback is the required size of the model, as propagation lengths can be very large, thus lateral sizes of at least 40 μm and more away from the source would be necessary to include majority of the effects. Such large models would require huge amount of computational power (especially limiting is the computer memory) and are thus not really feasible.

Alternative method is the usage of the so-called Floquet transform method [32], [33] (FTM). FTM highly reduces memory requirements as it enables simulations of a single period (geometry) with individual source anywhere in the basic cell by using the Floquet transform to decompose non-periodic dipole source to a linear superposition of Bloch periodic terms. Details on the method itself can be found in [32]. Drawback of this approach is that it requires large number of simulations for accurate results (many Bloch periodic terms). Numerous simulations are required due to application of different phases for in/out going waves at the edge of domain, required to cancel unwanted coherence between dipoles from neighboring domains. With parallelization this can be tolerable and FTM is also used for simulations in this work.

When constructing FEM model with FTM, we need to consider some specifics that we will describe in the following. Simulation domain needs to contain at least one, but multiple (integer) periods can also be used. On top (vertical dimension) unbounded areas that are stretching to infinity (e.g. glass, air), need to be truncated using open boundaries, absorbing all incident light with zero reflectivity. Open boundaries like perfectly matching layer (PML) or absorbing boundary conditions (ABC) are applied here. An important aspect is also the distance between open boundary and thin film stack. If the boundary is too close to the stack, possible coupling of evanescent waves to the boundary can happen influencing the simulation accuracy, on the other hand if the boundary is too far away, this can result in larger domain, requiring more computational power, elongating the simulation time. Here a rule of thumb is applied that the minimal distance between boundary and thin film stack is around 1~1.5 * simulated wavelength. In lateral directions where periodicity is applied, 2 pairs of periodic Floquet boundary conditions are used. For periodic boundary conditions, special care needs to be taken when meshing, as mesh shape and size needs to be identical on both repeating

sides, otherwise large errors can happen. For the rest of the device, meshing of the structure with general rule of thumb can be used, with 8-10 elements per distance of effective wavelength.

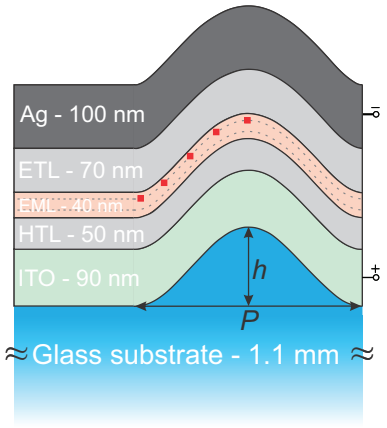
It needs to be mentioned that by using FTM (or other FEM method) angular intensity distribution (AID) of emitted light of OLED device in the far-field cannot be gained directly, only the total outcoupling efficiency and the Purcell factor can be calculated directly. For far field AID calculation, a reciprocity principle [34], [35] can be employed, that enables to calculate AID as a consequence of any single dipole (or continuous spatial emission by multiple dipoles) at any position in the OLED stack. For each plane wave entering from outside under specific angle of incidence, it can be recalculated (by knowing E field (simulations) at the dipole(s) location) how this dipole contributes to emission into this specific angle in the far field. Extending simulations to multiple incident angles (both zenith and azimuth), AID in the far field for all simulated incident angles can be gained. This approach can only access modes that reach the far field medium (glass, air), while all other modes are inaccessible, giving only partial data. For total evaluation, reciprocity principle for calculating AID and FTM for calculating outcoupling efficiency and Purcell factor, could be used as complementary methods, enabling simulations of device with thin and optically thick layers as well as nano and micro-sized textures or other outcoupling solutions.

2.2 Corrugated OLED structure description and model

In this contribution the focus is only on thin film stack and optical properties connected with it. In simulations glass substrate is treated as half infinitive, this is from experimental point similarly as by attaching a large glass hemisphere on top of the substrate, that enables extraction of almost all light that reaches the substrate. By this, losses due to TIR at substrate/air interface are excluded and additional back reflections into the thin film stack are neglected, thus only waveguide and SPP losses are included. Due to this, outcoupling efficiency through entire paper is considered for light reaching the substrate and consequently air by using a glass hemisphere (ignoring minimal losses at glass hemisphere/air interface). We focus on standard red bottom emitting OLED [10], [16], with high electrical efficiency $\gamma = 1$ and intrinsic radiative efficiency $\eta_{rad,e} = 0.7$. Simulated stack, with layer thicknesses marked, is presented in Figure 1(a). Emission layer (EML), where light is generated, is sandwiched between two blocking layers (for electrons - EBL and holes - HBL), and two transport layers (for electrons - ETL and holes HTL), that ensure high recombination rate in EML. Contacts are realized by opaque Ag cathode and a transparent indium tin oxide (ITO) anode. In our simulation model, EBL, HBL and EML were joined into single EML layer, to avoid very thin layers that can be very problematic to mesh and add unnecessary complexity to the device. This can be justified due to very similar optical properties of these layers so only minimal difference is expected. Emission dipoles are positioned at EML/HBL interface, as majority of recombination events occurs in vicinity of HBL, due to higher hole conductivity of EML. Entire thin film stack is deposited on top of a flat or sine textured substrate. A sinusoidal texture is selected as it is commonly used and can be experimentally fabricated on e.g. silicon or glass master by e-beam or other etching techniques. Additionally, selected sine texture exhibits smooth morphology without any abrupt changes, minimizing possibility of introducing electrical defects. All results in this contribution are related to this texture shape.

When layers are deposited on top of a textured substrate, they experience layer growth which is a combination of conformal and isotropic growth [36]. In this case a more conformal growth (linear combination of both 0.3*isotropic + 0.7*conformal) was used, which is the most common growth ratio in many amorphous materials. Actual layer growth as used in model can be seen in Figure 1(b).

a)



b)

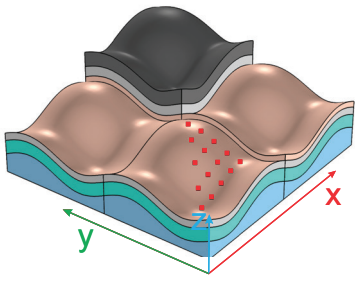


Figure 1: a.) Thin film stack of a standard red bottom emitting OLED on a corrugated glass substrate. b) Position of dipoles on a corrugated substrate (red dots shown on 1/8th of the period area only)– snapshot from Comsol simulator

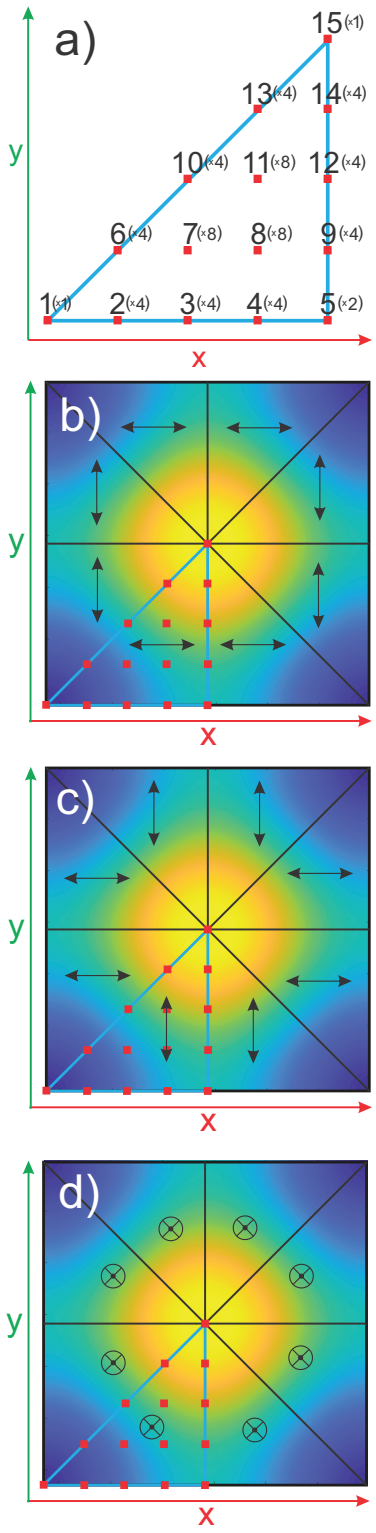


Figure 2: a.) Top view of dipole numbering on top of 1/8 of sine texture with weights factors in brackets. b-d.) Top view of sine textures, with marked dipole positions (red dots shown on 1/8th of the period area only) and arrows showing dipole orientations as defined and used in simulations. The three analyzed situations with respect to dipole orientations are denoted with horizontally – 1 (b), horizontally – 2 (c) and vertically (d) oriented dipoles.

In EML a continuous homogenous spatial emission in the emission layer is assumed, i.e. an uninterrupted distribution of dipoles across the entire emission layer. With laterally symmetrical textures, such as the 2D sine texture in this case – Figure 1 (b), an advantage of the symmetry of the structure can be taken and only dipoles on a smaller area can be simulated. In this case, this means that by considering dipoles on only 1/8 of the period (see Figure 1 (b) with red dots indicating dipole positions), the coverage of emission sources over the entire period and thus structure can be described. On the other hand, for non-symmetrical textures (e.g. saw profile or random) all possible locations of dipoles need to be considered. In the case of the sine texture, 15 dipoles positioned at constant distances from each other within the 1/8 of the texture were used, with the aim to consider as many possible positions of the dipoles on the texture, including extreme positions (e.g. on top and bottom of the texture). The numbering of the dipoles starts with no. 1 at the bottom (minimum) of the texture and ends at the top (maximum) with no. 15. Other dipole positions and corresponding number markings can be read from Figure 2(a) (top view of the dipole area, which can be linked to Figure 1(b)). It must also be taken into account that not all dipole positions, once extended to the whole period, make the same contribution to the total outcoupling efficiency, as some dipoles represent larger area than others - see Figure 2(a) (weighing factors for entire period marked with x-times) and Figure 2 (b-d). For example, area corresponding to dipole at location 15 (also 1) when extended to the whole period represent the same area as a dipole at location 7 (8 or 11) before extension, resulting in 8-times lower contribution for dipole at location 15 (or 1) than for dipole at location 7 (8 or 11). To compensate for this, an additional weighting factors are added to each simulated dipole according to the represented area in the whole structure - see weighting factors in brackets in Figure 2(a), next to the dipole number.

The orientation of the dipole is defined by its dipole moment direction, which for horizontally oriented dipoles points in the *x, y* plane and for vertically oriented dipoles in ±*z* direction according to the globally defined coordinate system and not according to the texture surface normal. For vertically oriented dipoles, this direction is uniquely defined in ±*z* direction. While for two horizontally oriented dipoles the orientation in the *x, y* plane is in general free, only with the requirement of 90 degrees between them. Due to introduced symmetry in used model, the orientation is defined in the initial simulation domain (1/8 of the period), where two horizontally oriented dipoles are differentiated as horizontally oriented - 1, where dipole moment direction points in ±*x*-direction, and as horizontally oriented - 2,

where dipole moment direction points in ±*y*-direction-see Figure 2 (b-d). Looking at the symmetry, extension over the texture diagonal leads to a change of dipole moment direction by 90 degrees in a defined coordinate system. As our definition of dipole orientation is defined on the starting 1/8 of the structure, even though the dipole moment is rotated by 90 degrees, the orientation with respect to the structure remains the same and is still treated as the same orientation as defined in the original 1/8 of the period. For details on the orientation of dipoles over the entire period, see Figure 2 (b-d).

3 Results

3.1 Flat plane device

To verify the presented FEM model, a simple device with a flat plane is simulated and results are compared (see Figure 3) with an internally developed TMM model which has been derived theoretically and verified experimentally [16].

Two orientations of dipoles are considered separately in this case: horizontally oriented-1 (identical results have been obtained for the horizontally oriented-2 in case of flat device) and vertically oriented (along *z* axis). In Figure 3(a) simulation results are presented for the outcoupling efficiency - $\eta_{out}(\lambda)$ and in Figure 3(b) the Purcell factor - $F(\lambda)$ (see definitions in Eq. 1). For both horizontally and vertically oriented dipoles very good agreement between the results can be observed, especially for the outcoupling efficiency. On the other hand, some differences in the Purcell factor can be seen, but the deviations from the correct results are small and should even decrease with texturization due to multiple random scattering events, resulting in reduced unwanted coherence between random scattering events resulting dipoles (boundary conditions).

3.2 OLED on corrugated substrate - effect of dipole location and orientation

FEM model is used to analyze optical properties, with the focus on light outcoupling of the red OLED thin-film stack deposited on a sine textured substrate with a period $P = 800$ nm and different height ranging from 0 (flat) to 400 nm (see definition of P and h in Figure 1). The effect of dipole positions and heights on outcoupling efficiency is analyzed. Results are presented for wavelength of 612 nm, that corresponds to the emission spectrum peak presented in Figure 3(a).

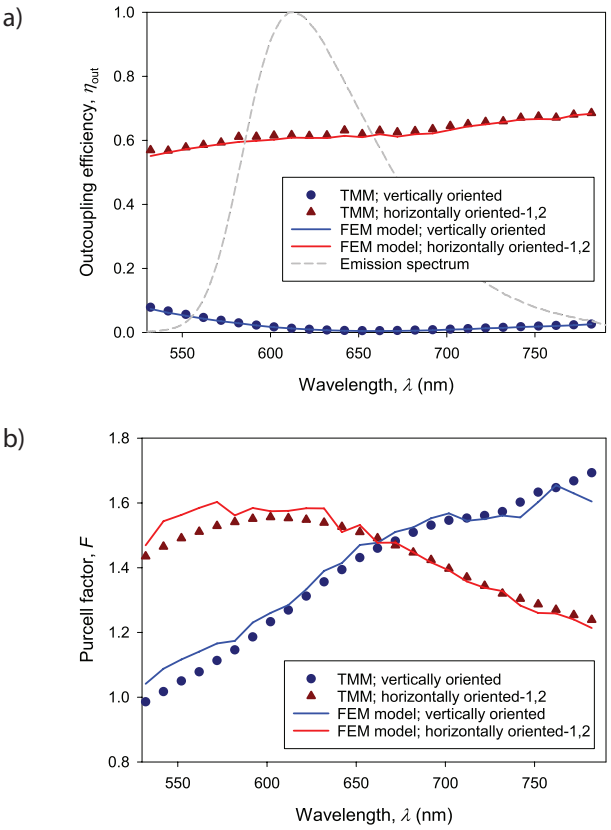


Figure 3: Comparison between two simulation models of a flat plane OLED. Symbols and lines represent results obtained with the TMM method and the FEM model, respectively. a) Outcoupling efficiency (Light extraction to substrate), b) Purcell factor.

First, the focus is on how dipole positions and orientations influence light outcoupling for different heights of the sine texture. For this, simulations of outcoupling efficiency for each of 15 dipoles individually for all three orientations and with different heights (0-400 nm) of the texture were carried out. Results of the simulations are presented in Figure 4(a-c), where lines represent outcoupling to substrate for each dipole individually and the crosses with dashed lines present weighted average of all 15 dipoles, which is actually the result corresponding to situation when all dipoles were included in calculation at once. Since the dipoles are not coupled in a coherent manner, such averaging can be carried out.

First observation from the results plotted in Figure 4 (a-c) is a high spread of results depending on the position of the dipole, indicating high influence of dipole position on the outcoupling efficiency. It has to be noted that global orientation of dipoles in one orientation set (e.g., horizontally oriented -1) remains the same independent of the dipole position. Differences are increasing with increasing texture height. This is expected, as the differences in actual vertical positions of dipoles

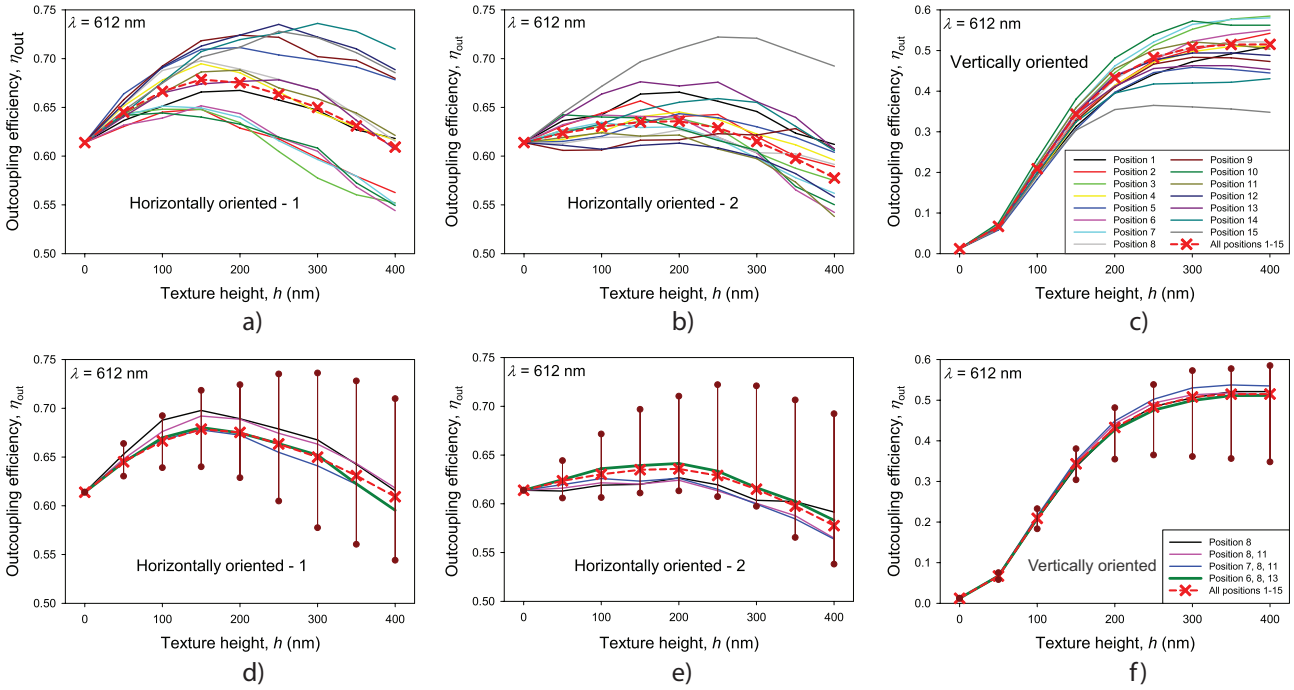


Figure 4: Outcoupling efficiency (to glass substrate) for each individual dipole according to its position on texture for different heights of the texture. a) Horizontally - 1 oriented dipoles, b) Horizontally - 2 oriented dipoles and c) Vertically oriented dipoles. d), e), f) - comparison between weighted average of all dipole positions taken into account and specifically selected ones. Added are maximum deviations for both higher and lower outcoupling efficiency. d) for horizontally - 1 oriented, e) horizontally - 2 oriented and f) vertically oriented dipoles.

are larger for the textures with higher *h*. Differences in outcoupling efficiencies between specific dipole locations can also be very high, especially for horizontal orientations, with absolute differences between minimum and maximum value above 10% for horizontal dipoles and even above 25% for vertical dipoles at texture height of 400 nm.

For a visual presentation of the effect of dipole location for the three different orientations, outcoupling efficiencies are compared again for OLED structure with the sine texture with $P = 800$, $h = 250$ (max. outcoupling with $a = 0.24$). The outcoupling efficiency according to the dipoles position on one quarter of the sine texture is shown in Figure 5. For both horizontal orientations, the highest outcoupling efficiency can be observed for the dipoles which are located on top of the texture, while outcoupling starts to decrease when moving towards the lower positions, again it slightly increases at the lower end. For horizontal-1, a high outcoupling at the ridge can be observed, while for horizontal-2 at the same position no such increase can be observed. With vertically oriented dipoles, in contrast to both horizontally oriented dipoles, a minimal outcoupling efficiency is achieved at the top end of the texture, which increases towards the middle of the texture, while outcoupling decreases again at the minimum. The outcoupling efficiency seems to follow the inclination on the texture. For horizontal dipoles a lower outcoupling at higher inclinations (separately in x or y direction for horizontal-1 and horizontal-2) is gained. While with vertical dipoles at higher inclinations a higher outcoupling efficiency is observed. This would indicate, as a highly simplified approximation, that textures with less steep features are required for an optimal outcoupling with horizontally oriented dipoles, while for vertically oriented dipoles exactly the opposite is required, i.e. textures with steeper features, indicating that the final outcoupling efficiency is a compromise between both scenarios. The optimal texture would also change with the general orientation of the dipoles, since a different texture would be optimal if there would be more vertically oriented dipoles or more horizontally oriented dipoles. Ultimately, the outcoupling cannot only be related to the inclination of the texture, as there are a number of other effects, such as the actual texture shape, the emission wavelength, the thin-film structure, all of which are specific to each individual OLED design, but these findings can serve as guidelines for further research. In addition, the mixture of many optical effects, with a high dependency not only on the shape and size of the texture but also on the emitting dipole positions and orientations, shows the importance of optical modeling and simulations for the planning, optimization and analysis of optimal optical solutions for achieving the highest outcoupling of individual OLED design.

3.3 Effect of number of dipoles used in simulations

To evaluate how much each outcoupling efficiency at each dipole position differs from weighted average, in Figure 6 total relative deviation from weighted average is presented, calculated as abs(($\eta_{out(i)}$)-$\eta_{out(average)}$) / $\eta_{out(average)}$), where *i* is the number of the dipole (1-15), and summed over all texture heights.

A high spread of deviations between all dipole positions is observed. What can also be clearly observed is the difference in the deviations at the same positions but different orientations, which indicates that the deviation is not only location-dependent but also strongly orientation-dependent. For example, dipoles at position 3 show high deviations for horizontally-1 and vertically oriented dipoles, but very low deviations for horizontally – 2 oriented dipoles. Overall, the smallest deviations for all three orientations can be observed for dipoles at position 8 and 11.

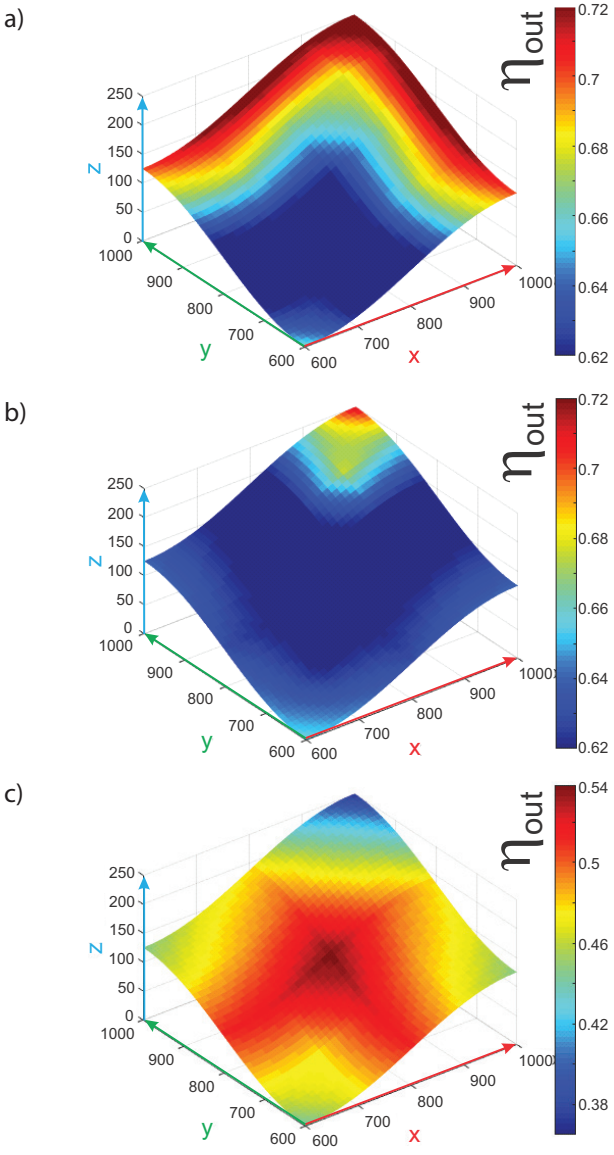


Figure 5: Outcoupling efficiency (color) for different dipole locations on top of a texture (*P* = 800, *h* = 250) for a) horizontally - 1, b) horizontally - 2 and c) vertically oriented dipoles. See Figure 2 for dipole orientation.

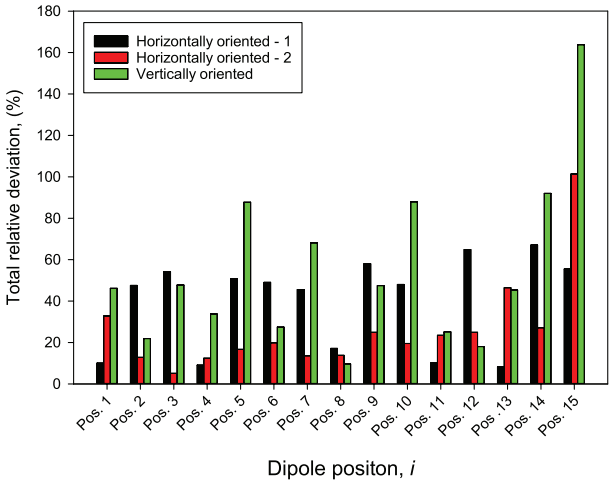


Figure 6: Total relative deviation from weighted average for each dipole and orientation.

Investigation on what is the minimal number of dipoles and what are their locations to approach the results obtained in simulations using 15 dipole locations were done. The first choice would be to take a single dipole position, preferably the dipole at position 8, which generally shows the least deviation from the averaged total data. On the other hand, a single dipole position would theoretically allow us to hit a special location where the results would differ significantly from all others (e.g., constructive or destructive coherence, etc.), so that multiple dipole positions would be preferable. To compare the outcoupling trends, in Figure 4 (d, e, f) the outcoupling for a single dipole at location 8 as the dipole with the smallest total deviation from the weighted average, the combination of the dipoles at locations 8 and 11 as two of the dipoles with the smallest deviation from the weighted average, special case of the combination of dipoles at the locations 7, 8, 11 as the combination of dipoles which are most represented on the geometry, and which are also at center locations, and at the end the combination of dipoles at the locations 6, 8, 13 which show the best agreement with the weighted average over 15 dipole locations are shown. Interestingly, the most representative combination of dipoles was the combination of dipoles at locations 6, 8 and 13, which are also located at central locations but are more widely spread than the dipoles at sites 7, 8 and 11 – see Figure 2. This combination of dipole locations follows weighted data for 15 dipole locations very well. It should be noted that even by simulating a single dipole at location 8 or a combination of other dipole locations, as shown in Figure 4 (d, e, f), a good agreement with general trends

is obtained, albeit with an over- or under- estimation of the actual outcoupling efficiency. These results show that even by simulating a smaller number of carefully selected dipole locations, it is possible to predict outcoupling trends, which greatly reduces the simulation time, although for the most accurate data, as many dipole positions as possible would have to be included in the simulations. On the other hand, it must also be mentioned that not every dipole location or even the combination of two or three dipole locations with the wrong selection (e.g. dipoles at extreme points, symmetry, e.g. no. 1, 5, 15) leads to good results. Not only can these results differ significantly from the actual data, they can also lead to false trends. In Figure 4(d, e, f), vertical lines representing the maximum and minimum output values at each texture height are added, showing high deviations from the actual weighted average, and also different trends for both horizontally oriented dipoles, with maximum output at much higher heights (250 - 300 nm) of the texture than with weighted average (150 - 200 nm). Therefore, three carefully selected dipole positions, preferably in the middle and wide spread, are necessary for a good adaptation to several dipole positions. It should be noted that this study was performed for sine shaped textures, while for other texture shapes other combinations of dipole positions may be more suitable and need to be investigated separately.

3.4 Simulation improvements of outcoupling efficiency due to substrate corrugation

So far only each individual dipole by position and orientation was evaluated, without commenting on the improvement of the outcoupling as a whole. From the presented results it can be observed that with increasing height of the texture outcoupling efficiency also increases and reaches a maximum for horizontally -1 oriented dipoles at the height of 150 nm and for horizontally - 2 oriented dipoles at 200 nm, whereas with even higher heights of the texture outcoupling starts to decrease. For vertically oriented dipoles, the outcoupling efficiency increases with increasing texture height and saturates at heights above 300 nm Thus, the optimal height depends on the actual orientation of the dipoles, with which the ratio between the individual contributions can be determined, that will influence the final output. The actual orientation of the emitter material molecules on corrugated substrates may also differ from that on flat substrates and must be determined and taken into account. The advantage of modelling, where outcoupling efficiency of light is calculated for each orientation separately, is the simple and straightforward possibility to recalculate the final outcoupling to the actual distribution of the dipole orientations without additional simulations by simply weighing each contribution. If we assume for this case that the general orientation of the dipoles does not change (a = 0.24) when deposited on corrugated substrates, the highest *EQE* ($\eta_{ele} = 1, \eta_{rad} = 0.7$) for glass substrate (or for air by using a glass hemisphere) of 47.7% at a texture height of 250 nm can be found, which is more than 25% higher than for flat plane device with 37.6% *EQE* – see Figure 7(b), indicating a high potential of sine corrugated substrates for the outcoupling of light from the OLED thin film structure. Moreover, added is outcoupling efficiency as calculated by using only 3 dipole locations (6, 8, 13), to show almost perfect matching with the simulation results for 15 locations used. In addition, the comparison of the Purcell factor between flat and textured structure (Figure 7(a)) displays only a minimal difference, indicating that texturing does not have a major impact on the microcavity in this case.

It needs to be noted, that optimal texture height of h = 250 nm for P = 800 nm, was determined for a single wavelength at emission peak of 612 nm, while if wavelengths over entire emission spectrum would be included in the optimization process, possibly different height would result in best outcoupling efficiency, thus further optimization would need to be employed.

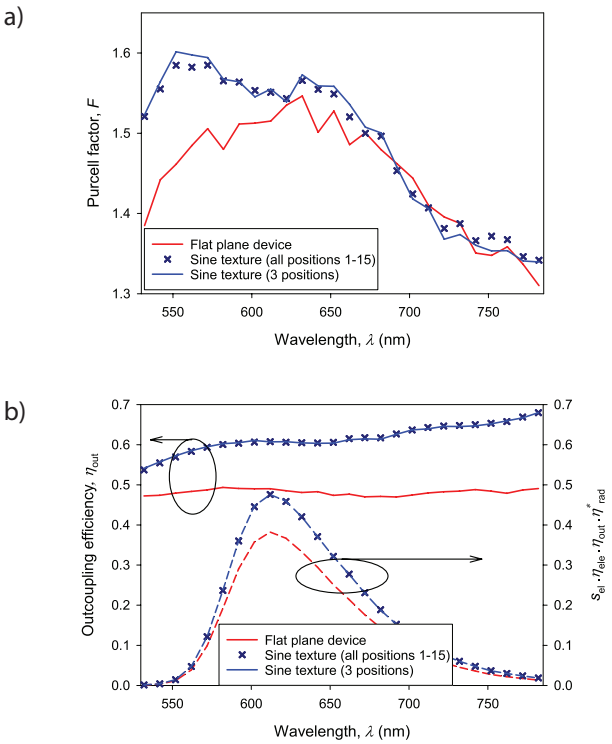


Figure 7: Comparison of simulation results for flat plane OLED and OLED on textured substrate with P = 800 and h = 250 nm. Anisotropy of a = 0.24 is considered for both cases. Added are simulations results for only 3 dipole positions (6, 8, 13). a) Purcell factor – averaged over multiple positions; b) outcoupling efficiency and *EQE* to glass substrate (to air by using a glass hemisphere)

4 Conclusions

A modeling approach based on FEM was presented to research effects of dipole position and orientation on the outcoupling efficiency of red OLED devices with periodically corrugated substrates. High deviations from the averaged outcoupling efficiency for individual positions and orientations of emitter dipoles were revealed, although it is shown that even with a smaller number (three) of carefully selected dipole positions the outcoupling over the wide area of sinusoidal texture height with very reasonable accuracy can be predicted and the number of required simulations reduced by a factor of 5. For an optimal texture, outcoupling tendencies corresponding to texture inclination are shown, with opposite effects for horizontally and vertically oriented dipoles. This shows how important it is to optimize the outcoupling solutions for each specific OLED design, especially for dipole orientation. Finally, a possible 25% improvement in *EQE* (improved outcoupling efficiency) is shown, over flat plane devices by using a sine textured substrate with a period of 800 nm and a height of 250 nm, with the possibility of additional improvements. Modeling and simulations show a high potential for further design and optimization of future outcoupling solutions.

5 Acknowledgments

The author shows appreciation to M. Topič and J. Krč for their valuable suggestions, advices and support in writing this paper. The author acknowledges the financial support from the Slovenian Research Agency (P2-0197 and J2-1727).

6 Conflict of interest

Author declares no conflict of interest.

7 References

1. Y. Chang and Z. Lu, "White Organic Light-Emitting Diodes for Solid-State Lighting," *Journal of Display Technology*, vol. 9, no. 6, pp. 459–468, Jun. 2013, https://doi.org/10.1109/JDT.2013.2248698.
2. S. Reineke, "Complementary LED technologies," *Nature Materials*, vol. 14, no. 5, Art. no. 5, May 2015, https://doi.org/10.1038/nmat4277.
3. S. Reineke, M. Thomschke, B. Lüssem, and K. Leo, "White organic light-emitting diodes: Status and perspective," *Rev. Mod. Phys.*, vol. 85, no. 3, pp. 1245–1293, Jul. 2013, https://doi.org/10.1103/RevModPhys.85.1245.
4. J. Song, H. Lee, E. G. Jeong, K. C. Choi, and S. Yoo, "Organic Light-Emitting Diodes: Pushing Toward the Limits and Beyond," *Advanced Materials*, vol. 32, no. 35, p. 1907539, 2020, doi: https://doi.org/10.1002/adma.201907539.
5. Y. Yin, M. U. Ali, W. Xie, H. Yang, and H. Meng, "Evolution of white organic light-emitting devices: from academic research to lighting and display applications," *Mater. Chem. Front.*, vol. 3, no. 6, pp. 970–1031, May 2019, https://doi.org/10.1039/C9QM00042A.
6. L. Xiao, S.-J. Su, Y. Agata, H. Lan, and J. Kido, "Nearly 100% Internal Quantum Efficiency in an Organic Blue-Light Electrophosphorescent Device Using a Weak Electron Transporting Material with a Wide Energy Gap," *Advanced Materials*, vol. 21, no. 12, pp. 1271–1274, 2009, https://doi.org/10.1002/adma.200802034.
7. D. Volz, "Review of organic light-emitting diodes with thermally activated delayed fluorescence emitters for energy-efficient sustainable light sources and displays," *JPE*, vol. 6, no. 2, p. 020901, Apr. 2016, https://doi.org/10.1117/1.JPE.6.020901.
8. Z. Yang *et al.*, "Recent advances in organic thermally activated delayed fluorescence materials," *Chem. Soc. Rev.*, vol. 46, no. 3, pp. 915–1016, Feb. 2017, https://doi.org/10.1039/C6CS00368K.
9. S. R. Forrest, D. D. C. Bradley, and M. E. Thompson, "Measuring the Efficiency of Organic Light-Emitting Devices," *Advanced Materials*, vol. 15, no. 13, pp. 1043–1048, 2003, doi: https://doi.org/10.1002/adma.200302151.
10. R. Meerheim, M. Furno, S. Hofmann, B. Lüssem, and K. Leo, "Quantification of energy loss mechanisms in organic light-emitting diodes," *Appl. Phys. Lett.*, vol. 97, no. 25, p. 253305, Dec. 2010, https://doi.org/10.1063/1.3527936.
11. M. C. Gather and S. Reineke, "Recent advances in light outcoupling from white organic light-emitting diodes," *JPE*, vol. 5, no. 1, p. 057607, May 2015, https://doi.org/10.1117/1.JPE.5.057607.
12. A. Salehi, X. Fu, D.-H. Shin, and F. So, "Recent Advances in OLED Optical Design," *Advanced Functional Materials*, vol. 29, no. 15, p. 1808803, 2019, https://doi.org/10.1002/adfm.201808803.
13. S. Möller and S. R. Forrest, "Improved light outcoupling in organic light emitting diodes employing ordered microlens arrays," *Journal of Applied*

Physics, vol. 91, no. 5, pp. 3324–3327, Feb. 2002, https://doi.org/10.1063/1.1435422.

14. H. Greiner, "Light Extraction from Organic Light Emitting Diode Substrates: Simulation and Experiment," *Jpn. J. Appl. Phys.*, vol. 46, no. 7R, p. 4125, Jul. 2007, https://doi.org/10.1143/JJAP.46.4125.
15. H. Bae, J. S. Kim, and C. Hong, "Simulation for light extraction efficiency of OLEDs with spheroidal microlenses in hexagonal array," *Optics Communications*, vol. 415, pp. 168–176, May 2018, https://doi.org/10.1016/j.optcom.2018.01.044.
16. M. Kovačič *et al.*, "Combined optical model for micro-structured organic light emitting diodes," *Informacije MIDEM*, vol. 46, no. 4, Art. no. 4, Jan. 2017.
17. M. Kovačič *et al.*, "Coupled Optical Modeling for Optimization of Organic Light-Emitting Diodes with External Outcoupling Structures," *ACS Photonics*, vol. 5, no. 2, pp. 422–430, Feb. 2018, https://doi.org/10.1021/acsphotonics.7b00874.
18. A. Gasonoo *et al.*, "Outcoupling efficiency enhancement of a bottom-emitting OLED with a visible parylene film," *Opt. Express, OE*, vol. 28, no. 18, pp. 26724–26732, Aug. 2020, https://doi.org/10.1364/OE.397789.
19. J.-H. Yen, Y.-J. Wang, C.-A. Hsieh, Y.-C. Chen, and L.-Y. Chen, "Enhanced light extraction from organic light-emitting devices through non-covalent or covalent polyimide–silica light scattering hybrid films," *J. Mater. Chem. C*, vol. 8, no. 12, pp. 4102–4111, Mar. 2020, https://doi.org/10.1039/C9TC06449D.
20. E. Wrzesniewski *et al.*, "Enhancing Light Extraction in Top-Emitting Organic Light-Emitting Devices Using Molded Transparent Polymer Microlens Arrays," *Small*, vol. 8, no. 17, pp. 2647–2651, 2012, https://doi.org/10.1002/smll.201102662.
21. H.-W. Chang *et al.*, "Nano-particle based scattering layers for optical efficiency enhancement of organic light-emitting diodes and organic solar cells," *Journal of Applied Physics*, vol. 113, no. 20, p. 204502, May 2013, https://doi.org/10.1063/1.4807000.
22. Y. Li *et al.*, "Tailor-made nanostructures bridging chaos and order for highly efficient white organic light-emitting diodes," *Nature Communications*, vol. 10, no. 1, p. 2972, Jul. 2019, https://doi.org/10.1038/s41467-019-11032-z.
23. H. Liang *et al.*, "Corrugated organic light-emitting diodes to effectively extract internal modes," *Opt. Express, OE*, vol. 27, no. 8, pp. A372–A384, Apr. 2019, https://doi.org/10.1364/OE.27.00A372.
24. Y. Sun and S. R. Forrest, "Enhanced light out-coupling of organic light-emitting devices using embedded low-index grids," *Nature Photonics*, vol. 2, no. 8, Art. no. 8, Aug. 2008, https://doi.org/10.1038/nphoton.2008.132.
25. Y. Qu, C. Coburn, D. Fan, and S. R. Forrest, "Elimination of Plasmon Losses and Enhanced Light Extraction of Top-Emitting Organic Light-Emitting Devices Using a Reflective Subelectrode Grid," *ACS Photonics*, vol. 4, no. 2, pp. 363–368, Feb. 2017, doi: 10.1021/acsphotonics.6b00847.
26. D. Riedel, T. Wehlus, T. C. G. Reusch, and C. J. Brabec, "Polymer-based scattering layers for internal light extraction from organic light emitting diodes," *Organic Electronics*, vol. 32, pp. 27–33, May 2016, https://doi.org/10.1016/j.orgel.2016.02.004.
27. J.-M. Jin, *The Finite Element Method in Electromagnetics*. John Wiley & Sons, 2015.
28. M. Furno, R. Meerheim, M. Thomschke, S. Hofmann, B. Lüssem, and K. Leo, "Outcoupling efficiency in small-molecule OLEDs: from theory to experiment," in *Light-Emitting Diodes: Materials, Devices, and Applications for Solid State Lighting XIV*, Feb. 2010, vol. 7617, p. 761716, https://doi.org/10.1117/12.840043.
29. K. A. Neyts, "Simulation of light emission from thin-film microcavities," *J. Opt. Soc. Am. A, JOSAA*, vol. 15, no. 4, pp. 962–971, Apr. 1998, https://doi.org/10.1364/JOSAA.15.000962.
30. "The COMSOL® Software Product Suite," *COMSOL Multiphysics®*. https://www.comsol.com/products (accessed Jul. 17, 2019).
31. "Simulating Plasmon Effects in Nano-Structured OLED Cathodes Using COMSOL Multiphysics® Software." https://www.comsol.com/paper/simulating-plasmon-effects-in-nano-structured-oled-cathodes-using-comsol-multiph-27012 (accessed Nov. 11, 2020).
32. L. Zschiedrich, H. J. Greiner, S. Burger, and F. Schmidt, "Numerical analysis of nanostructures for enhanced light extraction from OLEDs," in *Light-Emitting Diodes: Materials, Devices, and Applications for Solid State Lighting XVII*, Mar. 2013, vol. 8641, p. 86410B, https://doi.org/10.1117/12.2001132.
33. L. Zschiedrich, T. Blome, and H. J. Greiner, "Simulation of advanced OLED light extraction structures

with novel FEM methods," in *Organic Photonics VI*, May 2014, vol. 9137, p. 91370O, https://doi.org/10.1117/12.2054146.

34. R. J. Potton, "Reciprocity in optics," *Rep. Prog. Phys.*, vol. 67, no. 5, p. 717, Apr. 2004, https://doi.org/10.1088/0034-4885/67/5/R03.
35. S. Zhang, E. R. Martins, A. G. Diyaf, J. I. B. Wilson, G. A. Turnbull, and I. D. W. Samuel, "Calculation of the emission power distribution of microstructured OLEDs using the reciprocity theorem," *Synthetic Metals*, vol. 205, pp. 127–133, Jul. 2015, https://doi.org/10.1016/j.synthmet.2015.03.035.
36. M. Sever *et al.*, "Combined model of non-conformal layer growth for accurate optical simulation of thin-film silicon solar cells," *Solar Energy Materials and Solar Cells*, vol. 119, pp. 59–66, Dec. 2013, https://doi.org/10.1016/j.solmat.2013.05.016.

Arrived: 11.11.2020
Accepted: 16.03.2021

Original scientific paper
https://doi.org/10.33180/InfMIDEM2021.106

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 51, No. 1(2021), 85 – 94

Practical Floating Capacitance Multiplier Implementation with Commercially Available IC LT1228s

*Natchanai Roongmuanpha, Worapong Tangsrirat**

School of Engineering, King Mongkut's Institute of Technology Ladkrabang (KMITL), Bangkok, Thailand

Abstract: A practical realization of a tunable floating capacitance multiplier using commercially available integrated circuits, namely LT1228 is proposed. The synthetic capacitor utilizes only two IC LT1228s along with two passive components (one resistor and one capacitor). The capacitance multiplication factor is electronically controllable through the transconductance gain of the LT1228. The effects of non-ideal transfer gains and parasitic elements of the LT1228 on the circuit performance have been evaluated in detail. The applicability of the proposed floating capacitance multiplier as a second-order band-pass filter is also presented. The claimed theory is verified by several PSPICE simulations and experimental test results.

Keywords: capacitance multiplier; impedance simulation circuit; commercially available integrated circuit; electronically tunable

Praktična uporaba množilnika plavajoče kapacitivnosti s komercialnim IC LT1228s

Izvleček: Predstavljena je praktična uporaba nastavljivega množilnika plavajoče kapacitivnosti z uporabo komercialnega integriranega vezja LT1228. Sintetičen kondenzator uporablja le dva IC LT1228 in dva pasivna elementa (upor in kondenzator). Faktor množenja je elektronsko nastavljiv s transkonduktančnim ojačenjem LT1228. Natančno so opredeljeni prenosi neidealnih ojačenj parazitnih elementov. Uporabnost množilnika je prikazana na pasovnem filtru drugega reda. Teorija je verificirana v PSPICE simulatorju in z eksperimentalnimi testi.

Ključne besede: kapacitetni množilnik; impedančno simulacijsko vezje; komercialno integrirano vezje; elektronska nastavljivost

* *Corresponding Author's e-mail: drworapong@gmail.com*

1 Introduction

It is well known that the capacitance multiplier is a significant electronic block in the fabrication of high capacitance values in integrated circuit (IC) technology [1]-[2]. This is due to the large-value capacitors requiring a large silicon area on the IC chip. To overcome this limiting problem, the capacitance multiplier circuit which performs the multiplication of small capacitance values can be very useful [3]-[4]. Therefore, the design of capacitance multiplier circuits becomes an essential research issue in the area of analog ICs. Over the years, there are various floating capacitance multiplier circuits reported by several researchers employing numerous versatile active elements [5]-[13]. However, careful observation of the topologies reported in these references reveals that they still suffer from one or more of the following restrictions:

1. They contain three or more active components [5]-[6], [10], [12], which enlarge the area on the chip, and relatively high power dissipation.
2. They need to employ more than two passive components [7], [9]-[10].
3. They are unavailable in commercial IC form [6]-[9], [11]-[12], which cannot be practically implemented using already existing readily available ICs.
4. They lack the electronic adjustability for the capacitance multiplying factor [7], [9]-[10]. The in-

ternal tuning feature would be desirable for modern mixed-signal systems.

5. They use different types of active components for their implementations [5], [12]-[13].

The attention aim of this work is, therefore, to design a floating and tunable capacitance multiplier using already existing commercially available ICs, namely LT1228 [14]. The LT1228 structure internally consists of an operational transconductance amplifier (OTA) and a current feedback operational amplifier (CFOA) in the same IC package. Thus, it may be noted that LT1228 has now become a popular commercial IC for designing several types of analog signal processing circuits and applications [15]-[20]. Two LT1228s and two passive components, i.e. one resistor and one capacitor, are employed in this design. The capacitance scaling factor of the simulated circuit can be altered through the tunable transconductance gains of the LT1228s and/or the resistor in the circuit. A careful non-ideality analysis for the proposed capacitance multiplier circuit is investigated in detail. The second-order RLC band-pass filter implemented with the proposed tunable active capacitance simulator is given as an application. To verify the workability of the proposed circuit, it has been simulated in the PSPICE program using macro-model of IC LT1228, and also experimentally tested in a laboratory using commercially available IC namely LT1228s.

2 Circuit description

2.1 Commercially available IC LT1228

The LT1228 is a commercially available IC manufactured by Linear Technology Corporation [14]. The LT1228 internal circuit, which has the properties of both the operational transconductance amplifier (OTA) and the current feedback operational amplifier (CFOA), is shown in Fig.1(a). The OTA provides an electronic gain control with a differential voltage-to-current converter, whose transconductance gain (g_m) depends on an external bias current, while the CFOA is implemented to drive load low-impedance loads with excellent linearity at high frequencies. The circuit representation block of the LT1228 and its equivalent circuit are given in Fig.1(b) and 1(c), respectively. In ideal operation, the function of the LT1228 can be described by the following matrix relation:

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ v_x \\ v_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & R_{OL} & 0 \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \\ i_x \\ i_o \end{bmatrix} \quad (1)$$

In equation (1), R_{OL} is the transresistance gain of the LT1228, which is ideally considered to be infinite. The g_m-parameter of this IC can be adaptable electronically with the help of the external bias current I_B and the expression is given by:

$$g_m = 10 I_B \quad (2)$$

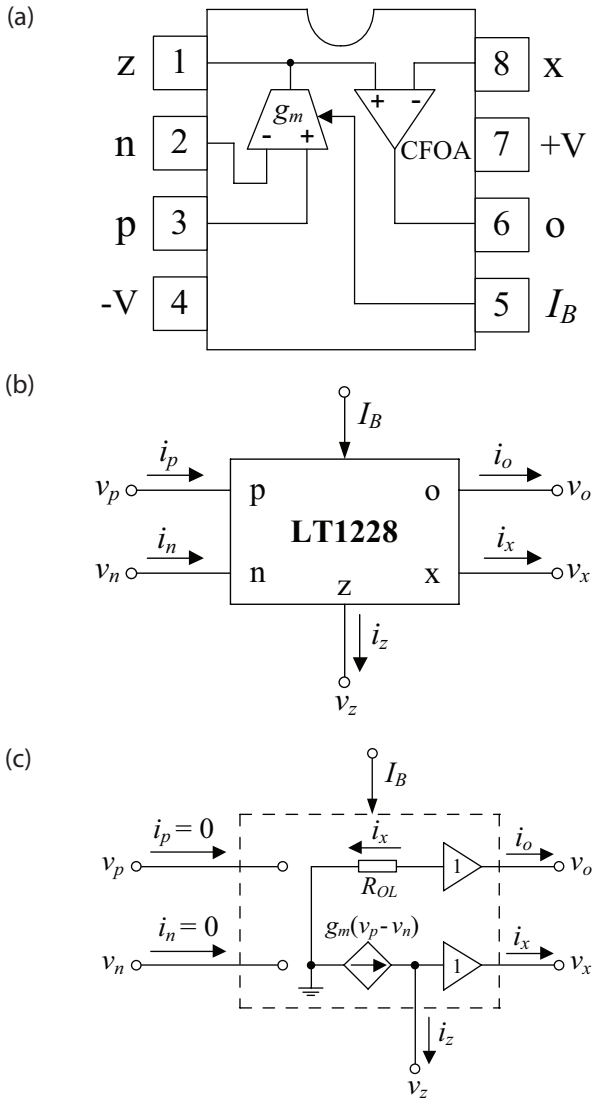


Figure 1: Commercially available IC LT1228: (a) package information; (b) electrical symbol; (c) equivalent circuit

2.2 Proposed floating capacitance multiplier design

The schematic diagram of the proposed floating capacitance multiplier circuit is given in Fig.2(a). It is composed of only two LT1228s, one resistor, and one capacitor. The equivalent circuit for the proposed capacitor implementation of Fig.2(a) is shown in Fig.2(b). Assuming that the matching condition of $g_m = g_{m1} = g_{m2}$ is satisfied, routing circuit analysis shows that the equivalent

input impedance looking between ports v_1 and v_2 of the proposed circuit in Fig.2(a) can be obtained as:

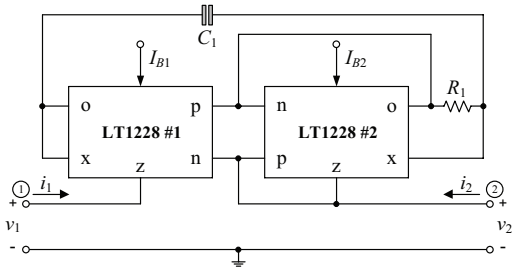
$$Z_{eq} = \frac{v_{id}}{i_{in}} = \left(\frac{v_1 - v_2}{i_1}\right) = \left(\frac{v_2 - v_1}{i_2}\right) = \frac{1}{sC_{eq}} = \frac{1}{s(g_m R_1 C_1)} \quad (3)$$

It is obvious that the proposed circuit of Fig.2(a) implements a floating tunable lossless capacitance with equivalent capacitance being given by:

$$C_{eq} = (g_m R_1) C_1 = K C_1 \quad (4)$$

where $K = g_m R_1$ represents the capacitance multiplication factor. The relation in (4) reveals that the capacitance magnification with a large multiplication factor is easily feasible by appropriate choosing g_m and/or R_1. Also from equation (2), the electronic tuning capability of the proposed design is evident through the bias currents of the LT1228s. It should be further noted here that two transconductance gains for this implementation need to be equal. This can be done easily by using simple current mirror to supply equal external bias currents to the two LT1228s.

(a)



(b)

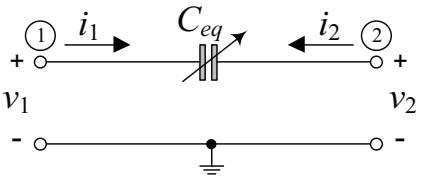


Figure 2: Proposed floating capacitance multiplier implementation: (a) circuit diagram; (b) ideal equivalent impedance

2.3 Non-ideality performance analysis

Consider the non-ideal transfer gains of the LT1228, the characteristic of the LT1228 given in equation (1) can be re-described by the following matrix equation:

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ v_x \\ v_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \alpha g_m & -\alpha g_m & 0 & 0 & 0 \\ 0 & 0 & \beta & 0 & 0 \\ 0 & 0 & 0 & R_{OL} & 0 \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \\ i_x \\ i_o \end{bmatrix} \quad (5)$$

In above equation, $\alpha = (1 - \varepsilon_{gm})$ and $\beta = (1 - \varepsilon_v)$, where $|\varepsilon_{gm}| << 1$ and $|\varepsilon_v| << 1$ are the transconductance tracking error and the voltage transfer error, respectively. Therefore, an analysis of the simulator given Fig.2(a) with the consideration of these parasitic gains gives the following expression for the equivalent input impedance looking into port 1 and ground as:

$$Z'_{eq1} = \left.\frac{v_1}{i_1}\right|_{v_2=0} = \frac{1}{sC'_{eq1}} = \frac{1}{s(g_{m1} R_1 C_1)(\alpha_1 \beta_1)} \quad (6)$$

It is obvious that the parasitic gains α_1 and β_1 directly deviate the value of the working capacitance C_1. To compensate for this, it can be governed by tuning the appropriate value for the $g_{m1}R_1$ product. On the other hand, the non-ideal equivalent impedance looking into port 2 and ground can be approximately found as:

$$Z'_{eq2} = \left.\frac{v_2}{i_2}\right|_{v_1=0} = \frac{1}{sC'_{eq2} + \left(\frac{1}{R'_{ex}}\right)} = \frac{1}{s(R_1 C_1 \beta_2)(g_{m2}\alpha_2) + (\beta_2 - 1)(g_{m2}\alpha_2)} \quad (7)$$

From equation (7), due to the LT1228 non-ideal gains, there is an extra undesired parallel resistance (R'_{ex}) appearing in parallel with the non-ideal equivalent capacitance. The non-ideal equivalent circuit for this case can then be represented as in Fig.3, where $C'_{eq2} = (R_1 C_1 \beta_2)(g_{m2}\alpha_2)$ and $R'_{ex} = 1/(\beta_2\text{-}1)(g_{m2}\alpha_2)$. Since a typical value of R'_{ex} is of the order of hundreds of kΩ, the parasitic elements C'_{eq2} and R'_{ex} introduce an extra pole at low frequency, which restricts the operating frequency range of the circuit. This effect on the frequency response of Z'_{eq2} will be shown in the following section.

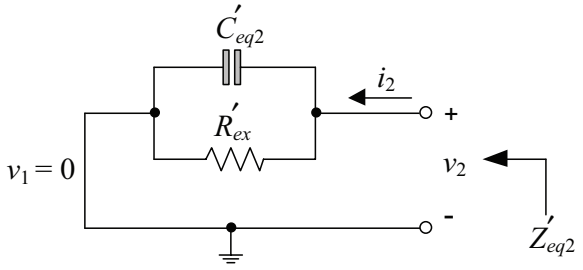


Figure 3: Non-ideal equivalent input impedance Z'_{eq2}.

In practice, if the parasitic impedances at the corresponding LT1228 terminals are taken into account, then the practical circuit model of the LT1228 can be drawn in Fig.4. At terminals p, n and z, there are the parasitic resistances R_p, R_n, and R_z appearing respectively in parallel with the parasitic capacitances C_p, C_n, and C_z. Their

impedance values are theoretically equal to infinity. On the other hand, the parasitic resistance R_x appears in series at terminal x. By considering $v_2 = 0$, the impedance of the designed capacitor with the consideration of the parasitic element effects can be given by:

$$Z''_{eq1} = \frac{v_1}{i_1}\bigg|_{v_2=0} = \frac{1}{sC''_{eq1}} = \frac{1}{s\left[\frac{g_{m1}R_1C_1}{1+\left(\frac{R_{x1}}{R_{OL1}}\right)} - C_{z1}\right] - \left(\frac{1}{R_{z1}}\right)} \quad (8)$$

where R_{OLi}, R_{xi}, R_{zi}, and C_{zi} (i = 1, 2) are the parasitic elements R_{OL}, R_x, R_z, and C_z of the i-th LT1228, respectively. For practical realization, R_{OL1} and R_{z1} are typically very large, yielding $R_{OL1} >> R_{x1}$ and $R_{z1} >> 1$. Therefore, an equivalent capacitance $C''_{eq1} \cong (g_{m1}R_1C_1 - C_{z1})$ is obtained from equation (8). It is further mentioned that there is not any additional parasitic pole and zero due to the parasitic elements, and the operating frequency limitation can be expressed as: $f \leq \min [1/2\pi(g_{m1}R_1C_1 - C_{z1})]$.

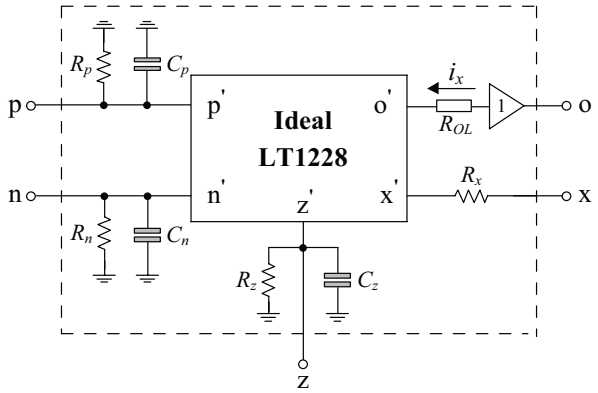


Figure 4: Practical LT1228 model with parasitic elements.

By defining $v_1 = 0$ and conducting relevant analyses, we can obtain the following expression for the non-ideal impedance seen between terminal 2 and ground as:

$$Z''_{eq2} = \frac{v_2}{i_2}\bigg|_{v_1=0} = \frac{1}{sC''_{eq2}} = \frac{1}{s\left[\frac{g_{m2}R_1C_1}{1+\left(\frac{R_{x2}}{R_{OL2}}\right)} - C''_2\right] - \left[\frac{g_{m2}}{1+\left(\frac{R_{OL2}}{R_{x2}}\right)} + \frac{1}{R''_2}\right]} \quad (9)$$

)

where $R''_2 = R_{n1}//R_{p2}//R_{z2}$ and $C''_2 = C_{n1}+C_{p2}+C_{z2}$. In equation (9), the negative terms exhibit non-ideal behavior of the proposed capacitance simulator by introducing a parallel resistive effect. Since $R_{OL2} >> R_{x2}$ and $R''_2 >> 1$, then equation (9) reduces to

$$Z''_{eq2} = \frac{1}{sC''_{eq2}} \cong \frac{1}{s\left[\frac{g_{m2}R_1C_1}{1+\left(\frac{R_{x2}}{R_{OL2}}\right)} - C''_2\right]} \quad (10)$$

The consideration of the above effect implies that in the frequency range of $f \leq \min [1/2\pi(g_{m2}R_1C_1 - C''_2)]$, and the inequality $g_{m2}R_1C_1 << C''_2$, the simulator operates practically as an expected ideal capacitance multiplier.

3 Computer simulation validation

To verify our proposed design, the circuit in Fig.2(a) has been simulated in PSPICE program using the macromodel parameters for the LT1228 provided by Linear Technology Corporation [14], with DC supply voltages of ±5 V. In simulations, the component values are taken as: R_1 = 1 kΩ, C_1 = 50 pF and $I_B = I_{B1} = I_{B2}$ = 200 µA. From equation (2), the transconductance gains are calculated as: $g_m = g_{m1} = g_{m2}$ = 2 mA/V. Also, from the relation in (4), the capacitance multiplication factor, and the simulated equivalent capacitance are calculated as: K = 2 and C_{eq} = 0.1 nF, respectively. The simulation results for input signals v_{id} and i_{in} of the proposed capacitance multiplier are given in Fig.5, when a 1-MHz sinusoidal signal of an amplitude 50 mV (peak) was applied as an input signal. The phase difference between v_{id} and i_{in} was observed to be 86.77° leading, as against the theoretical value of 90°. The corresponding frequency responses are also given in Fig.6. The total power consumption is measured to be 0.12 W when v_1 and v_2 are kept grounded.

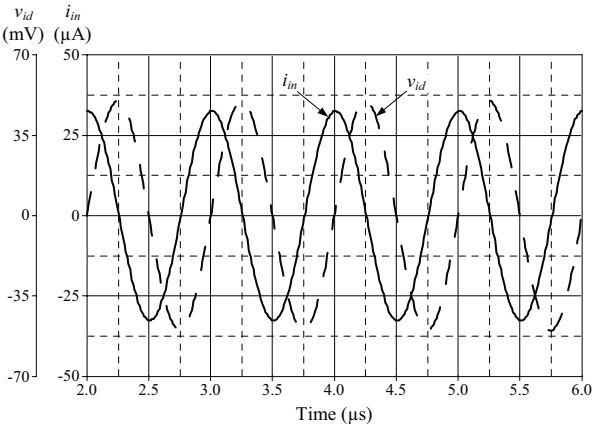


Figure 5: Simulation results for v_{id} and i_{in} of the proposed floating capacitance multiplier circuit in Fig.2(a).

In order to evaluate the impact of the unwanted parasitic resistance R'_{ex} the frequency responses of the non-

ideal equivalent impedance Z'_{eq2} ($Z'_{eq2} = v_2/i_2$) when v_1 =0 are depicted in Fig.7. It is observed that, at low frequency range between 1 kHz and 20 kHz, R'_{ex} mainly causes drop of the magnitude response of the Z'_{eq2} and also some deviates in phase response as depicted. However, some circuit techniques which reduce the parasitic impedance effects can be applied in the proposed capacitance multiplier circuit to improve the frequency performance [21]-[23].

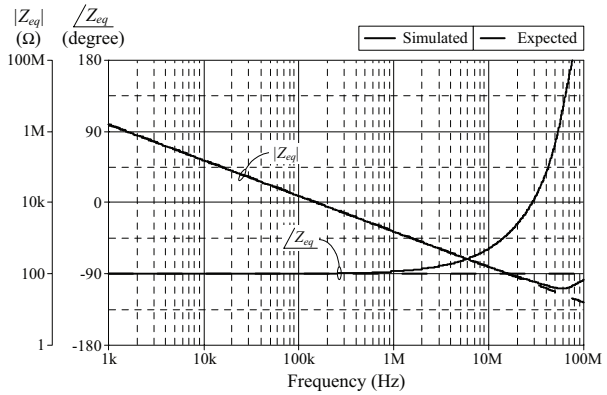


Figure 6: Expected and simulated frequency responses of the proposed floating capacitance multiplier circuit in Fig.2(a).

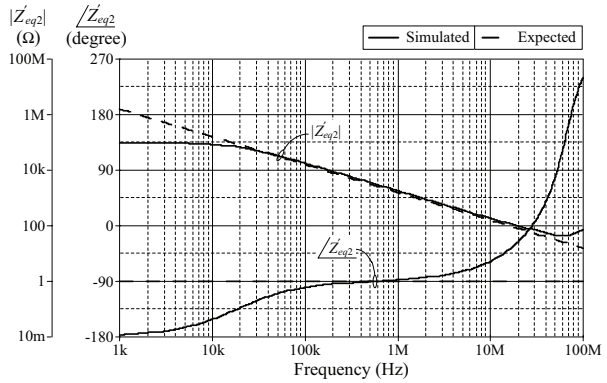


Figure 7: Frequency responses of the non-ideal equivalent input impedance Z'_{eq2} in Fig.3.

The adjustability of the proposed capacitance multiplier circuit is assessed by tuning the capacitance multiplication factor ($K = g_m R_1$), and also shown in Fig.8. Variations of C_{eq} against g_m and R_1 are demonstrated as examples. The C_{eq} tuning with g_m (varied from 0.1 mA/V to 10 mA/V) while keeping R_1 constant at 20 kΩ is shown in Fig.8(a), whereas the results in Fig.8(b) are obtained by setting g_m fixed at 10 mA/V and varying R_1 from 0.5 kΩ to 20 kΩ. It is evident from the results that the simulated capacitance value C_{eq} can enhance up to approximately 200 times with the maximum error in all cases less than 10%.

Fig.9 shows the temperature analysis results of the proposed capacitance multiplier circuit in Fig.2(a), where the ambient temperature is changed from 0°C to 100°C in the step of 20°C. From Fig.9, the simulation results demonstrate that the magnitude response has deviated with a variation of -8% ~ +22% over the temperature range of 0°C to 100°C.

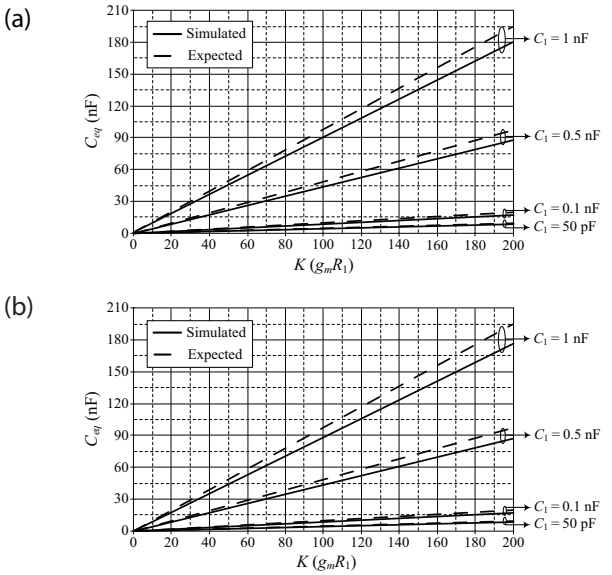


Figure 8: Variation of C_{eq} with the multiplication factor ($K = g_m R_1$): (a) g_m = 0.1 mA/V to 10 mA/V (I_B = 10 µA to 1000 µA) and R_1 = 20 kΩ; (b) g_m = 10 mA/V (I_B = 1000 µA) and R_1 = 0.5 kΩ to 20 kΩ

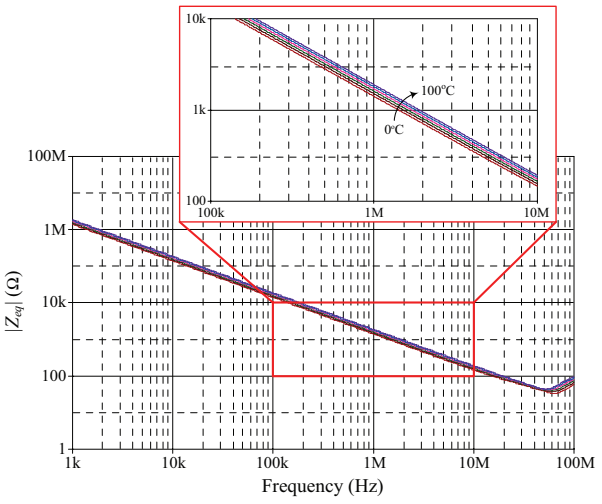


Figure 9: Temperature analysis results of the proposed floating capacitance multiplier circuit in Fig.2(a).

4 Experimental Evaluation

In the experimental evaluation, the availability of the proposed floating capacitance multiplier circuit in

Fig.2(a) has been verified in the laboratory using off-shelf IC's LT1228 [14] under ±5V supply voltages. All experimental measurements were performed through Keysight EDU-X 1002G oscilloscope and HP4395A impedance analyzer. To perform the experimental test, the components used have been: g_m = 2 mA/V (I_B = 200 µA), R_1 = 1 kΩ, and C_1 = 50 pF, yielding C_{eq} = 0.1 nF. Fig.10 shows the measured input waveforms v_{id} and i_{in} of the proposed circuit in Fig.2(a), when the input signal is 100 mV peak-to-peak at 1 MHz. The phase shift between v_{id} and i_{in} obtained from this experiment is measured as 86.8°. The corresponding frequency responses of the equivalent input impedance Z_{eq} are also represented in Fig.11. It appears from Figs.10 and 11 that the proposed circuit behaves as a lossless capacitor as expected.

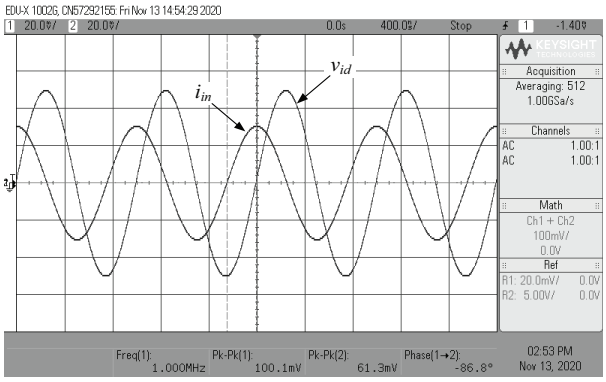


Figure 10: Measured time-domain behavior of the proposed floating capacitance multiplier circuit in Fig.2(a).

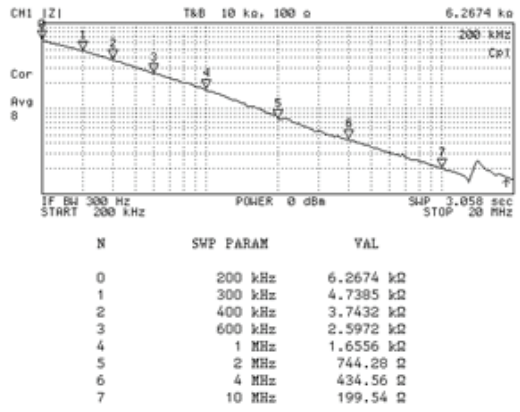
So as to survey the electronic tunability of the capacitance multiplier circuit, the measured magnitude and phase responses with three different values of g_m (i.e. g_m = 0.5 mA/V, 3 mA/V, and 5 mA/V) are shown in Fig.12. These results were obtained by taking R_1 = 1 kΩ and C_1 = 50 pF. This tuning process leads to obtain K = 0.5, 3 and 5 (C_{eq} = 25 pF, 0.15 nF, and 0.25 nF), respectively.

On the other hand, the magnitude-frequency responses of Z_{eq} for different values of R_1 are depicted in Fig.13. In Fig.13, setting g_m = 1 mA/V and C_1 = 50 pF, and different values for R_1 as 5 kΩ, 10 kΩ and 20 kΩ, results in the theoretical equivalent capacitances of C_{eq} = 0.25 nF, 0.5 nF, and 1 nF, respectively.

5 Illustrative application

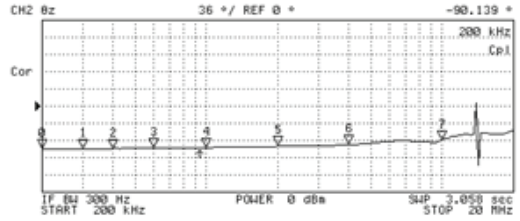
In this section, illustrative applicability of the proposed floating capacitance multiplier given in Fig.2(a) has been considered. It may be utilized in the implementation of the second-order RLC voltage-mode band-pass

(a)



N	SWP PARAM	VAL
0	200 kHz	6.2674 kΩ
1	300 kHz	4.7385 kΩ
2	400 kHz	3.7432 kΩ
3	600 kHz	2.5972 kΩ
4	1 MHz	1.6556 kΩ
5	2 MHz	744.28 Ω
6	4 MHz	434.56 Ω
7	10 MHz	199.54 Ω

(b)



N	SWP PARAM	VAL
0	200 kHz	-90.139 °
1	300 kHz	-89.404 °
2	400 kHz	-88.955 °
3	600 kHz	-88.053 °
4	1 MHz	-86.797 °
5	2 MHz	-84.349 °
6	4 MHz	-81.167 °
7	10 MHz	-71.401 °

Figure 11: Measured frequency behavior of the proposed floating capacitance multiplier circuit in Fig.2(a). (a) magnitude behavior ($|Z_{eq}|$); (b) phase behavior ($\angle Z_{eq}$)

(BP) filter as shown in Fig.14. The transfer function of the filter can be given by:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\left(\frac{R_{BP}}{L_{BP}}\right)s}{s^2 + \left(\frac{R_{BP}}{L_{BP}}\right)s + \left(\frac{1}{L_{BP}C_{eq}}\right)} \tag{11}$$

The center frequency (ω_c) and the quality factor (Q) are respectively expressed below:

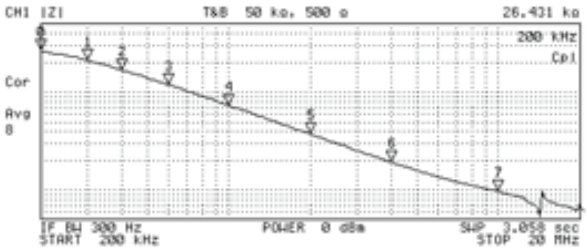
$$\omega_c = 2\pi f_c = \frac{1}{\sqrt{L_{BP}C_{eq}}} \tag{12}$$

and

$$Q = \left(\frac{1}{R_{BP}}\right)\sqrt{\frac{L_{BP}}{C_{eq}}} \tag{13}$$

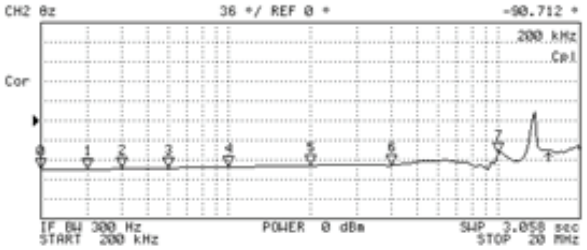
As an example for the circuit simulation, the following passive and active components were chosen as: R_{BP} = 3.3 kΩ, L_{BP} = 1 mH, and C_{eq} = 0.1 nF (g_m = 2 mA/V, R_1 = 1

Magnitude response



N	SWP PARAM	VAL
0	200 kHz	26.431 kΩ
1	300 kHz	22.523 kΩ
2	400 kHz	16.875 kΩ
3	600 kHz	11.838 kΩ
4	1 MHz	7.3235 kΩ
5	2 MHz	3.7322 kΩ
6	4 MHz	1.9232 kΩ
7	10 MHz	964.2 Ω

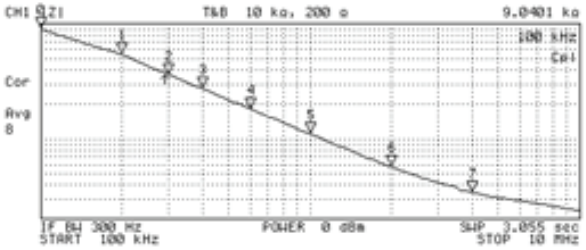
Phase response



N	SWP PARAM	VAL
0	200 kHz	-90.712 °
1	300 kHz	-89.632 °
2	400 kHz	-88.507 °
3	600 kHz	-86.948 °
4	1 MHz	-85.231 °
5	2 MHz	-82.577 °
6	4 MHz	-83.156 °
7	10 MHz	-61.257 °

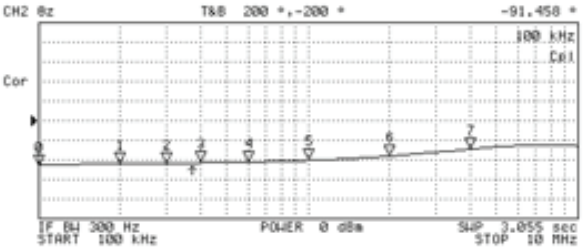
(a)

Magnitude response



N	SWP PARAM	VAL
0	100 kHz	9.0401 kΩ
1	200 kHz	5.4065 kΩ
2	300 kHz	3.6174 kΩ
3	400 kHz	2.7185 kΩ
4	600 kHz	1.818 kΩ
5	1 MHz	1.0969 kΩ
6	2 MHz	568.71 Ω
7	4 MHz	339.95 Ω

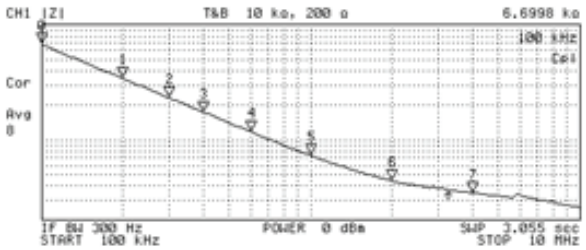
Phase response



N	SWP PARAM	VAL
0	100 kHz	-91.458 °
1	200 kHz	-87.653 °
2	300 kHz	-87.022 °
3	400 kHz	-86.241 °
4	600 kHz	-84.588 °
5	1 MHz	-81.155 °
6	2 MHz	-72.427 °
7	4 MHz	-57.8 °

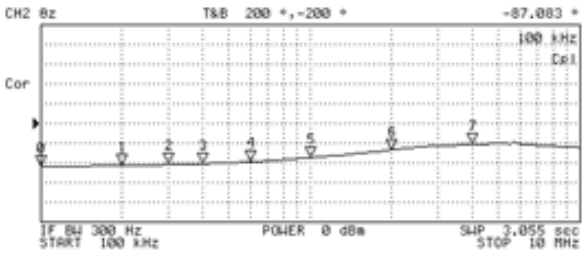
(b)

Magnitude response



N	SWP PARAM	VAL
0	100 kHz	6.6998 kΩ
1	200 kHz	3.4039 kΩ
2	300 kHz	2.2913 kΩ
3	400 kHz	1.7308 kΩ
4	600 kHz	1.1679 kΩ
5	1 MHz	728.97 Ω
6	2 MHz	438.58 Ω
7	4 MHz	342.88 Ω

Phase response

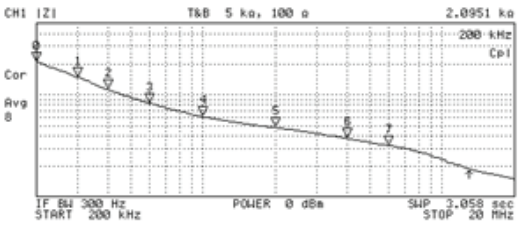


N	SWP PARAM	VAL
0	100 kHz	-87.083 °
1	200 kHz	-85.402 °
2	300 kHz	-83.531 °
3	400 kHz	-81.618 °
4	600 kHz	-77.721 °
5	1 MHz	-69.601 °
6	2 MHz	-53.82 °
7	4 MHz	-42.191 °

(c)

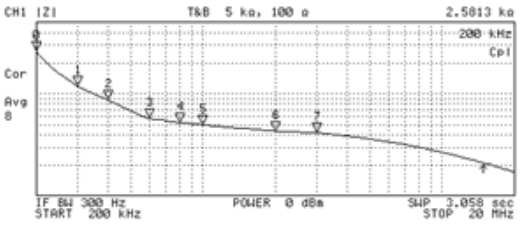
Figure 12: Measured frequency responses of Z_{eq} for different g_m.(a) g_m = 0.5 mA/V (K = 0.5, C_{eq} = 25 pF); (b) g_m = 3 mA/V (K = 3, C_{eq} = 0.15 nF); (c) g_m = 5 mA/V (K = 5, C_{eq} = 0.25 nF)

(a)



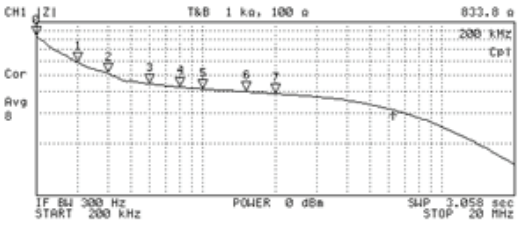
N	SWP PARAM	VAL
0	200 kHz	2.0951 kΩ
1	300 kHz	1.4825 kΩ
2	400 kHz	1.1176 kΩ
3	600 kHz	819.72 Ω
4	1 MHz	605.91 Ω
5	2 MHz	473.06 Ω
6	4 MHz	371.67 Ω
7	6 MHz	317.08 Ω

(b)



N	SWP PARAM	VAL
0	200 kHz	2.5813 kΩ
1	300 kHz	1.187 kΩ
2	400 kHz	860.11 Ω
3	600 kHz	565.6 Ω
4	800 kHz	516.3 Ω
5	1 MHz	492.23 Ω
6	2 MHz	427.13 Ω
7	3 MHz	411.61 Ω

(c)



N	SWP PARAM	VAL
0	200 kHz	833.8 Ω
1	300 kHz	587.5 Ω
2	400 kHz	505.98 Ω
3	600 kHz	440.37 Ω
4	800 kHz	421.06 Ω
5	1 MHz	411.32 Ω
6	1.5 MHz	397.1 Ω
7	2 MHz	386.81 Ω

Figure 13: Measured magnitude-frequency responses of Z_{eq} for different R_1(a) R_1 = 5 kΩ (K = 5, C_{eq} = 0.25 nF); (b) R_1 = 10 kΩ (K = 10, C_{eq} = 0.5 nF); (c) R_1 = 20 kΩ (K = 20, C_{eq} = 1 nF)

kΩ, and C_1 = 50 pF). The ideal and simulated frequency responses of the filter in Fig.14 are exhibited in Fig.15, in which the calculated and simulated values of f_c are found to be 503 kHz and 509 kHz, respectively. The simulated frequency characteristics are in good agreement with the predicted responses, thereby confirming the practical utility of the proposed capacitance multiplier circuit. The corresponding frequency spectrum of the output voltage (v_{out}) of the BP filter is also recorded in Fig.16, where the total harmonic distortion (THD) values observed is well within 1.17%.

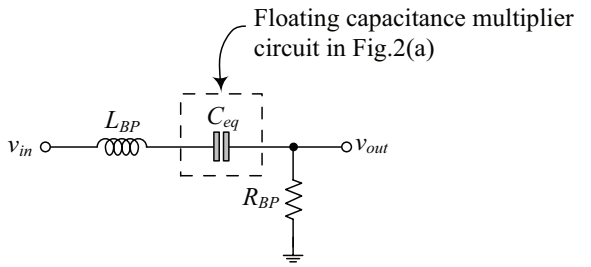


Figure 14: Second-order RLC voltage-mode BP filter implemented with C_{eq} from Fig.2(a).

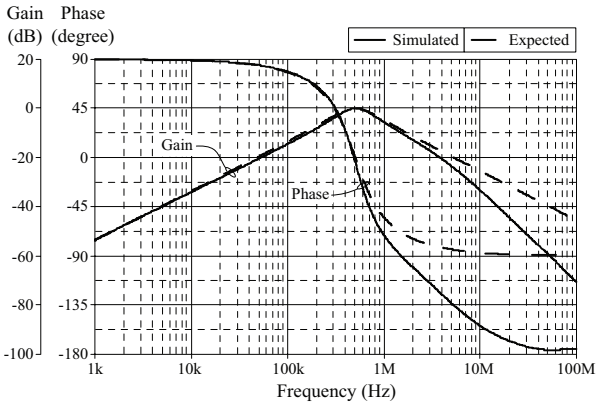


Figure 15: Expected and simulated frequency characteristics of the BP filter in Fig.14.

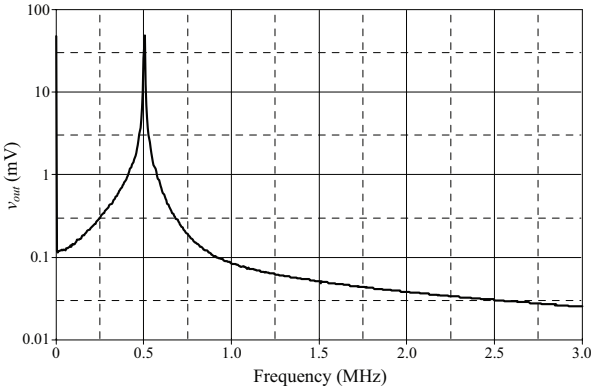


Figure 16: Output frequency spectrum of v_{out}.

Finally, in order to inspect random deviations of the BP filter center frequency due to the process and mismatch variations, Monte-Carlo analysis simulation has been evaluated with the same given parameters that resulted in the frequency characteristic of Fig.15. The simulations were performed 200 times with a 5% Gaussian deviation of relevant g_m, R_1, and C_1. The histogram of the center frequency is shown in Fig.17. According to statistical analysis results, the mean value is at 522 kHz with a standard deviation of 9.4 kHz, corresponding to 1.8% deviation from the nominal value.

6 Conclusive Discussion

This work is an attempt to present a practical realization of the tunable floating capacitance multiplier circuit using a commercially available IC LT1228. The synthetic capacitance simulator is constructed with two LT1228s, one resistor, and one capacitor. The electronic tuning feature of the simulated floating capacitor can be achieved by means of external bias currents of the IC LT1228s. The communication further discusses a second-order RLC voltage-mode band-pass filter to validate the applicability of the proposed capacitor simulation. PSPICE simulation and experimental results of the commercially available IC LT1228 are also included to demonstrate the convincing characteristics of the proposed circuit and its practical significance.

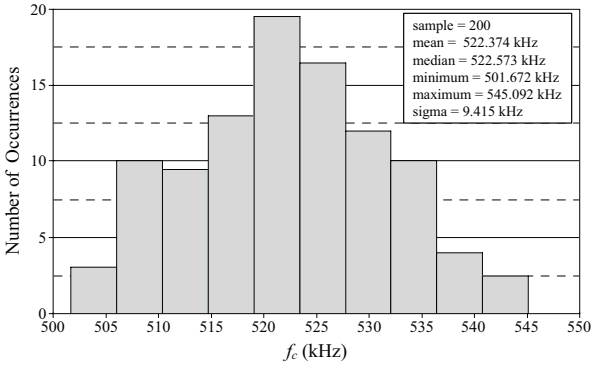


Figure 17: Monte-Carlo analysis results showing the deviation in the standard deviations of the BP filter center frequency.

7 Acknowledgment

This work was supported by King Mongkut's Institute of Technology Ladkrabang.

8 Conflict of interest

The authors confirm that this article content has no conflict of interest.

9 References

1. S. Pennisi, "CMOS multiplier for grounded capacitors", *Electron. Lett.*, vol.38, no.15, pp.765-766, 2002 https://doi.org/10.1049/el:20020517
2. M. A. Al-Absi, E. S. Al-Suhaibani, and M. T. Abuelma'atti, "A new compact CMOS C multiplier", *Analog Integr. Circ. Sig. Process.*, vol.90, no.3, pp.653-658, 2017. https://doi.org/10.1007/s10470-016-0822-1
3. W. Tangsrirat, "Resistorless tunable capacitance multiplier using single voltage differencing inverting buffered amplifier", *Rev. Roum. Des Sci. Techn.-Électrotechn. et Énerg*, vol.62, no.1, pp.72-75, Jan-March 2017.
4. W. Tangsrirat, O. Channumsin, and J. Pimpol, "Electronically adjustable capacitance multiplier circuit with a single voltage differencing gain amplifier (VDGA)", *Informacije MIDEM- J. Microelectron. Electron. Comp. Materials*, vol.49, no.4, pp.211-217, 2019. https://doi.org/10.33180/InfMIDEM2019.403
5. M. T. Ahmed, I. A. Khan, and N. Minhaj, "Novel electronically tunable C-multipliers", *Electron. Lett.*, vol.31, no.1, pp.9-11, Jan. 1995 https://doi.org/10.1049/el:19950018
6. M. T. Abuelma'atti and N. A. Tasadduq, "Electronically tunable capacitance multiplier and frequency-dependent negative-resistance simulator using the current-controlled current conveyor", *Microelectron. J.*, vol.30, no.9, pp.869-873, Sep.1999. https://doi.org/10.1016/s0026-2692(99)00025-7
7. P. V. A. Mohan, "Floating capacitance simulation using current conveyors", *J. Circuits Syst. Comput.*, vol.14, no.1, pp.123-128, 2005. https://doi.org/10.1142/s0218126605002209
8. O. Channumsin, and W. Tangsrirat, "Electronically tunable floating capacitance multiplier using FB-VDBAs", *Engineering Letters*, vol. 24, no.3, pp.365-369, 2016.
9. H. Alpaslan, "DVCC-based floating capacitance multiplier design", *Turkish J. Electr. Eng. Comput. Sci.*, vol.25, no.2, pp.1334-1345, 2017. https://doi.org/10.3906/elk-1509-112
10. M. T. Abuelma'atti, Z. J. Khalifa, and S. K. Dhar, "New CFOA-based lossless floating inductor and capacitance/resistance multipliers for low frequency applications", *J. Active Passive Electron. Devices*, vol.14, pp.229-237, 2019.
11. W. Tangsrirat and O. Channumsin, "Tunable floating capacitance multiplier using single fully balanced voltage differencing buffered amplifier", *J. Commun. Tech. Electron.*, vol.64, no.8, pp.797-803, Aug.2019. https://doi.org/10.1134/s1064226919080163
12. M. A. Al-Absi, A. A. Al-Khulaifi, "A new floating and tunable capacitance multiplier with large multiplication factor", *IEEE Access*, vol.7, pp.120076-120081, Aug. 2019. https://doi.org/10.1109/ACCESS.2019.2936800
13. M. A. Al-Absi, M.T. Abulema'atti, "A tunable floating impedance multiplier", *Arab. J. Sci. Eng.*, vol.44,

no.8, pp.7085–7089, Mar. 2019.
https://doi.org/10.1007/s13369-019-03792-z
14. Linear Technology, "100MHz current feedback amplifier with DC gain control", LT1228 datasheet, 1994.
15. S. Siripongdee and W. Jaikla, "Universal filter using single commercially available IC: LT1228", Proceedings of 2016 3rd International Conference on Mechatronics and Mechanical Engineering (ICMME-2016), October 21-23, Shanghai, China, p.14002, 2017.
https://dx.doi.org/10.1051/matecconf/201795
16. A. Chaichana, S. Siripongdee, and W. Jaikla, "Electronically adjustable voltage-mode first-order allpass filter using single commercially available IC", Proceedings of IOP Conference Series: Materials Science and Engineering, January 19-22, Tokyo, Japan, p.012009, 2019.
https://dx.doi.org/10.1088/1757-899X/559/1/012009
17. N. Roongmuanpha, T. Suesut, W. Tangsrirat, "Electronically tunable triple-input single-output voltage-mode biquadratic filter implemented with single integrated circuit package", *Advances in Science, Technology and Engineering Systems Journal*, vol.6, no.1, pp.1120-1127, 2021.
https://dx.doi.org/10.25046/aj060125
18. P. Moonmuang, N. Roongmuanpha, T. Pukkalanun, W. Tangsrirat, "On the realization of simulated lossy inductors using voltage differencing buffered amplifiers", *Proceedings of 2020 8th International Electrical Engineering Congress (iEECON)*, Chiang Mai, Thailand, 2020.
https://doi.org/10.1109/iEECON48109.2020.229469
19. N. Roongmuanpha, W. Tangsrirat, "SITO current-mode multifunction biquad using readily available IC LT1228s", *Proceedings of The 6th International Conference on Engineering, Applied Sciences and Technology (ICEAST-2020)*, July 1-4, Thailand, pp. 108-111, 2020.
https://doi.org/10.1109/ICEAST50382.2020.9165538
20. N. Roongmuanpha, T. Pukkalanun, W. Tangsrirat, "Practical realization of electronically adjustable universal filter using commercially available IC-based VDBA", *Engineering Review*, vol.41, no.3, 2021.
https://doi.org/10.30765/er.1547
21. A. Fabre and H. Barthelemy, "Composite second-generation current conveyor with reduced parasitic resistance", *Electron. Lett.*, vol.30, no.5, pp.377-378, Mar.1994.
https://doi.org/10.1049/el:19940302
22. F. Sequin and A. Fabre, "New second-generation current conveyor with reduced parasitic resistance and bandpass filter application", IEEE Trans. Circuits Syst.I: Fundam. Theory Appl., vol.48, no.6, pp.781-785, Jun.2001.
https://doi.org/10.1109/81.928161
23. G. Feeri, N. C. Guerrini, and M. Diqual, "CCII-based floating inductance simulator with compensated series resistance", *Electron. Lett.*, vol.39, no.22, pp.1560-1562, Oct.2003.
https://doi.org/10.1049/el:20031046

Arrived: 27. 02. 2021
Accepted: 01 .04. 2021

Boards of MIDEM *Society* | *Organi društva* MIDEM

MIDEM *Executive Board* | *Izvršilni odbor* MIDEM

President of the MIDEM Society | Predsednik društva MIDEM
Prof. Dr. Barbara Malič, Jožef Stefan Institute, Ljubljana, Slovenia

Vice-presidents | Podpredsednika
Prof. Dr. Janez Krč, UL, Faculty of Electrical Engineering, Ljubljana, Slovenia
Dr. Iztok Šorli, Mikroiks d.o.o., Ljubljana, Slovenia

Secretary | Tajnik
Olga Zakrajšek, UL, Faculty of Electrical Engineering, Ljubljana, Slovenia

MIDEM Executive Board Members | Člani izvršilnega odbora MIDEM
Prof. Dr. Slavko Bernik, Jožef Stefan Institute, Slovenia
Izr. Prof. Dr. Miha Čekada, Jožef Stefan Institute, Ljubljana, Slovenia
Prof. DDr. Denis Đonlagić, UM, Faculty of Electrical Engineering and Computer Science, Maribor, Slovenia
Prof. Dr. Leszek J. Golonka, Technical University, Wroclaw, Poljska
Prof. Dr. Vera Gradišnik, Tehnički fakultet Sveučilišta u Rijeci, Rijeka, Croatia
Mag. Leopold Knez, Iskra TELA, d.d., Ljubljana, Slovenia
Mag. Mitja Koprivšek, ETI Elektroelementi, Izlake, Slovenia
Doc. Dr. Gregor Primc, Jožef Stefan Institute, Ljubljana, Slovenia
Prof. Dr. Janez Trontelj, UL, Faculty of Electrical Engineering, Ljubljana, Slovenia
Doc. Dr. Hana Uršič Nemevšek, Jožef Stefan Institute, Ljubljana, Slovenia
Dr. Danilo Vrtačnik, UL, Faculty of Electrical Engineering, Ljubljana, Slovenia

Supervisory Board | Nadzorni odbor

Prof. Dr. Franc Smole, UL, Faculty of Electrical Engineering, Ljubljana, Slovenia
Prof. Dr. Drago Strle, UL, Faculty of Electrical Engineering, Ljubljana, Slovenia
Igor Pompe, retired

Court of honour | Častno razsodišče

Darko Belavič, Jožef Stefan Institute, Ljubljana, Slovenia
Dr. Miloš Komac, retired
Dr. Hana Uršič Nemevšek, Jožef Stefan Institute, Ljubljana, Slovenia

Informacije MIDEM
Journal of Microelectronics, Electronic Components and Materials
ISSN 0352-9045

Publisher / Založnik:
MIDEM Society / Društvo MIDEM
Society for Microelectronics, Electronic Components and Materials, Ljubljana, Slovenia
Strokovno društvo za mikroelektroniko, elektronske sestavne dele in materiale, Ljubljana, Slovenija

www.midem-drustvo.si