SHIFTER DESIGNS FOR ASICs

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Keywords: computer science, shifters, phase shifters, logarithmic shifters, data buses, data paths, arithmetic operations, decoders, ALU, Arithmetic-Logic Unit, FPU, Fast Processing Units, ASIC, Application Specific Integrated Circuits, VLSI circuits, Very Large Scale of Integration circuits, CAD, Computer Aided Design, logical simulations, electrical simulations, MAGIC computer tools, IRSIM computer tools, SPICE computer tools, Simulation Program with Integrated Circuit Emphasis computer tools, transmission gates, restoring buffers, propagation delay, power dissipation

Abstract: This paper presents four versions of 32 bit shifter designs that can be used in ASICs, namely: barrel shifter and logarithmic shifter, each implemented with pass transistors and transmission gates. The circuits are designed in the standard MOSIS scalable CMOS n-well technology with the 0.8 μm minimal feature size fabrication process. The design procedure is thoroughly explained. The designs are logically and electrically simulated. They are compared according to the functionality, wafer area, number of transistors, delay and power dissipation. The usage and optimization guidelines are given.

Načrtovanje premikalnih podsklopov za integrirana vezja po naročilu

Ključne besede: računalništvo, pomikalniki, pomikalniki fazni, pomikalniki logaritmični, vodila podatkovna, operacije aritmetične, dekoderji, ALU enota aritmetično-logična, FPU enote obdelave hitre, ASIC vezja integrirana za aplikacije specifične, VLSI vezja integracije zelo visoke stopnje, CAD snovanje računalniško podprto, simulacije logične, simulacije električne, MAGIC orodja računalniška, IRSIM orodja računalniška, SPICE orodja računalniška, vrata prenosna, bufferji obnovitveni, zakasnitev razširjanja, stresanje moči

Izvleček : V prispevku predstavljamo štiri tipe 32-bitnih pomikalnih vezij, ki jih lahko uporabimo pri načrtovanju integriranih vezij po naročilu. To sta matrični in logaritemski premikalni vezji, pri čemer je vsako lahko izvedeno s prehodnimi tranzistorji, oz. prenosnimi vrati. Vezja so načrtovana v standarni MOSIS CMOS tehnologiji z n otokom in minimalnimi risanimi dimenzijami 0.8 μm. Podrobno smo razložili postopek načrtovanja. Opravili smo logično in električno simulacijo vezij ter jih med seboj primerjali glede na funkcionalnost, površino čipa, število tranzistorjev, hitrost in porabo. Podali smo napotke za uporabo in optimizacijo vezij.

1. INTRODUCTION

Shifting of binary numbers is an arithmetic operation required in many operations such as multiplication, division and bit-manipulation. Shifting is performed in specially designed circuits. Shifters are part of every contemporary datapath, usually located at the output of the Arithmetic-Logical Unit (ALU).

Shift operations can be classified into left-right, logical, arithmetical or circular shift (rotating). Usually shifting is implemented only in one direction, i.e., right. Shifting left by m bits is realized with a shift right of $n–m$ bits in an n-bit machine /1/. During the logical shift the LSB takes the value of a predefined input (usually 0/1 or bit-stream from an outer source). Arithmetical shift is a shift operation where the MSB, which represents the sign of the binary number, is preserved. Circular shift puts the LSB in the place of MSB and vice-versa. All sorts of shift operations are required in modern processing units /2, 3/.

According to implementation, shifters can be classified into shift-register (sequential logic) and flow-through (combinatorial logic) types. In the shift-register type, shift by one bit requires at least one machine cycle. In the flow-through type, the time required for shifting depends only on the circuit combinatorial delay and it is usually shorter than one machine cycle. The dominant shifter implementation in modern datapaths is the flow-through type. The flow-through shifters can further be classified into /4,6/:

- binary shifter,
- crossbar switch,
- barrel shifter,
- logarithmic shifter,
- other shifter implementations.

The common requirements set upon shifter implementations in modern datapaths are:

1. bus width of 32 or 64 bits (n bits in general),
2. performing $n \times n$ shift in one clock cycle,
3. performing many types of shifter operations according to control signals (left-right, logical, arithmetic or circular shift, masking, etc.)
4. separate control signals, usually perpendicular to direction of data,
5. coded control signals,
6. low propagation delay and no degradation of output signal electrical characteristics,
7. compatibility with the rest of the datapath.

Barrel and logarithmic shifter implementations satisfy these requirements best, and thus are two most frequently used shifters /4, 5, 6/.

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Binary shifter only performs a one-place left-right shift, and crossbar switch is a universal circuit and a basis for a barrel shifter design.

In this paper, designs of barrel and logarithmic shifter in most common logic styles and comparisons of their performance are presented. The general block schematic of the designed shifters is shown in Fig. 1.

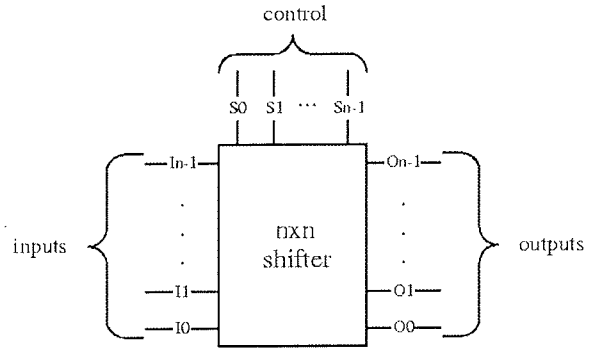

Fig. 1. General shifter block.

The design requirements set upon shifter designs are as noted above except for the requirement no. 3. For the purpose of comparison only the circular right shift as the most common shift operation is implemented. Other shift operations can be easily implemented by adding some peripheral circuitry /2, 3/ and by modifying control signals. Furthermore, the layouts of the shifters are designed in standard MOSIS /7/ scalable CMOS (SCMOS) n-well technology using 2 metallization layers, in such a way that they follow both the standard SCMOS, as well as submicron SCMOS (SCMOS_SUBM) set of design rules. They are, therefore, without any modification of the circuit or layout design, realizable in a whole range of different fabrication processes offered by MOSIS Service, starting with the 2 μm minimal feature process down to the more recent 0.35 μm minimal feature fabrication process.

Given the above mentioned requirements, the shifters are designed with the goal of a minimal layout area on the chip. Circuit and layout designs are modified and optimized in order to satisfy these requirements and the functionality of the shifters or, in some cases, to lower the circuit power dissipation to the acceptable level. No attempts to optimize the circuits according to other criteria (e.g. delay, current drive, etc.) are undertaken. This is to insure the impartiality of the shifter performance comparison.

Next, a detailed overview of the shifter circuit and layout design is given. The shifter performance is evaluated through simulations, which are described in the following section. At the end of the paper, the performance of shifter designs and some usage and optimization guidelines are presented.

2. Shifter design

2.1. Circuit design

Barrel shifters

All versions of barrel shifters are based on the crossbar switch. A version of crossbar switch with pass transistors is shown in Fig. 2.

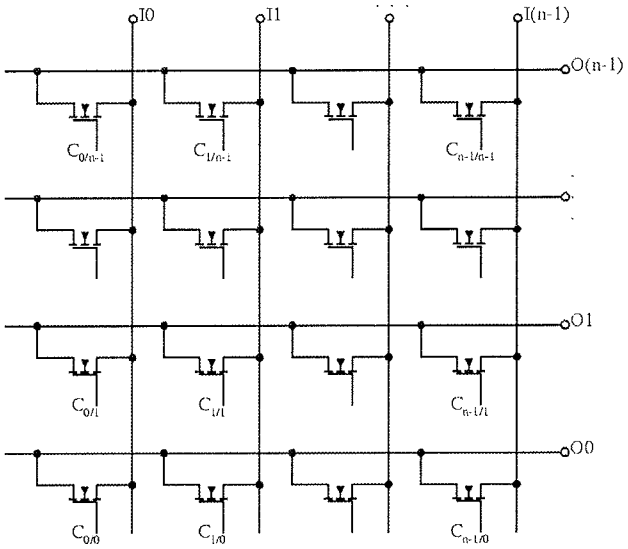

Fig. 2. Crossbar switch with pass transistors.

The crossbar switch can in theory emulate any multi-input multi-output logical function. By careful design of wiring one can readily obtain the main field of the barrel shifter shown in Fig. 3a. Control inputs to the pass transistors are designated *Si* and only one of them is high at a time, defining the shift value. If we replace the pass transistors in the circuit in Fig. 3a with transmission gates, we obtain the main field of the barrel shifter with transmission gates shown in Fig. 3b. As usual in circuits with transmission gates, this shifter requires both inverted and non-inverted control signals designated *Si'* and *Si,* respectively. By examination of both schematics, one can easily deduce that they perform the required function: circular right shift.

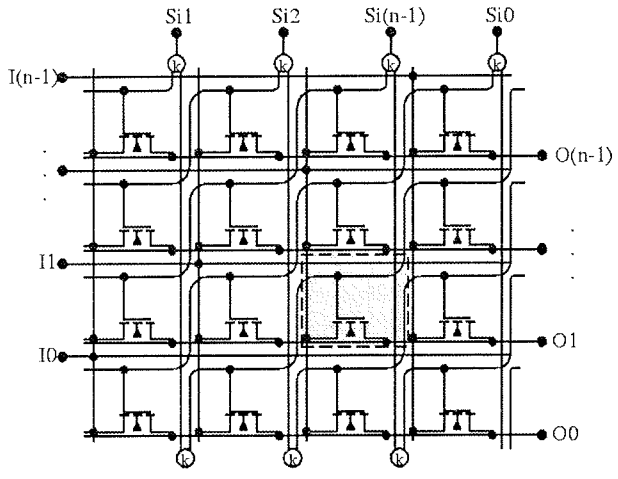

Fig. 3a. Main field of the barrel shifter: with pass transistors

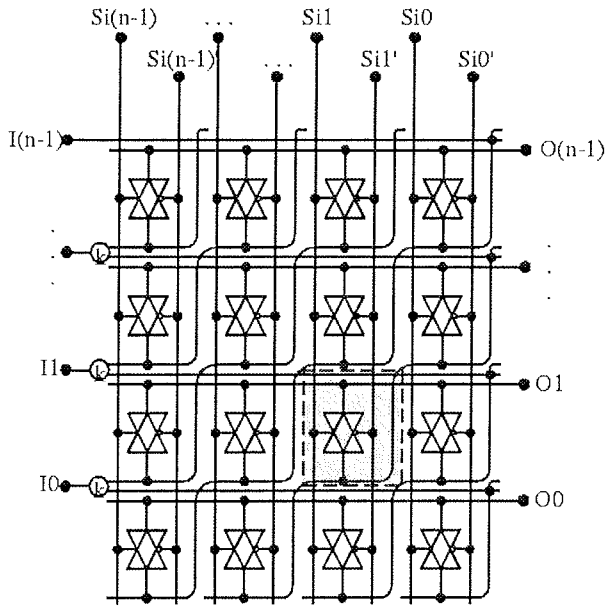

Fig. 3b. Main field of the barrel shifter: with transmission gates.

In order to comply with the requirements set upon the shifter designs, and to have coded control input signals, a decoder must be added to the circuit. In order to minimize the layout area, a NOR decoder in dynamic logic with p-type precharge transistors is chosen /4, 6/. The schematic of this decoder is shown in Fig. 4.

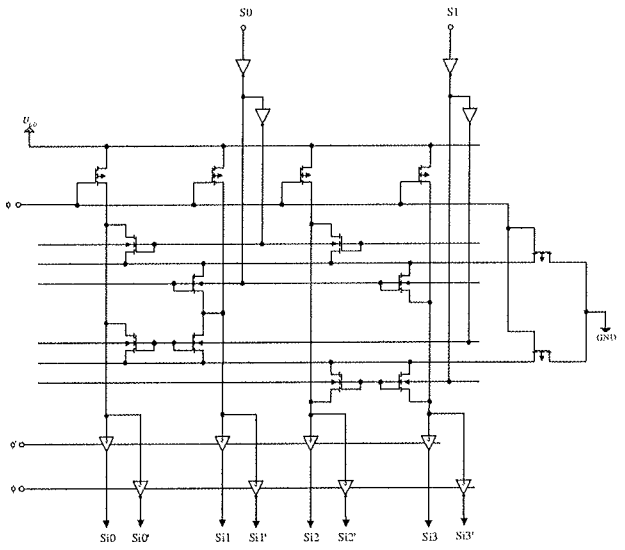

Fig. 4. NOR decoder in dynamic logic (4-bit example).

During the precharge phase the clock ϕ is low, and during the evaluation phase the clock is high. Outputs of the decoder are control inputs $Si_{(0\div n-1)}$ to the barrel shifter main field.

In order to ensure the correct logic value of control inputs *Si* and *Si'* during the precharge phase /4/, interface clocked buffers, specially devised for this purpose, are used. The circuitry is shown in Fig. 5. The buffer exists in two versions: inverting and non-inverting, depending on the used output. Both buffer versions are used in the decoder for the barrel shifter with transmission gates and can be seen in Fig 4. Only the non-inverting buffer version is used in decoder for the barrel shifter with pass transistors. Both decoders require an inverted clock ϕ'. It should be noted that the shifters are fully functional even without the interface buffers /8/, but the power dissipation is too large, due to the current leakage during the evaluation phase.

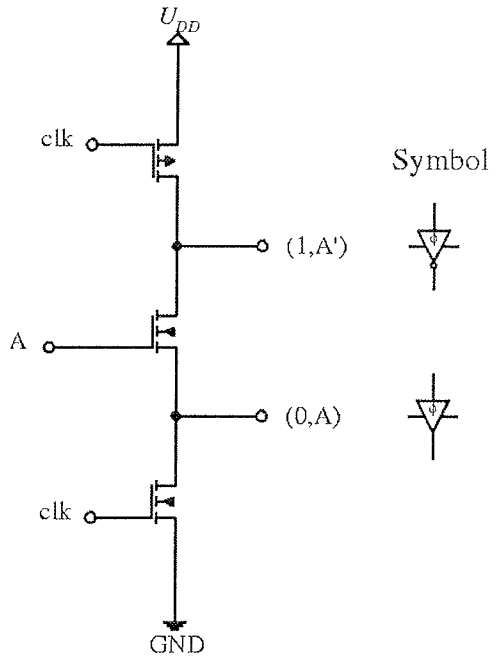

Fig. 5. Interface clocked buffers.

An interface is required to connect the barrel shifter main field with the rest of the datapath. A column of inverters at the input and at the output of the barrel shifter main field is used for this purpouse. Being in pair, these inverters do not influence the logic function of the shifter. When integrating these shifters in an actual datapath, the inverters could be replaced by latches or some other form of interface.
Degradation of electrical characteristics of output signals is a common problem in pass transistor logic. In the nMOS pass transistor the output high voltage level is lowered by the amount of the transistor threshold voltage. This effect can lead to increased power dissipation and lower noise margins of the output signals /4/. The signal level can be restored using the buffer shown in Fig. 6. The feedback transistor *Tr* pulls the inverter input high when the output of the buffer goes low, and prevents the lasting intermediate voltage value in buffer. This buffer is used at the outputs of the barrel shifter with pass transistors instead of regular inverters.

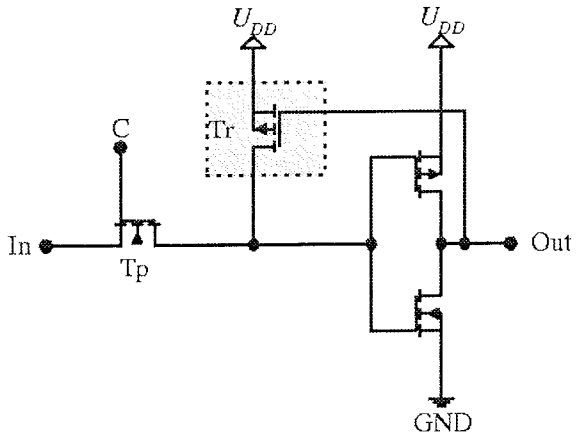

Fig. 6. Output level-restoring buffer with adjacent nMOS pass transistor /4/.

Logarithmic shifters

While the barrel shifter implements the whole shifter as a single switch field, the logarithmic shifter uses a multistage approach. The total shift value is decomposed into stages. Each stage shifts the data by some fixed amount, usually by power-of-two /4/. The shift stages can be represented with columns of multiplexers. The basis for such logarithmic shifter in base 2 is shown in Fig. 7. Such a logarithmic shifter has $\log_2 n$ stages for n-bit data bus and is usually smaller than the equivalent barrel shifter /4/. Note that the control signals S for this shifter are already encoded, i.e. no decoder is required.

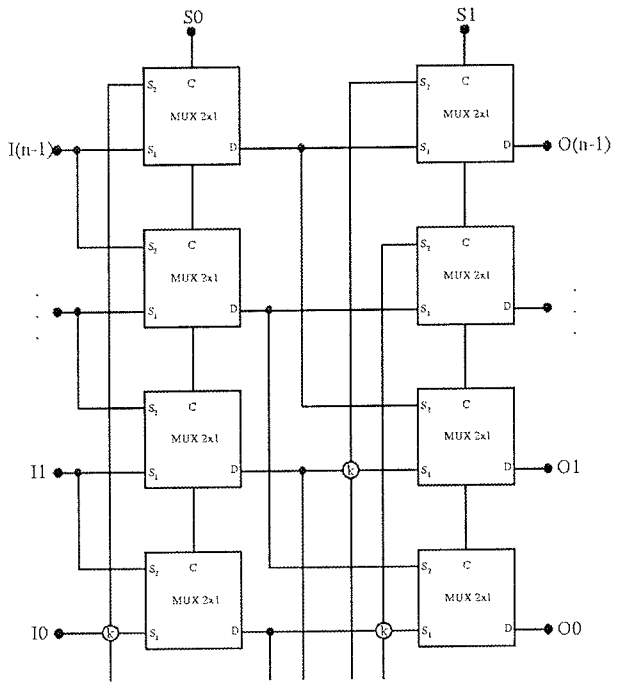

Fig. 7: Logarithmic shifter basic schematic (only first two stages).

The design of the multiplexer determines the logarithmic shifter type. Two multiplexer designs are implemented: with nMOS pass transistors and with transmission gates. The logarithmic shifter basic cells are shown in Fig. 8. An inverting buffer is placed at the output of the multiplexer. The odd number of stages in 32-bit shifter ($\log_2 32 = 5$), combined with the input inverter column, ensures that the output signal is in-phase with the input signal. As in the case of a barrel shifter, the restoring buffer is used at the output of the logarithmic shifter cell with pass transistors.

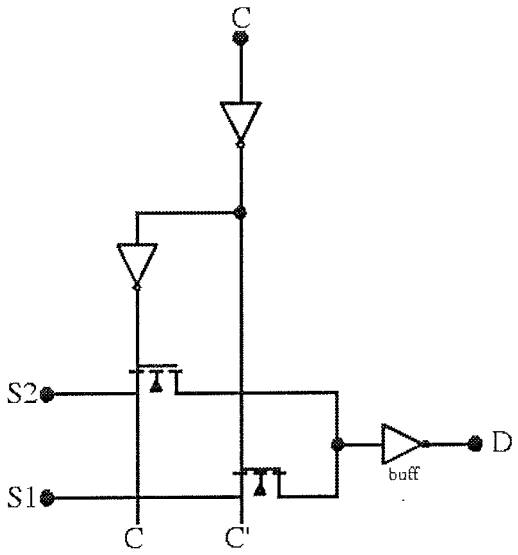

Fig. 8a. Logarithmic shifter basic cells: multiplexer with pass transistors.

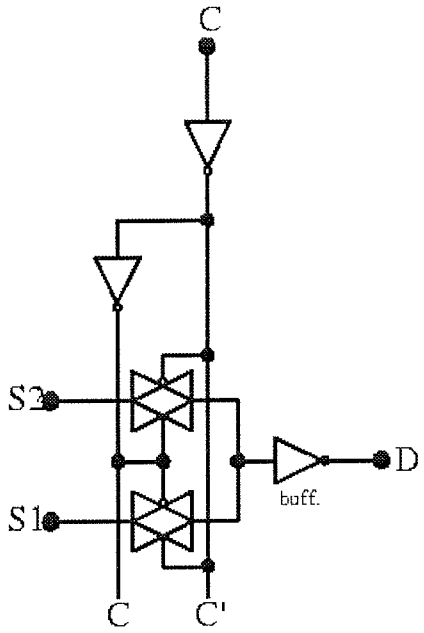

Fig. 8b Logarithmic shifter basic cells: multiplexer with transmission gates.

2.2. Layout design

The shifter layouts are designed by MAGIC, a widely accepted software tool /9/. The layouts are designed so that they follow both the standard scalable CMOS and submicron scalable CMOS set of design rules from MOSIS /7/. The chosen fabrication process is HP CMOS26G 0.8 μm n-well process with 3 metallization layers (of which only 2 are used in the design). This fabrication process was chosen because it supports both the standard and submicron set of scalable CMOS design rules, as well as a supply voltage of 5V, and because of the availability of parameter files for many computer tools /10/. The main features of this fabrication process are listed in Table I. The ratio of *p* to *n* channel widths in a layout is usually determined from the requirement for symmetrical output characteristic, equal rise and fall times or minimal propagation delay /4, 6/. This ratio is chosen to be 4, which, according to Table I, corresponds to the ratio of MOSFET *K* constants. Beside this requirement, the layouts are designed with the primary goal of achieving minimal chip area.

Table I Parameters of MOS fabrication process HP CMOS26G, run N68O /10/.

Minimal Feature Size	Supported Set of Design Rules	Lambda	# of Gates per mm²	Operating Voltage
0.8 μm	SCMOS (_TM) SCMOS_SUB	0.5 μm 0.4 μm	6200	5.0 V
Normalized MOSFET *K* Constants	**Ratios of MOSFET's *K* Constants**	**Threshold Voltages**	**Minimum Inverter Delay**	
$K'_n = 1.2704 \cdot 10^{-4} A/V^2$ $K'_p = 3.2077 \cdot 10^{-5} A/V^2$	$K'_n/K'_p = 3.960$ $\sqrt{K'_n/K'_p} = 1.990$	$U_{GS0n} = 0.7086V$ $U_{GS0p} = -0.8446V$	290 ps	

The shifter layouts are compiled of many basic shifter cell layouts. A basic cell is designed in such a way that it can be easily connected with the equal adjoining cells. After arranging arrays of basic cells, the final layout is obtained by adding contacts, external connections and power supplies.

Barrel shifters

The layout of the barrel shifter consists of two main parts: main field and decoder. Both are composed of basic cells.

The layouts of the barrel shifter basic cells are shown in Fig. 9. The schematics of the same basic cells can be seen shaded in Fig. 3 (the contacts *k* are implemented in only some cells when the layout is complete).

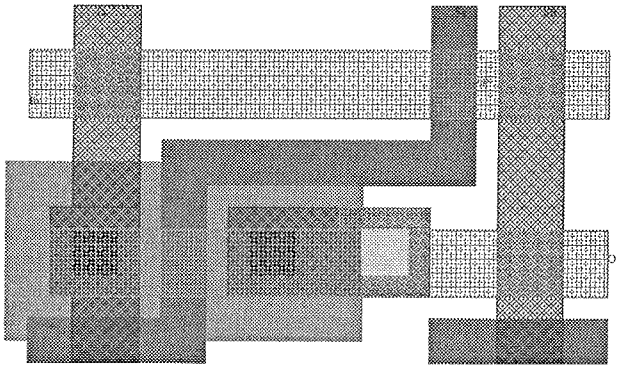

Fig. 9a. Barrel shifter basic cells layouts: cell with pass transistors.

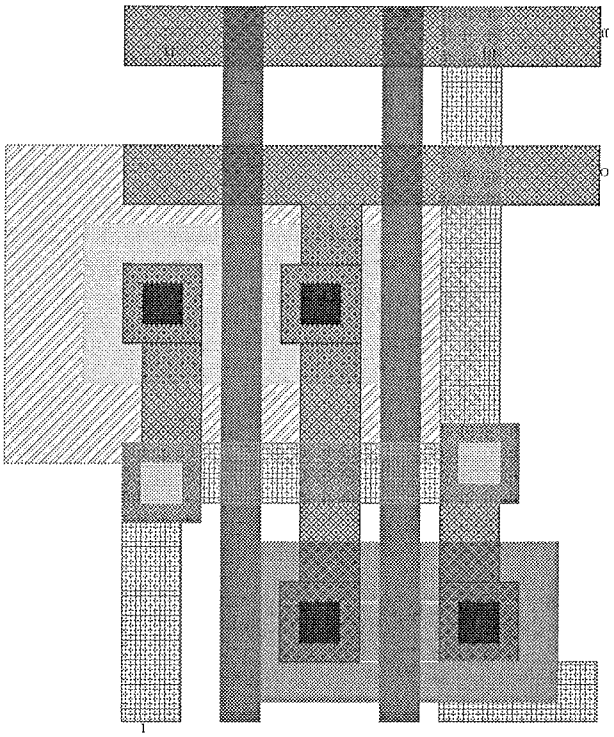

Fig. 9b Barrel shifter basic cells layouts: cell with transmission gates.

The same decoder is used for both shifters. The layout of its basic cell is shown in Fig. 10.

The layout of the output level-restoring buffer (Fig. 6) is adjusted to the vertical pitch of the basic shifter cell in Fig. 9a and shown in Fig. 11.

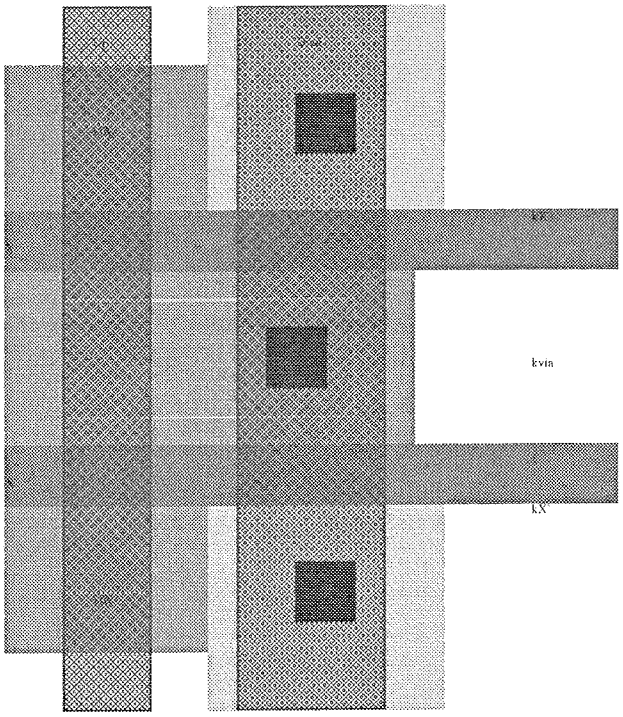

Fig. 10. Decoder basic cell layout.

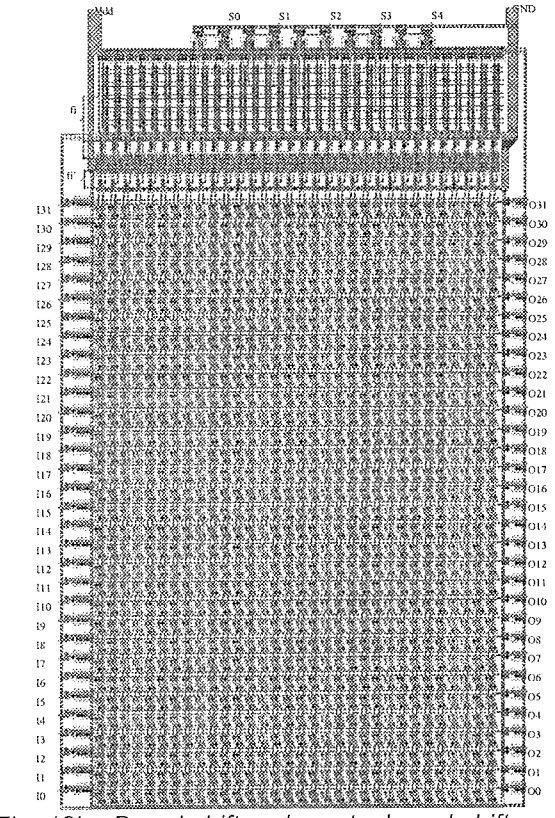

Fig. 12b. Barrel shifters layouts: barrel shifter with transmission gates.

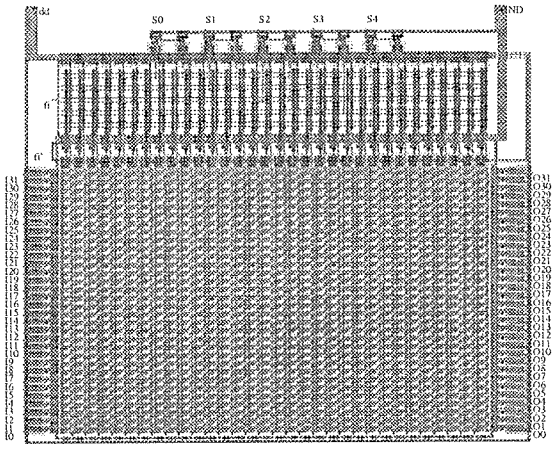

Fig. 12a. Barrel shifters layouts: barrel shifter with pass transistors

The layouts of other inverters and buffers are not shown separately, as their design is traditional. The vertical buffers, which drive the control signals into the decoder field (Fig. 4), have channel widths of twice the minimal size, because of the large capacitive load of polysilicon control lines in decoder field. The precharge *p*-type transistors in the NOR decoder have also larger widths, determined by the horizontal pitch of the basic decoder cell.

The final layouts of the barrel shifters are shown in Fig. 12. Note the different aspect ratio of these two layouts (the barrel shifter layout with transmission gates is much higher due to the difference in basic cell size).

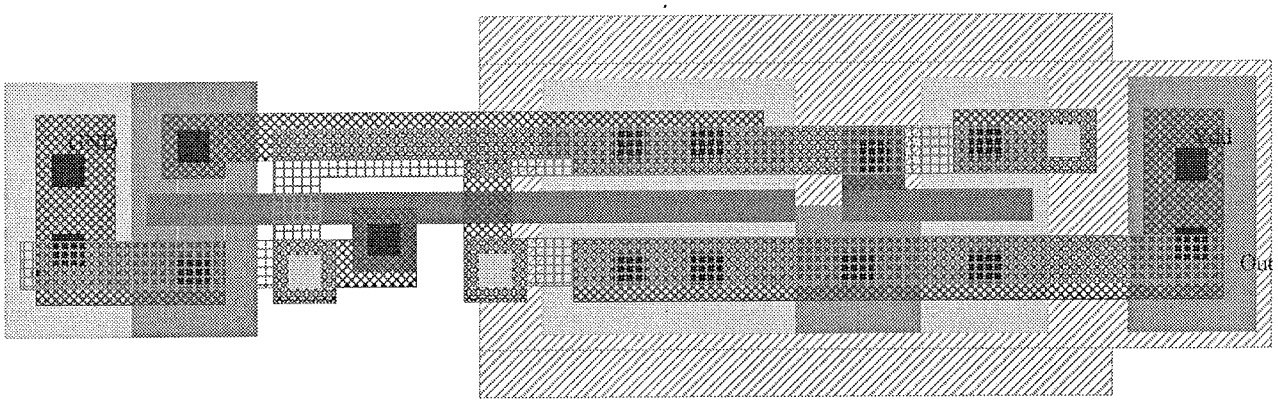

Fig. 11. The output level-restoring buffer layout.

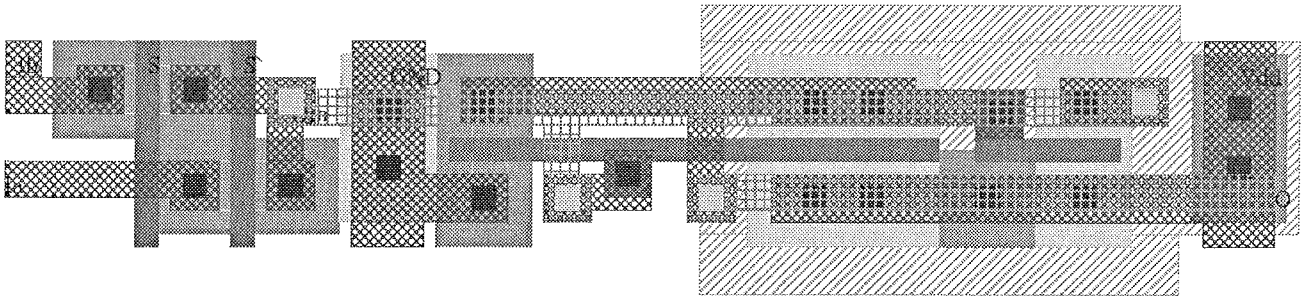

Fig. 13a. Logarithmic shifter basic cells layouts: multiplexer with pass transistors.

Logarithmic shifters

The layout of a logarithmic shifter consists of two parts: columns of multiplexers and switch field between the columns. The layouts of logarithmic shifter basic cells are shown in Fig. 13.

The vertical buffers, which are twice the minimal size, are added in the path of control signals at the top of each multiplexer column. These buffers are shown together with multiplexer cells in Fig. 8. This is necessary due to the large capacitance of polysilicon multiplexer control lines. The switch field connects the output of the cell m in the stage k with the input of the cell $(m\text{-}2^k)$ modulo 2^n in the stage $k+1$, and is typical of logarithmic shifters. It is made in two metal layers. The minimal distance between the vertical metal lines determines the size of the switch field. The width of the switch field increases exponentially with the stage shift value – 2^k /4/.

The complete layouts of the logarithmic shifters are shown in Fig. 14. The difference in layout aspect ratio is also visible in this case.

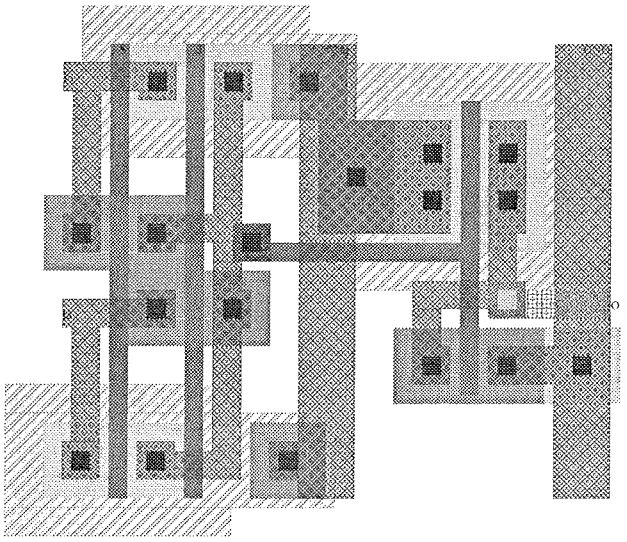

Fig. 13b. Logarithmic shifter basic cells layouts: multiplexer with stransmission gates.

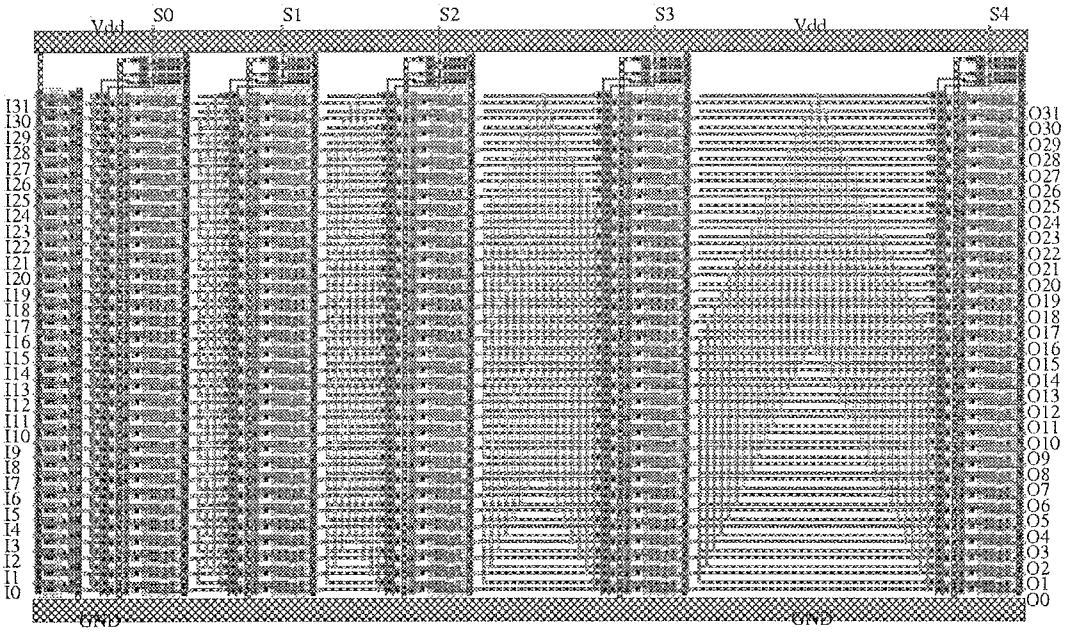

Fig. 14a. Logarithmic shifters layouts: logarithmic shifter with pass transistors,

Finally, the layout complexity of the designed circuits is presented in Table II by comparing: the number of transistors, linear dimension in units of λ, and chip area for implementation in the HP CMOS26G 0.8 μm fabrication process.

Table II. Layout parameters of designed circuits.

Shifter circuit layout*	Number of Transistors			Linear size	Chip Area, S (λ=0.4 μm), mm²
	nMOS	pMOS	Total	height × width, λ	
Barrel 1	1364	180	1544	848 × 989	0.134
Barrel 2	1428	1204	2632	1522 × 894	0.218
Logarithmic 1	522	362	884	645 × 1080	0.111
Logarithmic 2	522	522	1024	1635 × 829	0.217

* 1 corresponds to circuit version with nMOS pass transistors
2 corresponds to circuit version with transmission gates

3. SIMULATIONS

In order to evaluate circuit performance, logical and electrical simulations are used. The simulations are performed with circuit models extracted from the layout by using MAGIC and additional tools that come with the software /9/. All circuit models are extracted with the parameters of HP CMOS26G 0.8 μm *n*-well fabrication process.

For logic validation, debugging of design and initial electrical simulation, the event-driven electrical simulator IRSIM /11/ is used. It enables easy handling of wide data buses and logical states. The results obtained with this program include logical values, propagation delays and power dissipation /8/. However, due to the simple MOS transistor model based on resistance, this program could only give the approximate values of electrical parameters; the range of values and their relationships.

Simulations in IRSIM showed that all designed shifters were fully functional at a chosen clock frequency of 50 MHz. The results of one typical simulation are shown in Fig. 15.

IRSIM simulations determine the combinations of input and control signals for which the propagation delay is the largest. After initial simulations in IRSIM, additional electrical simulations for chosen input and control signal combinations are performed by SPICE /12/, in order to determine the circuit electrical parameters: voltage levels, propagation delay and power dissipation. The MOS transistors are modeled with the SPICE Level 3 MOSFET model obtained from MOSIS /10/. This model offers the advantage of faster convergence compared to the more sophisticated BSIM (Level 4 and 5) SPICE MOSFET models also available from MOSIS. The accuracy of the model is satisfying for the used minimal feature size of 0.8 μm. Summarized results of SPICE simulations are given in Table III.

Two types of propagation delays are determined from SPICE simulations: the delay from control input to output ($S \rightarrow O$, t_{DSO}) and delay from input to output ($I \rightarrow O$, t_{DIO}). The control input to output delay for barrel shifters, which have a decoder in dynamic logic, and require clock signals,

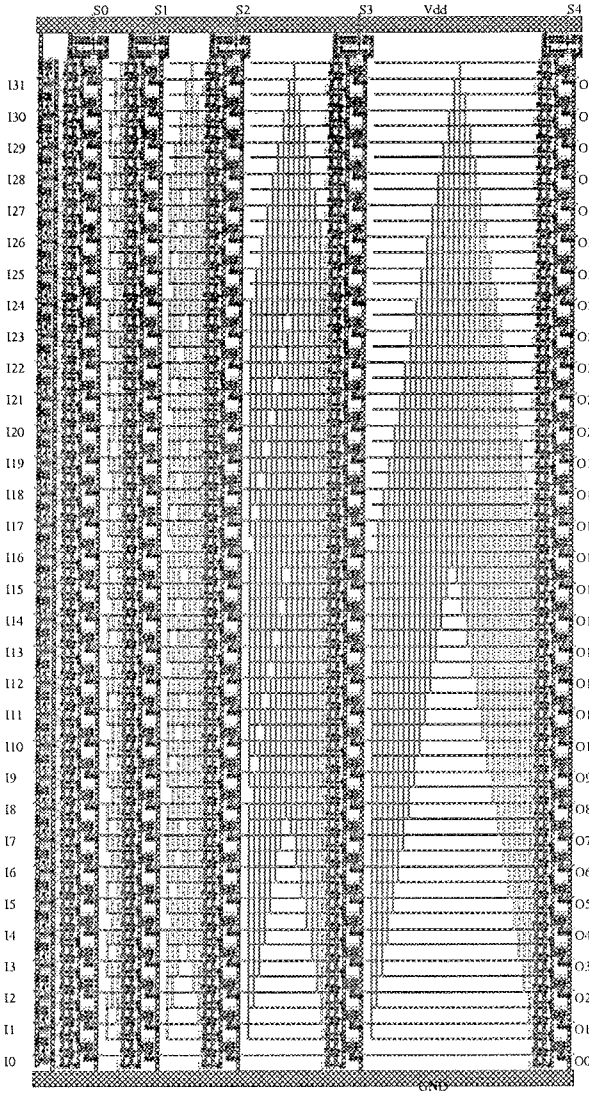

Fig. 14b. Logarithmic shifters layouts: logarithmic shifter with transmission gates.

Table III. Summarized results of SPICE simulations.

Simulated Shifter Circuit	Propagation delay, ns			Average Power Dissipation P_t, mW	Specific Power Dissipation P/S, W/cm²
	t_{DSO}	t_{DIO} H→L	t_{DIO} L→H		
Barrel 1	7.1	1.7	1.1	6.4	4.8
Barrel 2	1.4	0.6	0.5	6.0	2.8
Logarithmic 1	2.6	1.8	1.6	5.8	5.2
Logarithmic 2	2.4	1.2	1.1	5.2	2.4

is defined starting from the rising edge of clock signal ϕ, i.e., from the beginning of the circuit evaluation phase. Only the longest delay t_{DSO} is shown in Table III regardless of the transition direction. The input to output delays are evaluated for both high to low (HL) and low to high (LH) transitions of the output signal for various input and output signals. The longest delays t_{DIO} are given separately for HL and LH transitions. Fig. 16 shows the simulated electric signals from a typical SPICE simulation.

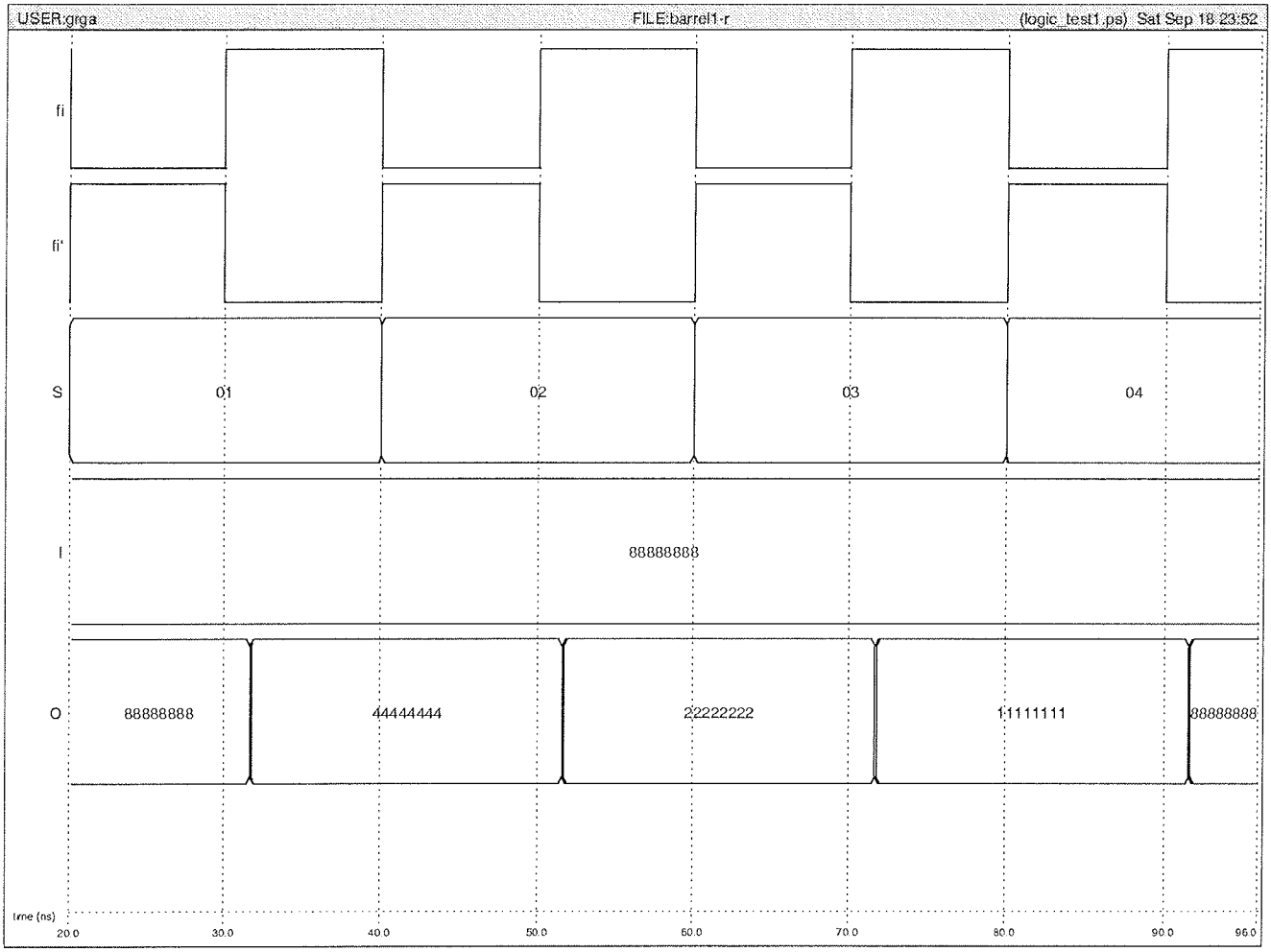

Fig. 15 Signal simulated by IRSIM (logic validation for barrel shifter with pass transistors).

Note the difference in the propagation delays for HL and LH transitions. High to low transition time is always longer. This is caused with the lower output voltage of the nMOS pass transistor and lower current drive of pMOS transistor in the transmission gate. Both of these effects cause slower rising of the signal at the output of the pass logic (which is than inverted in the output buffer). The level-restoring buffer, shown in Fig. 6, can only partially decrease this problem. The difference in delay times is however smaller for the circuits with transmission gates, which are therefore more often used in present pass logic circuits /4, 5/.

The total power dissipation of the circuits is evaluated at the clock frequency of 50 MHz (and corresponding input signal frequency of 25 MHz, see Fig. 15) for selected signal pattern by simulations over a longer time period. The input and control signal patterns were chosen to achieve the maximum dynamic power dissipation by permanent change of logic states at every clock cycle at as many circuit nodes as possible. The final signal pattern is determined by test simulations. The calculated specific power dissipation, dissipated power to chip area ratio, is given in Table III. This parameter is an indicator of thermal flux in VLSI chips and limits the integration density as well as the clock frequency for the circuit implemented in the chosen fabrication process.

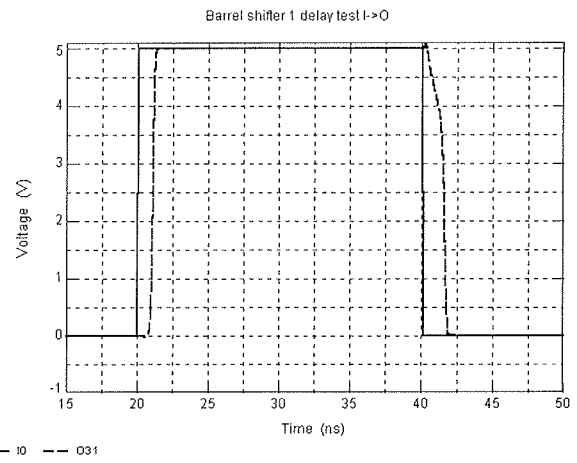

Fig. 16 Signals simulated by SPICE (propagation delay t_{DIO} for barrel shifter with pass transistors).

4. COMPARISONS AND CONCLUSIONS

The comparison of designed circuits can be made according to many criteria: number of transistors, chip area, speed, power dissipation. All designed circuits offer the same functionality; they perform circular right shift at the clock frequency of at least 50 MHz and satisfy all the requirements listed in the introductory section. One must also note, according to delay times shown in Table III, that the majority of the circuits could support significantly higher clock frequencies.

The main design difference is the existence of the dynamic logic decoder in the barrel shifters, and therefore the requirement for independently generated non-overlapping clock pair ϕ and ϕ' in these shifters. This requirement must not be considered as a deficiency, since in the datapath where this shifter would be integrated, a clock would be present anyway. By using the decoder in dynamic logic, the chip area and transistor count are minimized. Dynamic logic circuits usually have a higher speed due to the lower capacitive load /4/. In the case where the decoded control signals are already available in the chip, one would implement only the barrel shifter's main field, which would lead to significant circuit simplification, decreased chip area and increased speed.

The logarithmic shifters presented in this work are designed in combinatorial pass and static logic and do not require clock signals. When integrating these shifters in the datapath, one can add latches at the input and output of the shifter. Pipelined versions of logarithmic shifters with multiplexers in dynamic logic and with latches appeared in the literature, and are used mostly in high-performance chips /3/.

The comparison of the main shifter parameters is given in Table IV. The comparison is performed according to three criteria: complexity, delay and power dissipation.

According to Table IV, no shifter comes as a clean winner. The application of a particular shifter will depend on the requirements set upon the chip as a whole. The shifters with nMOS pass transistors have in general lower complexity. The logarithmic shifter has lower complexity than the barrel shifter in equivalent logic style. In particular, the logarithmic shifter with pass transistors has the lowest transistor count and smallest chip area. The lowest propagation delay is achieved in the barrel shifter with transmission gates. The logarithmic shifter with transmission gates has the smallest power dissipation. However the total power dissipated in other circuits is not substantially larger. The difference in the specific power dissipation is much larger and determined by the difference in the used chip area. The specific power is not a deciding design criterion except in some special cases (low-power electronics with reduced cooling possibilities).

The barrel shifter with transmission gates, due to its high speed and low power demands, seems to be the best choice for implementation in general purpose ASIC designs if no limits to the chip area are set. In the applications where a circuit with low power dissipation is needed, the best choice is the logarithmic shifter with transmission gates. The shifters with pass transistors should be preferred if the chip area is limited. The barrel shifter has the disadvantage of larger power dissipation and, especially, substantially larger control signal delay t_{DSO}.

Further improvements of the shifters are possible. For example, it is possible to enlarge or replace interface buffers or decoders. With none or small gain in chip area, one can also enlarge the otherwise minimal channel width of pass transistors. With such modification one could equalize the LH and HL propagation delays in shifters with transmission gates or lower the propagation delay in shifters with pass transistors. By adding additional peripheral and control circuitry one can enhance the shifter functionality to support more shift operations.

Finally, it is worth noting that the shifter design procedures presented in this work can be used as application guidelines for integrated circuits in general.

Acknowledgments

This paper is supported by *"Ministry for Science and Technology"* of the Republic of Croatia within the sci-

Table IV. The comparison of shifter designs and performance.

Designed Shifter Circuit	Complexity		Delay			Power	
	Tot. # Tran.	Chip Area	t_{DSO}	t_{DIO} HL	t_{DIO} LH	Tot. Power	Spec. Power
Barrel 1	1.747	1.207	5.071	2.833	2.200	1.231	2.000
Barrel 2	2.977	1.964	1.000	1.000	1.000	1.154	1.167
Logarithmic 1	1.000	1.000	1.857	3.000	3.200	1.115	2.167
Logarithmic 2	1.158	1.955	1.714	2.000	2.200	1.000	1.000

entific project *"036001 Research on VLSI/ULSI semiconductor structures"*. We are grateful to Dr. Adrijan Baric for many useful suggestions regarding the paper.

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Prispelo (Arrived): 17.07.00 *Sprejeto (Accepted): 22.11.00*