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PLANARIZATION METHODS IN IC FABRICATION TECHNOLOGIES

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Abstract: Planarization methods that are widely used in IC fabrication technologies employing 2 interconnect metalization layers are reviewed. Methods allowing only partial planarization are discussed, including fluidic methods (spin-on glass, polyimide), CVD dielectric layer deposition and etch-back, and some of their combinations. There is still a large interest in these relatively simple planarization methods, especially in regard to their refinement and fine tuning to the application at hand, despite the fact, that total global planarization, such as afforded by the CMP method, is widely considered to be the planarization method of the future. A representative, but by no means exhaustive, list of references is presented.

Pregled planarizacijskih metod v mikrelektronskih tehnologijah

Ključne besede: polprevodniki, mikroelektronika, integrirana vezja, planarizacija topografije, SOG, centrifugalno nanašanje stekla, poliimid, PECVD, nanosi iz plazemske faze, žrtvovana plast

Izvleček: Predstavljene so metode planarizacije, ki se široko uporabljajo v mikroeletronskih tehnologijah za proizvodnjo integriranih vezij z dvema plastema kovinskih (aluminijevih) povezav. Te metode omogočajo le delno planarizacijo. Obravnavane so fluidična planarizacija s centrifugalnim nanosom stekla in poliimida, planarizacija s CVD dielektrično plastjo ter uporaba žrtvovane plasti v kombinaciji fluidnih in CVD plasti. Kljub temu, da je kemijsko-mehansko poliranje površine rezine planarizacijska metoda, ki bo verjetno sčasoma prevladala, vlada danes še vedno veliko zanimanje za preprostejše metode delne planarizacije, posebno v povezavi z njihovimi izboljšavami in prilagoditvijo konkretnim potrebam določenega proizvodnega procesa. Navedena je reprezentativna, nikakor pa ne popolna, literatura na opisano tematiko.

Introduction

It is widely recognized that in IC fabrication technologies some sort of planarization, i.e. reduction of the vertical distances between topography features and reduction of the side wall slopes, becomes unavoidable as circuit features are scaled to submicron dimensions. Considerations of wafer topography become most critical during the final steps of fabrication, when several metallization and dielectric layers are deposited. The stacking of layers on top of one another in the multilevel interconnect technologies can result in poor step coverage of the metal lines as they cross over steps, and metal stringers that remain at the foot (or sides) of a sharp step after anisotropic etching /1/. If these two problems can be overcome in an IC fabrication process in which no planarization is used, eventually the limited depth of field of optical lithography tools would require some planarization to be used. In technical literature the term planarization is often used quite loosely and in connection with quite varied processing goals. In this review only planarization of dielectric layers as it applies to the multilevel interconnect technology is considered, i.e. the planarization of the dielectric layers that are formed between patterned metal layers.

There are several degrees of planarization that are achievable with different techniques, and, indeed, only different degrees of planarization are required in different cases.

1. The first degree of planarization involves only a reduction of the step slopes in the topography of the dielectric film, without significant step heights reduction.
2. Partial planarization (or semi-planarization) involves, in addition to the step slope reduction, also a reduction of the step heights.
3. In complete local planarization complete reduction of the step heights is attempted in areas of dense topography (i.e. where the spaces in the underlying metal layer topography are relatively close together), but isolated features on the wafer still exhibit some step height.
4. In the complete global planarization the surface of the dielectric layer is completely planarized over arbitrary topography.

A quantitative measure of the step-height reduction, referred to as the planarization factor β, is given by /1/

$$\beta = 1-(s_1/s_o)$$

where s_1 and s_o are the final and the initial step heights, respectively. In complete planarization β = 1 and 0 if no planarization exists. In cases where the planarization process involves only a reduction of the step slopes β = 0, however, the effects of the planarization process can be quantified by determining the so called transition angle, i.e. the angle between the wafer plane and the tangent to the dielectric layer at the step half–heights. The transition angles can be measured directly from the electron micrographs of the planarized structures. (Fig.1)

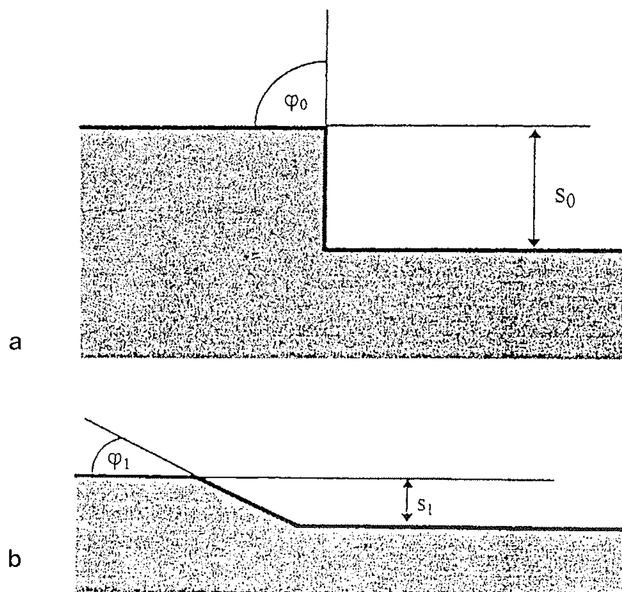

Fig. 1 *(a) Definition of the planarization factor $\beta = 1-(s_1/s_o)$; s_1 and s_o are the final and the initial step heights, respectively. (b) In cases where the planarization process involves a reduction of the step slope, its effects are quantified by the final transition angle φ_1*

There is a penalty involved in applying planarization techniques in IC fabrication. It is related to the fact, that after planarization the dielectric layer is by necessity not of uniform thickness all over the device area which means that the openings (vias) that allow forming electrical contacts between different metallization layers are of different depths. If the via sidewalls are sloped, the dimensions of the shallow vias will continue to increase during the time needed to completely etch the deep vias, possibly exceeding the width of the underlying metal pattern. In such cases a complete and global planarization may be in fact undesirable and a partial planarization of the device topography preferable /2/. There are at this time some technologies that require global planarization, e.g. LCD technologies where the globally planarized wafer surface is the lower electrode of a LC display /3/, in ferroelectric memory devices /4/, and devices incorporating optical components /5/. Global planarization techniques, especially chemical mechanical polishing (CMP), are at this time at the forefront of the process development efforts, however, they are not yet standard in the IC manufacturing, and will not be discussed further. On the other hand, there is still a large interest in partial planarization techniques, especially in regard to their refinement and fine tuning to the application at hand /6,7/, and a review of these is presented in this contribution. One should bear in mind, though, that the more levels of metal are required the less effective the partial planarization techniques become and the greater the need for processing that allows vertically sided contact holes. In this sense the global and the partial planarization techniques are converging.

Fluidic Methods - Spin-on Glass

Spin-on dielectric (SOD) planarization techniques utilize low viscosity of certain materials, e.g. photoresists, polyimides and spin-on glasses (SOG), which can fill the trenches in wafer topography /8/. These methods are simple to apply and usually require low processing temperatures (below 400 °C). However, compatibility of the fluidic materials with the standard dielectric materials can be a serious concern, and, as a rule, only limited planarization can be achieved by such methods. /9/

SOG is a frequently used planarization material /8/, and there are several different materials used for these purposes, silicate SOG and siloxane SOG being the most common. Planarization techniques utilizing these materials combine the planarizing effect of the spun-on films with the oxide like material characteristics of the SOG materials, resulting in simple and straightforward processing /10/. These materials are fairly compatible with other materials and processes in the IC fabrication technologies, and are easily integrated into the fabrication process flows. A SOG planarization film is always formed on a substrate towards which it exhibits good adhesion. Therefore, when such a film is dried and cured, shrinkage can occur only in a direction perpendicular to the substrate plain, while in the substrate plain the film is constrained. This results in build-up of the tensile stress parallel to the wafer surface. This stress is usually below 10^9 dyne.cm^{-2}, however, it has been shown /11/ that due to built-in stress SOG films have a propensity for cracking.

In IC fabrication the maximum temperature at which a SOG film can be cured is usually limited to 420 °C, or lower, because of the presence of the underlying aluminum inter-

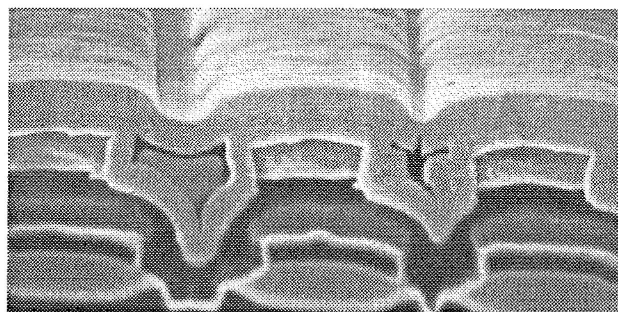

Fig. 2 *Top view of s triple stack stucture (for definition see text), planarized with a SOG partial etch back technique. Crack in the remaining SOG filler can claerly be noted, (M = 10^4).*

connection layer. After such a low temperature cure the SOG film is not completely densified and contains significant amount of silanols (in siloxane materials) and adsorbed water. If the film can be densified at a higher temperature, typically 800 - 900 °C, a sylanol and moisture free film is obtained, as demonstrated by IR spectroscopy /12/. However, some porosity still remains, as demonstrated by rehydration experiments in which freshly densified films are exposed to an atmosphere saturated with water and from which the films can reversibly adsorb H_2O /9/. These observations indicate that moisture (and possibly silanol) content in SOG films can be, due to reactions of the moisture from the film with the aluminum, potentially a serious source of quality degradation problems /1, 13/. (Fig. 2)

Rapid evaporation of the solvent from the SOG material during the deposition process challenges detailed analysis and prediction of the degree of planarization possible with such a process. The rheological (fludic) deposition models, which are used in analysis of the spin-on processes and are based on the Navier–Stokes equations /14, 15/, suggest that covering a patterned wafer with a fluidic film (SOG, photoresist or polyimide) results in a completely flat top surface of the film, which remains flat until a considerable amount of solvent is removed from the material. After the removal of the solvent only non-volatile components of the film material remain on the wafer surface. If the proportion of the non-volatile components in a SOG material is **k**, the planarization factor achieved during the evaporation of the solvents is simply $\beta = \mathbf{k}$, and thus the planarization only partial. In case of Accuglass 204 siloxane SOG material, which contains 10 % of nonvolatile components (as specified by the producer), a maximal planarization factor of β = 0.1 could is expected. However, application of such a film to the patterned wafer clearly shows that this is no the case. Due to gross transport of the planarizing material, driven by the surface tension during evaporation of the solvents, in dense topography planarization factors as high as 0.85 (depending on the details of the wafer topography) can be achieved, and less than 0.1 on isolated topography features. This indicates that the transport of the planarizing material during the evaporation of the solvents plays a crucial role in the SOG planarization process. Also, the quality of the surface underlying the planarization film appreciably effects the planarization process. These effects can not be predicted by the rheological models /9/. Typically, planarization by SOG films deposited on patterned wafers (patterned aluminum on field oxide) simultaneously exhibits surface and topography effects. All of the above precludes total global planarization with such a process.

If two SOG films are deposited consecutively, the second film being deposited after considerable densification of the first one, an increase of the planarization factor β by aprox. 10 % is achievable. The resulting planarization factor of a two-step planarization process can be quite reliably predicted for a predetermined site on the wafer. (Table 1, Ref. 9.).

Quite clearly a multiple-step planarization by SOG a material is a process of diminishing returns and total planarization, even locally at a predetermined site, may not be a realistic goal of such a multi-step process.

Table 1. Planarization factors after different stages of SOG (Accuglass 204) planarization process

Planarization stage	planarization factor
deposition (including evaporation of solvents at 100 °C): isolated lines	0.09
deposition (including evaporation of solvents at 100°C): dense topography	0.9
densification	0.9
compound (evaporation + densification): dense topography	0.81
double planarization: dense topography	0.86
triple planarization: dense topography	0.90

Fluidic Methods - Polyimide

Polyimide films are also frequently used as an interlevel dielectrics. Their use is justified primarily by the ease of their application, which parallels the application of photoresists, and also by the good chemical and physical properties of the cured films and their general compatibility with most materials encountered in IC fabrication. As the polyimide films are formed from a solution that typically contains 15 to 30 % of solids, they have attractive planarizing properties, such as the ability of filling of narrow trenches without forming voids during curing, and relatively high (compared to SOG) planarization factors. In contrast to SOG planarization processing, application of several polyimide films consecutively presents no serious problems, thus enhancing the (local) planarization factors achievable by this material beyond 0.95. Some impressive multi metal processes using polyimide films as interlevel dielectric have been reported /16/, however, the material has not gained widespread acceptance. Among the several reasons for this is the sensitivity of its cross–linking curing process to the precise curing temperatures and schedules /17/, its hygroscopicity, questionable adhesion of the polyimide to metal under conditions of stress, and relative complexity of the integration of the polyimide etching process into a fabrication process.

Reflow of Doped Glass

When processing temperatures above 400 °C are not a consideration (e.g. if the underlying patterned layer is polysilicone), deposition and thermal reflow of doped glasses offer an attractive step reduction and/or partial planarization possibility. It is well known that the composition of the doped glass (e.g. boron and phosphorus doped glass (BPSG)) strongly influences the reflow temperature at which the surface tension of the film drives the redistribution of the film material /1/. Optimizing glass doping for low temperature reflow makes the planarizing film susceptible to moisture, resulting in poor reliability of fabricated ICs /18/. In designing a successful planarization process involving BPSG both of these tendencies have to be considered and balanced. As an example, the transition angles after reflow planarization (30 min at 950 °C) of BPSG films deposited by a PECVD method and densified, in the range of 2.4 to 3.1 w % of B and 4.4 to 5.4 w % of P are shown in Table 2 /19/. At this compositions the transition angles

are not minimal, however, structural stability of such films is greatest. The so called single stack structure is an array of 600 nm thick and 1,2 μm wide parallel aluminum lines formed on a flat, oxidized wafer; in the double stack structure the metal lines are formed on top of oxide lines of the same dimensions, resulting in a 1,2 μm step in topography. Both types of structures were prepared at two different separations of the lines, 1 μm and 2,5 μm. The transition angle between the topography levels before the planarization has in all cases been close to 90 deg. (Fig. 3)

Fig. 3 A sigle stack structure (1 μm trench width) planarized by a BPSG reflow process. The doping of the planarizing material is 3.1 w % P, 4.5 w % B, 30 min reflow at 950 °C planarization. The transition angle after reflow is 22.0 deg, and β = 0.6.

Table 2. Transition angles in single and double stack structures, after BPSG densification and reflow, at different film compositions.

w. % B	W. % P	transition angle (deg)			
		line separation 1 μm		line separation 1 μm	
		double s.	single s.	double s.	single s.
3.1	4.5	22.7	22.0	19.7	19.0
2.4	5.4	24.6	23.2	23.1	16.4
2.5	3.2	30.8	30.9	33.0	33.5
1.6	4.6	40.0	35.9	36.9	34.3
2.8	4.4	29.8	21.3	30.5	22.2

Thermal reflow of a BPSG film can in favorable circumstances lead to nearly complete local planarization. Recent advances in the glass-flow processing allow for simultaneous deposition and reflow and reduced processing temperature /20/.

Etch-back and Sacrificial Layers

One of the simplest methods available for smoothing steps in wafer topography, and one that is the easiest to integrate into a fabrication technology, is the deposition of a CVD glass layer that is significantly thicker than the step it must cover and subsequent etch-back to the desired film thickness /1/. The method is based on the isotropic and thus nonconformal nature of the CVD deposition process, which results in a dielectric film with topography features less extreme than the features of the film it covers. But the nature of the deposition process is also the cause of one of the difficulties in applying the method in topographies with high aspect ratii, i.e. the formation of voids between metal lines if the thickness of the metal layer exceeds aprox. one half of the minimum spacing between the metal lines. A process combining plasma enhanced and low temperature CVD TEOS allows high aspect ratio (as high as 0.85) topographies to be filled without void formation /21/. Such a process can provide partial planarization with planarization factors exceeding 0.5, but not total planarization, either local or global.

An extension of the above method is the sacrificial layer technique. It is widely used in two-metal processes and allows a high degree of planarization between steps that are 2 to 10 um apart, but works less well for planarizing isolated features /7/. The process involves coating a CVD dielectric layer with a film that will later be etched off (sacrificed). Usually sacrificial layers are formed from low viscosity fluids that, after appropriate heat treatment, produce solid films with planarized, often practically flat, surfaces. Photoresists, plyimides and SOG films are used for these purposes. Therefore after the formation of the sacrificial film the planarization of the CVD film topography can not exceed the planarization that can be achieved by the fluidic methods. However, during the rapid etch back of the sacrificial layer the topmost parts of the CVD layer become exposed first and with suitable etch chemistry, that allows the CVD and sacrificial layers to be etched at equal rates, further planarization is achieved. As the sacrificial layer planarization process is well described in literature and models for predicting the degree of planarization available /22, 23/ it will not be further discussed.

When a SOG material is used as the sacrificial layer, an extension of the process is possible in which the SOG material is not etched back completely but is allowed to remain filling the gaps in the CVD dielectric layer /7/. Fig. 4 dem-

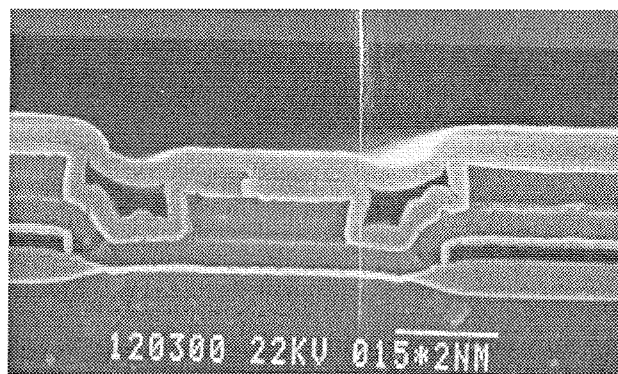

Fig. 4. Planarization of the sunken via (via itself not shown) between two double stack structures, with a SOG partial etchback process. The dark structures between the metal lines are SOG fillers that remain after the SOG etchback and Metal 2 is deposited directly on the structure.

onstrates the planarization of a sunk contact by such a method in a 1.2 um process, using Accuglass 204 SOG material. The SOG etchback process is sometimes extended by depositing a thin CVD dielectric film on top of the SOG fillers, thus forming a dielectric sandwich structure, (Fig. 5).

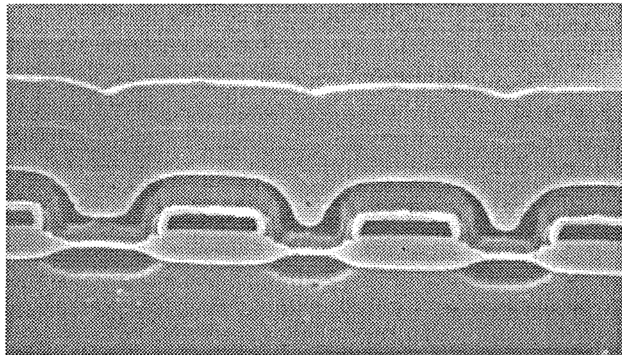

Fig 5 A SOG - CVD sandwich structure. The double stack (patterned polysilicone on FOXT) structure has been planarized SOG partial etchback process and then covered by a doble CVD layer. The second of these is a sacrificial layer to be planarized by etchback.

A major and unsolved difficulty of this process remains the partial incompatibility of the low–temperature cured SOG material with the materials it contacts and possible reliability problems this might cause. The use of polyimide instead of SOG in a similar process has been reported /24/, apparently with similar reliability problems.

Conclusion

The described planarization methods are widely used in technologies employing 2, and sometimes 3, interconnect metallization layers. A detailed understanding of the planarization process is required to design a IC fabrication process which results in the required degree of planarization on a production wafer. Global planarization with these processes is extremely difficult, if not impossible, to achieve, but local planarization with a planarization factors exceeding of 0.9 is certainly within their reach. Their use requires suitable changes in the design rules. As the trend in advanced IC design today is toward the elimination of all such restrictions regarding the dielectric layers, even in technologies with more than 2 interconnect levels, it seem that this goal, which has not yet been reached, is attainable only with development of methods of total global planarization, together with technologies that allow vertically sided contact holes and vias of varying depths to be completely filled.

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