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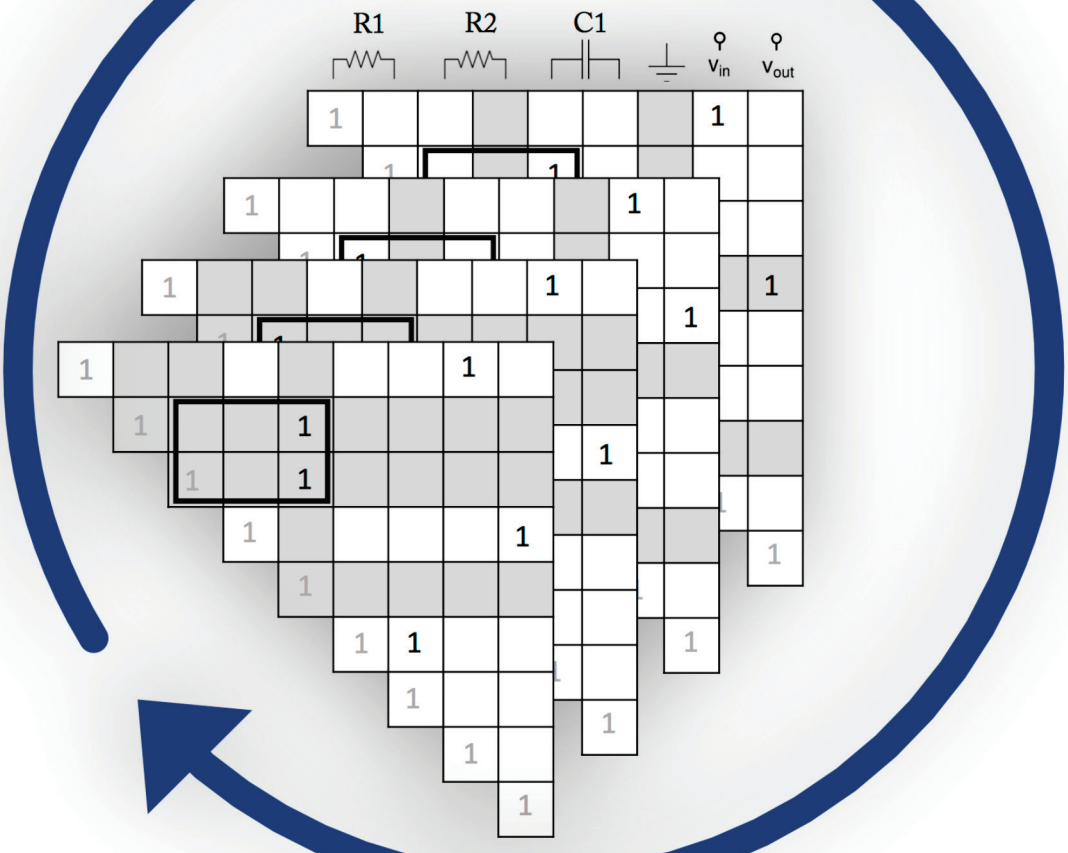

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Reliability analysis and SFG modeling of a new modified Quadratic boost DC-DC converter

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Abstract: In the present scenario, direct current boost converters play a vital role in automobiles and various industries. The direct current boost converters are designed by diverse topologies in which every topology has its benefits. The task arises in developing a converter with reduced losses, increased efficiency, robust and high gain. In this paper, a novel topology for the DC-DC conversion is proposed for high-intensity discharge lamps. The designed topology is the modified structure of the quadratic boost converter and hence named as the modified quadratic boost converter. The model, which is proposed, is more efficient with increased performance. This model is compared with an existing model, and the results are verified. The open loop small-signal analysis of the proposed topology is carried out using the switching flow graph modeling method to perform the dynamic analysis. The reliability analysis of the converter introduced is done for ensuring the lifetime operation of the converter. From reliability analysis, it is observed that the proposed topology is 14 years more reliable than the compared existing topology. It is also identified that the derived one is 6% more efficient than the compared one. A 40 W prototype, which is suitable for HID lamps, is developed to validate the theoretical results.

Keywords: MQB (Modified Quadratic Boost); voltage stress; efficiency; SFG (Switching Flow Graph); frequency domain; reliability

Zanesljivostna analiza in SFG modeliranje novega modificiranega kvadratičnega DC-DC pretvornika navzgor

Izvleček: Direktni pretvorniki navzgor danes predstavljajo pomembno vlogo v industriji. Realizirani so v različnih topologijah. V članku je predlagana nova topologija DC-DC pretvornika za uporabo v visokotlačnih sijalkah. Predlagana topologija sloni na kvadratičnem pretvorniku navzgor z izboljšanim izkoristkom in učinkovitostjo. Rezultati so preverjeni in primerjani z obstoječim modelom. Odprtozančna analiza majhnih signalov je opravljena na osnovi je opravljena z modelom grafa preklopnega poteka. Zanesljivostna analiza je pokazala, da je zanesljivostna doba predlagane topologije 14 let daljša od obstoječe topologije. Teorija je verificirana na osnovi idealnega prototipa moči 40 W, ki je primeren za napajanje HID sijalk.

Ključne besede: kvadratičen pretvornik; napetostni stres; izkoristek; SFG; frekvenčna domena; zanesljivost

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1 Introduction

In the present generation, high gain DC-DC converters find their application in various fields. Due to power crisis and shortage of electricity generations, the efficient use of the available energy in the present scenario plays a significant role [16]. In this case, DC- DC boost converters play a major role in renewable power plants. There are various topologies for the DC-DC boost converters with different drawbacks such switch voltage stress, losses in the nonlinear elements, very less voltage gain and so on. The methods to achieve high step-up, low cost, and high-efficiency DC-DC conversion constitute a significant consideration. The high-intensity discharge lamps are used in automobiles, which are powered by the batteries at low voltage. Hence, it is needed to step-up the voltage to the high level of output voltage. The operating voltage of the HID lamps is 80-90 V which cannot be achieved by conventional boost converter with 12 V supply. To achieve a highly efficient DC-DC boost conversion with reduced losses and high voltage gain, the below model is proposed with reduced number of inductors compared to the model considered for the comparison.

Various topologies had been constructed in the recent years to achieve high voltage gain for numerous applications. There are several methods to produce the high gain in DC-DC converters. Voltage multiplier cell, switched capacitor, switched inductor, voltage-lift cell, coupled inductor is integrated with the conventional DC-DC topologies to boost the voltage conversion ratio. Cockcroft and Dickson multiplier cells are used to boost the voltage of the converters. Dickson and Cockcroft multiplier cell are incorporated in the boost converter, and their performance is analyzed in [1, 2]. The gain of the converter is further increased by the adding coupled inductor to the topology, and it is reported in [3]. This leads to increase in the number of components. Boost converter integrated coupled inductors are reported in the literature [4, 5]. However, the use of multiple coupled inductors complicates the dynamic analysis of those topologies [6]. Ultra gain converters are derived by voltage lift cells which are introduced by F.L. Luo [7, 8]. However, high gain is achieved with self and relift techniques with too many components[15]. Two or more methods are integrated to attain high voltage gain and combine its advantages for better performance. The coupled inductor is combined with switched capacitor cell to derive high step-up converter, and quasi-resonant operation is employed to reduce the switching loss [9, 10]. Asymmetrical and symmetrical hybrid switched inductor converters are proposed in [11] for PV grid connected system. However, the above-mentioned topologies are derived by adding additional components to the existing converters. In this paper, we have derived a high gain converter with the simple modification in the conventional topology. The primary objective of the work is to design a DC-DC boost converter, which is more efficient in conversion with much-reduced losses, compared with an existing converter and must be suitable for meeting the requirements of high-intensity discharge lamps.

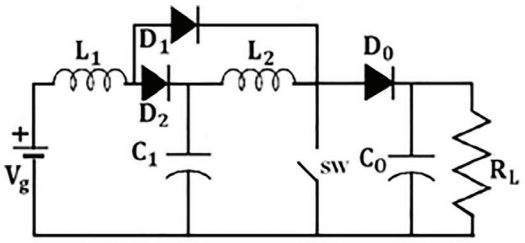
The variation in the derived topology presented in this paper is the alteration of the existing converter, i.e., Quadratic boost converter with the addition of only one capacitor and a removal of a diode [12]. The maximum stress voltage across all the components in the modified topology is found to be lower compared to the quadratic boost converter. The proposed topology is compared with quadratic boost converter and existing converter in the literature. Mostly, comparative study will be based on efficiency, voltage stress, volume, and reliability. We have compared the proposed topology with the existing topology based on reliability using FIDES guide [13]. The superiority of the proposed topology is proved based on the reliability, which is not reported in the literature until now.

The paper is organized as follows: Section 2 provides the modes of operation of the proposed topology. Section 3 gives steady-state analysis in CCM and DCM condition, the design of passive components, efficiency analysis, time domain and frequency domain analysis. The proposed topology is evaluated with the existing converters, and it is presented in section 4. Reliability study is performed on proposed topology and compared with the existing topology, and it is shown in section 5. Section 6 presents the simulation results to provide evidence to the theoretical calculation, and a prototype is raised to confirm the derived topology. Finally, the paper is terminated in section 7.

2 Structure of proposed converter

Figure 1(a) and (b) present the conventional quadratic boost converter and modified quadratic boost converter as proposed topology respectively. The modification made in the existing quadratic boost converter is the removal of one diode and addition of capacitor. The total number of devices in both the converters is same with the single switch. A number of passive components in quadratic boost converter are four, and it is five in the proposed topology. The diode count in the proposed converter is two, but it is three in the quadratic boost converter. The converter mainly comprises of two inductors, three capacitors, two diodes, resistive load, and a switch. The advantage of the modification made in the topology is discussed in section 4. Figure 2 (a) and (b) provide the mode 1 and mode 2 of the proposed topology.

(a)



(b)

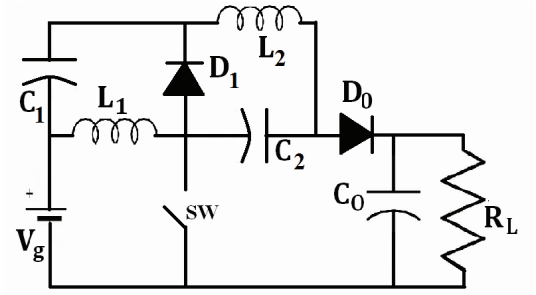


Figure 1: (a) Quadratic boost converter (b) Proposed topology

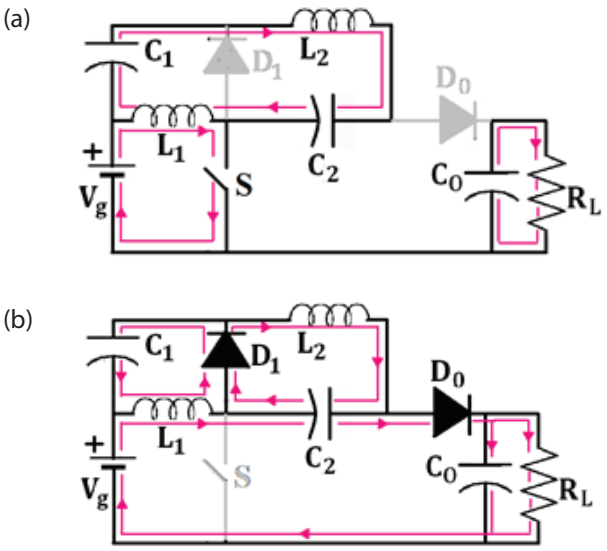


Figure 2: (a) Mode 1 (b) Mode 2

Mode 1: The states of device conduction and current path for the conducting state of the S are given in Figure 2(a). When switch SW is ON, inductor L_1 and L_2 are charged to the supply voltage V_g. Diode D_1 is reverse biased by the negative polarity of the supply voltage through the switch. Diode Do also reverse biased by the voltage across the inductor L_2. Load voltage is due to the charge in the output capacitor.

Mode 2: Figure 2(b) gives the current path when the switch S is in non-conducting state. Diode D_1 and D_O are forward biased due to the voltage of the capacitor. The inductor L_1 and L_2 started to discharge through these diodes. The output voltage is equal to the summation of the input voltage, capacitor C_1 and C_2 voltage. Figure 3 gives the current through all the passive components and diode.

3. Analysis of the proposed topology

3.1 Steady State Analysis in CCM

Voltage across the inductor L_1 and L_2 in ON and OFF mode is written as follows

$$V_{L1} = V_g \tag{1}$$

$$V_{L2} = V_g + V_{C1} - V_{C2} \tag{2}$$

$$V_{L1} = -V_{C1} \tag{3}$$

$$V_{L2} = -V_{C2} \tag{4}$$

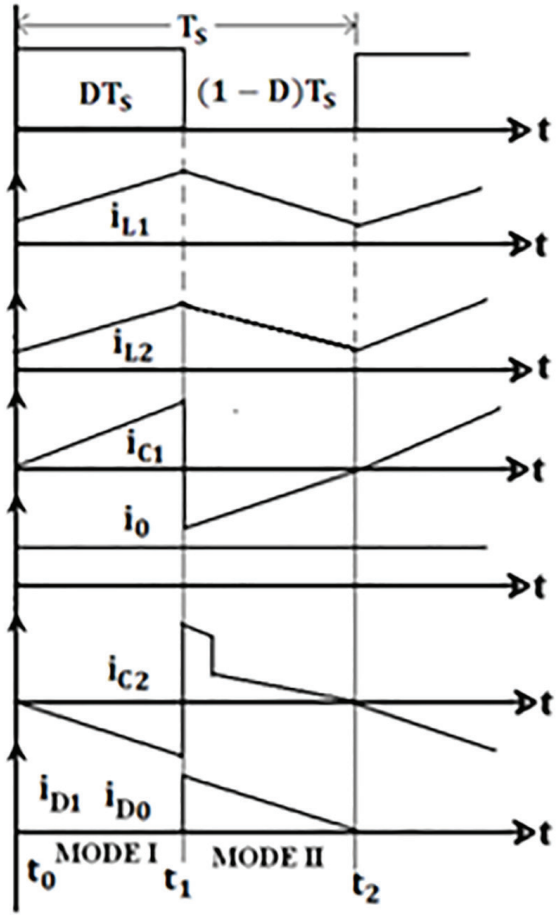


Figure 3: Current waveforms of the MQB converter

By applying volt-sec balance principle to the Equations (1)-(4), capacitor voltage C_1 and C_2 is obtained as

$$V_{C1} = V_{C2} = \frac{V_g D}{1-D} \tag{5}$$

The output voltage is given as

$$V_O = V_g + V_{C1} + V_{C2} \tag{6}$$

By simplifying the Equation (6), the voltage gain of the converter is obtained as

$$G_{VCCM} = \frac{V_O}{V_g} = \frac{1-D^2}{[1-D]^2} \tag{7}$$

Current through the capacitor C_1 and C_2 is written and by applying charge-sec balance principle, the current through the inductor L_1 and L_2 is obtained as

$$I_{L1} = \left[\frac{1+D}{1-D}\right]^2 \frac{V_g}{R_L};\ I_{L2} = \frac{1+D}{1-D}\frac{V_g}{R_L} \tag{8}$$

3.2 Boundary Conditions for Inductor L_1 and L_2

Figure 4 shows the inductor L_1 and L_2 current waveform at Discontinuous Conduction Mode (DCM) condition. The condition for inductor L_1 to operate in DCM as follows

$$I_{L1} < \frac{\Delta i_{L1}}{2} \tag{9}$$

I_{L1}= average current through the inductor L_1
Δi_{L1}= Ripple of the current through the inductor L_1

Substituting Equation (8) in (9)

$$\left[\frac{1+D}{1-D}\right]^2 \frac{V_g}{R_L} < \frac{V_g D T_S}{2L_1} \tag{10}$$

Solve the Equation (10)

$$\frac{2L_1 f_S}{R_L} < \frac{D}{G_{VCCM}{}^2} \tag{11}$$

The DCM condition for inductor L_1 is given as

for DCM $K_{L1} < K_{Crit1}$ (12)

The condition for inductor L_2 to operate in DCM as follows

$$I_{L2} < \frac{\Delta i_{L2}}{2} \tag{13}$$

I_{L2}= average current through the inductor L_2
Di_{L2} = Ripple of the current through the inductor L_2

Substituting Equation (8) in (13)

$$\frac{V_O}{R_L} < \frac{[V_g + V_{C1} - V_{C2}]DT_S}{2L_2} \tag{14}$$

Simplification leads to

$$\frac{2L_2 f_S}{R_L} < \frac{D}{G_{VCCM}} \tag{15}$$

The DCM condition for inductor L_2 is given as

for DCM $K_{L2} < K_{Crit2}$ (16)

3.3 Steady State Analysis in DCM

Applying volt-sec balance principle on inductor L_1

$$V_g D_1 - V_{C1} D_2 = 0 \tag{17}$$

Applying volt-sec balance principle on inductor L_2

$$[V_g + V_{C1} - V_{C2}]D_1 - V_{C2} D_2 = 0 \tag{18}$$

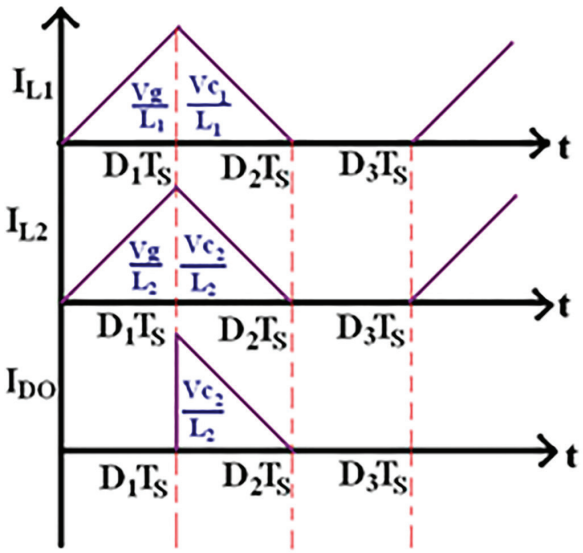


Figure 4: Inductor L_1 and L_2Current waveform at DCM

By simplifying the Equations (17) and (18), capacitor voltage is obtained as

$$\frac{V_O}{V_g} = 1 + 2\left[\frac{D_1}{D_2}\right] \tag{19}$$

Output diode DC component current must be equal to the DC load current, $I_{DO} = I_O$
The DC component of the output diode current is

$$I_{DO} = \frac{1}{T_S}\int_0^{T_S} I_{DO}(t)\,dt \tag{20}$$

According to the Figure 4, peak diode current can be obtained by multiplying the slope of the waveform with the time interval.

Simplify the integral (20) and rearrange to yield

$$\frac{V_O}{V_g} = \frac{D_1 D_2 T_S R_L}{2L_2} \tag{21}$$

Solving the Equations (19) and (21) yield the voltage conversion ratio of the proposed topology in DCM

$$G_{VDCM} = \frac{V_O}{V_g} = \frac{1 \pm \sqrt{1 + \frac{8D_1^{\,2}}{K_{L2}}}}{2} \tag{22}$$

The complete modified quadratic boost converter's conversion ratio including CCM and DCM are

$$G_V = \begin{cases} \dfrac{1-D^2}{[1-D]^2} & \ldots\ldots\ldots\ldots CCM \\ \dfrac{1 \pm \sqrt{1 + \frac{8D^2}{K_{L2}}}}{2} & \ldots\ldots\ldots\ldots DCM \end{cases} \tag{23}$$

3.4 Design of Inductor and Capacitor

Current ripple, voltage ripple, and switching frequency are required to design the passive elements of the converter. The peak-to-peak current ripple of Inductor L_1 and L_2 is given as

$$\frac{\Delta i_{L1}(DT)}{2} = \frac{V_O(1-D)D}{2(1+D)L_1 f_S} = I_{L1} \tag{24}$$

$$\frac{\Delta i_{L2}(DT)}{2} = \frac{V_O(1-D)D}{2(1+D)L_2 f_S} = I_{L2} \tag{25}$$

Using Equation (8), the design equation of Inductor L_1 and L_2 is obtained as

$$L_1 = \frac{(1-D)^2 DR_L}{2(1+D)^2 f_S};\ L_2 = \frac{(1-D)DR_L}{2(1+D)f_S} \tag{26}$$

The peak to peak voltage ripple of capacitor C_1, C_2 and C_O is calculated and rearranged to yield the design equations of the capacitor

$$C_1 = \frac{I_O D}{\Delta V_{C1} f_S};\ C_2 = \frac{I_O D}{\Delta V_{C2} f_S};\ C_0 = \frac{I_O D}{\Delta V_{CO} f_S} \tag{27}$$

3.5 Power loss and Efficiency analysis

The power losses and efficiency of the proposed topology are calculated by considering parasitic resistance, diode threshold voltage, and on-state resistance of the switch. In this calculation, R_{L1}, R_{L2} is the ESR of the inductor, R_{C1}, R_{C2} and R_{CO} are the ESR of the capacitor, R_{DS} and R_F are the on-state resistance of the switch and diode respectively. V_F is the diode threshold voltage.

RMS value of switch current:

$$I_{S(RMS)} = \begin{cases} I_{L1} + I_{L2} \ldots\ldots 0 < t < DT \\ 0 \qquad\qquad \ldots\ldots DT < t < T \end{cases} \tag{28}$$

$$I_{S(RMS)} = \sqrt{\frac{\int_0^{DT} I_{L1} + I_{L2}^{\,2} dt}{T}} = \frac{2\sqrt{D}[1+D]V_g}{R_L[1-D]^2}$$

Similarly, average and RMS currents of diodes are obtained as

$$I_{D1(avg)} = I_{D2(avg)} = I_O \tag{29}$$

$$I_{D1(RMS)} = I_{D2(RMS)} = \frac{I_O}{\sqrt{1-D}} \tag{30}$$

RMS value of capacitor current:

$$I_{C1(RMS)} = I_{C2(RMS)} = I_{C3(RMS)} = I_O\sqrt{\frac{1+D}{1-D}} \tag{31}$$

RMS values of the inductor currents are taken from Equation (8).

Total losses of the converter = $P_L + P_{SW} + P_D + P_C$

$$\begin{aligned} P_{loss} &= I_{L1}^{\,2} R_{L1} + I_{L2}^{\,2} R_{L2} + I_{S(RMS)}^{\,2} R_{DS} + \\ &+ I_{D1(avg)} V_F + I_{D1(RMS)}^{\,2} R_F + I_{D2(avg)} V_F + \\ &+ I_{D2(RMS)}^{\,2} R_F + I_{C1(RMS)}^{\,2} R_{C1} + I_{C2(RMS)}^{\,2} R_{C2} + \\ &+ I_{C3(RMS)}^{\,2} R_{C3} \end{aligned} \tag{32}$$

$$\text{Efficiency} = \eta = \frac{P_{out}}{P_{out} + P_{loss}} \tag{33}$$

3.6 Time domain and Frequency domain Analysis

3.6.1 Time domain analysis.

The important objective of investigating the time domain and frequency domain analysis of a converter is to design a control system. The desired requirement of the system can be attained by an appropriate design of control system. The converter taken for comparison combines the features of impedance source converter and quadratic boost converter [11]. This topology is derived to achieve high voltage gain. However, it can operate only with D<0.5 as positive output converter. Figure 5 gives the responses of the proposed topology and quasi Z source topology [11], which is taken for comparison. It is observed in Figure (a)-(d), the proposed topology has excellent settling time and less overshoot compared to the quasi Z source topology. The settling time of the proposed topology is just 42% of the converter taken for comparison, and the results are presented in Figure 5(c) and (d). The time domain analysis of both the converter explains the time response of the proposed converter, which takes less time for stable operation than the compared converter.

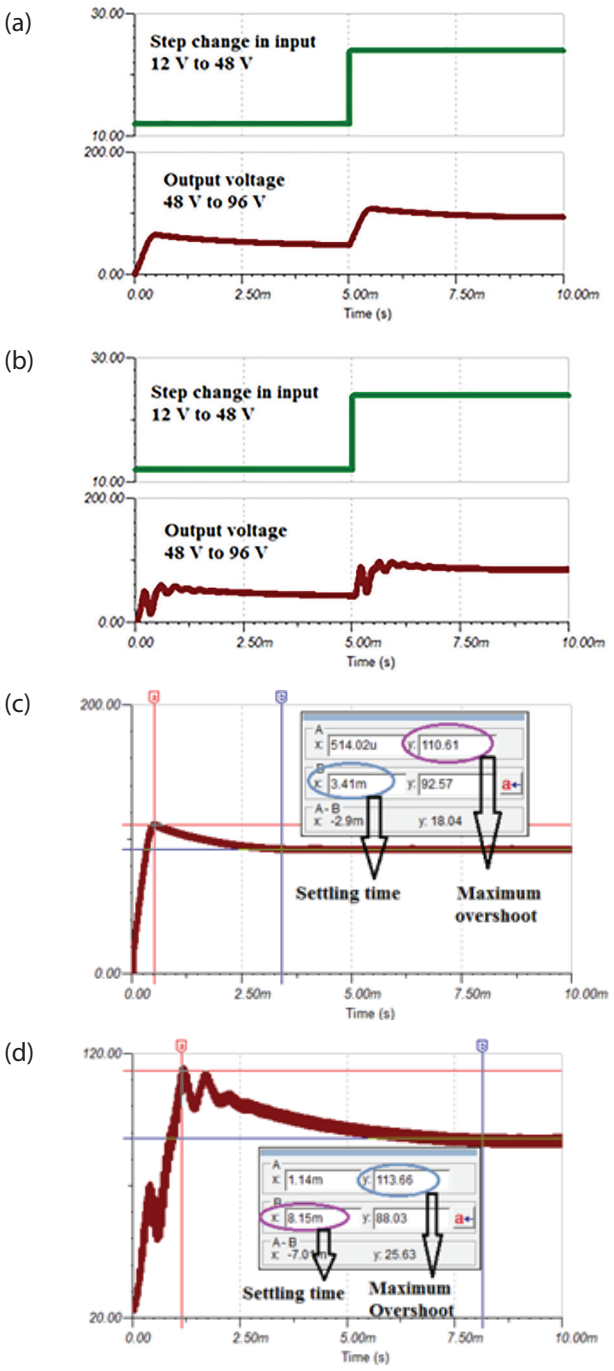


Figure 5: Time domain analysis (a) Output voltage of MQB converter for the step change in input.(b) Output voltage of Quasi Z source topology for the step change in input. (c) Settling time and maximum overshoot of MQB converter (d) Settling time and maximum overshoot of Quasi Z source topology

3.6.2 Frequency domain analysis.

To simplify the analysis, output capacitor of the converter is not considered. Order of the system is four. Figure 6 provides the signal flow graph of the MQB converter for small signal analysis.

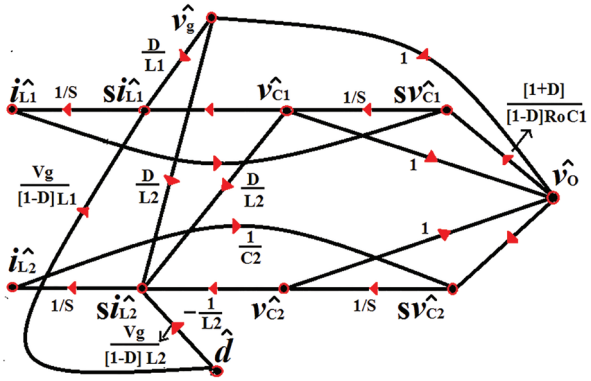


Figure 6: Small-signal analysis of MQB converter

Averaged and linearised state equations are derived using steady-state analysis to develop signal flow graph. By adding perturbation to the linearised equation, the AC equations are used to draw the signal flow graph[17]. Individual loop and non-touching loop gains are identified from the figure 6. Finally, forward path gains are traced to apply mason's gain formula to derive the transfer function.

Table 1 presents the values of the circuit parameters used for transfer function calculation to perform frequency domain analysis. Table 2 furnishes the complete frequency domain analysis of the proposed topology and the transfer functions are also provided in the table.The root locus diagram for input to output

Table 1: Circuit parameters for frequency domain analysis of the proposed topology

Po(W)	Vg(V)	Vo(V)	Ro(Ω)	fs(kHz)	L1(uH)	L2(uH)	C1(uF)	C2(uF)	Co(uF)
40	24	96	230	60	72	287	10	10	5

Table 2: Loops and their gains-SFG

Loops(L)	Loop gains	Non-touching loop gain
$L_1 = \tilde{i}_{L1} \rightarrow s\tilde{v}_{C1} \rightarrow \tilde{v}_{C1} \rightarrow s\tilde{i}_{L1} \rightarrow \tilde{i}_{L1}$	$I_{D2rms} = I_{DOrms} = \frac{I_O\sqrt{1-D}}{1-D}$	$L_1L_2 = \frac{-D'}{S^4L_1L_2C_1C_2}$
$L_2 = \tilde{i}_{L2} \rightarrow s\tilde{v}_{C2} \rightarrow \tilde{v}_{C2} \rightarrow s\tilde{i}_{L2} \rightarrow \tilde{i}_{L2}$	$L_2 = \frac{-1}{S^2L_2C_2}$	$L_1L_5 = \frac{-D'}{S^3L_1C_1C_2R_O}$
$L_3 = \tilde{v}_{C1} \rightarrow s\tilde{i}_{L2} \rightarrow \tilde{i}_{L2} \rightarrow s\tilde{v}_{C2} \rightarrow \tilde{v}_{C2} \rightarrow \tilde{v}_O \rightarrow s\tilde{v}_{C1} \rightarrow \tilde{v}_{C1}$	$L_3 = \frac{D[1+D]}{S^3L_2C_1C_2R_O[1-D]}$	$L_2L_4 = \frac{-[1+D]}{S^3L_2C_2C_1R_O[1-D]}$
$L_4 = \tilde{v}_{C1} \rightarrow \tilde{v}_O \rightarrow s\tilde{v}_{C1} \rightarrow \tilde{v}_{C1}$	$L_4 = \frac{[1+D]}{SC_1R_O[1-D]}$	
$L_5 = \tilde{v}_{C2} \rightarrow \tilde{v}_O \rightarrow s\tilde{v}_{C2} \rightarrow \tilde{v}_{C2}$	$L_5 = \frac{-1}{SC_2R_O}$	

Input to output transfer function

Forward paths(FP) from $\tilde{v}_g \rightarrow \tilde{v}_O$	Gain
$\tilde{v}_g \rightarrow s\tilde{i}_{L1} \rightarrow \tilde{i}_{L1} \rightarrow s\tilde{v}_{C1} \rightarrow \tilde{v}_{C1} \rightarrow \tilde{v}_O$	$FP_{g1} = \frac{-D}{S^2L_1C_1}$
$\tilde{v}_g \rightarrow \tilde{v}_O$	$FP_{g2} = 1$
$\tilde{v}_g \rightarrow s\tilde{i}_{L2} \rightarrow \tilde{i}_{L2} \rightarrow s\tilde{v}_{C2} \rightarrow \tilde{v}_{C2} \rightarrow \tilde{v}_O$	$FP_{g3} = \frac{D}{S^2L_2C_2}$
$\tilde{v}_g \rightarrow s\tilde{i}_{L1} \rightarrow \tilde{i}_{L1} \rightarrow s\tilde{v}_{C1} \rightarrow \tilde{v}_{C1} \rightarrow s\tilde{i}_{L2} \rightarrow \tilde{i}_{L2} \rightarrow s\tilde{v}_{C2} \rightarrow \tilde{v}_{C2} \rightarrow \tilde{v}_O$	$FP_{g4} = \frac{-D^2}{S^4L_1C_1L_2C_2}$

Transfer function:

$$\frac{\tilde{v}_O(s)}{\tilde{v}_g(s)} = \frac{\sum FP_{gK}\Delta_K}{\Delta} = \frac{FP_{g1}[1-L_2] + FP_{g2}[1-L_1-L_2] + FP_{g3}[1-L_1] + FP_{g4}}{1-L_1-L_2-L_3-L_4-L_5+L_1L_2+L_1L_5+L_2L_4}$$

Control to output transfer function

Forward paths(FP) from $\tilde{d} \rightarrow \tilde{v}_O$	Gain
$\tilde{d} \rightarrow s\tilde{i}_{L2} \rightarrow \tilde{i}_{L2} \rightarrow s\tilde{v}_{C2} \rightarrow \tilde{v}_{C2} \rightarrow \tilde{v}_O$	$FP_{g1} = \frac{V_g}{S^2[1-D]L_2C_2}$
$\tilde{d} \rightarrow s\tilde{i}_{L1} \rightarrow \tilde{i}_{L1} \rightarrow s\tilde{v}_{C1} \rightarrow \tilde{v}_{C1} \rightarrow s\tilde{i}_{L2} \rightarrow \tilde{i}_{L2} \rightarrow s\tilde{v}_{C2} \rightarrow \tilde{v}_{C2} \rightarrow \tilde{v}_O$	$FP_{g2} = \frac{-V_g}{S^4[1-D]L_1C_1L_2C_2}$
$\tilde{d} \rightarrow s\tilde{i}_{L1} \rightarrow \tilde{i}_{L1} \rightarrow s\tilde{v}_{C1} \rightarrow \tilde{v}_{C1} \rightarrow \tilde{v}_O$	$FP_{g3} = \frac{-V_g}{S^2[1-D]L_1C_1}$

Transfer function:

$$\frac{\tilde{v}_O(s)}{\tilde{d}(s)} = \frac{\sum FP_{gK}\Delta_K}{\Delta} = \frac{FP_{g1}[1-L_1] + FP_{g2} + FP_{g3}[1-L_2]}{1-L_1-L_2-L_3-L_4-L_5+L_1L_2+L_1L_5+L_2L_4}$$

and control to output transfer function are shown in Figure 7(a) and (c) respectively. Magnitude and phase plot for both the derived transfer functions are given in Figure 7(b) and (d) . From root locus in Figure 7(a), it is observed that the input to output transfer function has two complex poles and zeros and two real poles and zeros. One real pole and zero lie in the right half of the s-plane. Similarly, the control to output transfer function has two complex poles, two complex zeros and two real poles.One real pole lies in the right half of the s-plane. The status of pole-zero locations is given in Table 3.

Table 3: Poles and zeros of the open loops transfer function

Input to output transfer function				
Poles and zeros	Values	Damping	Overshoot (%)	Frequency (rad/sec)
Poles(4)	$2.6x10^4$	-1	0	$2.6x10^4$
	$-416+1.87x10^4i$	0.0223	93.2	$1.87x10^4$
	$-416-1.87x10^4i$	0.0223	93.2	$1.87x10^4$
	$-2.25x10^4$	1	0	$2.25x10^4$
Zeros(4)	$3.12x10^4$	-1	0	$3.12x10^4$
	$-2.18x10^4i$	0	100	$2.18x10^4$
	$+2.18x10^4i$	0	100	$2.18x10^4$
	$-3.12x10^4$	1	0	$3.12x10^4$
Control to output transfer function				
Poles and zeros	Values	Damping	Overshoot (%)	Frequency (rad/sec)
Poles(4)	$2.6x10^4$	-1	0	$2.6x10^4$
	$-416+1.87x10^4i$	0.0223	93.2	$1.87x10^4$
	$-416-1.87x10^4i$	0.0223	93.2	$1.87x10^4$
	$-2.25x10^4$	1	0	$2.25x10^4$
Zeros(2)	$3.05x10^4$ $x10^4i$	0	100	$3.05x10^4$
	$-3.05x10^4$ $x10^4i$	0	100	$3.05x10^4$

By investigating the bode diagram of $\tilde{V}_{\dot{O}}(s)/\tilde{V}_{\dot{g}}(s)$, it is understood that the magnitude curve of the function starts with a gain of 7.62 dB at $1.02X10^3$ rad/sec and the magnitude curve slope becomes -40 dB/dec. The phase curve has a phase reduction of -180°, so the curve reduced from 360° to 180°. Similarly, the magnitude and phase plot continue accordingly to the values of poles and zeros. Due to the presence of zero in the right of the s-plane and low value of phase margin, the system exhibits non-minimum phase behavior. Bode plot of the duty cycle to output transfer function is similar to previous transfer function bode plot except the phase margin is 0.0237°.

4 Advantages of the proposed converter

The proposed topology is compared with the quadratic boost converter and quasi Z source topology proposed in [11]. Even though the gain of the proposed converter is less compared to the quadratic boost converter for the same duty cycle, MQB converter's performance is superior compared to other two converters taken for the same power and voltage rating. Table 4 gives all the theoretical formula derived for the proposed topology and is tabulated along with the quasi z-source and the quadratic boost converter. Figures 8(a)-(d) furnishes the comparative graphs of the MQB converter with other converter taken for comparison. Figure 8(b) endows the capacitor voltage stress for different output voltage rating. The proposed converter has very low buffer capacitor stress compared to another converter.

Switch and diode voltage stress is determined using switch utilization (SUF) and diode utilization factor (DUF)

$$\text{SUF or DUF} = \frac{P_{rated}}{\sum_{M=1}^{n} V_M I_M} \tag{34}$$

Where V_M = voltage stress across the switch or diode.

I_M = current stress through the switch or diode.

Switch and diode utilization factors are calculated using the equation (34). From the Figure 8(c), it is observed that the SUF of the MQB converter is 1.7 and 2.7 times of the quadratic boost and quasi z-source topology respectively. Similarly, from the Figure 8(d), it is detected that the DUF of the MQB converter is 1.8 and 4.7 times of the quadratic boost and quasi z-source topol-

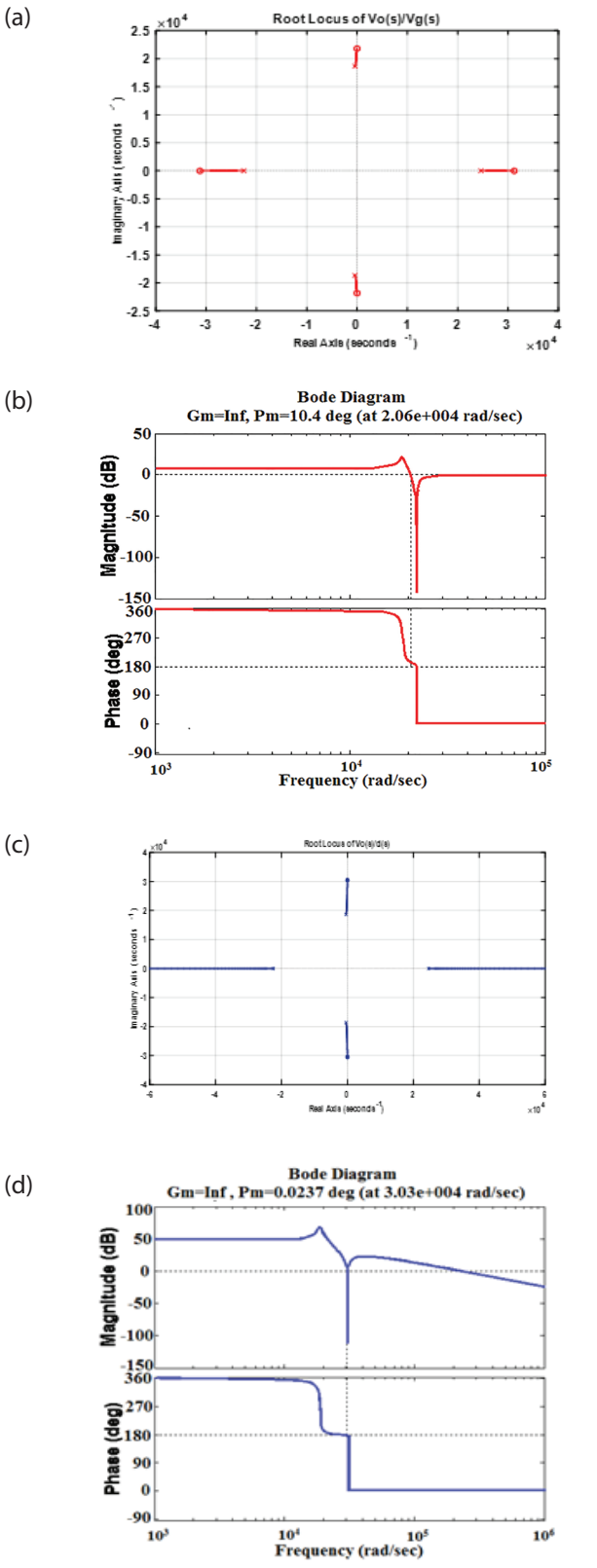


Figure 7: Frequency domain analysis (a) Root locus diagram of input to output transfer function (b) bode plot of input to output transfer function (c) Root locus diagram of control to output transfer function (d) bode plot of control to output transfer function

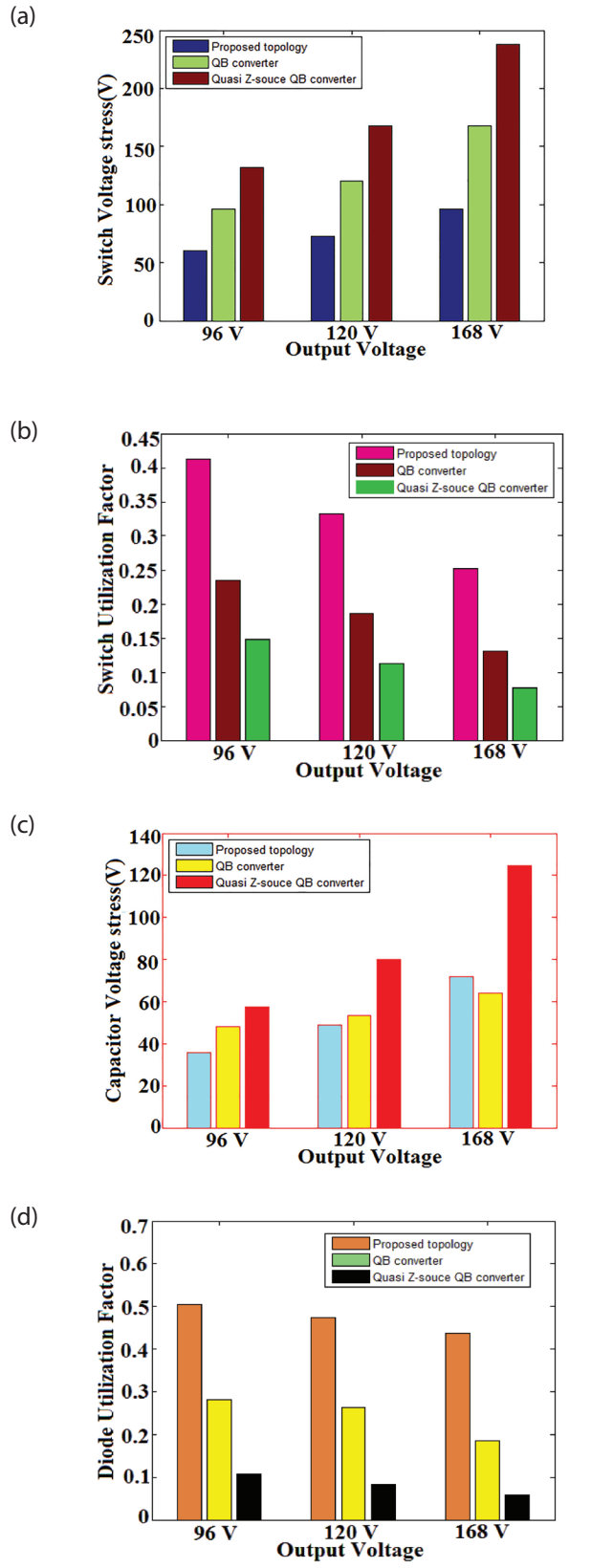


Figure 8: (a) Output voltage Vs switch voltage stress (b) Output voltage Vs capacitor voltage stress (c) Output voltage Vs switch utilization factor (d) Output voltage Vs diode utilization factor

ogy respectively. The proposed converter is also compared with the converter in [14]. It is observed that the gain of the converter in [14] is just similar to the proposed converter. The converter [14] achieves the same

Table 4: comparison of proposed converter with existing topology

Sno	Parameter	Proposed Topology	Quadratic boost converter	Quasi Z-source topology[11]
1	Voltage gain	$\frac{1-D^2}{(1-D)^2}$	$\frac{1}{[1-D]^2}$	$\frac{1}{1-2D}$
2	Inductor design	$L_1 = \frac{R_O[1-D]^2 D}{2[1+D]^2 f_S}$ $L_2 = \frac{R_O[1-D]D}{2[1+D]f_S}$	$L_1 = \frac{R_O[1-D]^4 D}{2f_S}$ $L_2 = \frac{R_O[1-D]^3 D}{2f_S}$	$L_1 = \frac{R_O[1-2D]^2 D}{2f_S}$ $L_2 = \frac{R_O[1-2D]D}{2[1-D]f_S}$ $L_3 = \frac{R_O[1-2D]}{2f_S}$
3	Switch voltage stress	$\frac{V_g}{1-D}$	V_O	$\frac{V_g[1+D]}{1-2D}$
4	Switch current stress	$\frac{2\sqrt{D}I_O}{1-D}$	$\frac{[2-D]\sqrt{D}I_O}{[1-D]^2}$	$\frac{2\sqrt{D}I_O}{1-2D}$
5	Diode current stress	$I_{D1rms} = I_{DOrms} = \frac{I_O}{\sqrt{1-D}}$	$I_{D1rms} = \frac{I_O\sqrt{D}}{[1-D]^2}$ $I_{D2rms} = I_{DOrms} = \frac{I_O\sqrt{1-D}}{1-D}$	$I_{D1rms} = I_{D3rms} = \frac{I_O\sqrt{1-D}}{1-2D}$ $I_{D1rms} = \frac{I_O\sqrt{D}}{1-2D}$
6	Capacitor Voltage stress	$V_{C1} = V_{C2} = \frac{V_g D}{1-D}$	$V_{C1} = \frac{V_g}{1-D}$	$V_{C1} = \frac{V_g}{1-D}$ $V_{C2} = \frac{V_g D}{[1-D][1-2D]}$
7	Diode voltage stress	$V_{D1} = V_{DO} = \frac{V_g}{1-D}$	$V_{D1} = V_{D2} = \frac{V_g}{1-D}$ $V_{DO} = V_O$	$V_{D1} = \frac{V_g}{1-D}$ $V_{D2} = \frac{2DV_g}{[1-D][1-2D]}$ $V_{D3} = \frac{V_g}{[1-D][1-2D]}$
8	Total device count	3-Diode;1-Switch; 2-Inductor 2-Capacitor	2-Diode;1-Switch 2-Inductor; 3-Capacitor	3-Diode;1-Switch;3-Inductor; 2-Capacitor
SUF(Switch Utilization Factor)(P_O = 40 W, V_g = 24 V, V_O = 96 V)				
9	SUF	0.412	0.235	0.148
DUF(Diode Utilization Factor)(P_O = 40 W, V_g = 24 V, V_O = 96 V)				
10	DUF	0.505	0.282	0.107

voltage conversion ratio with four capacitors whereas, with the proposed topology, it is three capacitors. The MQB converter possesses a total component count of 8 whereas the converter [14] has nine devices with 3-diodes, 4- capacitors, 2-inductors and a switch. Switch voltage stress in both the converters is observed to be same and it is measured by the equation Vg/[1-D].

5 Reliability study of the proposed converter

Reliability analysis is carried out with the help of FIDES guide [13]. Fides is a guide used for reliability computation of electronic components and structures. The reliability prediction is usually stated in FIT (number of failures for 10^9 hours). It is composed of two parts such as reliability evaluation and audit guide. It takes account of the mechanical and electrical stresses. In addition to that, it takes the complete life profile of the system. Reliability calculation helps to predict the failure rate of the converter by considering all the factor of the converter when it is integrated with the application. The reliability analysis is started by predicting the life profile of the converter used in trucks. The conditions such as operating time of the converter, the location of the application, the type of atmosphere where the converter is to be integrated, and the type of use must be tabulated which would be further used in the reliability prediction as in Table 5. In India, trucks are allowed to run only during night hours to avoid traffic. According to the traffic rules, life profile of the converter is designed.

The main objective of the reliability study is to calculate the mean time to failure (MTTF) of a converter when it is integrated into the application. The failure rates of every component that are incorporated in the converter circuit are to be calculated to find the mean time to failure. The failure rate that is calculated from the predictions are expressed in FIT (FIT = failure in 10^9 hours). The MTTF is calculated by the below equation.

$$\mathrm{MTTF} = \frac{1}{\lambda_S + \lambda_D + \lambda_C + \lambda_I} \tag{35}$$

λ is the symbol of failure rate and the general equation for calculating the failure rate is given in Equation (36). The failure rates are calculated for the capacitor, inductor, switch, and diodes.

$$\lambda = \lambda\mathrm{physical}.\ \Pi\mathrm{pm}.\ \Pi\mathrm{process} \tag{36}$$

The component junction temperature is calculated as below,

$$T_{j-comp} = T_{ambient} + R_{JA}.P_{dissipated} \tag{37}$$

In Equation (37), the power dissipation denotes the losses occurring in the diode and switch which are given in Equations (37) and (38).

$$P_{d1} = P_{dO} = \frac{V_f \times P_o}{V_o} + \frac{P_o^{\,2}}{(1-D)V_o^{\,2}}.R_f \tag{38}$$

$$P_{SW} = P_o^{\,2}\left\{\frac{4\,D\,R_{ds(on)}}{V_o^{\,2}(1-D)^2} + \frac{f_s.C_o}{(1-D)^2 I_o^{\,2}}\right\} \tag{39}$$

Table 5: Life profile of the converter

Condition		Temperature and humidity			Temperature cycling			
Phase title	Time (hrs)	On/Off	Ambient temp (˚C)	Relative humidity (%)	ΔT(˚C)	No of cycle (/ year)	Cycle duration (hrs)	Max temp during cycling (˚C)
Night/ on	3660	on	125	22	25	305	12	150
Day/ off	4380	off	35	20	10	365	12	45
Night/ off	720	off	30	30	5	60	12	35

Table 6: Specifications of the components

Component	Model no	Description
Diode	MUR510	TO-220AC [R_{JA} = 30 °c/w]
Switch	IRF 520	TO-220 [R_{JA}= 62.5 °c/w, Rds(on)= 0.23 Ω]
Capacitor	Aluminium solid electrolyte capacitor	[100V, 5A] 10-20 μF; Resr = 0.2 to 0.5 Ω
Inductor	Toroid, powered iron core wire wound inductor	17 μH, (Resr = 0.009 Ω) 303 μH (Resr = 0.091 Ω

The Table 6 shows the specifications of the components that are selected. From the stress values and the base failure rate values of the components, the failure rate value is calculated and tabulated in Table 7 along with the failure rate values of the compared quazi z source converter, which is calculated similarly.

Table 7: Failure rate values of components

Failure Rate	Proposed MQB Converter	Compared Quazi z converter
λ_S	384.04	451.1853
λ_D	2863.92	5037
λ_I	3.026	4.539
λ_C	101.304	110.4

The above failure rate values are used in the Equation (35) to calculate the mean time to failure of the converter which is given below.

For the proposed modified quadratic dc-dc boost converter,

$\lambda_S + \lambda_D + \lambda_C + \lambda_I = 3352.2787$ FIT

MTTF = 34.05 years

For the compared quadratic quazi z source converter,

$\lambda_S + \lambda_D + \lambda_C + \lambda_I = 5603.1243$ FIT

MTTF = 20.37 years

Thus from the reliability analysis, the mean time to failure is calculated. When comparing both the converters, the proposed modified quadratic boost converter can work without failure for nearly 14 year more than the compared converter due to the lesser number of component counts and reduced losses in the components. While including the controller circuit and the gate driver circuit the value might vary depending upon the methods used.

6 Simulation and experimental results

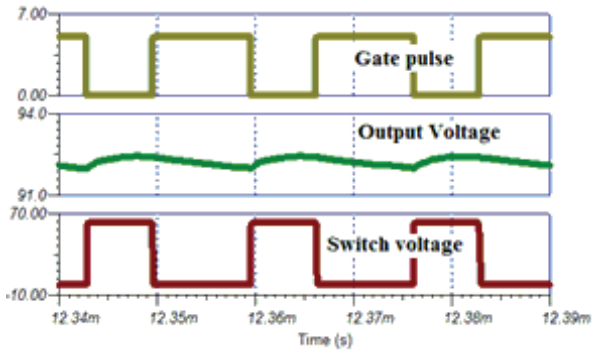
Simulation is carried out with Tina software and presented in the Figures 9(a)-(g). The proposed topology is simulated in Tina design suite TI version 9. The circuit response to the input voltage is calculated in the transient and mixed mode of Tina. In a transient analysis, the DC operating point can be calculated which is used to check with the theoretical results obtained from the steady-state analysis. By comparing the simulation results and the theoretical results, the values are more satisfactory. The voltage across the inductors and capacitors during turn ON and turn OFF period are same as that of the theoretical values. The calculated voltage gain and capacitor voltage by volt-second balance principle are more accurate to the simulation results.
(a) (b)

Figure 9(h) gives a pictorial representation of the efficiency between the converters, in the form of the graph. The efficiency analysis of converter is carried out by estimating the losses in the conversion process. The losses are mainly due to switching frequency, power diodes, passive elements such as inductor and capacitors. The output power versus the efficiency is plotted, and we infer from the graph that the converter's efficiency decreases with increase in the power ratings, but the rate of decrease in efficiency varies. The rate of decrease of the efficiency is less in proposed converter when compared to the compared converter. From the efficiency and loss analysis, it's more obvious that the proposed converter is much dominant than the compared converter.

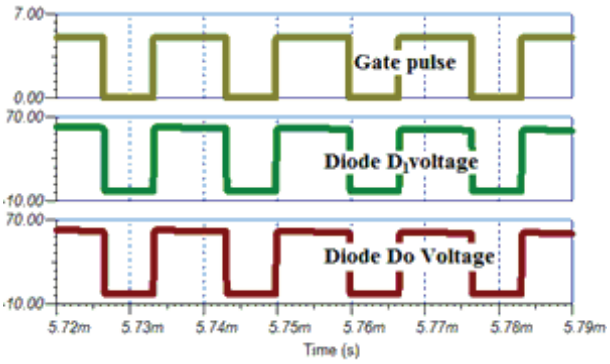
Figure 10 shows the hardware that is developed for the converter proposed. The dsPIC controller generates a switching pulse of 5 V amplitude and 20 kHz frequency. A power supply of 230 V is given to the transformer, which is stepped down to 15 V and 40 V respectively. 15 V is given to the dsPIC controller kit, and 40 V is given to the bridge rectifier circuit. The rectifier converts the 40 V AC to 40 V DC, which is given to the converter for input supply. The 15 V AC is again stepped down to 5 V

Table 8: Components of hardware circuit

Parameters		Components	
Input voltage	40 V	Switch	IRF520
Output power	40 W	Diode	MUR510
Switching frequency	20 kHz	Inductor	400 uH, 1 mH
Output voltage	93 V	Capacitor	10 uF
Duty cycle	0.4	dsPIC Controller	dsPIC33FJ64MC802
		Gate driver circuit	IRS2110



(a)



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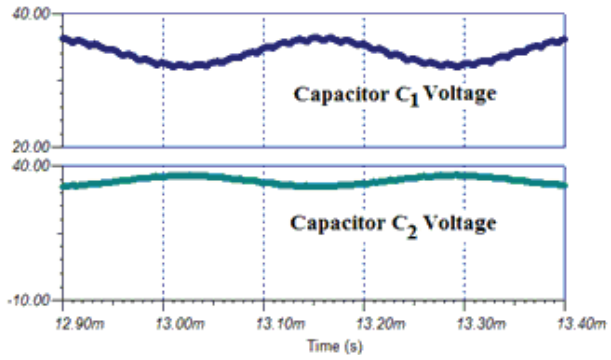

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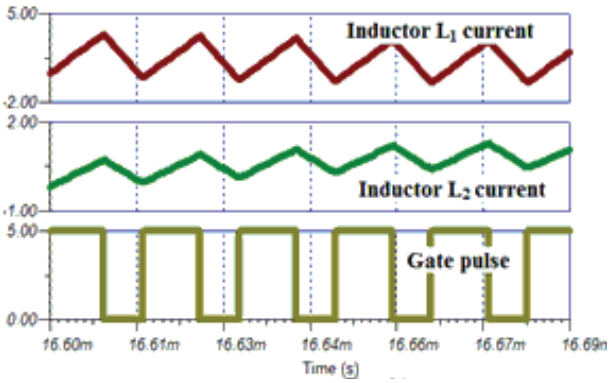

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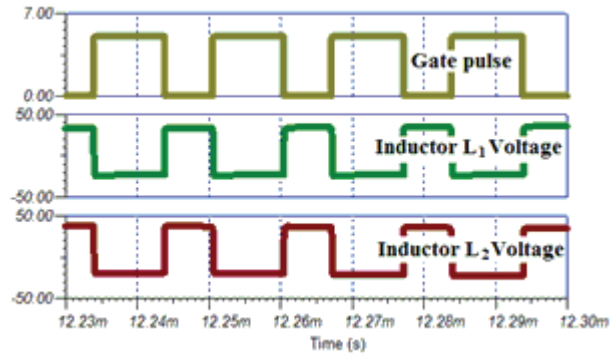

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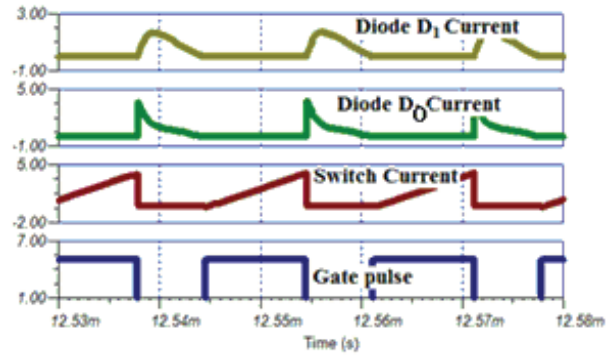

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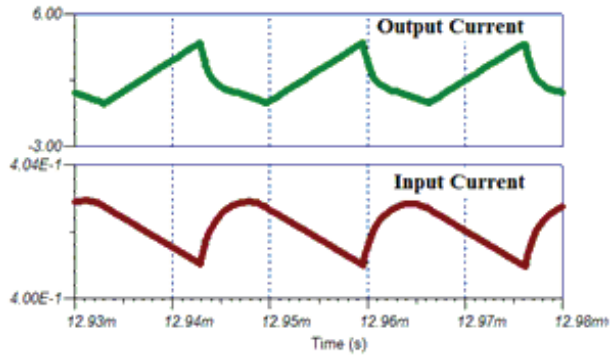
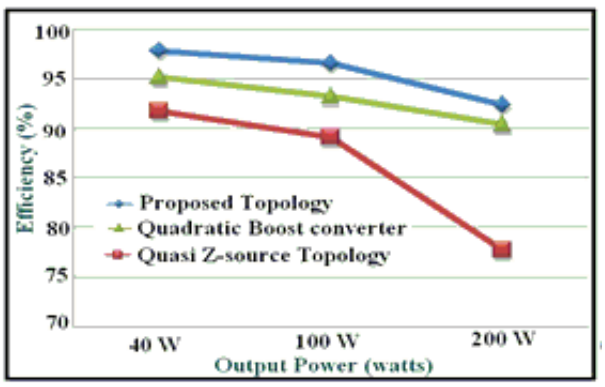


(g)



(h)

Figure 9: Simulation results (a) Output and Switch voltage (b) Diode voltages (c) Capacitor voltages (d) Inductor currents (e) Inductor voltages (f) Switch and diode currents (g) Input and output currents (h) output power Vs Efficiency.

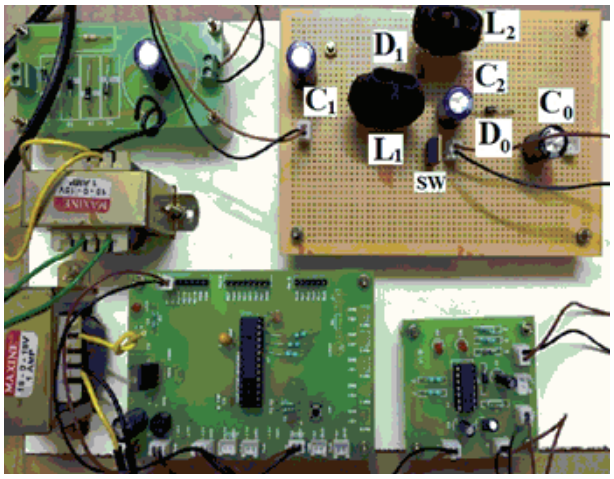


Figure 10: Photograph of the hardware

as a power supply to the controller and the gate driver circuit. Table 8 gives the components and parameters used for the hardware circuits

The Figure 11(a) shows the switching pulse waveform generated from the dsPIC controller with 0.4 duty cycle. The ON time of the switch is hence 40 % and the OFF time is remaining 60%. Thus for that duty cycle, the boost ratio is 2.33 and the output voltage for 40 V input is 90 V. The Figure 11(b) shows the input and output waveforms of the converter. The input voltage given to the converter is 40 V and the output voltage of the converter is 90 V. The channel 2 shows the output voltage and the channel 1 shows the input voltage. The voltage across the switch connected to the converter model is taken between drain and source and given in Figure 11(c). Theoretically, by $\frac{V_g}{1-D}$ the maximum switch voltage is 66 V, and it is observed that the hardware switch voltage is very close to the theoretical value. However, conventional quadratic boost converter has switch voltage stress equals to its output voltage. The proposed topology with low switch voltage stress uses low $R_{ds(on)}$ switches which reduces the cost of the component. A closer inspection shows that the hardware results validate the simulation and theoretical results. To increase the voltage gain, the coupled inductor can be incorporated. Thus, the proposed converter can be extended in the future for further increase in voltage conversion ratio.

7 Conclusion

The proposed topology for the operation of high-intensity discharge lamps has been described in this work. The same topology can be operated with PV source as an input. The converter is more suitable to

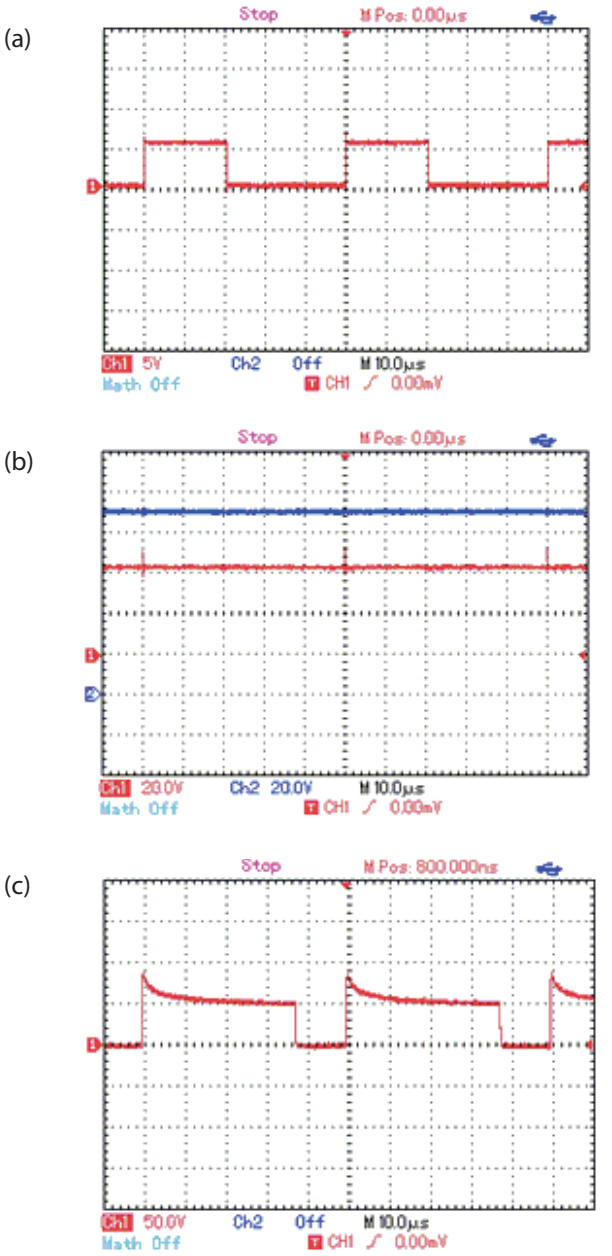


Figure 11: Experimental results (a) Gate pulse (Amp: 5 V/div; Time period: 10us/div) (b) Input and output voltage (Input voltage: Ch1: Amp: 20V/div; Time period: 10us/div; Output voltage: Ch2: Amp: 20V/div; Time period: 10us/div) (c) Voltage across the switch

be operated for lower power ratings and the efficiency decrease slightly with the increase in the power ratings. The output response with variation of input supply is studied in open loop conditions. The attractive features of the MQB converter are:

It has low buffer capacitor voltage stress.

SUF of the proposed converter is approximately 2-3 times greater than that of the compared converter.

Similarly, DUF of the MQB converter is 2-5 times higher than the converter taken for comparison. SUF and DUF of the proposed topology are very high compared to another converter. Therefore, it allows us to choose low rating semiconductor devices and which results in low cost of the devices.

The efficiency of the proposed converter is 6% higher as that of the compared converter for 40 W power rating, and the results of the output voltage and current make it more suitable for operation of the high-intensity discharge lamps.

The reliability of the MQB converter is about 15 years more reliable than the compared converter. The reliability analysis of the converter, when compared with the existing converter, shows that it is more reliable.

The hardware developed for the converter shows a satisfactory result for the voltage gain, which is found theoretically .In the future work, bidirectional version of the converter can be developed with the controller. The reliability analysis can be done for the gate driver circuit and the controller circuit so that it would give better details about the reliability analysis.

8 List of symbols and abbreviations

S	MOSFET switch
L_1, L_2	Inductor
C_1, C_2, C_O	Capacitors
R_L	Output resistor
D_1, D_O	Diodes
Vg	Input voltage
V_O	Output voltage
V_{L1}, V_{L2}	Inductor voltage
I_{L1}, I_{L2}	Inductor current
V_{C1}, V_{C2}	Capacitor voltage
D	Duty cycle
f_S	Switching frequency
G_{VCCM}	Voltage gain in CCM
G_{VDCM}	Voltage gain in DCM
Δi_{L1}, Δi_{L2}	Ripples in the inductor current
ΔV_{C1}, ΔV_{C2}	Ripples in the capacitor voltage
K_{crit1},K_{crit2}	Critical value of K at the boundary between the modes for L_1 and L_2
MQB	Modified quadratic boost
SFG	Switching flow graph
HID	High-intensity discharge
SUF	Switch utilization factor
DUF	Diode utilization factor
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
K_{cric1},K_{cric2}	Critical value decides CCM and DCM
$I_{S(RMS)}$, $I_{D(RMS)}$,	Switch and diode RMS current
$I_{D1(avg)}$, $I_{DO(avg)}$	Diode average current
$I_{L1(RMS)}$, $I_{L2(RMS)}$	Inductor RMS current
$I_{C(RMS)}$	Capacitor RMS current
P_{LOSS}	Power loss of the components
P_{out}	Output power
L_1, L_2…	Loop gains of signal flow graph
FP	Forward path in SFG
Gm	Gain margin
Pm	Phase margin
λ	Item failure rate
$\lambda_{Physical}$	Physical contribution
Π_{PM}	Part manufacturing
T_j	Component junction temperature (°C)
R_{JA}	Junction to ambient thermal resistance (°C/W)
MTTF	Mean Time to Failure

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Low-Voltage Highly Linear Floating Gate MOSFET Based Source Degenerated OTA and its Applications

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Abstract: The paper proposes a novel low-voltage highly linear floating gate MOSFET based source degenerated OTA. The low voltage operation of the proposed OTA is achieved by using floating gate MOSFETs as input transistors and the linearity is increased by using source degeneration linearization technique. The proposed OTA has low power supply requirement of ±0.6V, rail-to-rail input differential voltage range and wide bandwidth of 1.472 GHz. The applications of the proposed OTA such as active inductor, tunable resistors and filters are also proposed. Finally, the simulation results of the proposed circuits using typical parameters of UMC 0.18 µm CMOS technology are depicted to confirm the theoretical analysis.

Keywords: Active inductor; filters; floating gate MOSFET; OTA; resistors

Nizkonapetostni linearen vhodno izrojen OTA na osnovi MOSFETa s plavajočimi vrati in njegova uporaba

Izvleček: Članek predlaga nov nizkonapetostni linearen vhodno izrojen OTA na osnovi MOSFETa s plavajočimi vrati. Nizko napetostno delovanje je zagotovljeno z uporabo vhodnih MOSFET-ov s plavajočimi vrati, linearnost pa je povečana za uporabo tehnike izroditve vira. Predlagan OTA zahteva napajanje ±0.6V, polni diferencialen napetostni obseg in široko pasovno širino 1.472 GHz. Predlagana je uporaba OTA kot dušilka, nastavljiv upor in filter. Simulacijski rezultati v UMC 0.18µm CMOS tehnologiji potrjujejo teoretične analize.

Ključne besede: aktivna dušilka; filter; MOSFETR s plavajočimi vrati; OTA; upor

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1 Introduction

In recent years, with miniaturization of technology, the demand of low voltage power supply has become essential. For designing of analog circuits, it has become the major factor that they operate with low supply voltage and power as their digital counterparts. Analog designers face many difficulties and challenges due to the limited voltage headroom, because the threshold voltage and drain-to-source saturation voltage of CMOS technologies do not scale down at the same rate as the supply voltage or do not scale at all with low supply voltage. The power supply requirement of analog circuits can be reduced by two techniques known as technology modification and transistor implementation [1]. Using technology modification technique, the device technology dependent threshold voltage can be reduced. But, higher threshold voltage gives better noise immunity and the lower threshold voltage reduces the noise margin to result in poor signal to noise ratio (SNR). Hence, for present day CMOS technology, reduction in threshold voltage is limited to the noise floor level, below which further reduction will introduce an amount of noise sufficient to result in very complex circuits.

Some of the transistor implementation techniques available in literature are level shifters, self-cascode MOSFETs, sub-threshold MOSFETs, bulk-driven MOS-

FETs, floating gate MOSFETs [2-3], etc. Out of these floating gate MOSFETs present a unique advantage of programmability of threshold voltage, which can be lowered from its conventional value, thus makes it suitable for low voltage applications [4-5]. FGMOS is also compatible with standard double-poly CMOS process technology and has been used to develop digital-to-analog (D/A) converters [6], voltage controlled resistors [7]-[8], neural networks [9], operational transconductance amplifiers [5], dividers [8, 10], etc. Motivated by the unique characteristics of the floating gate MOSFETs, a highly linear OTA is proposed. The OTA is a versatile building block employed as the active cell in many analog integrated circuits such as continuous-time filters [11-14], variable gain amplifiers [15], etc.

The paper is organized as follows. The operation of floating gate MOSFET is discussed in Section 2. Section 3 proposes floating gate MOSFET based source degenerated OTA. The applications of proposed OTA such as active inductor, tunable resistors and filters are proposed in Section 4. In Section 5, simulation results are given to demonstrate the effectiveness of the proposed circuits. The paper is concluded in Section 6.

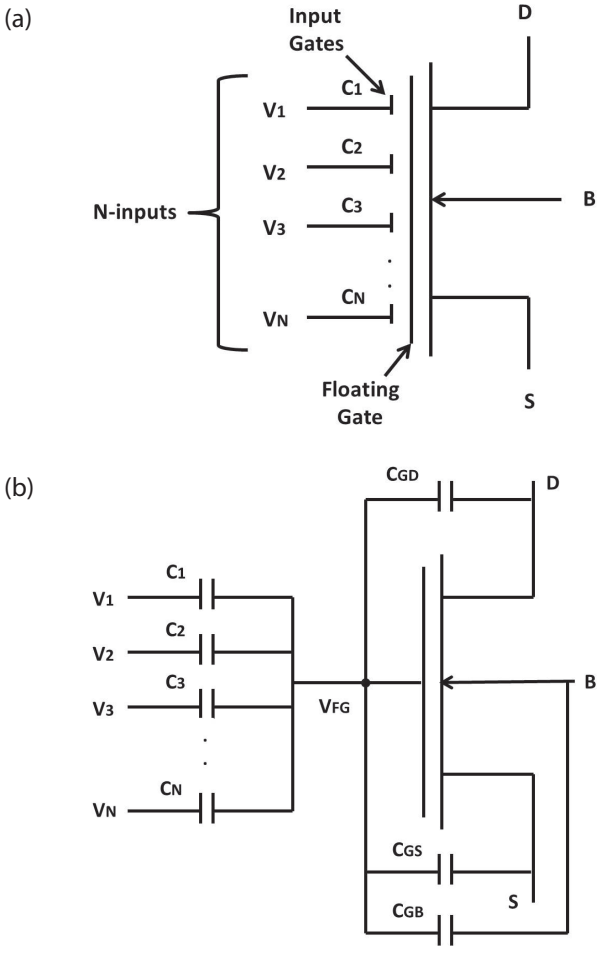

Figure 1: Floating gate MOSFET (a) Symbol and (b) equivalent circuit model

2 Operation of floating gate MOSFET

The structure of floating gate MOSFET is similar to a conventional MOSFET. The difference between these two is the gate, which is electronically isolated, creating a floating node in DC, and a number of secondary gates electrically isolated from the floating gate, above which they are deposited. There exist only capacitive connection between inputs and floating gate [16]. The floating gate which is completely surrounded by highly resistive material serves as charge storage device. Therefore, the first application of the floating gate MOSFET was to store the digital information for very long period in structures such as EPROMs, EEPROMs and Flash memories [17]. Along with this, floating gate MOSFET devices show easy addition and compression of voltage signals, as well as allow a reduction of the effective threshold voltage. The threshold voltage of a floating gate MOSFET can be controlled by the amount of the static charge stored in the floating gate. This property has prompted their use in low voltage low power analog circuits [18]. The symbol and equivalent circuit model of N-input floating gate MOSFET are shown in Figures 1 (a) and (b) respectively. In both the figures, V_i (for i=1, 2,…, N) are the control input voltages and D, S and B are the drain, source and substrate, respectively.

The drain current I_D of n-type N-input floating gate MOSFET in saturation region is given as [19, 20]:

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(W/L\right)\left(\frac{\sum_{i=1}^{N} C_i V_{iS}}{C_T} + \frac{C_{GD}}{C_T}V_{DS} + \frac{C_{GB}}{C_T}V_{BS} - V_T\right)^2 \quad (1)$$

Where μ_n is the electron mobility, C_{ox} is the gate-oxide capacitance per unit area, (W/L) is the aspect ratio, $\sum_{i=1}^{N} C_i$ is the sum of the N-input capacitances, V_{iS} is the applied input voltage at the i^{th} input gate with respect to source, V_{DS} is the drain-to-source voltage, V_{BS} is the substrate-to-source voltage, V_T is the threshold voltage, C_T $(= \sum_{i=1}^{N} C_i + C_{GD} + C_{GS} + C_{GB})$ is the total capacitance seen by the floating-gate, C_{GD} is the parasitic capacitance between floating-gate and drain, C_{GS} is the parasitic capacitance between floating-gate and source, and C_{GB} is the capacitance between floating-gate and substrate. Equation (1) can also be written as:

$$I_D = K_n\left(V_{FGS} - V_T\right)^2 \quad (2)$$

Where $K_n\left(=\frac{1}{2}\mu_n C_{ox}\left(W/L\right)\right)$ is the transconductance parameter and $V_{FGS}=\left(\frac{\sum_{i=1}^{N}C_i V_{iS}}{C_T}+\frac{C_{GD}}{C_T}V_{DS}+\frac{C_{GB}}{C_T}V_{BS}\right)$ is the voltage between floating gate and source of the floating gate MOSFET.

3 Proposed floating gate MOSFET based source degenerated OTA

The proposed floating gate MOSFET based source degenerated OTA is shown in Figure 2. The two differential pairs formed using two-input floating gate MOSFETs M_1, M_3 and M_2, M_4 are connected in series to reduce the distortion [21]. The transistors M_1-M_4 are biased in the saturation region. The differential pairs are also source degenerated by resistors R_1 and R_2. Two input voltages V_1 and V_2 are applied at one of the gate terminals of transistors M_1 and M_2, respectively. The proposed circuit is properly biased with current sources of same values connected to the source terminals of transistors M_1, M_2, M_3 and M_4.

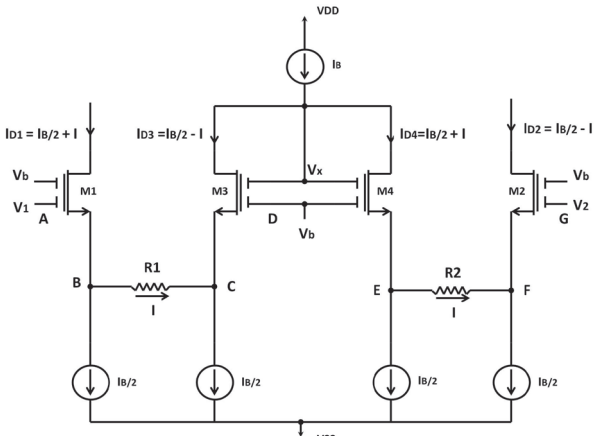

Figure 2: Proposed floating gate MOSFET based source degenerated OTA

Using (2), the drain currents I_{D1}, I_{D2}, I_{D3} and I_{D4} of transistors M_1, M_2, M_3 and M_4, respectively are given as

$$I_{D1}=\frac{I_B}{2}+I=K_n\left(V_{FGS1}-V_T\right)^2 \quad (3)$$

$$I_{D2}=\frac{I_B}{2}-I=K_n\left(V_{FGS2}-V_T\right)^2 \quad (4)$$

$$I_{D3}=\frac{I_B}{2}-I=K_n\left(V_{FGS3}-V_T\right)^2 \quad (5)$$

$$I_{D4}=\frac{I_B}{2}+I=K_n\left(V_{FGS4}-V_T\right)^2 \quad (6)$$

where I_B is the bias current, I is the current flowing through the resistors R_1 and R_2, K_n is the transconductance parameter, V_T is the threshold voltage, V_{FGS1} is the voltage between floating-gate and source of transistor M_1, V_{FGS2} is the voltage between floating-gate and source of transistor M_2, V_{FGS3} is the voltage between floating-gate and source of transistor M_3 and V_{FGS4} is the voltage between floating-gate and source of transistor M_4.

The voltages V_{FGS1}, V_{FGS2}, V_{FGS3}, and V_{FGS4} are given as

$$V_{FGS1}=\frac{C_1}{C_T}V_{1S}+\frac{C_2}{C_T}V_{bS}+\frac{C_{GD}}{C_T}V_{DS1}+\frac{C_{GB}}{C_T}V_{BS1} \quad (7)$$

$$V_{FGS2}=\frac{C_1}{C_T}V_{2S}+\frac{C_2}{C_T}V_{bS}+\frac{C_{GD}}{C_T}V_{DS2}+\frac{C_{GB}}{C_T}V_{BS2} \quad (8)$$

$$V_{FGS3}=\frac{C_1}{C_T}V_{xS}+\frac{C_2}{C_T}V_{bS}+\frac{C_{GD}}{C_T}V_{DS3}+\frac{C_{GB}}{C_T}V_{BS3} \quad (9)$$

$$V_{FGS4}=\frac{C_1}{C_T}V_{xS}+\frac{C_2}{C_T}V_{bS}+\frac{C_{GD}}{C_T}V_{DS4}+\frac{C_{GB}}{C_T}V_{BS4} \quad (10)$$

where C_1 & C_2 are input capacitances, V_{1S} & V_{2S} are the applied input voltages with respect to source at one of the gate terminals of transistors M_1 & M_2 respectively, V_X is the applied voltage with respect to source at one of the gate terminals of transistors M_3 & M_4, V_{bs} is DC bias voltage with respect to source, V_{DS1}, V_{DS2}, V_{DS3} & V_{DS4} are drain-to-source voltages of transistors M_1, M_2, M_3 & M_4 respectively, V_{BS1}, V_{BS2}, V_{BS3} &V_{BS4} are substrate-to-source voltages of transistors M_1, M_2, M_3 & M_4 respectively, and $C_T\left(=\sum_{i=1}^{N}C_i+C_{GD}+C_{GS}+C_{GB}\right)$ is the total capacitance seen by the floating-gate. Applying KVL in the loop ABCDEFG of Figure 2, the loop equation can be written as

$$V_1-V_{FGS1}-IR_1+V_{FGS3}-V_{FGS4}-IR_2+V_{FGS2}-V_2=0 \quad (11)$$

Substituting V_1-V_2= V_{in} (differential input voltage) and R_1=R_2=R, (11) is modified as

$$V_{in}-2IR=V_{FGS1}-V_{FGS3}+V_{FGS4}-V_{FGS2} \quad (12)$$

Using (7), (8), (9), and (10) in (12), the current (I) flowing through resisters R_1 and R_2 is given as

$$I = \frac{K_n\left(V_{in} - 2IR\right)}{2}\sqrt{\frac{I_B}{2K} - \frac{\left(V_{in} - 2IR\right)^2}{16}} \quad (13)$$

From Figure 2, the output current (I_{out}) of proposed OTA can be observed as

$$I_{out} = I_{D1} - I_{D2} = 2I \quad (14)$$

Using

(13) and (14), the output current (I_{out}) is given as

$$I_{out} = K_n\left(V_{in} - I_{out}R\right)\sqrt{\frac{I_B}{2K} - \frac{\left(V_{in} - I_{out}R\right)^2}{16}} \quad (15)$$

Equation (15) shows the relationship between output current (I_{out}) and differential input voltage (V_{in}) of proposed OTA. The transconductance of the proposed OTA can be calculated as

$$G_m = \frac{g_m}{1 + g_m R} \quad (16)$$

where $g_m = \sqrt{\frac{K_n I_B}{2}}$ is the transconductance of the transistors M_1-M_4. The nonlinear term in (15) depends on $V_{in} - I_{out}R$ rather than V_{in}. When $R >> 1/g_m$, the nonlinear term becomes zero and thereby high linearity can be achieved. The complete circuit of proposed OTA is shown in Figure 3, in which resistors R1 and R2 are replaced with the help of transistors M_{R1}-M_{R2} and M_{R3}-M_{R4}, respectively. These transistors (M_{R1}-M_{R4}) are operating in the ohmic region. The differential inputs V_1 and V_2 are applied at one of the input gates of floating-gate transistors M_1 and M_2 respectively and the output currents I_{out1} and I_{out2} are also taken out differentially, which allows the proposed OTA to be categorized as fully differential OTA. The fully differential structure of the OTA helps for better linearity as the even harmonics are cancelled out and only odd harmonics are left to contribute in total harmonic distortion. The common-mode voltage variations at the output nodes due to the fully differential structure can be stabilized by Common-Mode Feedback (CMFB) circuits. But the inclusion of CMFB circuits may results in stability issues as well as increases the complexity and power consumption. A current source formed by PMOS transistor M_5 is used for biasing purpose. Three current mirrors are formed using NMOS transistors M_6–M_{10}, M_{17}–M_{18}, M_{19}–M_{20} and two current mirrors are formed using PMOS transistors M_{11} – M_{13}, M_{14} – M_{16}. These current mirrors are used to copy the currents at the appropriate nodes of the circuit. The remaining transistors are used to transfer the currents at the appropriate nodes.

4 Applications of proposed OTA

The proposed OTA is used to develop some of the important analog building blocks such as active inductor, tunable resistors and filters.

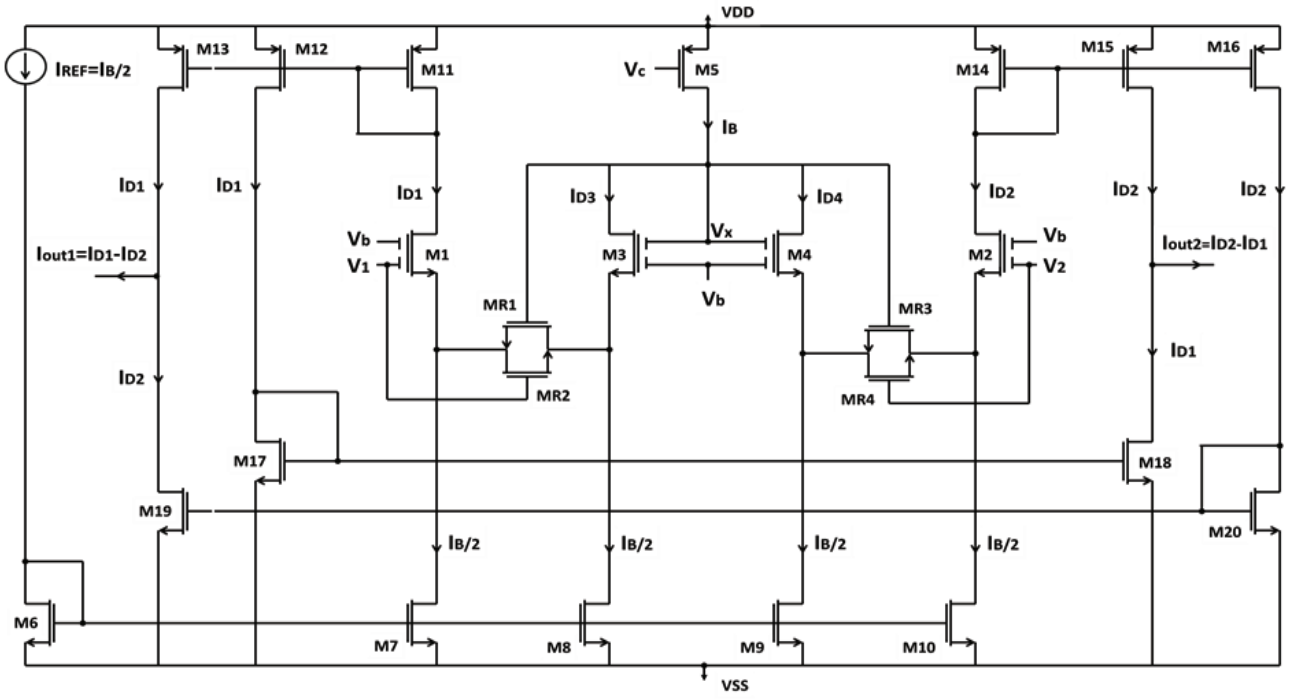

Figure 3: Complete circuit diagram of proposed OTA

4.1 Active inductor

The proposed active inductor is shown in Figure 4. The inductor has been developed using a capacitor C and two proposed OTA.

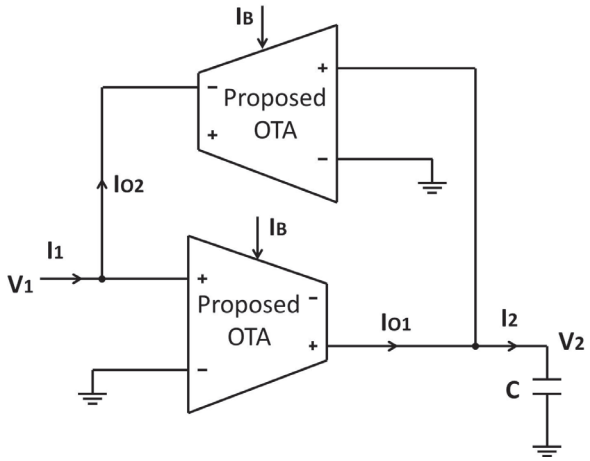

Figure 4: Proposed active inductor

In Figure 4, the current (I_2) flowing through capacitor C is given as

$$I_2 = I_{O1} = G_m V_1 \tag{17}$$

where G_m is the transconductance of the proposed OTA and V_1 is the input voltage.

The input current (I_1) can be written as

$$I_1 = I_{O2} = G_m V_2 = G_m \frac{I_2}{sC}; \tag{18}$$

where V_2 is the voltage across capacitor C.

Using (17) and (18), the current (I_1) is modified as

$$I_1 = \frac{V_1}{s\left(C/G_m^2\right)} = \frac{V_1}{sL_{eq}} \text{ ; where } L_{eq} = C/G_m^2 . \tag{19}$$

From (19), it can be seen that the value of equivalent inductance depends on the transconductance G_m of the proposed OTA.

4.2 Tunable resistors

Tunable resistors have a significant role in the analog circuit design because they can be employed as tuning elements in various analog circuit applications. The tunable floating and grounded resistors based on proposed OTA are shown in Figures 5 (a) and (b), respectively.

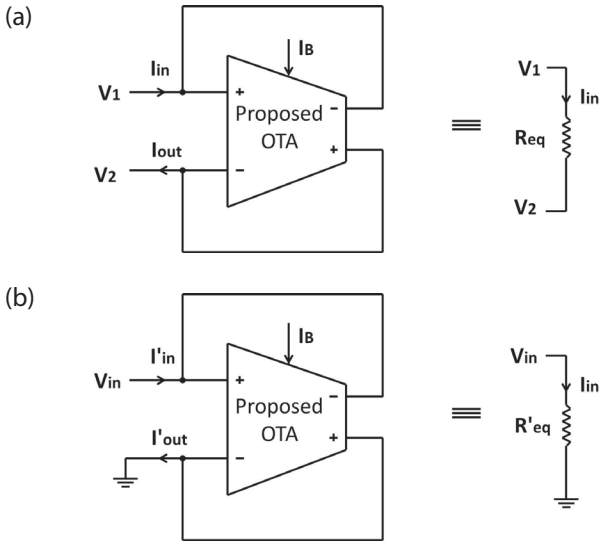

Figure 5: Proposed tunable resistors (a) floating resistor and (b) grounded resistor

In Figure 5 (a), the input current (I_{in}) is given as

$$I_{in} = I_{out} = G_m \left(V_1 - V_2\right) \tag{20}$$

where V_1 and V_2 are the input voltages and G_m is the transconductance of proposed OTA.

From (20), the equivalent resistance (R_{Feq}) is given as

$$R_{Feq} = \frac{\left(V_1 - V_2\right)}{I_{in}} = \frac{1}{G_m} ; \tag{21}$$

where

$$G_m = \frac{I_{in}}{\left(V_1 - V_2\right)}$$

The grounded resistor shown in Fig 5(b), it is observed that $V_2 = 0$, and $V_1 = V_{in}$. Substituting the values of V_1 and V_2 in (21), the equivalent resistance (R_{eq}) is given as

$$R_{eq} = \frac{V_{in}}{I_{in}} = \frac{1}{G_m^{'}} ; \text{ where } G_m^{'} = \frac{I_{in}}{V_{in}} \tag{22}$$

From (21) and (22), it can be seen that the equivalent resistances R_{Feq} and R_{eq} of floating and grounded resistors, respectively are varied with the transconductance.

4.3 Tunable filters

The tunable low-pass, high-pass and band-pass filters based on proposed OTA are presented.

4.3.1 Low-pass filters

The low-pass filters based on proposed OTA is shown in Figure 6.

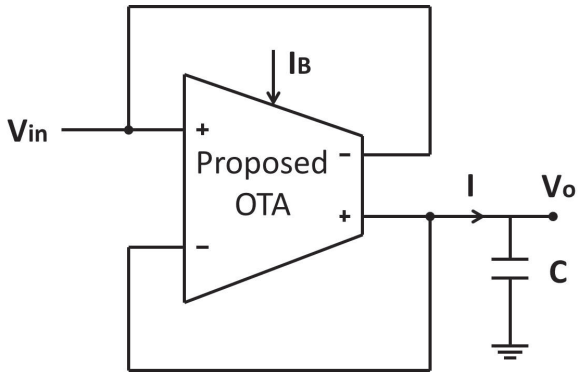

Figure 6: Proposed low-pass filter

In the figure, the current (I) flowing through capacitor C and the output voltage (V_0) are given as

$$I = G_m\left(V_{in} - V_0\right) \tag{23}$$

$$V_0 = I/sC \tag{24}$$

where G_m is the transconductance of proposed OTA. Using (23) and (24), the transfer function of first order low-pass filter can be written as

$$\frac{V_o}{V_{in}} = \frac{G_m}{G_m + sC} \tag{25}$$

4.3.2 High-pass filters

The high-pass filter based on proposed OTA is shown in Figure 7.

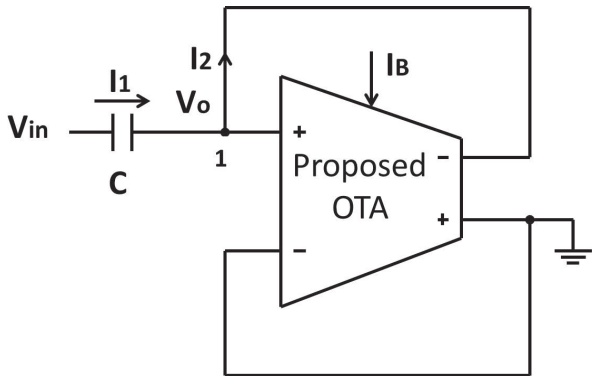

Figure 7: Proposed high-pass filter

In the figure, applying KCL at node 1, we get

$$\left(V_{in} - V_0\right)sC - G_m V_0 = 0 \tag{26}$$

where G_m is the transconductance of proposed OTA. From (26), the transfer function of first order high-pass filter can be written as

$$\frac{V_o}{V_{in}} = \frac{sC}{G_m + sC} \tag{27}$$

4.3.3 Proposed band-pass filters

The band-pass filter based on proposed OTA is shown in Figure 8. In the figure, applying KCL at nodes 1 and 2, we get

$$\left(V_{in} - V_1\right)sC_1 = G_m V_1 + \left(V_1 - V_0\right)G_m \tag{28}$$

$$sC_2 V_0 = G_m\left(V_1 - V_0\right) \tag{29}$$

Using (28) and (29), the transfer function of first order band-pass filter can be written as

$$\frac{V_o}{V_{in}} = \frac{sC_1 G_m}{s^2 C_1 C_2 + sG_m\left(C_1 + 2C_2\right) + G_m^2} \tag{30}$$

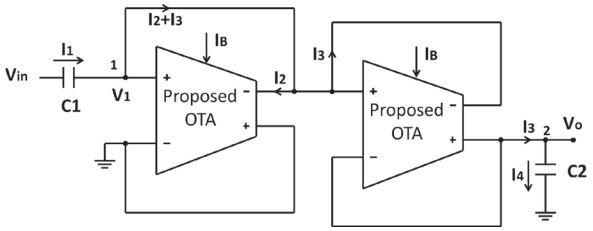

Figure 8: Proposed band-pass filter

5 Simulation results

In this Section, the simulation results of proposed OTA and its applications such as inductor, tunable resistors and filters are presented. The workability of all of the proposed circuits have been verified by Cadence EDA tool using typical parameters of UMC 0.18µm CMOS technology.

5.1 Simulation results of floating-gate MOSFET based source degenerated OTA

The DC transfer characteristic of the proposed OTA (Figure 3) is shown in Figure 9. From the plot, it can be seen that the output current of the OTA varies linearly with respect to the input differential voltage (V_{in}) and the range of the input differential voltage for linear operation is -0.6V to +0.6V.

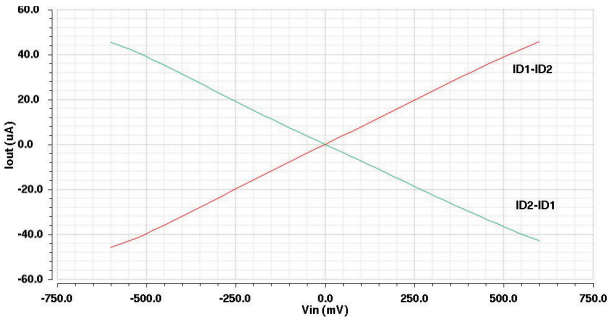

Figure 9: DC transfer characteristic of proposed OTA

The frequency response of the proposed OTA is shown in Figure 10. From figure, the transconductance is observed as -82.41dB (75.5µA/V) and the bandwidth is 1.47GHz for capacitive load of 1pF. Also, it is evident that the proposed OTA is stable as the gain is negative in decibels (dB) when phase angle is -180^0. The bandwidth gradually decreases for the larger values of capacitive loads.

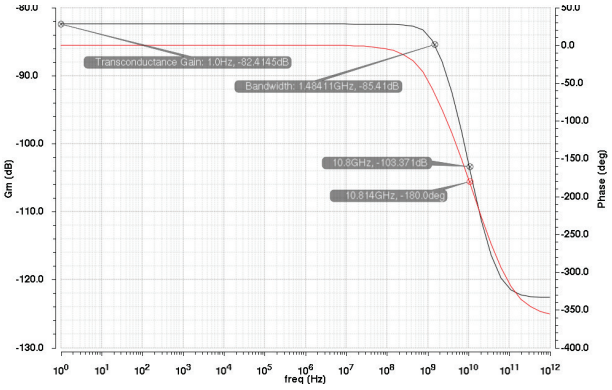

Figure 10: Frequency response of proposed OTA

The variation of the transconductance with respect to bias current (I_B), ranging from 120µA to 200µA with the increment of 20µA is plotted in Figure 11 and the corresponding values of transconductance are obtained as 70.08 µA/V, 72.78 µA/V, 75.54 µA/V, 80.18 µA/V and 87.85 µA/V, respectively.

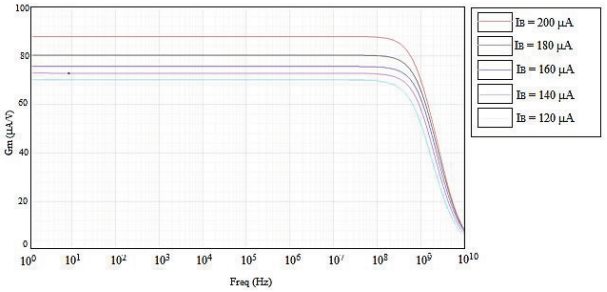

Figure 11: Variation of transconductance with respect to bias current (I_B)

For the distortion analysis of the proposed OTA, the sinusoidal differential input voltage of 5MHz with peak-to-peak amplitude ranging from 0.1V to 1.2V is employed.

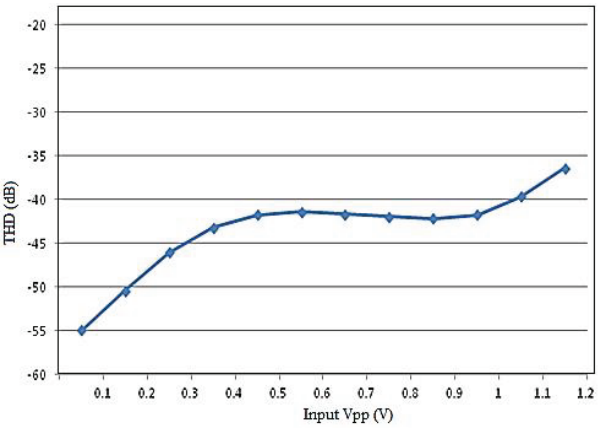

Figure 12: Total Harmonic Distortion plot of proposed OTA

Table 1. Comparison of proposed OTA with other OTAs available in literature

References	Power Supply (V)	Gm (µA/V)	Bandwidth (MHz)	Input Range (Vpp)	Power Consumption (mW)	THD (db) @Frequency (MHz) @Input (Vpp)
[22]	±0.9	22	-	1	0.057	-
[23]	1.5	40	65	0.95	0.126	-110@0.001@0.35
[24]	0.8	28.4	-	0.8	0.0312	-40@1@0.8
[25]	1.5	155	40	0.6	0.042	-55@5@0.1
[26]	2	266	175	0.6	0.160	-48@0.001@0.4
[27]	±1.5	850	780	0.4	20	-
[28]	±1.5	46	-	3	2.6	-60@0.1@3
[29]	0.5	245	10	0.5	0.11	-45@5@0.4
[30]	0.7	-	-	1.4	0.010	-35@5@0.4
Proposed work	±0.6	75.5	1472	1.2	0.56	-42@5@1

Figure 12 shows the total harmonic distortion (THD) obtained in the output waveform as a function of the peak-to-peak input voltage and it is observed that for differential input voltage (V_{in}) ranging from 0.1V to 1V, distortion is still low (≤ -42dB). The comparison between the performance parameters of proposed highly linear floating gate MOSFET based source degenerated OTA with the existing OTAs available in literature is listed in Table 1. From the table it is observed that the proposed circuit has rail-to-rail input voltage range with low power supply and high bandwidth.

5.3 Simulation results of active inductor

For the simulated inductances the value of the capacitance (C) is chosen as 1pF. The values of equivalent inductance (L_{eq}) are obtained as 0.129 mH, 0.155mH, 0.175 mH, 0.188 mH and 0.203 mH for different values of transconductance (Gm) as 87.85 µA/V, 80.18 µA/V, 75.54 µA/V, 72.78 µA/V and 70.08 µA/V, respectively.

5.4 Simulation results of proposed tunable resistors

Figure 13 shows the I-V characteristics of the floating resistor (Figure 5(a)) operating at supply voltages of ±0.6V. The current I_{in} is plotted for various values of V_2 ranging from -0.3V to 0.3V with the increment of 0.15V, while V_1 is varied from -0.3V to 0.3V. From the plot, it can be seen that the proposed circuit behaves as linear floating resistor over the differential input voltage range from -0.3V to 0.3V. The values of the equivalent resistance (R_{Feq}) are obtained as 9.21 KΩ, 8.84 KΩ, 8.69 KΩ, 8.43 KΩ and 8.21 KΩ for V_2 equals to -0.30V, -0.15V, 0V, 0.15V and 0.30V, respectively. Also, the grounded resistor is realized by connecting the second input voltage source (V_2) to the ground. The values of the equivalent grounded resistor (R_{eq}) for different values of applied bias current (I_B) as 120 µA , 140 µA, 160 µA , 180 µA and 200 µA are obtained as 10.82 KΩ , 9.5 KΩ, 8.69 KΩ, 7.75 KΩ and 7.19 KΩ, respectively.

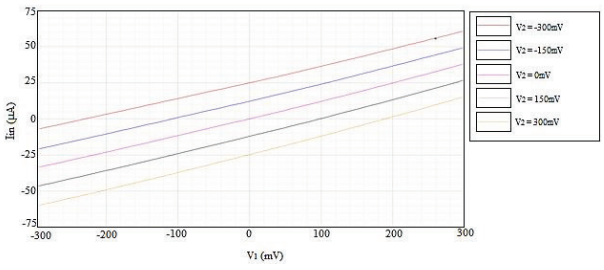

Figure 13: DC characteristic of proposed floating resistor

5.5 Simulation results of proposed filters

The proposed OTA is used to develop first order low pass, high pass and band pass filters. The frequency response of first order low pass, high pass and band pass filters for various values of bias current ranging from 120µA to 200µA with the increment of 20µA are shown in Figures 14 (a), (b) and (c), respectively.

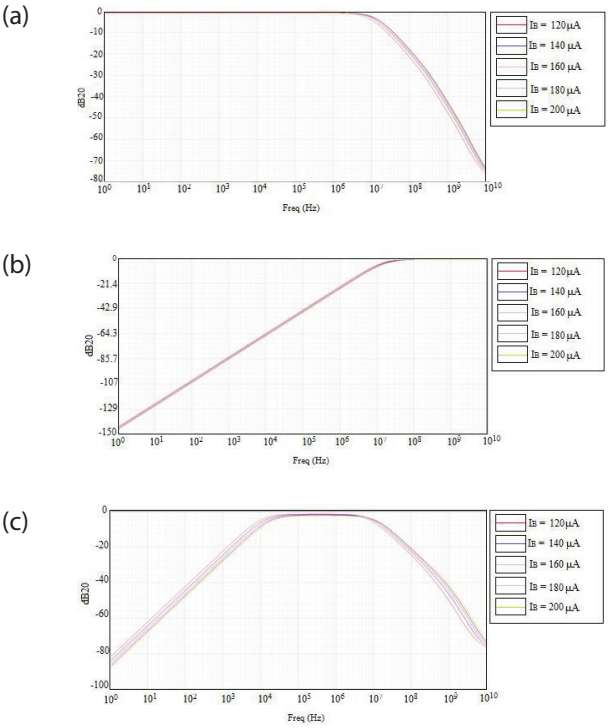

Figure 14: Frequency response of proposed first order: (a) low pass, (b) high pass and (c) band pass filters

6 Conclusions

A highly linear floating gate MOSFET based source degenerated OTA is developed. The proposed OTA utilizes floating gate MOSFETs to reduce the power supply requirement of the circuit and source degeneration technique is used to increase the linearity of the designed OTA. The proposed OTA operates at ±0.6V power supply. The circuit has rail-to-rail input voltage range with transconductance gain of 75.5µA/V. The 3db bandwidth of the designed OTA is 1.47GHz. The proposed OTA has wide input voltage differential range, low power supply requirement and high bandwidth.

7 Acknowledgment

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Analog Circuit Topology Representation for Automated Synthesis and Optimization

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Abstract: For several decades, computers have helped analog designers with circuit simulation and evaluation. To further simplify and speed-up designer's work, novel methods are being introduced that help to fine-tune numerical parameters to meet the performance criteria. With a lack of capable engineers, a shortage of specific knowledge or time to design an analog building block, software for fully automated synthesis of both topology and parameters is becoming crucial. Most research in this field is based on circuit modifications according to evolutionary principles of survival of the fittest. One of the challenges of the design of appropriate software is a representation of a circuit topology that will allow topology modifications with the smallest possible computational effort. Many existing solutions suffer either from the uncontrolled growth of the size of the circuit (so-called bloat) or from the limitation of the topology structure to a set of predefined blocks. In this paper, we discuss an analog circuit topology representation in a form of a binary upper-triangular matrix that is both bloat safe and offers a large solution space. We describe the basic structure of the matrix, the redundancy phenomena of logical elements, and the translation of the matrix representation to a regular SPICE netlist. We use an evolutionary algorithm to evolve the topology matrix and a classical parameter optimization algorithm to tune the circuit parameters. Based on a high-level circuit definition and a fixed building-block bank, our topology representation technique showed success in a fully automatic synthesis of passive circuits. We demonstrate the ability to automatically discover a passive high-pass filter topology.

Keywords: Automated synthesis, analog circuits, computer-aided design, evolutionary algorithms

Zapis topologije analognega električnega vezja za namen avtomatske sinteze in optimizacije

Izvleček: V procesu načrtovanja analognih električnih vezij računalniki že desetletja sodelujejo kot orodje za simulacijo ter evalvacijo. V pomoč pri delu razvijalca so že sedaj na voljo orodja, ki so sposobna avtomatično optimizirati numerične parametre vezja in s tem doseči določene kriterije delovanja. Zaradi pomanjkanja inženirjev, znanja in časa za razvoj analognih sklopov je smiselno razmišljati o programski opremi, ki bi bila zmožna ne samo izbrati primerne parametre za doseganje zahtevanih lastnosti temveč tudi sestaviti ustrezno topologijo. Večina dosedanjega dela na tem področju temelji na spreminjanju posameznih delov topologij po evolucijskih principih. Eden od glavnih izzivov pri razvoju tovrstnega orodja je računalniška predstavitev topologije vezja na način, ki bo omogočal računsko čim manj zahtevno spreminjanje topologije. Ena od slabosti nekaterih obstoječih rešitev je velika možnost nekontrolirane rasti sheme vezja preko vseh meja med iskanjem rešitve (t.i. napihovanje, angl. bloat), druga pogosta pomanjkljivost pa je vnaprejšnja omejitev strukture topologije. V tem članku predlagamo zapis predstavitve topologije analognega električnega vezja v obliki binarne zgornje trikotne matrike, ki omogoča ogromen iskalni prostor, hkrati pa zagotavlja imunost pred razlezenjem med postopkom iskanja. Opisujemo osnovno strukturo primernega matričnega zapisa, fenomen redundance logičnih elementov ter razložimo pretvorbo matrike v standarden zapis vezja (angl. netlist) primeren za obdelavo v simulatorju SPICE. Matriko nato spreminjamo s pomočjo posebnega evolucijskega algoritma, številske parametre vezja pa z eno od obstoječih metod za numerično optimizacijo. Primernost zapisa za popolnoma avtomatično sintezo analognega vezja smo preizkusili na primeru razvoja pasivnih vezij. Na podlagi visokonivojske zahteve ter vnaprej znane knjižnice možnih električnih elementov je algoritem sestavil pasivni visokoprepustni filter.

Ključne besede: Avtomatska sinteza, analogna vezja, računalniško-podprto načrtovanje, evolucijski algoritmi

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1 Introduction

The designing of an analog circuit is a demanding task even for a skilled analog designer. Due to constantly increasing time-pressure, lack of experienced engineers and growing industry needs, designers more and more often use computers to support the design process.

Computers and dedicated software have been used to aid the circuit designers since the introduction of SPICE [1]. Soon, designers started to use various mathematical methods to optimize circuit parameters to reach or even overcome the desired performance (e.g., [2], [3], [4], [5]). However, the optimization of the parameters alone is often not enough to meet the required objectives. In that case, a designer needs to rearrange the topology, which means that the parameters have to be optimized again. The recent advances in the field of analog circuit computer-aided design have to do with the combined automatic parameter optimization and the topology calculation of a desired circuit [6].

Majority of the topology search methods use some kind of evolutionary computation, and some early examples of the approach are IDAC [7], OASYS [8], OPASYN [9] and DARWIN [10]. Those early approaches were based on a random selection of topology parts from a predefined library. Consequently, the topology structure was fixed in advance, which seriously limited the size of the solution space. However, the invention of genetic programming (GP) by Koza et al. [11] has mainly removed this limitation and opened door for the first serious attempts in automated topology design. GP is an idea of automated development of a computer program using an evolutionary algorithm. Each program is presented by a tree-like structure, where branches and leaves represent various computer instructions. Koza already proposed this method for automated analog circuit synthesis, where a computer program was built using instructions for setting up a circuit topology [12]. One of the main problems of GP is so-called *bloat*, a phenomenon of an uncontrolled growing of a program tree. Lohn and Colombano [13] proposed a linearization of the circuit-building instructions, which inherited both advantages and disadvantages of standard GP. A binary or *switching* rectangular topology matrix representation was proposed by Györök [14]. His proposal, however, did not include further reproduction mechanisms and was not designed for fast checks of a single terminal connectivity. Gan et al. [15] suggested an undirected weighted graph representation where graph vertices represent component nodes, while component types and values are represented by branch weights. The idea results in a relatively efficient, lightweight circuit representation, but is limited to basic passive two-terminal components.

All the above-mentioned issues mainly stem from an inappropriate representation of a circuit topology. It is therefore vital for the successful computerizing of the analog circuit synthesis to have a suitable topology representation, which is the main focus of our paper.

The structure of this paper is as follows. In the following section we discuss the main idea behind of our analog circuit representation and its basic properties. We also present algorithms that allow conversion to a SPICE netlist. Later, in Section 3 we describe the algorithm used to alter and evolve the circuit topology in such a way that a solution fits the high-level requirements given at the beginning. In Section 4, we show that our approach is indeed successful in synthetizing an analog circuit from scratch.

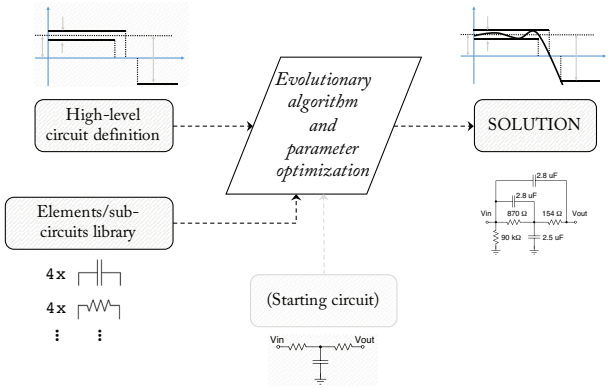

Figure 1: The main idea behind our analog circuit topology synthesis tool.

2 Circuit representation technique

Figure 1 summarizes the concept of our approach. Central to the synthesis is an evolutionary algorithm that searches for an optimal topology, augmented with an additional parameter optimization method. The algorithm builds the population of circuits using the elements and sub-circuits from the library according to the rules that we describe in this section. During the evolution and optimization process, a specified high-level circuit definition serves as a cost function, which the algorithm tries to minimize. The whole process can be arbitrarily biased with a starting circuit.

There are several requirements that we have to consider in order to obtain a circuit representation suitable to be used in the above described process. The representation should…

- … lend itself to computationally inexpensive modification of topology;
- … be able to prevent uncontrolled growing of a circuit;
- … provide a large search space;
- … allow simple detection of forbidden or unwanted connections.

2.1 The Topology matrix

Probably the most obvious way of decoding a circuit topology is an upper-triangular square binary matrix as shown in Figure 2. The matrix has one row and column assigned to each one of the terminals of all of the elements from the library as well as all the possible main terminals such as GND, V_{in}, V_{out} and similar. The size of the matrix does not change during the evolution. Rather, an element is connected or disconnected from the circuit by setting the corresponding matrix elements to one or zero. Specifically, in order to connect two terminals together, we put a logical one to a place where a row representing the first terminal intersects the column representing the second terminal. By definition, every terminal is connected to itself. That is why the matrix has all ones on the principal diagonal. That way, we can form any possible topology using the elements from the library.

It is obvious that an element is excluded from the final circuit when none of the rows or columns belonging to that element contain any ones (except for the diagonal elements, which connect each terminal to itself). Notice, however, that there are other cases that also exclude an element from the circuit. For example, an element is also excluded when only one of its terminals is connected elsewhere or all of its terminals are short-connected together.

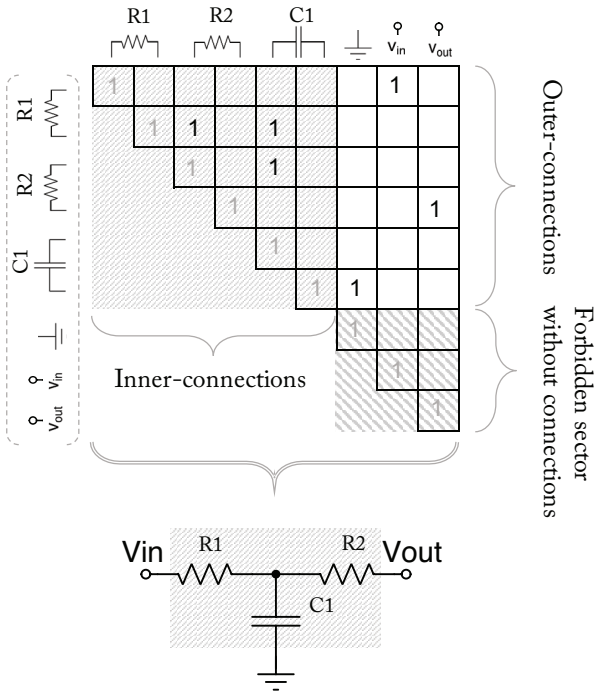

Figure 2: An example of a topology matrix, its main sectors, and the actual circuit that the matrix encodes.

Notice that the topology matrix contains several sectors. The first one is a so-called Inner-connections sector, where all connections between elements and sub-circuits are defined. The second one, the Outer-connections sector, contains all the connections to the outside world. It is easy to detect certain forbidden connections in this sector. Namely, there should only exist a single logical one in each row; otherwise, some outer terminals would be connected together, which is nonsense from the design point of view. There is one more sector (the Forbidden sector), within which no connections are allowed. The reason is the same as before—the outer terminals should not connect to each other. It is very important that we are able to detect some of these nonsense situations easily even before we start a computationally expensive circuit simulation.

2.2 Redundant connections

Consider the Inner-connections sector of the topology matrix depicted in Figure 2. It turns out that exactly the same topology can be represented by four different encoding patterns as shown in Figure 3. Namely, as soon

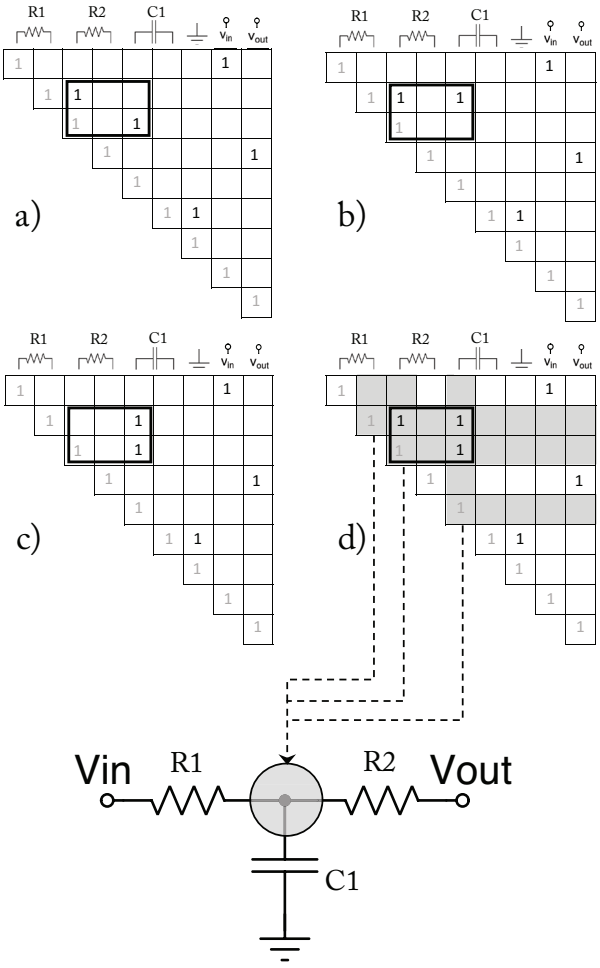

Figure 3: Four different Inner-connections parts of the topology matrix that represent the same T-type circuit.

as we connect two different terminals to a third terminal, we automatically connect the first two terminals together as well. We can observe a similar phenomenon in the genetic code of living organisms, referred to as *degenerate genetic code* [16]. Code degeneracy is important in preserving genotypic diversity as different genotypes (matrix encodings in our case) can represent the same phenotype (a resulting circuit in our case). It is however crucial to have all the connections (even the redundant ones) encoded in the matrix when it comes to creating a netlist to be used by a simulation software like SPICE. By creating a fully redundant matrix, terminals are identified with all joint nodes. As seen on Figure 3 d), all logical fields marked grey belong to a joint node between R1, R2 and C1. The first step of building a SPICE netlist from a topology matrix is therefore filling the matrix with all the redundant connections.

The basic idea behind the procedure of filling the matrix with all the redundant connections is to find all the incomplete rectangles (formed by exactly three logical ones in any three of their four vertices) and fill the remaining vertex with a logical one as well. The algorithm that implements this reads as follows (see also Figure 4):

Repeat
(check up and right, insert diagonally) Scans the matrix along its diagonal from left to right and looks for a missing logical one in the direction (*x*, *-y*). This finds all the rectangles with one existing vertex placed verti-

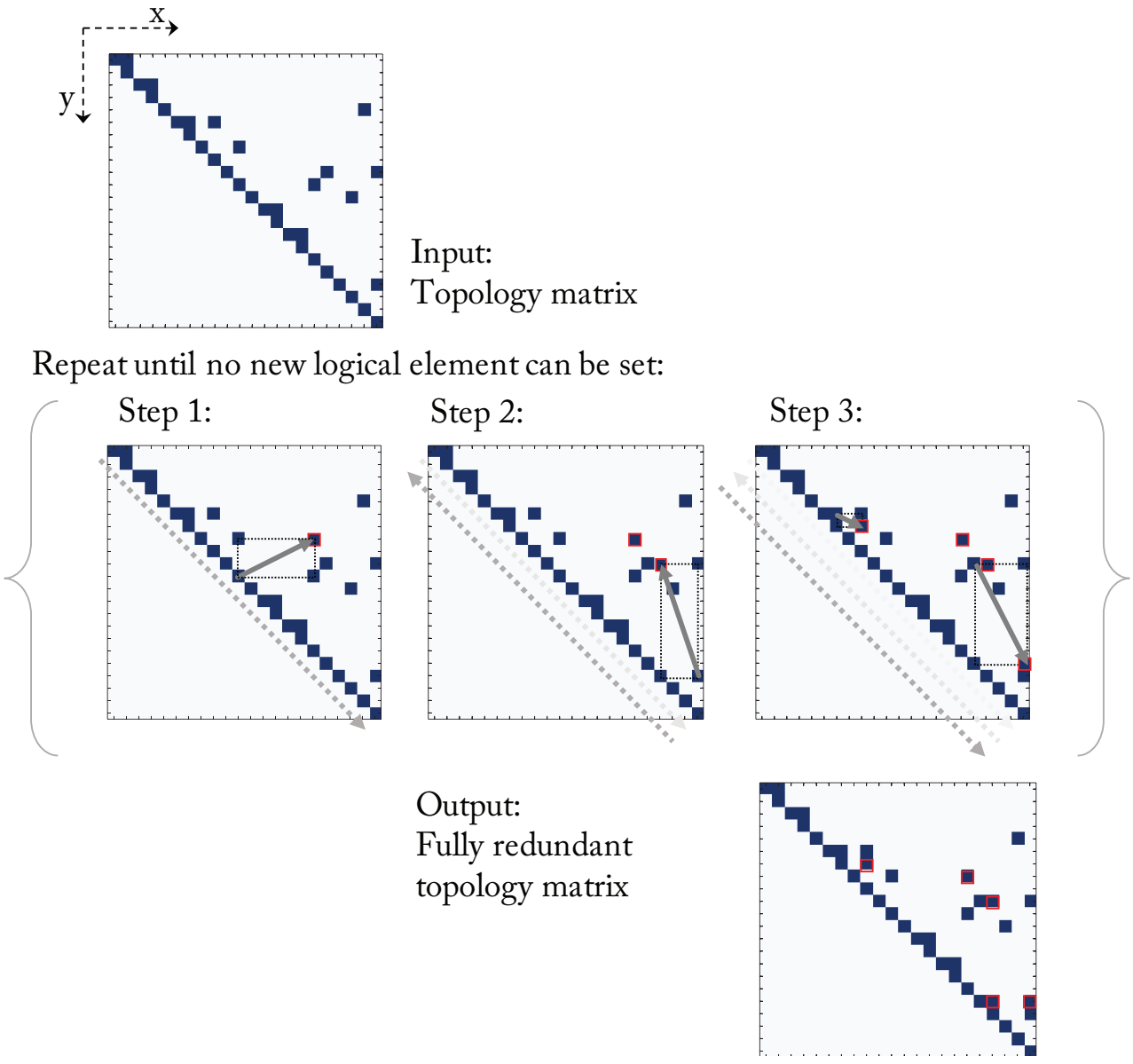

Figure 4: A procedure of finding all the redundant logical ones to build a full topology matrix.

cally and the other horizontally from a certain diagonal element.

(check right and diagonally, insert up) Scans the matrix along its diagonal from right to left and looks for a missing element in the direction *-y*. It finds all the rectangles with two existing vertices in the same column.

(check up and diagonally, insert right) Scans the matrix along its diagonal from left to right and looks for a missing element in the direction *x*. It finds all the rectangles with two existing vertices in the same row.

Until no new logical one was inserted

2.3 Parameter vector

Apart from the circuit topology, we also need to encode the numerical parameters such as resistances, capacitances, or transistor gate widths and lengths, in order to fully describe a circuit. We simply store those parameter values in a plain one-dimensional real vector, which leaves us with a complete genotype of a circuit, represented by a topology matrix and parameter vector.

2.4 Matrix-to-netlist conversion

Since we will analyze the circuit using numerical SPICE models, we need to translate the topology matrix together with the parameter vector into a SPICE netlist. The netlist has a simple syntax as shown on the right of Figure 5. Each line starts with the name of an element, the first character of which defines the element or sub-circuit type. The number that follows is simply the number of the element if there are more of the same type. Following the element name, there are the numbers of the nodes in the circuit to which the element is connected. At the end of each line there is usually a numerical parameter of the element or a model name.

Once we have calculated a fully-redundant topology matrix, there is not much work left to do to build a netlist. We demonstrate the whole procedure on the case shown in Figure 5. Let us first identify the node number of terminal V_{out}. The terminal is represented by the diagonal logical one in the bottom right corner of the matrix, pointed to by the darkest gray arrow. From this point, we search for the topmost logical one within the same column. The row index of this logical one represents the node number to be used in the netlist. We

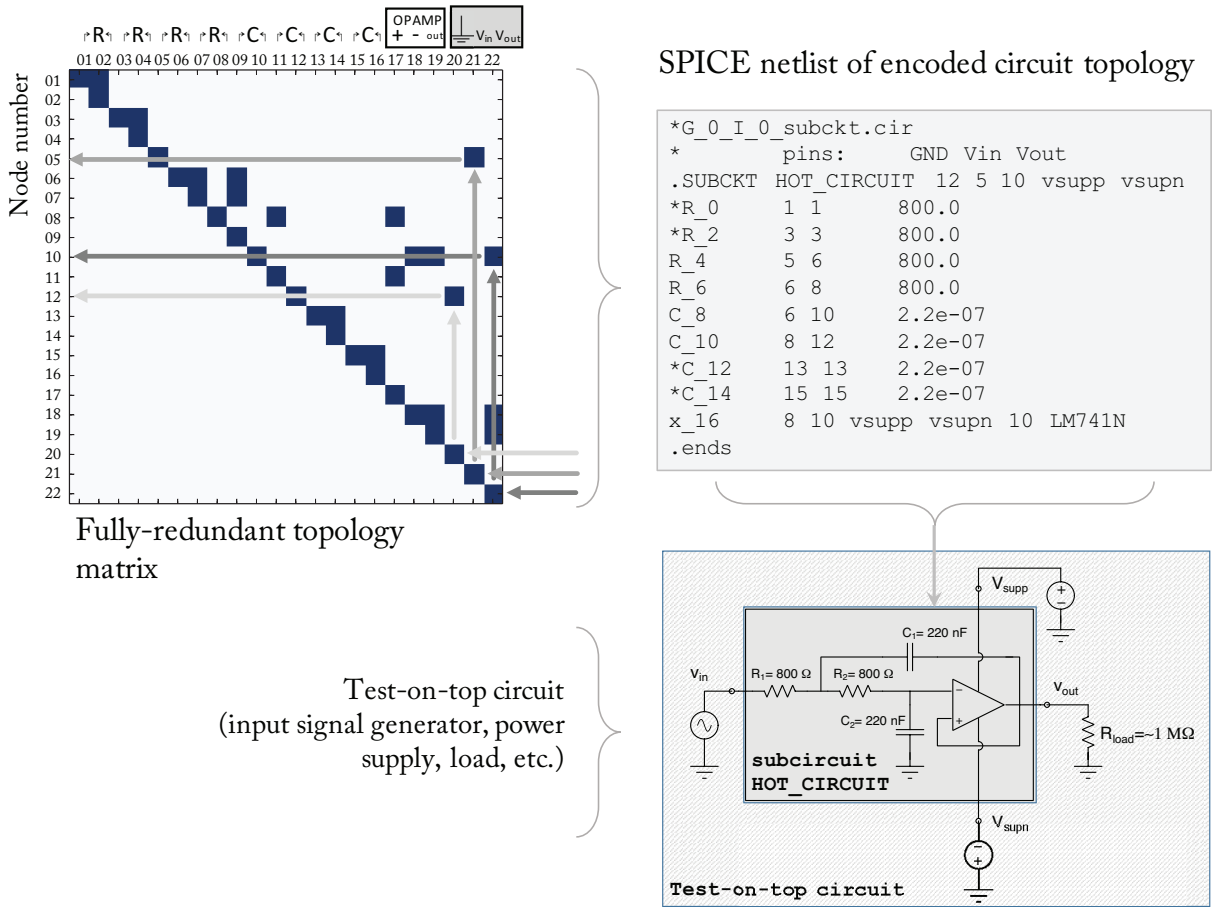

Figure 5: The conversion from a topology matrix to a netlist.

repeat the same procedure for each and every terminal contained in the matrix. In Figure 5, there are two additional arrows indicating the node number identification for terminals V_{in} and ground although all the terminals follow the same procedure.

It could happen that a diagonal logical one is the only non-zero logical element in the column. In that case, the node number assigned to the terminal is simply the row number of that diagonal logical one (i.e., the left terminals of R_0, R_2, C_{12} and C_{14}). The matrix, netlist, and topology in Figure 5 represent a Sallen-Key active LP filter. Notice that not all available elements are used in the resulting topology. We can see from both the matrix and the netlist that four of the nine available building blocks have their terminals connected together. This automatically means they are excluded from the topology. In the netlist, we commented out the excluded elements using an asterisk (*) to save Spice some unnecessary computation.

Notice that the resulting circuit is coded as a sub-circuit in the netlist. During the evaluation process, this sub-circuit is encapsulated in a special test circuit providing the necessary power supplies, input signals, loads, and measurement points as seen in the bottom right of Figure 5.

3 Search algorithm

Up to this point, we have explained how we encode an individual circuit (the genotype) and how we build a netlist suitable for its simulation (the phenotype). We are now ready for developing an evolutionary algorithm that will evolve a circuit based on a specific fitness specification. The algorithm is similar to the one that we used in [17].

Evolution is a process that allows a biological population to adapt to a given environment by means of change in the heritable characteristics of individuals [18]. The favorable changes mean more chance for an individual of surviving in a particular environment. That way, the population becomes better and better adapted to given conditions. This simple and robust procedure is often used as a means of global optimization [19], and we use it in our work as well. For the purposes of this research, we adapted the three basic evolutionary operators: selection (survival of the fittest), crossover (reproduction, also called recombination), and mutation.

3.1 Selection

The first step of an evolutionary algorithm is usually selection of the fittest individuals that will take part in crossover and/or mutation operations, thus producing offspring. One of the standard methods of selecting best individuals is so-called *tournament selection*. The idea is first to chose a few individuals from the populations at random to be part of a tournament. The winner of a tournament (the individual with the best fitness) is chosen to participate in crossover or mutation. We can easily adjust selection pressure by changing the tournament size. Weak individuals have a greater chance to be selected when the tournament size is smaller.

After we have obtained two winning individuals, we decide between crossover and mutation as shown in Figure 6. The decision is made randomly, based on a given probability. It is not unlikely that, during crossover, we exchange two identical parts of genetic material, which results in two offspring identical to their parents. It turned out that it is beneficial to the algorithm if we discard such offspring and repeat the genetic operation before even evaluating the circuits.

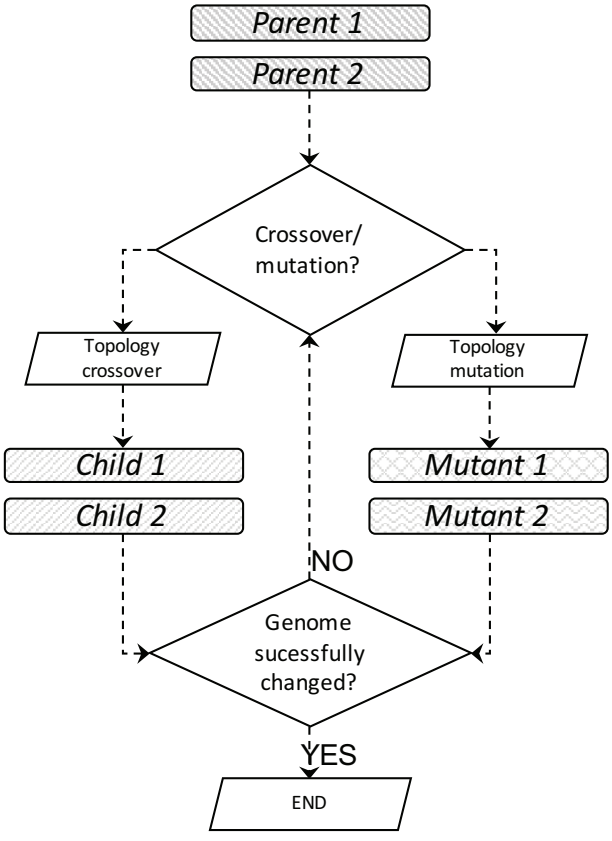

Figure 6: Deciding between crossover and mutation.

Note that tournament selection chooses the best individual from a randomly created subset of individuals. Because of the random selection it might happen that the fittest individuals are not selected at all and therefore could not proceed into the next generation. To prevent this kind of loss, we employ additional elit-

ist selection to ensure that a certain number of the fittest individuals proceed to the next generation even though they have not been selected during any of tournaments.

3.2 Crossover

The basic idea of our crossover technique is closely connected with the encoding type of an upper-triangular matrix. Recall that each logical one on a matrix diagonal corresponds either to a pin of an element or an outer connection (see Figure 2). Each logical one on the right of a particular diagonal element connects the pin to the corresponding pin on its right (see the row of the elements above the matrix in Figure 2). Similarly, each logical one above a particular diagonal element connects the pin to the corresponding pin on its left. As soon as we delete all logical ones from both, the row and column intersecting the diagonal element in question, we remove every information about how that particular pin is connected with the rest of the circuit. Our crossover operator exchanges information about the connections of any number of pins between one and four where the number of exchanged pins is randomly selected. Figure 7 shows examples where one (N = 1) and three (N = 3) pins are exchanged. The parent on the right is deliberately shown as a full upper-triangular matrix to better illustrate the effect of crossover.

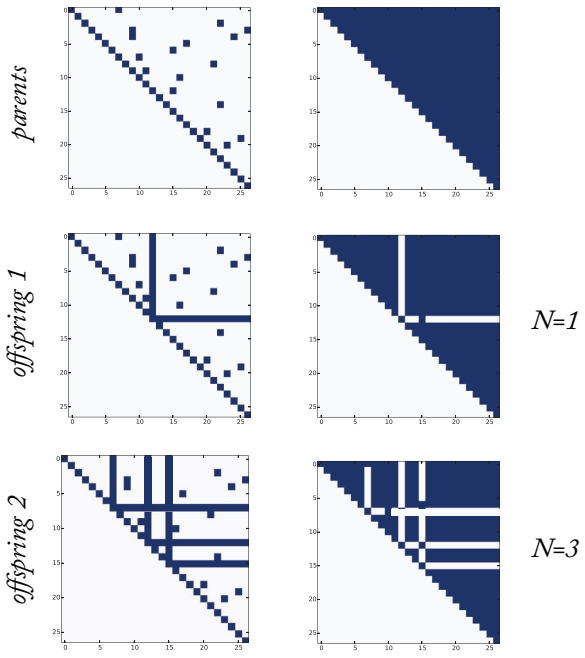

Figure 7: Topology matrix crossover examples exchanging information about one (N = 1) and three (N = 3) pin connections.

3.3 Mutation

Mutation is a random modification of genotype of a selected individual. Our implementation of a mutation operator randomly changes circuit connections in three different ways. It either removes, moves, or adds a logical one to a connection matrix. In case when a mutation operator is selected to be carried out upon the selected individual, one of these three mutation variants is performed based on an evenly distributed random choice.

3.4 Parameter vector optimization

Apart from the circuit topology, the circuit parameters have to be optimized during the evolution as well. We use the PSADE global optimization algorithm [2] to perform this task. PSADE is a hybrid method combining simulated annealing and differential evolution. The method was proven successful on a class of circuit optimization problems, so we use it to alter and additionally optimize the evolving circuit numerical parameters. Parameter optimization is however computationally expensive and optimizing each and every circuit in the generation would make the process unwieldy. It turned out that applying parameter optimization every 10th generation on three randomly chosen circuits (from the 10 best ones in the current population) is quite beneficial to the evolutionary process.

3.5 Circuit evaluation

One of the most important aspect of every evolutionary process (and indeed any optimization) is evaluation of the performance (a.k.a. fitness) of the members of the population. There are few general guidelines as how to do this and a designer mainly has to rely on his or her experience. The goal of our research was to synthetize a passive analog high-pass filter, with –3 dB starting pass band frequency of 8 kHz and the deepest possible damping in stop-band but not higher than –40 dB. We selected four main performance criteria: ripple, damping, f_{pass}, and gain as illustrated in Figure 8. Filter optimization penalty functions are usually designed with a fixed frequency domain structure [3] (i.e., the frequency ranges defining the ripple, dumping, and gain measurements are fixed during the optimization). When evaluating the frequency response, the real damping (or slope) is measured correctly only when f_{pass} is matched to wanted frequency (Figure 8 top). Some evaluated filters might have a proper shape overall, but at wrong frequency. This does not necessary mean that damping is wrong but rather that f_{pass} is off.

Frequency-fixed fitness detection works well for parameter optimization with a fixed topology. In our evolution procedure topology changes, but parameters are fixed until the PSADE triggers. With filters, mainly the topology (the order and type) defines the shape of frequency response, and parameters define bands [20]. This is why we allow f_{pass} to be off during the evolution, but measure other properties correctly (Figure 8 bottom). Doing so, we do not a-priori discriminate circuits, whose f_{pass} is off, but have other qualities.

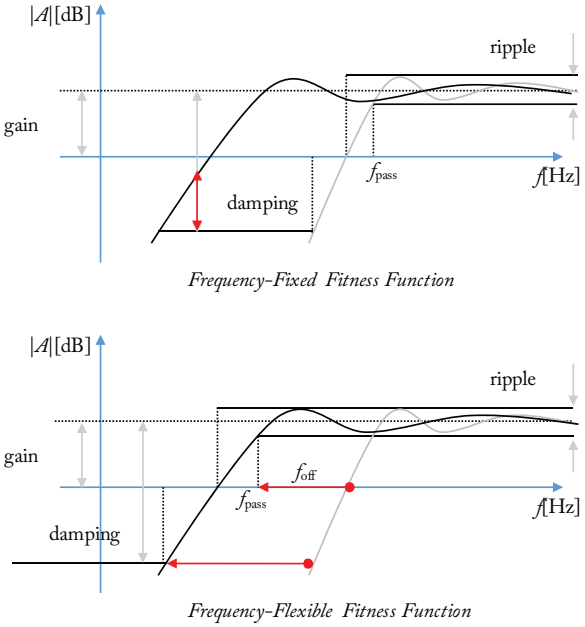

Figure 8: Frequency-Fixed versus Frequency-Flexible fitness function.

We calculate the overall fitness of the circuit using the following cost function:

$$r = \begin{cases} ripple - 0.5\,dB, ripple > 0.5\,dB \\ 0, ripple \le 0.5\,dB \end{cases} \quad (1)$$

$$d = \begin{cases} 40\,dB - damping\ , damping < 40\,dB \\ 0, damping \ge 40\,dB \end{cases} \quad (2)$$

$$f_{off} = \left| \log_{10} 8\,kHz - \log_{10} f_{pass} \right| \quad (3)$$

$$g = \left| 0\,dB - gain \right| \quad (4)$$

$$\text{cost} = w_1 r + w_2 d + w_3 f_{\text{off}} + w_4 g \quad (5)$$

where r is ripple larger than 0.5 dB in the pass band, damping is d, smaller than -40 dB in stop band, f_{off} is a difference between f_{pass} and 8 kHz and g is the gain objective. After a number of initial experiments we empirically set the weights to be $w_1 = 1$, $w_2 = 20$, $w_3 = 7$, and $w_4 = 10$. In addition, we weight every individual resulting in an unsuccessful measurement or simulation with factor of $10^3 * N_{nosucess}$, and we weight every individual with a forbidden short-circuit detected already in binary topology matrix with $2 * 10^4 * N_{SC}$, where N_{SC} is a number of detected short-circuits and $N_{nosucess}$ is a number of unsuccessful measurements and analyses.

All measurements were made using the PyOPUS Python library for circuit optimization, which enables simultaneous circuit evaluation on multiple processing cores [21]. Simulations were executed using HSpice.

3.6 The evolutionary algorithm

Figure 9 summarizes the complete evolutionary algorithm used in our research. As the first step, we create an initial random population of topology matrices and parameter vectors. This is done simply by creating topology matrices with evenly distributed logical ones through the whole matrix. Before entering the main optimization loop, we evaluate the initial population and sort the individuals according to their fitness. After performing the genetic operations of selection, crossover and mutation, we evaluate the newly generated individuals. If at least one of them fits the design criteria, we stop the procedure. Otherwise, if the generation number is divisible by ten, we randomly select three of the best ten individuals and run the PSADE optimization algorithm on their parameter vectors.

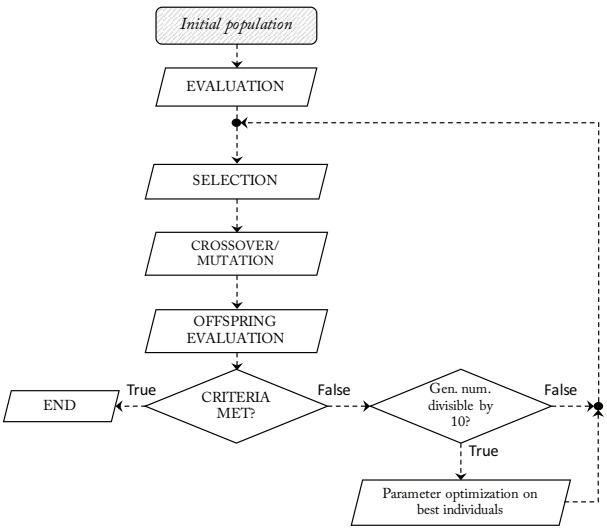

Figure 9: The evolutionary search procedure.

4 Results

In this section, we show the results of two separate runs of our evolutionary algorithm using identical algorithm parameters but with different fitness func-

tions. We included six resistors and six capacitors in the element library to be used by the algorithm. The initial parameters were randomly chosen for every circuit in the initial population ranging from 1 kΩ to 10 MΩ for the resistors and 1 pF to 10 μF for the capacitors. The same values were also used as the constraints for the PSADE parameter optimization. The population size in both runs was set to 400 individuals. The parameters are summarized in Table 1.

Table 1: Evolution parameters.

Population size	400
Tournament size	3
Elite size	8
Crossover probability	0.8
Mutation Probability	0.2

In the first run, we wanted to evolve a high-pass filter with at least –40 dB damping in the stop-band, at least one decade below f_{pass}. The evolution produced a solution after only 430 generations, which took about an hour using a cluster of 10 Core i5 Linux machines. We can observe the resulting circuit in Figure 10 (1) and its frequency response on Figure 11 (1). The resulting RC filter is comprised of three capacitors and four resistors. Its frequency response shows a low (almost zero) ripple in pass band, 0 dB gain and –40 dB/decade slope. There is a return point from –50 dB towards –40 dB at 0.9 kHz.

In the second case, we required steeper damping of –60 dB. In this case, the evolution reached the maximum limit of 2000 generations, which took approximately five hours on the same hardware. The resulting circuit (the circuit in Figure 10 (2) with the values in brackets) met most criteria except for f_{pass}, which settled at 1 kHz instead of 8 kHz. The reason for this failure, however, was not the evolutionary algorithm itself but rather the internal limit on the maximum number of iterations of the PSADE parameter optimization algorithm, which was set to 10^5. This internal limit was set in order to keep each parameter optimization run reasonably short during the topology evolution. After we have run the additional PSADE optimization on the final topology, the starting frequency of the pass-band moved to the desired value (cf. the plots of the second run in Figure 11). It took PSADE additional $5 \cdot 10^6$ iterations to fine-tune the circuit parameters. The final circuit is comprised of five capacitors and four resistors, which form an RC filter with a similar frequency response as in the first case, except with better damping (Figure 10 (2) and Figure 11 (2) – "fine-tuned"). Similarly to the first case, there is a return point from -61 dB towards -55 dB, which slightly violates the damping criterion. This problem could be solved simply by increasing the weight factor assigned to damping in the cost function.

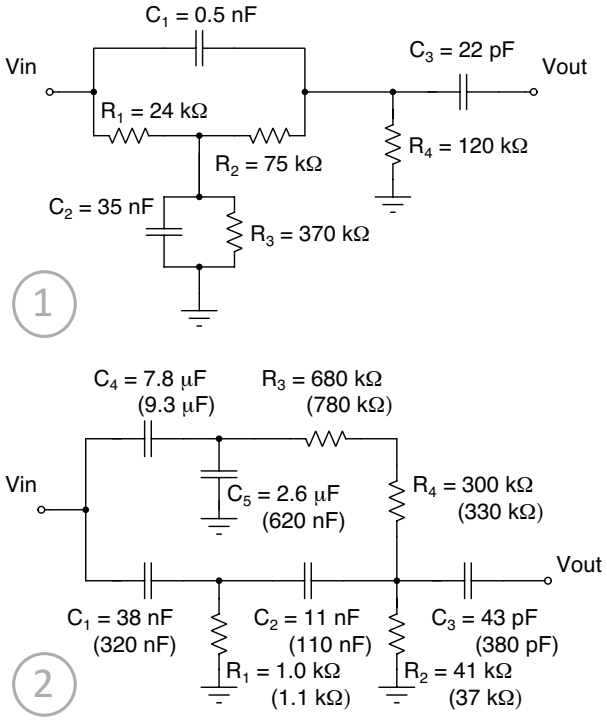

Figure 10: Automatically evolved filter topologies and their numerical parameters when requiring dumping of –40 dB (1) and –60 dB (2). With second circuit, parameters given in brackets are the raw algorithm solution and fine-tuned ones are given above.

Note that both topologies shown in Figure 10 are the raw output of the algorithm. An analog human designer will still see some obvious (topological) redundancies like, for example, the serially connected resistors R_3 and R_4 in the second filter.

4.1 A Comparison to other existing approaches

In this subsection, we compare our approach to other known analog circuit topology representations for evolutionary algorithms found in the literature. A brief glance at Table 2 reveals that our matrix representation technique surpasses the competitive approaches in several categories.

Representations used by Koza [12] and Lohn [13] suffer quite seriously from bloat that manifests itself in many redundant circuit branches, which makes it difficult to control the evolution. We have eliminated this problem because a connection matrix cannot change its size during the evolution. Furthermore, we limit a number and the types of allowed components by specifying a pre-defined component library to be used by the algo-

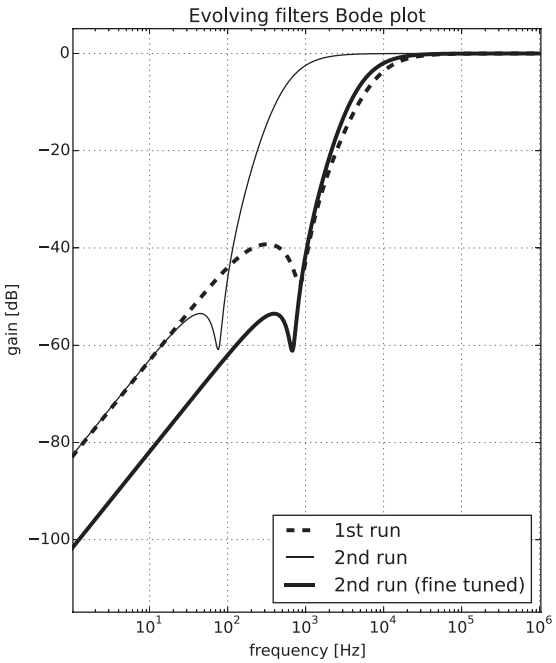

Figure 11: Frequency responses of automatically evolved both topology and parameters for two high-pass filters. For the second run, additional parameter fine-tuning was carried out.

rithm. The only redundancies that emerge in our case are some parallel/serial repetitions of same-type components.

With Koza [12], Lohn [13], and Gan [15], the basic building blocks are limited to two-pole components. Although the methods allow the usage of transistors, one of their three terminals should always be fixed beforehand to one of the outer connections. However, with our matrix representation it is possible to use building blocks having an arbitrary number of terminals, which vastly increases the circuit search space.

The approach proposed by Kruiskamp [10] is limited to combine 24 predefined topologies which is hardly practical for real-life problems. With our representation, there is no limit on the type and size of the evolved topology other than the one imposed by the size of a connection matrix and a pre-defined component library.

Koza [12], Lohn [13] and Györök [14] do not suggest any routine for short-circuit checks directly on the circuit representation level. Our approach incorporates efficient checking of a connection matrix. Configurations resulting in a short-circuited topology are excluded from further unnecessary and potentially expensive computations.

The approach by Kruiskamp [10] requires quite some information about the desired circuit topology structure to be input by the practitioner in advance. Many other methods, on the other hand, demand very little or even no such information. This way, the evolution is able to come up with a completely new topology for a certain task. Our method is flexible in this aspect because it allows a practitioner to enter an arbitrary amount of prior knowledge about the circuit by constructing an appropriate component library. By adding different sub-circuits to the library, or injecting known topologies into the initial generation of the evolutionary search, he or she can freely control the amount of entered knowledge.

Implementation of genetic programming can be quite an arduous task, involving genetic tree definition, tree-to-netlist conversion, and other complex mechanisms.

Table 2: A comparison to other existing circuit topology representation techniques.

	Bloat-safe?	Final topology size	Number of sub-circuit terminals	Search space size	Built-in topology check	Prior-knowledge required	Implementation complexity	Reproduction mechanisms complexity
Kruiskamp [10]	yes	limited	arbitrary	limited	yes	high	low	low
Koza [12]	no	unlimited	two	enormous	no	low	high	high
Lohn [13]	no	unlimited	two	enormous	no	low	high	low
Györök [14]	yes	limited	arbitrary	controllable	no	low	low	/
Gan [15]	yes	limited	two	controllable	yes	low	low	low
This work	yes	controllable	arbitrary	controllable	yes	controllable	low	low

It is also very important that our matrix representation can be implemented quite easily. Furthermore, unlike different genetic trees reproduction operators, our reproduction mechanisms are straightforward to implement and work natively with the upper-triangular connection matrix. Györök [14], as seen in Table 2, does not propose any reproduction mechanism other than a Monte Carlo method.

5 Conclusions

We developed an analog circuit representation technique for automated topology synthesis in the form of an upper-triangular binary matrix. The representation prevents bloat during the evolution so that the circuit cannot grow over the limits. Nevertheless, the implementation still enables a search over quite a large solution space whose size can be controlled by the element/sub-circuit library. We observed the redundancy phenomenon in the matrix-to-netlist conversion, which is important for maintaining the genetic diversity of a population of circuits but is problematic from the netlist generation point of view. We proposed a procedure of generating a fully-redundant matrix that lends itself easily to generation of a SPICE netlist. Based on the proposed topology representation, we developed the crossover and mutation genetic operators and an evolutionary algorithm suitable for evolving an arbitrary circuit based on a high-level statement about its required properties. We demonstrated the suitability of the approach with an evolution of a passive high-pass filter. We believe that the results of this research can easily be extended to synthetizing more complex passive and even active circuits, which will be a focus of our future research.

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Extraction of two wire Loop topology using Hybrid Single Ended Loop Testing

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Abstract: Performance of the Digital Subscriber Line (DSL) depends on the line topology and the noise power spectral density (PSD). Single ended loop testing (SELT) is the preferred and economical method for identifying the loop topology. In this paper SELT based on a combination of Correlation Time Domain Reflectometry (CTDR) and Frequency Domain Reflectometry (FDR) is proposed to identify the topology of a two wire line. In CTDR, complementary codes are used to probe the line and the reflections are correlated with the probe signal. For lines with multiple discontinuities, a Maximum Likelihood principle is developed along with data de-embedding technique. The prediction accuracy of the CTDR is limited but the main advantage is, it does not need any prior knowledge of the loop. To improve the accuracy of prediction, FDR with optimization algorithm is developed. This Hybrid method has the advantage of predicting the loop accurately without any prior knowledge of the loop. An improvement to the hybrid method to overcome the issues associated with the initial prediction for multiple discontinuity loops is implemented. The proposed CTDR and FDR use the existing modem for probing the line which avoids the need for additional hardware. As the SELT measurements are done online, the effect of cross talk and AWGN is considered. The developed algorithm is tested for standard ANSI loops and the results shows good prediction capability of this algorithm. However, when there are more number of discontinuities, the contribution of the far end reflection in the received echo signal is very feeble and this limits the prediction accuracy of far end discontinuity.

Keywords: SELT; Correlation Time Domain Reflectometry (CTDR); Frequency Domain Reflectometry (FDR); Hybrid method; Complementary Codes; Optimization.

Prepoznava topologije dvožičnih povezav v naročniški zanki s hibridno metodo testiranja na enem kraju

Izvleček: Učinkovitost digitalne naročniške linije (DSL) je odvisna od njene topologije in šuma moči sprektralne gostote. Za določevanje topologije zanke je priporočeno in ekonomično uporabiti testiranje na enem kraju (SELT). V članku je za določevanje topologije predlagan SELT na osnovi korelacijske reflektometrije v časovni domeni (CTDR in reklektometrije v frekvenčni domeni (FDR). Predlagana metodologija uporablja obstoječ modem in ne zahteva dodatne strojne opreme. SELT meritve so opravljene v živo, zato smo upoštevali tudi vplive presluhov in AWGN. Algoritem je testiran za standardne ANSI zanke in rezultati kažejo na njegovo dobro sposobnost napovedovanja.

Ključne besede: SELT; CTDR; FDR; hibridna metodologija; komplementarne kode; optimizacija

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1 Introduction

The service provider has to estimate the Quality of Service (QoS) afforded over a subscriber loop under realistic circumstances. Apart from the data rate, QoS also prescribes the delay in the transmission (in ms), the packet loss and Bit Error Rate (BER). QoS is a function of subscriber line conditions which includes the line topology and noise Power Spectral Density (PSD). A double ended loop measurement allow easy estimation of loop impulse response and the noise PSD, but needs a test device at the far end of the loop and is not economical prior to a service commencement. An economical SELT would require a reuse of the network operator's central office (CO) side DSL modem resources to perform measurements [1].

The physical loop consists of gauge changes, bridge taps and loop discontinuities that result in change of characteristic impedance. When a signal is injected through the line, reflections (echo) will be generated from all these discontinuities. These generated echoes are analysed to extract the location and the type of discontinuity. S. Galli et al [2-5] have used pulse TDR to characterize the loop. A pulse is considered as a probe signal and is transmitted through the loop and the reflections produced by each discontinuity are observed in time. The time domain reflection which contains the signature of the loop is then analyzed to predict the loop topology. Clustering of the TDR trace [3-4] and the use of statistical data [5] are included to reduce the time and to increase the accuracy respectively. These techniques provide a good estimation of the loop but are computationally intensive and cannot be easily implemented in current DSL modems. A more practical method described by Carine Neus et al [7] uses one port scattering parameter S11 in time domain to estimates the loop topology. The S11 measurement is however done off line with a vector network analyzer over the entire band width [6]. David E. Dodds [8, 9] has proposed FDR for identifying the loop impairments. The measurement phase uses a signal generator to probe the line up to 1.3MHz in steps of 500 Hz and the reflections are coherently detected. However if there are multiple discontinuities close to each other (<100m), detecting all discontinuities in a single step is not possible. If the discontinuities are far from each other the order of variation of the reflection makes it difficult to predict all the discontinuities in a single step.

SELT and Double Ended Loop Testing (DELT) are together employed in [10], to predict the loop topology. In [11] Genetic Algorithm (GA) based optimization method is used to estimate the line topology. In this paper [11], S11 is measured from CO end using SELT probing and the transfer function (H) measured from both the ends using DELT are considered as inputs. An initial solution (topology) is assumed and multi objective optimization algorithm is used to obtain the final optimum solution. For both these methods additional equipment are needed in the measuring phase and the measurement cannot be done on line.

SELT estimation is performed in two phases. In measurement phase the reflections are captured; termed as SELT – PMD function in G.SELT [12] and a second phase called as interpretation phase when analysis is done for topology estimation; termed as SELT-P function in G.SELT. The measurement phase of the proposed method reuses the blocks of the DSL modem and hence only a small code is needed that can be easily compiled into any modem. In this step the line is sounded sequentially once by employing CTDR and next by employing FDR. In the interpretation phase, the first step consists in analyzing CTDR results to obtain an approximate estimation of the distance and the type of the discontinuities [14, 15]. The topology learning from the CTDR application is used to generate an FDR data for the estimated loop. In the second step of the interpretation phase the generated FDR data is compared with a target (measured) FDR data in mean squared sense to arrive at an exact estimate of the loop topology. The analysis of measured data may be performed in the modem to a limited extent or offline where more computing resourcesare available.

Section 2 of this paper details the Correlation Time Domain Reflectometry (CTDR) for the initial loop topology estimation. In section 3, measurement and interpretation phase of Frequency Domain Reflectometry (FDR) is discussed. Section 4 gives the result of topology estimation of standard ANSI loops and the concluding remarks are drawn in section 5.

2 Correlation time domain reflectometry (CTDR)

Reflections from each discontinuity are characterized by the length and type of discontinuities present in the loop. The possible echo paths of a line with single bridge tap is shown in Figure1.

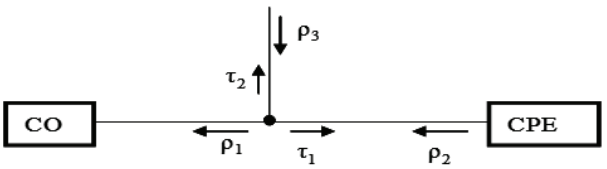


Figure 1: Representation of a loop with possible echo paths

Spread spectrum (SS) techniques using the existing modem can be used for identifying the characteristics of the loop without scarifying the response resolution. In the proposed CTDR method, data is loaded in all the subcarriers at a time and the reflections are used for the estimation of the loop topology. The Digital Subscriber Line (DSL) modem can work in full duplex mode. It can simultaneously transmit and receive data with an additional firmware. This firmware helps in the modification of the filter coefficients present in the front end of the modem. CTDR method does not need any prior knowledge of the loop but the accuracy of prediction is limited due to the variation in propagation velocity with frequency and the gauge of the copper medium. A mathematical model for the time domain echo is developed based on the two port network theory.

2.1 Mathematical model for Time domain Echo Signal

The proposed TDR method uses existing Discrete Multi Tone (DMT) modem with its bit loading algorithms. The received echo signal *r(t)* for a probe signal *p(t)* is given by

$$r(t) = \sum_{i=1}^{M} e_r^{(i)}(t - T_i) + N_0(t) \quad (1)$$

Where,
M - number of discontinuities in the line,
$N_0(t)$ - noise present in the channel
T_i - time of arrival of the ith echo
$e_r^{(i)}(t)$ - echo generated by the ith discontinuity given by

$$e_r^{(i)}(t) = p(t) * h_{ep}^{(i)}(t) \quad (2)$$

Where,
p(t) - probe signal
$h_{ep}^{(i)}(t)$ - impulse response of the ith echo path.

Complementary codes which have good autocorrelation property are used as probe signals *p(t)* [14] and the received echo signal *r(t)* is correlated with the probe signal.

$$W(t) = r(t) \otimes p(t) \quad (3)$$

$\otimes$ – represents correlation operation. The signal *w(t)* contains the signature of the loop and can be used to estimate the loop topology.

2.2 Analysis of CTDR signal

Correlated signal will have its peak when transmitted signal has completed its round trip of any discontinuity. The time difference between the peaks and the propagation speed of the (v) medium are used to estimate the distance of the discontinuity. Complementary codes are used as probe signal [14, 15]. With complementary codes, the correlated signal is 2*N* times stronger and the noise is build up by a factor $\sqrt{2N}$. Thus SNR improvement with complementary code CTDR to direct impulse probe scheme is $\sqrt{2N}$. To further reduce the effect of AWGN noise, averaging over number of symbols is performed. Noise reduction by averaging technique and the use of complementary codes improves the overall SNR significantly.

The attenuation and reflections in the loop reduces the strength of the reflected signal from each discontinuity and the peaks from distant discontinuities are not clear in the correlated signal. To overcome this limitation, Maximum Likelihood (ML) principle [14] with data de-embedding is incorporated. ML principle is employed to identify the nature and type of discontinuity one after the other. Data de-embedding process masks the reflections of the identified discontinuity in the overall echo signal to unravel the signatures of the unknown discontinuities. Thus by incorporating the de-embedding process, overall predictability of the CDTR method is enhanced. This improved CTDR method illustrated in Figure 2 has the following steps:

1. Estimate the ith discontinuity location from the peak position of *W(t)* (equation 3).
2. Hypothesize discontinuity by considering all the possible topologies. $\left\{T_j^{(i)}\right\}$ is the set of all possible topologies at step *i* and *j = 1,2…N, N* is the number of possible topologies based on the magnitude of the reflection coefficient. Each possible topology consists of the previously identified line segments and the hypothesized discontinuity followed by an infinite loop section. The unknown segment of the loop after the hypothesized discontinuity is represented by an infinite loop section so as to eliminate any reflection from the unknown section.
3. Simulate echo for all the possible topologies. $\left\{h_j^{(i)}(t)\right\}$ is the simulated echo signal for each of the topologies in $\left\{T_j^{(i)}\right\}$, at step *i*.
4. Generate the error vector $e_j^{(i)}$ in the localized time interval t_1 to t_2, corresponding to the hypothesized topologies $\left\{T_j^{(i)}\right\}$ at step *i*.

$$e_j^{(i)} = \sum_{t1}^{t2} r(t) - h_j^{(i)}(t) \quad (4)$$

5. Choose the maximum likelihood topology by comparing the calculated error (*e*). The corresponding simulated signal is considered as $h^{(i)}(t)$ and the topology is $T^{(i)}$.
6. If the selected topology is bridge tap, set BT=1and continue.
7. The de-embedded signal after the removal of ith discontinuity is $d^{(i+1)}(t) = r(t) - h^{(i)}(t)$.
8. Generate the corresponding correlated signal $w^{(i+1)}(t)$
9. If there is no peak in $w^{(i+1)}(t)$ then the hypothesized topology $T^{(i)}$ is the estimated topology. Else continue.
10. i=i+1.
11. Estimate ith discontinuity location from the peak position of $w^{(i)}(t)$.
12. If BT=1 generate $T^{(i)}$ by including a bridge tap with $T^{(i-1)}$ and continue. Else go to step 2.
13. Generate corresponding $h^{(i)}$.
14. De-embedding: $d^{(i+1)}(t) = r(t) - h^{(i)}(t)$
15. Set BT=0;
16. Go to step 8.

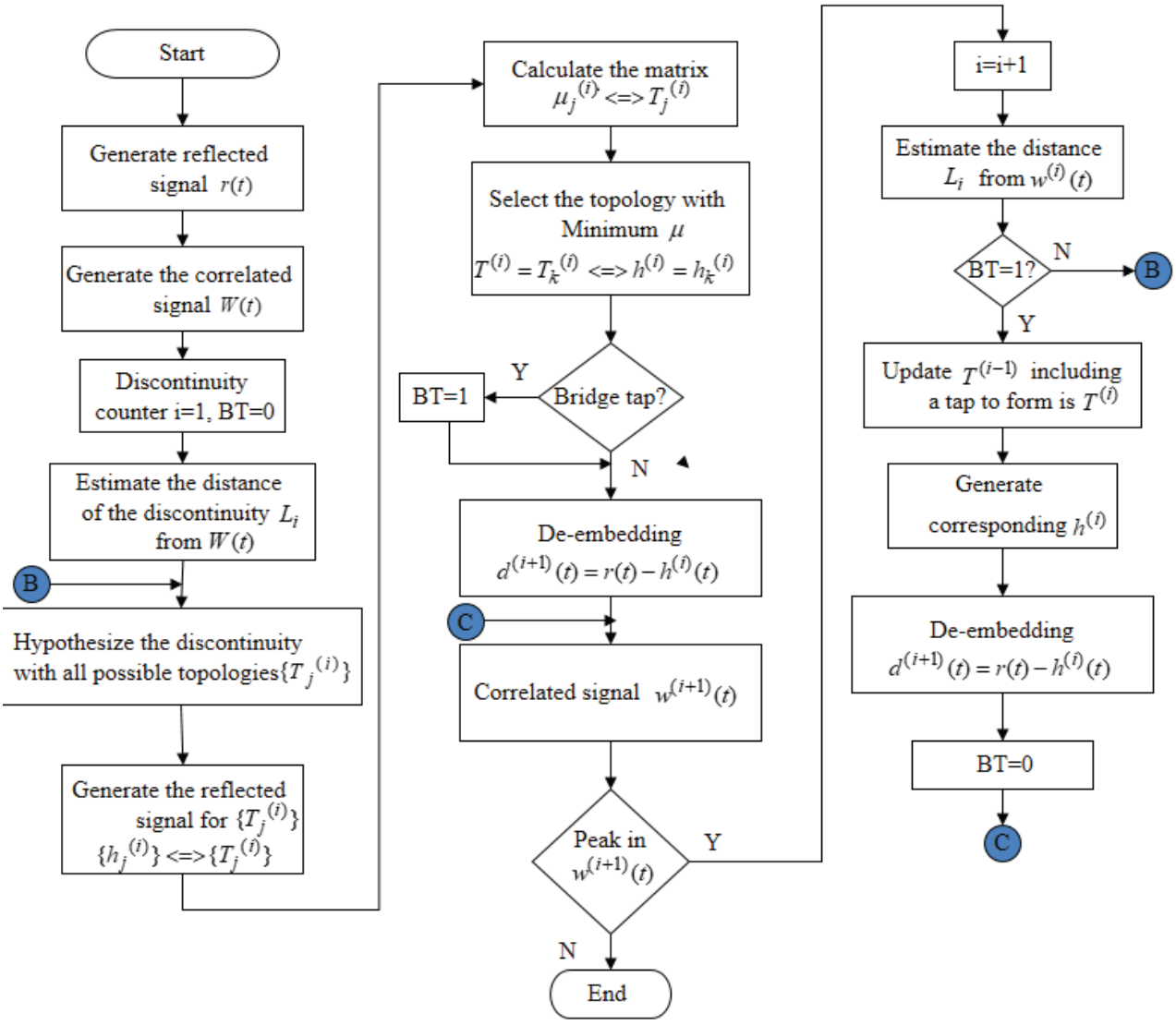


Figure 2: Step by step Maximum Likelihood approach with De-embedding

3 Frequency domain reflectometry (FDR)

A FDR measurement method is based on single tone excitation. Each tone in a DMT symbol is sounded individually and its echoes are captured using the DSL Modem. As explained above, additional firmware at the modem helps to extract the reflections. The total received echo signal is the sum of echo signals of individual tones and is used in the analysis phase to predict the loop topology. The mathematical model for the echo signals in frequency domain is developed and is used in the optimization algorithm.

3.1 Mathematical model for FDR

The received echo signal for the nth tone along with the effect of noise is given by,

$$R(f_{n)} = \sum_{i=1}^{M} \left(R^{(i)}(f_n) + N_o(f_n) \right) \quad (5)$$

Where,
M- number of echo paths in the loop
$N_0(f_n)$ - noise in the echo signal.
$R^{(i)}(f_n)$ - received signal from the ith echo path when nth tone is sounded given by,

$$R^{(i)}(f_n) = S(f_n) Hecho^{(i)}(f) \quad (6)$$

Where,
$S(f_n)$ - spectrum of the transmitted data (Energy only in the nth bin)
$Hecho^{(i)}(f)$ - transfer function of the ith echo path given by,

$$Hecho^{(i)}(f) = F(\tau^{(1)}, \tau^{(2)}, \ldots \tau^{(i-1)}) H^{(i)}(f) \rho^{(i)}(f) \quad (7)$$

Here $F(\tau^{(1)}, \tau^{(2)}, \cdots \tau^{(i-1)})$ is a frequency dependent function that includes the transmission coefficients of all the discontinuities preceding the ith discontinuity and $\rho^{(i)}(f)$ is the reflection coefficient of the ith discontinuity. $H^{(i)}(f)$ is the line transfer function [13,14].

$$H^{(i)}(f) = e^{-\gamma Li} \quad (8)$$

Where,
Li - length of the ith echo path.
γ - Propagation constant which is a function of frequency, given by

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)}$$

The total received echo signal is sum of echo signals for all the transmitted tones.

$$R(f) = \sum_{n} R(f_n) \quad (9)$$

*R(f)*is the received echo signal from all discontinuities as seen at the receiver FFT output and contains information about these discontinuities. The frequency range of the input signal determines the predictable range and resolution of the FDR method. The minimum measurable distance (resolution) increases with range of frequency as higher range will have complete periodic information even for a shorter length. Amplitude of the echo signal depends on the attenuation in the line and attenuation is doubled due to the round trip travel along the loop. The lower tones (low frequency tones) suffer less attenuation compared to the higher tones and are essential for longer loops. Thus there is a need to balance the contrasting requirement between reach and resolution.

The initial topology estimated by CTDR method is used as a guess topology and optimization is carried out based on the guess topology.

3.2 Optimization method

The steps involved in this algorithm are
Simulate FDR echo signal for the initial topology (Φ) estimated using Correlation Time Domain Reflectometry $\hat{R}(\Phi, f_n)$, using equation (5).

Obtain the FDR echo signal $R(f_n)$ from measurements.
Calculate the cost function (MSE)

$$MSE = \left(\sum_{n=1}^{N} \left| \hat{R}(\Phi, f_n) - R(f_n) \right|^2 \right) \quad (10)$$

Obtain the accurate line topology by minimizing the cost function using Nelder-Mead simplex optimization algorithm.

Nelder-Mead optimization algorithm [16] iteratively improves Φ in terms of line segment lengths until the best solution (close match) is found.

4 Simulation results

The developed Hybrid method is used for the prediction of the ANSI standard telephone lines [13] shown in Figure 3. The parameters used for the simulation of CTDR and FDR are tabulated in Table.1.

Test loops 1 to 5 are plain lines with different lengths and gauge. End of line is the only discontinuity and it is considered as an open termination with reflection coefficient is 1 and the correlated signal will have a positive peak. FDR signal for a plain line will be a decaying sinusoidal wave satisfying the equation [18,19]

$$R(f) = a_1 \exp(-a_2 f) \cos(a_3 f + a_4) \quad (11)$$

Where, a1, a2, a3and a4 depend on the gauge, length and the termination.

Table 1: Parameters used for Simulation

Parameters	Values in CTDR	Values in FDR
Total transmitted power	21dBm as specified in DSL standard [13]	-36.5dBm/Hz as per PSD mask specified in DSL standard[13]
No of bits per tone	2 bits, 4QAM	2 bits, 4QAM
Tone considered	6 - 511	6 – 110 (One tone at a time)
Crosstalk noise [13]	24 ADSL NEXT and FEXT	24 ADSL NEXT and FEXT
AWGN PSD	-130 dBm/Hz	-130 dBm/Hz
Velocity of Propagation (VoP)	0.63 C (C- speed of light)	--
Number of frames	10000	--

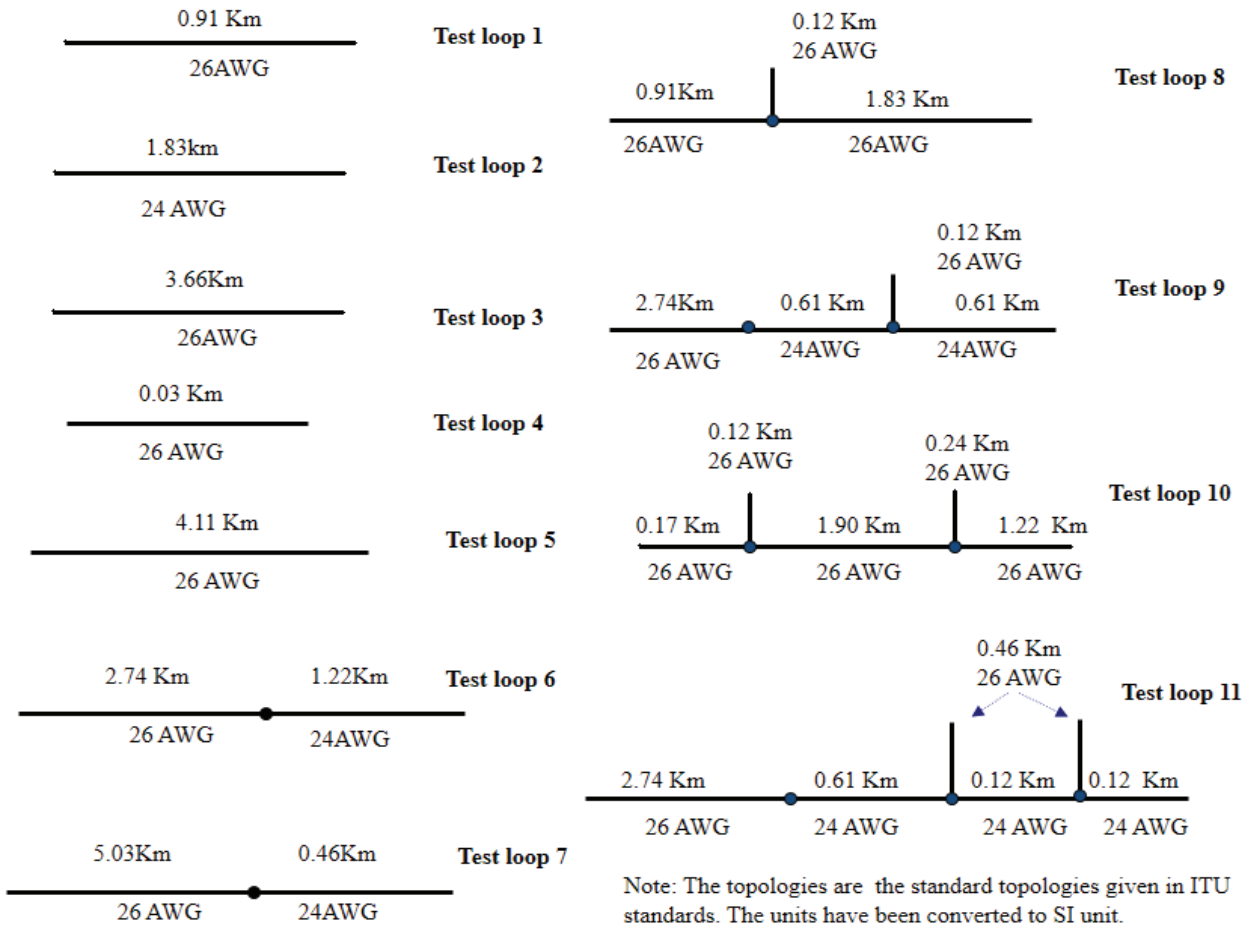


Figure 3: TEST loops

The waveforms and the analysis of plain line are explained with test loop 2 which is a medium reach (1.83 Km, 24 AWG) with open end. For this loop, the variation of correlation amplitude with reach is shown in Figure 4. The peak value of the signal is positive (0.002398) at a distance 1.80 Km.

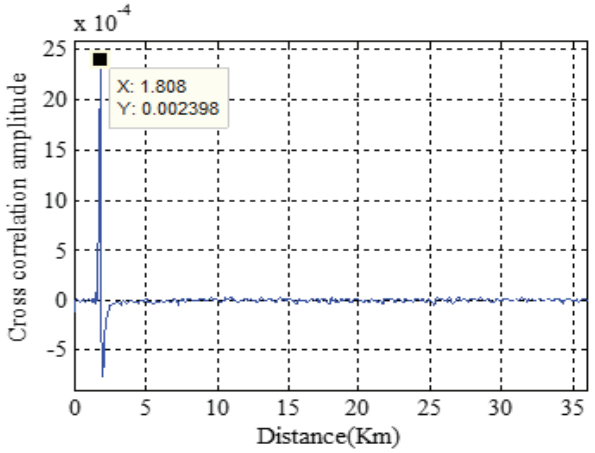


Figure 4: Correlation amplitude Vs distance for test loop2

The possible topologies with the above prediction (1.80 Km, open end) and calculated error (e) are tabulated in Table 2, from which the line is understood as 1.80 Km of 24 AWG.

Table 2: Possible topologies for Test loop 2

Sl. No	Hypothesized discontinuity	possible topology	MSE
1	End of loop (open)	1.80 Km line, 26 AWG	2.40e-3
2	End of loop (open)	1.80 Km line, 24 AWG	**8.35e-5**

The frequency domain received echo signal for this loop (Test loop 2) is shown in Figure 5. The FDR is a decaying sinusoidal waveform.

With the initial guess of 1.80 Km, 24AWG (Predicted using CTDR), the optimization algorithm is used and Figure 6 shows the variation of mean square error with the line length for both gauges and the line is predicted as 1.83 Km, 24 AWG line.

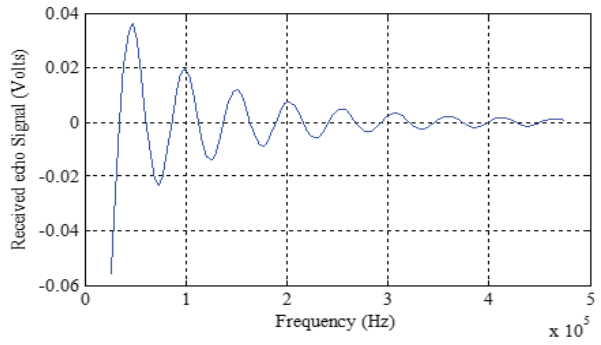


Figure 5: Frequency Domain Reflectometry signal for test loop2

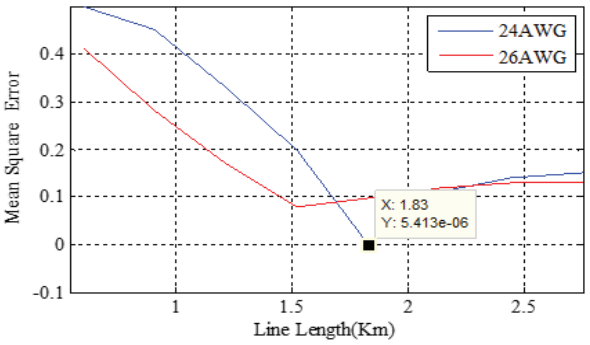


Figure 6: Error curve for test loop2

Test Loops 7 to 11 are loops with one or more discontinuities. For lines with multiple discontinuities, depends on the type of discontinuity and its length, the dominant portion of the received signal varies. Following are the observations made with different discontinuities.

The influence of the gauge change in the final signal is much lesser due to its low reflection coefficient of ~ -0.03.

The reflection coefficient at the bridge tap is ~ -0.3. Hence the influence of the received signal from the bridge tap is predominant.

When the numbers of discontinuities are higher than two, the reflection from the later segments of the loop is not felt in the overall received signal and these segments are not predicted with good accuracy.

In summary, the magnitudes of transmission and reflection coefficients of different discontinuities are tabulated in Table 3 [2].

The analysis of lines with multiple discontinuities is explained with test loop 11. Figure 7 shows the correlated signal amplitude with distance for test loop 11. Negative peak with amplitude 3.19e-6 at 2.88 Km indicates negative reflection coefficient and gauge change or bridge taps are the possible topologies.

Table 3: Magnitude of Transmission and Reflection coefficients of different discontinuities

Sl. No.	Type of Discontinuity	Reflection Coefficient	Transmission Coefficient
1.	Gauge Change	0.03	0.97
2.	Bridge Tap	0.33	0.33*
3.	End of Loop (Open)	1	0

* one wave will travel along the BT and other wave will travel along the next loop section

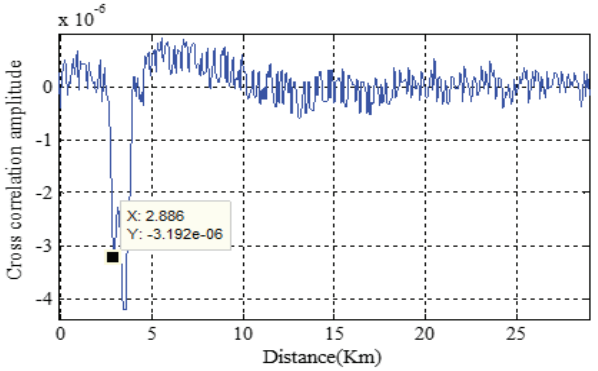


Figure 7: Correlation amplitude Vs distance for test loop 11

All the possible topologies with this observation and the mean square error (e) between the simulated echoes for these possible topologies with the received echo are listed in Table 4. From this table, topology with gauge change (S No1) is identified as the correct topology till first discontinuity ($T^{(1)}$).

The echo due to the identified first segment is removed from the received echo. Figure 8(a) shows the de-embedded signal $w^{(2)}(t)$ after removing the reflection from identified topology ($T^{(1)}$). Negative reflection at 3.49 Km is inferred as bridge tap and the length of the second line segment is 0.7Km (3.58Km- 2.88 Km). Construction of all possible topologies (including the identified topology segments) is listed in Table 5. The MSE helps in identifying the gauge of the line segments. With identifying the tap as 26 AWG, $w^{(3)}(t)$ is generated and the length of the bridge tap is estimated as 0.18Km (3.76Km – 3.58 Km). De-embedding the echo based on the identified loop segments results in $w^{(4)}(t)$ from which the third segment of loop is estimated as 0.61Km (4.19 Km-3.58 Km) with open end. In $w^{(5)}(t)$ there are no peaks visible and CTDR estimated topology is shown in Figure 8(d). The de-embedding process is shown in Figure 8(a-c).

Table 4: Possible topologies for first discontinuity (Test loop 11)

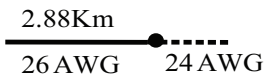
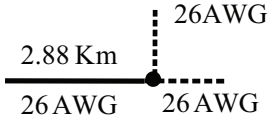
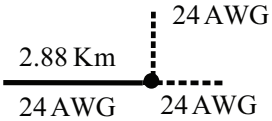
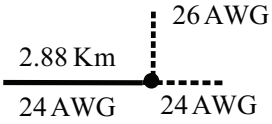
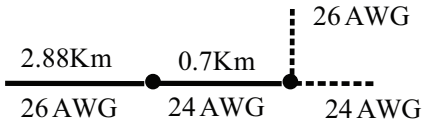
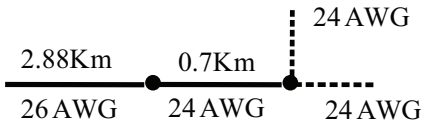
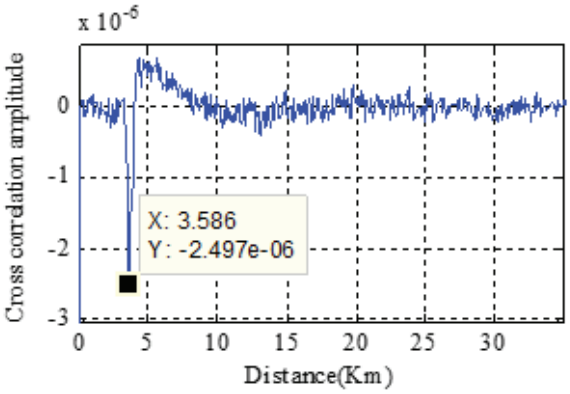
Sl. No	Hypothesized discontinuity	Possible topology (dotted line indicates infinite length)	MSE
1	Gauge change		1.05e-6
2	Bridge tap (Taps with Open end)		1.11e-5
3	Bridge tap (Taps with Open end)		1.25e-5
4	Bridge tap (Taps with Open end)		1.11e-4
5	Bridge tap (Taps with Open end)		1.03e-4

Table 5: Possible topologies at second discontinuity for test loop 11

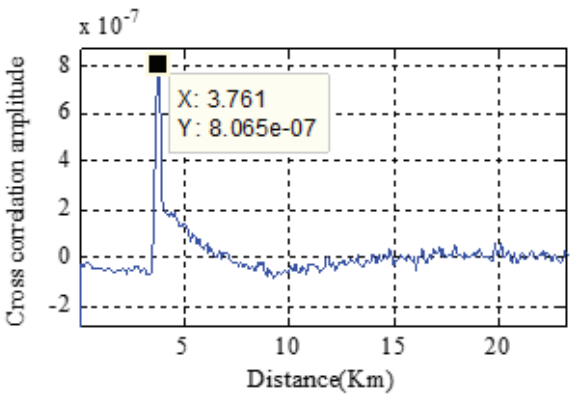
Sl. No	Hypothesized discontinuity	possible topology (dotted line indicates infinite length)	MSE
1	Gauge change followed by bridge tap(Taps with Open end)		4.04e-6
2	Gauge change followed by bridge tap (Taps with Open end)		4.40e-6

The CTDR estimation for test loop11 is not complete. This is due to the very less contribution of the far end reflection in the overall received signal. With this as the initial guess, FDR prediction converged to MSE error of 0.0028. For lines with more discontinuities, the CTDR prediction of the number of discontinuities may not be complete. As the FDR step in the hybrid method focuses only on the accuracy of the segment lengths, there is no possibility of correct prediction if the initial guess is incomplete in the number of discontinuities. This limitation is found to be serious for complex topologies. The hybrid method is improved to address this issue by adding a discontinuity in the initial guess from CTDR step when the MSE error after global search is higher than the set threshold value. This additional modification is shown in Figure 9. As the CTDR is capable of predicting first two discontinuities and from practical understanding the maximum number of discontinuities is not more than 4, this outer loop is set with a maximum limit of two.

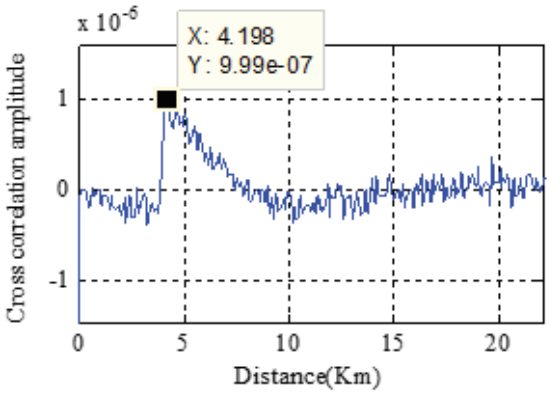
This issue of non convergence for test loop 11 with FDR is due to wrong specification of number of discontinuities as the initial guess. The improved hybrid method is employed. The converged line topology with improved hybrid method is shown in Figure 10.



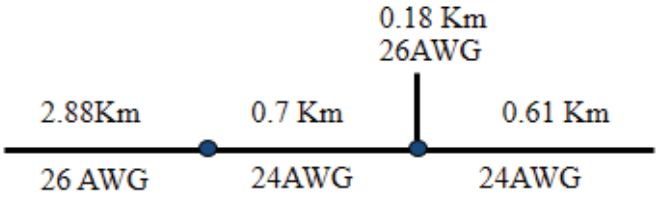
$(a): w^{(2)}(t)$



$(b): w^{(3)}(t)$



$(c): w^{(4)}(t)$



$(d): \Pr edicted \quad Topo\log y$

Figure 8: De-embedded signal for test loop 11

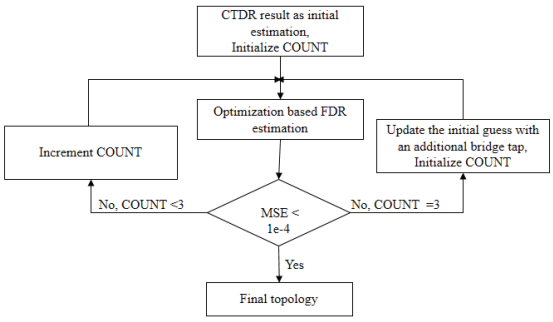


Figure 9: Improved Hybrid method

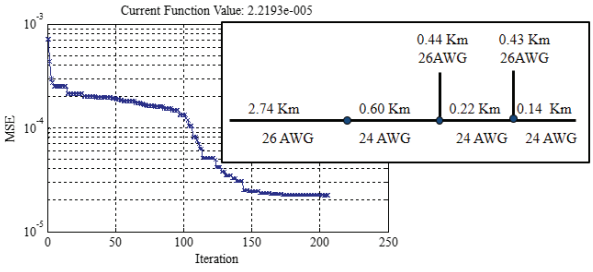


Figure 10: The convergence for test loop 11

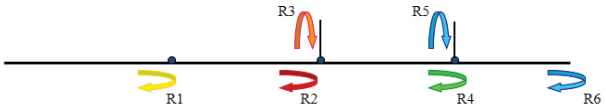


Figure 11: Reflection analysis of test loop 11

The summary of results for all the test loops is presented in Table 6.

The variance in Table 6 is very small which indicates that the same optimum topology was obtained with repeated trails. The estimation error is less in the case of plain loops and loops with one or more discontinuities. For test loop 11, the first two line segments and the first bridge tap length are predicted with good accuracy but the segment 3, 4 and tap2 length are not accurate. Figure 11 shows the schematic representation of the reflection from each discontinuity. Strength of the reflection from each junction is calculated based on the reflection and transmission coefficients for comparison. Table 7 compares the % contribution of each reflection in the received echo signal as per the transmission and reflection coefficients listed in Table 3. Signal attenuation and gauge are not considered in this calculation as the focus is to quantify the effect of

Table 6: Summary of results using Hybrid method for Telephone Lines

Test Loop	Actual Loop Topology (Km)	Initial Estimate using CTDR (Km)	% error	Estimated Topology Using CTDR and FDR (Km)	% error	% Variance in the estimation
Test Loop1	0.91, 26 AWG	0.94, 26 AWG	3.33	0.91, 26 AWG	--	0
Test Loop2	1.83, 24 AWG	1.80, 24 AWG	1.16	1.83, 24 AWG	--	0
Test Loop3	3.66, 26 AWG	3.87, 26 AWG	5.73	3.66, 26 AWG	--	0
Test Loop4	0.03, 26 AWG	--	--	0.03, 26 AWG	--	0
Test Loop5	4.11, 26 AWG	--	--	4.11, 26 AWG	--	0
Test Loop6	Segment1 – 2.74, 26 AWG	2.75, 26 AWG	4.06	2.74, 26 AWG	0.25	0.04
	Segment 2 -1.22, 24 AWG	1.38, 24 AWG		1.21, 24 AWG		
Test Loop7	Segment1- 5.03, 26 AWG	--	--	5.01, 26 AWG	0.55	0.3
	Segment 2- 0.46, 24 AWG	--		0.45, 24 AWG		
Test Loop8	Segment 1 -0.91, 26 AWG	0.94, 26 AWG	4.1	0.91, 26 AWG	--	0.1
	Bridge tap-0.15, 26 AWG*	0.17, 26 AWG*		0.15, 26 AWG*		
	Segment 2- 1.83, 26 AWG	1.90, 26 AWG		1.83, 26 AWG		
Test Loop9	Segment 1- 2.74, 26 AWG	2.84, 26 AWG	6.3	2.74, 26 AWG	0.24	0.1
	Segment2 -0.61, 24 AWG	0.57, 24 AWG		0.61, 24 AWG		
	Bridge tap-0.15, 26 AWG*	0.18, 26 AWG*		0.15, 26 AWG*		
	Segment 3-0.61, 24 AWG	0.70, 24 AWG		0.60, 24 AWG		
Test Loop10	Segment 1 - 0.17, 26 AWG	0.18, 26 AWG	7.3	0.17, 26 AWG	0.27	0.2
	Bridge tap 1 - 0.12, 26 AWG*	0.08, 26 AWG*		0.12, 26 AWG*		
	Segment 2- 1.90, 26 AWG	2.01, 26 AWG		1.90, 26 AWG		
	Bridge tap 2 - 0.24, 26 AWG*	0.26, 26 AWG*		0.24, 26 AWG*		
	Segment 3 -1.22, 26 AWG	1.31, 26 AWG		1.21, 26 AWG		
Test Loop11	Segment 1 – 2.74, 26 AWG	2.88, 26 AWG	--	2.74, 26 AWG	3.06	1.2
	Segment 2 – 0.61, 24 AWG	0.7, 24 AWG		0.60, 24 AWG		
	Bridge tap 1 – 0.46, 26 AWG*	0.18, 26 AWG*		0.44, 26 AWG*		
	Segment 3- 0.15, 24 AWG	0.61, 24 AWG		0.22, 24 AWG		
	Bridge tap 2 – 0.46, 26 AWG*	--		0.43, 26 AWG*		
	Segment 3 -0.15, 24 AWG	--		0.14, 24 AWG		

*Indicates Bridge Tap

individual reflections on the final echo. Around 89% of the received echo is contributed by the reflections R1, R2 and R3. Even though R4 reflection is considered as 6 %, due to the higher distance of travel, attenuation will be higher and hence net overall contribution in the received signal will be much lesser than 6%. R5 and R6 have 2% weightage in the received signal even without considering the attenuation effect. This results in very feeble contribution in the measured echo. Hence accuracy of these line segments, in the predicted topology does not influence MSE to a significant level. This explains the reason for higher prediction error in the segments 3, 4 and Tap 2.

Analyses are conducted to study the improvement in prediction ability with increase in the strength of the probe signal PSD (by 3 and 6 dBm/Hz). As shown in Table 8, prediction ability improved with these cases. However, it must be noted that as per ITU standards [13], signal strength increase beyond 3 dBm/Hz is not recommended as it induces crosstalk noise in other lines. So the allowed strength of the probe signal is -33.3 dBm/Hz.

5 Conclusion

The combined CTDR and FDR method is developed for the extraction of loop topology of two wire telephone lines. CTDR can be employed where there is no initial knowledge of the loop. But the accuracy of CTDR estimation is limited. On the other hand, FDR method can predict the topology with higher accuracy but requires a reasonable initial knowledge of the topology. The pro-

Table 7: Reflection strength contribution (test loop11)

Reflection	Weightage of transmission and Reflection coefficients in the received signal (Excluding the attenuation effect)		
	Sequence of approximate reflection and transmission coefficients	Total	% contribution in the received signal (Ri/∑Ri)
R1	0.03	0.03	6.0
R2	0.97*0.33*0.97	0.3104	62.2
R3	0.97*0.33*1*0.33*0.97	0.1024	20.52
R4	0.97 *0.33*0.33*0.33*0.97	0.0338	6.7
R5	0.97*0.33*0.33*1*0.33*0.33*0.97	0.0112	2.2
R6	0.97*0.33*0.33*1*0.33*0.33*0.97	0.0112	2.2
∑Ri		0.499	

Table 8: Test loop 11 prediction summary with increased power

	Actual length (Km)	Predicted length with -36.5 dBm/Hz(Km)	Predicted length with -33.3 dBm/Hz(Km)	Predicted length with -30.3 dBm/Hz(Km)
Segment 1 (R1)	2.74	2.74	2.74	2.74
Segment 2 (R2)	0.61	0.59	0.60	0.61
Tap 1@ junction 2 (R3)	0.46	0.43	0.44	0.44
Segment 3 (R4)	0.15	0.28	0.22	0.17
Tap 2 @ junction 3 (R5)	0.46	0.23	0.43	0.47
Segment 4 (R6)	0.15	0.35	0.14	0.16

posed improved hybrid algorithm combines the advantage of both the methods and accurately estimates the loop topology without any initial knowledge about the loop. Maximum Likelihood procedure with de-embedding is used in this paper to mask the strong reflections after identifying the discontinuities. This helps in estimating the far end discontinuities which has minimum contribution in the overall reflected signal. Simulation results of standard ANSI loops shows that the error in the prediction is less than 0.3% for lines with one or two discontinuities. For lines with more number of discontinuities the prediction accuracy is around 3% due to the feeble contribution of far end reflections in the received signal. This proposed method has the significant advantage in the measurement phase as measurement can be directly implemented on the DSL modem with a minimal additional firmware. The interpretation of the measured data can be carried out either online or offline.

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Subthreshold Modeling of Triple Material Gate-All-Around Junctionless Tunnel FET with Germanium and High-K Gate Dielectric Material

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Abstract: In this paper, a subthreshold analytical model for Triple Material Gate-All-Around (TMGAA) Junctionless Tunnel FET (JLTFET) with Germanium and High-K gate dielectric material is developed. Various performance metrics like Transconductance-to-Drain Current ratio, Subthreshold leakage current, and Subthreshold Swing are derived to model the subthreshold behavior of the device. The gate structure incorporates the effect of Germanium (Ge) and High-K gate dielectric material (Titanium Oxide) to combat the adverse effects imposed by the short channel. The subthreshold characteristics of Ge based JLTFET is compared with Silicon (Si) based TFET with SiO_2 as gate dielectric. The results concede that the developed model is highly immune to hot carrier damage because of high transconductance-to-drain current ratio of 50 V^{-1}, minimal leakage current, and subthreshold swing less than 40 mV/dec. The results of the proposed analytical model are validated using 2-D Sentaurus TCAD device simulator.

Keywords: Germanium; Junctionless; High-K gate dielectric; Hot Carrier Reliability; Tunnel FET; Transconductance-to-Drain Current ratio; Subthreshold Current; Subthreshold Swing.

Podpragovno modeliranje brezspojnega tunelskega FET iz treh materialov in neprekinjenimi vrati z germanijem in vrati iz dielektrika z visokim K

Izvleček: V članku je predstavljen podpragovni analitični model brezspojnega tunelskega FET (JLTFET) iz treh materialov in neprekinjenimi vrati (TMGAA) z germanijem in vrati iz dielektrika z visokim K. Za modeliranje podpragovnega obnašanja elementa so uporabljeni številni parametri, kot so razmerje transkonduktance s ponornim tokom, podporagovni uhajalni tok in podpragovni razpon. Za kompenziranje vplivov kratkega kanala struktura vrat vključuje vpliv germanija in titanovega oksida kot dilektričnega materiala z visokim K. Podpragovna karakteristika JLTFET z germanijem je primerjana silicijevim TFET z vrati iz SiO_2. Rezultati izkazujejo, da je model neobčutljiv na poškodbe vročih elektronov zaradi visokega transkonduktance s ponornim tokom (50 V^{-1}), majhnega uhajalnega toka in podpragovnega razpona manjšega od 40 mV/dec. Rezultati so potrjeni z analitičnim modelom v 2-D Sentaurus TCAD simulatorju.

Ključne besede: germanij; brezspojno; isolator vrat z visokim K; vroči elektroni; tunelski FET; razmerje transkonduktance s tokom ponora; podpragovni tok; podpragovni razpon

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1 Introduction

Aggressive downscaling of devices has almost reached a sub-nanometre regime, which deteriorates the gate control over the channel. Several novel device architectures have been introduced to suppress the Short Channel Effects (SCEs) [1]. For many technology generations, the gate electrode structures were made of silicon and silicon dioxide as gate dielectric material. As the channel length is reduced tremendously, other potential alternatives have to be explored to improve the subthreshold device characteristics [2 - 5]. Conventional Si based TFETs, suffers from an exponential increase

of the subthreshold leakage current and requires a very high gate voltage for TFET operation. Also, due to the continuous scaling of oxide thickness, the gate leakage current through the SiO_2 layer will be high. A potential candidate to continue FET scaling with improved subthreshold characteristics is Junctionless Tunnel FET (JLTFET) [6].

Junctionless FETs (JLFETs) have several advantages like diminished short channel effects, high I_{ON}/I_{OFF} ratio and nearly ideal subthreshold slope (SS ~ 60 mV/dec). The concept of gate material engineering is also incorporated to overcome the adverse short channel effects. Many analytical models have been proposed for junctionless TFETs. Triple Material Gate-All-Around (TMGAA) structures employ three gate materials with different work functions.

The gate material engineering [7 – 8] suppresses the peak electric field at the drain side, which is interpreted as a continuous reduction of Hot Carrier Effects (HCEs). Along with this, the usage of Germanium and Titanium Oxide (TiO_2) as High-K gate dielectric material [9 – 14] will improve the hot carrier reliability of the proposed device. High-K gate dielectric materials will minimize the tunneling of electrons through the gate-oxide interface and hence gate leakage current will also be minimized.

Subthreshold Current/Swing plays a vital role in low power circuits [15 – 19]. The use of Ge-based TMGAA-JLTFETs will efficiently enhance the subthreshold characteristics of the device. Device scientists have disclosed numerous analytical models for subthreshold analysis of MOSFETs [20 – 24]. But the effectiveness of combined design of Germanium (Ge), High-K gate dielectric (Titanium Oxide – TiO_2), Gate-All-Around (GAA) structure and three region doping profile in the channel has not yet been explored in short channel (12nm) junctionless tunnel FETs. Therefore, in this research work, we have developed a subthreshold analytical model of 12nm Triple Material Gate-All-Around (TMGAA) Junctionless Tunnel FET (JLTFET) with Germanium and High-K gate dielectric material for improved hot carrier reliability. An intensive comparative study with Si-SiO_2 interface is also carried out and the analytical model results are also simulated using TCAD.

In this paper, subthreshold analytical modeling has been developed by solving the 2-D Poisson equation by parabolic approximation. The key performance parameters like transconductance-to-drain current ratio, subthreshold current and subthreshold swing are derived by varying the device parameters such as drain-to-source voltage, germanium thickness, oxide thickness, channel length, and doping concentration. The obtained analytical and simulation results manifests that this transistor possesses higher transconductance, lower leakage current and steeper subthreshold slope compared to the bulk silicon FETs. The proposed analytical model results are validated using TCAD Sentaurus device simulator.

2 Mathematical Modeling

The cross sectional view and structure of the 12nm Ge based Triple Material Gate-All-Around Junctionless Tunnel FET (Ge-TMGAA-JLTFET) is shown in Fig.1. In this structure, the gate electrode comprises of three materials M1, M2, and M3 with different work functions. These three distinct materials are deposited over the respective gate lengths L_1, L_2 and L_3, with total gate length (12 nm) defined as $L = L_1 + L_2 + L_3$. The gate materials are chosen in such a way that $\emptyset_{M1} > \emptyset_{M2} > \emptyset_{M3}$. The work function of tunneling gate metal M_1 is $\emptyset_{M1}$ = 4.8 eV (Au), gate material M_2 with $\emptyset_{M2}$ = 4.6 eV (Mo), gate material M_3 at drain side is with $\emptyset_{M3}$ = 4.4 eV (Ti). The proposed model has a 12nm germanium channel, which is heavily n-type doped at $10^{19}cm^{-3}$. The formation of source and drain regions is without separate doping on the germanium channel.

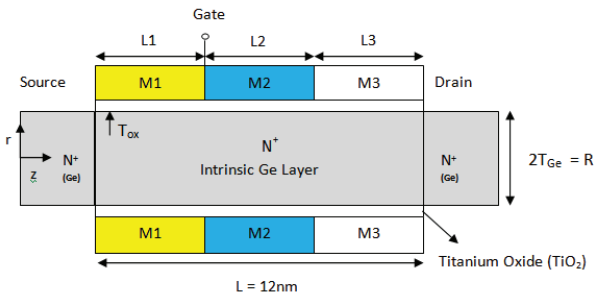

Figure 1: Cross section of 12nm Ge based Triple Material Gate-All-Around Junctionless Tunnel FET (Ge-TMGAA-JLTFET)

The 2-D Poisson's equation for the potential distribution in the channel is written as [4],

$$\frac{1}{r}\frac{\partial}{\partial r}\left(\frac{r\partial\phi_i(r,z)}{\partial r}\right)+\frac{\partial^2\phi_i(r,z)}{\partial z^2}=-\frac{qN_D}{\varepsilon_{Ge}};i=1,2,3 \quad (1)$$

where Ø(r, z) is the 2-D channel potential profile, q is the electric charge, N_D is the channel doping concentration, which is assumed to be uniform and ε_{Ge} is the permittivity of germanium. The potential profile in the vertical direction can be related by a simple parabolic function given by,

$$\phi(r,z)=S_1(z)+S_2(z)r+S_3(z)r^2 \quad (2)$$

where $S_1(z)$, $S_2(z)$ and $S_3(z)$ are arbitrary functions of z only.

The Poisson's equation is solved separately under the three gate metal regions by considering the boundary conditions stated below:

(a) The surface potential is a function of z only.

$$\phi(r=0,z)=S_1(z)=\phi_S(z) \tag{3}$$

(b) The electric field in the center of germanium pillar is zero.

$$\left.\frac{\partial\phi(r,z)}{\partial z}\right|_{r=0}=0 \tag{4}$$

(c) The electric field at the gate oxide interface is continuous.

$$\left.\frac{\partial\phi(r,z)}{\partial z}\right|_{r=R}=\frac{\varepsilon_{ox}}{\varepsilon_{Ge}R}\left[\frac{\psi_G-\phi_S(z)}{\ln\left(1+\frac{t_{ox}}{R}\right)}\right] \tag{5}$$

(d) The potential at the source end is:

$$\phi\left(r=0,z=0\right)=V_{bi} \tag{6}$$

(e) The potential at the drain end is:

$$\phi(r=R,z=L=L_1+L_2+L_3)=V_{bi}+V_{ds} \tag{7}$$

where, $\psi_G=V_{GS}-\phi_{M_i}+\chi+\frac{E_G}{2};i=1,2,3$ (8)

V_{GS} is the gate to source bias, E_G is the energy band gap of germanium, χ is the electron affinity of germanium, $\emptyset_{Mi}$ is the gate metal work function of three different materials and V_{bi} is the built-in potential.

In germanium based TMGAA-JLTFETs, we have three different gate materials with different work functions. Hence, the flat-band voltage for the three gate metal regions can be written as;

$$V_{FB_1}=\phi_{M1}-\phi_{Ge};V_{FB_2}=\phi_{M2}-\phi_{Ge};V_{FB_3}=\phi_{M3}-\phi_{Ge} \tag{9}$$

Where $\emptyset_{M1,}$ $\emptyset_{M2}$ and $\emptyset_{M3}$ denote the work functions of three different gate materials and $\emptyset_{Ge}$ is the work function of germanium.

Using the boundary conditions (3 – 7), we get the potential distribution under each gate metal region as;

$$\phi_{S1}(z)=P_1e^{\lambda z}+Q_1e^{-\lambda z}-\frac{\phi_{g1}}{\lambda^2};\quad for\quad 0\le z\le L_1 \tag{10}$$

$$\phi_{S2}(z)=P_2e^{\lambda(z-L_1)}+Q_2e^{-\lambda(z-L_1)}-\frac{\phi_{g2}}{\lambda^2};\ for\ L_1\le z\le L_1+L_2 \tag{11}$$

$$\phi_{S3}(z)=P_3e^{\lambda(z-(L_1+L_2))}+Q_3e^{-\lambda(z-(L_1+L_2))}-\frac{\phi_{g3}}{\lambda^2};\quad for\ L_1+L_2\le z\le L_1+L_2+L_3 \tag{12}$$

where the constants P_i and Q_i shown in (10 - 12) are obtained from the boundary conditions (3 - 7)

$$P_i=\frac{1}{(e^{\lambda L_i}-e^{-\lambda L_i})}\left[V_{bi}(1-e^{-\lambda L_i})+\frac{\phi_{g_i}}{\lambda^2}(1-e^{-\lambda L_i})+V_{ds}\right];i=1,2,3 \tag{13}$$

$$Q_i=\frac{1}{(e^{\lambda L_i}-e^{-\lambda L_i})}\left[V_{bi}(e^{\lambda L_i}-1)+\frac{\phi_{g_i}}{\lambda^2}(e^{\lambda L_i}-1)-V_{ds}\right];i=1,2,3 \tag{14}$$

The minimum surface potential under the gate metal region M_1 is given by:

$$\frac{d\phi_{S1}(z)}{dz}\Big|z=z_{\min}=0 \tag{15}$$

$$\phi_S(z_{\min})=2\sqrt{P_1Q_1}-\frac{\phi_g}{\lambda^2} \tag{16}$$

where, $\phi_g=-\left[\frac{qN_D}{\varepsilon_{Ge}}+\lambda^2\psi_G\right]$, $\lambda^2=\frac{2\varepsilon_{ox}}{R^2\varepsilon_{Ge}\ln\left(1+t_{ox}/R\right)}$ *and* $z_{\min}=\frac{1}{2\lambda}\ln\left(\frac{Q_1}{P_1}\right)$ (17)

2.1 Transconductance-to-Drain Current Ratio

The Transconductance-to-Drain Current ratio is strongly related to the performance measure of a device. This is obtained by differentiating the minimum surface potential with respect to gate-to-source voltage and it is given by [23],

$$\frac{g_m}{I_{ds}}=\frac{\frac{\partial\phi_S(\min)}{\partial V_{gs}}}{\frac{K_BT}{q}} \tag{18}$$

where K_B denotes Boltzmann constant = 1.38x10^{-23} and T is the Temperature.

On substituting (16) in (18), we get the Transconductance-to-Drain Current ratio as,

$$\frac{g_m}{I_{ds}} = \frac{-q}{K_B T \alpha}\left[\left(\sqrt{2(\beta-1)}\right)\left(1+\frac{1}{2\sqrt{V_{GS}}}\right)\right] \quad (19)$$

$$where\ \alpha = (e^{\lambda L_1} - e^{-\lambda L_1})/2\ \ and$$

$$\beta = -(e^{\lambda L_1} - e^{-\lambda L_1})/2$$

2.2 Subthreshold Current

In order to reduce the low power consumption, the supply voltage has been scaled down aggressively, which has driven attention towards the subthreshold leakage current. Hence, current in this subthreshold region has to be determined to assess the performance and reliability of the device.

The net current density in a semiconductor device can be defined as the total sum of drift and diffusion current densities. For Junctionless TFETs, the doping profile is uniform throughout the channel and because of the absence of concentration gradient, diffusion current density is neglected.

Hence, the total current density of Ge-TMGAA-JLTFET is written as,

$$J(r,z) = -q\mu n(r,z)E(z) \quad (20)$$

where E(z), is the applied electric field along the position of the channel (z).

In general, there are two electric field components which depends on both r and z. The electric field component along the channel is lateral electric field E (z) and the electric field component perpendicular to the channel is vertical electric field E(r). While analyzing the subthreshold current of the device, only E (z) is considered. Since, electron transport velocity along the channel can only be determined by the lateral electric field component (i.e. E (z)), which is obtained as follows,

$$E(z) = \frac{d\phi(r,z)}{dz} = \left[\frac{\lambda}{Sinh(\lambda L_j)}\right]\begin{bmatrix} V_{bi}\left[Cosh(\lambda z) - Cosh(\lambda(z-L_j))\right] \\ +\frac{\phi_{g_j}}{\lambda^2}\left[Cosh(\lambda z) - Cosh(\lambda(z-L_j))\right] \\ +V_{ds}\left[Cosh(\lambda z)\right] \end{bmatrix}; j = 1,2,3 \quad (21)$$

and $n(r,z) = n_i \exp\left(\frac{q}{K_B T}\left(\phi_j(r,z)\right)\right); j = 1,2,3$ is the electron carrier concentration.

By integrating (20), the subthreshold current is expressed as:

$$I_{ds}(z) = -\int_0^R q\mu\pi t_{ge} n_i \exp\left(\frac{q}{K_B T}\left(\phi_j(r,z)\right)\right)\left[\frac{\lambda}{Sinh(\lambda L_j)}\right] x$$

$$\begin{bmatrix} V_{bi}\left[Cosh(\lambda z) - Cosh(\lambda(z-L_j))\right] \\ +\frac{\phi_{g_j}}{\lambda^2}\left[Cosh(\lambda z) - Cosh(\lambda(z-L_j))\right] \\ +V_{ds}\left[Cosh(\lambda z)\right] \end{bmatrix} dr \quad (22)$$

By assuming that the subthreshold leakage occurs primarily at $z = z_{min}$, we obtain the subthreshold current as,

$$I_{ds} = \frac{\mu\pi t_{ge}^2 n_i^2 K_B T\left(1 - e^{-qV_{ds}/K_B T}\right)}{\delta N_D} \quad (23)$$

where $\delta = \exp\left(\vartheta_1 + \vartheta_2 + \vartheta_3\right)$

$$\vartheta_l = \frac{L_l}{q\left(\phi_{l,\min}/K_B T\right)}; l = 1,2,3$$

And μ = *electron carrier mobility = 3900 cm^2 /(V – s).*

2.3. Subthreshold Swing

Subthreshold swing normally describes the exponential behaviour of leakage current. For devices requiring high speed and low power, the subthreshold swing should be minimized. With steep subthreshold swing, improved I_{ON}/I_{OFF} ratio can be obtained and device reliability can be enhanced. Subthreshold slope is defined as the change in gate voltage required to reduce the subthreshold current by one decade. Subthreshold swing is the inverse of subthreshold slope.

Subthreshold swing is given as [24],

$$SS = \left(\frac{\partial \log I_{DS}}{\partial V_{GS}} \right)^{-1} \tag{24}$$

After approximation we obtain;

$$SS = \frac{K_B T}{q} \ln(10) \left[\frac{\partial \phi_{s,\min}}{\partial V_{gs}} \right]^{-1} \tag{25}$$

where,

$$\frac{\partial \phi_{s,\min}}{\partial V_{gs}} = \frac{\partial}{\partial V_{gs}} \left(\frac{\left\{ \left[\left(V_{bi} + \frac{\phi_{g1}}{\lambda^2} \right) \sqrt{2(\beta - 1)} \right] - V_{ds} + \left[V_{ds} \sqrt{2(\beta - 1)} \left(V_{bi} + \frac{\phi_{g1}}{\lambda^2} \right) \right] + \left[\frac{qN_D}{\varepsilon_{Ge}} + \lambda^2 (V_{GS} - V_{FB}) \right] \right\}}{Sinh(\lambda L_1)} \right) \tag{26}$$

On substituting (26) in (25) and on simplification, the final expression of subthreshold swing is obtained as,

$$SS = \frac{K_B T}{q} \ln(10) \left[\frac{-1}{\alpha} \left[\sqrt{2(\beta - 1)} \left(1 + \frac{1}{2\sqrt{V_{GS}}} \right) \right] \right]^{-1} \tag{27}$$

3 Results and Discussions

The proposed analytical model is verified using a 2-D TCAD device simulator. With uniformly n-type doped (N_d=10^{19}cm^{-3}) source, drain and channel regions, a germanium based TMGAA Junctionless TFET structure is implemented. The developed model has a triple material gate-all-around structure, where the work functions of gate metals M1, M2 and M3 are chosen to be 4.8eV, 4.6eV, and 4.4eV respectively. The analytical model results are plotted using MATLAB and compared with the TCAD device simulator results. Drift Diffusion (DD) model has been employed to model the carrier transport mechanism in device simulation. Also, to model the carrier concentration, Shockley-Read-Hall (SRH) recombination model combined with Auger recombination model are used in the simulation.

The total channel length of the proposed device is chosen to be 12nm. The remaining device parameters used are: channel thickness (t_{ge}) is 2nm, gate-oxide thickness (t_{ox}) is 1nm and V_{ds} = 0.3V. The length of the three gate metal regions is: L_1= L_2= L_3=4nm.

The transconductance-to-drain current ratio of 12nm germanium and silicon based triple material gate-all-around junctionless tunnel FET is shown in Fig.2. The results clearly indicate that the developed Ge based TMGAA-JLTFET has higher value of transconductance-to-drain current ratio of nearly 50V^{-1}. However, in silicon based JLTFETs with SiO_2 as gate dielectric material, the ratio is 35V^{-1}, which is less when compared to the proposed germanium based device. This implies that Ge-TMGAA-JLTFETs are profoundly insusceptible to Hot Carrier Effects (HCEs). Such a model with a high value of g_m/I_{ds} ratio is strongly desired for high-efficiency photovoltaic cell applications. Thus, the anticipated analytical results of the proposed model are validated against TCAD device simulation results.

The variation of transconductance-to-drain current ratio along the channel length is plotted for different values of High-K gate dielectric materials in Fig.3. As the channel length increases, g_m/I_{ds} ratio also increases. The term 'K' denotes the relative permittivity of the gate oxide material. Materials with high relative permittivity are useful in manufacturing high-value capacitors, high power RF transmitters and some electro-optical appliances. With higher relative permittivity of Titanium Oxide (TiO_2), the g_m/I_{ds} ratio is increased. The use of high-K gate dielectric material over conventional gate dielectric material (Silicon dioxide – SiO_2), has offered augmented carrier generation efficiency in the channel region. Thus, the projected model with germanium

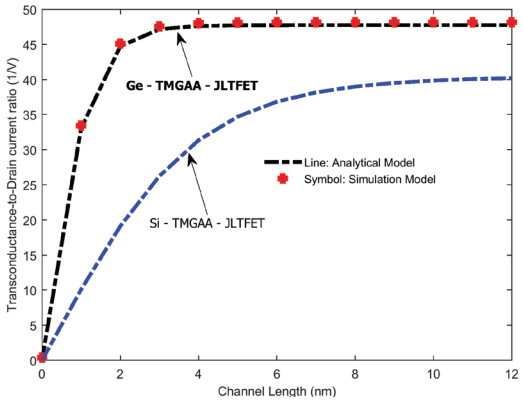

Figure 2: Transconductance-to-Drain Current ratio of Ge-TMGAA-JLTFET and Si-TMGAA-JLTFET with L=12nm, t_{ox}=2nm and t_{ge}=4nm.

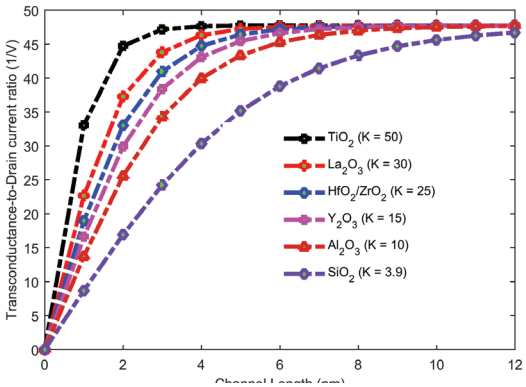

Figure 3: Plot of Transconductance-to-Drain Current ratio of Ge-TMGAA-JLTFET for different values of High-K gate dielectric materials.

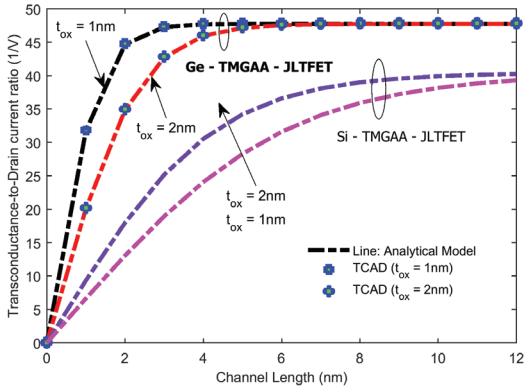

Figure 4: Variation of Transconductance-to-Drain Current ratio of Ge and Si based TMGAA-JLTFET for different values of gate oxide thickness.

and high-K gate dielectric material has significantly contributed to the performance of the device.

From Fig.2, we have noticed the combined supremacy of germanium and titanium oxide in proliferating the transconductance-to-drain current ratio. Here in Fig.4, also, it is clearly witnessed that the characteristics of the proposed device are better than in conventional Si-SiO_2 based devices. Fig.4. depicts the g_m/I_{ds} variation of Ge versus Si based TMGAA-JLTFET for various values of oxide thickness t_{ox}=1, 2nm. For thinner oxide thickness of t_{ox}=1nm, the g_m/I_{ds} ratio is high for both devices. But, the overall ratio is much higher for Ge-TMGAA-JLTFET, which again proves to be pertinent for high-efficiency, low power solar cell applications.

Fig.5. (a) illustrates the variation of subthreshold current for Ge and Si based TMGAA-JLTFET for various values of V_{ds}=0.3V and 0.4V. It is shown that in the proposed device the subthreshold leakage current is minimized when compared to Si-SiO_2 based junctionless TFETs. With Si-SiO_2 interface, several unwanted side effects can occur, remarkably the Hot Carrier Effect (HCE), which causes a displacement in the threshold voltage value and consequently leads to subthreshold leakage. For V_{ds}=0.3V, the subthreshold leakage is smaller compared to V_{ds}=0.4V. Also, when the gate voltage equals the drain voltage, the hot carrier injection is at maximum.

For higher drain voltages, the peak electric field will be at the drain end. The high electric field leads to avalanche multiplication of carriers. These carriers in turn gain high energy and become "Hot" electrons. The hot carriers can easily get trapped into the oxide layer and cause severe reliability issues. But with the incorporation of three different doping profiles in the gate region, the peak electric field at the drain side is suppressed effectively, shown in Fig.5.(b).

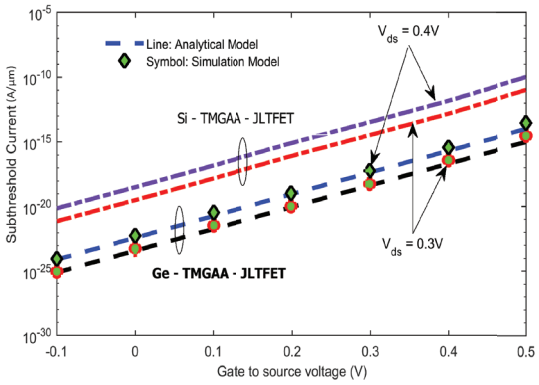

Figure 5.a: Variation of Subthreshold Current of Ge and Si based TMGAA-JLTFET for different values of drain-to-source voltage.

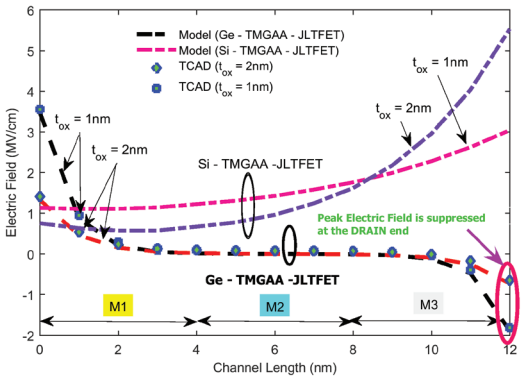

Figure 5.b: Electric Field variation of Ge and Si based TMGAA-JLTFET along the channel length for various values of oxide thickness.

Hot carrier damage may affect the endurance of non-volatile memory. Hot Carrier Effect (HCE) refers to device degradation or instability caused by hot carrier injection. This HCE being an important factor in the small-scale integrated circuits has to be reduced with-

out negotiating the advancements in device scaling. Hence, our proposed model (Ge-TMGAA-JLTFET) has overcome this hot carrier degradation with the usage of Titanium Oxide (TiO_2) as gate dielectric material. Fig.6. depicts the variation of subthreshold current for various channel lengths, L=15nm, 30nm and 45nm. Short channel (12nm) device using High-K dielectric material, offers improved hot carrier reliability, which is endorsed by minimum subthreshold leakage current of 10^{-25}A/μm near the subthreshold regime.

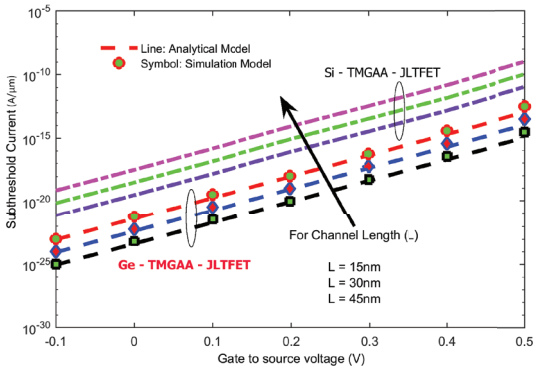

Figure 6: Subthreshold Current variation of Ge and Si based TMGAA-JLTFET for different channel lengths of L=15nm, 30nm and 45nm.

The plot of subthreshold swing along the channel length for various values of germanium thickness is shown in Fig.7. The proposed analytical model results are compared with Si based TMGAA-JLTFET and simulated using TCAD device simulator. It is inferred that the subthreshold swing has attained a minimum value of 35mV/dec, when compared to Si based JLTFETs having subthreshold swing less than 50mV/dec. With minimum germanium film thickness, the subthreshold degradation is also minimal.

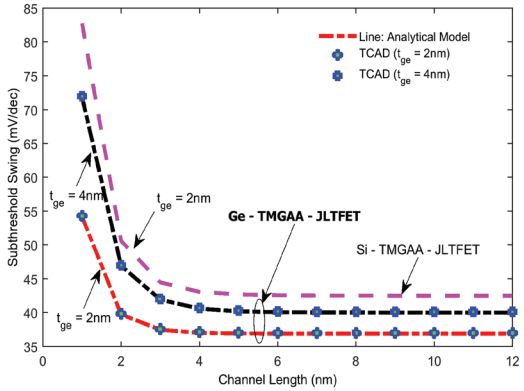

Figure 7: Dependence of Subthreshold Swing of Ge and Si based TMGAA-JLTFET along the channel lengths for various values of germanium thickness.

Fig.8. illustrates the dependence of subthreshold swing of Ge-TMGAA-JLTFET for various values of oxide thickness. As the oxide thickness is reduced from 3nm to 1nm, we witness that the subthreshold swing is also reduced to a greater extent. This demonstrates that, with thinner gate oxide, the electric field component can pervade the channel region more easily. Once the electric field components are strong enough, then the gate controlling capability is reinforced and subthreshold degradation in minimized. With lightly doped drain structure, the peak electric field at the drain end is suppressed and hence Drain Induced Barrier Lowering (DIBL) effect is also reduced tremendously.

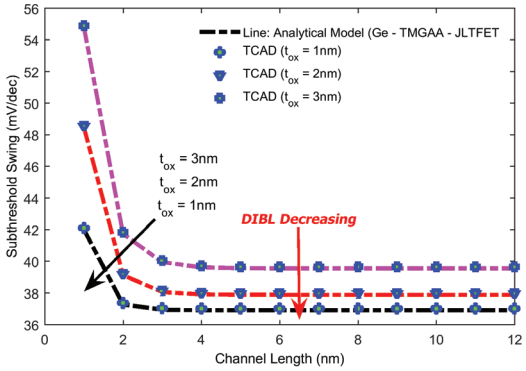

Figure 8: Plot of Subthreshold Swing of Ge-TMGAA-JLTFET along the channel lengths for various values of oxide thickness.

Fig.9. depicts the subthreshold swing of Ge-TMGAA-JLTFET for various values of doping concentration. For junctionless TFETs, the doping profile is uniform throughout the device. With higher doping concentration of $N_d=10^{20}cm^{-3}$, it is inferred that the subthreshold degradation is reduced.

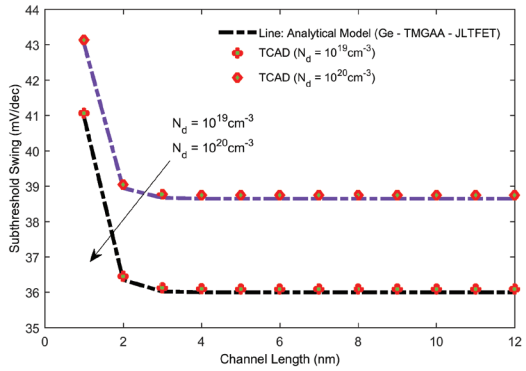

Figure 9: Subthreshold Swing of Ge-TMGAA-JLTFET along the channel lengths for various values of doping concentration.

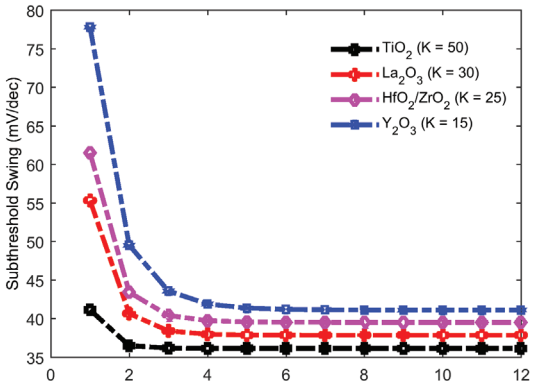

Figure 10: Plot of Subthreshold Swing of Ge-TMGAA-JLTFET along the channel lengths for different types of High-K gate dielectric materials.

The dependence of subthreshold swing of Ge-TMGAA-JLTFET for various types of High-K gate dielectric materials is shown in Fig.10. The subthreshold swing of the proposed model has been evaluated for various high-K gate dielectric materials such as Yttrium oxide, Hafnium/Zirconium oxide, Lanthanum oxide and Titanium oxide. The values of Transconductance-to-Drain Current ratio and Subthreshold Swing of Ge-TMGAA-JLTFET for different types of High-K gate dielectric material are listed in Table.1. The first row of Table.1 clearly indicates that, among different High-K materials, Titanium oxide offers less subthreshold swing and high g_m/I_{ds} ratio. It is visualized from Fig.10 that, Titanium oxide with higher dielectric constant, can hold large number of charge carriers and subthreshold degradation of the device is also reduced. The precise results of Ge and Si based TMGAA-JLTFET are listed in Table.2. The results suggest that the proposed model incorporated with Germanium, Titanium oxide and three different gate materials such as Gold, Molybdenum, and Titanium is a good solution and also as an excellent candidate for Improved Hot Carrier reliability.

4 Conclusions

In this paper, a subthreshold model of 12nm triple material gate-all-around junctionless tunnel FET with germanium and titanium oxide as high-K gate dielectric material is developed. The enhanced subthreshold characteristics of this novel device have been verified and validated by comparing the results with Si-SiO_2 based JLTFETs. Transconductance-to-Drain Current ratio, Subthreshold Current and Subthreshold Swing are derived analytically and simulated using the 2-D Sentaurus TCAD device simulator for various device parameters. Good agreement is obtained between our proposed analytical model and obtained simulation results. The results concede that Ge-TMGAA-JLTFET with TiO_2 exhibits improved hot carrier reliability with higher g_m/I_{ds} ratio, low leakage current and steep subthreshold swing. The proposed model proves to be an excellent device for high-efficiency photovoltaic cells, solar cell applications and solid-state LEDs.

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Table1: Transconductance-to-Drain Current ratio and Subthreshold Swing for Ge-TMGAA-JLTFET for different types of High-K gate dielectric material

High-K gate dielectric materials	Dielectric Constant (K)	Ge-TMGAA-JLTFET	
		Transconductance-to-Drain Current ratio (V^{-1})	Subthreshold Swing (mV/dec)
Titanium Oxide , TiO_2	50	49	35
Lanthanum Oxide, La_2O_3	30	45	39
Hafnium/Zirconium Oxide, HfO_2/ZrO_2	25	43	43
Yttrium Oxide, Y_2O_3	15	42	45

Table 2: Subthreshold parameters of Ge and Si-TMGAA-JLTFET with Titanium Oxide as gate dielectric material

Subthreshold Parameters	Device Type (L = 12nm)	
	Ge – TMGAA-JLTFET	Si – TMGAA-JLTFET
Transconductance-to-Drain Current Ratio	$49V^{-1}$	$39V^{-1}$
Subthreshold Current with Vgs = -0.1V	10 - 25A/μm	10 - 20A/μm
Subthreshold Swing	<35mV/dec	<50mV/dec

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A Novel Approach to Reduce the PMEPR of MCPC Signal Using Random Phase Algorithm

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Abstract: This paper aims to reduce the Peak-to-Mean Envelope Power Ratio (PMEPR) of a Multicarrier Complementary Phase Coded (MCPC) signal. A MCPC signal consists of P subcarriers which are phase modulated by N distinct phase sequences. Each of these P subcarriers is spaced by the inverse duration of a phase element, which constitutes an Orthogonal Frequency Division Multiplexing (OFDM) signal. A probabilistic approach, namely, Random Phase Updating (RPU) algorithm, is used to reduce the PMEPR of the generated MCPC signal. The technique is applied to higher order MCPC signals and a comparison of the peak sidelobe ratio (PSLR) and integrated sidelobe ratio (ISLR) is performed. The complex envelopes, autocorrelations and ambiguity functions of the MCPC signal obtained by the above mentioned methods are analysed. The Complementary Cumulative Distribution Function (CCDF) is plotted to validate the PMEPR reduction obtained by the application of the RPU algorithm which enables us to determine the most suitable approach required for radar applications.

Keywords: Integrated Sidelobe Ratio (ISLR); Multicarrier Complementary Phase Coded (MCPC); Orthogonal Frequency Division Multiplexing (OFDM); Peak to Mean Envelope Power Ratio (PMEPR); Peak Sidelobe Ratio (PSLR); Random Phase Updating (RPU)

Nov način zniževanja PMEPR MCPC signala z uporabo naključnega faznega algoritma

Izvleček: Članek opisuje zmanjšanje vršno-srednjega razmerja moči (PMEPR) večnosilčnega komplementarno fazno kodiranega (MCPC) signala. MCPC signal vsebuje podnosilce P, ki so fazno modulirani z N različnimi faznimi sekvencami. Vsak podnosilec P je ločen z inverznim trajanjem faznega elementa, ki oblikuje OFDM signal. Za zniževanje PMEPR je uporabljen verjetnostni pristop z naključno fazno osvežitvijo (RPU). Tehnika je uporabljena na višjih redih MCPC signala. Opravljanje primerjava razmerja vrhnjega snopa (PSLR) in razmerja integriranega snopa (ISLR). Analizirani so kompleksni ovoji, avtokorelacije in nejasne funkcije MCPC signala. Za validacijo znižanja PMEPR na osnovi RPU funkcije je uporabljena CCDF funkcija kot najboljši pristop za uporabo v radarju.

Ključne besede: ISLR; MCPC; OFDM; PMEPR; PSLR; RPU

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1 Introduction

The most important characteristics of a radar signal are its range and resolution [1]. In order to improve the range of the signal, the pulse width must be increased. This hampers its resolution. On the other hand, decreasing the pulse width improves the resolution of the radar signal but results in deterioration of its range. We use pulse compression technique to balance the trade-off between the range and resolution of the radar signal. Phase coding of the transmitted radar signal helps achieve pulse compression.

The advantage of a multicarrier system over single carrier transmission in terms of bandwidth efficiency [2] is clearly demonstrated by the Orthogonal Frequency Division Multiplexing (OFDM) technique. OFDM technology forms the foundation for a number of communication systems such as Digital Audio and Video Broadcasting, IEEE 802.11g, Digital Subscriber Lines (xDSL). The latest applications include LTE and LTE Advanced. OFDM has also been applied to radar systems for object tracking and target detection. This application has been realized in different types of multipath and clutter environments.

However, the multicarrier signals have high variations present in the complex envelope. These variations are quantified by a parameter, namely Peak to Mean Envelope Power Ratio (PMEPR). Higher value of PMEPR indicates more abrupt variations in the complex envelope of the signal and the power amplifier at the transmitter end has to be very sensitive to track these sudden variations. Since design of such a sensitive amplifier is complicated, reduction of the PMEPR of the radar signal becomes essential.

The radar signal is phase coded using P4 [3] phase sequences which are complementary in nature. This helps us to accomplish Pulse Compression. The generated signal is a MCPC Signal as described by N. Levanon in [4]. The only drawback of this signal is its high value of PMEPR.

Several attempts have been made to reduce the effect of PMEPR in multicarrier schemes and emphasis is on data transmission applications, using methods such as near- complementary sequence [5], peak power reduction of OFDM signals with sign adjustment [6], tone reservation [7,8] and a joint technique [9]. However several authors have investigated to reduce PMEPR in multicarrier signals for radar applications. In [10], phase modulation is used and in [11] PMEPR is reduced using iterative least square algorithm and in [12] genetic algorithm used. The objective of this paper is to address the issue of high PMEPR of a MCPC radar signal using RPU algorithm whose implementation until now has only been restricted to data transmission systems.

2 Characteristics of MCPC Signal

The multicarrier phase-coded signal is based on the principle of OFDM technique. It comprises of N subcarriers which are phase modulated by N distinct phase sequences. The frequencies of the subcarriers are $1/t_b$ apart, where t_b is the duration of each phase element.

$$s(t)=\begin{cases}\sum_{p=1}^{N} A_p \exp\left[j\left\{ 2\pi f_s t\left(\frac{N+1}{2}-p\right)+\theta_p \right\}\right] \sum_{q=1}^{N} u_{p,q}\left[t-(q-1)t_b\right], & 0\le t\le Nt_b \\ 0, \quad elsewhere\end{cases} \tag{2}$$

Where, $u_{p,q}(t)=\begin{cases}\exp\left(j\phi_{p,q}\right), & 0\le t\le t_b \\ 0 \quad , \quad elsewhere\end{cases}$

A_p is the amplitude weight applied to the subcarriers and θ_p is the random phase shift introduced by the transmitter to each carrier. $\phi_{p,q}$ is the q^{th} phase of the p^{th} subcarrier.

The phase sequences are generated using P4 phase sequences.

The equation for generating P4 phase sequence is given in equation 1.

$$\phi_q=\frac{\pi}{N}(q-1)^2-\pi(q-1) \quad q=1,2,3.....N \tag{1}$$

For a 5 x 5 MCPC we generate the P4 phase sequences by setting N = 5. The first sequence which is obtained by cyclically shifting to attain the other 4 phase sequences. The P4 phase sequences obtained are shown in Table 1. All the phases are in radians.

Table 1: P4 Phase Sequences

Seq 1 [rad]	Seq 2 [rad]	Seq 3 [rad]	Seq 4 [rad]	Seq 5 [rad]
0	-2.513	-3.769	-3.769	-2.513
-2.513	-3.769	-3.769	-2.513	0
-3.769	-3.769	-2.513	0	-2.513
-3.769	-2.513	0	-2.513	-3.769
-2.513	0	-2.513	-3.769	-3.769

The phase sequence order of a MCPC signal is used to indicate the phase sequence which is used to modulate a particular subcarrier. For example, a phase sequence order of [3 5 2 1 4] involves the phase modulation of the first subcarrier with phase sequence 3, second subcarrier with phase sequence 5 and so on, where the phase sequences are obtained from Table 1.The complex envelope [3] of the MCPC signal is given by equation 2.

Using the above equations the complex envelopes for MCPC signals having different number of subcarriers such as 7 x 7, 9 x 9, 11 x 11, etc. can be generated using their respective phase sequences. The block diagram for generating the MCPC signal is as shown in Fig. 1.

The PMEPR value for different phase sequence orders is

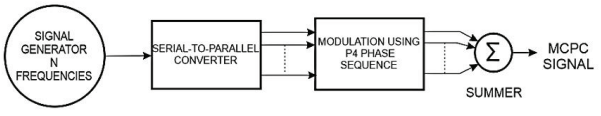

Figure 1: Generation of MCPC Signal

illustrated in Table 2.

Table 2: PMEPR values of MCPC signals for different sequence orders

Sequence order	PMEPR using P4
[3 5 2 1 4]	4.39
[3 4 5 1 2]	1.73
[3 1 2 5 4]	2.97
[3 2 4 1 5]	3.48

The ambiguity function for the phase sequence order [3 5 2 1 4] is depicted in Fig. 2.

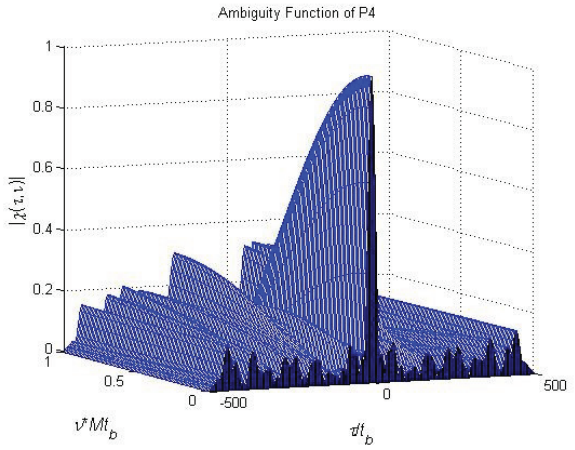

Figure 2: Ambiguity Function of MCPC signal

Autocorrelation function is the correlation of a signal with a delayed copy of itself as a function of delay [13]. The width of the mainlobe gives an idea about the range of the radar signal and the sidelobe power levels govern the resolution of the signal.

Ambiguity function [14] is a two-dimensional function of delay and Doppler frequency that measures the correlation between a waveform and its Doppler distorted version. Autocorrelation and the ambiguity function together help analyze the target detection capabilities of the radar signal. When we have multiple point targets we have a superposition of ambiguity functions. A weak target located near a strong target can be masked by the sidelobes of the ambiguity function cantered around the strong target. Hence, we have to minimize the minor lobes for detection of secondary targets.

The quality of the radar signal can also be assessed using Peak Sidelobe Ratio (PSLR) and Integrated Sidelobe Ratio (ISLR). The Peak Sidelobe Ratio (PSLR) is the ratio between the returned signal of the mainlobe and that of the maximum sidelobe power. The Integrated Sidelobe Ratio (ISLR) is the ratio of the energy in the sidelobes to that contained in the mainlobe. The PSLR and ISLR for the conventional 5 x 5 MCPC signal were found to be 8.32dB and 3.34dB respectively.

3 Random Phase Updating Algorithm

The only drawback of the MCPC signal is its high value of PMEPR. Reducing this quantity will result in the reduction of the variations in the complex envelope. This issue can be addressed by using one of the methods suggested in [5]. However the technique thus adopted must not only ensure a reduction in PMEPR but also maintain acceptable autocorrelation and ambiguity functions. An effective approach is to make use of the Random Phase Updating (RPU) algorithm [15] which comes under the purview of the probabilistic domain. The block diagram for generating the MCPC signal with RPU algorithm is shown in Fig. 3.

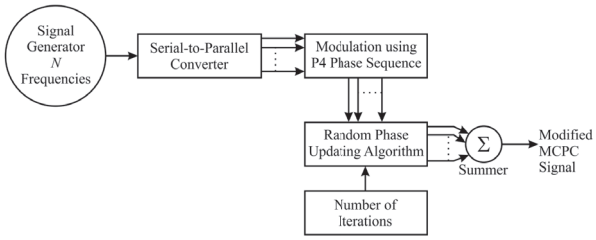

Figure 3: RPU Algorithm for generation of MCPC signal

The random phase updating algorithm generates phases and adds them to the pre-existing P4 phase values as given by equation 3.

$$\left(\phi_p\right)_i = \left(\phi_p\right)_{i-1} + \left(\Delta\phi_p\right)_i \tag{3}$$

In equation 3, *i* denotes the iteration, and *p* denotes the subcarrier. $(\phi_p)_i$ is the phase of the p^{th} subcarrier in the i^{th} iteration and $(\Delta\phi_p)_l$ is the incremental phase added to the p^{th} subcarrier in the i^{th} iteration.

The algorithm uses the number of iterations as the control parameter. The incremental phases are generated based on a particular probability density function and added to each subcarrier. Gaussian distribution or uniform distributions are used to generate these incremental phases. The complex envelope is obtained and the corresponding value of PMEPR is calculated for every iteration. Once the required number of iterations is carried out, the complex envelope and the phase sequences corresponding to the lowest value of PMEPR are selected. The autocorrelation function and the ambiguity function are plotted for the selected complex envelope. The flowchart in Fig. 4 describes the random phase updating algorithm.

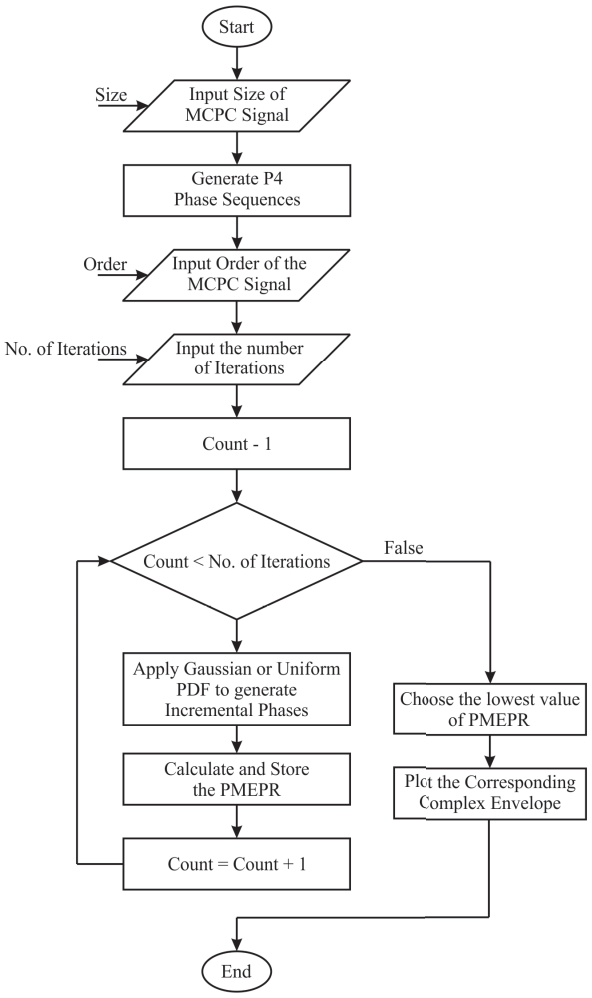

Figure 4: Flowchart of the RPU Algorithm

The Gaussian distribution is given by $\Delta\phi_p = N(0, x^2)$

The Uniform distribution is given by $\Delta\phi_p = Unif(0, x^2)$

Here, $(\Delta\phi_p)$ is the incremental phase generated based on a particular distribution. x belongs to {0.1, 0.25, 0.5, 0.75, 1} for a 5 x 5 MCPC signal. Similarly, x belongs to {0.1, 0.25, 0.4, 0.55, 0.7, 0.85, 1} for a 7 x 7 MCPC signal and {0.1, 0.21, 0.32, 0.43, 0.55, 0.66, 0.77.0.88, 1} for a 9 x 9 MCPC signal. For each subcarrier, the incremental phases are obtained by calculating the CDF of one of the values in the vector 'x' which is selected randomly.

4 Results

In this section, a comparison is made between the conventional MCPC signal and the signal subjected to the Random Phase Updating Algorithm for a large number of iterations. This technique has been applied to the MCPC signal that is based on the cyclic shifts of the P4 phase sequences for the order [3 5 2 1 4]. The complex envelope, autocorrelation and ambiguity function obtained using the RPU algorithm are plotted against those obtained using the conventional method.

In the random phase updating algorithm, the random numbers generated can be either repetitive or non-repetitive in nature. If the random numbers are repetitive, the number of possible combinations is large. For a 5 x 5 MCPC signal, there are 5^5 different combinations possible if the random numbers are repetitive and only 5! combinations if the random numbers are non-repetitive. A comparison of the results obtained using both the results is made in this section.

Further, for the generation of the incremental phases, the random phase updating algorithm uses either Gaussian Distribution or Uniform Distribution. A comparison of the results obtained using the above mentioned distributions along with the two methods of generation of random numbers is performed in this section.

Due to the random nature of the phase updating process, the complex envelope, autocorrelation function and ambiguity function need not be unique. However, the lowest value of PMEPR for the complex envelope remains the same when the number of iterations are very large.

It could be observed that the lowest value of PMEPR obtained when the random numbers were generated in a repetitive manner was almost identical to those obtained by generating non-repetitive numbers.

4.1 RPU Using Gaussian Distribution

The results obtained in this subsection illustrate the complex envelope, autocorrelation function and the

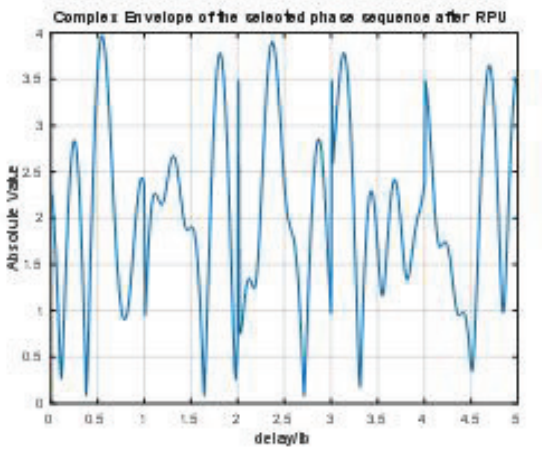

Figure 5: Complex Envelope of MCPC signal using RPU algorithm

ambiguity function obtained for a 5 x 5 MCPC signal with phase sequence [3 5 2 1 4] using the RPU algorithm where the incremental phases are generated based on Gaussian distribution. Fig. 5, Fig. 6 and Fig. 7 illustrate the case where the random numbers are non-repetitive in nature.

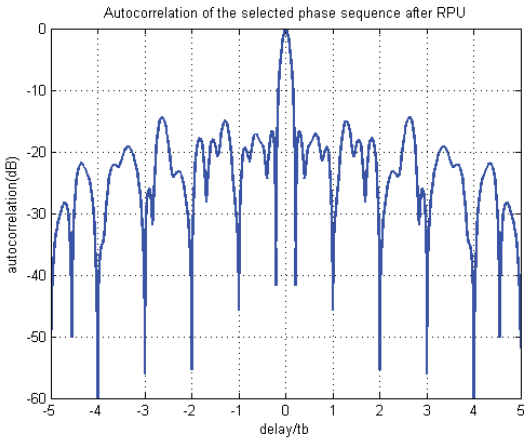

Figure 6: Autocorrelation Function of MCPC Signal using RPU Algorithm

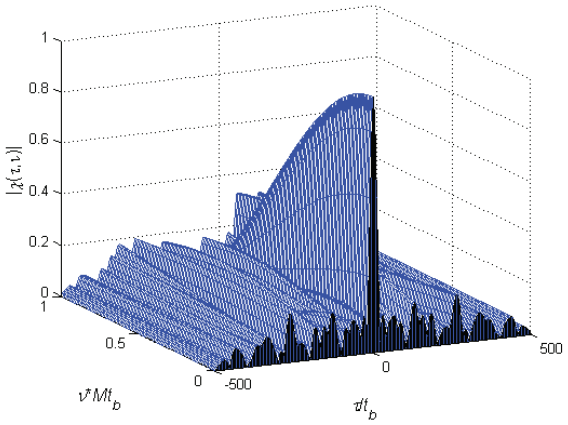

Figure 7: Ambiguity Function of MCPC Signal using RPU Algorithm

Table 3 shows the comparison of PMEPR between conventional method and the RPU algorithm.

Table 3: PMEPR comparison table

Sequence Order	PMEPR using conventional MCPC Signal	PMEPR using RPU algorithm	
		Using non-repetitive random numbers	Using repetitive random numbers
[3 5 2 1 4]	4.39	2.99	2.99
[3 4 5 1 2]	1.73	1.53	1.54
[3 1 2 5 4]	2.97	2.59	2.58
[3 2 4 1 5]	3.48	2.27	2.25

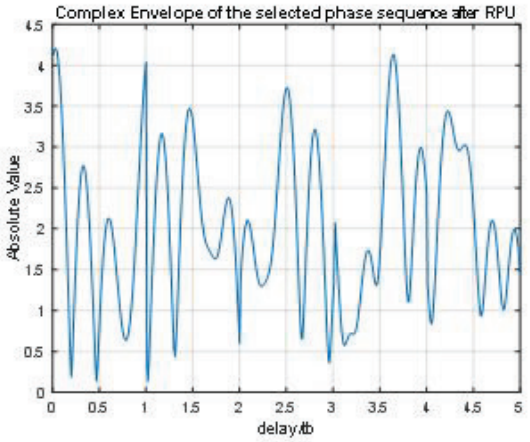

Figure 8: Complex Envelope of MCPC signal obtained by RPU Algorithm

It can be clearly observed that the PMEPR values obtained using both the methods of generating random numbers are identical and better than those obtained using the conventional method.

The autocorrelation function shown in Fig. 6 has sidelobe power levels at approximately 15dB. This shows that the target detection capabilities of the radar signal are preserved after applying the technique.

From Fig. 7 it can be seen that the sidelobe ridges in the ambiguity function are lower for high Doppler shifts when compared to the conventional MCPC signal demonstrating that the target detection capabilities have been conserved.

The PSLR and ISLR for the MCPC signal after the application of the RPU technique were found to be -6.92dB and 4.45dB respectively. It can be observed that these values are higher than that obtained for the conventional MCPC signal, showing that there is a slight degradation in the resolution of the signal. There is a trade-off between PMEPR reduction and increased sidelobe-power levels. However, this minor disadvantage of distribution of the mainlobe power amongst the sidelobes does not compare with the advantage of PMEPR reduction.

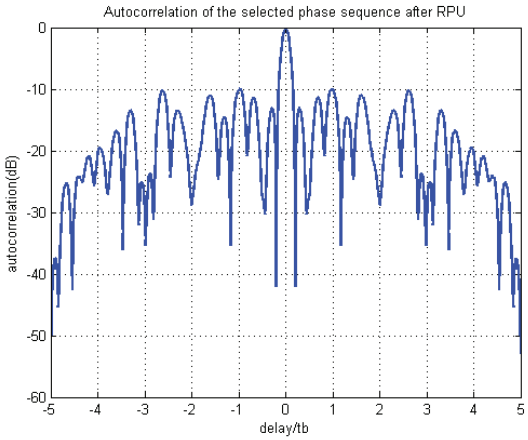

Figure 9: Autocorrelation Function of MCPC Signal obtained by RPU Algorithm

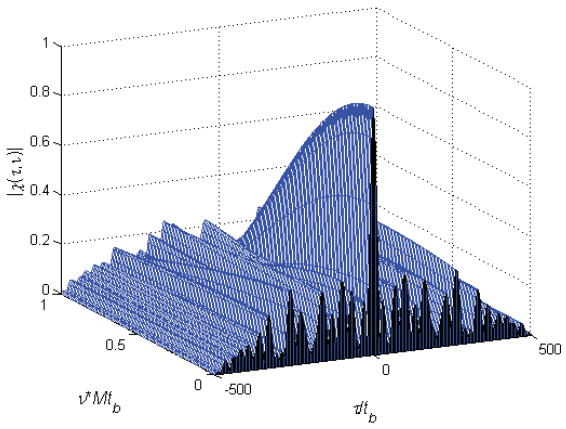

Figure 10: Ambiguity Function of MCPC Signal obtained by RPU Algorithm

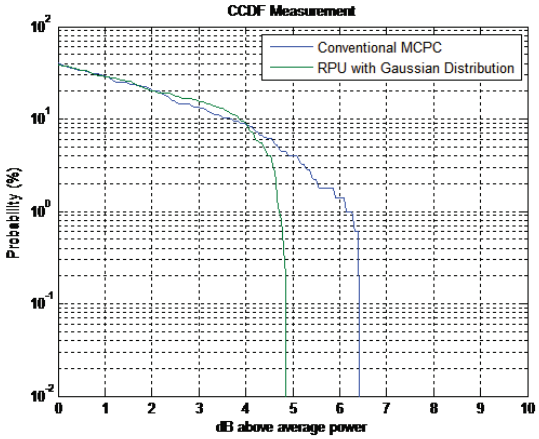

Figure 11: CCDF comparison

4.2 Using Uniform Distribution

This section demonstrates results obtained when the incremental phases are generated based on Uniform distribution for the sequence order [3 5 2 1 4]. The graphs plotted in Fig. 8, Fig. 9 and Fig. 10 illustrate the complex envelope, autocorrelation function and ambiguity function respectively for this case.

The PMEPR comparison between conventional MCPC signal and the signal obtained by the application of RPU algorithm based on Uniform distribution is illustrated in Table 4.

Table 4: PMEPR comparison table

Sequence Order	PMEPR using Conventional MCPC Signal	PMEPR using RPU algorithm	
		Using non-repetitive random numbers	Using repetitive random numbers
[3 5 2 1 4]	4.39	3.01	2.99
[3 4 5 1 2]	1.73	1.57	1.53
[3 1 2 5 4]	2.97	2.56	2.60
[3 2 4 1 5]	3.48	2.24	2.26

From Table 4, it can be noted that the PMEPR value has considerably reduced for all sequence orders when RPU algorithm is incorporated in the phase generation process of MCPC signal generation.

The autocorrelation function obtained indicates peak sidelobe power levels to be approximately 10dB which suggests that the target tracking ability of the signal based on Uniform distribution is marginally inferior to the signal obtained using Gaussian distribution.

The ambiguity function obtained shows that the signal has low sidelobe power levels at higher Doppler shifts similar to the case when Gaussian distribution is used, which is a favourable aspect. The PSLR and ISLR were found to be 4.75dB and 7.19dB respectively. The resolution of the radar signal is worse than that of the conventional MCPC signal and that of the signal obtained using Gaussian distribution but is still effective in reducing PMEPR.

4.3 Complementary Cumulative Distribution Function (CCDF)

The CCDF curve provides an idea of the distribution of power of the complex envelope around the mean. It is

a plot of Power levels above the Average Power in dB vs Probability of occurrence of that particular power level above the mean power in the complex envelope under consideration. As the area under the curve increases, the power variation around the mean increase and this leads to an increased value of PMEPR. Conversely, as the area under the curve reduces, the PMEPR also has a lower value as the power variations around the mean is reduced.

The graph in Fig. 11 illustrates the comparison between the conventional MCPC signal and the signals obtained using the RPU algorithm with Gaussian distribution. It can clearly be seen that the complex envelope obtained using the RPU algorithm with Gaussian PDF has a much lesser area than the conventional MCPC signal and hence possesses a much lesser value of PMEPR. Thus the results obtained using the CCDF graph are in coherence with those shown in Table 3 and Table 4.

4.4 RPU Algorithm applied to Higher Order MCPC Signals

In this subsection, the RPU algorithm is applied to MCPC signals with greater number of subcarriers to assess whether the technique performs favourably in different scenarios. From the previous subsections, we can observe that the PMEPR value obtained using both Gaussian distribution and Uniform distributions are identical. Therefore, either of these distributions can be used for the reduction of PMEPR. Table 5 and Table 6 illustrate the PMEPR comparison between conventional MCPC and MCPC signal obtained using RPU algorithm for a 7 x 7 and 9 x 9 MCPC signal respectively. The number of possible sequence orders for a 7 x 7 and a 9 x 9 MCPC signal are 7! and 9! respectively. Since the values are very large, the Table 5 and Table 6 shows the sequence orders corresponding to the highest, lowest and an intermediate value of PMEPR obtained for a given order of the MCPC signal.

Table 5: PMEPR comparison for MCPC of order 7 x7

Sequence Order 7 x 7	PMEPR using Conventional MCPC signal	PMEPR using RPU algorithm
[2 5 6 7 4 1 3]	6.14	3.44
[7 1 2 3 4 5 6]	1.92	1.75
[7 1 3 2 6 4 5]	4.01	3.29

It can be inferred that the RPU algorithm delivers promising results in terms of PMEPR reduction for a 7x7 and 9x9 MCPC signal and can be suitably applied to higher order signals.

Table 6: PMEPR comparison for MCPC of order 9 x 9

Sequence Order 9 x 9	PMEPR using Conventional MCPC signal	PMEPR using RPU algorithm
[5 9 1 7 2 4 3 6 8]	7.76	3.43
[5 6 7 8 9 1 2 3 4]	1.95	1.57
[5 9 7 1 2 3 6 8 4]	4.86	3.56

The PSLR and ISLR for the discussed signals are shown in Table 7.

Table 7: PSLR and ISLR comparison table

Signal	PSLR(dB)	ISLR(dB)
7 x 7 Conventional MCPC	-7.38	5.52
7 x 7 MCPC with RPU	-7.35	6.55
9 x 9 Conventional MCPC	-7.33	7.04
9 x 9 MCPC with RPU	-6.89	7.43

It can be seen that in both 7 x7 and 9 x 9 MCPC signals, the conventional MCPC signal has lower PSLR and ISLR values than that obtained after application of the RPU technique. This shows that the resolution degrades and follows the trend of the 5 x 5 case. The advantage of PMEPR reduction compensates this limitation.

5 Conclusion

The MCPC signal has many advantages in terms of bandwidth efficiency and pulse compression capability when compared to other radar signals which makes it more suitable for radar applications. Its only limitation is the high value of PMEPR. This paper has successfully addressed this drawback through the application of the random phase updating algorithm.

Section IV showed the application of the RPU algorithm based on Gaussian and Uniform distribution and both techniques provided favourable results. The technique was also found to be successful in reducing PMEPR for higher order MCPC signals as well. The CCDF further validates the reduction of PMEPR by portraying the power distribution about the mean.

The autocorrelation functions plotted for the complex envelopes generated using Gaussian and Uniform distribution indicate that the sidelobe levels using Gaussian distribution is lesser than that of the Uniform distribution. Though the PMEPR values obtained for a particular phase sequence is identical in both these distributions, the Gaussian distribution fares slightly better in resolving the targets due to a lower sidelobe power level.

The Random Phase Updating algorithm being an iterative approach is computationally intensive and increases design complexity of the radar system. The random nature of the procedure makes in-depth analysis of the technique difficult. However, the advantages of this technique dominate these limitations and can be considered as a successful approach to reduce PMEPR, aiding the generation of a better MCPC signal.

6 Acknowledgment

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