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FPGA Implementation of a Space Vector Pulse Width Modulation Technique for a Two-Level Inverter

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Abstract. The paper presents a design and a hardware implementation of a Space-Vector Pulse-Width Modulation (SPVPWM) IP core. The aim of this work is to benefit from the FPGA component in controlling electric drives and in power-electronic applications. Subsequently, we can expand the libraries of predefined complex functions and circuits for reuse and to speed up the design process of AC control algorithms. The SVPWM generator is fully customizable where the modulation index, carrier frequency, modulating-signal frequency and delay time (dead-time) can be set easily by the user. The proposed SVPWM generator, implemented on cyclone IV ALTERA education board associated with an experimental set-up composed of a three-phase inverter and AC load, works properly, uses a reduced number of logic elements (LE) and is well optimized to be used in open or closed-loop motion-control applications.

Keywords: Logic element, FPGA, three-phase inverter, SVPWM, variable speed.

FPGA izvedba pulzno-širinske modulacije prostorskega vektorja za dvonivojski pretvornik

V prispevku sta predstavljena načrtovanje in strojna izvedba IP-jedra generatorja pulzno-širinske modulacije prostorskega vektorja (SPVPWM) s ciljem izrabe vezja FPGA pri krmiljenju električnih pogonov in aplikacij močne elektronike. S tem razširimo knjižnice ponovno uporabnih vezij in pohitrimo proces razvoja krmilnih algoritmov. Generator SPVPWM je popolnoma prilagodljiv in omogoča nastavitev modulacijskega indeksa, nosilne frekvence, modulacijske frekvence signala in zakasnitve (mrtvih časov). Predlagani SVPWM-generator, ki je izveden na učni razvojni plošči z vezjem Cyclone IV izdelovalca Altera ter povezan na trifazni inverter in izmenično breme, deluje pravilno. Vezje zasede manjše število logičnih elementov (LE) in je dobro optimizirano za odprto- ali zaprtozančni nadzor gibanja.

1 INTRODUCTION

Adjustable speed drives (ASD) are the main components in many industrial applications that are used in converting the electrical energy to mechanical energy with a controlled speed. The ASD controller design has been significantly improved due to the development of the two-level inverter driven by a pulse- width modulation (PWM) technique. Among the existing pulse-width modulation algorithms, space- vector pulse-width modulation (SVPWM) is more attractive thanks to its inherent optimized switching that significantly reduces the power switching loss and increases the DC bus voltage utilization.

The SVPWM technique is a kind of a modulation scheme with a superior performance compared to sinus PWM and third harmonic injection PWM for the inverter-control applications. In the conventional SVPWM algorithm, it is always necessary to perform many trigonometric operations and coordinate matrix transformations to determine the sector position of the equivalent voltage space vector. These complex calculations will inevitably produce a large number of calculations, thus reducing the overall processing speed of the digital system and making the control program design more complicated, and hence, occupying more resources and taking a longer time to run. Therefore, from the practical application point of view, it is necessary to overcome the digital implementation complexity using an adequate hardware and to make the conventional SVPWM easily implementable.

Using the FPGA circuit to implement PWM strategies is proposed for the first time in [1] and it has been also used for the ac motor drives or three-phase ac-voltage control systems [2]. Many papers have reported and tried to propose optimized space-vector PWM for open and closed vector control of the AC machines driven by voltage-source inverters. The proposed implementations use a huge amount of resources due to the trigonometric functions, transformations and switching-time complex calculations in a (d-q) reference frame [3],[4],[5]. In order to save the hardware-resource utilization, a simplified strategy is proposed to generate SVPWM

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waveforms eliminating trigonometric function using bus-clamping technique in [6],[7],[8].

Another strategy based on a generalized scalar PWM approach is detailed in [9] by extracting voltage signals based on the pulse-width calculations during rotation of the reference vector instead of calculating the turn-on and turn-off times of the power switches [10],[11].

Chen *et al.* propose a technique that simplifies the region identification in determining sectors and reduces the total switching frequency of the dual inverter [12],[13].

The main contribution of this paper is implementing an efficient SVPWM on FPGA, to control two-level three- phase inverters for adjustable-speed drives. The modified SVPWM is optimized to have simple digital logic functions for sector selection and a set of arithmetic subtractions and multiplexing to calculate the switching time based on the reference voltage in the (*abc*) frame rather than using the (α,β) frame. This strategy allows the user to completely avoid the trigonometric calculation, which will eventually reduce both the calculation time and the FPGA logic element utilization compared to the implemented SVPWM in the literature. The proposed SVPWM generator is implemented on a low-cost DE0-nano Altera educational board with a cyclone IV FPGA. The achieved design is proven to work properly. The rest of the paper is organized as follows. Section 2 is devoted to the theory behind the space vector PWM. The digital hardware implementation is detailed in Section 3. Simulations and experimental results are highlighted in Section 4. Finally, in Section 5, some concluding remarks are given.

2 PRINCIPLE OF SPACE VECTOR PWM

In order to generate an AC voltage of a desired amplitude and frequency from a fixed DC bus source, the inverter switches are switched on and off using a modulating circuit shown in Fig. 1.

The output phase voltage vector $v^{T}=[v_a\ v_b\ v_c]$ of a balanced star-connected AC load fed by the voltage-source inverter is expressed by the equation below:

$$\begin{pmatrix} v_a \\ v_b \\ v_c \end{pmatrix} = \frac{1}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ -\frac{1}{2} & 1 & -\frac{1}{2} \\ -\frac{1}{2} & -\frac{1}{2} & 1 \end{bmatrix}\begin{pmatrix} S_a \\ S_b \\ S_c \end{pmatrix} U_{dc} \qquad (1)$$

where *Sp* are the upper switches states and (*p=a*, *b*, or *c*) are the phases of the inverter.

SVPWM is inherently a voltage-control scheme that uses the reference voltage space-vector to calculate the optimum switching pattern for the three-phase inverter to ensure that the desired space-vector voltage is obtained.

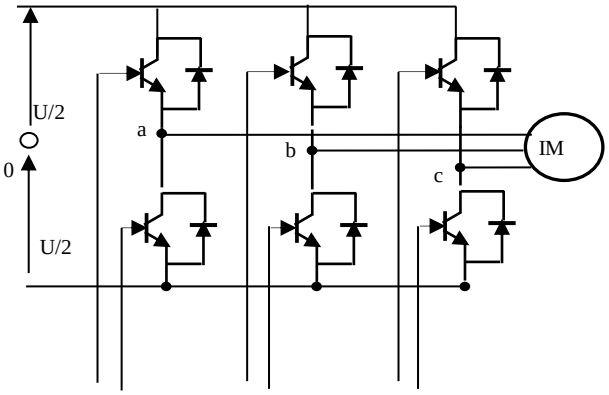

Figure 1. Two level controlled voltage source inverter.

These calculations are performed in an (*α,β*) complex plane or "space-vector" plane based on the Clarke transformation of the reference three-phase voltage $V_r^{T}=[v_a\ v_b\ v_c]$ given by:

$$V_r = \begin{pmatrix} V_{r\alpha} \\ V_{r\beta} \end{pmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ 0 & \sqrt{3} & -\sqrt{3} \end{bmatrix}\begin{pmatrix} v_a \\ v_b \\ v_c \end{pmatrix} \qquad (2)$$

According to equations (1) and (2), the eight possible switching states of the power switches will generate eight possible voltages (V_i, i=0..7) as shown in Table 1.

Table 1. The switching states and inverter output voltages

Sect	$S_a\ S_b\ S_c$	$[v_a\ \ v_b\ \ v_c]$	$[V_{i\alpha}\ \ V_{i\beta}]$	V_i
0	-1 -1 -1	$[0\ \ 0\ \ 0]U_{dc}$	$[0\ \ 0]U_{dc}$	V_0
4	1 -1 -1	$\left[\frac{2}{3}\ \ \frac{-1}{3}\ \ \frac{-1}{3}\right]U_{dc}$	$\left[\frac{2}{3}\ \ 0\right]U_{dc}$	V_1
6	1 1 -1	$\left[\frac{1}{3}\ \ \frac{1}{3}\ \ \frac{-2}{3}\right]U_{dc}$	$\left[\frac{1}{3}\ \ \frac{1}{\sqrt{3}}\right]U_{dc}$	V_2
2	-1 1 -1	$\left[\frac{-1}{3}\ \ \frac{2}{3}\ \ \frac{-1}{3}\right]U_{dc}$	$\left[\frac{-1}{3}\ \ \frac{1}{\sqrt{3}}\right]U_{dc}$	V_3
3	-1 1 1	$\left[\frac{-2}{3}\ \ \frac{1}{3}\ \ \frac{1}{3}\right]U_{dc}$	$\left[\frac{-2}{3}\ \ 0\right]U_{dc}$	V_4
1	-1 -1 1	$\left[\frac{-1}{3}\ \ \frac{-1}{3}\ \ \frac{2}{3}\right]U_{dc}$	$\left[\frac{-1}{3}\ \ \frac{-1}{\sqrt{3}}\right]U_{dc}$	V_5
5	1 -1 1	$\left[\frac{1}{3}\ \ \frac{-2}{3}\ \ \frac{1}{3}\right]U_{dc}$	$\left[\frac{1}{3}\ \ \frac{-1}{\sqrt{3}}\right]U_{dc}$	V_6

The switching states are almost similar to the "Grey Codes". To change from one state to the other, only one phase-arm changes the state. When the Clarke transformation is performed on eight inverter switching

states, it translates into six voltage vectors. e.g $|V_1|^2=|V_2|^2= |V_i|^2=⅔U_{dc}$, i=1..6 but with different angles, as well as two zero vectors V_0 and V_7 of the zero length. These space vectors are graphically shown in Fig. 2. It can be seen that the adjacent switching state transform to adjacent space vectors in a transformed two-phase (α,β) plane.

The space vector modulation (SVM) can best be explained based on a two-phase representation of Fig. 2.

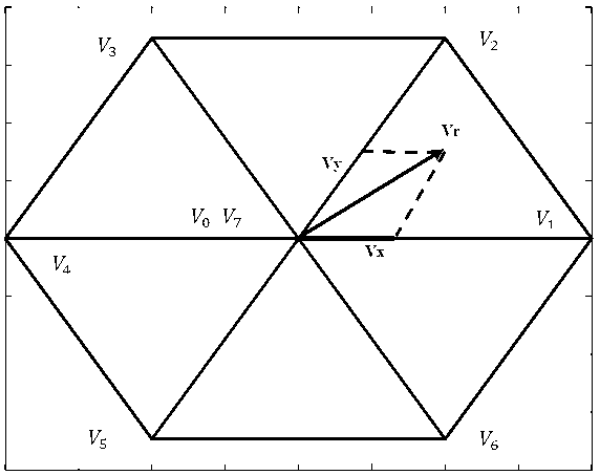

Figure 2. Principle drawing SVM for a three-phase two level-VSI.

Reference voltage V_r is to be generated by the inverter. First, it is located on one sector i (i=1,..6) defined by two adjacent active vectors V_i and V_{i+1}. Then it can be approximated based on a timely switching among (V_i, V_{i+1}) and one or two zero vectors. In this case, vector V_2 should be applied for a longer time than V_1 since V_r is nearer to V_2; and the time of the zero vectors should also be applied to reduce the magnitude.

The objective of using the space-vector PWM technique is to approximate reference voltage vector V_r using the eight switching patterns. One simple method of approximation is to generate the average output of the inverter in a small period, T_s, to be the same as that of V_r in the same period.

Usually, the switching times are derived using complex trigonometric calculations which makes the SVPWM implementation inefficient and takes more resources from the digital hardware [4],[5].

The SVPWM controller is designed to drive the inverter to generate desired voltage V_r by projecting the instantaneous transformed voltage in a sector (x) defined by two adjacent vectors (V_x , V_y) expressed during modulation period T_s as:

$$T_s = V_x T_x + V_y T_y + V_z T_z \qquad (3)$$

where T_x and T_y are the on-times of adjacent non-zero vectors V_x, V_y. They are calculated based on projections of two adjacent vectors of an appropriate sector among the six sectors using equations below:

$$\begin{pmatrix} V_{r\alpha} \\ V_{r\beta} \end{pmatrix} T_s = \begin{bmatrix} V_{x\alpha} & V_{y\,\alpha} \\ V_{x\beta} & V_{y\,\beta} \end{bmatrix} \begin{pmatrix} T_i \\ T_{i+1} \end{pmatrix} \qquad (4)$$

$$\begin{pmatrix} T_i \\ T_{i+1} \end{pmatrix} = \begin{bmatrix} V_{x\alpha} & V_{y\,\alpha} \\ V_{x\beta} & V_{y\,\beta} \end{bmatrix}^{-1} \begin{pmatrix} V_{r\alpha} \\ V_{r\beta} \end{pmatrix} T_s \qquad (5)$$

and $T_z= T_s -(T_x +T_y)$ is the on-time of appropriate zero-vector V_z.

Equation (5) is usually used for a digital implementation of SVPWM in most papers in the literature either for the microcontroller or FPGA, but it is not optimal and uses more recourses and makes the algorithm more complex compared to the simpler Sine PWM. In this paper, a more intelligent implementation of SVPWM is achieved by an intelligent manipulation of equation (5).

3 DIGITAL FPGA IMPLEMENTATION OF SVPWM

Field Programmable Gate Arrays (*FPGAs*) offer many advantages in the digital implementation of controlers for power-electronic systems. Since the complexity of the SVPWM algorithm is related to a sector selection and the calculation of the switching times, which is huge relatively to reference (α,β) , our idea is to calculate switching times T_x and T_y,using the original frame (*abc*):

$$\begin{pmatrix} T_x \\ T_y \end{pmatrix} = \frac{T_s}{U_{dc}} \begin{bmatrix} V_{x\alpha} & V_{y\,\alpha} \\ V_{x\beta} & V_{y\,\beta} \end{bmatrix}^{-1} \begin{bmatrix} 2 & -1 & -1 \\ 0 & \sqrt{3} & -\sqrt{3} \end{bmatrix} \begin{pmatrix} v_a \\ v_b \\ v_c \end{pmatrix} \qquad (6)$$

Table 2 gives the conditions for the sector selection in terms of instantaneous desired reference-voltage values V_r in the (*abc*) frame. The obtained conditions can be transformed to simple logical functions in terms of the line-to-line voltages or difference comparisons ($v_{ab}=v_a-v_b$, $v_{bc}=v_b-v_c$ *and* $v_{ca}=v_c-v_a$). This reduces and simplifies enormously the calculations of the SVPWM algorithm.
A general overview of the SVPWM generator composed of a combinatory logic that determines at the same time active sector **Sec** $_i$ and the timing pattern generator with the T_x T_y T_z timing calculation is based on Figure 3 and Table 2.

Table 2. The switching conditions and times for each sector

Switching Conditions	$\begin{pmatrix} T_i \\ T_{i+1} \end{pmatrix}$
SecI (V_{100}-V_{110}) $v_a > v_b > v_c$ **100|110**	$\frac{T_s}{U_{dc}}\begin{pmatrix} v_a - v_b \\ v_b - v_c \end{pmatrix}$
Sec II (V_{110}-V_{010}) $v_b > v_a > v_c$ **010|110**	$\frac{T_s}{U_{dc}}\begin{pmatrix} v_a - v_c \\ v_b - v_a \end{pmatrix}$
Sec III (V_{010}-V_{011}) $v_b > v_c > v_a$ **010|011**	$\frac{T_s}{U_{dc}}\begin{pmatrix} v_b - v_c \\ v_c - v_a \end{pmatrix}$
Sec IV (V_{011}-V_{001}) $v_c > v_b > v_a$ **011|001**	$\frac{T_s}{U_{dc}}\begin{pmatrix} v_b - v_a \\ v_c - v_b \end{pmatrix}$
Sec V (V_{001}-V_{101}) $v_c > v_a > v_b$ **001|101**	$\frac{T_s}{U_{dc}}\begin{pmatrix} v_c - v_a \\ v_a - v_b \end{pmatrix}$
Sec VI (V_{101}-V_{100}) $v_a > v_c > v_b$ **101|100**	$\frac{T_s}{U_{dc}}\begin{pmatrix} v_c - v_b \\ v_a - v_c \end{pmatrix}$

The first column of the table gives conditions on how to determine the sector where the reference space vector is located using only line-to-line voltages . For example, if $V_b > V_c > V_a$, then sector III is selected. It can be used in generating switching patterns of the inverter as shown in Figure 3 for all the sectors (I…VI).

3.1 Sector determination and active-time calculation

The switching diagram for sector I is illustrated in Figure 3 and with the same way are attained the same switching equations for other sectors.

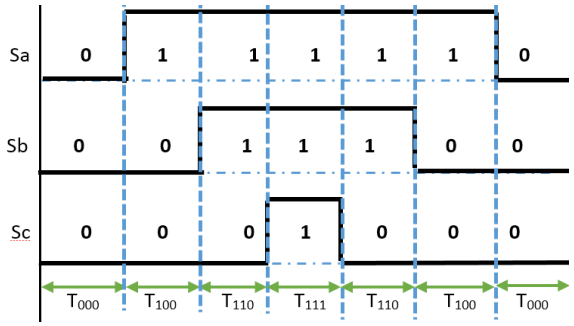

Figure 3. Switching-time pattern for Sector I.

Figure 4 illustrates the switching times calculated using Table 2 for a normalized balanced three-phase reference voltage on one period simulated using MATLAB software.

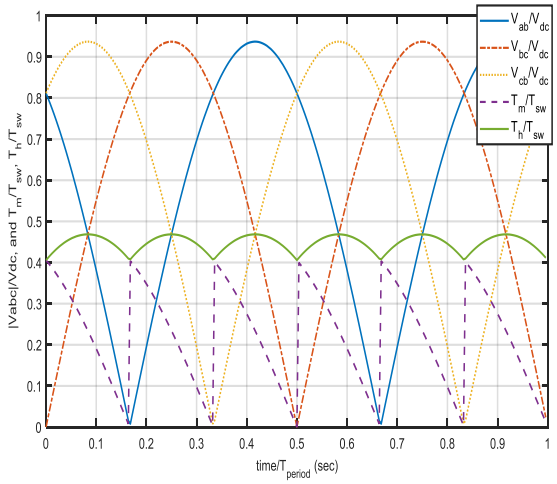

Figure 4. Switching times for Balanced three-phase pattern with a 50% modulation depth.

Figure 5 presents the digital circuit for sector selection and switching time calculation. The comparators calculating the differences $v_{pq}=v_p - v_q$ ($p=a,b$ or c and $q=b,c$ or a) give the amplitude of the difference with a sign that gives the result of the comparison, (e.g. if difference $v_{ab}=v_a - v_b$ is positive, then flag **A** is set to 1, else **A** is reset to 0), and according to Table 2, the digital logic condition for the sector selection is simplified and this in turn will save enormous FPGA resources.

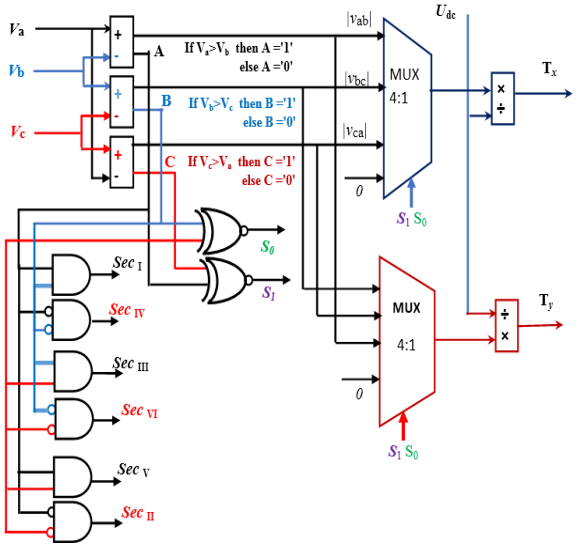

Figure 5. Sector selector and timing of the active vectors.

The differences are also used as an input to two (4:1) multiplexers to select for each sector condition the appropriate switching-on times (T_x and T_y) which simplifies the switching-times calculation to only few operations compared to other modified SVPWM algorithms which use complex trigonometric calculations.

3.2 SVPWM generator

To drive the three-phase switches, SVPWM pulses S_a , S_a and S_b are generated by a comparision with a triangle carrier signal with switching times T_l , T_h and T_z calculated in the previous stage, as showen in Figure 6.

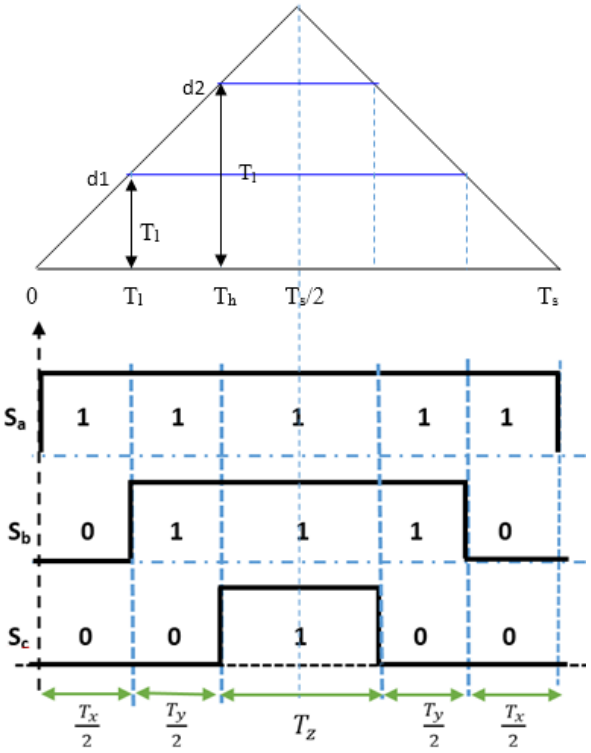

Figure 6. SVPWM digital implementation.

This switching strategy is identical for all sectors. The SVPWM generator is controlled by threshold values T_h, T_l and next signals logic and the state output is governed by the selected sector logic calculated by the data path of Figure 6.

The SVPWM threshold values required for the PWM pulse generator, $T_l = T_x/2$ and $T_h = (T_x + T_y)/2$, are calculated as follows:

$$T_l = (v_a - v_b)\frac{T_s}{2U_{dc}} \tag{7}$$

$$T_h = (v_a - v_c)\frac{T_s}{2U_{dc}} \tag{8}$$

$$T_z = T_s - 2T_h \tag{9}$$

The obtained design is optimal and uses few logical and arithmetic operations compared to the modified optimized SVPWM implementations.

4 SIMULATION AND IMPLEMENTATION

Figure 7 shows the hardware set-up constructed at our laboratory to test and validate experimentally the developed PWM techniques. The hardware used for the digital implementation is an Altera DE0-Nano board. It contains 22K logic elements Cyclone IV FPGA. The Altera Quartus software is used as a development tool (IDE) for editing, compiling, and synthesis of the hardware implemented in the VHDL language.

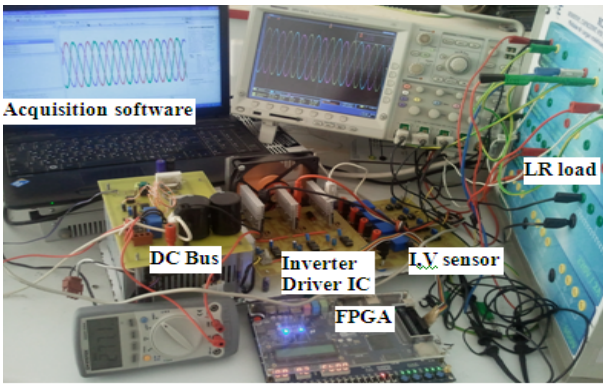

Figure 7. Experimental hardware set-up.

A general RTL synoptic schematic of the implemented optimized SVPWM modulator is shown in Figure 8.

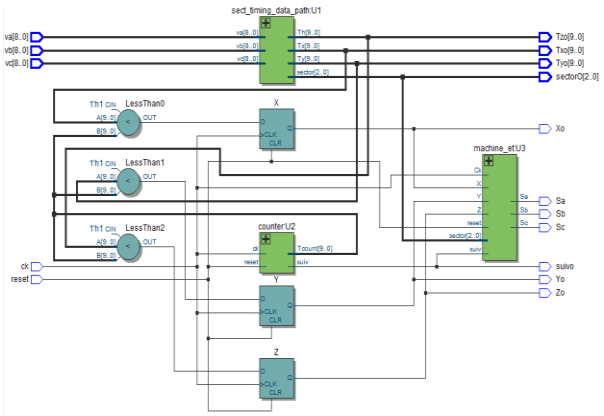

Figure 8. RTL view of the optimized SVPWM.

After a successful synthesis of the design, a report is generated by IDE which summarises, shows, and saves of the used recourses (Figure 9).

Flow Summary	
Flow Status	Successful - Sun Jan 15 16:18:55 2017
Quartus Prime Version	15.1.0 Build 185 10/21/2015 SJ Lite Edition
Revision Name	modif_SVPWM
Top-level Entity Name	mod_SVPWM
Family	Cyclone IV E
Device	EP4CE22E22C7
Timing Models	Final
Total logic elements	903
Total combinational functions	903
Dedicated logic registers	18
Total registers	18
Total pins	69
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total PLLs	0

Figure 9. Compiler flow summary of optimized SVPWM.

The simulation results, presented in Figures 10 and 11, show a functional simulation for one period of a three-phase balanced AC reference voltage.

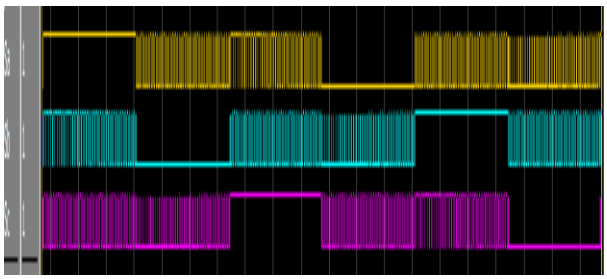

Figure 10. Global simulation results of the SVPWM generator.

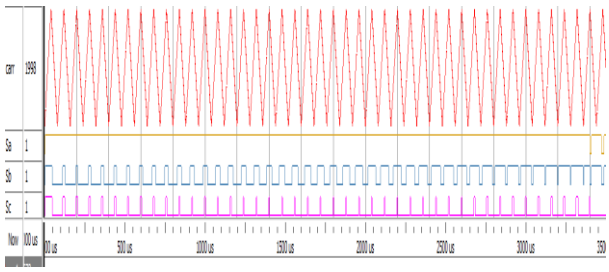

Figure 11. Generated switching for Sector I (V100-V110).

Figure 12 presentes a zoomed area of a switching period for Sector I.

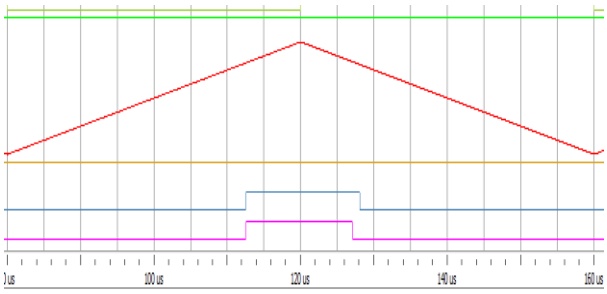

Figure 12. Zoomed area for one sample time of the SVPWM generator.

The experimental real-time SVPWM patterns generated by the FPGA board and visualised by a digital scope are highlighted in Figures 13 and 14 for Sector VI.

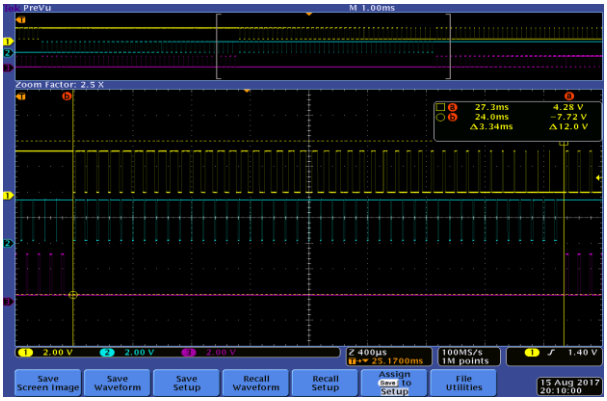

Figure 13. Generated switching pulses for Sector 6.

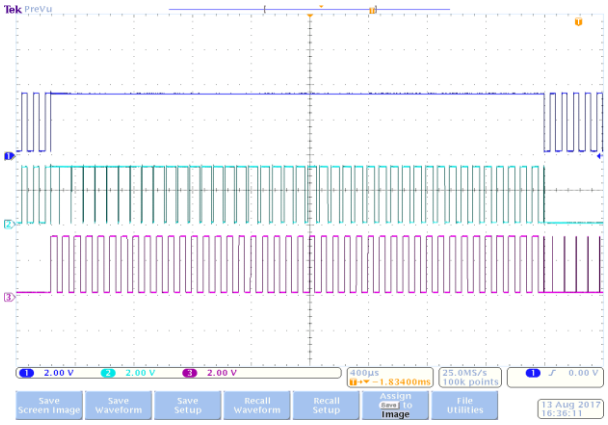

Figure 14. Zoomed results for one sector of the SVPWM generator.

A high-resolution (Hi-Res) mode in digital scope is used to filter out the difference between two phase patterns switches (Sa-Sb) shown in Figure 15. The obtained curve is a sinusoidal voltage of the reference voltage at the desired 50 Hz frequency.

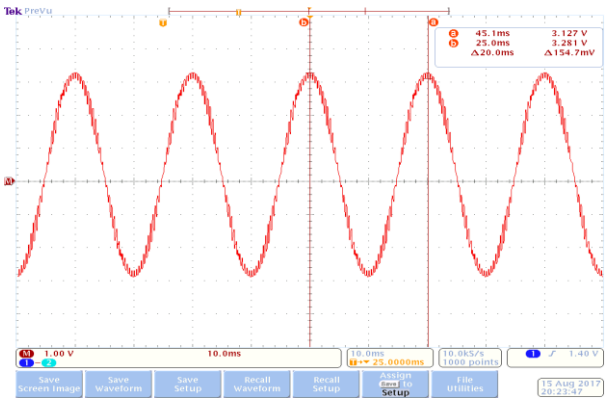

Figure 15. Experimental results of three filtered line-to-neutral output voltages (S_a-S_b).

5 CONCLUSION

This paper presented the design and implementation of an optimized SVPWM generator using FPGA. This PWM modulator can be used in many inverter control applications for AC drives. To design such module on FPGA, a novel approach is introduced in order to reduce the number of used logic elements (LEs) compared to previous designs [15], [16], [17]. The modified SVPWM is optimized so as to have simple digital logic functions for sector selection and a few sets of arithmetic subtractions and multiplexing to calculate the switching times. This strategy overcomes the trigonometric shortcomings of the conventional SVPWM algorithm. Experimental results confirm that the proposed SVPWM scheme works properly for the AC-voltage generation.

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