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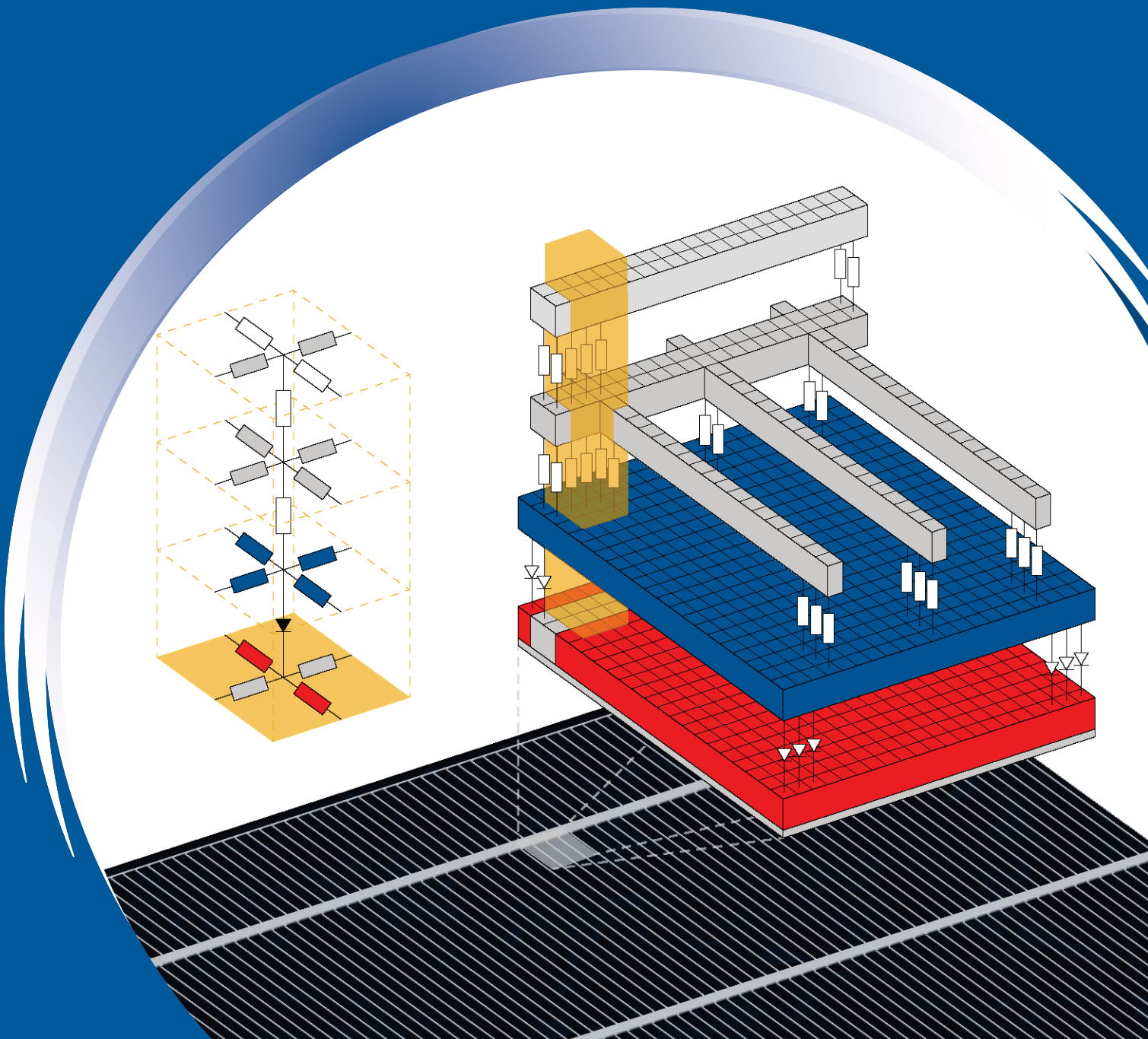

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Original scientific papers | Izvirni znanstveni članki

Editorial | Uvodnik

Dear reader,

Year 2019 ran out and this editorial brings up some statistics about manuscripts submitted in the previous year. In 2019 we received more than 110 manuscripts, out of which only 19 have been accepted for publication so far, while 22 were out of scope and 56 manuscripts were rejected. The number of manuscript submissions that are out of the journal's scope has been drastically reduced. The success rate remains below 20% in 2019 and reflects determination for quality that will path long-term quality growth. Citation metrics with JCR IF-2018=0.476, SNIP-2018=0.265 and CiteScore-2018=0,61 is an important performance indicator. In 2019 we published 26 original scientific papers and I sincerely thank all reviewers and Editorial Board Members for their valuable contribution to the journal.

Year 2019 was also a milestone year for our journal. On 25 Sep 2019 our journal was accepted to the growing DOAJ family of open-access journals (Informacije MIDEM – Journal of Microelectronics, Electronic Components and Materials). Next to a digital object identifier (DOI) to all papers, the papers are accessible from WoS, Scopus or DOAJ by a single mouse click. We sincerely hope that the open-access papers will help us in wider dissemination and larger readeship.

This issue marks another milestone. We have been publishing our journal for half of a century and it is my great honor and privilege to express gratitude to all, who served as editors, reviewers and authors of Informacije MIDEM – Journal of Microelectronics, Electronic Components and Materials in 49 volumes so far. Certainly, with this editorial we are starting the 50th volume and the 50th year of continuous publishing. As a part of your success in science and engineering we commit ourselves to continue serving you and look forward to receiving your future manuscript(s) on our submission page (http://ojs.midem-drustvo.si/).

Last but not least, do not let the covid-19 pandemic harm joy and peace in each home, office or research laboratory. Stay safe and healthy!

Prof. Marko Topič
Editor-in-Chief

31 March 2020

Original scientific paper
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A 0.35μm Low-Noise Stable Charge Sensitive Amplifier for Silicon Detectors Applications

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Abstract: The Charge Sensitive Amplifier (CSA) is the key module of the front-end electronics of various types of Silicon detectors and most radiation detection systems. High gain, stability, and low input noise are the major concerns of a typical CSA circuit in order to achieve amplified susceptible input charge (current) for further processing. To design such a low-noise, stable, and low power dissipation solution, a CSA is required to be realized in a complementary metal-oxide-semiconductor (CMOS) technology with a compact design. This research reports a low-noise highly stabile CSA design for Silicon detectors applications, which has been designed and validated in TSMC 0.35 um CMOS process. In a typical CSA design, the detector capacitance and the input transistor's width are the dominant parameters for achieving low noise performance. Therefore, the Equivalent Noise Charge (ENC) with respect to those parameters has been optimized, for a range of detector capacitance from 0.2 pF – 2 pF. However, the parallel noise of the feedback was removed by adopting a voltage-controlled NMOS resistor, which in turn helped to achieve high stability of the circuit. The simulation results provided a baseline gain of 9.92 mV/fC and show that ENC was found to be 42.5 e–with 3.72 e–/pF noise slope. The Corner frequency exhibited by the CSA is 1.023 GHz and the output magnitude was controlled at -56.8 dB; it dissipates 0.23 mW with a single voltage supply of 3.3 V with an active die area of 0.0049 mm^2.

Keywords: CMOS; CSA; Front-End; Low- noise; Silicon detector

Nizkošumen stabilen ojačevalnik za silicijeve detektorje

Izvleček: Na naboj občutljiv ojačevalnik (Charge Sensitive Amplifier - CSA) je osnovni del vhodne elektronike različnih silicijevih senzorjev in večine sistemov detekcije sevanja. Veliko ojačenje, stabilnost in nizek šum so glavne zahteve tipičnih CSA vezij za doseganje zadovoljivega ojačenja naboja (toka) za nadaljnje procesiranje. Za razvoj nizko šumne, stabilne rešitve z nizko porabo mora biti CSA realiziran v kompaktni CMOS tehnologiji. V delu predstavljamo nizko šumen, stabilen CSA za silicijev detektor, ki je bil preverjen v TSMC 0.35 um CMOS tehnologiji. V tipičnem CSA sta kapacitiven detektor in vhodna širina tranzistorja glavna parametra za doseganje nizkega šuma. Ekvivalenten šumni naboj ej bil optimiran za detektiranja kapacitivnosti v razponu od 0.2 pF – 2 pF. Paralelni šum povratne vezave je bil odstranjen z napetostno krmiljenim uporom, ki je pripomogel tudi k stabilnosti vezja. Simulacije so pokazale ojačenje 9.92 mV/fC in ENC 42. 5 e– z naklonom 3.72 e–/pF. Vogalna frekvenca CSA je 1.023 GHz, in kontroliranim izhodnim signalom pri -56.8 dB. Poraba moči je 0.23 mW pri 3.3 V napajanju in aktivni površini 0.0049 mm^2.

Ključne besede: CMOS; CSA; vhod; nizek šum; silicijev detektor

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1 Introduction

The Modern Front-End Electronics (FEE) for High Energy Physics Experiment (HEPE) are mixed-signal circuits in which the ultimate performance is set by the analog circuit applied to Solid State Detectors. The X-Rays-Sensors interaction produces a very small current and has to be amplified in a low noise circuit before any further signal processing either on-chip or off-chip with digital techniques. In multi-detector systems, multiple channels create several complications. In order to limit the power dissipation-noise problem, the sensor should be placed adjacent to the front-end amplifier. However, this results in decreased detector resolution because of heat transfer. Moreover, the process technology utilized for designing a preamplifier determines the overall size and price of the silicon-based detector systems. When a soft X-rays strikes a semiconductor detector, charges are generated. Various types of X-ray detectors including Silicon PIN Detectors, Silicon Drift Detectors (SDDs), Silicon Strip Detector (SSD), etc. have been extensively used in order to quantify the energy and photon count of incident X-rays. This type of detectors designed with a thick Si substrate is very useful for 2-D tracking in a high multiplicity environment because of the large charge collection area along with low anode capacitance [1]. Through going X-rays, create electron-hole pairs in the depletion zone of the detector and these charges drift towards the electrodes as illustrated in Fig.1. This drift (current) creates the signal (voltage) which is very weak and must be amplified by a CSA connected to each strip.

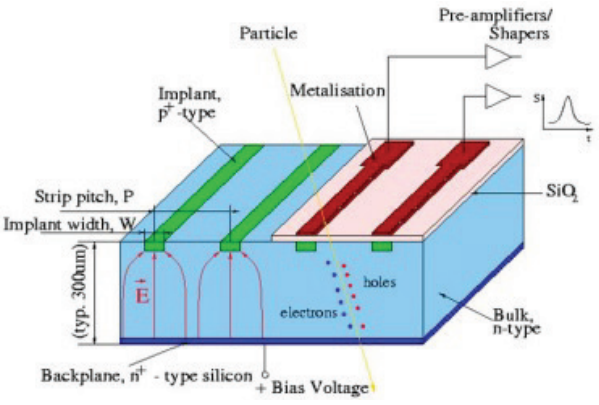

Figure 1: Principle of operation of a silicon strip detector [2].

From the signals on the individual CSA, the amplitude of the output voltage is realized. That voltage depends on the energy of the incident particles and must be measured with the highest accuracy and precision [3]. The input node voltage of the CSA increases and the voltage with the opposite polarity is generated at the output terminal simultaneously. Hence, the output potential through feedback loop forces the input potential of the CSA to become zero because of high open-loop gain as evident from Fig.2. The total amount of the current pulses is integrated on the feedback capacitor and the corresponding output is a step voltage pulse [3, 4] as described in equation (1).

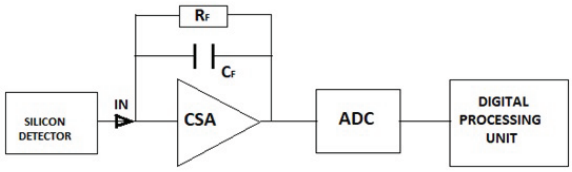

Figure 2: Silicon detector readout architecture for digital processing, the CSA is used for extracting the charge at each strip and convert it into voltage.

$$V_{CSA}(t) = \frac{1}{C_f}\int_0^T i_e(t)\,dt + V_0 \quad (1)$$

Where, VCSA(t) is the output voltage of the CSA at the time t, $i_e(t)$ is the input current injected in the detector, T is the integration period, C_f the feedback capacitor and V_0 is the offset voltage of the circuit.

As the input signals intercepted by CSA are generally very low. For a given signal source, the CSA noise performance depends on the noise created within the amplifier itself and the signal impedance seen by the amplifier input. Therefore, the CSA input stage must ensure that optimum noise matching is obtained for the given source impedance. The choice of the design parameters of the input stage of CSA influences the noise matching. So the total equivalent input noise should be kept as small as possible for a given detector capacitance up to 2pF. The main problem in the design of nuclear spectroscopy Very Large Scale Integration (VLSI) readout front ends is the implementation of low-noise; low power Charge Sensitive Amplifier (CSA). The selection of the process (CMOS or BiCMOS) determines the performance and generally the noise-related design methodology. A VLSI preamplifier costs much less than a hybrid one or a preamplifier unit [5]. CMOS exhibits several advantages over other concurrent technologies and and is preferred in VLSI circuit design [6-7]. A very popular approach in designing the VLSI CSA is the usage of an operational amplifier (Op-amp), with the R-C feedback network. Since Cdet (the detector parasitic capacitance) is quite large, about 15pF, the stability becomes a critical issue in that design [8]. For a complete validation of the CSA with CMOS technology, the overall system specifications are needed [8, 9]. In [10] H. Wang et al, proposed a CSA based Polyvinylidene Fluoride (PVDF) transducers. The circuit

works for low power dissipation and low frequency; but it iss prone to low conversion gain, high feedback capacitance that occupies more die area. A. Baschirotto et al [11], designed a CSA using a single-ended amplifier. The circuit works at high frequency and very low voltage; however, the disadvantages of that circuit are high power consumption and high Equivalent Noise Charge (ENC); furthermore, the circuit was prone to the parallel noise generated by the feedback resistor. The single-ended amplifier is a good architecture despite it is prone to both process variations and signal degradation. Indeed, the current mirrors, which generate the bias voltage for proper operation of the amplifier, contribute the common-mode noise. Thus, increasing the size of the input transistor of such an amplifier does not improve noise performance because of the bias current limitation [4]. Therefore, it is necessary to propose an optimal circuit to avoid unnecessary power dissipation and heat in closely packed pixel arrays. Secondly, the ENC should be optimized with respect to detector capacitance and the input transistor width, by performing AC and transient analysis.

In this article, a low-noise CSA designed in 0.35 µm CMOS technology process is proposed. The circuit consists of a single-ended gain block and a feedback network. The CSA bandwidth is compromised by a large detector capacitance. In order to compensate this, a common-source (CS) input design is adopted to isolate the capacitance, preventing it from affecting the bandwidth. Furthermore, CS topology is linear and power-efficient [12]. The feedback resistor stabilizes the gain-bandwidth product of the circuit. The resistor is an NMOS transistor operating as a voltage-controlled resistor; it also reduces the parallel noise contribution. The proposed circuit works with a low-energy capacitive silicon detector for X-ray detection applications.

2 Materials and methods

The CSA has been designed for a 0.35 µm TSMC process, to perform the initial conversion of current pulses into voltage pulses. Table 1 below presents the design specifications of a CSA circuit for Silicon-PIN detector applications.

Table 1: CSA specifications required for silicon detector for two vendors.

Vendor Parameters	Hamamatsu (H4083)	Amptek (A250)
Power consumption	150 mW@12V	14 mW@6 V
Count rate	2.6 MHz	2.5MHz
Detector capacitance	0 – 25 pF	0 – 250 pF
ENC (Cin = 5pF)	240 e-	76 e-
Noise slope	4 e-/pF	11.5 e-/pF
Sensitivity	22 mV/MeV (Si)	176 mV/MeV (Si)

In order to increase the gain of the CSA, we choose a three-stage configuration for the design. The single-ended configuration of the circuit in Fig. 3, is preferred to the differential one for the reduction of power consumption. The choice of the N-channel input transistor relies on the lower thermal noise compared to the P-type at high frequency, since the 1/f noise is negligible in the frequency region after 10 kHz [13, 14]; in addition, N-channel MOS, gives a lower series white noise with respect to the P-channel counterpart, because of its higher transconductance [13]. The current source at M1's drain is provided by M2, a P-channel MOSFET with smaller transconductance.

The second stage is the Miller stage. In this stage, the transistors M3 and M4 are connected in cascade whereas the transistor M5 forms the current mirror. Such a stage in the CSA incorporates a higher output resistance. The maximum signal swing must be kept limited so that all the transistors remain in the saturation region of operation, i.e., VGS> VT and VDS> VGS-VT [13]. Therefore, the bias current of M3 is kept at a specific low value (12.5 uA) in order to keep its output impedance high. Capacitor Cm provides a gain and the dominant pole in that stage; so, resistor Rm suppresses direct transmission through Cm at high frequencies.

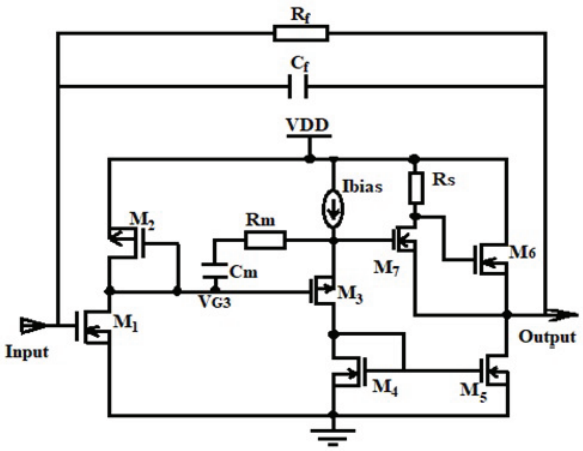

Figure 3: Schematic of the proposed structure of the CSA.

The third stage consists of an N-channel MOSFET M7 which results in a negative gain of the entire circuit so that one can apply the negative feedback. It is biased by a low current through RS. The value of Rs is set to

300 Ω so that M7 operates in the saturation region. Feedback from Vout is connected to one of the two inputs through an on-chip feedback capacitor up to 20 pF and a resistor of 30 MΩ at the top-level design. The circuit was designed with thick oxide transistors that allow a relatively high supply voltage of 3.3 V in a standard 0.35 µm CMOS technology process.

2.1 Analysis of the CSA circuit

The first stage is a cascade topology based on a common source amplifier so that the input is free from parasitic capacitance and the feedback amplifier controls the gate voltage. Therefore, the CSA input becomes a virtual ground and the detector capacitance is less significant to the CSA bandwidth.

The drains of M1 and M2 are common. When M1 is in the saturation region, we have the equation bellow:

$$V_{G3} = |V_{THP2}| + |(V_{in} - V_{THN1})| \sqrt{\frac{\mu_n}{\mu_p}\left(\frac{W_1}{L_1}\right)\left(\frac{L_2}{W_2}\right)} \quad (2)$$

When M1 enters in the triode region, the following equation (2) holds

$$\mu_n\left(\frac{W_1}{L_1}\right)\left[2\left(V_{in} - V_{THN1}\right)V_{G3} - {V_{G3}}^2\right] = \mu_p\left(\frac{W_2}{L_2}\right)\left(V_{G3} - V_{THP2}\right)^2 \quad (3)$$

with this topology, the dopants are not concentrated near the surface, so their effect is less than expected. Therefore, the voltage at the gates of M2 and M3 should depend on Rm and the reference current of M2.

In the second stage of CSA circuit, transistor M3 is in the saturation region and its drain-source current is defined by the formula:

$$I_x = \frac{1}{2} C_{ox}\mu_p\left(\frac{W_3}{L_3}\right)\left(V_{G3} - V_{THP3}\right)^2 \quad (4)$$

Transistor M3 remains in the saturation region until the device enters the triode region where

$$V_{G3} = V_{THP3} + \sqrt{\frac{2I_{bias} + 2V_{THP3}/R_m}{C_{ox}\mu_p\left(\frac{W_3}{L_3}\right)}} \quad (5)$$

As the whole circuit is designed to work in the saturation region, equations (2) and (5) involve:

$$I_{bias} = C_{ox}\mu_p\left(\frac{W_3}{L_3}\right)\left[V_{THP2} - V_{THP3} + \left|\left(V_{in} - V_{THN1}\right)\right|\sqrt{\frac{\mu_n}{\mu_p}\left(\frac{L_2}{W_2}\right)}\right]^2 - \frac{V_{THP3}}{R_m} \quad (6)$$

The biasing current helps to deplete a larger portion of the substrate and the p-well. That current depends on both the geometric and threshold voltage of transistors M1, M2 and M3. Those parameters are influenced by the mismatch of the circuit. At threshold voltage of the transistor, the instantaneous current flowing from source to drain gets a sudden boost and the additional gate voltage rise causes an exponential increase of the current. The threshold voltage of a transistor is not constant and depends on physical, electrical, and environmental factors. It has two parts: ΔV_{TH0} that is supposed to be persistent for a given technology, device, etc. [15] and ΔV_{TH} that depends on operational parameters. The V_{TH} can be expressed in the equation (6) as

$$V_{TH} = V_{TH0} + \Delta V_{TH} \quad (7)$$

Assuming V_{TH0} constant for each transistor and ΔV_{TH} identical for each type of transistor, the final expression of Ibias can be expressed as follows:

$$I_{bias} = C_{ox}\mu_n\left(\frac{W_1 \times W_3}{L_3 \times W_2}\right)\left(V_{GS1} - V_{THN0} - \Delta V_{THN0}\right)^2 - \frac{V_{THP0}}{R_m} - \frac{\Delta V_{THP}}{R_m} \quad (8)$$

Fluctuations in ΔVTH occur mainly because of temperature and voltage variations which initiate effects such as Drain Induced Barrier Lowering (DIBL), short channel effects, narrow width effect, back bias dependent threshold shift, hot carrier effect, etc. So, the biasing current as a function of the threshold voltage was computed for the limited amount of current for the circuit [15] [16].

2.1 Noise optimization of the CSA circuit

One of the primary objectives of a typical CSA design is the minimization of the ENC and this necessitates a precise input stage design. In general, the noise associated with the drain current of the input device is the vital part of the ultra-low-noise design, [17]. Past research on ENC noise minimization in the CSA focused on the geometric characteristics (W and L) or the transconductance (gm) of the input transistor. However, the leakage current is a crucial parameter of the detector which seriously affects the resolution and reliability of the detector. It is related to many factors, such as the quality of silicon, process flow, temperature, etc. which is difficult to accurately express by analytical formula. Gate-controlled diodes have been frequently used to characterize leakage current components and extract minority carrier lifetime [16] [24]. Some detailed leakage current analyses with gate-controlled diodes have been performed in regular thickness wafer for a radiation detector [16]. This research, presents the ENC as a function of the detector capacitor and the feedback for a fixed value of W and L, according to the adopted

CMOS process. The leakage current is 10nA. The different contributions are evaluated as follows:

The most prominent thermal noise contribution can be calculated as:

$$ENC_{th}^{\ 2} = 4K_B Tn\gamma\alpha_n \frac{\left(C_{\det} + C_f + C_g\right)^2}{g_m C_g} \frac{N_{th}}{\tau_p} \quad (9)$$

In which KB is the Boltzmann constant, T is the room temperature, η is the body factor, γ is the inversion factor, αn the excess noise factor, Nth is the shaper noise index for the thermal noise, τp is the peaking time, Cdet the detector capacitance, Cf the feedback capacitance, Cg the gate capacitance and gm the input MOSFET transconductance.

The flicker noise or the noise due to 1/f is expressed as:

$$ENC_f^{\ 2} = K_f \frac{\left(C_{\det} + C_f + C_g\right)^2}{C_g} N_f \quad (10)$$

Where Kf is the flicker noise coefficient and Nf the shaper noise index for flicker noise. Considering the fact that, $g_m = \sqrt{2\mu \frac{C_g I_D}{L^2}}$ with Cg = Cox WL [12], equations (9) and (10) are respectively written as:

$$ENC_{th}^{\ 2} = 4K_B Tn\gamma\alpha_n \frac{\left(C_{\det} + C_f + C_{ox}WL\right)^2 L}{\sqrt{2\mu I_D}\left(C_{ox}WL\right)^{\frac{3}{2}}} \frac{N_{th}}{\tau_p} \quad (11)$$

$$ENC_f^{\ 2} = K_f \frac{\left(C_{\det} + C_f + C_{ox}WL\right)^2}{C_{ox}WL} N_f \quad (12)$$

The white parallel noise contribution to the MOSFET gate current due to the detector leakage current, can be written as:

$$ENC_i^{\ 2} = 2qI_{leak} N_i \tau_p \quad (13)$$

Where, Ileak is the leakage current associated with shot noise, and Ni is the shaper noise index for the shot noise. This term doesn't depends on W and ID.

Different components of the ENC were optimized with respect W and ID first, and the with respect to Cg. A first-order (n = 1) shaper has been used. Therefore the thermal noise is optimal if

$$\frac{\partial ENC_{th}^2}{\partial W} = 0 \quad (14)$$

Equation (14) is satisfied. The solution of that equation (14) is Wth = ((Cdet + Cf)/3CoxL), where, Wth = 42 µm for Cdet=Cf = 0.2 pF. Similarly, the flicker noise is optimal when equation (15) is satisfied.

$$\frac{\partial ENC_f^2}{\partial W} = 0 \quad (15)$$

The solution of that equation (15) is: Wf= 3 Wth with (Wf=126 µm).

The ENC as a function of ID and W is computed for both the thermal and the flicker noise. In this study, the lowest width (Wth= 42 µm) has been considered for achieving a minimal thermal noise contribution. The flicker (1/f) noise of the drain current of the preamplifier is associated with the input transistor. This is because of the generation and recombination of carriers in the two depleted regions from impurity atoms and lattice defects [16]. The instability of the drain current (ID) is established by the variation of charge in the depletion region, which constitutes the channel width. Therefore, an optimal width involves an optimal drain current of 70µA. If the trapping and releasing of carriers were purely random, the noise spectrum would be uniform. The ENC of the whole CSA circuit is calculated by adding the contributions of thermal noise, flicker noise and the shot noise [14, 17, 18]. In order to make noise as small as possible, Kf is needs to be as small as possible. Its value depends on the adopted technology process as well. Therefore, the total ENC can be expressed as:

$$ENC_{total}^2 = ENC_{th}^{\ 2} + ENC_f^{\ 2} + ENC_i^{\ 2} \quad (16)$$

$$ENC_{total}^2 = 4K_f N_f (C_f + C_{\det}) + \\ + \frac{64}{3} K_B Tn\gamma\alpha_n \frac{N_{th}}{\tau_p} \frac{\sqrt{C_{\det} + C_f}}{\sqrt{6\mu_n I_D}} + 2qI_{leak} N_i \tau_p \quad (17)$$

Where, ENC_{th}, ENC_f and ENC_i are the thermal flicker and shot noise components respectively. Mostly, ENC_{th} is the dominant part of overall ENC noise. Equation (14) is computed and the ENC could be represented by the following expression.

$$ENC = 42.5e^- + 3.72e^- / pF \quad (18)$$

Input transistor capacitance, Cin, contributes to the total capacitance of the input of the preamplifier, Ctot, which affects the series white noise and the 1/f noise contribution to the total noise. If the width of the gate-channel is reduced, Cin as well as the transconductance (gm) decrease, which results in higher series white noise spectral density. In order for the transconduct-

ance to be as large as possible, a relatively large width transistor is preferred [15, 18]. Moreover, if the detector capacitance dominates over the transistor capacitance, a large Cin value results in a small noise increment. However, such a Cin can be balanced by matching it to the detector capacitance. Table 2 and Table 3 illustrate the constant parameters used for this design and the transistor sizing for the proposed CSA design.

Table 2: Main constant parameters.

Symbol	Quantity	Values
n	body factor	1.5
α_n	excess noise factor	0.93
γ	inversion factor	0.53
N_f	shaper noise index for flicker noise	3.69
N_{th}	shaper noise index the thermal noise	0.92
K_f	flicker noise coefficient	$8.5.10^{-25}C^2m^{-2}$
g_m	input transistor transconductance	614 µS

Table 3: Transistor parameters (W/L).

Transistors	W/L (µm)
M1	42/0.35
M2	0.84/0.35
M3	18/0.35
M4	18/0.35
M5	12/0.35
M6	12/0.35
M7	9/0.35

3 Results and discussions

The proposed CSA circuit performance was verified using LTspice simulator and the layout was implemented in 0.35 µm CMOS technology process from TSMC, using Electric VLSI, which is an open source tool for integrated circuit design. Fig. 4 shows the gain of the proposed CSA. It is controlled by the Ibias value for a feedback loop of Rf = 150 kΩ and Cf = 2 pF. Frequency domain analysis was performed from 1Hz to 10 GHz. The bias current is adjusted by changing the value of the external resistor allowing changing the transconductance as represented in equation (7). The gain (absolute value) varied from 40.6 dB to 53.8 dB. The highest bandwidth of the amplifier is achieved for 12.5µA bias current, and is equal to 1.023 GHz. The optimization of the bias current of the second stage is very important for stabilizing the gain-bandwidth product and maintaining signal integrity [19]. The capacitor of the detector was set to 1 pF and the parasitic capacitance of the input transistor is around 20 fF. So, total input capacitance was 1.02 pF.

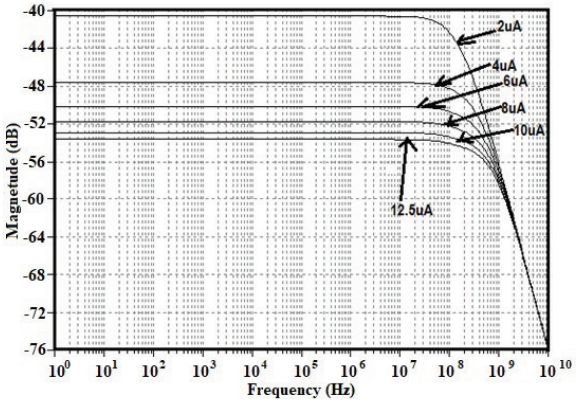

Figure 4: Influence of Ibias on the gain.

One of the most critical points in CSA is the loop gain stability, which is determined by its feedback capacitance. Nevertheless, a resistor has a parasitic capacitance and a capacitance has a parasitic resistance. Thus, an RC feedback network (Rf-Cf) models the feedback circuit. Loop-gain stability has been evaluated during the charge vs voltage conversion when Rf-Cf is bypassed [9]. The Opamp equivalent load capacitors are also taken into consideration by varying Cf. For achieving the highest stability of the circuit, the gain is adjusted by the Rf-Cf sizing. Rf was implemented by associating the drain-source resistance of a N-channel MOSFET device biased to be in the triode strong inversion region. Under this condition, the parallel noise was eliminated; the circuit is therefore stable and continuously sensitive and can be maintained in this condition without adjustment for spectroscopy purpose [10, 22, 23 and 24]. Thus, with that technique, we achieved a feedback resistance of 30 MΩ with a W/L = 25. The magnitude of the gain is therefore represented for each parameter of the feedback network. Thus, for Rf = 150 kΩ, Cf is varied from 2 pF to 20 pF. Fig.5 shows the variations of the gain for different values of Cf. For frequencies lower than 100 kHz, the parasitic capacitance of the input transistor and the resistive feedback affect the gain of the CSA and its bandwidth. The closed loop bandwidth achieved in this topology is 459.6 MHz. The circuit is immune to those parasitic effects for frequencies greater than 100 kHz. The same analysis could be applied to Fig. 6, where a MOSFET controller resistor, sized to be 150 kΩ, substituted the resistive feedback. The gain is immune to the resistive feedback and the parasitic capacitance. These results confirm the stability of the circuit with a feedback MOSFET resistor. A bandwidth of 1.023 GHz can be achieved without compromising the stability of the circuit (with output magnitude of -56.8 dB). By adjusting Ibias as shown in

Fig. 4, the bandwidth could be increased to more than 1.9 GHz.

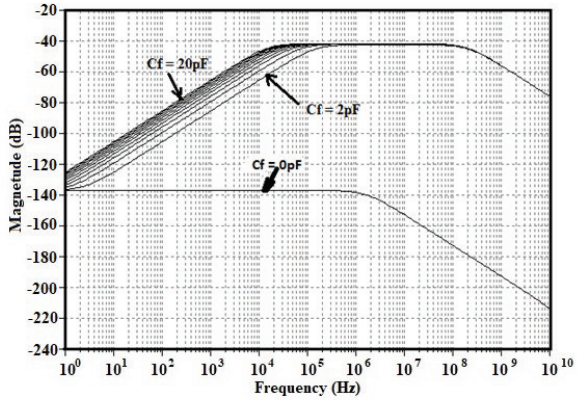

Figure 5: Influence of Cf on the gain with Rf feedback.

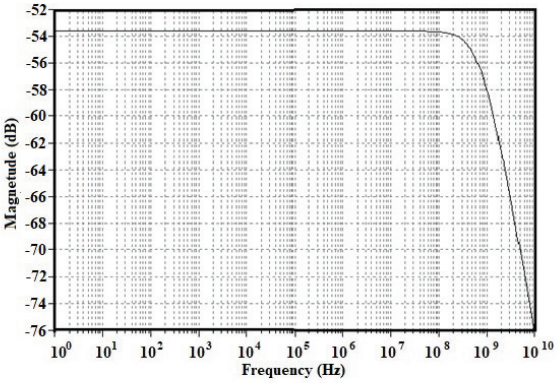

Figure 6: Influence of Cf on the gain using a MOSFET equivalent of Rf.

In Fig. 7 the Input-referred-noise (IRN) is plotted in the frequency range of 1 GHz to 10 GHz. The IRN (noise density) value extracted is 2.38 nV/√Hz. Furthermore, while designing a recording analog front-end (AFE), a lower IRN ensures the better signal quality and low power consumption will extend the lifetime of the device [19]. However, in the CSA, the parameter that embodies the noise performance is the ENC (Equivalent-Noise-Charge), namely the input charge necessary to get at the output a signal equal to noise. Its calculus was based on this intrinsic definition, neglecting the standard calculus depending on the post-CSA circuit, not present in this design [10]. Therefore, the ENC was computed and extracted based on equation (14); it presents a constant value of 42.5 e- for a detector capacitance of 0pF and noise performance increases with a slope of 3.72 e-/pF. For exhibiting the dominant component of the input noise, the ENC as a function of ID and W for the thermal component is computed in Fig. 8, and compared to the flicker noise component, which depends on W as shown in Fig. 8 and Fig. 9. In Fig. 8, when increasing the current in the input transistor, its thermal noise decreases but the bandwidth over which the thermal noise is integrated increases by the same amount; both effects cancel each other out. It can be depicted in Fig.8 and Fig .9 that the most dominant component of the ENC noise is the thermal noise component. Thus, if the device operates in a low count rate environment, substantial reductions in power consumption can be obtained with little or no noise penalty by reducing the bias current of the input transistor provided a good separation between the preamplifier rise and fall time is ensured [25].

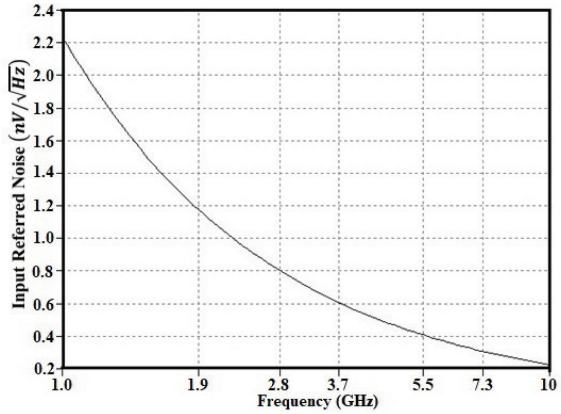

Figure 7: CSA Input-Referred Noise.

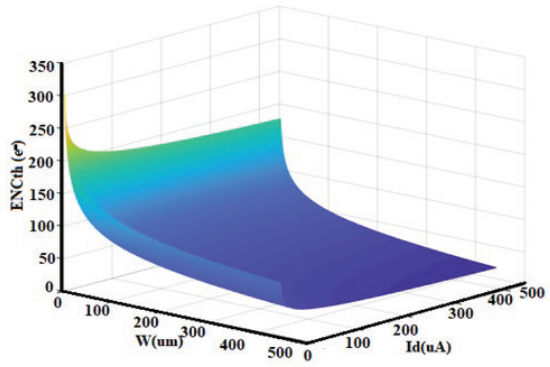

Figure 8: ENCth as a function of W and Id.

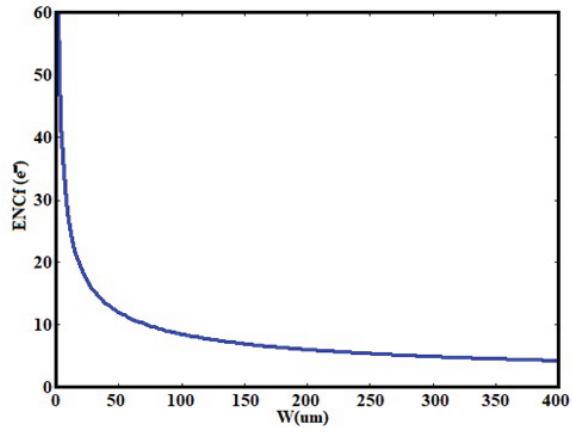

Figure 9: ENCf as a function of W.

The transient response of CSA is shown in Fig.10 and Fig.11. A current pulse with an amplitude of 33 µA and width of 1ns (206250 electrons) is injected into the detector. The output of CSA achieves a peak of 330mV and decreases thereafter because of the feedback action. For a detector capacitor of 0.2 pF, the bias current of M3 is varied and the results are shown in Fig.10. It is evident that Ibias helps to keep a lower offset and better resolution of the circuit. The same analysis is made by fixing the bias current at 12.5 µA and varying the detector capacitor from 0.2 pF to 2 pF on Fig.11. The highest amplitude (1.23 V) is obtained with 0.2 pF detector capacitance; while the highest capacitor (2 pF) generates saturation of the CSA. The output voltage is distorted and the energy information is lost which results in a circuit with low resolution. [5][26]. The fall time of the signal is about 300ns (determined by Cf and Rf).

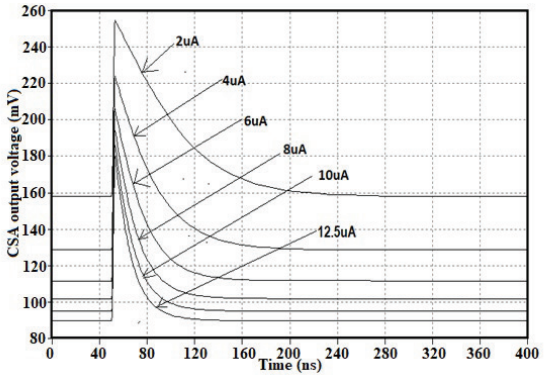

Figure 10: Ibias effect on CSA output voltage.

The amplitude of the signal charge obtained with a semiconductor detector is determined by the input particle energy such as soft X-rays and gamma rays and by the material of the semiconductor [14]. For Si-PIN diodes, the capacitance scales with area, so large area detectors exhibit more noise [21]. For SDDs, the capacitance is much lower and nearly independent of area. This noise is weakly dependent on temperature and leakage current. Since leakage current increases exponentially with temperature, reducing temperature helps dramatically [1].

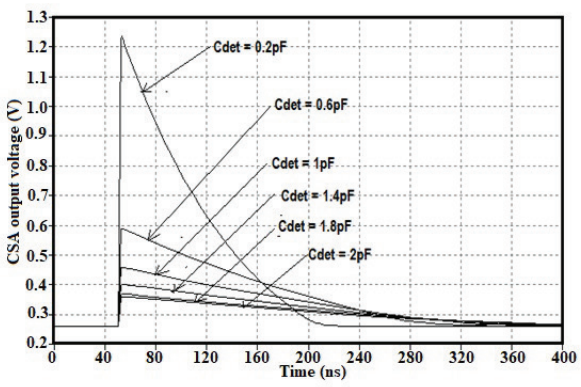

Figure 11: Cdet effect on CSA output voltage.

The total core layout area occupied by the proposed CSA is (88x55.7) µm2 as shown in Fig. 12. Parasitic extraction was used to extract the netlist with parasitic. The voltage supply is 3.3 V; the total power consumption is about 0.23 mW for the whole circuit. In this research, the gain-bandwidth product of the circuit was stabilized by means of a high-frequency feedback loop, which operates according to the voltage controlled NMOS resistor (Rf) technique [10] with resistance between 30 kΩ and 30 MΩ and a capacitance of 2 pF. The response of the circuit to different input charges results in good amplification. The gain linearity of the specific preamplifier implementation was extracted and the circuit energy response is shown on Fig. 13. The non-linearity of the CSA's gain shown on Fig. 14 (within 4.6% up to Qin=420 fC, and within 0.8% up to 300 fC) is mostly due to the second order effect of the dependence of Rf (MOSFET) on the input charge. The single MOSFET feedback network provides minimum thermal noise and high linearity, but requires baseline stabilization, and can be realized in multiple stages. [22]. The absolute value of the conversion gain is 9.92mV/fC.

Fig. 15 shows the Monte-Carlo results of the proposed circuit for 500 runs. The output signal and the histogram of the conversion gain of the circuit are shown for 10 fC injected at the input of the detector. The output signal varies from 100mV to 50 mV due to the variations of the different parameters of the circuits with the tolerance of 10%. In fact, the process variation of Ibias increases the dc-gain of the core amplifier as explained in the previous sections. The highest sensitivity of the design is then presented on Fig.15a, for a weak amount of injected charge (10fC); the circuit achieved an amplitude of 100mV. However, the histogram of conversion gain observed on Fig.15b shows a mean value of 9.79 mV/fC, and a standard deviation of 1.64 mV/fC. This indicates that the results obtained with Monte-Carlo models do not differ significantly for 500 runs and the CSA performance is quite stable and reliable.

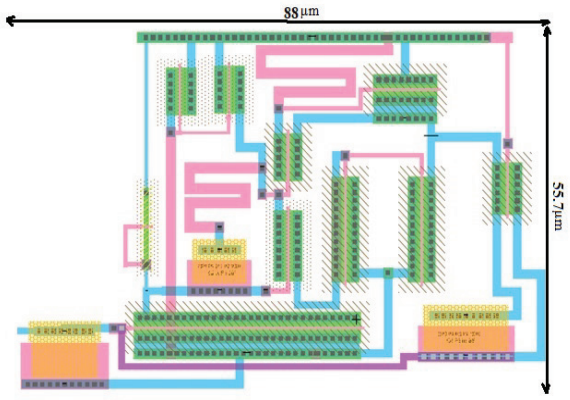

Figure 12: The core layout of the CSA circuit.

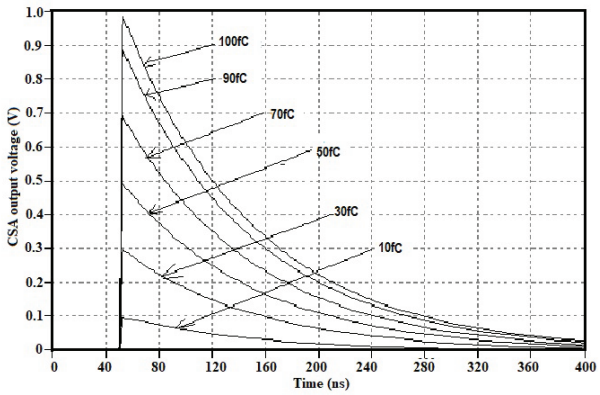

Figure 13: CSA output voltage for different input charge

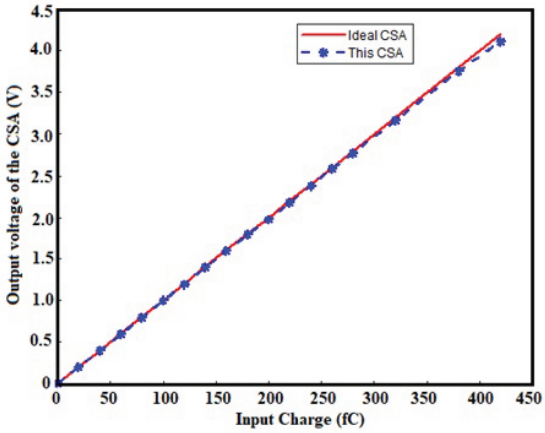

Figure 14: Output voltage vs input charge of the CSA circuit

As a summary, in Table 4 the overall features of the CSA circuit are shown. The effort in reducing power consumption, ENC and active die area of the chip comes in the parallel with similar application design present in literature [5, 8, 10, 11, 14, 21, 26]. Considering the significant difference in the input capacitance, the results are encouraging. Therefore, the preamplifier performance is in agreement with the initial specifications

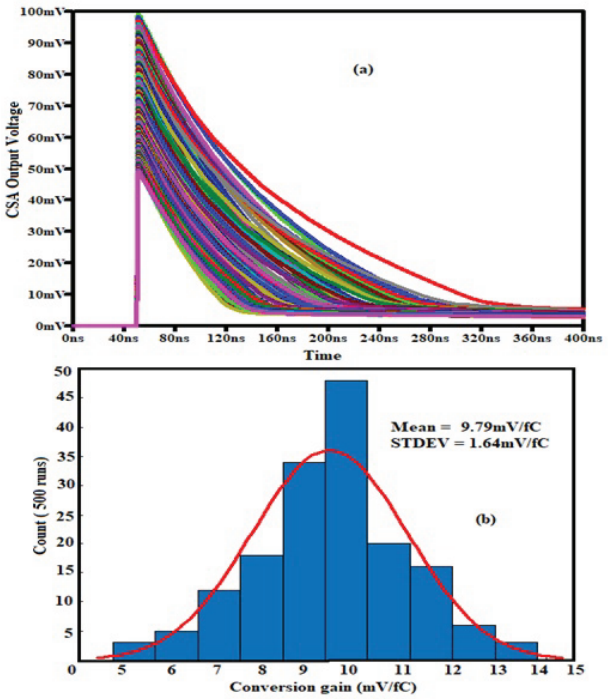

Figure 15: Post-layout Monte-Carlo simulation results (a) Output voltage (b) Conversion gain.

required. On the one hand, the design of the input and feedback transistors allowed us to achieve high linearity, wide bandwidth and sufficient low noise to ensure the good resolution of the below-threshold part of the spectrum in [26]. On the other hand, the optimization of Ibias helps to control the dc gain of the circuit and avoid saturation of the device. Operational Amplifier stability has been guaranteed with a 53.8 dB minimum dc-gain.

4 Conclusions

In this research, a 0.35 µm low-noise stable CSA circuit has been designed for Silicon detector applications.

Table 4: CSA performance summery and comparison.

Parameter	This Work	[5]	[8]	[17]	[21]	[10]
CMOS Technology	0.35 µm	0.35 µm	0.13 µm	0.13 µm	0.35 µm	0.18 µm
Power Supply	3.3 V	1.65 V	1.8 V	1.2 V	3.3 V	1.8 V
Power Consumption	0.23 mW	0.165 mW	1.1 mW	4.8 mW	--	2.1 µW
Input Parasitic Capacitance	0.2 pF – 2 pF	2 pF	15 pF	5 pF	10 pF	--
ENC	42.5 e + 3.72 e/pF	254 e- +13.5 e/pF	418 e	600 e + 100 e/pF	650 e	--
Amplifier Gain	9.92 mV/fC	2.81 mV/fC	0.5 mV/fC	10 mV/fC	15 mV/fC	0.8 µV/fC
Active area (mm^2)	0.0049	0.004212	--	0.7225	0.75	0.038
Input Dynamic Range	0– 480 fC	0 – 120 fC	--	0 – 60 fC	80 fC	150 pC – 450 pC

As per CSA, design requirements, the detector capacitance and the input stage transistor aspect ratio have been optimized in order to achieve the possible low noise and high gain performance. Moreover, adopting NMOS feedback voltage-controlled resistor technique, parallel noise that could be generated by the feedback resistance is removed which in turn ensures high stability of the design. This CSA operates at the amplification of 53.8 dB and works up to 1.023 GHz. It achieved a Charge-Voltage Conversion Factor of 9.92 mV/fC, which is compatible with the state-of-the-art. With a supply voltage of 3.3 V, it dissipates very low power of 0.23 mW. Furthermore, the proposed CSA active die area is only 0.0049 mm2. The satisfactory linearity of this circuit could be used to improve the energy resolution of X-ray radiation detection systems. The achieved results make the proposed CSA a compatible candidate for multi-channel front-end readout ASIC for Silicon detectors applications.

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6 Conflict of Interest

The authors declare no conflict of interest. Besides, the founding sponsors had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, and in the decision to publish the results.

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Back Propagation Neural Network in Predicting the Thermal Fatigue Life of Microelectronic Chips

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Abstract: The present study gives an efficient approach to predict the thermal fatigue lives of microelectronic chips under cyclic thermal load using back propagation (BP) artificial neural network method. Strain based and stress-strain based thermal fatigue life models are established, respectively, according to the experimental results of thermal fatigue tests and the singularity parameters at the failure interface calculated by finite element method (FEM). According to the existing FEM results, the BP approach is configured to predict the singularity parameters at the failure interface in the new chips once the dimensions and thermal-mechanical properties of solders are obtained. By comparison, the predicted thermal fatigue lives according to the established thermal fatigue life models are in good agreement with the experimental results. The thermal fatigue life prediction of microelectronic chips based on the BP network approach is feasible.

Keywords: thermal fatigue, microelectronic chips, BP, singularity parameters, life prediction

Nevronske mreže z vzvratnim širjenjem pri napovedovanju temičnega utrujenosti mikroelektronskega čipa

Izvleček: Članek predstavlja učinkovit način napovedovanja življenjske dobe mikroelektronskega čipa zaradi termičnega staranja pri cikličnih termičnih obremenitvah z uporabo nevronskih mrež z vzvratnim širjenjem. Vzpostavljeni so modeli termične utrujenosti glede na rezultate poskusov in izračunov parametrov singularnosti po metodi FEM. Primerjava novih in obstoječih modelov je pokazala dobro ujemanje z rezultati meritev. Napovedovanje termične utrujenosti čipov na osnovi BP mrež je mogoče.

Ključne besede: termična utrujenost; mikorelektronski čip; BP; singularnost; napovedovanje življenjske dobe

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1. Introduction

The electronics industry is mainly driven by the demand for smaller size with lower power consumption while having increased functionality and lower cost. Because of high-density and cost-effective performance, microelectronic chip has been widely used as the core component of automatic control and power converters in various industrial field [1, 2]. Exposed to the switching on-off and random fluctuations of power in the actual operation, the microelectronic chipset is often subjected to cyclic temperature loads. At the same time, the multi-layer package structure inherent in power electronics has an interface layer of a plurality of different materials inside. When the interface layer is under the action of cyclic temperature load, the irreversible plastic deformation accumulates from the interface, due to the mismatch of the coefficients of thermal expansion in different layers. When the cumulative plastic deformation reaches a critical level, the crack begins to nucleate and grow, and finally the device is permanently ineffective [3-6]. The solder layer plays an important role in the mechanical and electric connections, therefore, its performance, especially, thermo-mechanical properties, has become an important factor affecting the whole reliability of the microelectronic chips. Generally, the strength and failure properties joints are dominated by the properties of both the solder material itself and the interface bonding [7, 8]. To obtain the

excellent interface bonding, usually the solder material needs to satisfy the following requirements: 1) proper melt temperature; 2) excellent wettability or adhesive properties; 3) enough strength for bonding. Besides, adaptation to surroundings becomes much more important from the social requirements [9, 10]. However, such requirements for the solder materials cannot give a quantitative evaluation of strength and thermal fatigue life for older joints. To give a proper estimation of strength and thermal fatigue life, numerical analysis and failure criterion (including thermal fatigue law) are necessary to obtain the parameters describing the stress or strain state and the evaluation criteria [11-13]. Since Hattori et al. [14] suggested a singularity parameter approach for the interface reliability of plastic IC packages using two stress intensity parameters that characterize the stress distribution near a bonded edge along the interface, similar methods had been widely adopted to predict the crack initiation or delamination of the microelectronic chip [15, 16]. However, such a method, strictly, is based on the concept of point failure, which may difficultly be observed by the physical experiment, and is valid only for the cases that the geometric shape of the solder joints and the loading conditions are the same with that used to build up the fatigue law [17, 18]. Meanwhile, the stress intensity factor at the edge of the interface is always dependent on the test condition, assembly geometry, mechanical property of materials and their interactions, as well as the impact of process parameters [19, 20], which leads to the result that the precise models and a large amount of calculation are necessary to obtain the stress intensity factors at the failure interfaces of different chips. Soft-computing is doubtless a good alternative for handling this complex problem as it is tolerant of imprecision and uncertainty. Up to date, various soft-computing methods, e.g. artificial neural network [21-23], and genetic programming (GP) [24, 25] have been used in the field of thermal fatigue.

In the present work, the thermal fatigue life models of microelectronic chips based on interfacial singular stress-strain fields are established. Thermal fatigue tests are carried out to obtain the thermal fatigue lives of the chips, and the three dimensional finite element thermal mechanical analysis is also conducted to get the singularity parameters at the failure interface. Therefore, the parameters in the established model are determined. Also, to save the workload of calculating singularity parameters of new chips, an attempt has been made to predict these parameters by applying the BP neural network approach and accordingly, the thermal fatigue lives of these chips can be calculated.

2. Thermal fatigue prediction model

2.1 Thermal fatigue test

Five types of chips, denoting as I-V chips, are packaged in one chipset. The working powers of I-V chips are 35.7, 33.3, 25.8, 20.0 and 14.5 w, respectively. Each chip has the same layered stacking structure, and the materials from top to bottom are, in order, silica gel, wafer (silicon), solder Pb-5Sn, Cu, solder SnAg3Cu0.5, Cu, insulate layer, and the substrate, as shown in Fig. 1. Before the thermal fatigue tests, the silica gel protector is cleaned and the chips are cut out from the chipset by a wire cutter. The cyclic temperature varies from -40 to 90 °C in the thermal fatigue test, as shown in Fig. 2. It is accomplished by the specially designed heating box inserted in a bigger low temperature container which is always kept -40 °C by the liquid nitrogen. When the chips are heated, the sliding door of the heating box is close, the embedded heating tubes work. When cooled, and the sliding door is open and the heating tubes are powered off. All the chips are put into a same heating box to undergo the cyclic temperature load.

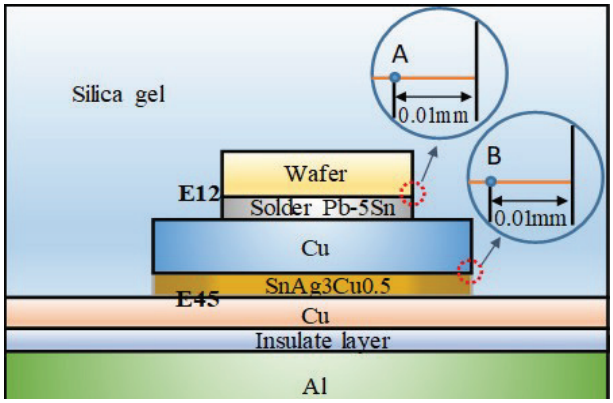

Figure 1: Structure of the chip

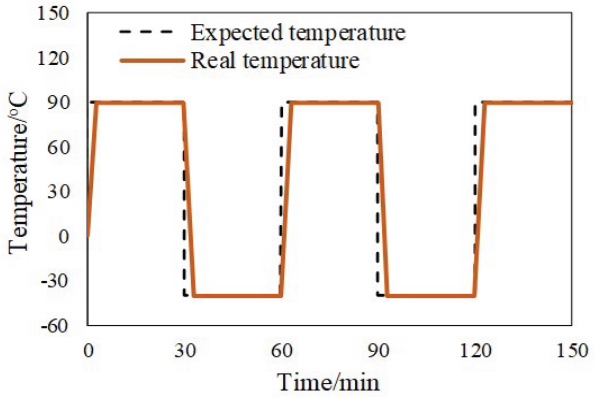

Figure 2: Ambient temperature cycles

To detect the fatigue failure, the electric resistance of the chips measured by a digital resistance meter for certain

intervals. According to the sketch of electronic resistance variation during the thermal cycles, the crack morphology of chip IV when the electronic resistance increasing (RI) reaches 10 % and 15 % are respectively observed by the JSM-6301F scanning electron microscope (SEM) (JEOL, Tokyo, Japan). The samples are covered by carbon before and the analysis is conducted under 20 kV in the SEI mode, the observed SEM images are shown in Fig. 3. It can be seen that many micro-cracks appear at the interface between the wafer and solder Sn-5Pb (E12) at 10 % RI, and the micro cracks have gradually merged into a main crack when RI reaches 15 %. While at this time micro cracks start to appear at the interface between solder SnAg3Cu0.5 and Cu (E45). The locations of the E12 and E45 have been demonstrated in Fig. 1, and the representative data points at the E12 and E45 are also selected to analyze the connection between cyclic stress-strain variations from FEM analysis to the experimental thermal fatigue cracking. It is interesting that the main crack also comes into being firstly from the E12 in the other four chips. For the convenience, we define the fatigue life limit Nf when the electronic resistance increasing reaches 15 % [26]. Fig. 4 shows the measured electronic resistance variations of each chip, and the tested fatigue life Nf is listed in Table 1.

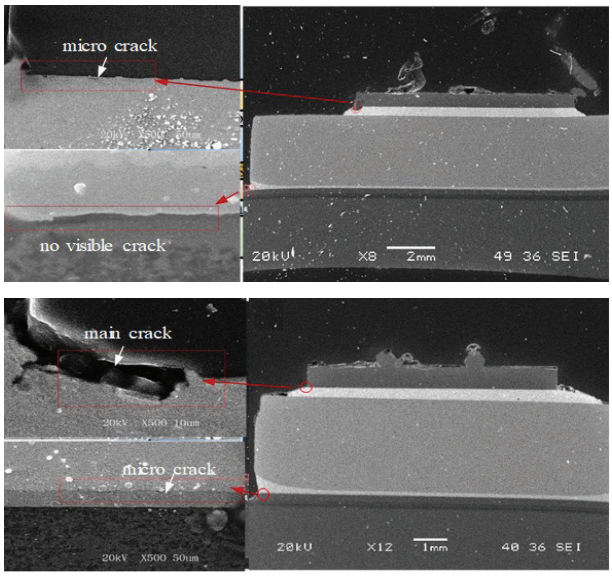

Figure 3: SEM observations of fatigue crack morphology of IV chip: (a-c) 10% RI, (d-f) 15% RI

Table 1: Fatigue life limit N_f for the tested I-V chips

Chip type	I chip	II chip	III chip	IV chip	V chip
N_f/cycles	910	830	1030	980	1040

2.2 FEM analysis

Three dimensional thermal conduction and thermal stress analysis have been carried out to obtain inter-

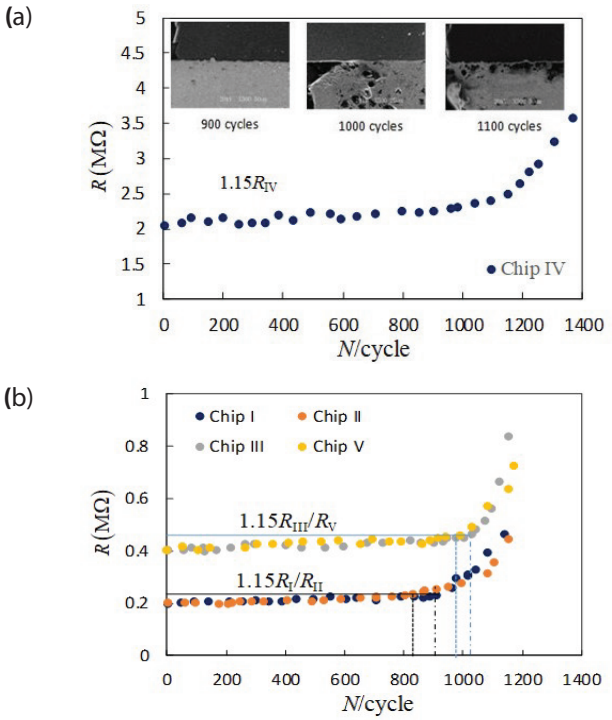

Figure 4: (a)Electronic RI with thermal cycles and (b) the corresponding thermal fatigue lives

facial stress-strain fields of the chips undergoing the cyclic thermal load. The load condition is the same as what applied in the thermal fatigue tests. Here IV chip is taken as an example to depict the general features. To obtain the accurate stress and strain distribution at the interface, FEM submodel analysis is carried out, and the boundary condition of the submodel is obtained from the former thermal conduction and stress analysis of the whole chipset by automatic interpolation, as shown in Fig. 5.

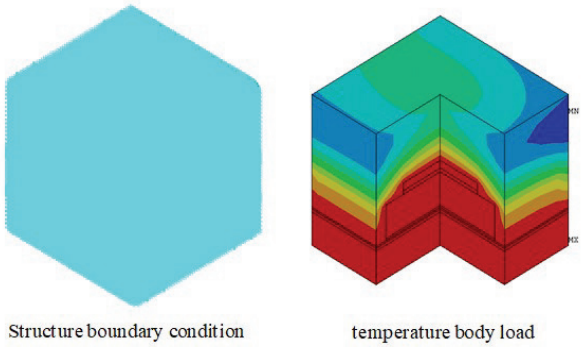

Figure 5: Boundary condition interpolation

Fig. 6 shows the stress variation at the E12 and E45 with thermal cycles, where $\sigma t=(\sigma^2+\tau^2)^{1/2}$ donates the maximum traction when the normal stress is tensile at the interface. It can be found that the E12 is under compress, while the E45 is under tension at the heating

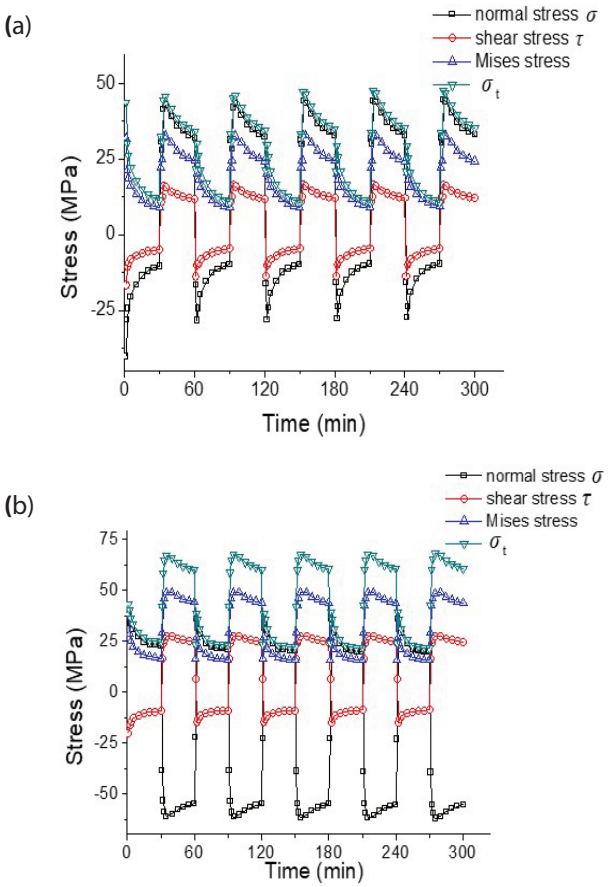

Figure 6: Stress variation near the interface edge: (a) E12; (b) E45

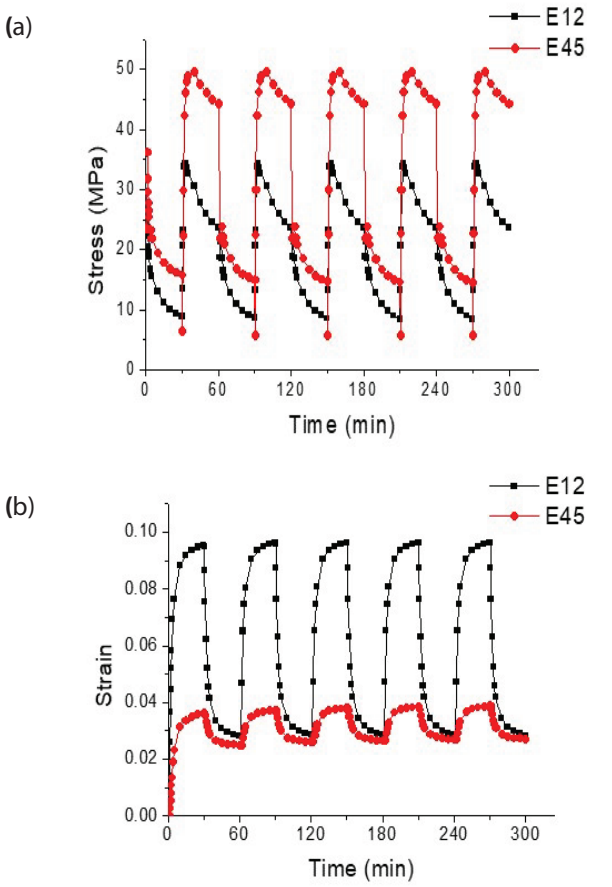

Figure 7: Comparison of E12 and E45: (a) Mises stress (b) Equivalent strain.

step. However, the opposite is true at the cooling step. There are two stress shocks, one is in the heating process and the other in the cooling process. The second shock is much stronger than the first one. The stress near the edge varies in the first several cycles, but it is saturated after 3 cycles. Fig. 7 shows the variations of Mises stress and equivalent strain at the E12 and E45. It can be seen that the stress range is severe at the E45, but the strain range is severe at the E12 since Pb5Sn is softer. Therefore, it follows that the actual fatigue failure mode is determined by the coupling stress and strain controlled mechanism.

According to the instant singular field theory [27-29],

$$\sigma_i = \frac{K_i(t)}{r^{\delta_i(t)}}, \quad \varepsilon_e = \frac{K_\varepsilon(t)}{r^{\varsigma(t)}} \tag{1}$$

where $K_i(t)$ and $K_s(t)$ denote the stress and strain intensity factors, $\delta i(t)$ and $\varsigma(t)$ are the stress and strain singular orders, i = σ, τ denotes the normal and shear stress, respectively, and r denotes the distance from the singular edge.

Picking up the stress and strain distributions at the corresponding steady states along the interface edge, the

Table 2: Singular stress field parameters at the E12 interface edge

Chip No.	Maximum stress state in the heating step				Maximum stress state in the cooling step			
	Normal Stress		Shear Stress		Normal Stress		Shear Stress	
	δ_σ	K_σ /MPa.mm$^\delta$	δ_τ	K_τ /MPa.mm$^\delta$	δ_σ	K_σ /MPa.mm$^\delta$	δ_τ	K_τ /MPa.mm$^\delta$
I	0.04119	-20.53	0.03882	-9.382	0.1551	13.59	0.04223	14.00
II	0.04305	-19.98	0.04005	-9.202	0.1524	12.99	0.04350	13.59
III	0.05363	-18.12	0.03861	-9.241	0.1627	12.55	0.04298	13.75
IV	0.04186	-19.55	0.04144	-8.939	0.1559	12.63	0.04431	13.45
V	0.05254	-17.77	0.03867	-9.134	0.1758	11.30	0.04137	13.66

Table 3: Singular stress field parameters at the E45 interface edge

Chip No.	Maximum stress state in the heating step				Maximum stress state in the cooling step			
	Normal Stress		Shear Stress		Normal Stress		Shear Stress	
	δ_σ	K_σ /MPa.mm$^\delta$	δ_τ	K_τ /MPa.mm$^\delta$	δ_σ	K_σ /MPa.mm$^\delta$	δ_τ	K_τ /MPa.mm$^\delta$
I	0.04012	27.18	0.03184	-12.87	0.01688	-53.85	0.04195	19.78
II	0.03348	28.71	0.03523	-12.14	0.01957	-52.44	0.04322	19.18
III	0.07525	21.58	0.02823	-13.35	0.07769	-35.02	0.03464	21.57
IV	0.07966	21.23	0.02806	-13.40	0.11488	-27.59	0.03080	22.52
V	0.1171	16.42	0.02805	-13.36	0.1629	-19.83	0.03049	22.53

If a unit length is taken, Eq. (3) can be simplified as

Table 4: Singular strain field parameters at the E12 and E45 interface edges

Chip No.	E12				E45			
	Maximum state		Minimum state		Maximum state		Minimum state	
	ς	K_ε / mm$^\varsigma$	ς	K_ε / mm$^\varsigma$	ς	K_ε / mm$^\varsigma$	ς	K_ε / mm$^\varsigma$
I	0.5855	2.166E-03	0.5660	9.871E-04	0.5482	1.156E-03	0.6585	1.297E-04
II	0.5829	1.853E-03	0.5768	7.819E-04	0.5647	8.242E-04	0.7642	2.398E-05
III	0.5745	1.661E-3	0.5588	7.514E-04	0.4760	2.433E-03	0.6023	2.093E-04
IV	0.5883	1.322E-03	0.5854	5.773E-04	0.4654	2.823E-03	0.6011	2.429E-04
V	0.5775	1.312E-03	0.5599	6.341E-04	0.4384	3.728E-03	0.5710	2.785E-04

stress and strain intensity factors and singular orders can be determined numerically. Applying the FEM submodel analysis to each chip, the singularity parameters as described above are summarized and listed in Tables 2-4, respectively.

2.3 Thermal fatigue models based on interfacial singularity

Thermal cycles lead to the coupled stress and strain cycles, though their peaks do not appear simultaneously, which attributes to the visco-properties of solder materials. This fact means that both stress and strain cycles contribute to thermal fatigue failures. Instead of using stress or strain as the parameters for thermal fatigue life evaluation, here the stress and strain intensity factor ranges and their corresponding singular orders are adopted to formulate the thermal fatigue law. At the interface edge, the ranges of stress and strain are written as

$$\Delta\sigma_j = \frac{K_{j\max}}{r^{\delta_{\max}}} - \frac{K_{j\min}}{r^{\delta_{\min}}}, \Delta\varepsilon = \frac{K_{\varepsilon\max}}{r^{\varsigma_{\max}}} - \frac{K_{\varepsilon\min}}{r^{\varsigma_{\max}}} \tag{2}$$

For the materials with tiny defects, the fatigue strengths and thresholds of fatigue crack propagation match those without defects. Namely, only several points with large stress in materials generally cannot affect fatigue characteristics. Therefore, using the stress-strain range within a region to describe the thermal fatigue behavior is more accurate than only by one or two points. Here the concept of characteristic length of fatigue failure is introduced, i.e., when the average stress or strain range within a characteristic length l arrives at or exceeds the fatigue limit, the thermal fatigue crack begins to initiate or propagate [30]. The average stress range $\Delta\bar{\sigma}$ within l at the interface edge can be expressed as

$$\Delta\bar{\sigma} = \frac{1}{l}\left[\int_0^l \frac{K_{\max}}{r^{\delta_{\max}}}dr - \int_0^l \frac{K_{\min}}{r^{\delta_{\min}}}dr\right] = \\ = \frac{1}{l^{\delta_{\max}}}\frac{K_{\max}}{1-\delta_{\max}} - \frac{1}{l^{\delta_{\min}}}\frac{K_{\min}}{1-\delta_{\min}} \tag{3}$$

If a unit length is taken, Eq. (3) can be simplified as

$$\Delta\bar{\sigma} = \frac{K_{\max}}{1-\delta_{\max}} - \frac{K_{\min}}{1-\delta_{\min}} \tag{4}$$

Then the range of stress and strain intensity factors can be written as

$$\Delta K_\sigma = \frac{K_{\sigma\max}}{1-\delta_{\sigma\max}} - \frac{K_{\sigma\min}}{1-\delta_{\sigma\min}}, \Delta K_\tau = \\ = \frac{K_{\tau\max}}{1-\delta_{\tau\max}} - \frac{K_{\tau\min}}{1-\delta_{\tau\min}}, \Delta K_\varepsilon = \frac{K_{\varepsilon\max}}{1-\varsigma_{\max}} - \frac{K_{\varepsilon\min}}{1-\varsigma_{\min}} \tag{5}$$

where ΔK_σ and ΔK_τ represent the multi-axes effects when both normal and shear stress are considered.

Therefore, strain-controlled and stress-strain controlled fatigue laws are respectively considered, as shown in Eqs. (6-7).

$$\left(\Delta K_{\varepsilon}\right)^{m_1} N_{\mathrm{f}} = C_{\varepsilon} \tag{6}$$

$$\left(\Delta K_{\varepsilon}\right)^{m_1}\left[\left(\Delta K_{\sigma}\right)^2 + \left(\Delta K_{\tau}\right)^2\right]^{m_2} N_{\mathrm{f}} = C_{\varepsilon\sigma} \tag{7}$$

where m_1, m_2, C_ε, and $C_{\varepsilon\sigma}$ are constants determined by test results.

By fitting the results of thermal fatigue tests and the singularity parameters at the failure interface obtained from FEM analysis, one obtains

$$\left(\Delta K_{\varepsilon}\right)^{0.4} N_{\mathrm{f}} = 87.9 \tag{8}$$

$$\left(\Delta K_{\varepsilon}\right)^{0.4}\left[\left(\Delta K_{\sigma}\right)^2 + \left(\Delta K_{\tau}\right)^2\right]^{1.74} N_{\mathrm{f}} = 3.93\times10^{7} \tag{9}$$

Theoretically, once the stress-strain intensity factors and their singular orders at the failure interfaces of new chips are obtained, their thermal fatigue lives can be predicted. However, the calculation of thermal mechanical analysis to get the singularity parameters at the failure interface is not easy and time-consuming for the engineers. Therefore, a BP neural network based method is necessary to be established for the singularity parameters to predict the thermal fatigue life.

3. BP model for thermal fatigue life prediction

3.1 Principle of BP neural network

The classic BP artificial neural network is a three or more than three layers hierarchical forward neural networks (i.e. including an input layer, an output layer, and one or more hidden layers). The algorithm consists of two parts: the forward transmission of information and the back propagation of errors. In the forward transfer process, the input information passes to the output layer through the hidden layer. If the desired output is not obtained at the output layer, the error change value of the output layer is calculated, and the network passes the error signal back along the original connection path and modifies the weight of neurons in each layer until the desired goal is reached [31]. Therefore, it is user-kind to clear these mathematical difficulties by a black box. Since the singular orders and intensity factors can be expressed in following form,

$$K, \varsigma = f\left(\text{load condition, geometry, material properties, } \cdots\right) \tag{10}$$

It is possible to estimate the singular orders and intensity factors by a trained neural network instead of FEM analysis. However, to train an efficient neural network, a huge amounts of FEM analysis results as the samples for training are necessary. That is, the user can obtain the singular orders and intensity factors of new chips simply through the well trained neural networks.

3.2 Variables in BP model

The logical route of the developed method is shown in Fig. 8. To reach the stated goal of BP network predicting the stress-strain intensity factors and their singular orders, four variables, i.e., elasticity of modulus E, thickness t and width w of solder Pb-5Sn, and cyclic temperature range ΔT, are considered and used as the parameters of the input layer of BP network. According to the different values of input variables, 60 sets of samples are prefabricated from FEM simulation, among which 50 sets are selected as training data, and the remaining 10 sets are used as test data.

3.3 Predicted results

The BP model for thermal fatigue life prediction is accomplished by the MATLAB neural network toolbox. The parameters of BP network, including the neuron number in the hidden layer, target error, learning rate are set to 13, 0.0001, and 0.35, respectively. When the testing results meet the accuracy requirement, the

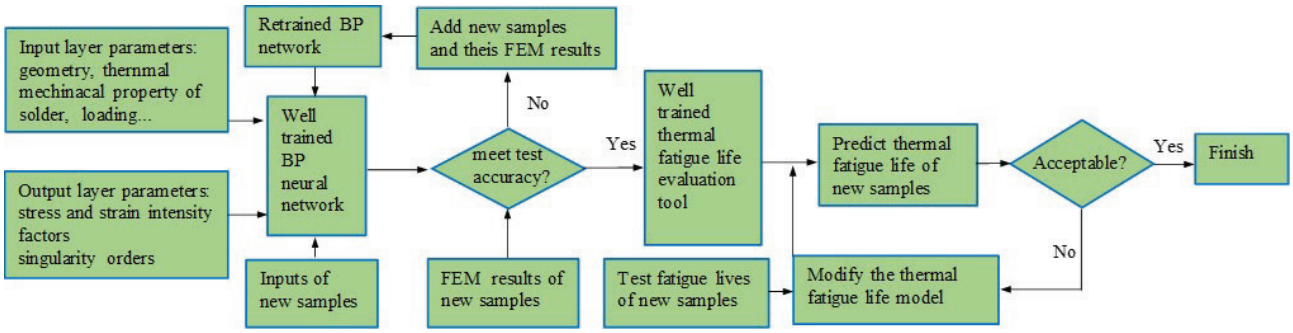

Figure 8: Logical route of developed thermal fatigue life prediction

trained BP network can be used to predict the singular orders and intensity factors in different stages. The detailed input data of the chips to be predicted are listed in Table 5, and the predicted intensity factors (Kσ, Kτ, Kε) and their corresponding singular orders (δσ, δτ, ε) of E12 at steady states are depicted in Figs. 9-11, respectively. The FEM results of these chips are also listed for comparison. The average predicting error of Kσ, Kτ, Kε and δσ, δτ, ε at the heating and cooling stages are 2.13 %, 3.32 %, 5.04 %, 2.04 %, 4.89 %, 3.67 %, 4.78 %, 1.67 %, 1.31 %, 2.87 %, 1.93 %, and 3.90 %, respectively, indicating that the trained BP neural network can predict the stress-strain intensity factors and singular orders at the failure interface with good accuracy.

When the singular parameters at the heating and cooling stage are predicted, the thermal fatigue lives of the chips can be calculated by Eqs. 8-9, as listed in Table 6. When compared with the tested results, the stress-strain controlled fatigue law can get more accurate predicting results than strain controlled one strain-controlled, indicating that the thermal fatigue failure of the chips is not just governed by strain, but by the

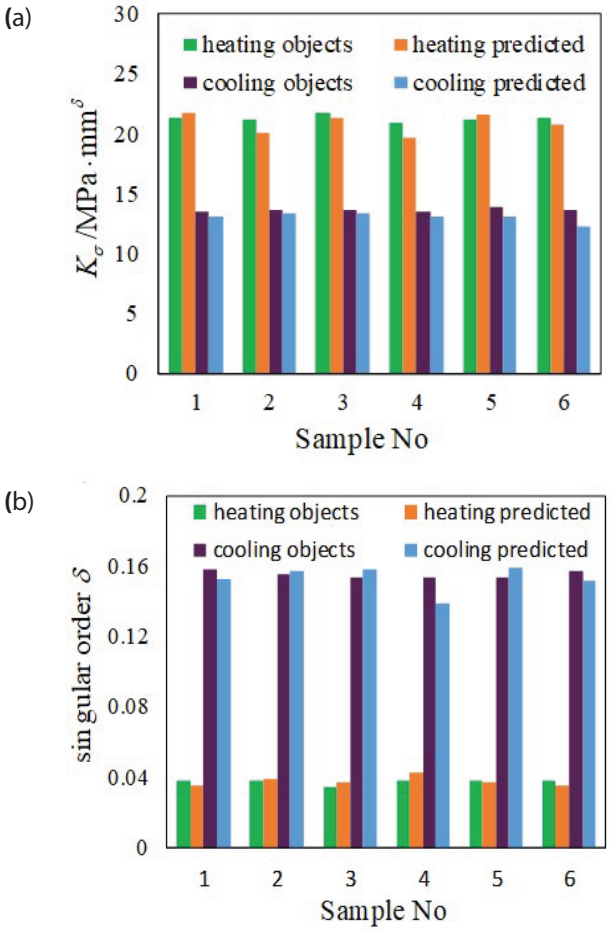

Figure 9: Predicting results of BP network for normal stress field: (a) Intensity factors, (b) Singular orders

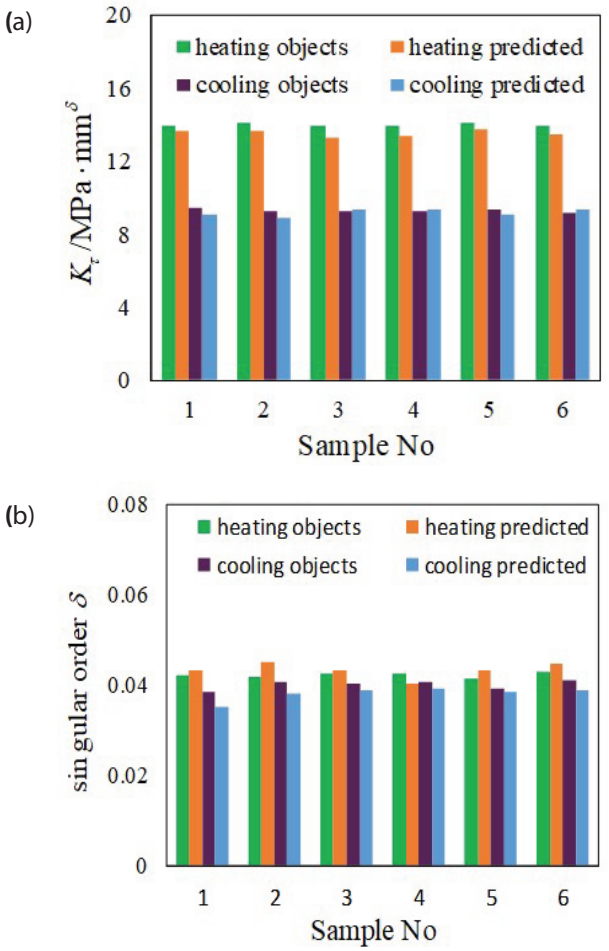

Figure 10: Predicting results of BP network for shear stress field: (a) Intensity factors, (b) Singular orders

mutual effect of interfacial stress and strain. On the whole, the differences between the predicted outputs and experimental results are quite small. The thermal fatigue life prediction method of microelectronic chips based on the BP neural network is feasible.

Table 5: Predicting inputs of BP network

Sample No.	Chip type	t /mm	w /mm	E /GPa	ΔT /°C
1	I	0.24	6.6	16.10	130
2	II	0.22	7.0	16.24	120
3	III	0.22	6.6	16.91	130
4	IV	0.22	6.8	15.62	110
5	V	0.23	6.4	16.12	130
6	II	0.21	6.6	16.58	120

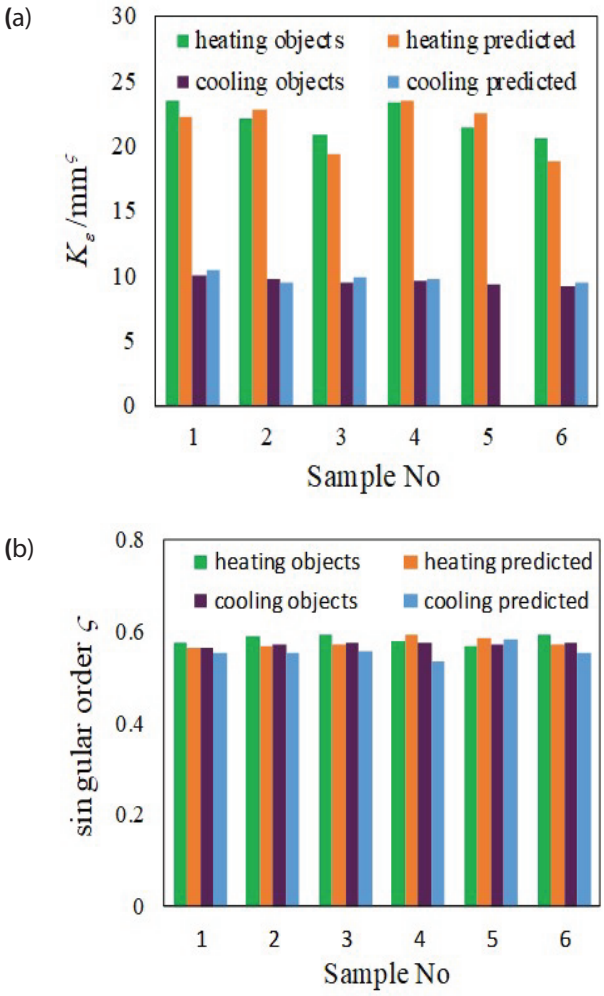

Figure 11: Predicting results of BP network for strain field: (a) Intensity factors, (b) singular orders

Table 6: Comparison of predicted and tested thermal fatigue lives of the selected chips: (a) Intensity factors, (b) singular orders

Sample No.	Chip type	Tested life / cycles	Predicted life/cycles			
			Eq. (8)	Error /%	Eq. (9)	Error /%
1	I	970	1008	3.92	983	1.65
2	II	890	951	6.85	857	3.71
3	III	1070	1014	-5.23	1090	1.87
4	IV	1060	1110	4.50	1108	1.87
5	V	1010	942	6.73	1053	4.26
6	II	950	1014	6.31	986	3.79

4 Conclusions

The present study gives an efficient approach for the thermal fatigue lives prediction of microelectronic chips under thermal cycles using the BP method. Thermal fatigue tests and FEM stress–strain singularity analysis at the failure interfaces are conducted to establish the interfacial singularity based thermal fatigue life prediction model. To save the calculation, a BP neural network model is established to predict the interfacial singularity parameters of new chips. The results show that the established BP method can effectively predict the necessary singularity parameters for thermal fatigue life evaluation. Strain-controlled and stress-strain controlled thermal fatigue models can both give reasonable prediction. The application of the thermal fatigue models demonstrates a fact that the thermal fatigue of chips can be evaluated uniformly no matter what the shapes, dimensions and the thermo-mechanical properties of the solders are, as long as the relevant stress–strain intensity factor and singular parameters at the failure interface can be obtained.

However, as the outcome of numerical analysis and experimental results, the thermal fatigue model involves several factors such as the local interfacial singularity, the diversification of singular field parameters in the FEM analysis, and the measurement of thermal fatigue life during physical experiments throughout the modeling process. Further research based on other computational intelligence approaches, like computational intelligence aided design, can be employed to predict thermal fatigue lives under different loading conditions.

5 Acknowledgements

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6 Conflict of interest statement

The authors declare no conflicts of interest.

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Optimisation of Front Metallisation Pattern in Silicon Solar Cells for Annual Energy Yield

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Abstract: With photovoltaic installations reaching into the 1 TWp range and the demand for green electric energy on the rise, every fraction of a percent of increased solar cell efficiency counts, and would result in a substantial increase in the annual energy yield of the installed photovoltaic capacities. An optimisation of the front metallic grid would provide a relatively simple yet cost-effective boost to the solar cell efficiency. We employed a freely available 2.5D photovoltaic simulator to model shading and resistive losses of the front metallisation grid, and for further optimisation of the grid for annual energy yield regarding the irradiation distribution. We were, therefore, able to increase the effective efficiency of the simulated solar cells up to 1% over the whole year depending on the location.

Keywords: Energy yield optimisation; Metallisation grid optimisation; PVMOS

Optimizacija sprednje metalizacije silicijevih sončnih celic na nivoju letnega donosa energije

Izvleček: Maksimalna skupna inštalirana vršna moč sončnih elektrarn je začela posegati v 1 TWp območje, popraševanje po čisti električni energiji pa je vedno večje, zato je dobrodošlo tudi najmanjše povečanje izkoristka sončnih celic, ki pa bi, zaradi masovne uporabe, izdatno pripomoglo k letnem izplenu energije sončnih elektrarn. Optimizacija prednje metalizacije predstavlja enostavno in poceni možnost povečanja izkoristka sončnih celic. Z uporabo 2.5D fotovotaičnega simulatorja smo modelirali izgube zaradi upornosti in senčenja prednje metalizacije in optimizirali prednjo metalizacijo za čimvečji letni izplen energije. Na tak način nam je uspelo povečati efektivni izkoristek modeliranih celic za do 1% v celem letu, odvisno od modelirane lokacije.

Ključne besede: Optimizacija energijskega izplena, Optimizacija prednje metalizacije, PVMOS

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1 Introduction

A booming market for photovoltaics (PV) has exceeded 400 GWp [1] of installed PV capacity in 2017 and the prognosis shows that it is to reach as much as 1 TWp of installed PV capacity by 2022/23 [2]. Operation at terawatt-scales gives us the ability to vastly increase the global energy production with even the smallest increase in the performance of each individual solar cell. As PV technologies are spreading to every corner of the globe, an idea of optimising solar cells to their expected operating conditions instead of standard test conditions (STC), has arisen, maximising their annual energy yield instead of promoting performance at STC, since they hardly ever occur during field operation. Since Silicon wafer based PV technologies still take up the majority of the global market [1], an optimisation of screen printed front metallisation of top contacted silicon solar cells, could lead to a vast energy yield increase with virtually no additional production costs [3].

Optimisation of front metallic grids can be approached analytically as performed by A. R. Burgers [4], and then applied to a STC or energy yield optimisation as performed by A.R. Burgers et al. [3]. But in order to be able to accurately evaluate the effects of more complex front metallisation grids, to optimise them and to optimise them with respect to arbitrary operating conditions and annual energy yield, more elaborate numerical tools need to be employed.

In our contribution we evaluate the use of PhotoVoltaic Module Simulator (PVMOS) [5] as a tool to accurately

simulate the effects of front metallisation shading and resistive losses on the maximum power point of a silicon solar cell. On that basis we will further optimise the metallisation grid at different irradiation levels, and finally try to estimate the impact on the annual energy yield. With that knowledge we will undertake the challenge of optimising a solar cell metallisation according to yearly irradiation distributions at different locations and assess the impact on estimated annual energy yield compared to STC cell optimisation.

2 Modelling

PhotoVoltaic Module Simulator (PVMOS) developed by Bart Pieters [5] is a 2.5D quasi-SPICE simulator designed to efficiently simulate photovoltaic devices. It allows for creation of an accurate device model in two dimensions and the third dimension is simulated by stacking and interconnecting 2D layers. Sheet resistances are defined for each layer, or more accurately each segment of a layer, allowing for simulation of patterned structures. The connection between planar patterned layers could either be resistive, a p-n junction (described by a one or two-diode model) or it could implement an arbitrary *J-V* characteristic. A simplified part of a 4-layer (ribbon, front metallisation, emitter, and bulk with bottom metallisation) silicon solar cell model could therefore be represented as shown in Fig. 1, where vertical resistive connections are omitted for simplicity. A detailed explanation of the PVMOS simulator is available in [6].

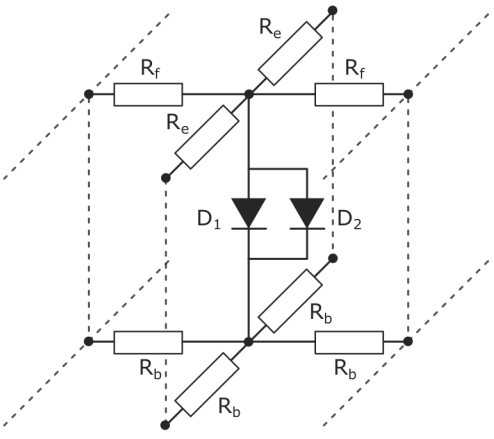

Figure 1: Simplified PVMOS model of a small section of a 3D cell

After the simulation nodal voltages and currents along all three axes become available along with the cumulative *I-V* characteristic, which allows for evaluation of the simulated structure on the device level as well as on a local, more detailed level. In this work PVMOS will be used as a tool to model shading and resistive losses of the front metallisation pattern.

We built a set of MATLAB scripts and tools around the PVMOS simulator allowing for automatic geometry generation, geometry and solar cell parameter sweeps, and energy yield estimation, since a normal simulation procedure would require more than 10 individual manual steps.

3 Results and discussion

3.1 Analysis of front metallisation losses

According to literature [7] losses associated with the front metallisation can be divided into two categories, namely shading and resistive losses, whose individual effects on the *I-V* curve are depicted in Fig. 2. One can see that shading losses mainly affect the short circuit current, while resistive losses decrease the fill-factor of the cell. In the following subchapters fractional power losses of individual origin will be evaluated through PVMOS simulations and the trends will be compared to analytical expressions from previous work. All symbols used are defined in the Appendix.

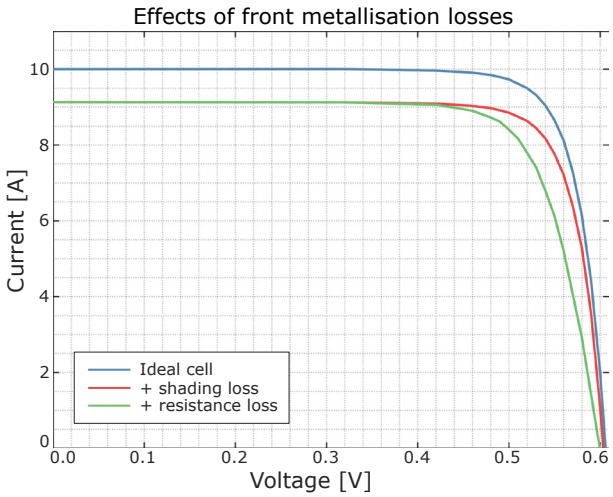

Figure 2: Effects of shading and resistive losses on an *I-V* curve.

3.1.1 Fractional power loss

Since different cell configurations are evaluated, producing a variety of power-voltage curves and therefore different maximum power points (MPP), it is necessary to employ a measure of power loss that is comparable between configurations. The measure - fractional power loss *p* [7] is defined as the ratio between lost power P_{loss} and power in the MPP P_{MPP} of an ideal, unshaded cell as shown in equation (1).

$$p = \frac{P_{loss}}{P_{MPP}} = \frac{P_{ideal} - P_{lossy}}{P_{MPP}} \quad (1)$$

3.1.2 Shading losses

Cell's self-shading losses are mainly caused by direct finger and busbar shading and are generally linearly proportional to the area of the shading elements.

Busbars

From definition [7] busbar shading losses p_{sb} are proportional to the ratio of the busbar width W_B and the spacing between them B, as it is evident from equation (2). Fig. 3 shows shading loss obtained by PVMOS simulations and as one would expect it exhibits a linear relation.

$$p_{sb} = \frac{W_B}{B} = 2\frac{W_B N_B}{W_C} \propto W_B N_B \quad (2)$$

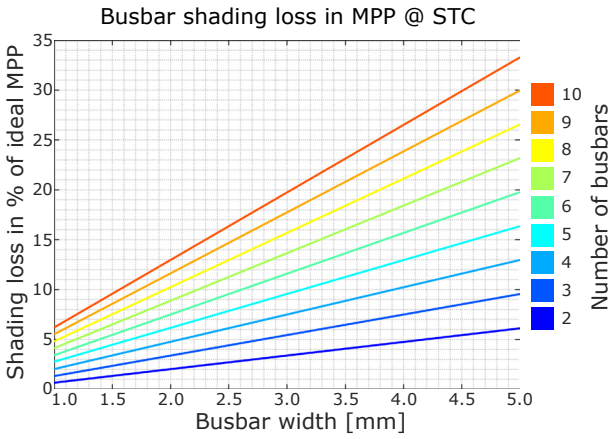

Figure 3: Busbar shading loss in correlation with the number of busbars and their width.

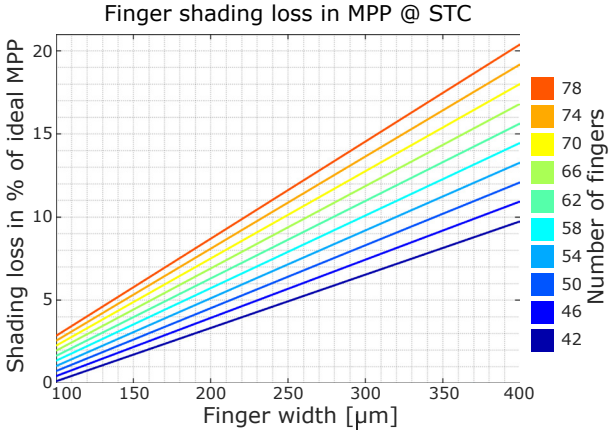

Figure 4: Finger shading loss in correlation with the number of fingers and their width.

Fingers

Finger shading losses are by definition [7] quite similar to the busbar case. The losses p_{sf} are proportional to the ratio of the finger width W_F and their spacing S. The relation is show in equation (3) and PVMOS simulation results in Fig. 4.

$$p_{sf} = \frac{W_F}{S} = 2\frac{W_F N_F}{H_C} \propto W_F N_F \quad (3)$$

3.1.3 Resistive losses

From intuition resistive losses should decrease with increasing busbar width and with an increasing number of busbars. Resistive losses p_{rb} are defined according to [7] in equation (4), where m is a factor related to tapering of the busbar (4 for linear tapering and 3 for uniform busbar width).

$$p_{rb} = \frac{1}{m} A^2 B \rho_b \frac{J_{MPP}}{V_{MPP}} \frac{1}{W_B} = \\ = \frac{1}{m} A^2 B \rho_b \frac{W_C}{2} \frac{J_{MPP}}{V_{MPP}} \frac{1}{W_B N_B} \propto \frac{1}{W_B N_B} \quad (4)$$

As we can see from Fig. 5 resistive losses do indeed decrease with increasing busbar width in a $1/x$ fashion as it is also evident from equation (4). One can also observe that a decrease in resistive losses is gradually decreasing with an increasing busbar number, which is also in accordance with equation (4).

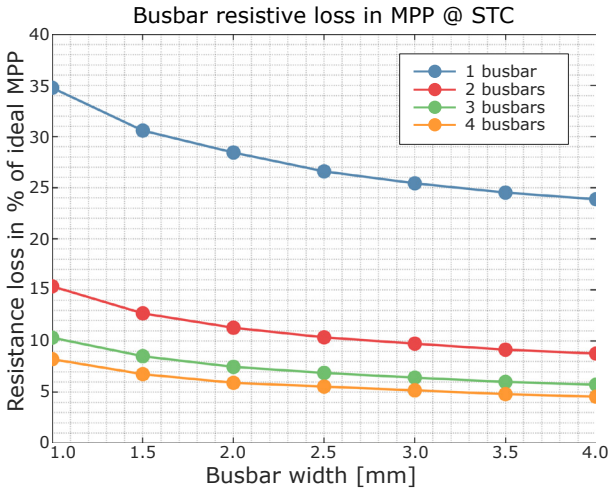

Figure 5: Busbar resistive loss in correlation the number of busbars and their width.

Fingers

Resistive losses due to finger metallisation are actually a combined effect of resistive losses in the top layer of

the p-n junction due to lateral current flow and actual resistive losses due to current flow along the fingers. Since one depends on the other we have not separated their effect because we cannot directly influence the emitter resistance with the design of the front metallisation. Combined equation for resistive losses due to front contact fingers p_{rf} [7] is therefore given in equation (5). Parameter m relates to the tapering of the fingers in the same fashion as before.

$$p_{rf} = \frac{1}{m} B^2 \rho_f \frac{J_{MPP}}{V_{MPP}} \frac{S}{W_F} + \frac{\rho_e}{12} \frac{J_{MPP}}{V_{MPP}} S^2 =$$
$$= \frac{1}{m} B^2 \rho_f \frac{H_C}{2} \frac{J_{MPP}}{V_{MPP}} \frac{1}{N_F W_F} + \frac{\rho_e H_C^2}{48} \frac{J_{MPP}}{V_{MPP}} \frac{1}{N_F^2} \propto \quad (5)$$
$$\propto K_1 \frac{1}{W_F N_F} + K_2 \frac{1}{N_F^2}$$

Given the parameters of the cell one could establish which of the two parts will prevail and determine the characteristics of the implied resistive losses. Fig. 6 gives the results of finger resistive loss obtained via PVMOS simulations. The fluctuations seen in the results are probably a consequence of an inappropriate spatial resolution causing a discrepancy between the real and the simulated finger widths. Those points would require a higher resolution for simulation but would result in longer simulation times which were out of scope for this contribution.

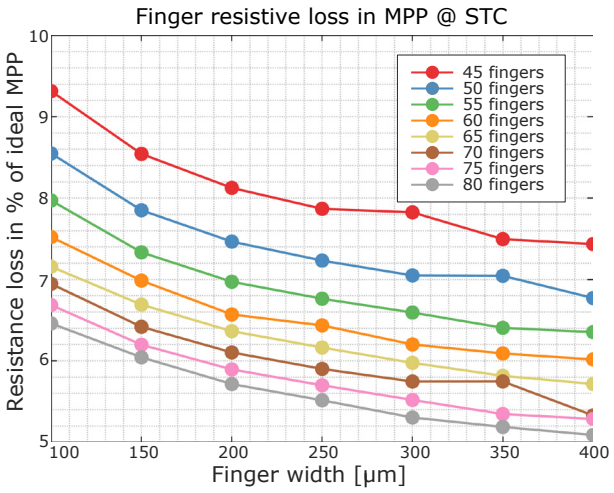

Figure 6: Finger resistive loss in correlation with the number of fingers and their width.

3.1.4 Combined loss effect

A solar cell generally exhibits a combination of the aforementioned loss effects. Their interplay is determined by the chosen metallisation geometry. It can be seen from Figs. 7 and 8 that for some chosen parameters there exists an optimal solution or combination of other free parameters minimising the loss. Figs. 7 and 8 respectively show loss change trends with different busbar and finger configurations.

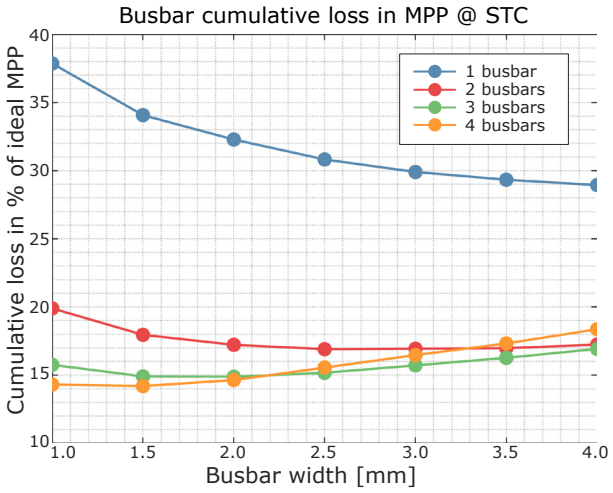

Figure 7: Influence of busbars on the cumulative losses. Number of fingers is fixed to 60 and their width to 100 µm.

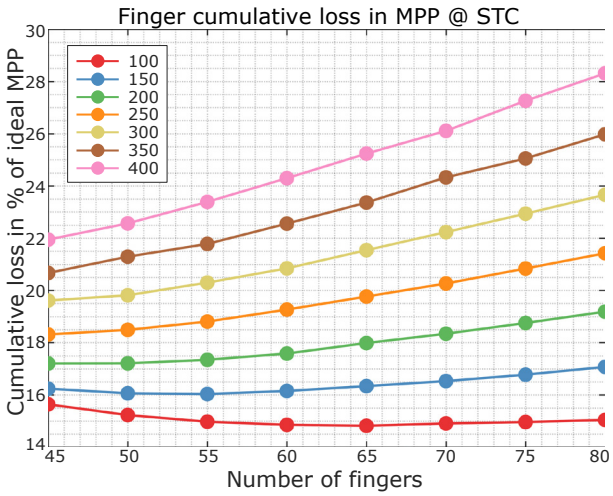

Figure 8: Influence of fingers on the cumulative losses. Number of busbars is fixed to 3 and their width to 2 mm.

3.2 Optimisation of front metallisation pattern for STC conditions

Given the results from the previous sections, one could pose a question whether there exists an optimal metallisation geometry, that reduces shading and resistance losses to a minimum. As mentioned before one can only change (given the H-grid metallisation) the metallisation pattern in terms of busbar width W_B, busbar number N_B, finger width W_F and number of fingers N_F. We could, if necessary, explore other grid patterns, finger and busbar tapering for shading loss reduction

and multilevel grid design, but in the scope of this work we have limited ourselves to the most common, basic, busbar-finger H-grid.

We chose to make a sweep of possible different configurations of number of busbars (2-6) and fingers (45-80) under STC conditions. The simulations provided us with a set of *I-V* curves from which we were able to calculate maximum power points for every configuration as shown in Fig. 9.

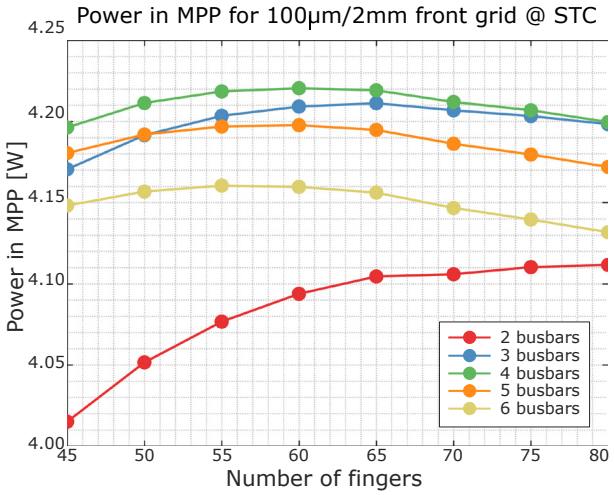

Figure 9: MPP dependence on finger and busbar number for 100 µm/2 mm configuration.

We have chosen a configuration with the highest MPP to be the optimal front metallisation grid at STC. With the chosen busbar width W_B of 2 mm and chosen finger width of 100 µm, the optimal configuration turned out to be 4/60 (busbars/fingers). Since modern technologies allow for finger widths under 100 µm we also repeated our simulations at 50 µm finger width. The results are shown in Fig. 10.

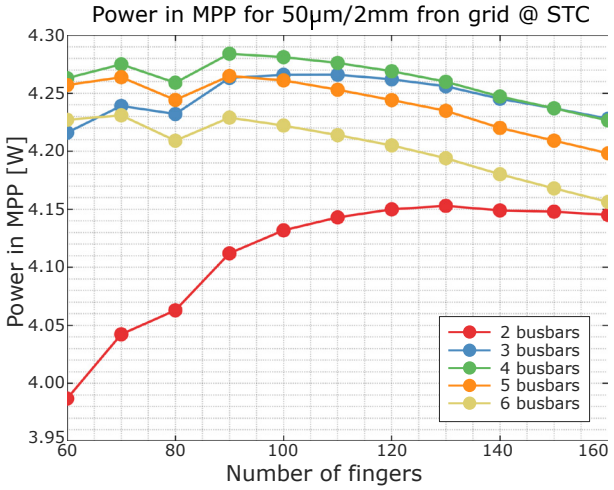

Figure 10: MPP dependence on finger and busbar number for 50 µm/2 mm configuration.

One can see, that MPP points follow the same trends as before with broader fingers. The kink at 80 fingers is due to bad resolution of the structuring image. Because of the sampling, a resolution that produced fingers exactly 50 µm wide, missed some of the fingers. Increasing the resolution by a small fraction seemed to lessen the error because all fingers were included. But with increasing resolution fingers became narrower than 50 µm, which is why we think the error is still present. An accurate result would require doubling or tripling the resolution, which we could not afford in the scope of this work. Still we could deduce that the optimum lies somewhere around 90 fingers and 4 busbars for the 50 µm fingers.

Fig. 11 shows comparison of *I-V* and power-voltage curves of both optimal 100 m/2mm and 50 µm/2mm configurations. One can observe, that the MPP of the 50 µm configuration is slightly higher mostly due to decreased shading and therefore increased short circuit current, which coincides with the fact that between the cases finger width halved while the number of fingers increased by slightly less than a factor of 2.

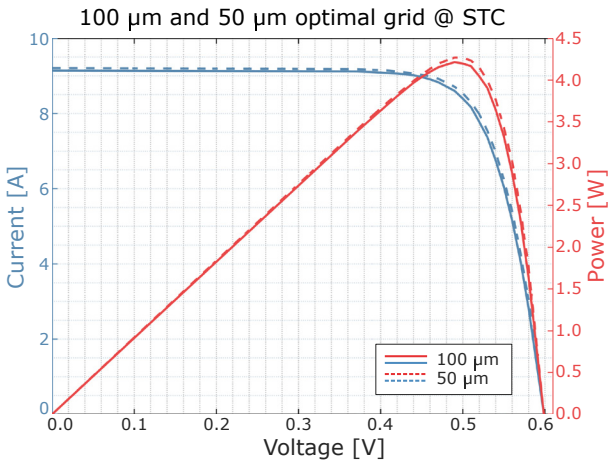

Figure 11: Difference between *I-V* and *P-V* curves for optimal 100 µm/2 mm and 50 µm/ 2mm configurations.

Because of the required high resolution for an accurate simulation of 50 µm wide fingers and consequentially long simulation times, we could not afford to optimise the energy yield with the 50 µm/2mm grid, since we could not trust the calculation of the MPP at low resolutions. We therefore chose the 100 µm/2mm grid for further calculations.

3.3 Optimisation of front metallisation for yearly energy yield

Using the same method, that we have used to optimize the front metallisation for STC, we approached optimi-

sation for yearly yield. To further reduce the number of possible simulation combinations and decrease simulation time, we have fixed the W_B to 2 mm and W_F to 100 µm in the following simulation cases. The same process could be applied to any given grid geometry.

We have chosen three inherently different places for evaluation, since yearly irradiation profiles [8] for Sahara Desert, Ljubljana and Stockholm should vary significantly. Fig. 12 shows annual irradiation (flat oriented surface, direct illumination) vs. irradiation level for all three places.

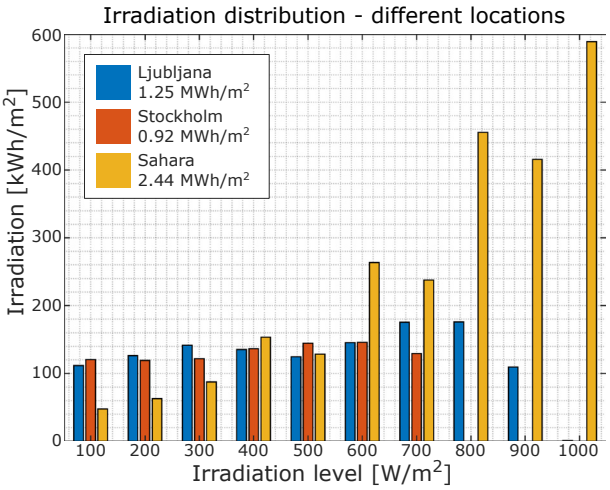

Figure 12: Annual irradiation distribution for Ljubljana, Stockholm and Sahara.

Because annual irradiation peaks lie at different irradiation levels and distinct metallisation patterns perform differently under various irradiation levels, we presumed that there exists a metallisation pattern that would maximise the annual energy yield. The optimal metallisation should favour irradiation level with highest yearly irradiation, but should also provide best all-year-round performance. With respect to that one can assume that the optimal metallisation geometry of for e.g. Sahara Desert should best match the optimal one at STC, since irradiation peak is near 1000 W/m².

We performed *I-V* curve sweeps for different number of busbars and different number of fingers, all at different irradiation levels up to 1000 W/m² in 100 W/m² steps. From a pool of simulated *I-V* curves we calculated maximum power points for each geometry and each irradiation level. With the aforementioned data we were able to estimate annual energy yields for each of the selected locations and each metallisation geometry. At each irradiation level, we took into account the efficiency of the metallisation grid and annual irradiation at the selected location, which gave us expected energy yield at each irradiation level. Summation of those partial energy yields gave us an estimate of the annual energy yield. In the end we chose a geometry, that produced the highest annual energy yield. Energy generation profiles are given in Fig. 13, 14 and 15 for each of the locations respectively. By optimising the front metallisation, we were able to increase the annual energy yield by up to approximately 1% (in the case of Stockholm), for a flat oriented surface and direct illumination.

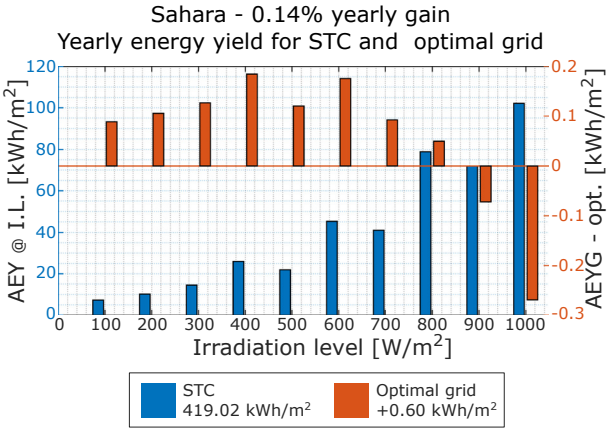

Figure 13: Sahara – Annual energy yield at different irradiation levels for STC optimal grid (blue) and annual irradiation level energy yield gains (AEYG) for an optimal grid (orange).

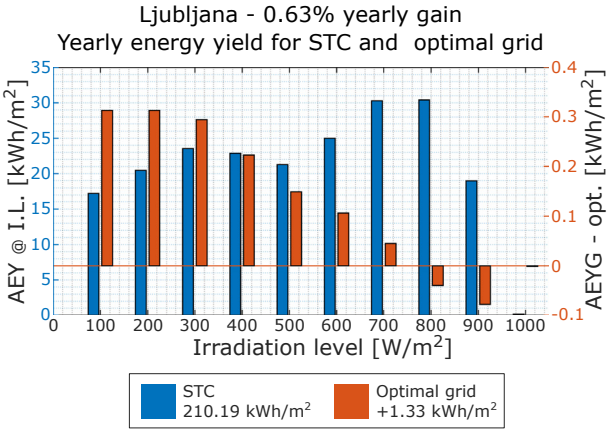

Figure 14: Ljubljana – Annual energy yield at different irradiation levels for STC optimal grid (blue) and annual irradiation level energy yield gains (AEYG) for an optimal grid (orange).

As it can be seen from Fig. 13, 14 and 15 optimal metallisation geometries allow for a performance increase over lower irradiation levels and a slight decrease at higher irradiation levels. Nevertheless, the configuration allows for a greater annual energy yield. Table 1 shows differences between optimal geometries for STC and optimal geometries for annual energy yield (AEY) and effective efficiencies.

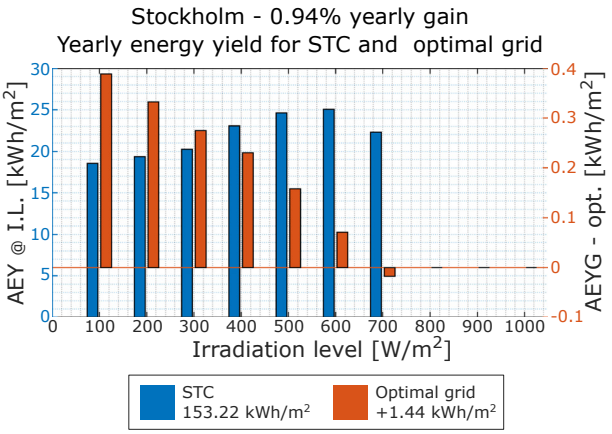

Figure 15: Stockholm – Annual energy yield at different irradiation levels for STC optimal grid (blue) and annual irradiation level energy yield gains (AEYG) for an optimal grid (orange).

If we take yearly irradiation into consideration, we can see, that places with higher annual irradiation or more precisely places with an irradiation peak at higher irradiation levels require a denser front metallisation grid for a better effective efficiency. From a theoretical point of view higher irradiation levels allow for higher optically generated currents, therefore increasing resistive losses and thus requiring front metallisation patters with lower overall resistance, resulting in a higher number of fingers. On the other hand, current densities at lower irradiation levels are substantially smaller therefore resistive losses play a less important role and front metallisation is designed in such fashion that it minimises shading loss, while still providing a low enough resistance for current collection, resulting in a lower overall number of fingers. Shown in Fig. 16 and 17 are shading and resistive losses of optimal metallisation grids for each of the locations at different irradiation levels. It is clearly shown, that higher overall irradiation calls for denser metallisation grids and therefore higher shading loss (e.g. Sahara Desert) and lower overall irradiation needs a metallisation pattern that mitigates shading loss therefore increasing resistive losses (e.g. Stockholm). Ljubljana as a place of average latitude is therefore an average between two extremes with average shading and resistive losses.

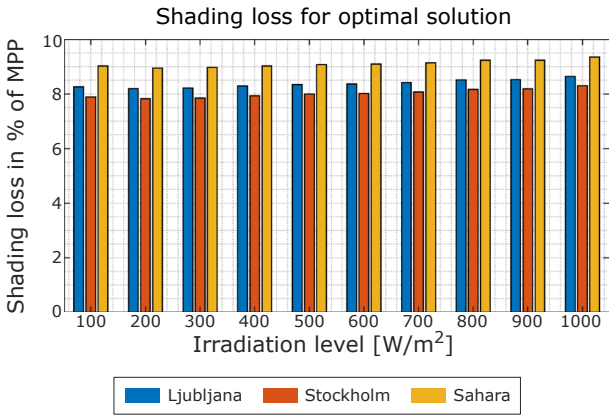

Figure 16: Shading losses at different irradiation levels for an optimal, location specific grid.

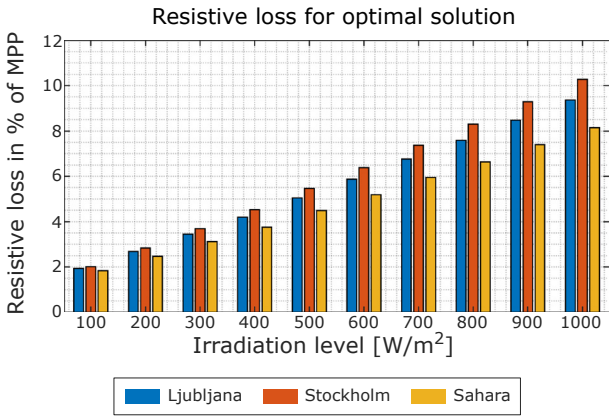

Figure 17: Resistive losses at different irradiation levels for an optimal, location specific grid.

4 Conclusion

We have evaluated the effects on losses in MPP due to front metallisation. We have established that for each irradiation level there exists an optimal busbar and finger geometry. With that in mind we have optimised metallisation patterns for either STC or annual energy yield. With the aforementioned optimisation we have achieved an annual energy yield increase of up to 1% in comparison with STC case.

Table 1: STC and annual energy yield optimised geometry parameters, their expected annual energy yields and effective efficiencies.

	Optimised for STC				Optimised for AEY			
	N_B	N_F	AEY [kWh/m²]	ηeff [%]	N_B	N_F	AEY [kWh/m²]	ηeff [%]
Sahara	4	60	419.02	17.17	3	60	419.62	17.20
Ljubljana	4	60	210.19	16.82	3	50	211.51	16.92
Stockholm	4	60	153.22	16.65	3	45	154.65	16.81

Although our study was limited to only three places, 10 irradiation levels on a horizontal plane and that we have only optimised for finger and busbar numbers, we have still established a workflow with PVMOS as a core component, for an estimation of annual energy yield and its optimisation according to the front metallisation. With an established workflow we could also extend our optimisation to busbar and finger width, more irradiation level bins or different metallisation patterns (e.g. tapered fingers and busbars, other for example "organic" metallisation topologies [9]). The model could also be expanded to include thermal modelling, irradiation at different orientations and inclination angles, and diffuse light therefore providing an extensive tool for annual energy yield estimation.

5 Acknowledgements

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6 Conflict of Interest

The authors declare no conflict of interest.
The founding sponsors had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, and in the decision to publish the results.

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8 Appendix

Symbol	Explanation
R_f	Fingers' sheet resistance
R_e	Emitter's sheet resistance
D1,2	First and second diode
R_b	Structured sheet resistance of the bulk
p	Fractional power loss
P_{loss}	Absolute power loss
P_{MPP}	Power in the MPP
P_{ideal}	Power of an ideal unshaded cell
P_{lossy}	Power of the lossy cell
p_{sb}	Fractional busbar shading power loss
p_{sf}	Fractional finger shading power loss
p_{rb}	Fractional busbar resistive power loss
p_{rf}	Fractional finger resistive power loss
W_c	Width of the cell
H_c	Height of the cell
W_B	Width of the busbars
N_B	Number of busbars
A	Same as height of the cell in this case
B	Half the spacing between busbars
W_F	Width of the fingers
N_F	Number of fingers
S	Spacing of fingers
m	Tapering factor
ρ_b	Resistance of the busbars
ρ_f	Resistance of the fingers
J_{MPP}	Current density in MPP
V_{MPP}	Voltage in MPP

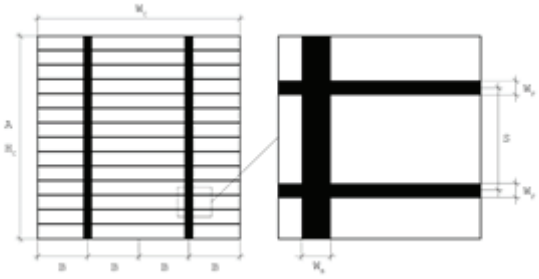

Figure: Definitions of cell's physical dimensions.

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Simple CMOS Square Wave Generator with Variable Mode Output

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Abstract: A novel square-wave generator based on a single CCCII (current controlled conveyor), with only two external grounded passive components is proposed in this paper. The circuit provides precise, electronically controllable, voltage or current output square-wave signals. The simulation results using 0.18 mm CMOS parameters and experimental verification confirm the feasibility of the proposed circuit. The proposed generator can operate very well at up to 25 MHz with nonlinearity less than 5%.

Keywords: Square-wave generator; CCCII; variable mode output; electronically controllable; simulation; experimental results.

Enostaven CMOS generator kvadratnega vala s spremenljivim izhodom

Izvleček: Predstavljen je nov generator s kvadratnim valom na osnovi enojnega CCCII (current controlled conveyor) z le dvema zunanjima pasivnima elementoma. Vezje zagodavlja natančen, elektronsko nastavljiv napeotsni ali tokovni izhodni signal kvadratne oblike. Simulacije so izvedene v 0.18 mm CMOS tehnologiji in eksperimentalno preverjene. Generator lahko dobro deluje do 25 MHz, pri čemer je njegova nelinearnost manjša od 5%.

Ključne besede: generator kvadratnega vala; CCCII; nastavljiv izhod; eelektronski nadzor; simulacije, eksperiment

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1 Introduction

Square signal generators are widely used in communication, instrumentation, electronic and control systems such as generation of the carrier signal in communications or clock signals in electronic systems, or as control signals driving synchronous motors with permanent magnets [1]. They also find their place in various other applications based on processing of analogue signals, they are used for defining the duty cycle of a voltage controlled oscillator in sensor interfaces, in the operation of A/D and D/A converters, signal processing functions, as well as the clock pulse in digital systems.

Among various current mode devices, the second generation current conveyor (CCII) is one of the most versatile building blocks [2]. It is also characterised by a high slew rate, wide bandwidth, and a large dynamics range. In CCCII function, R_x (intrinsic resistance) can be modified by varying the bias current I_B, resulting in more precise voltage-following characteristic between ports *x* and *y*, thereby allowing the design of numerous tunable applications [2].

The proposed generator possesses the following advantages: a single active element and grounded passive components-based realization; the electronically adjustable period and oscillating condition (OC); operational frequency of up to 25 MHz; and low power consumption (1mW). It can be used for the generation of rectangular waveforms and pulse width modulation waveforms, considering that many applications such as music synthesizers, voltage regulation and power delivery units need the period adjustment function in the waveform generator. Based on HSPICE simulation and experimental results, the performance of the proposed square-wave generator is shown, and the obtained results are fully in line with the conducted theoretical analysis.

2 Proposed square-wave generator circuits

The proposed variable mode square-wave generator-relaxation oscillator is shown in Fig. 1.

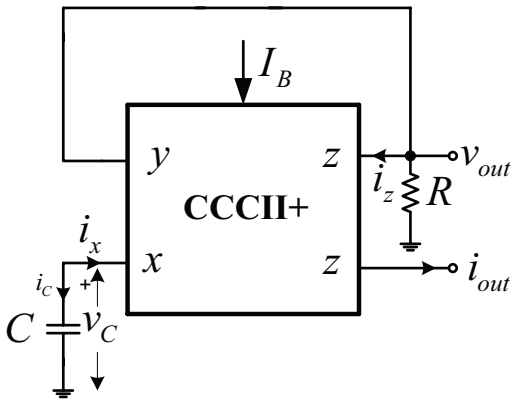

Figure 1: Variable mode square-wave generator.

Square-wave generator in Fig. 1 consists of only one active component-CCCII; capacitor and one grounded resistor (which can be electronically controlled). The circuits employ a Schmitt trigger connection with a grounded capacitor. The oscillation frequency depends strongly on the nonlinear behaviour of the CCCII and the value of the *x* terminal resistance. The terminal relationships of CCCII in an ideal situation can be described as [2]

$$i_y = 0; v_x = v_y + i_x R_x; i_z = i_x \quad (1)$$

These equations, however, represent the CCCII in the linear operating region, when current at *x* port and voltages at *z* and *x* ports are limited [3]. In fact, CCCII is a nonlinear component and outside of the linear region the currents at *x* port and the voltages at *z* and *x* ports are saturated. A detailed structure of the proposed CC-

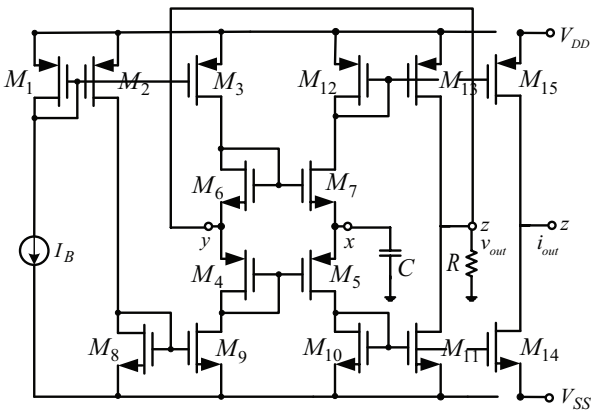

Figure 2: Schematic view of the CMOS square-wave generator based on CCCII.

CII based square-wave generator is shown in Fig. 2 (the well-known realization of classic translinear structure of CCCII). In order to generate the current output, it is necessary to add two additional MOS transistors (to form additional *z* output-dual output CCCII).

The resistor *R* can be replaced with an active resistor R_{eq} at port *z*, composed of two MOSFET transistors. The parasitic resistances (the transresistance) of ports *x* is approximated as [4]

$$R_x \cong 1\Big/\left[\sqrt{2I_B C_{ox}}\left(\sqrt{\mu_p W_p/L_p}+\sqrt{\mu_n W_n/L_n}\right)\right] \cong 1\Big/\left(g_{mn}+g_{mp}\right) \quad (2)$$

where g_m denotes the transconductances of the transistors M_6 (M_7) and M_4 (M_5) (function of bias current I_B) - the NMOS and PMOS components of translinear loop. μ is the carrier mobility; C_{OX} is the gate capacitance per unit area, respectively. This nonlinear relation (2) implies the real limits of the bias currents in the possible practical implementation [4, 5].

The voltage output v_{out} (Fig. 1) has two possible saturation levels; V_{SAT+}=-V_{SAT-}=V_{DD}, and v_{out} can be expressed only either as V_{SAT+} or as V_{SAT-}, because the proposed configuration possesses high positive feedback. At steady-stage operation, we can assume that v_{out} switches from V_{SAT-} to V_{SAT+}. The voltage across the capacitor *C* (v_C) that is charged from the lower threshold voltage (V_{TH-}) to V_{SAT+} and can be expressed as

$$v_C = \left(V_{TH-} - V_{SAT+}\right)e^{-t/R_x C} + V_{SAT+} \quad (3)$$

At the end of first half-period, the capacitor voltage retained its upper threshold voltage (V_{TH+}). On the basis of the internal structure of CCCII and its terminal relationships we can conclude that V_{TH-} and V_{TH+} can be given by

$$V_{TH+} = \left(1 - R_x/R\right)V_{SAT+}; V_{TH-} = \left(1 - R_x/R\right)V_{SAT-} \quad (4)$$

The interval at which the capacitor is charged-T_1, can be derived from (3) as

$$T_1 = R_x C \ln\frac{V_{TH-} - V_{SAT+}}{V_{TH+} - V_{SAT+}} = R_x C \ln\left(\frac{2R}{R_x} - 1\right) \quad (5)$$

Analogously, the interval in which the capacitor discharged can be expressed as

$$T_2 = R_x C \ln\frac{V_{TH+} - V_{SAT-}}{V_{TH-} - V_{SAT-}} = R_x C \ln\left(\frac{2R}{R_x} - 1\right) = T_1 \quad (6)$$

From (5) and (6), bias current I_B can be used for controlling the period of oscillation, owing to the existing dependency between the value of the transresistance of ports *x* (defined with equation (2)) and thus the duration of the intervals T_1 and T_2. Additional controllability would be achieved by installation of an active resistor R_{eq} at port *z* of CCCII, or an active *C*. For oscillation, the oscillator must fulfil two Barkhausen conditions: the loop gain must be slightly greater than unity; the loop phase shift must be 0 or 360 degrees [6]. The proposed circuits (relaxation oscillator) basically possess a certain form of amplifiers with positive feedback (forming circuits with two threshold voltage levels- Schmitt trigger comparator). In this way a portion of its output was fed back re-generatively to the input, and one of the output transistors is driven to saturation (ON state) and the other to cut-off (OFF state). In order for the proposed generator circuit to be able to generate a square wave output signal (voltage/current) – a oscillation condition (OC), it is necessary to set the value of capacitor *C*, the time constant that defines the rate of change on the *x* port of the CCCII, as well as the trigger thresholds levels. Namely, it is necessary that the trigger threshold, which depends directly on the value of R_x, be reached fast enough (a function of time constant), in order to change the condition at the output of the generator circuit at all. Also, from (5) and (6) it is obvious that $2R>R_x$ must be satisfied as one of OC. From these facts it is clear that there is control of the oscillation conditions over the electronically controlled value of the resistance R_x. For the oscillations to start, it is necessary that the initial value of the loop gain be greater than 1, which is provided with slope dv_x/di_x at i_x=0.The output frequency f_o can be given by

$$f_o = \frac{1}{T_1 + T_2} = \frac{1}{2R_x C \ln\left(2R/R_x - 1\right)} \qquad (7)$$

The voltage limits of *x* terminal are dominant, in order to describe the nonlinear behaviour of the proposed circuits. In this case the capacitor *C* can be assumed to be charged with the dependent voltage source $v_x=v_y+i_xR_x$ through terminal resistance, controlled by the bias current. In the context of the functional dependency expressed in this way, the operation of the proposed relaxation oscillator can be analysed on the basis of the current-controlled resistive elements (CCCII) driving plot (DP) in conjunction with the capacitor *C*-as seen by the capacitor at node (port) *x*. In the proposed relaxation oscillator, Fig.1, the linear capacitor *C* is connected at port *x*, e.g. to a current-controlled resistor described by functional relation (2), which is not bijective. This approach can be found in well-known texts pertaining to the problem of nonlinear system analysis [7-10] as original Chua vintage, because any two-terminal resistive device is characterized by its driving-point (DP) characteristic [8]. For the proposed circuits, Fig. 1, port *x* possesses such a characteristic. Fig. 3 shows the driving-point (DP) characteristic of CCCII port *x* (voltage vs. current) depending on the applied bias current I_B. This dependency was recorded using MOS transistors with aspects ratios (*W/L*) given in Table 1 at V_{DD}=-V_{SS}=2.5 V and *R*=5 kΩ, using HSPICE simulation. In the generator circuit defined in Fig. 1, with the CCCII internal structure given in Fig. 2, a variable current source

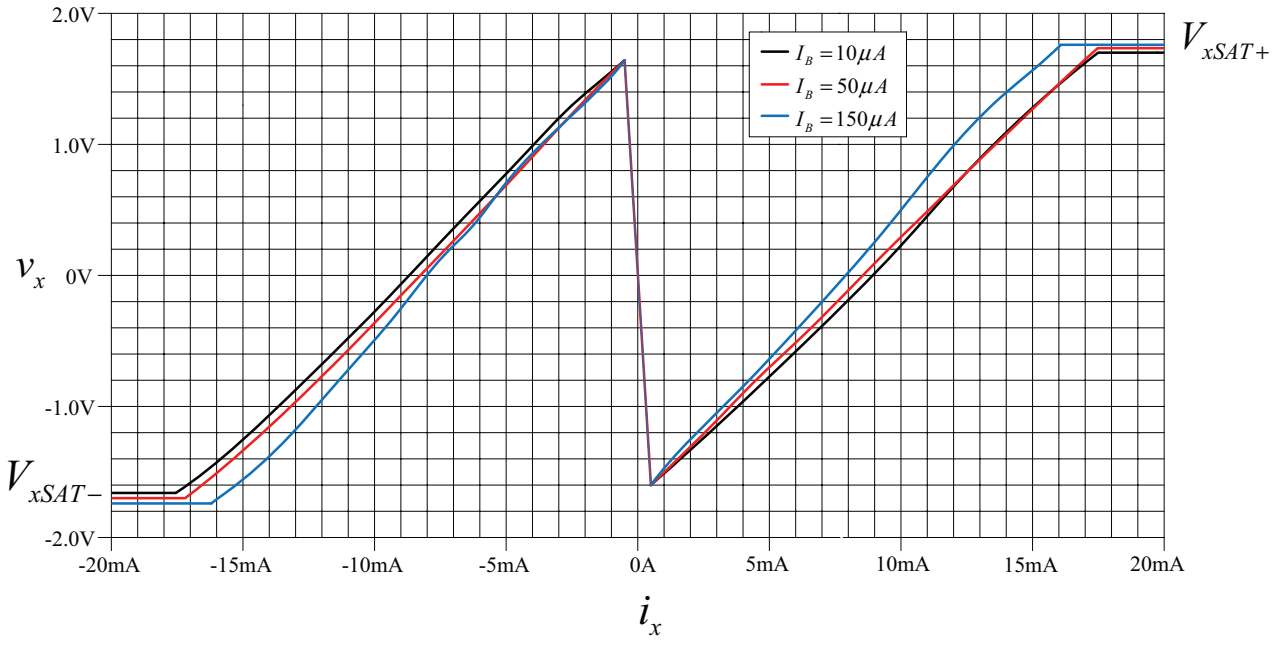

Figure 3: The v_x-i_x curve for current-controlled resistor at CCCII x port

i_x is connected to port *x* instead of capacitor *C*, recording voltage across port *x* (v_x) for different current values I_B. This approach captured the characteristic that also included the reaction circuit existing in the proposed generator circuit.

With this recorded characteristic, the expected properties were confirmed for the proposed circuit, which has a strong nonlinearity (the exact position of the intersections of branches with different slopes depend on the step used in simulation procedure - the resolution itself in Fig. 3) which allows it to produce strong feedback as a pre-condition for the operation of the relaxation oscillator. To give a physical interpretation of this situation, it is necessary to observe that $\dot{v}_C = \dot{v}_x = i_C = -i_x$, thus defining the dynamics (the sign of $\dot{v}_x$) of the characteristic shown in Fig. 3. We reach the state (not the equilibrium point) defined by threshold levels in a finite forward and backward time period. The nonlinear DP reveals the meaning of voltages V_{xSAT} ($|V_{xSAT\pm}| \approx 1.8$ V) and threshold voltages at port *x* V_{xTH} ($|V_{xTH\pm}| \approx 1.6$V), defining the limits of possible changes in *x* port voltage, as well as the extent of approximations that are included in equation (2)-(7) (the obtained values for threshold voltages indicated that the value for the intrinsic resistance was $R_x \approx 200\Omega$). Fig. 3 shows the influence of the bias current on the slope of the DP plot, as well as the slope dv_x/di_x at $i_x=0$ - the slope of the characteristic ensures that the loop gain in the proposed circuit is sufficient to establish the oscillations in the systems with a positive feedback (R_x is actually the positive differential resistance of the outer branches). As was described in [10] regarding the obtained characteristics shown in Figure 3, the locus of the response of the oscillator, following an initial state or excitation, can be estimated by choosing a sequence of points, choosing each new point at a short distance along the slope line of the previous point. The proposed generator possesses the slope at the equilibrium point greater than 2, and we can obtain the portrait of the oscillator in the state plane or the Lienard plane [10], as valuable tools in establishing the nature of the oscillator behavior. The locus for the relaxation oscillator, Fig. 1, for the steady-state response is almost a parallelogram in the Lienard plane, as for some other known solutions of relaxation oscillators [10]. The locus is almost horizontal at the top and the bottom of the locus, moving from one passive region to the other. These last segments of the locus are due to the fast regenerative switching intervals.

The above equations ((2)-(7) - for the case of a small signal operation) fail to adequately represent the real behaviour of the circuit for a large signal operation, because the input resistance R_x is no longer constant. Namely, in this situation R_x possesses different values for high and low voltage level at *x* input [3], and consequently CCCII definition equations must be changed. Defining these different values for R_x as R_{xh} and R_{xl} for these two levels, the period of the oscillation can be expressed as

$$T = T_1 + T_2 = R_{xh} C \ln\left(\frac{2R}{R_{xh}} - 1\right) + R_{xl} C \ln\left(\frac{2R}{R_{xl}} - 1\right) \quad (8)$$

In the situation described in equation (8), we will come to a position to control the duty cycle of the generated oscillation. For the proposed square-wave generator, the obtained voltage levels and operation frequency range, the difference between R_{xl} and R_{xh} can be neglected, and consequently we are practically not in a position to electronically adjust the duty cycle.

2.1 Non-ideal effects

The parasitic components at the CCCII terminal can affect the value of the (7) at high frequency [2, 4]. The terminals *y* and *z* possess high-value parasitic resistance at parallel with low-value parasitic capacitance, while port *x* only already defined the serial resistance R_x. Considering the nonideal gains of active elements-CCCII (tracking errors), the port relations (1) can be rearranged as: $i_y=0$; $v_x=\alpha v_y+i_x R_x$; $i_z=\beta i_x$; where $\alpha=1-\varepsilon_v$ and ε_v ($|\varepsilon_v|<<1$) represents the voltage tracking error from *y* to *x* terminal, $\beta=1-\varepsilon_p$ and ε_p ($|\varepsilon_p|<<1$) denotes the current tracking error from *x* to *z* terminal of the CCCII, respectively. Generally, these tracking factors remain constant and frequency independent within low to medium frequency ranges. Taking the non-idealities of the CCCII into account, (7) respectively, becomes

$$f_o' = \frac{1}{T_1 + T_2} = \frac{1}{2R_x C \ln\left(2R'/R_x\ \alpha\beta - 1\right)} \quad (9)$$

where $R`=R//R_z//R_y$. From (9), it is obvious that the nonideal parameters have only a slight effect on oscillating frequency and condition.

At high frequencies the voltage and current transfer function of CCCII, α and β, becomes frequency dependent-$\alpha(s)$ and $\beta(s)$, $s=j\omega$. Also, parasitic impedances at all ports will be changed, and can be calculated as proposed in [11]- on port *x* an inductance L_x in series with R_x will appear, and it can be calculated after calculation of R_x, from the -3dB cut-off frequency, f_x, of the impedance $Z_x=v_x/i_x$, by $L_x=R_x/2\pi f_x$. Similar procedure is used for determination of C_y, C_z. In this situation, the value of *R'* and R_x will be changed in accordance with parasitic impedances at ports *y* and *z*, appearing in parallel with *R*.

Within the operating range of the proposed generator (up to 25 MHz), the influences of the effects described here are not significantly affected, so that in the further analysis of the operation they are not captured.

For any divergence in the value of the parameter in relation to its nominal value, it is possible to determine the value of the frequency f_0 and calculate the corresponding error-the size of the error in determining the f_0, which occurs as a consequence of the non-ideal nature of the components applied in the circuit proposed in Fig. 1. For example, in equation (9), parameter α was replaced with $(1+\delta\alpha/100)\alpha$, where $\delta\alpha$ stands for the percentage divergence in the value of the α parameter in relation to its nominal value, whereupon the value of the f_0 is calculated. After this, the percentage error-*e*, in measuring of f_0 is calculated as

$$e = \frac{f_o^{'} - f_o}{f_o} 100 \tag{10}$$

where f_o is the frequency of oscillation defined with (7),

and $f_o^{'}$ defined with (9).

The values in Table 1 correspond to the case where all the parameters of interest are known within the limits of ±1 % in relation to their nominal values, based on a uniform distribution of probability – the *uncertainty budget* which is based on the procedures described in GUM [12]. The specific nature of the uncertainty budget set in this manner is reflected in the fact that for certain parameters it is not possible to establish exact values of sensitivity coefficients, since the values depend on the form of the approximations of the function *ln* (in the form of a stepped series). The sensitivity to these parameters is represented as the interval of possible values.

If values in the upper bounds of such intervals are taken as a base for calculation of the combined measuring uncertainties, this would result in a probably unjustified increase of the measuring uncertainty. However, it is not possible to determine to what extent this would be unjustified, by using the usual procedures of determining the measuring uncertainty, as described in GUM [12]. It is equally possible, for example, to make use of the mean values of sensitivity. By assuming a uniform distribution of the sensitivity (of the first error derivatives per parameter), standard measuring uncertainty equalling 2.2% is obtained, i.e. an expanded uncertainty (for the coverage factor *k*=2) amounting to 4.4% – however, it will always remain unknown how far we are from a realistic estimate.

The evaluation of uncertainty in the results of measuring obtained through a simulation of the impact made by variations of all the parameters of interest can be based on one of the methods known by their common name 'The Monte Carlo' method [13] (provided by the HSPICE software package itself). It is expected that such a method offers a more realistic evaluation of uncertainty, given the fact that it does not imply any assumptions, either regarding the distribution of the output value, the error in the measuring results, or the distributions of the sensitivity values. This analysis is used to investigate the effect of the process parameters and the mismatch between transistors, and it also gives the lower and upper limits of the interval, which contains 95% of error-absolute value of the difference between the predicted and observed output value (Monte Carlo predicts the behavior of a circuit statistically when part values are varied within their tolerance range by 5%). Under the above described assumptions, the result of implementation of the Monte Carlo variants is shown in Fig. 4. The measuring uncertainty obtained here amounts to 1.8 %, and it ought to be compared with the data obtained from the uncertainty budget (4.4%). The number of individual simulations was 1000. During this analysis, the bias current was I_B=80 μA, while the capacitor value was 100 pF (*R*=5 kΩ).

The extreme PVT (process-voltage-temperature) variation observed is +/-10%. This tolerance is applied over

Table 1: Uncertainty Budget (the size of the error in determining the frequency of generated square-wave output signal, which occurs as a consequence of the non-ideal nature of the components applied in the circuit proposed in Fig. 1)

Parameter	Estimate	Standard uncertainty	Type	Distribution	Sensitivity coefficient	Contribution to the standard uncertainty
R_x	»1 kW	0.58 %	B	Uniform	-1	0.58 %
C	100 pF	0.58 %	B	Uniform	-1	0.58 %
a	1	0.58 %	B	Uniform	(-1 ÷ -3)	1.16 %
b	1	0.58 %	B	Uniform	(-1 ÷ -3)	1.16 %
R'	5 kW	0.58 %	B	Uniform	(-1 ÷ -3)	1.16 %
e	0					2.2 %

the 0 ^{0}C to 100 ^{0}C temperature range, +/-5% supply variation and +/-5% variation of on-die calibrated capacitor. The +/-10% tolerance is mainly attributed to nonlinearity of current mirroring (as a consequence of the mismatch of the characteristics of the used MOS transistors, much less as a result of possible instability of the bias currents) with respect to temperature, supply variation and small but finite variation of the calibrated capacitor. In [14] highly accurate and stable solutions for realization of current reference sources in 0.18 µm CMOS technology are proposed, based on the behaviour of an original unbalanced current mirror structure. The obtained results confirm the conclusion resulting from the conducted analysis mentioned above, regarding the acceptable sensitivity characteristic of the proposed generator.

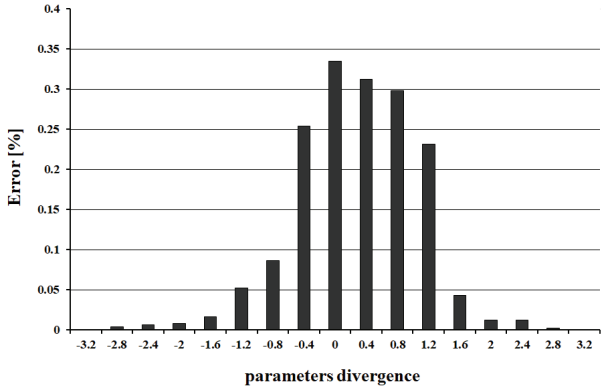

Figure 4: Distribution of errors in the behaviour of the square-wave generator, for divergence in the value of parameters, from their nominal values

3 Simulation and experimental results

The proposed generator was verified with the 0.18µm TSMC level-49 CMOS process using HSPICE simulation. The supply voltages of ±2.5 V (V_{DD}=+2.5 V, V_{SS}=-2,5 V, while the grounded nodes were fixed on 0 V) and the variable bias current I_B (can vary in range from 10 µA up to 400 µA) are used in the simulation. The aspect ratios (*W/L* ratios) of MOS transistors used in CMOS implementation of CCCII are given in Table 2. It should be noted that the proposed circuits can work with the power supply in the range ±1.25 V-±2.5 V; however, with a decrease in the supply voltage, distortion increases in the output square-wave signal, which can be partially offset by the correct selection of passive components and the bias current. The power consumption of the proposed square-wave generator varies in the range from 0.12 mW to up to 1 mW.

Table 2: MOS transistor aspect ratios (*W/L*)

Transistors	W/L (µm)
M_1-M_3	30/2
M_4, M_5	50/0.35
M_6, M_7	20/0.35
M_8, M_9	10/2
M_{10}	10/1
M_{11} (M_{14})	20/2
M_{12}	30/1
M_{13} (M_{15})	50/2

Fig. 5 shows transient responses of voltage and current output of the proposed square-wave generator. The obtained oscillation frequency of 3.846 MHz, I_B=10 µA, Fig. 5a, for the voltage output, is similar to the designed oscillation frequency, equation (7). The transient responses of the generated square-wave current signals when I_B is changed to 80 µA are shown in Fig. 5b, while the frequency is now changed to 3.425 MHz (1% error). The performance of the proposed generator at the higher frequency is further checked when the capacitor value is changed from 100 pF to 20 pF, Fig. 5c. The total harmonic distortion (simulated THD - as a measure of the deviation of the shape of the generated output voltage/current signals from the ideal square-wave signal, all in accordance with the definition of THD [10]) over full frequency operating range of the proposed CCCII-based square wave generator is lower than -23.35 dB (6.8%), and it is comparable with the results obtained in [15].

Additionally, variations of theoretically calculated and simulated values of oscillation frequency f_0 against bias current I_B - the tuning aspects of the circuits, for C = 50 pF, and R=10 kΩ are simulated. In order to confirm the results obtained through theoretical analysis of the proposed relaxation oscillator and the ensuing derived equations, the recorded simulation characteristic (green curve in Fig. 6) was compared with the curve (red curve in Fig. 6) obtained at the basis of the derived relation (7), for the frequency of the output square-wave signal. Moreover, since the relation (2) defines the approximate value of the internal resistance of port *x* (which prevents the direct implementation of (2) in (7), since it would cause an error in calculation of f_0), its value is measured directly at the input port *x* of CCCII, in the process of simulation verification and for different values of current I_B. The obtained values for R_x are completely in accordance with the results obtained in [4, 5], which only confirms the already stated fact about the very complex dependence of this CCCII parameter on the current I_B.

The variation of simulated oscillation frequency is found very close to the theoretical oscillation frequency. Choosing a larger time step between the points at which this transfer characteristic is determined would give substantially flatter transfer characteristic. However, the author tried to describe as accurately as possible the characteristics of the proposed generator.

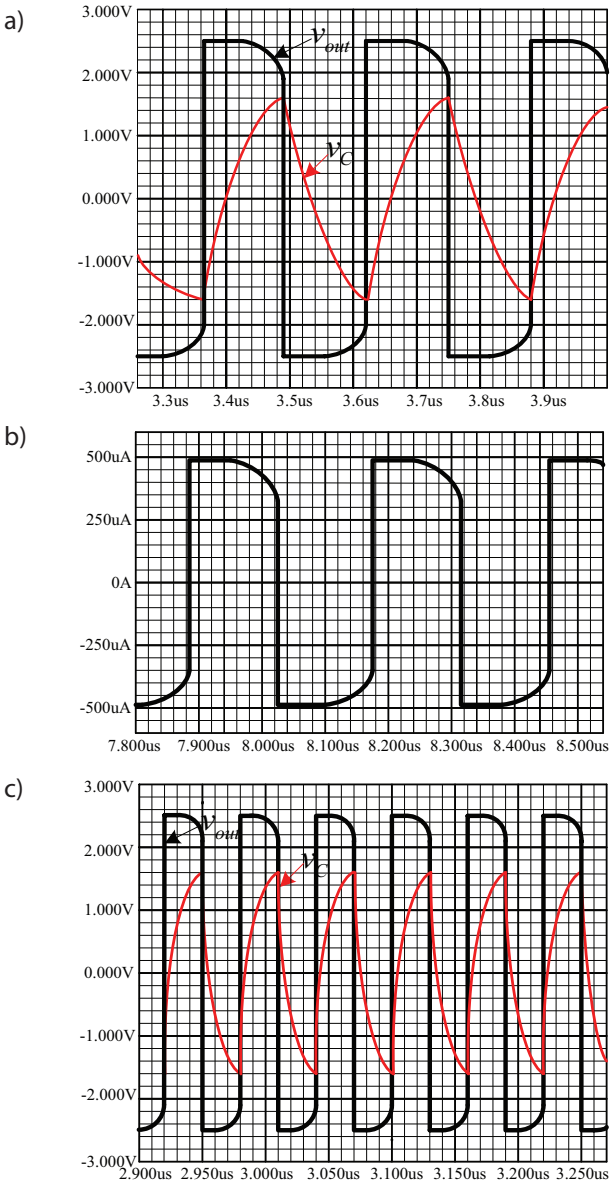

Figure 5: Simulated waveforms of outputs of the proposed square-wave generator a) f_0=3.846 MHz, I_B=10μA, C=100pF, R=5kΩ, b) f_0=3.425 MHz, I_B=80μA, C=120pF, R=5kΩ, c) f_0=16.666 MHz C=20pF, I_B=50μA, R=5kΩ.

The thermal performance of the proposed generator is further investigated, and simulated waveform of voltage output for different temperature values (25, 55 and 70 °C) is shown in Fig. 7. It can be observed from Fig. 7

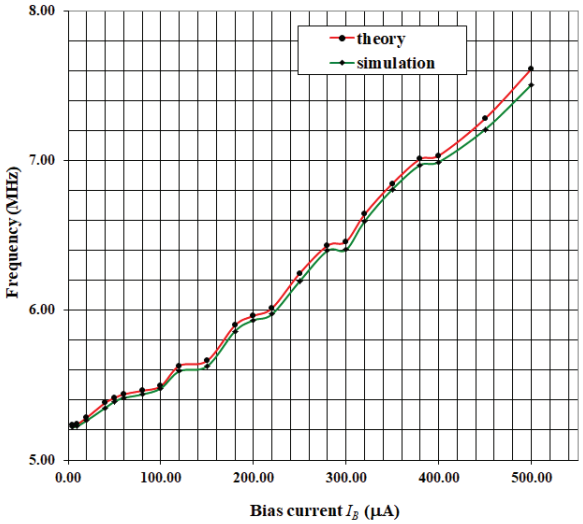

Figure 6: Variation of oscillation frequency, f_0 against bias current, I_B

that frequency f_0 is only slightly affected by the temperature variation, and for example, when the circuits operate at 70°C, the frequency, f_0 is 384.6 kHz (C=1 nF, I_B=50 μA, R=5 kΩ), which represents a 5% deviation from the value at 25 °C. The percentage variation of output voltage amplitude over specified temperature range was 0.0024%, while output current stability was 0.0287 μA/°C. The temperature stability of of intrinsic resistance R_x strongly depends on the physical parameter defined in equation (2). On the basis of analysis conducted in [16, 17], we can conclude that

$$\frac{1}{R_x}\frac{\partial R_x}{\partial T}=\frac{3}{4}T^{-1} \tag{11}$$

e.g. R_x contributes a positive temperature coefficient, thus current biasing circuit that provides a negative temperature coefficient is required for the compensation.

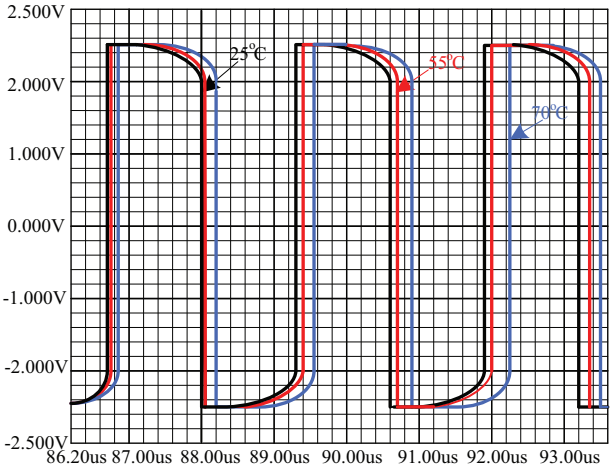

Figure 7: Simulated waveform for different values of temperature (25, 55 and 70°C)

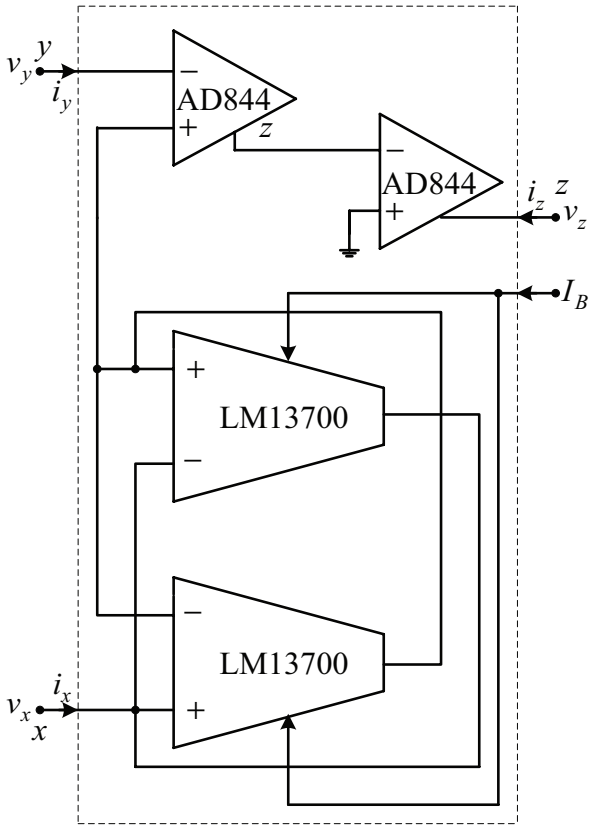

Figure 8: Implementation of CCCII

For experimental verifications, the CCCII+ were realized using commercially available AD844 (CFA) ICs as a current conveyor, while with LM13700 AN (OTA) an electronically tunable floating resistance simulator was obtained, which acts as the parasitic resistance at the node *x* of the CCCII, Fig. 8. By varying the external bias current which is applied to LM13700, the frequency of the oscillations is tuned.

The power supply voltages of ±5 V are applied to AD844 and ±9 V is applied to LM13700. The bias currents are set to I_B=140 μA (the current source with stability of 0.5% was used) and passive components used are R=5 kΩ and C=0.01 μF. The experimentally observed waveforms of voltage output signals are shown in Fig. 9.

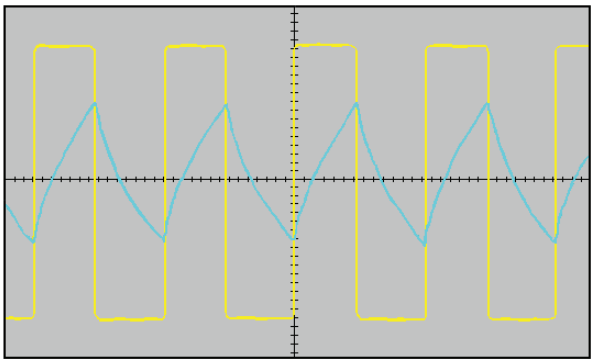

Figure 9: Experimental results (scale: x-axis 0.2 ms/div and y-axis 2 V/div)

Table 3 shows the comparison of the proposed generator with previously reported generator circuits. It is observed that the following features are available from the proposed circuit: only one active element; use of

Table 3: Comparison of the proposed generator circuit with previously reported circuits

Ref.	Active element type	No. of active element	No. of passive components	All grounded passive components	Duty cycle adjustable	Max. operational frequency [MHz]	Power consumption
[3]	CCII+	1	2R, 1C	no	no	0.5	-
[15]	CCII+	3	5R, 1C	no	no	0.15	14.59 mW
[18]	MO-DXCCTA	1	1 R, 1 C	yes	yes	32.5	1 mW
[19]	FTFN	1	2R, 1C	no	yes	5	2.81 mW
[20]	DVCC	2	3R, 1C	yes	yes	0.8	763 mW
[21]	OTA	3	1C	yes	no	0.0505	71.3 μW
[22]	CFOA	2	3R, 1C	no	yes	2	458 mW
[23]	CCII	2	3R, 1C	no	no	0.26	384 mW
[24]	MO-CCCDTA	2	1C	yes	no	0.2	-
[25]	CG-VDCC	1	2R, 1C	yes	yes	4.3	6.28 mW
[26]	OTRA	2	3R, 1C	no	no	1	-
[27]	CCII	2	6R, 1C	no	no	0.737	400 mW
[28]	MO-CIDITA	1	1C	yes	yes	75	0.5 mW
[29]	DVCC	2	3R, 1C	yes	no	2.5	-
[30]	MO-DVCCTA	1	1R, 1C	yes	yes	1	226 mW
This work	CCCII	1	1R, 1C	yes	no	25	0.12 mW-1 mW

minimal number of passive grounded components; independent tuning of oscillation frequency; wide range of operating frequency; less complexity in terms of transistors count and low power consumption. The solution proposed in [18] also uses only one active element and offers a higher operation frequency range, but the deployed active element demands a bias voltage in currents for proper operation. Also, MO-CIDITA [18] possesses a much more complex internal structure with more MOS transistors then CCCII.

The proposed circuit has lesser complexity in terms of design and component requirements in comparison with circuits (on the same basic platform - based on the use of CCII) presented in [3, 15, 21, 23, 27]. In standings with the comparative operating frequency, the generator proposed here can work in the megahertz range (MHz), which is an important advantage of the described design in many modern electronics and communication applications. The proposed circuit consumes the least power compared to all other circuits, except the generator proposed in [21].

4 Conclusion

This paper presents a new square-wave generator using only one CCCII, grounded resistors and one capacitor, which reduces noise effects and guarantees a low parasitic effect. The oscillation frequency of the proposed relaxation oscillator has been shown to strongly depend on the nonlinear behaviour of the CCCII where the value of the *x* terminal resistance R_x is a very important factor in determining the oscillation frequency. The bias current is used to control the oscillating condition and oscillating frequency, which can also be adjusted by changing resistance and capacitor value. Both voltage and current signals can be obtained within a single topology (mixed output mode), which has gained recent popularity in analog signal processing. The circuit shows a good high frequency performance of the current mode circuits and is free from high frequency limitations such as slew rate and gain reduction problems in the OA realization. The proposed circuit exhibits low sensitivity properties and possesses high output impedances at current terminals, thus ensuring insensitive current outputs that require no additional current followers to be sensed. Application of only grounded passive components makes the circuit suitable for IC implementation. Finally, a good match between theoretical, simulation and practical results was confirmed in the paper.

5 Acknowledgments

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6 Conflicts of interest

The author declares no conflict of interest. The founding sponsors had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, and in the decision to publish the results.

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Analog / Radio-Frequency Performance Analysis of Nanometer Negative Capacitance Fully Depleted Silicon-On-Insulator Transistors

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Abstract: The negative capacitance field-effect transistor can break the limitation of the Boltzmann tyranny. In this study, the analog and radio-frequency (RF) performance of a nanometer negative-capacitance fully depleted silicon-on-insulator (NC-FDSOI) transistor is investigated. The analog/RF parameters of the NC-FDSOI device are compared with the conventional FDSOI counterparts for transconductance, output conductance, gate capacitance, cutoff frequency, and maximum oscillation frequency. In addition, the effect of ferroelectric thickness on the analog/RF performance of NC-FDSOI device is analyzed and discussed. The results show that even when operated at low voltages, NC-FDSOI transistors enable analog/RF performance improvement in traditional FDSOI counterparts at low power in the case of a suitable ferroelectric thickness.

Keywords: negative capacitance effect; NC-FDSOI transistor; analog / RF Performance; ferroelectric capacitance

Analogna in radio frekvenčna analiza učinkovitosti nanometrskega polno osiromašenega silicijevega tran-zistorja na izolatorju z negativno kapacitivnostjo

Izvleček: Poljski tranzistor z negativno kapacitivnostjo lahko premaga oviro Boltzmannove tiranije. V članku je raziskan analogna in radio frekvenčna učinkovitost nanometrskega polno osiromašenega silicijevega tranzistorja na izolatorju z negativno kapacitivnostjo (NC-FDSOI). Analogni/RF parametri NC_FDSOI elementa, kot so: transkonduktanca, izhodna konduktanca, kapacitivnost vrat, frekvenca odklopa in največja frekvenca osciliranja, so primerjani s klasičnim FDSOI. Dodatno je analiziran vpliv feroelektrične debeline NC-FDSOI elementa. Rezultati kažejo boljšo učinkovitost NC-FDSOI tranzistorjev tudi pri nizki napajalni napetosti in ustrezni feroelektrični debelini.

Ključne besede: efekt negativne kapacitivnosti; NC-FDSOI tranzistor; analogna / RF učinkovitost; feroelektrična kapacitivnost

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1 Introduction

In the past decade, complementary metal-oxide-semiconductor (CMOS) transistors have experienced unprecedented development, shrinking device sizes, and advances in integrated device design and fabrication, bringing the CMOS technology into the nanometer era. However, continued miniaturization has also brought about various new constraints, such as high-power consumption caused by chip overheating [1]. To solve these problems, steep switching characteristics and lower operating voltage can be achieved by lowering the sub-threshold slope (SS). NCFETs based on ferroelectric on a gate stack have attracted significant attention in the field of advanced CMOS devices due to their lower SS (<60 mV/decade) [2]-[8]. Recently, NCFETs have proven to be suitable for a variety of low-

power applications, such as wearables, bioelectronics, and the Internet of Things [9]-[12]. Furthermore, with the advent of the 5G era in radio-frequency (RF) applications, the analog/RF performance of NCFETs must be tested. FDSOI technology is popular because it better overcomes short channel effects and is significantly less expensive to manufacture than fin field effect transistors (FinFETs). In previous studies, FDSOI transistors showed good analog/RF performance [13, 14]. However, the relationship between the negative capacitance effect and analog/RF performance parameters for FDSOI devices is still not understood. Therefore, in this work, we address this deficiency by simulating analog/RF performance of 20-nm NC-FDSOI transistors with different ferroelectric thicknesses (T_{fe}) utilizing a computer-aided-design (TCAD) tool.

2 Materials and methods

At present, most negative-capacitance transistors are implemented by adding ferroelectric materials [15]-[20]. There are two main types of structures used in the negative capacitance transistors: metal-ferroelectric-metal insulator-semiconductor (MFMIS) and metal-ferroelectric insulator-semiconductor (MFIS). Owing to the better performance of the MFMIS NCFET in terms of it being hysteresis-free [21], a NCFET with MFMIS structure is used in this work. Then, the TCAD tool is used to add a ferroelectric capacitor to the gate on the underlying conventional FDSOI to form an NC-FDSOI transistor. The structure of the FDSOI and NC-FDSOI transistor are shown in Fig. 1.The gate of NC-FDSOI used an HfO2 based ferroelectric with coercive field, Ec = 1 MV/cm and remnant polarization, Pr = 5 μC/cm2. For better compatibility with the CMOS process[22], a smaller ferroelectric thickness is chosen (T_{fe} = 1, 2, 3, and 4 nm).

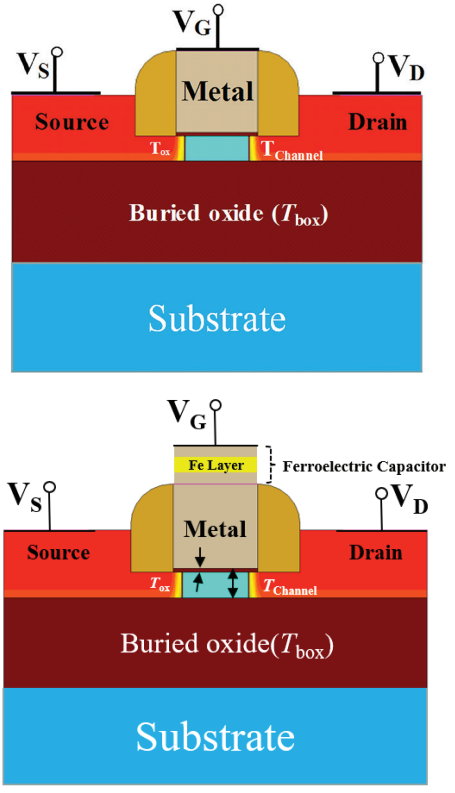


Figure. 1: FDSOI and NC-FDSOI device structure.

The device parameters used for numerical simulation are summarized in Table 1.The TCAD mixed-mode device simulator is used to simulate the NC-FDSOI and FDSOI transistors [23], and the frequency characteristics of the NCFDSOI and FDSOI are discussed by AC small-signal analysis. The simulation uses a variety of physical models, such as Fermi statistics, doping-dependent mobility, high-field saturation, mobility degradation at interfaces, Shockley-Read-Hall recombination, and density-gradient quantization. The Poisson and Landau-Khalatnikov equations are solved self-consistently by the TCAD tool [24, 25]. The LK equation, which relates the polarization (P) and electric field (E), is given in Eq. (1) [26, 27]:

$$E = 2\alpha P + 4\beta P^3 + 6\gamma P^5 + \rho \frac{dP}{dt} \quad (1)$$

where α, β, γ, and ρ are ferroelectric material parameters and P is the polarization strength. In this work, RF performance parameters are extracted from the two-port network.

Table 1: device structural parameters

Parameter	FDSOI	NC-FDSOI
Channel Length(L_g)	20nm	20nm
Spacer Length(L_{sp})	10nm	10nm
Channel Doping(N_d)	$10^{14}cm^3$	$10^{14}cm^3$
Channel Thickness($T_{channel}$)	5nm	5nm
Oxide Thickness(T_{ox})	0.9nm	0.9nm
Work-founction(Φ_m)	4.52	4.52
ferroelectric thickness (T_{fe})	0	1,2,3,4nm
Coercive Field(E_c)	0	$1MV/cm^3$

3 Results and discussion

Fig. 2(a) and (b) shows the transfer characteristics of drain current (I_{ds}) versus gate voltage (V_{gs}) for a conventional FDSOI and NC-FDSOI fixed at drain voltages (V_{ds}) of 0.7 and 0.05 V. It can be seen that the current of the NC-FDSOI is always greater than that of the FDSOI, and the SS is lower, whether it is working in a linear or saturated region. The results show that the current-amplifi-

cation capability of the NC-FDOI is significantly stronger than that of the conventional FDSOI (~60% addition, T_{fe}=3 nm) at V_{ds} =0.7 V. When the thickness of the ferroelectric (T_{fe}) of the NC-FDSOI is set to 6 nm, SS=43 mV/decade breaks the limit of the SS for the transistor at room temperature, where SS is extracted from Eq. (2):

$$SS = \frac{1000}{\frac{d}{dV_{gs}} \log_{10} I_{ds}} \quad (2)$$

As the SS decreases, the ratio of on- and off-state currents (I_{on}/I_{off}) increases compared to the FDSOI, which indicates that the NC-FDSOI is more suitable for high-speed switching applications than the conventional FDSOI. Experiments under actual environmental measurements also show that NC-FDOSI has good current amplification capability and low SS, which the SS is reduced from 78 mV/decade to 73 mV/decade, and the drain current is increased from 4 μA to 7 μA [28]. Fig. 2(c) and (d) shows the output characteristics of I_{ds} versus V_{ds} for their fixed values at V_{gs}=0.7 and 0.4 V. As shown in Fig. 2(c) and (d), the ferroelectric has an enhanced effect on the output characteristics of the device, whether at high or low V_{gs}. However, at low V_{gs}, the internal gate voltage (V_{in}) is lowered due to the influence of the ferroelectric, and the negative differential resistance (NDR) effect is generated [29].

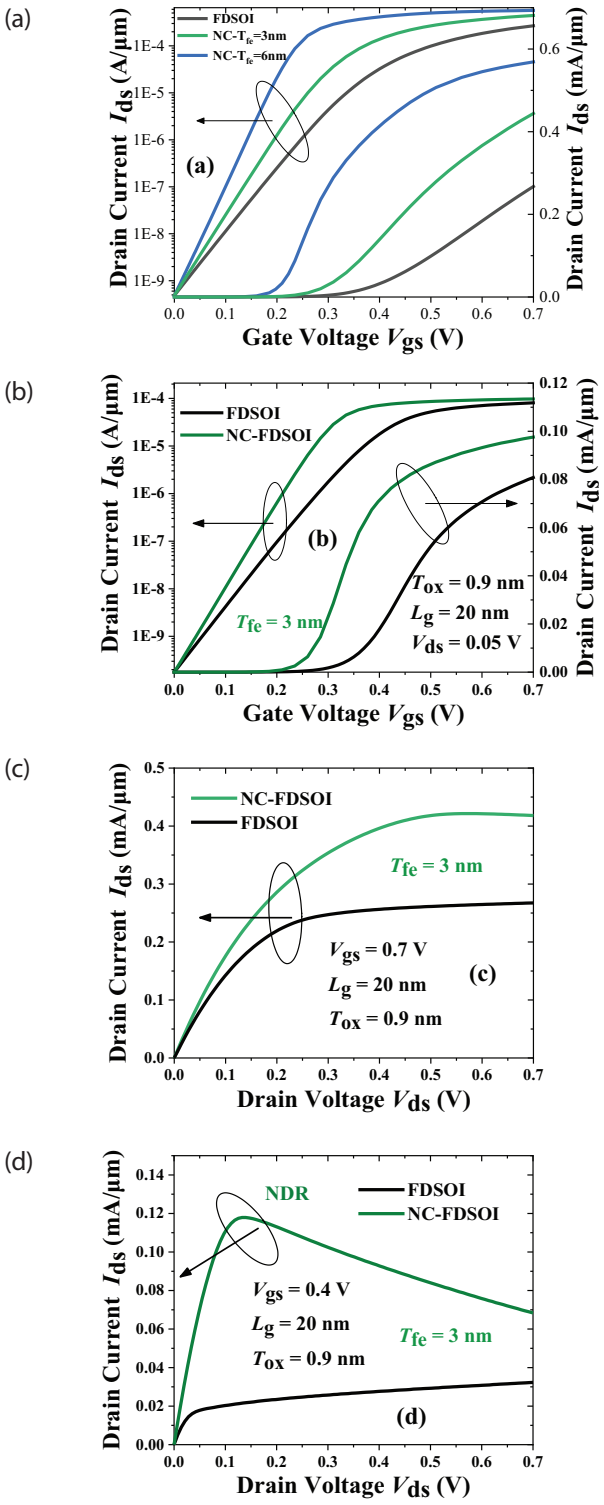


Figure 2: (a) I_{ds} with V_{gs} for FDSOI and NC-FDSOI at V_{ds}=0.7 V. (b) I_{ds} with V_{gs} for FDSOI and NC-FDSOI at V_{ds} =0.05 V. (c) I_{ds} with V_{ds} for FDSOI and NC-FDSOI at V_{gs} =0.7 V. (d) I_{ds} with V_{ds} for FDSOI and NC-FDSOI at V_{gs} =0.4 V.

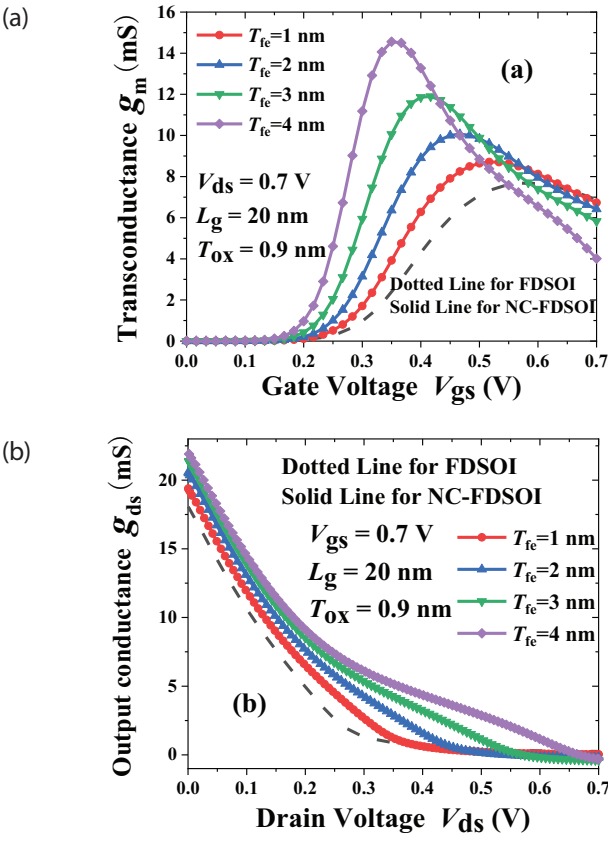
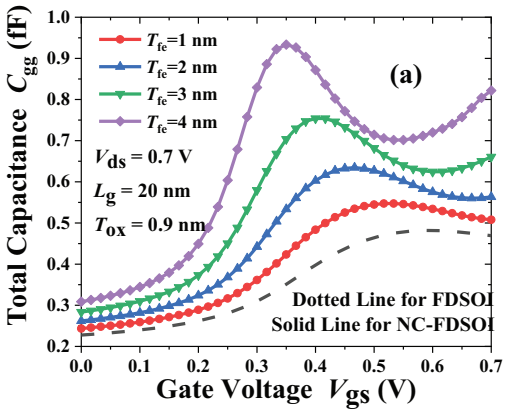


Figure. 3: (a) Transconductance (g_m) with V_{gs} for FDSOI and NC-FDSOI. (b) output conductance (g_{ds}) with V_{ds} for FDSOI and NC-FDSOI.

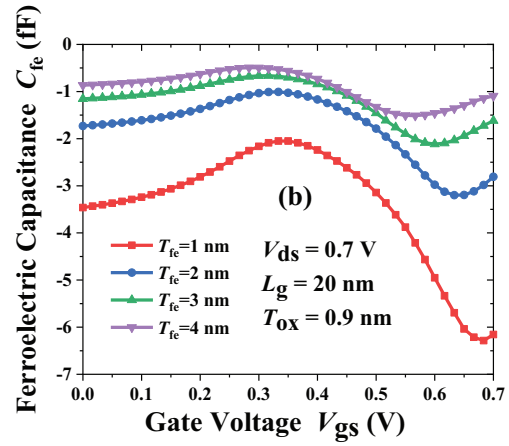
Fig. 3(a) shows transconductance (g_m) with V_{gs} at V_{ds} = 0.7 V and the output conductance (g_{ds}) as a function of V_{ds} fixed at V_{gs} = 0.7 V, where g_m determines the device's gain. The g_m and g_{ds} values for both the devices are obtained by Eqs. (3) and (4), respectively:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \tag{3}$$

(a)



(b)



(c)

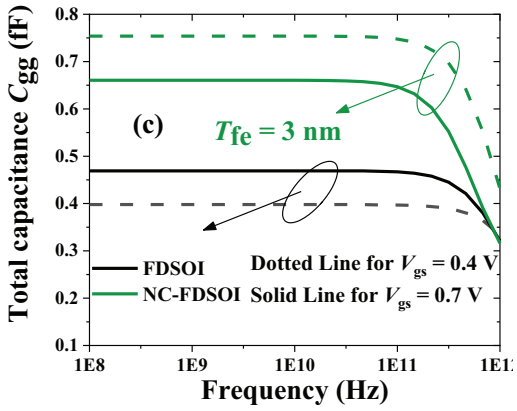


Figure. 4: (a) gate capacitance (C_{gg}) with V_{gs} for FDSOI and NC-FDSOI. (b) ferroelectric capacitance (C_{fe}) with V_{gs} for NC-FDSOI. (c) gate capacitance (C_{gg}) with frequency for FDSOI and NC-FDSOI.

$$g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}} \tag{4}$$

It can be clearly seen from Fig. 3(a) and (b) that the g_m and g_{ds} values of the NC-FDSOI are much larger than those of the FDSOI device, and the g_m and g_{ds} values of the NC-FDSOI are further increased as the thickness of the ferroelectric increases. As the current gain decreases, g_m will gradually decrease after reaching the peak, but overall it will be larger than that of the FDSOI. This indicates that the NC-FDSOI transistor gain increases as T_{fe} increases within a certain range due to the negative-capacitance effect. The high transconductance makes the NC-FDSOI suitable for high-gain amplifier applications.

Fig. 4(a) and (b) shows the total gate capacitance (C_{gg}) and ferroelectric capacitance (C_{fe}) of the NC-FDSOI with V_{gs} at different ferroelectric thicknesses (T_{fe} = 1, 2, 3, and 4 nm). Simply lowering the threshold voltage (V_{th}) and lowering SS is not enough to improve circuit performance. The important device parameters that affect performance specifications, such as power dissipation and intrinsic delay, are the total gate capacitance [30]. Therefore, it is necessary to analyze the impact of the ferroelectric thickness in the gate stack on C_{gg}. As shown in Fig. 4(a), as the thickness of the ferroelectric increases, the gate capacitance increases compared with the FDSOI total capacitance (C_{mos}). As shown in Fig. 4(b), this is mainly due to the decrease in the absolute value of the ferroelectric capacitance (C_{fe}). Fig. 4(c) shows the variation of C_{gg} with frequency at V_{gs} = 0.4 and 0.7 V. In Fig. 4(c), C_{gg} begins to decrease after approximately100 GHz, and the C_{gg} of NC-FDSOI is larger at V_{gs} =0.4 V. This result is consistent with that shown in Fig. 4(a).

In Fig. 5(a) and (b), the cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) with V_{gs} at V_{ds} = 0.7 V, where f_T is extracted from current gain (h21) through an extrapolation of a 20-dB/decade slope, and f_{max} is extracted from Mason's unilateral gain through an extrapolation of a 20-dB/decade slope. It can be seen from Fig. 5(a) that the maximum f_T of the NC-FDSOI is the same as that of the conventional FDSOI. However, with the increase of V_{gs}, the NC-FDSOI leads to f_T achieving peaks at lower V_{gs} due to the increase of ferroelectric thicknesses compared to the baseline FDSOI (T_{fe} = 0) [26]. As is known from Eq. (5), this is because both g_m and C_{gg} peak at a lower V_{gs}, which is caused by a decrease in V_{th} as Tfe increases [31]. It can be seen from Eq. (6) that f_{max} is mainly affected by f_T and gate resistance (R_g), so f_{max} in Fig. 5(b) is the same as the f_T trend and peaks at a lower gate voltage. Under the influence of g_m reduction, f_T and f_{max} gradually decrease after reaching

the peak value and are lower than that of the FDSOI at high gate voltage, and the RF performance of the circuit will deteriorate at high gate voltage. Therefore, the NC-FDSOI performs better at low bias voltages:

$$f_T = \frac{g_m}{2\pi C_{gg}} \tag{5}$$

$$f_{\max} = \frac{f_T}{\sqrt{4R_g\left(g_{ds} + 2\pi f_T C_{gd}\right)}} \tag{6}$$

(a)

(b)

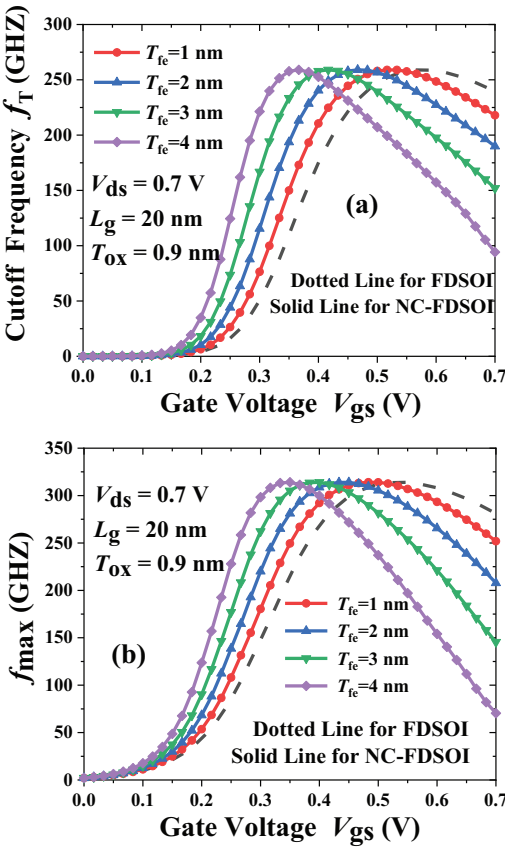


Figure. 5: (a) cutoff frequency (f_T) with V_{gs} for FDSOI and NC-FDSOI.(b) maximum oscillation frequency (f_{max}) with V_{gs} for FDSOI and NC-FDSOI.

4 Conclusions

In this work, a comparison of analog/RF performance between NC-FDSOI and FDSOI transistors is demonstrated, and the effects of ferroelectric thickness on the analog/RF parameters of the NC-FDSOI are analyzed. The f_{max} was measured for the first time, and through a one-to-one comparison with FDSOI, the high frequency dependence of the C_{gg} and the V_{ds} dependence of the g_{ds} were achieved for the first time.The results show that the NC-FDSOI is superior to the conventional FDSOI in terms of SS, g_m, and g_{ds}, and the effect is more significant with the increasing thickness of the ferroelectric. After the addition of the ferroelectric negative capacitance, the f_T and f_{max} values of the NC-FDSOI also peak at a low bias voltage. Therefore, in the case of a suitable T_{fe}, the NC-FDSOI can not only outperform the conventional FDSOI in terms of digital circuits but also achieve better analog/RF performance compared to the FDSOI with reduced power consumption.In the future we will also study the effects of different ferroelectric parameters on analog/RF performance.

5 Acknowledgments

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6 Conflict of Interest

The authors declare no conflict of interest. The founding sponsors had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, and in the decision to publish the results.

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A Design and Optimization of a New, Three-Axis MEMS Capacitive Accelerometer with High Dynamic Range and Sensitivity

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Abstract: In this paper a three-axis capacitor accelerometer has been designed, analyzed and optimized using micro-electromechanical systems technology. The accelerometers are generally divided into three categories of single axis, two axes, and three axes in terms of their ability to measure acceleration. In the suggested structure, acceleration measurements are carried out on all three axes simultaneously using a mass and spring system, which makes it possible to achieve a high sensitivity at a low occupancy level without losing other accelerator factors. By taking difference in this structure, it is shown that each axis acceleration has a very low impact on the measured acceleration of the other two axes. If any external factor changes the value of a single capacitor, the original output of the capacitor does not change for detecting acceleration. In other words, the acceleration of any of these three axes, due to its designing features, does not influence the other two axes and the system performance cannot be disrupted by external factors. The other important characteristics of the accelerometers are dynamic range, operating frequency and sensitivity. This study covers a dynamic range up to 1000g and an operating frequency up to 20 kHz. The accelerometer sensitivity is 4 fF/g in the z axis direction while it is 9 fF/g in the x and y axes directions. In this paper, the simulation of the structure is performed using Intellisuite software. Moreover, a multi-objective genetic optimization algorithm has been used to determine the dimensions of the constituents of the spring and the weight.

Keywords: Accelerometer; Three Axis; MEMS; Dynamic Range; Operating Frequency

Zasnova in optimizacija novega troosnega MEMS kapacitivnega pospeškometra z velikim dinamičnim območjem in visoko občutljivostjo

Izvleček: V članku je predstavljena zasnova, analiza in optimizacija kapacitivnega pospeškometra z uporabo mikro elektromehanične tehnologije. Pospeškometri so običajno deljeni v tri skupine glede na zmožnost meritve pospeška v eni, dveh ali treh oseh. V predlagani strukturi se pospešek meri simultano v vseh treh oseh z uporabo sistema mase in vzmeti, kar omogoča doseganje visoke občutljivosti pri nizki stopnji zasedenosti in brez izgube ostalih parametrov pospeška. Z vnosom različnosti v strukturo je pokazano, da pospešek v eni osi zelo malo vpliva na meritve pospeška v drugih dveh oseh. Če katerikoli zunanji vpliv spremeni vrednost kondenzatorja, se originalen izhod kondenzatorja za detekcijo pospeška ne spremeni.Z drugimi besedami povedano, pospešek ene osi, zaradi narave zasnove, ne vpliva na ostali dve osi in delovanje sistema ni podvrženo zunanjim vplivom. ostale pomembne karakteristike pospeškometrov so dinamično območje, delovna frekvenca in občutljivost. Študija obsega dinamičen razpon do 1000g in delovno frekvenco 20 kHz. Občutljivost pospeškometra je 4 fF/g v z osi in 9 fF/g v x in y smeri. Simulacije so narejene s programskim paketom Intellisuite. Za določanje uteži in vzmeti je bil uporabljen več objektni optimizacijski algoritem.

Ključne besede: Accelerometer; Three Axis; MEMS; Dynamic Range; Operating Frequency

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1 Introduction

An accelerometer is a device that measure proper forces of acceleration and is one of the most important sensors widely used in modern systems. Accelerometers can provide a completely independent positioning device which detects position with reference to an original point without any use of a receiver or transmitter from a satellite or other sources. This feature is used in the navigation field. Furthermore, the efficiencies of engine, torque transfer system, and brake system can be evaluated via accelerometer. Accelerometers can be employed to measure the vibrations of automobiles, machines, buildings, control systems process, and device installation safety (Yuan et al. 2006; Marek et al. 2005).

These applications have all focused on making accelerometers smaller (i.e., occupying less room) and more sensitive. Generally, there are several types of MEMS[1] accelerometers: piezoelectric, piezoresistive, resonance oscillator, capacitive, SERVO, and tunneling phenomenon (Allen. 2005; Beeby et al. 2004). The aim of this study is to obtain a three-axis accelerometer with high dynamic range, high operating frequency, and high sensitivity with low occupancy level using MEMS technology. Compared with other types of accelerometers, the capacitive accelerometers have the several advantages such as high precision to a micro-g range, high sensitivity, proper response to the fix input, proper performance against noise, low temperature sensitivity, applicable in a wide range of temperature, low power consumption, low losses and simplicity of mechanical structure (Ashok Kumar et al. 2017; Lammel. 2015).

Up to now, many capacitive accelerometers have been designed and created. For example, (Kraft. 1996) proposed a single one-axis capacitive accelerometer which can measure acceleration in the direction of one axis. In order to have a good sensitivity in this structure, large-area capacitive planes are required. Therefore, the total occupancy level for making sensor is too high. Besides, this structure has a low dynamic range. In (Moghadam et al. 2014), a one-axis accelerometer with folded arms was presented. In this accelerometer, by reducing the spring constant, the sensitivity increase. In this scheme, reduced spring rigidity results low operating frequency and dynamic range of the sensor. (Terzioglu et al. 2015) Introduced a one-axis comb-like accelerometer. However, this accelerometer was limited to measure acceleration in a single axis direction and was thus inappropriate for applications that would require acceleration measurements in two or three axes directions. In (Tavakoli and Sani. 2015), a two-axis accelerometer was developed, in which the maximum capacitor changes was 975fF. The maximum measurable acceleration was 325g. A three-axis accelerometer without detecting the acceleration direction was offered in (Benevicius et al. 2013). In this accelerometer, in order to have a 3fF/g sensitivity and 1000g acceleration in the z axis direction, a dimension of at least 850*850um was needed for the plane beneath the weight. This condition was realized by designing a proper spring. The main problem in (Benevicius et al. 2013) was calculating acceleration in the direction of the other two axes with a very low sensitivity due to the change of capacitance caused by the change in the overlap area. For example, with 1um displacement, the capacitor value changed only about 2%, and for having a 3 fF/g sensitivity, only the acceleration of 20g could be measured. Besides, this accelerometer could not differentiate accelerations of different axes and could not realize the axis direction of the applied acceleration. A three-axis accelerometer composed of three separate accelerometers was presented in (Tez et al. 2015). This structure had three separate parts with around 0.4mm^2 surface area. In this context, by considering the required space for spring installation, a capacitor plane of around 500*500um could be used in the z axis direction. Considering the sensitivity of 3fF/g, the sensitivity of the maximum measurable acceleration would be 450g. Similarly, it can be proved that the required acceleration in (Tez et al. 2015) could not be satisfied along the other two axes.

In this paper a new structure is developed to cover a dynamic range up to 1000g and an operating frequency limit of up to 20 kHz with the sensitivity constraint of 3fF/g in all the three axes. Note that the suggested scheme, having the aforesaid advantages, has also kept a proper occupying level, which cannot be observed in any of the previous three-axis accelerometer structures. Moreover, this structure is able to separately measure accelerations along all the three axes. The acceleration effect of each axis on the measured accelerations of the other two axes is zero. Note that the accelerometer proposed in this paper is validated by simulation and has not entered the construction stage.

The present paper is organized as follows. In Section 2, principles of the accelerometer performance are presented. Section 3 focuses on the design of the proposed accelerometer. In this section, a new structure is indeed provided for three-axis accelerometers. In Sections 4 and 5, by analyzing the relations concerning this structure, the outputs are calculated and diagrammed and the results are then compared with other studies.

[1] *Micro-electromechanical Systems(MEMS)*

2 Analysis of MEMS accelerometer

Mechanical model of an accelerometer is shown in Fig. 1. This model is mainly comprised of a hanging weight with a defined mass, one (or several) spring(s), a fluid damper (mostly air), and a body which in fact forms the mechanical part of the accelerometer.

From Fig. 1, the relation between force (F) and displacement of the pending weight can be expressed as follows (Bao and Yang, 2007):

$$F(t) = M\frac{d^2x}{dt^2} + C\frac{dx}{dt} + Kx \tag{1}$$

Where x is mass displacement from its original state, C is damper coefficient, M is mass, and k is spring constant.

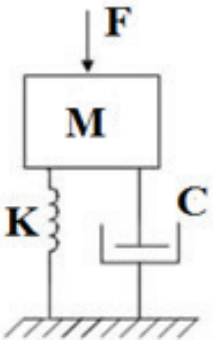

Figure 1: Mechanical model of the accelerometer (Acar and Shkel. 2007).

Force, *F*, can be generated by applying acceleration to the structure, and accordance with Newton' second law of motion (F=ma), *a* is the same acceleration that must be measured by the accelerometer.

Now, in order to obtain the amount of weight displacement due to the applied acceleration, Laplace transformation is to be taken from the differential equation of relation 1 and Newton's second law of motion to achieve a transition function with the applied acceleration as its input and the displacement as its output, thus (Bao and Yang, 2007):

$$H(s) = \frac{x(s)}{a(s)} = \frac{1}{s^2 + \frac{c}{m}s + \frac{k}{m}} \tag{2}$$

For frequencies below natural frequency, the following linear relation can be used for the mass and spring system (Acar and Shkel. 2007):

$$\frac{x}{a} = \frac{m}{k} \tag{3}$$

The natural frequency of mass-spring-damper is as follows (Momen et al. 2016):

$$f = \frac{1}{2\pi}\sqrt{\frac{k}{M}} \tag{4}$$

Eq. 3 shows the mechanical sensitivity of the system in the direction of the applied acceleration, which is equal to the value of weight displacement caused by the application of unit acceleration. As this relation shows, for increasing mechanical sensitivity, it is required to increase mass and decrease the spring rigidity coefficient; however, increased mass and decreased spring rigidity coefficient reduce the natural frequency of the spring according to relation 4. Therefore, these two issues must be kept in balance in the designing process.

In accelerometer sensors, acceleration is usually given in g. In capacitive accelerators, sensitivity is defined as the ratio of the capacitor changes due to a 1-g acceleration, and thus (Momen et al. 2016):

$$s = \frac{\Delta C}{g} = \frac{\Delta C}{x} \times \frac{x}{g} \tag{5}$$

If the field effect of the electrodes margin is disregarded, changes in capacitances due to air distance between electrodes can be expressed as follows (Bao and Yang, 2007):

$$\Delta C = \varepsilon A\left(\frac{1}{d-x} - \frac{1}{d+x}\right) \to x^2 << d^2 \to 2\varepsilon_{\prime} \tag{6}$$

Where d is the original air distance, A shows the total area of the planes comprising capacitor, and x is displacement from original state. From Eq. 6, it is clear that the change of the capacitance is proportional to the mass deviation, which is due to the acceleration applied to the system under the assumption that the deviation is small (Momen et al. 2016).

Besides, the most important parameters in accelerometers are dynamic range and operating frequency. The dynamic range refers to an acceleration range in which the accelerometer can do the measurements. The accelerometer operating frequency is the point in which the amount of applied acceleration varies rapidly. This acceleration can be measured using a high-operating frequency accelerometer (namely, an accelerometer that responds quickly to the rapid changes) (Bao and Yang, 2007).

In what follows, an accelerometer is designed, which is able to measure acceleration ranging from -1000g to +1000g and which covers a 20-KHz frequency limit.

3 Design of a new Accelerometer

In this section, the suggested structure is designed. To this end, first the capacitive planes and then the spring are designed. Finally, the complete structure is presented.

3.1 Designing of capacitive planes

The changes of capacitor in accelerometers are caused by three motions: changes in the overlapping of surfaces, air distance, and dielectric overlapping (Momen et al. 2016). The highest sensitivity is caused by the change of air distance. Therefore, air distance change parameter has been applied in all the three axis directions as the main distinguishing feature of the suggested scheme, compared to the previous methods. There are three parallel planes in the z axis direction: two of them are fixed and the third and the middle one is mobile. By making difference in the capacitance measurement, the two parallel upper and lower planes can minimize the noise effect on the obtained value. As an innovation, our suggested scheme is capable of measuring acceleration in the x and y axes directions. When the acceleration in the y axis direction is applied, as shown in Fig. 2, the mobile plane and the combs will be moved in the direction of the applied acceleration, and resultantly the values of capacitors C1 and C3 increase due to small air gap, while capacitors C2 and C4 have lower values than their original states. Using a single parameter, the following equation shows the total value of capacitive changes induced by the acceleration in the said axis direction:

$$Cy = C1 + C3 - (C2 + C4) \quad (7)$$

When no acceleration exists in the y direction, the result of the above relation will also be zero. If acceleration is applied in the positive direction of the y axis, the result will be positive; if acceleration is applied in the negative direction of the y axis, the result will be negative. If any acceleration other than the one in the desired axis direction is applied to the system, then the obtained value from the relation will be zero – although the value of any of the capacitors might change.

Besides, if the values of all the capacitors, due to any external factor (such as magnetic field), change similarly, the Cy is fixed and stable. For calculation of the applied acceleration in the x axis, as shown in Fig. 2, there are four capacitors C5, C6, C7, and C8. The total value of capacitor variation when acceleration is applied in the x axis direction can also be shown by a single parameter as follows:

$$C_x = C5 + C7 - (C6 + C8) \quad (8)$$

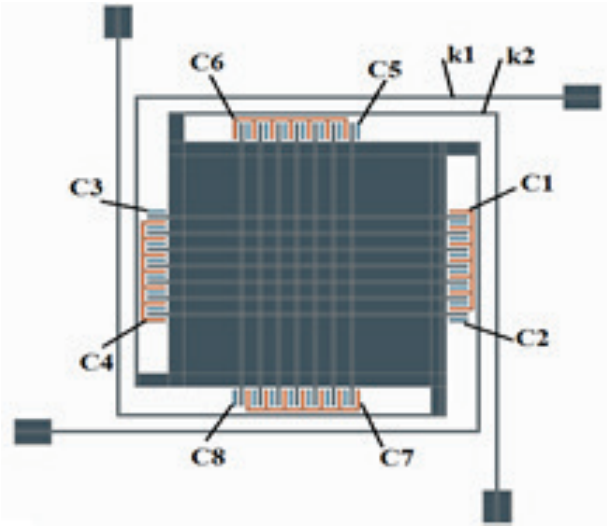

Figure 2: Acceleration measurement in the y axis direction

As said before, when acceleration is applied to one of the three axes directions, it exerts a zero effect on the other two axes. For example, if the acceleration is applied to the set in the x direction, the values of capacitors C5 and C7 increase (as the air distance between the two planes decreases) while the values of capacitors C6 and C8 decrease. Therefore, the Cx value would change from zero to a positive number in proportion to the applied acceleration. Moreover, since this value is positive, it can be inferred that the applied acceleration is in the positive direction of the x axis. A question might arise as what happens to the Cy value.

For all the four capacitors C1, C2, C3, and C4, the air distance would not change. The values of capacitors C1 and C2 are increased by increasing their overlapping. On the other hand, the values of capacitors C3 and C4 similarly decrease due to decreased overlapping surface, and so the Cy value does not change.

It is resulted that the acceleration applied in the x direction does not affect the Cy value. Here, it can also be shown that the acceleration used in each of the three axes directions has no effect on the measured capacitance for the other two axes directions.

For calculating the applied acceleration in z axis, there are two capacitors, which are formed using upper and lower surfaces of the mass bulk. There are also two fixed plates with air gap, which are placed at the ends

of the mass bulk and which complete the structure of the two capacitors. By Assuming that the capacitor between the upper surface of mass bulk and the upper fixed plane is C9 and the lower capacitor is C10, we have:

$$Cz = C9 - C10 \quad (9)$$

C_z is actually in proportion to the acceleration applied in the z axis direction. Here also, if acceleration is applied in the directions of the x and the y axes, C_z value remains unaffected.

3.2 Spring Design

Springs are components in the vibrational systems that react to the displacement, and since spring mass is insignificant compared to the main mass, this mass is usually disregarded. Force is generated in the spring when a relative displacement occurs in its two ends. For a linear spring, the spring force is proportional to the amount of deformation that is obtained from relation F = K * X, where F is the spring force, X the spring deformation amount (displacement of an end with respect to the other end of the spring), and K is the spring rigidity or spring constant.

Elastic elements, such as beams, act as a spring. For example, take a cantilevered beam with an end mass, m, as shown in Fig. 3. The beam mass (with respect to the mass m) has been disregarded.

Static deformation of the beam at its free end is expressed as follows:

$$\delta_{st} = \frac{WL^3}{3EI} \quad (10)$$

Where W=mg is the weight of mass m, E elasticity module, I inertia moment of cross section, and L is the beam length. Therefore, the spring constant is:

$$K = \frac{W}{\delta_{st}} = \frac{3EI}{L^3} \quad (11)$$

Therefore, the presented system in Fig. 3 can be considered a mass and spring system (Fig. 4), for which the value of the spring constant is calculated in relation 11 (Marek et al. 2005).

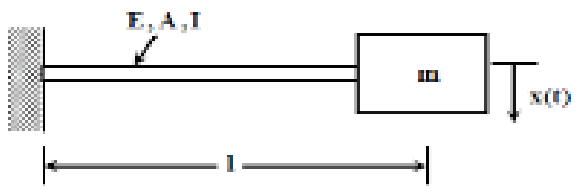

Figure 3: A cantilevered beam and mass of its end

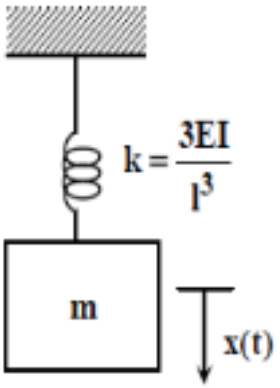

Figure 4: The mass and spring system (Beeby et al. 2004).

4 The complete structure of the suggested protocol

The upper schema of the complete structure of this protocol is given in Fig. 2. This structure, in addition to the combination of the capacitors said before, has four parallel springs, each of which is composed of two series springs. With regard to the explanations about spring designing, in calculations, the total rigidity of all the eight springs can be equated into one singular spring. The spring rigidity is calculated differently for each of the x, the y, and the z axes directions. In calculating spring rigidity in the z axis direction, springs k1 and k2 are series and their equivalent spring is parallel with three other similar springs. Here, first the movement perpendicular to the plane is calculated for one of the four springs. This movement is caused by three displacements: 1) displacement resulting from spring k1, 2) displacement resulting from spring k2, and c) displacement resulting from the torsion (due to the torque entered from k1 at the connection section of two springs) of spring k2, where the most displacement caused by it goes towards one end of spring k1 which is connected to the mass bulk. Regarding the spring rigidity equation for a cantilevered beam, the displacement due to spring k1 alone can be obtained from equation 12.

$$\delta_{k1} = \frac{pl_1^3}{3EI_1} \quad (12)$$

Where *p* is the imposed force from the mass bulk, and l, E, and I are respectively the length, Young's modulus (i.e., axial elastic modulus), and the inertia moment of

the spring (the index shows the spring number). In the same way, the displacement due to spring k2 alone can be obtained from equation 13.

$$\delta_{k2} = \frac{pl_2^3}{3EI_2} \tag{13}$$

Furthermore, the displacement due to the torsion (owing to the entered moment from k1 at the connecting point of the two springs) of spring k2 can be achieved from equation 14 (Bao and Yang, 2007).

$$\delta_\theta = \frac{p l_1^2 l_2}{G\beta b c^3} \tag{14}$$

In the above relation, *G, β, b,* and *c* are shear elastic modulus, constant coefficient from table, cross section, and thickness of the beam section related to spring k2, respectively. As such, the mass bulk displacement is produced from the sum of these three displacements. Since the spring rigidity is the ratio of the force on the displacement, we can obtain the spring rigidity of one of the four springs in the z axis direction as follows:

$$k_z = \frac{9EI_1I_2G\beta bc^3}{3G\beta bc^3\left(l_1^3I_2 + l_2^3I_1\right) + 9EI_1I_2l_1^3} \tag{15}$$

In this relation, I signifies the inertia moment of the cross section or the second surface torque, which is obtained from equation 16 (Beeby et al. 2004).

$$I = \frac{wt^3}{12} \tag{16}$$

In the above formula, *w* is the cross section and *t* is its thickness. By substitution of equation 16 into equation 15, the constant value of one of the four parallel springs in the z axis direction is achieved. Since the value of an equivalent spring for a number of parallel springs is obtained from the summation of their values, the final value of the equivalent spring in the z axis direction is equal to the value obtained for any of the springs:

$$K_z = \frac{12EG\beta bw_1t_1^3w_2t_2^3c^3}{G\beta bc^3\left(l_1^3w_2t_2^3 + l_2^3w_1t_1^3\right) + Ew_1t_1^3w_2t_2^3l_1^3} \tag{17}$$

For calculation of the spring constant in the x axis direction, Fig. 5 is considered which shows two of the total four springs. (Note that the calculation of the spring constant in this axis is completely different from that of the z axis. For example, while W_1 was formerly regarded as the beam width, it is here assumed as thickness since the direction of movement is perpendicular to the z axis.) These two springs are parallel but have dissimilar effects in the direction of x axis. Therefore, their constants must be separately calculated and added together. Due to the fact that the other two springs, versus the desired axis, are symmetrical and parallel to these two springs, it is simply enough to double the obtained value so that the spring constant along the x axis can be attained.

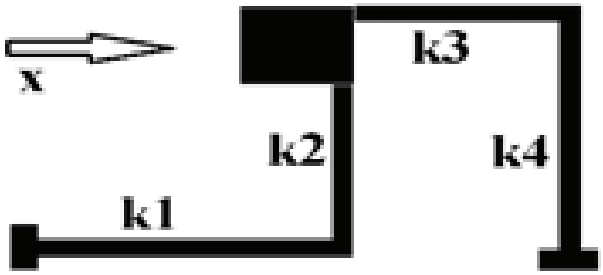

Figure 5: Two of the four influential springs in the x axis direction

Due to the existence of symmetry in this scheme, spring rigidity in the y axis direction is equal to that in the x axis direction. Hence, the equivalent spring rigidity in the direction of this axis can be written as follows:

$$K_{x,y} = 6E\frac{I_1I_2l_4^3 + I_4\left(I_1l_2^3 + 3I_2l_1l_2^2\right)}{l_4^3\left(I_1l_2^3 + 3I_2l_1l_2^2\right)} \tag{18}$$

5 Analysis of the suggested accelerometer

Up to now, the accelerometer structure has been designed. In this section, the suggested structure is analyzed. The analysis involves extraction of the natural frequency of the system along all the three axes, extraction of the output relations for the x and the y axes, as well as the extraction of output relations for the z axis.

5.1 Extraction of the natural frequency of the suggested accelerometer

By substituting the spring rigidity relations obtained in the previous section, the natural frequency of the system along all the three axes can be attained. For example, from equations 4 and 17, the natural frequency of the system in the z axis direction is:

$$f_z = \frac{1}{2\pi}\sqrt{\frac{12EG\beta bw_1t_1^3w_2t_2^3c^3}{G\beta bc^3\left(l_1^3w_2t_2^3 + l_2^3w_1t_1^3\right) + Ew_1t_1^3w_2t_2^3l_1^3}{m}} \tag{19}$$

Using equations 4 and 18, the natural frequency of the system in the x and the y axes directions is:

$$f_{x,y} = \frac{1}{2\pi}\sqrt{\frac{6E\dfrac{I_1 I_2 l_4^3 + I_4\left(I_1 l_2^3 + 3I_2 l_1 l_2^2\right)}{l_4^3\left(I_1 l_2^3 + 3I_2 l_1 l_2^2\right)}}{m}} \quad (20)$$

5.2 Extraction of output relations for the z axis

For calculation of the sensitivity, it is first required to calculate the capacitive changes due to displacement. In the z axis direction, two capacitors are used which are made by the upper and the lower planes between the main plane of the mass, which is mobile, and their values are calculated from equations 21 and 22 (Acar and Shkel. 2007).

$$C_{z1} = \frac{\varepsilon A_z}{d_z - z} \quad (21)$$

$$C_{z2} = \frac{\varepsilon A_z}{d_z + z} \quad (22)$$

Where A_z is the area of the plane that makes the capacitor between the main mass and the fixed planes for the formation of the z axis capacitor, d_z shows the original air distance (without applying acceleration), and z is the amount of displacement owing to the applied acceleration in this axis direction. Therefore, capacitor changes along the z axis is a result of the difference between these two values, and hence:

$$\Delta C_z = C_{z1} - C_{z2} \quad (23)$$

By substituting equations 21 and 22 into equation 23, we have

$$\Delta C_z = \varepsilon A_z \frac{2z}{d_z^2 - z^2} \quad (24)$$

Here, displacements which are much smaller than the original air distance are intended, and the term z^2 can be disregarded relative to d_z^2. In this context, the following relation can be expressed with a good approximation.

$$\Delta C_z = \frac{2\varepsilon A_z}{d_z^2} z \quad (25)$$

This relation shows that in the original displacements (as long as the amount of displacement relative to the original air distance is small), a linear relation exists between the capacitor changes and displacement in the z axis direction. Therefore, by replacing equations 17 and 25 into equation 5, the sensor sensitivity in the z axis direction can be achieved:

$$= \frac{\varepsilon A_Z m G \beta b c^3\left(l_1^3 w_2 t_2^3 + l_2^3 w_1 t_1^3\right) + E w_1 t_1^3 w_2 t_}{6EGbbw_1 t_1^3 w_2 t_2^3 c^3 d_Z^2} \quad (26)$$

From equation 26, it can be concluded that the accelerometer sensitivity depends on the original capacitor value, mass of the weight, original air distance, and the elements influencing the spring constant. If acceleration is applied in the z axis direction, the resulting displacement can be calculated as follows:

$$Z = \frac{m \times a_z}{k_z} \quad (27)$$

Where a_z is the applied acceleration, m is the weight mass, and k_z is the spring rigidity in the z axis direction which has been calculated above.

The mechanism for the accelerometer performance is that, by applying acceleration, the weight moves and resultantly the capacitive planes also move, which leads to the change of capacitance. Accordingly, by measuring the amounts of capacitor changes using a capacitor tester, one must be able to determine the amount of the applied acceleration. To do so, it is required to define a function in which capacitor changes are used as independent variable and its output value is the applied acceleration:

$$a_z = f\left(\Delta c_z\right) \quad (28)$$

To obtain such a relation, the spring rigidity from equation 17 is substituted in equation 27 and the value of acceleration is taken from equation 3, thus:

$$a_z = \frac{6d_z^2 EG\beta b w_1 t_1^3 w_2 t_2^3 c^3}{m\varepsilon A_z G\beta b c^3\left(l_1^3 w_2 t_2^3 + l_2^3 w_1 t_1^3\right) + E w_1 t_1^3 w_2 t_2^3 l_} \quad (29)$$

As is clear from the above relation, a linear relation exists between the applied acceleration and the capacitor changes, and by knowing the value of the capacitor changes, the applied acceleration can be calculated.

5.3 Extraction of output relations for the x and the y axes

Due to the existence of shape symmetry, calculations concerning the output relations for the x and the y axes are similar. As said before, the same springs, which

were used in the z axis direction, are simultaneously used for these two axes. This is a good advantage of the suggested protocol because it reduces the occupancy level of the scheme. Based on the explanations in the previous section, for calculating capacitor sensitivity, it is sufficient to calculate capacitor changes due to displacement. In the y axis direction, four capacitors are used. (In these relations, index y is used. For the x axis, the calculations are the same, and so they are not repeated.) The amounts of these four capacitors can be obtained from relations 30 to 33 (Acar and Shkel. 2007):

$$C_1 = \frac{\varepsilon n_f A_{sh}}{d_y - y} \tag{30}$$

$$C_2 = \frac{\varepsilon n_f A_{sh}}{d_y + y} \tag{31}$$

$$C_3 = \frac{\varepsilon n_f A_{sh}}{d_y - y} \tag{32}$$

$$C_4 = \frac{\varepsilon n_f A_{sh}}{d_y + y} \tag{33}$$

Where A_{sh} is the area of the plane forming the onecomb capacitor, d_y is the original air distance between the combs (without applying acceleration), y is the amount of displacement by applying acceleration in this axis direction, and n_f is the number of fingers on each side. Therefore, the capacitor changes in the y axis direction can be expressed as follows:

$$\Delta C_y = C_1 + C_3 - C_2 - C_4 \tag{34}$$

By substituting equations 30 to 33 into equation 34, we have:

$$C_y = \frac{4 n_f \varepsilon A_{sh} y}{d_y^2 - y^2} \tag{35}$$

Here also, displacements that are much smaller than the original air distance are attended and the term y^2 can be omitted relative to d_y^2. With a good approximation, we can write:

$$\Delta C_y = \frac{4 n_f \varepsilon A_{sh}}{d_y^2} y \tag{36}$$

With an argumentation similar to the calculations used for the z axis section, we can arrive at the sensitivity relation, and thus:

$$s_y = \frac{2 n_f \varepsilon A_{sh} m l_4^3 \left(I_1 l_2^3 + 3 I_2 l_1 l_2^2\right)}{3 d_y^2 E I_1 I_2 l_4^3 + I_4 \left(I_1 l_2^3 + 3 I_2 l_1 l_2^2\right)} \tag{37}$$

Similarly, a function can be defined here in a way that the capacitor changes are its independent variable and its output is the applied acceleration:

$$a_y = \frac{3 d_y^2 E I_1 I_2 l_4^3 + I_4 \left(I_1 l_2^3 + 3 I_2 l_1 l_2^2\right)}{2 m n_f \varepsilon A_{sh} l_4^3 \left(I_1 l_2^3 + 3 I_2 l_1 l_2^2\right)} \times \Delta c_y \tag{38}$$

6 Result and discussion

In this section, the proposed accelerometer simulation in Intellisuite software will be addressed, to prove the validity of the relationships extracted in the previous section. For this simulation, the dimensions of the various parts of this accelerometer were designed manually, with trial and error, and the results of this design are shown in Table 1. The output of the simulation is shown in Fig. 6. As can be seen in Fig. 6 and Table 1, the displacement value is 0.44μm due to the acceleration of 1000g, which is fully match with the results of the relationships presented in the previous section, thus proving the validity of the relationships extracted in this paper.

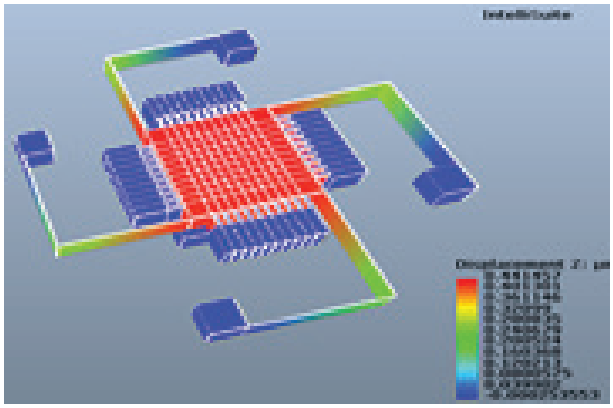

Figure 6: Simulation of the proposed accelerometer in Intellisuite software

So far, enough confidence has been gained that the analytical relationships are correct. We are now looking to extract the best possible dimensions for different parts of the accelerometer. An optimization algorithm is used for this purpose. In the suggested accelerometer, the mass bulk is square and hence a proper size must be found for its side. Therefore, the side of the mass bulk is a variable that needs to have the best value.

Table 1: Comparison between values obtained from analytical relationships and values obtained from simulation

	Movement with 1000g acceleration			Capacitor changes by applying 1000g acceleration			sensitivity
	X	Y	Z	X	Y	Z	Max.
Calculations	.44um	.44um	.44um	9.31pf	9.31pf	4.2p	9.31fF/g
simulation	.441um	.443um	.441um	9.3pf	9.28pf	4.19pf	9.3fF/g

The thickness of the mass bulk and of the spring must be equal so that the creation of this design can be accomplished. The value of this thickness is considered the second variable in this optimization. Besides, the width of the springs is assumed as the third variable. In order to facilitate the construction process, the widths of the two springs are presumed to be equal. The lengths of springs k1 and k2 are regarded as the fourth and the fifth variables, respectively, the values of which are highly influential in the accelerometer output.

In order to achieve the best values for the aforesaid variables, the present study has made use of multi-purpose optimization algorithm which is made of NSGA2 and SPEA algorithms – as presented in (Delfan Hemmati et al. 2012). This algorithm must search these five variables in a way that the best answers for the accelerometer characteristics can be found.

After running the algorithm, several answers were achieved, which are the members of Pareto front. The Pareto front members are some individuals from the population of each generation which are not overcome by any other member (that is, there is no other member in the population which is superior to them in terms of all the objective functions) (Delfan Hemmati et al. 2012). After running the shape algorithm, the Pareto front members are shown in the output (Fig. 7). In this figure, the horizontal axis (first target) shows the dynamic range and the vertical axis (second target) shows the sensitivity of each response. Out of all the individuals shown in Fig. 7, three answers have been selected, which are given in Table 2.

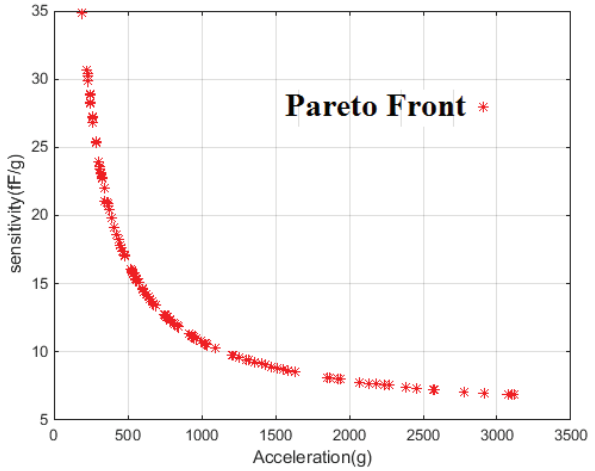

Figure 7: Members of the Pareto Front after optimization

Table 2: Optimization results

length and Width of Mass	Total Thickness	Width of Spring	Length of Spring 1	Length of Spring 2
697	57	41	196	199
699	53	40	261	230
697	44	32	343	378

Up to now, the values required for the five variables of mass bulk side, thickness, spring width, length of spring 1, and length of spring 2 have been obtained using the optimization algorithm. In Table 3, characteristics of the suggested accelerometer are compared to those of the previously designed accelerometers in the literature. As is observed, our proposed scheme has a good advantage over the previous ones recorded in the literature.

In order to confirm the correctness of the above relations, one of the optimization responses is here selected. This response has been completely simulated in the IntelliSuite software and the output results have been diagrammed as follows. By applying acceleration in all the three axes directions simultaneously in the range from - 1000 to + 1000, the value of displacement of the suspending mass is measured moment by moment – as shown in Fig. 8.

Moreover, the amount of the capacitance variations due to the displacement of the suspending mass is shown in Fig. 9. Obviously, displacements in the range below 0.5 microns are acceptable since the capacitors changes linearly in this range.

Fig. 10 shows the capacitance variations due to the application of acceleration in the z axis direction. In this figure, a comparison is made between the values obtained from optimization and the original values resulting from the trial and error. As shown in the figure, the original value of sensitivity in the z axis direction is 3.9fF/g which has hanged to 4.5fF/g after the optimization.

Furthermore, as is clear from Fig. 11, the amount of sensitivity in the x and the y axes directions has originally been 9fF/g, which has then changed to 10.6fF/g due to the optimization.

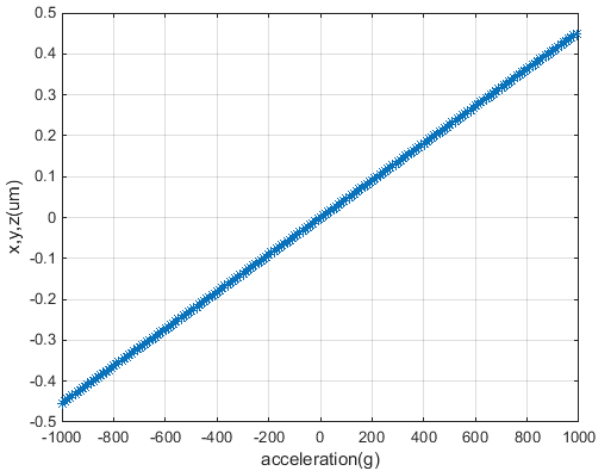

Figure 8: Displacement due to the application of acceleration in all the three axes directions

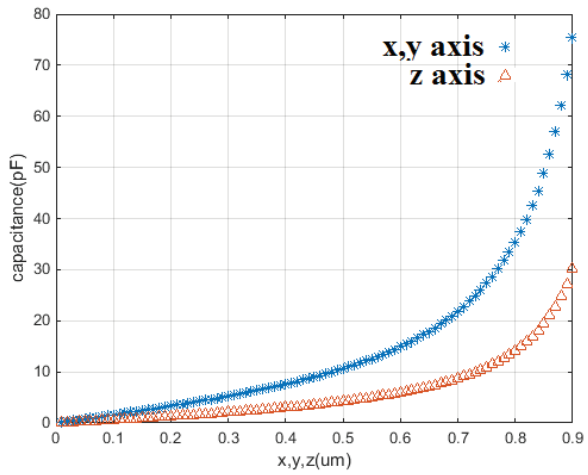

Figure 9: Capacitance variations by applying the displacement of the suspending mass

7 Conclusion

The present study has designed, analyzed, and optimized a new three-axis capacitor accelerator using microelectromechanical system technology. That a sensor can identify different acceleration directions, in addition to measuring them, is of paramount importance. In this structure, acceleration measurements in all the three axes directions are conducted along with the use of a mass and spring system, hence providing a high sensitivity, at the minimum occupancy level, without the loss of any other accelerometer factors. In designing this accelerometer, 10 capacitive groups are

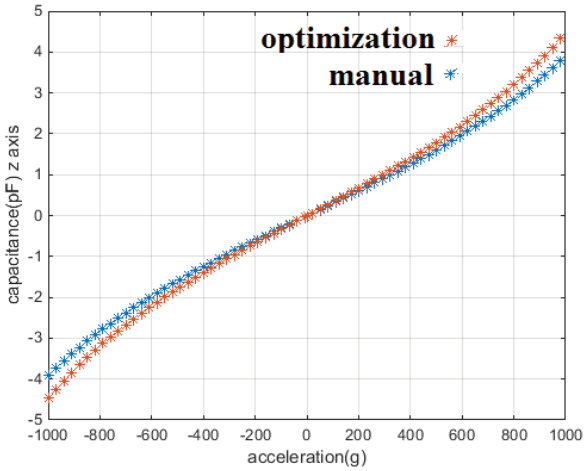

Figure 10: Capacitance variations after applying acceleration in the z axis direction

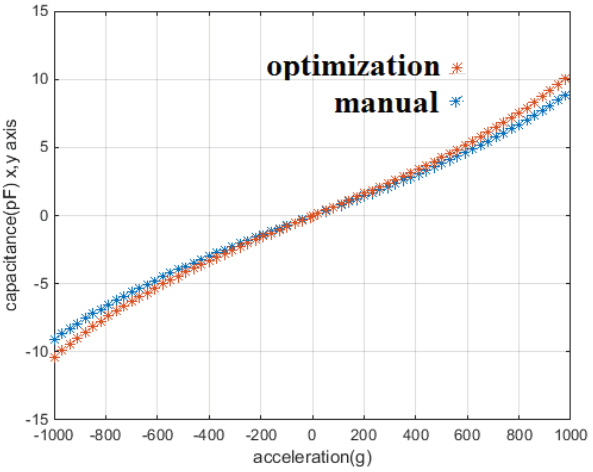

Figure 11: Capacitance changes after applying acceleration in the x and the y axes directions

employed, where two capacitors are used to calculate acceleration in the z axis direction and for each of the x and the y axes, four capacitive groups are considered. The reason for the use of different capacitive groups is that the sensor, in addition to measuring acceleration in each axis direction, can afford to realize the amount of acceleration of each axis separately and precisely. Besides, due to taking difference in this structure, the effect of the acceleration of each axis on the measured acceleration of the other axis is highly negligible. If an external factor such as electromagnetic waves changes the values of any singular capacitor, the original output of the capacitor measured for realizing the acceleration will not change. In other words, designing is done in such a way that the acceleration of each axis does not affect the other two axes, and yet the external factors cannot disrupt system performance. In this study, for determining the dimensions of the constituting parts

Table 3: Comparison of the suggested scheme with previous studies

Print Year	Range of X Axis	Range of Y Axis	Range of Z Axis	s fF/g	Area (mm^2)
2007–(Hamaguchi et al. 2007)	+-1g	+-1g	+-1g	1.08	1.14
2006- (Bais and Majlis, 2006).	0	0	+-5g	474	.92
2005-(Chae, et al.2005)	+-1g	+-1g	+-1g	6800	63
2009- (Zeimpekis and Kraft, (2009).	+-5g	0	0	9500	33.2
1996-(Chau et al.1996)	+-5g	0	0	1.2	0.42
2004- (Tsuchiya and Funabashi 2004)	0	0	+-500g	1.1	1.21
2005-(Bruschi et al. 2005)	+-100g	+-100g	0	2	1.51
2013-(Tavakoli, Sani, 2013)	+-66g	0	+-30g	10	1.16
2016-(Aydemir et al, 2016)	+-71g	+-71g	+-231g	21.6	56.6
This work1	+-1111g	+-1111g	+-1100g	9	1.2
This work2	+-2550	+-2550	+-2500	2.2	1.1
This work3	+-198	+-198	+-198	29	10.5

of the spring and the weight, the multi-objective optimization algorithm called NSGA2 has been adopted. This algorithm searches the five objectives, which are the dimensions of the elements, so that the best output results for the accelerometer can be obtained. Note that if any of the accelerometer factors such as dynamic range, operating frequency, and sensitivity is changed for a specific purpose, then the same structure can still be applied, and by using the suggested relations, only the geometric dimensions of the spring needs to be changed.

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MIDEM 2020

56th INTERNATIONAL CONFERENCE ON MICROELECTRONICS, DEVICES AND MATERIALS WITH THE WORKSHOP ON PERSONAL SENSOR FOR REMOTE HEALTH CARE MONITORING

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Hotel Jama, Postojna, Slovenia

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