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Voltage Mode Electronically Tunable Full-wave Rectifier

Predrag B. Petrović

University of Kragujevac, Faculty of Technical Sciences Čačak, Čačak, Serbia

Abstract: The paper presents a new realization of bipolar full-wave rectifier of input sinusoidal signals, employing one MO-CCCII (multiple output current controlled current conveyor), a zero-crossing detector (ZCD), and one resistor connected to a fixed potential. The circuit provides the operating frequency up to 10 MHz with increased linearity and precision in processing of low-level input voltage signal, with a very low harmonic distortion. The errors related to the signal processing and errors bound were investigated and provided in the paper. The PSpice simulations are depicted and agree well with the theoretical anticipation. The maximum power consumption of the converter is approximately 2.83 mW, at ±1.2 V supply voltages.

Keywords: bipolar transistor circuits; circuit analysis; circuit simulation; error analysis; rectifiers

Napetostni elektronsko nastavljiv polnovalni usmernik

Izvleček: Članek predstavlja novo realizacijo bipolarnega polnovalnega usmernika vhodnih sinusnih signalov z uporabo ene MO-CCCII (večizhodni tokovno krmiljen tokovni ojačevalnik), detektorja ničelnega prehoda (ZCD) in upora vezanih na fiksen potencial. Delovna frekvenca vezja je do 10 MHz z naraščajočo linearnostjo in natančnostjo v procesiranju nizko-nivojhih vhodnih napetostnih signalov z nizkim harmoničnim popačenjem. V članku so raziskane in predstavljene napake pri procesiranju signalov. Teoretična predvidevanja so potrjena s počjo PSPice simulacij. Največja poraba energije ojačevalnika je 2.83 mW pri napajalni napetosti ±1.2 V.

Ključne besede: vezja bipolarnega tranzistorja; analiza vezij; simulacije vezij; analiza napak; usmernik

** Corresponding Author's e-mail: predrag.petrovic@ftn.kg.ac.rs*

1 Introduction

Rectification is the essential and demanding aspect of signal processing in instrumentation, measurement and control. Rectifiers are widely applied in signal processing, signal–polarity detectors, amplitude modulated signal detectors, AC voltmeters and ampermeters, watt meters, RF demodulators, function fitting error measurements, RMS to DC conversions, sample and hold circuits, peak value detectors, clipper circuits [1-3], etc.. Owing to the threshold voltage of diodes, conventional diode rectifiers are limited and are only used in specific applications, such as DC voltage supplies. However, simple diode rectifiers cannot be used for applications requiring accuracy in the threshold voltage range. This can be overcome by using high precision integrated circuit rectifiers.

Although the use of current-mode (CM) active devices is restricted to current processing, it offers certain advantages such as higher usable gain, more reduced voltage excursion at sensitive nodes, greater linearity, lower power consumption, wider bandwidth, better accuracy and larger dynamic range compared to that of their voltage-mode counterparts. The CCII is a reported active component, especially suitable for the class of analog signal processing. However, the CCII cannot control the parasitic resistance at x (R_x) port, therefore – when it is used in some circuits, it inevitably requires external passive components, especially resistors [2]. This makes it inappropriate for IC implementation, as it occupies a greater chip area, high power dissipation and excludes electronic controllability. On the other hand, the recently introduced second-generation current controlled conveyor (CCCII) has the advantage of electronic adjustability over the CCII [4]. Also, the use of dual-output current-conveyors is found to be useful in the derivation of current-mode single input circuits.

In order to improve performance of OA-based circuits the use of the current conveyor was proposed in [5]. The full-wave rectifier [6], with a single three-output CCCII, two MOS transistors and a resistor with large cross-over distortion, was able to perform rectification at lower frequencies, e.g. 5 kHz. The papers [7-8] described full-wave rectifier circuits based on usage of two second-generation current conveyors (CCIIs) and four diodes. The rectifier circuits [9-10] offer a wide dynamic range and show a broadband operation thanks to the use of a CMOS class AB amplifier and current rectifier operation. The rectifier capable of providing output voltages nearly at the level of the input voltage combined with low power consumption is described in [11], which was also achieved through the circuit design proposed here. In [11], CMOS integrated active rectifier concept as an innovative approach for higher efficiencies is used.

A full-wave rectifier proposed in [12] is based on the usage of two plus-type second-generation current conveyors (CCII+s) and three MOSFETs. A voltage-mode (VM) rectifier with high-input impedance using dual-X current conveyors (DXCCII) and three MOSFETs, without passive components, is described in [13]. In [14], the current-mode (CM) rectifier uses two CCII+s and four diodes. The CM rectifier based on one current conveyor and one universal voltage conveyor (UVC) and two diodes is introduced in [15]. The circuits proposed in [16] employ at least two current and/or voltage conveyors as active elements and two diodes, and works in CM. A CM full-wave rectifier circuit with one active element – current differencing transconductance amplifier (CDTA) and four diodes and one resistor is reported in [17]. The circuits proposed in [18-19] are designed based on MOS transistors with fairly simple structure. The rectifier [18] requires a floating input voltage source, while the circuit [19] needs three external bias current sources to be realized separately. The circuits in [20], [21] use CDTA or DXCCII which have more complex internal structures with respect to CCII and DVCC. A CM full-wave rectifier based on a single modified Z-copy current difference transconductance amplifier (MZC-CDTA) and two switches is reported in [22].

This paper presents the principles of operation, and the detailed circuit design of the new bipolar realization of the full-wave rectifier. The features of the proposed circuit are: it employs one MO-CCCII, one zero-crossing detector, and one resistor connected to source voltage, which is suitable for fabrication in a monolithic chip. Unlike the rectifier described in [2-3], which was realized using the CMOS technology, the one described in this paper involves a simpler and more accurate control structure. Besides, the proposed circuit does not require a more precise bias voltages realization and complex transistor pairing, which was typical of the realizations described in [2-3]. The rectifier circuit provides the operating frequency of up to 10 MHz, with increased linearity and precision in processing of low level input voltage signals. The performance of the proposed circuit is illustrated by PSpice simulations, showing a good agreement with the calculation. The circuits proposed in this paper have been compared to similar circuits reported in literature.

2 Proposed full-wave rectifier circuits

Fig. 1 presents the proposed circuit of the full-wave rectifier.

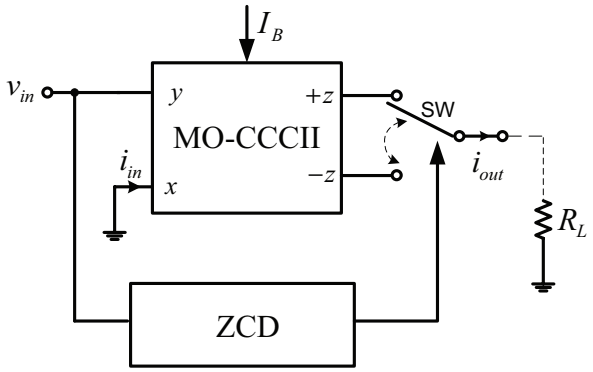


Figure 1: The proposed circuit of the full-wave rectifier

Conceptually, the rectifier presented in Fig. 1 is very similar to the one proposed in [6], the former, however, having more precise and new zero-crossing detection (ZCD) circuits, and without shunting of the high output of MO-CCCII. The proposed ZCD circuits demand considerably less resistance in the output stage (50 times) compared to the realization in [6]. This modification ensures greater linearity rectification within a wider frequency range. Additionally, this configuration imposes no limitations in realization of the analog switch, contrary to the circuit described in [6].

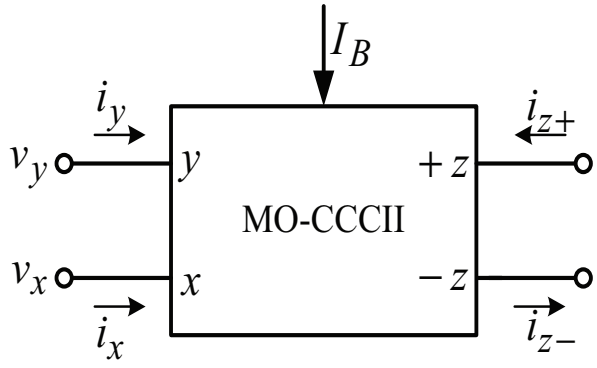


Figure 2: Electrical symbol of MO-CCCII

Generally, a MO-CCCII is a multiple-terminal active building block, as shown in Fig. 1. The electrical symbol of the MO-CCCII is shown in Fig. 2.

The port relations of the MO-CCCII can be presented by the following equation:

$$i_y = 0; v_x = v_y + i_x R_x; i_{z+} = +i_x; i_{z-} = -i_x \quad (1)$$

The schematic bipolar realization is shown in Fig. 3 [23]. According to equation (1), the MO-CCCII has a unity voltage gain between terminal *y* and *x* and a unity current gain between terminal *x* and *z*. The R_x is an inner resistance of a translinear mixed loop (Q_1 to Q_4) with grounded resistor equivalent controlled by bias current I_B. In this case, the parasitic resistance R_x at the terminal *x* can be expressed by:

$$R_x = \frac{V_T}{2I_B} \quad (2)$$

where V_T=26 mV at 27° C is the usual thermal voltage given by *kT/q*, *k*=Boltzmann's constant=1.38×10-23 J/K, *T*=the absolute temperature (in Kelvin's), and *q*= 1.6×10-19 C and I_B (Fig. 1) is the bias current of the conveyor which remains tunable over several decades.

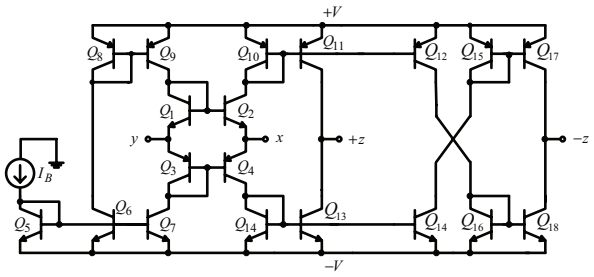


Figure 3: Bipolar realization of MO-CCCII

Precision in processing of the input voltage signal is directly dependent on the manner in which ZCD is able to reliably detect the moment when the input signal changes the polarity. This required the construction of new bipolar detector circuits, as shown in Fig. 4. The transistors Q_{19} and Q_{20} will promptly follow the variations in input voltage, thus reducing the total delay time of the comparator. The resistor R_1 has one end attached to the source from which it is powered together with the detectors. The resistor can be coupled to the source of a different voltage level, if this should prove necessary due to the demands of analog switches (realized with two complementary MOS transistors).

By the routine analysis of the proposed full-wave circuit shown in Fig. 1 and using the properties of MO-CCCII, for v_{in}>0, the *z*+ current (v_{in}/R_x) to pass on to the load. For v_{in}<0, *z*– current ($-v_{in}/R_x$) passes on to the load, thus inverting the negative cycle of input:

$$i_{out} = i_{z+} = \frac{v_{in}}{R_x}, \quad v_{in}(t) \geq 0 \quad (3)$$

$$i_{out} = i_{z-} = -\frac{v_{in}}{R_x}, \quad v_{in}(t) < 0 \quad (4)$$

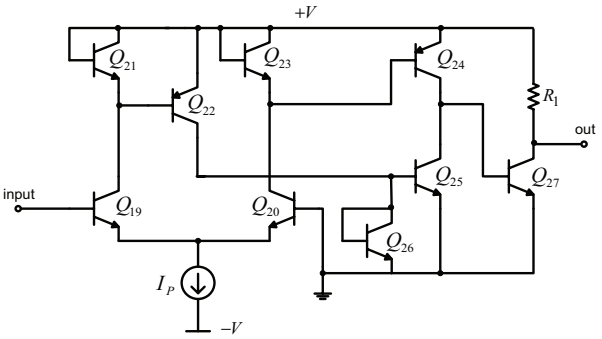


Figure 4: Bipolar realization of comparator

Unidirectional current flows through the load in either case, resulting in a full-wave rectified output.

Depending on the detected sign of the input signal (practically by detecting the negative half-period of input processing signal), over the ZCD (Fig. 1), the position of the switch SW (two complementary MOS transistors) can be determined. The control voltage signal, obtained on the output of the ZCD, defines the position of the switch SW and brings the current either from port *z*+, or from port *z*- of the MO-CCCII. Such control enables the current input from the port *z*+ on the load at the interval at which the input voltage signal is positive, i.e. from the port *z*- when the input voltage is negative. The output voltage v_{out} for input v_{in} is as follows:

$$v_{out} = \frac{R_L}{R_{in}} v_{in}; \quad v_{in} \geq 0 \quad (5)$$

$$v_{out} = -\frac{R_L}{R_{in}} v_{in}; v_{in} < 0 \quad (6)$$

where R_{in}=R_x. The equations (5) and (6) can be presented in form:

$$v_{out} = \frac{R_L}{R_{in}} |v_{in}| \quad (7)$$

Based on (7), it is obvious that the voltage value at the output of the proposed circuit corresponds to the rectified value of the input sinusoid signal with amplification or rectifier with attenuation. In the proposed

circuit, rectification is not performed by diodes, which implies fewer ripples, compared with the known diode rectifier circuits [14-17]. It is also possible to perform low-voltage (below threshold level of the diode) rectification using the proposed circuit.

3 Non-ideal Effects

The effects of MO-CCCII and comparator non-idealities on the full-wave rectifier performance are to be considered in this section. By considering the non-ideal MO-CCCII characteristics, equation (1) can be rewritten as:

$$i_y = 0; v_x = \alpha v_y + i_x R_x; i_{z+} = +\beta_p i_x; i_{z-} = -\beta_n i_x \quad (8)$$

where α=1-ε_v and ε_v ($|\varepsilon_v|$<<1) represents the voltage tracking error from y to x terminal, β_p=1-ε_p and ε_p ($|\varepsilon_p|$<<1) denotes the current tracking error from x to z+ terminal, while β_n=1-ε_n and ε_n ($|\varepsilon_n|$<<1) stands for the current tracking error from x to z- terminal of the MO-CCCII, respectively. Generally, these tracking factors remain constant and frequency independent within low to medium frequency ranges. Typical values of the non-ideal current transfer gains and the transconductance inaccuracy factor α, β_p and β_n range from 0.9 to 1, with an ideal value of 1. However, at higher frequencies these tracking factors become frequency dependent. Given the non-idealities, currents generated from MO-CCCII can be defined as:

$$i'_{out} = i_{z-} - i_{z+} = (\beta_p - \beta_n)\frac{\alpha v_{in}}{R_{in}} \quad (9)$$

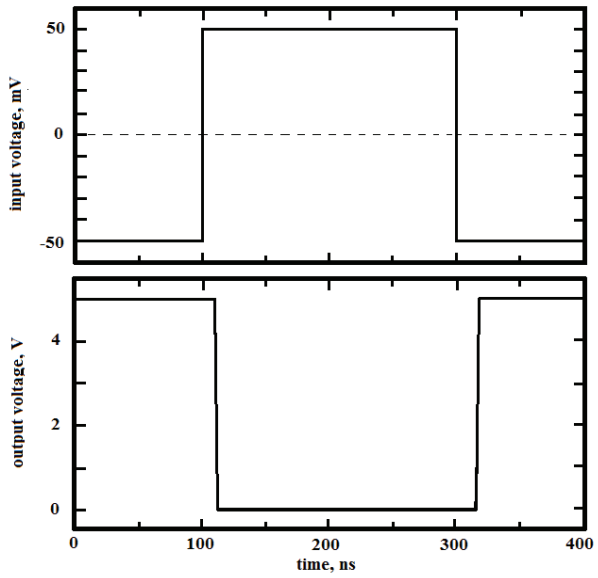
$$i'_{out} = 2\beta_p \frac{\alpha v_{in}}{V_T} I_B = 2\beta_p q \frac{\alpha v_{in}}{kT} I_B, \qquad v_{in}(t) \geq 0 \quad (10)$$

$$i'_{out} = -2\beta_n \frac{\alpha v_{in}}{V_T} I_B = -2\beta_n q \frac{\alpha v_{in}}{kT} I_B, \quad v_{in}(t) < 0 \quad (11)$$

which results in an absolute error as:

$$Error = \left| i_{out} - i'_{out} \right| \quad (12)$$

As for equations (10) and (11), the tracking errors slightly change the output current of the proposed full-wave circuits. However, the above relation does not include error when determining the interval in which the input voltage signal is negative (the ZCD error), which also defines the precision of the proposed rectification process. Fig. 5 a) shows the waveform of the output voltage in response to an input voltage step of ±50mV for the proposed comparator. In Fig. 5 b), the average delay times of the proposed comparator as a function of the input voltage amplitude is reported. As can be seen, at low input voltages, the response time of the proposed circuit is very small. The higher the input voltage, the lower the delay time, as the enhanced output voltage swing (due to the higher voltage values) causes Q_{19} and Q_{20} to completely turn-off. Simulation results confirm the fact that the proposed ZCD circuits are capable of high precision processing of the input signal. It is assumed that the incremental sensitivities of the output current i_{out} at parameters α, β_p, β_n and T are: 1; 1; 1 and -1 (all the active and passive sensitivities are of an equal unity in magnitude). Thus, the proposed circuit exhibits a low sensitivity performance.



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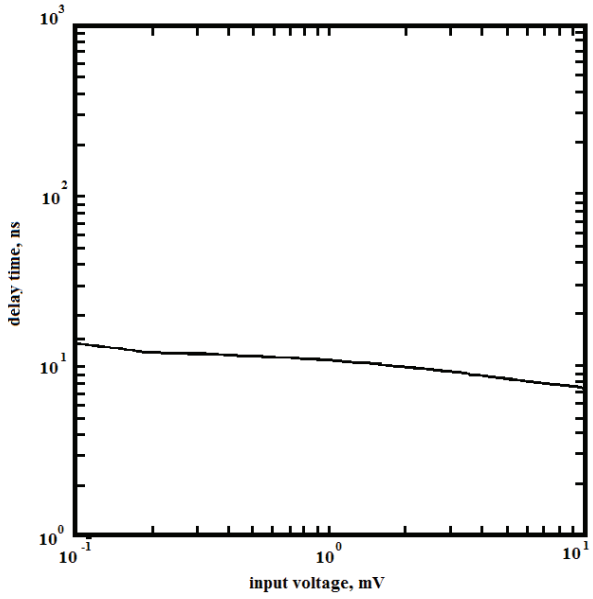


b)

Figure 5: a) Output voltage waveforms for proposed ZCD, b) Average delays time against input voltage

The error (12) is a function of input voltage signals and varies depending on its content. A way to express the error is to consider the values of the observed parameters as random quantities characterized by their PDFs (Probability Density Function). Therefore, the interval having a 2ε width, around the nominal value of the observed parameters needs to be defined and associated with a certain distribution, e.g. uniform distribution.

The Monte Carlo approach [24] gives the lower and upper limits of interval which contains 95% of error samples. The Monte Carlo analysis in PSpice was used for simulations with a given error on different parameters and components (Monte Carlo predicts the behaviour of a circuit statistically when part values are varied within their tolerance range by 5%), Fig. 6. This test is very useful for visualizing how a circuit runs with imperfect parameters as are used in reality. The number of individual simulation was 2000.

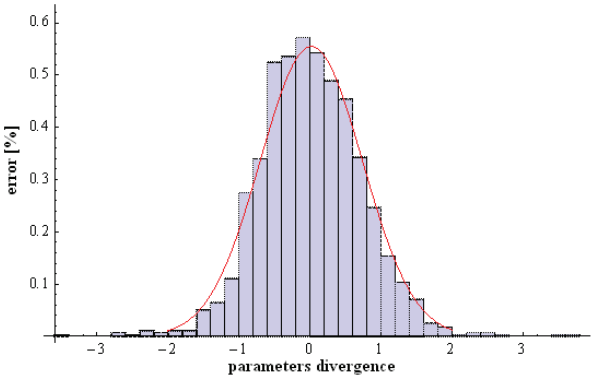


Figure 6. The distribution of errors, for the divergence in the value of the parameters, from their nominal values

4 Simulation Results

To confirm the given theoretical analysis, the proposed voltage-mode bipolar full-wave circuit in Fig. 1 was simulated using the PSpice program. The MO-CCCII and ZCD were realized by the schematic bipolar implementations given in Figs. 3 and 4, with the transistor model parameters of PR200N (PNP) and NP200N (NPN) of the bipolar arrays ALA400 from AT&T [25], Table 1. The supply voltages and the values of the bias currents were +V=–V=1.2 V and I_p=300 μA respectively, whereas the input voltage was within the range of ±100 mV. Parameters of National Semiconductor circuits AH510 [26] were used as analog current switch during simulation.

Table 1: PR200N and NP200N transistor parameters

Transistor type: NP200N
.MODEL NX2 NPN RB = 262.5 IRB = 0 RBM = 12.5 RC = 25 RE = 0.5 IS = 242E - 18 EG = 1.206 XTI = 2 XTB = 1.538 BF = 137.5 IKF = 13.94E - 3 NF = 1.0 VAF = 159.4 ISE = 72E - 16 NE = 1.713 BR = 0.7258 IKR = 4.396E - 3 NR = 1.0 VAR = 10.73 ISC = 0 NC = 2 + TF = 0.425E - 9 TR = 0.425E - 8 CJE = 0.428E - 12 VJE = 0.5 MJE = 0.28 CJC = 1.97E - 13 VJC = 0.5 MJC = 0.3 XCJC = 0.065 CJS = 1.17E - 12 VJS = 0.64 MJS = 0.4 FC = 0.5
Transistor type: PR200N
.MODEL PX2 PNP RB = 163.5 IRB = 0 RBM = 12.27 RC = 25 RE = 1.5 IS = 147E - 18 EG = 1.206 XTI = 1.7 XTB = 1.866 BF = 110.0 IKF = 4.718E - 3 NF = 1 VAF = 51.8 ISE = 50.2E - 16 NE = 1.65 BR = 0.4745 IKR = 12.96E - 3 NR = 1 VAR = 9.96 ISC = 0 NC = 2 TF = 0.610E - 9 TR = 0.610E - 8 CJE = 0.36E - 12 VJE = 0.5 MJE = 0.28 CJC = 0.328E - 12 VJC = 0.8 MJC = 0.4 XCJC = 0.074 CJS = 1.39E - 12 VJS = 0.55 MJS = 0.35 FC = 0.5

Time response of the proposed ZCD circuits is shown in Fig. 7, where the input voltage signal is of 1 MHz frequency and 20 mV peak. Resistor R_1=1 kΩ was used in the simulation process. This clearly infers that the proposed solution detectors are able to sense polarity of the input voltage signal with high precision, whereby the error resulting from imprecision in detection is negligible in practical applications.

The DC characteristic of the proposed circuit at a frequency of 1 MHz is shown in Fig. 8. Fig. 8 implies that

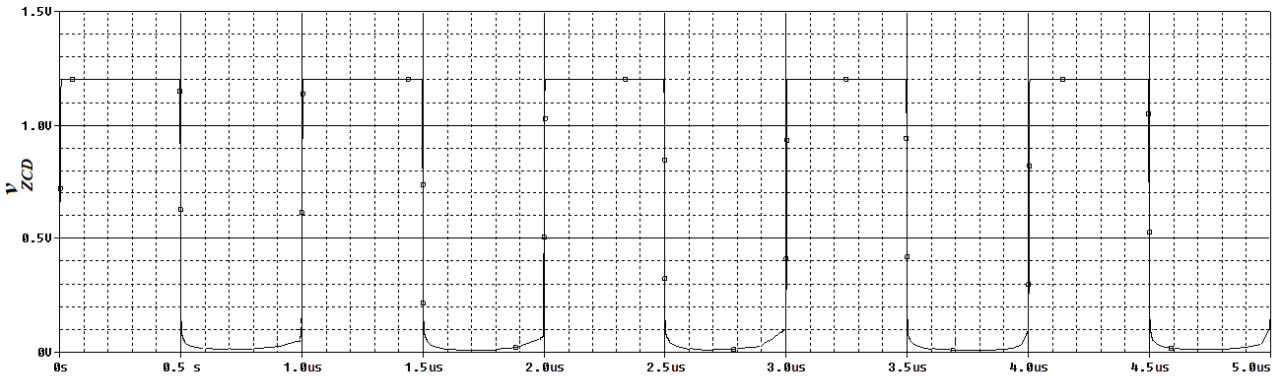


Figure 7: Time-domain response of proposed ZCD

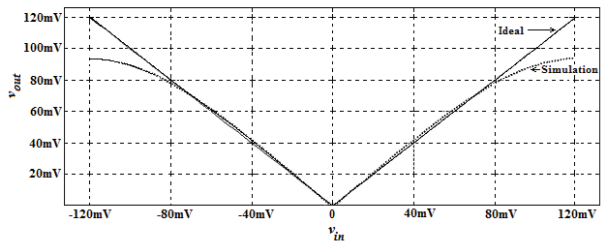
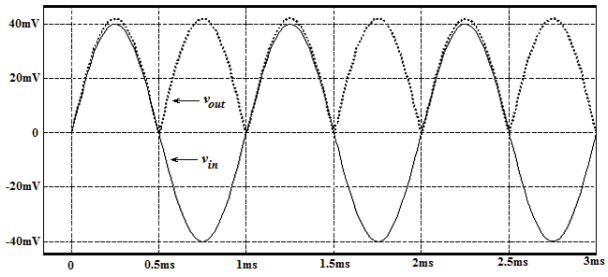


Figure 8: DC transfer characteristics for the proposed rectifier circuit

the proposed circuit retains a linear character in a wide voltage range.

Fig. 9 shows the wave form of the signal at the output of the circuit shown in Fig. 1 (voltage v_{out}), at different frequencies. For these simulations, the input signal is taken as a sinusoidal voltage signal at 40 mV peak value, the selected frequencies ranging from 1 kHz to 10 MHz. Fig. 9 shows that the output waveform of the proposed rectifier is in a good agreement with the theoretical ones at low and high frequencies. However, the higher the frequency of the processed signal, the greater the deviations.

The total power dissipation was 2.83 mW. Low power consumption of the proposed circuits occurs due to the application of low-voltage current mode and transconductance mode integrated circuits, along with the use of bipolar transistor technique. Applying the current mode signal processing to solve the issues under consideration is a sensible approach to the problem. However, similar and sometimes lower power consumption can be achieved using CMOS technology instead of the bipolar one.



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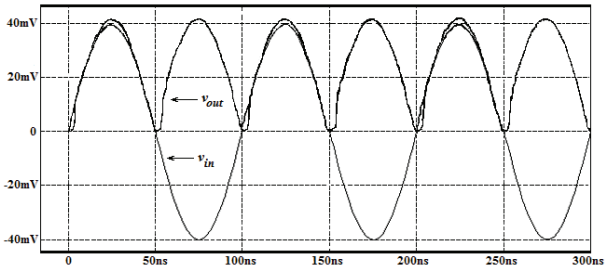

a)

Figure 9: Time-domain response of the proposed full-wave rectifier for different frequencies of a) 1 kHz and b) 10 MHz

To test the tunability of the gain of the proposed rectifier circuit, the bias current of the MO-CCCI (I_B) is changed and the results are shown in Fig. 10. For these simulations, the input signal is taken as a sinusoidal voltage signal with 100 kHz frequency and 50 mV peak value at a load of R_L=100 Ω.

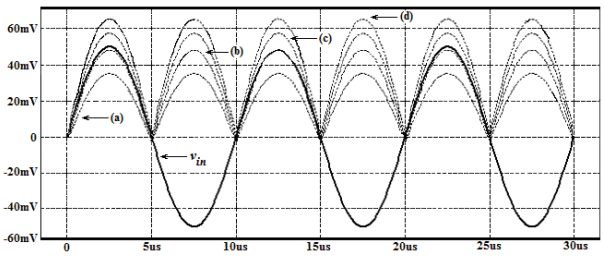

Figure 10: Tunability of the gain of the proposed rectifier with changing the bias current I_B a) I_B=200 μA; b) I_B=130 μA; c) I_B=115 μA; d) I_B=100 μA

4.1 Harmonic distortion

A further indication of the performance of each of the full-wave rectifiers can be gleaned by examining the distortion already present in a full-wave rectified signal. When a sinusoidal signal of frequency *f* is applied to a full-wave rectifier, the steady-state response at the output ideally consists of harmonic components at 2*f*, 4*f*, 6*f*, etc. [2]. The harmonics in the signal causes the distortion in the output of the circuit. Because of its periodic nature, these harmonic components can be analyzed by the Fourier series (with fast Fourier transform using PSpice).

In the case of a full-wave rectifier, the steady-state response at the output consists of even harmonics. Fig. 11 shows the total harmonic distortion of the output voltage of the proposed circuit, Fig. 1. The THD of the proposed circuit is -15.6 dB at 50 Hz and -20.8 dB at 1

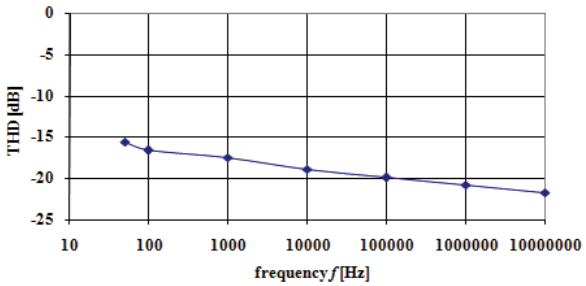

Figure 11: Total harmonic distortion (THD) versus frequency at input amplitude voltage of 50mV

MHz with an input signal of 50 mV. The THD is significantly lower than in [2], [27], [28] (the THD of previously reported circuit slowly increases with frequency), because of higher frequency ranges, the diode switching ON and OFF tends to become sluggish due to its higher impendence and more distortions.

4.2 Comparison with the Existing Circuits

To gain a better insight into the technique proposed here, the performance of the proposed circuits was compared to the previous one implementing full-wave rectifiers. Table 2 summarizes this comparison by showing some important parameters of the rectifiers. It should be assumed here that not all of the comparison realizations rely on the concept of a voltage-mode circuit, as is the one proposed in this paper.

The proposed rectifier requires fewer active components than the one described in [2], [22], [27], [31], along with lower THD of the output voltage and lower consumption. Additionally, the circuit described in this paper enables electronic control of the gain of the proposed rectifier circuit (amplitude of the output voltage signal).

5 Conclusion

In this paper, new full-wave rectifier topologies are given. The circuit employs only two active components and one resistor operating in VM, which is advantageous from the integration point of view. The performance of the proposed circuits is demonstrated by PSpice simulations using the bipolar arrays ALA400 from AT&T technology parameters. The effects of the non-idealities of the active elements are also investigated. The proposed circuit has a high precision and linearity, low power consumption and wide bandwidth.

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Table 2: Comparison of performance of different rectifiers

Ref.	Type of active building blocks used	Number of diodes	Number of resistors	Auxiliary bias sources	Maximum frequency	Maximum amplitude	Power consumption
[2]	4 CCCII, 3 MOS	-	-	yes	20 MHz	±1 V	9.43 mW
[6]	1 CCCII, 2 MOS	-	1	no	100 kHz	±10 mV	-
[12]	2 CCIIs, 3 MOS	-	-	no	22 MHz	±50 mV	-
[13]	1 DXCCII, 3MOS	-	-	yes	10 MHz	±150 mV	3.33 mW
[14]	2 CCIIs	4	2	no	10 kHz	3 V	-
[15]	1 CCIIs, 1 UVCs	2	-	no	500 kHz	±200 mA	1.19 mW
[16]	1 CCIIs, 1 UVCs	2	-	yes	1 MHz	±300 mV	-
[17]	1 CDTAs	4	1	no	10 MHz	±1 mA	-
[20]	1 CDTAs	2	1	no	Variable up to 42 MHz	±5 mA	-
[21]	1 DXCCIIs	2	1	no	1 MHz	±500 mV	-
[22]	1 MZC-CDTA, 2 MOS	-	-	no	10 MHz	±300 mA	14 mW
[27]	3OA, 3 AD633/AD	1	9	no	1 MHz	±5 V	-
[28]	3 CCCII	-	5	yes	5 MHz	±500 mV	-
[29]	1 OTA/1 DVCC	2	2/3	no	1 MHz	±200 mA	-
[30]	1 CDTA	4	-	yes	1 GHz	±210 µA	6.31 mW
[31]	1 CCII, 1 DXCCII	2	2	no	1 MHz	±350 mV	-
[32]	47 MOS, 9 CS	-	1	no	100 MHz	±200 mV	5.2 mW
[33]	2 CCII	2	3	yes	10 MHz	±1 V	-
This work	1 DOCCCIIs, ZCD, 2 MOS	-	1	no	10 MHz	±100 mV	2.83 mW

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