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Journal of Microelectronics, Electronic Components and Materials

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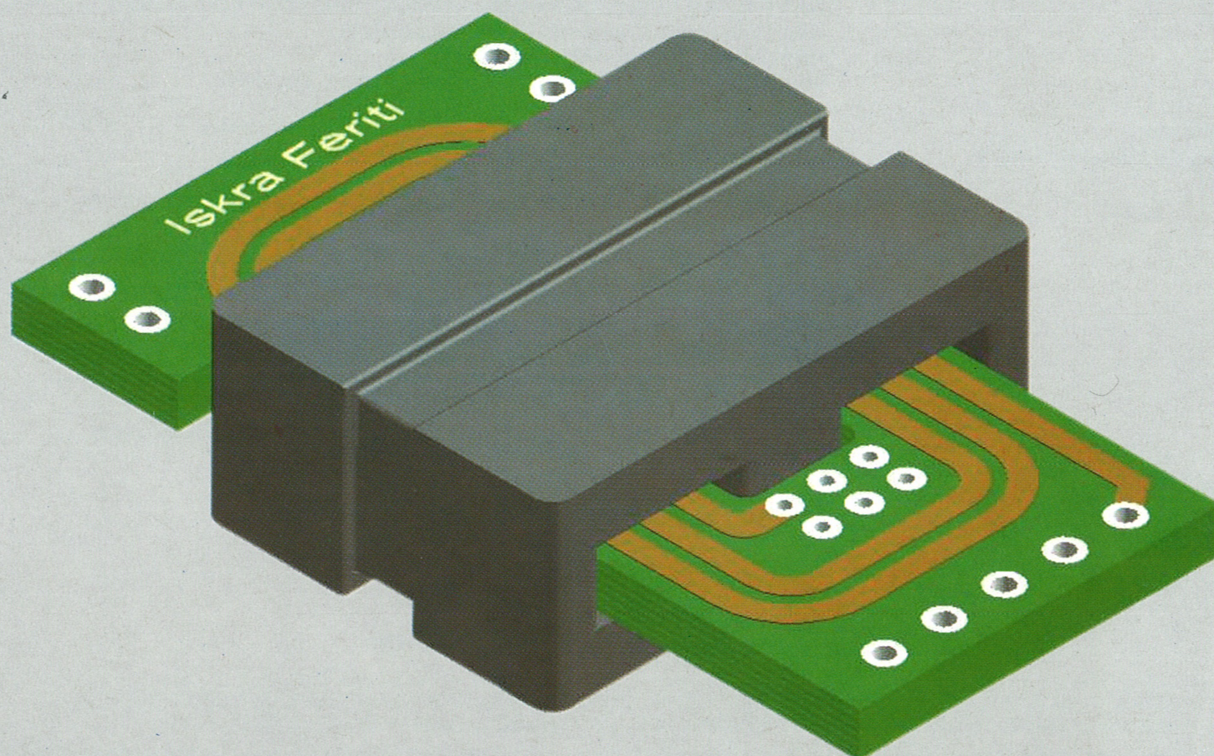

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ION IMPLANTATION; A MODERN TOOL OF SURFACE ENGINEERING

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Keywords: surface engineering, modern mehods, ion implantation, PSII, Plasma Source Ion Implantation, ion doping, vacuum, thin films, ions, ion beams, kinetic energy, depth of penetration, collisions, irradiation damages, IM, Ion Mixing, high energy irradiation, LSS theory, Lindhard, Scharff and Schiott theory, PKA, Primary Knock-on Atoms, TRIM code

Abstract: Ion implantation is a doping technique which uses energetic ion beams as vector of mass transport. The atoms to be implanted (often called impurity atoms) are thus ionized, accelerated, selected and directed towards the target. Due to the high kinetic energy (typically tens to hundreds of keV) the accelerated ions penetrate the target up to the depths from tens to thousands of nanometers. This method allows one to dope virtually all solids with any kind of atoms with high uniformity and up to very high concentrations. The basic principles, advantages and drawbacks as well as possible fields of applications of ion implantation technique are briefly presented.

Ionska implantacija, sodobna metoda za obdelavo površin

Ključne besede: obdelava površin, metode sodobne, implantacija ionov, PSII implantacija ionov iz virov plazme, dopiranje ionov, vakuum, plasti tanke, ioni, curki ionov, energija kinetična, globina prodiranja, trki, poškodbe vsled obsevanja, IM mešanje ionsko, obsevanje visokoenergijsko, LSS teorija Lindhard, Scharff and Schiott, PKA satomi izbiti prvotno, TRIM koda

Povzetek: Ionska implantacija je tehnika dopiranja, ki za prenos mase uporablja curke energetskih ionov. Atome, ki jih želimo implantirati, najprej ioniziramo, pospešimo, preberemo in usmerimo proti tarči. Zaradi njihove visoke energije (značilno desetine ali stotine keV) ioni prodrejo v tarčo do globine od nekaj deset do nekaj tisoč nanometrov. Metoda omogoča dopiranje praktično katerekoli trdne snovi s katerimikoli atomi do zelo visoke vsebnosti. Temeljne zakonitosti, prednosti in pomanjkljivosti, pa tudi možna področja uporabe te tehnike na kratko opisujemo v tem članku

1. Introduction; the history of ion implantation.

The beginnings of ion implantation are related to the Manhattan Project. Searching for the efficient method of fission isotopes production the scientists tested also the technique of mass separation of accelerated ions in magnetic field. This method was found less efficient than the diffusional and centrifugal isotope enrichment, however, the interest was attracted by the modification of the properties of target on which ions were collected. The observation that accelerated atoms are not deposited on the target surface but penetrate into its crystalline structure becamed a basis of ion implantation.

The rapid development of ion implantation in late sixties is mainly due to the emerging semiconductor industry. From technological point of view main characteristics of implantation such as: high uniformity, precision, repetability and low processing temperature resulted in the wide use of implantation for silicon doping. Till now this technique remains the basic doping method in silicon technology.

In early seventeens the development in the construction of industrial ion implanters required for efficient doping of bipolar devices resulted in high current implanters delivering ion beams in milliampers range. This made possible high dose implantations what opened new areas of applications, namely the modification of composition of metals. Quite soon the research projects devoted to study the effects of ion implantation into metals allowed to determine the beneficial role of nitrogen implanted into ferritic steels. This in turn resulted in the construction of dedicated implanters without mass separation but equipped with specialized target chambers containing manipulators permitting the homogenous treatment of details of complicated shapes. The huge market for the improvement of mechanical properties of tools leaded to a rapid development of this particular application, however, till now ion implantation into metals is used only in niche domains, mainly biomedical or highly precise cutting and forming tools.

Despite two main fields of applications, semiconductors and metals, ion implantation is also used for several specific purposes. Among them the fabrication of micrometer size membranes, optoelectronic and catalytic devices fabrication seems to be of particular interest. Recently, a new promising field of applications was identified, namely ion implantation into polymers. Low irradiation doses required and strong effects observed after implantation into polymers made this idea very promising.

The above description deals with classical ion implantation, i.e. the line-of-sight processes carried out at energy range of tens to hundreds of keV. Recently numerous new techniques have emerged from ion implantation such as: ion beam mixing, plasma source ion implantation or high energy ion irradiation. These methods will be shortly presented later on.

2. Description of the method.

2.1 Interaction of energetic ions with solids

Energetic ions when penetrate the solid target loose their energy in elastic collisions with target nuclei (so called nuclear stopping, S_n) and in inelastic collisions with the electrons (electronic stopping, S_e) /1/. The stopping is defined as:

$$S = dE/dx$$

where E is ion energy and x the length measured along the ion path in solid (total range) or along the beam direction (projected range). The dependence of stopping versus ion velocity is presented in Fig. 1. The important feature of these dependencies is that for high velocity the ion losses its energy mainly in collisons with target electrons, whereas at the end of the path, when the ion energy decreases the collisions with target

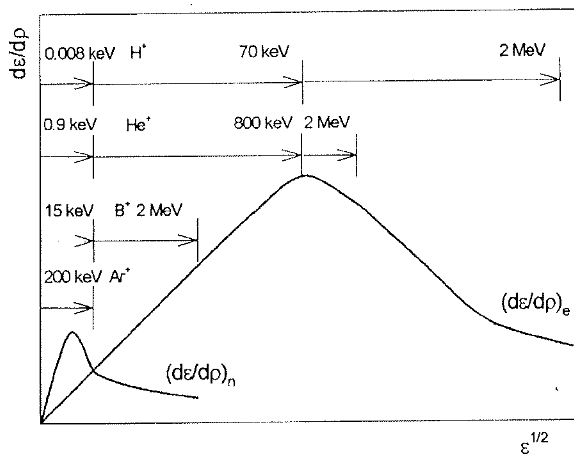

Fig. 1. Variations of nuclear stopping (Sn) and electronic stopping (Se) with the ion velocity. Please note that both, stopping and energy, are expressed in normalized values (defined in the LSS theory /2 LSS/).

nuclei dominate. The statistical character of the stopping process results in Gaussian-like distribution of implanted atoms, the determination of profile parameters was the first objective of the research on ion implantation. The first approach allowing the determination of stopping of ions in solid (hence the depth profile of implanted atoms) was developed by Lindhard, Scharff and Schiott /2/. The model, called from the authors names LSS theory, introduces normalized values of energy, range and standard deviation of atomic distribution. According to the LSS theory the depth distribution of implanted atoms can be described as:

$$N(x) = C_{max}\, e^{\left(-\frac{(x-Rp)^2}{2\Delta Rp^2}\right)}$$

Where C_{max} is maximum concentration of implanted atoms, R_p is a projected range of implanted ions, and ΔR_p is a standard deviation of atomic distribution. Maximum concentration of implanted atoms, C_{max}, can be calculated from the formula:

$$C_{max} = \frac{D}{\sqrt{2\pi\Delta R_p}}$$

Where D is implantation dose (i.e. the number of ions implanted in surface unit of the target).

The results of calculations were tabulated and can be used for the determination of the depth distribution parameters /3,4/. The development of Monte-Carlo numerical computer codes allowing the simulation of the processes occurring during the slowing down of the ions within the target made from them the generally used tool for the prediction of the effects of ion implantation. The best known and most widely used code is TRIM by Biersack and Ziegler /5/.

The energy lost in inelastic collisions with electrons leads to the creation of ionized states which, in most cases, recombine rapidly with target electrons. Consequently, these collisions lead only to slowing down the ions but do not induce structural changes to the target. The only exceptions can be observed in weakly bonded insulators or in processes using extremely heavy and energetic ions (with energies exceeding hundreds of MeV /6/). On the other hand the energy transferred from the ion to the target nuclei in elastic collision may reach tens or even hundreds of keV what exceeds the binding energy of atom in crystalline structure by orders of magnitude. The elastic collisions lead thus to the displacement of target atoms from their initial positions, hence to the radiation damage creation /1, 2, 4/. The radiation damage is an intrinsic and very important characteristic of ion implantation as each ion may displace even thousands of atoms from their lattice sites /7/. When the hit atom (often denoted as PKA from Primary Knock-on Atom) received sufficiently high energy it may collide with other atoms creating so-called displacement cascade, i.e. local volume characterized by a high concentration of radiation defects. The example of TRIM calculation showing the cascade formed by 100 keV argon ion implanted into iron is presented in Fig. 2. The radiation defect depth distribution can also be extracted from TRIM simulations together with the distribution of the implanted atoms. An example presenting the results obtained for 50 keV nitrogen ions implanted into iron up to a dose of $1\text{x}10^{17}$ atoms/cm^2 is shown in Fig. 3.

In order to understand better the specific character of ion implantation it is crucial to discuss in detail the processes occurring during the cascade evolution. The fast ion penetrating the target collides with few target atoms and is stopped after about 10^{-12} second. Therefore most of radiation damage is created by displaced target atoms, not by incoming ion itself. The typical defect created by atomic collision is a simple Frenkel pair. The separation between displaced atom and its vacancy is usually small therefore most of the created defects recombine during the cascade evolution. Molecular dynamic simulations /8/ allowed to get a deeper insight into damage process. The concentration of defects during cascade evolution extracted from molecular dynamic simulation is presented in Fig. 4. Three stages can be noticed. The first one is collisional phase

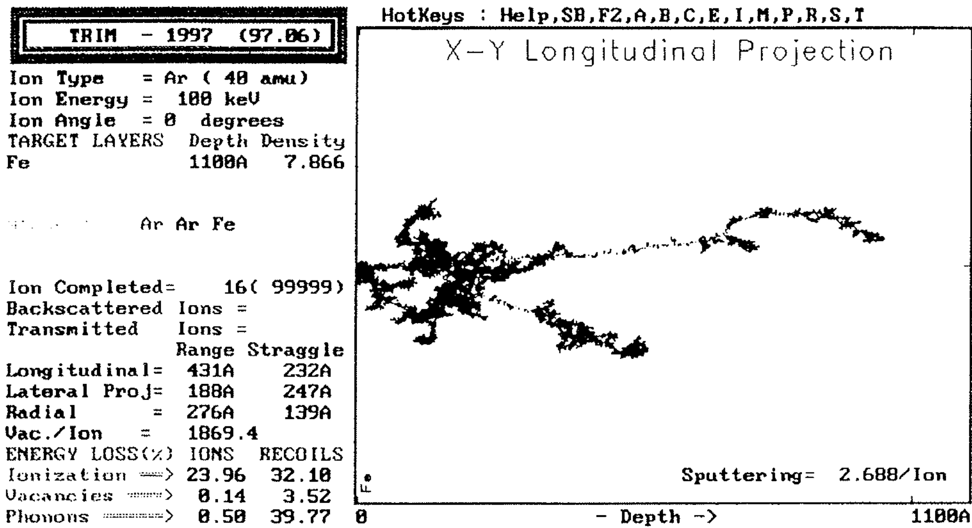

Fig. 2. Results of TRIM calculations showing the formation of displacement cascade in Ar implanted Fe. The ion path is shown as a solid line, the points correspond to displaced target atoms. One can note the formation of isolated cascades in the vicinity of primary knock-on atoms.

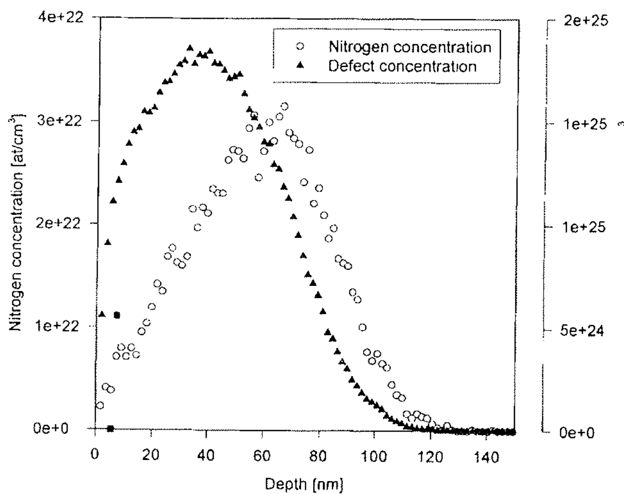

Fig. 3. Depth distribution of implanted atoms and of the defects created by 50 keV nitrogen implantation into iron. The left vertical scale corresponds to the defect concentration and the right scale to the implanted atom concentration.

(I) when ion collides with target nuclei. This stage takes about 10^{-12} sec and is characterized by rapidly increasing concentration of defects. This is followed by a displacement phase (II) when the ion is already stopped and collisions are created only by displaced target atoms. During this stage the recombination of close Frenkel pairs took place leading to a rapid decrease of defect concentration. This stage lasts about 10^{-11} sec. The last stage of cascade evolution is called cooling phase (III). All close Frenkel pairs disappeared already and the defect anihilation requires long range diffusion mechanisms. The average energy of displaced atoms drops below 1 eV, i.e. is in thermal energy range.

The spatial evolution of defects in cascade is of great importance for the phase formation in implanted systems. The structures of vacancy clusters formed in tungsten irradiated with various ions are presented in Fig. 5 /9/. One can note the density of the vacancy cluster strongly increases with the mass of the incoming ion. The vacancy cluster is surrounded by the interstitial-rich zone. It is believed /10/ that the phases formed in ion implantation mainly depend on processes in central, vacancy rich region of cascade during its cooling phase.

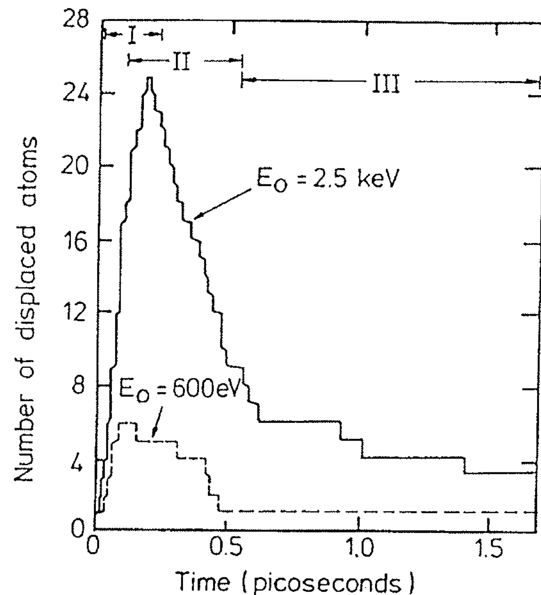

Fig. 4. Evolution of radiation defect concentration upon time for cascade created by 2.5 keV and 0.6 keV W atoms in tungsten.

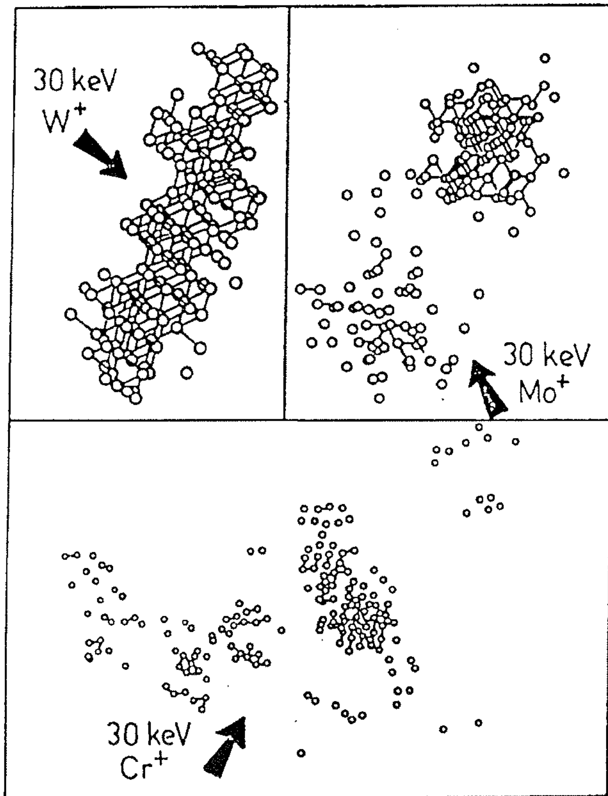

Fig. 5. Spatial distribution of vacancies in cascades formed by various ions in tungsten (picture taken from Ref. 9).

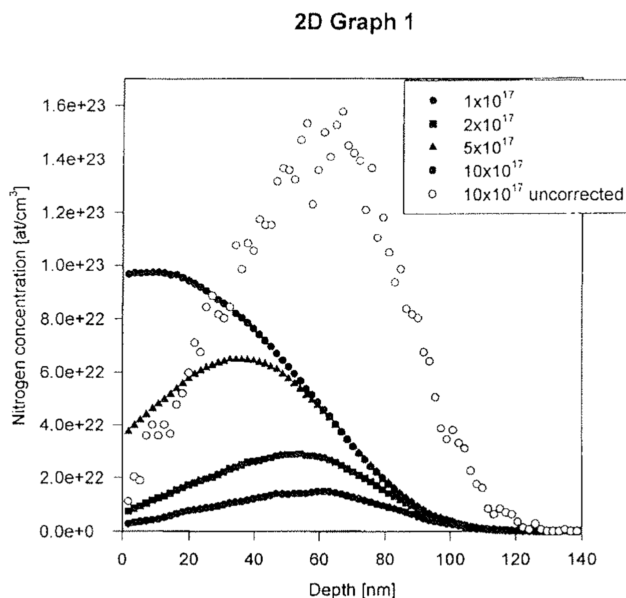

Fig. 6. Depth distribution profiles of 50 keV nitrogen ions implanted into iron up to doses of 1, 2, 5 and $10x10^{17}/cm^2$ corrected for the sputtering coefficient S = 0.8 (dashed lines) and profile for the highest dose of $10x10^{17}/cm^2$ directly extracted from TRIM simulation (solid line).

In the case when the displacement cascade touch the surface of the target some atoms may be ejected from the surface. This process is termed sputtering and is a main reason limiting the maximum concentration of the implanted atoms /11/. The parameter describing the sputtering is sputtering coefficient, S defined as number of target atoms ejected by one incoming ion. The S value vary from almost zero for light energetic ions to tens for heavy ions of low energy. As a general rule one can assume that the maximum concentration of implanted atoms is roughly proportional to 1/S /11/. The TRIM code do not take account of the target composition changes due to the implantation and sputtering, hence it can be used reliably only for the simulation of low dose implantations. For higher doses more advanced versions like TRIMDYN should be used or TRIM results should be corrected for sputtering effects. The importance of this correction is clearly visible on Fig. 6 showing the nitrogen profiles after high dose implantations into iron. Several profiles corrected for sputtering are presented together with the one without correction. The uncorrected calculations may lead to unrealistic nitrogen concentration exceeding the target atomic concentration.

2.2 Ion implanters

The layout of BALZERS MPB 202RP ion implanter is presented in Fig. 7. The device is composed of several main parts, such as:

Ion source. The role of ion source is to ionize the impurity atoms to make possible their acceleration in an electrostatic accelerator. In case of non-gaseous impurities these elements should first be vaporized, thus the ion sources are also equipped with high temperature oven.

Extraction optics. The ions formed in an ion source should be extracted from it and an ion beam should be formed. Taking into account that one of the main problems in implanters design is to maximize ion beam current the ion optics composed from extraction and focusing electrodes should ensure that as much as possible of extracted ions will be directed towards the target.

Accelerator. The role of an electrostatic accelerator is to create uniform electric field accelerating the ions to final energy. Once again the ion beam dispersion should be kept as low as possible to avoid the decrease of ion beam current.

Analyzing magnet. The ion beam extracted from the source may contain not only the impurity ions but also unwanted elements like noble gas atoms used to sustain the stable operation of ion source or chlorine atoms (in many cases the elements are introduced into an ion source in form of chlorides). Therefore these unwanted elements should be separated from the impurity atoms in magnetic analyzer. The typical analyzing magnets have the mass resolution reaching 500/M allowing the isotopic separation for all elements.

Scanning electrodes. The ion beam current density in beam footprint is usually non-uniform and the beam diameter is often too low (few cm^2). Therefore it is crucial to swap the beam over a large area what makes

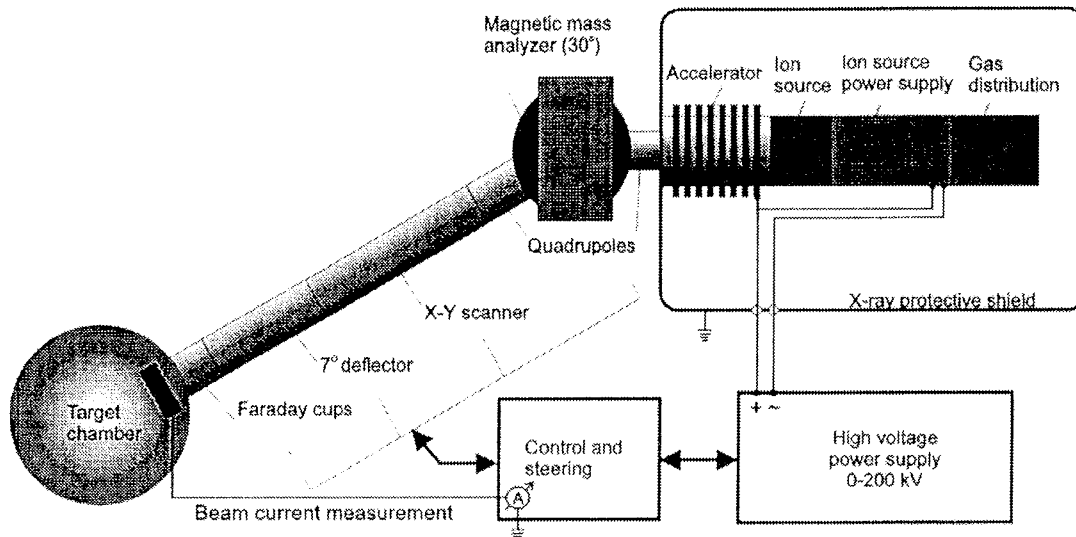

Fig. 7. Layout of the BALZERS MPB 202 RP ion implanter.

possible implantation of surfaces reaching one square meter and ensures uniform doping over the implanted area. The uniformity obtained in commercial implanters used in semiconductor technology reaches 2 % over wafer area and from batch to batch.

Target chamber. The vacuum chamber containing the samples to be implanted. The target chamber is fitted with the sample holder in which the samples are fixed. One of the major problems in the construction of target chambers and sample holders is evacuation of heat due to the incoming energetic ion beam. The total ion beam power may reach few hundreds of watts, almost completely transformed into heat. The temperature rise may thus be of the order of few hundreds of Kelvins. Such high temperature may be detrimental for the samples treated. In the case of nitrogen implantation into tools the complicated shapes of treated objects together with the tight temperature limits makes the target chamber and sample manipulator the most expensive parts of ion implanter.

2.3 Related techniques

During the development of ion implantation several derivative methods have emerged from this technology. The most widely used are briefly described below.

2.3.1 Ion beam mixing

Ion beam mixing (IM) /12,13/ is a two step process in which thin layer of material is deposited first on the surface of treated sample. This layer is then bombarded with inert gas ions. The incoming ions collide with the layer atoms transferring to them part of their kinetic energy. This permit the layer atom to penetrate the target. In IM process the ion beam serve thus only the purpose of energy carrier, the doping mass transport occurs from the deposited layer. In some cases the superstructure composed of numerous layers of different materials is also used. After ion bombardment this superstructure can be transformed into a homo-genous layer having the concentration depending on the initial sublayers thicknesses. The main advantages of IM with respect to classical ion implantation are no concentration limits due to the sputtering and much lower irradiation fluences required. From economical point of view the IM process is about one order of magnitude less expensive than ion implantation of metallic ions.

2.3.2 Plasma source ion implantation

One of the major disadvantages of ion implantation used for tool treatment is line-of-sight character of this process. It was the main reason to develop the plasma source ion implantation (PSII) process /14/ in which the treated object is confined in plasma and is polarized with high voltage negative pulses. The strong electric field first swap the electrons from the vicinity of the object creating an accelerating gap in which ions from plasma are accelerated towards the treated object. In PSII process all sides of the detail are treated simultaneously greatly improving the process efficiency.

2.3.3 High energy irradiation

The main interest of basic research in nuclear physics continuously move towards higher energies leaving many accelerators more available for the materials studies. Consequently more and more tandem accelerators and cyclotrones become available for solid state physics. This allows one to extend the materials studies towards the energies reaching few gigaelectronvolts. Very low beam currents available in such machines limit the research to studies of defect creation in solids. Very high energy deposition density reaching some keV/angstroem allowed the discovery of numerous spectacular effects such as giant plastic deformation /6/ or amorphization induced by inelastic collisions. The high energy irradiation remain, however, almost exclusively a research tool, the practical applications are not expected soon.

3. Main fields of application

3.1 Semiconductors

Ion implantation is a standard doping process in semiconductor technology used for MOS and bipolar devices fabrication /15/. Except of junction formation it is used also to diminish the contact resistance by doping of semiconductors in contact area or by using ion beam mixing of contact material with the semiconductor substrate. In many cases, especially in several compound semiconductors, ion implantation is the only used technique of type conversion. Since several years the high current implanters allowed the heavy doping of materials, thus the synthesis of compounds. One of the examples of this possibility is the fabrication of SIMOX devices in which high dose oxygen implantation into silicon leads to the formation of buried silicone oxide layer. These devices are characterized by a thin crystalline silicon layer on insulating SiO_2 substrate. Consequently the electrical insulation of elements formed within this layer do not require any polarized junction. High dose of germanium implantation into silicon leads to the synthesis of SiGe material characterized by much higher carrier mobility when compared with pure silicon. Complete reviews of current status of ion implantation in semiconductor technology can be found e.g. in recent papers of Pearton /15/.

3.2 Metals

The main field of applications of ion implantation for metal modification is the improvement of mechanical properties of steels and titanium alloys. Nitrogen implantation into tool and high speed steel may increase the lifetime of precise tools and details by a factor of four /16,17/. Taking into account that typical processing costs are less than one USD per cm^2 and the price of precise tools often exceeds thousands of dollars the use of implantation may lead to significant cost savings /18/ in many industrial applications. The unique features of ion implantation when compared with other surface modification methods are: no dimensional or surface finishing changes and no risk of layer delamination. The fact that implantation is used only in several niche applications in machine industry seems to be due mainly to the low thickness of the treated layer.

The rapidly growing market for ion implantation was identified in biomedical applications. The best known example is probably the implantation into hip joint prosthesis. Some data report the increase of their lifetime by a factor of 20 /19/. Less known is information concerning lower patient discomfort observed when using implanted dental drills from tungsten carbide.

3.3 Others

It is not possible to enumerate all applications of ion implantation. Some well established examples are: nanoporous filter fabrication via high energy irradiation of polymers, modification of optical properties of materials used for waveguide processing, changes in surface energy properties of plastics and polymers, modification of electron work function (allowing lifetime increase of lightning protectors) or increase of adhesion between layers and substrates. In general the use of ion implantation and related ion beam techniques may be expected in all fields requiring precise doping of thin surface layers.

4. Advantages and drawbacks

The kinetic character of doping in ion implantation results in the absence of any thermodynamical limitations, consequently any solid target can be doped with virtually all elements. Numerous impurities can be introduced into same target leading to the formation of multielemental phases. The radiation damage favorize the formation of metastable structures such as, e.g. amorphous phases. Another advantage comes from the fact that all process parameters can be controlled independently. This last feature is especially important when wide process temperature range is required. Ion implantation allows one to perform the same process in temperatures ranging from liquid helium to more than one thousand degrees centigrade. Very good precision, uniformity and repeatability (the differences in doping uniformity are usually lower than few atomic percent) are also of interest. In mechanical applications the absence of any dimensional or surface finishing changes as well as no risk of layer delamination are main advantages of ion implantation. Finally, the ion beam techniques are clean vacuum processes which do not produce any hazardous wastes requiring special treatment.

Main disadvantage of the method is low thickness of modified layer which rarely exceed few hundreds of nanometers. Most of ion beam techniques are also line-of-sight processes, therefore the treatment of the objects of complicated shapes require special manipulators and often part of the object surface is hidden against the ion beam. It is often claimed that ion implantation is a very costly treatment. Whereas the initial investment costs may be in fact heavy (modern ion implanter used in semiconductor industry costs even few millions of dollars) the processing costs are acceptable in most of applications. For example, the nitrogen implantation into steels costs about =0.5 USD/cm^2 and it should be noted that only the working part of the tool is treated. As a rule of thumb one can thus expect that the treatment costs do not exceed 20-30 % of tool costs whereas the lifetime increase may reach four times. Moreover main semiconductors companies exchange their equipment roughly every three years, hence on the second hand market three or four years old and fully operational implanters are available at surprisingly low cost (even few tens of thousands of USD).

5. Concluding remarks

The "gold rule" of technology claims that there are no good or bad methods, there are only correctly and improperly used techniques. Ion implantation is not, of course, a miraculous method able to replace all other doping techniques. It seems however, that this technique reached its maturity stage and proved to be one modern technologies very useful in many applications and necessary in modern material engineering. The experience gathered till now in many countries suggests that the most efficient way to implement this technique is the creation of specialized service center

equipped with modern universal ion implanter. Such a center should be preferentially located at the material research laboratory ensuring both; research studies and commercial services.

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AES CHARACTERIZATION OF PROTECTIVE THIN LAYERS ON THE AgNi0.15 CONTACT MATERIAL AFTER ITS TREATMENT IN THE RF PLASMA

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Keywords: electrical contacts, Ag contact materials, silver based contact materials, passivation, passivation thin films, RF plasma, AES analysis, Auger Electron Spectroscopy analysis, low cost implementations

Abstract: Well-known surface protection of Ag-contacts with the thin gold layer is rather expensive. We studied some cheaper types of protective layers. Thickness of the layer must be optional to avoid the corrosion effect of the surroundings and at the same time to insure sufficiently good electric conductivity between the two coated surfaces. Material that is used for the layers must be at least as good electric conductor as the ground material unless the contact characteristics deteriorate. Protection of contact surfaces is therefore a compromise between the increase of the contact stability and the deterioration of the initial contact characteristics. Three different protective layers were deposited on the AgNi0.15 contact material. After their treatment in the radio frequency plasma they were analyzed with the Auger spectrometer.

AES karakterizacija nanosov tankih zaščitnih plasti na AgNi0.15 kontaktnem materialu po obdelavi v RF plazmi

Ključne besede: kontakti električni, Ag materiali kontaktov srebrni, pasivacija, plasti tanke pasivacijske, RF plazma radiofrekvenčna, AES analize s spektroskopijo elektronsko po AUGER metodi, izvedbe cenene

Povzetek: Znana površinska zaščita Ag kontaktov s tankim nanosom zlata je cenovno neugodna. Študirali smo nekatere cenejše pasivacijske plasti, ki jih lahko nanesemo dovolj tanko, da preprečimo korozijski učinek okolice in hkrati ohranimo dovolj veliko električno prevodnost stika med pasiviranima površinama, ki ustreza dobremu električnemu kontaktu. Zaščitna plast na kontaktni površini poslabša kontaktne lastnosti, če ni iz električno bolj ali enako prevodnega materiala kot osnovni kontaktni material. Zato pomeni uvedba pasivacije kontaktnih površin kompromis med povečanjem stabilnosti kontakta in verjetnim poslabšanjem začetnih kontaktnih lastnosti. Tri različne pasivacijske tanke plasti smo nanesli na AgNi0.15 kontaktni material. Nanose tankih plasti po obdelavi v radiofrekvenčni plazmi (RF) smo analizirali s spektrometrom Augerjevih elektronov.

1 Introduction

The requirements for the stability of contact characteristics /1,2,3/ of switching devices are fulfilled if the parameters of the electric contact are within the limits that ensure the contact to work properly. The conductivity of the contact spot between the two surfaces should be sufficiently constant and the contact material should be conducting and chosen according to the known contact force. The contact material should not be affected by the surroundings that produce the corrosion layers and cause the deposition of foreign particles and layers. For testing contact material the AgNi0.15 alloy was chosen as a typical representative of the silver based material. Stability of AgNi0.15 contacts is affected primarily by the formation (and its growing with time) of Ag_2S surface layer in the industrial atmosphere.

2 Experimental

Test samples were made of the contact material AgNi0.15 in the form of the miniprofile-strip with the cross section of 2.6x0.3 cm^2. 50 mm long parts were cut from the strip. Contact surface was half-cylindrical in shape with the curve radius of 9 mm. Three different types of protective layers deposited on the test contacts were studied:

- Passivation by waxing. Test samples were treated in the water solution named Silverbrite /4/.
- Passivation by chromizing. Layer was made by anode oxidation according to the receipt /5/.
- Passivation by the solid layer. Solid layer Ti+TiN was formed by sputtering /6/.

All the three types of protective layers were tested for the resistance to sulfating in the K_2S solution. Samples were exposed to the wet atmosphere containing H_2S (climate test). Afterwards samples were treated by the radio frequency (RF) low pressure plasma /7/: first cleaning of the samples in the hydrogen plasma (1 minute of exposition, 1 mbar), then surface oxidation in the reactive oxygen plasma (0.5 minute, 0.6 mbar). Both procedures were performed in the standard discharge vessel which was a cylindrical glass tube with the diameter of 3 cm. Plasma was created by an inductively coupled RF generator. Hopkins liquid nitrogen cooled trap was used. Temperature of the samples was not measured.

After the treatment of all the three protective layers in plasma condition of the surface was examined /8/ with the Auger spectrometer (Physical Electronic Ind. SAM 545 A) with the static primary electron beam with the energy of 3 keV, the beam current of 0.5 μA, and the beam diameter of about 40 μm. Etching was performed

on the surface area of 10 mm x 10 mm with the two Ar^+ ion beams with the energy of 1 keV. The incidence angle of the ion beam was 47°. The etching velocity was about 1.7 nm/min and was calibrated with the standard Ni/Cr multilayer sample. For determining the element concentration (except for the nitrogen concentration where the factor was calculated from the standard sample of stehiometric TiN) the sensitivity factors were taken from the spectroscope manufacturer (PEI) manual. Results of the analysis were presented in the profile diagrams (Fig. 1-6).

3 Results and discussion

We found that the thin Silverbrite layer on the surface of the AgNi0.15 sample is resistant to the sulfading with K_2S (according to the standard test) and also to the wet atmosphere. Protective substance is attached to the Ag base material only by adhesion therefore after the treatment in hydrogen plasma it can not be detected by the Auger spectrometer any more. Very clean surface with only the traces of oxygen can be seen in Fig. 1. After additional exposition of the sample to the oxygen plasma very uniform (black) silver oxide coating is obtained. Formation of silver oxide was confirmed by the Auger analysis. The concentration of oxygen at the surface of the layer is 13 at.% while on the other side the concentration falls to 6 at.%. Thickness of the layer is more than 25 nm and is very clean (Fig. 2). Passivation layer of chromized AgNi0.15 sample is resistant to K_2S and to wet atmosphere containing H_2S. Thickness of the coating layers of the samples exposed to hydrogen plasma was less than 1 nm. Coating contains Cr and small concentrations of N, P and Ca on the surface (Fig. 3). After the additional exposition to oxygen plasma traces of carbon could be found on the surface, while the inner part of the layer is oxidized with less than 10 at.% of oxygen (Fig. 4). Chromium is removed by the oxygen plasma. AES analysis of the AgNi0.15 with the sputtered thin TiN layer after the treatment with hydrogen plasma indicates that only the surface of the layer is oxidized (Fig. 5). There are carbon atoms inside the TiN layer. They were built-in during the deposition of TiN. When the same sample is treated also with the oxygen plasma the TiN layer surface was oxidized to the high degree (Fig. 6). It is evident that carbon was removed from the surface region. Estimated thickness of this sample's oxide layer is 5 nm. Nitride layer is so

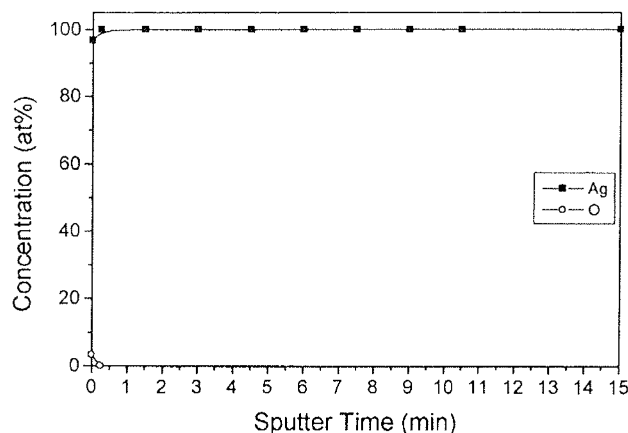

Fig. 1. Sample AgNi0.15 with the Silverbrite layer after exposition to hydrogen plasma

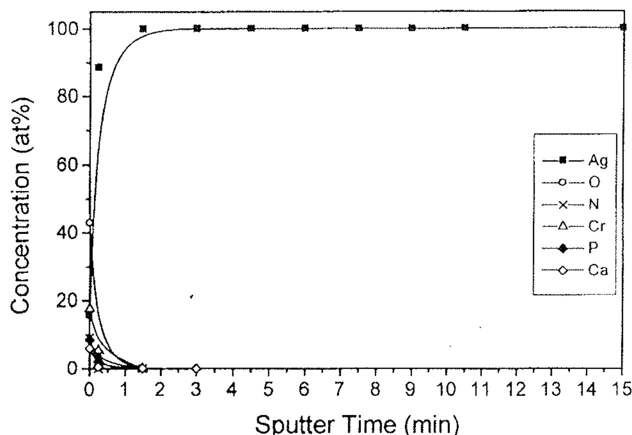

Fig. 3. Chromated AgNi0.15 sample after exposition to hydrogen plasma

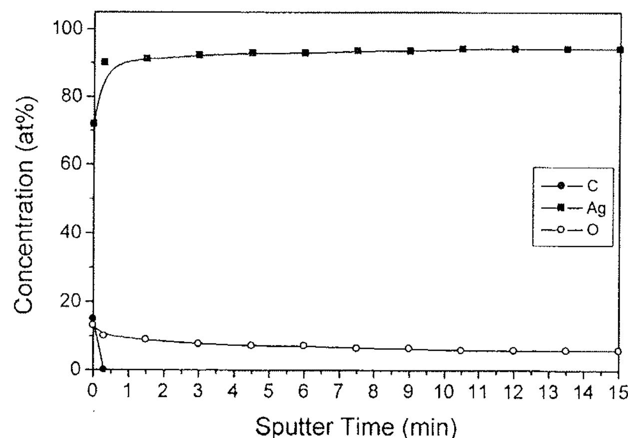

Fig. 2. Sample AgNi0.15 with the Silverbrite layer after exposition to hydrogen and oxygen plasma, respectively

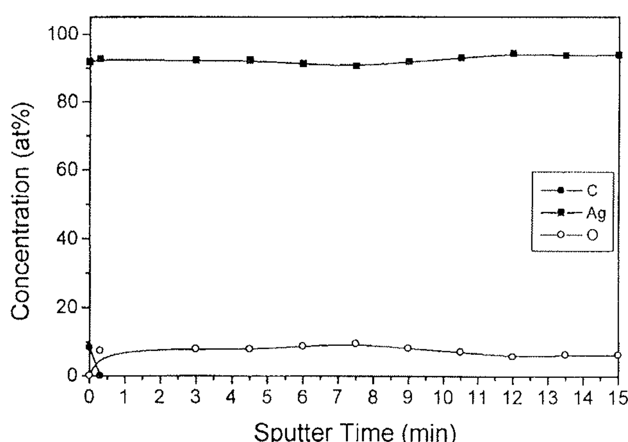

Fig. 4. Chromated AgNi0.15 sample after exposition to hydrogen and oxygen plasma, respectively

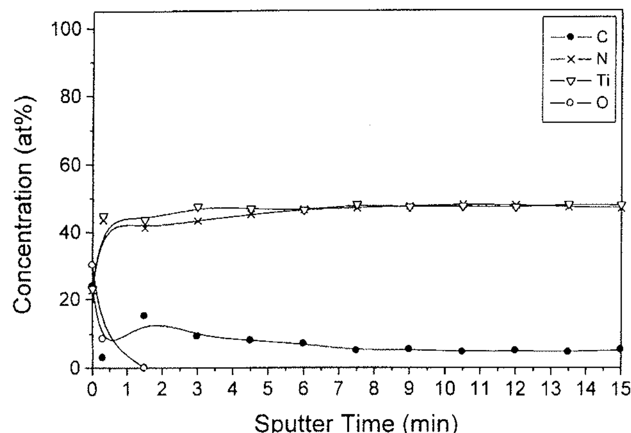

Fig. 5. Sample AgNi0.15 with the TiN thin layer after exposition to hydrogen plasma

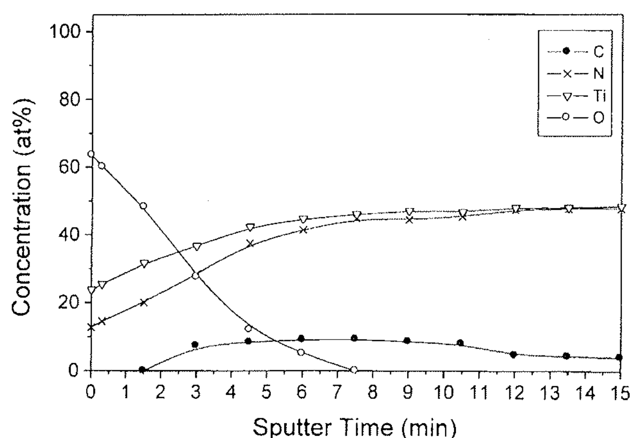

Fig. 6. Sample AgNi0.15 with the TiN thin layer after exposition to hydrogen and oxygen plasma, respectively

tightly bound to the base material that it is not removed during the treatment in the hydrogen RF plasma. Chemical resistance to the influence of the aggressive agents of the surroundings is excellent.

4 Conclusions

With the spectroscopy of Auger electrons three types of pasivation thin layers on the base contact material AgNi0.15 were analyzed after the treatment of samples in the hydrogen and oxygen RF plasma.

Results of pasivation of the contact material AgNi0.15 with respect to contact performances are very satisfactory therefore we suggest to consider also other contact materials on the silver basis.

TiN pasivation layer beside good contact performances exhibits also fair slide and wear properties. Therefore this type of layer is recommended for contacts in heavy duty switches (large number of switchings under difficult environmental conditions).

When Ag contact material is exposed to low pressure oxygen plasma oxidation to Ag oxide is possible. If the pasivation with plasma oxidation will prove to be effective it will be possible to clean and to protect the contacts in just one technological procedure.

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CHEAP MULTICHIP MODULES

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Keywords: MCM, MultiChip Modules, MCM technology, cheap modules, MCM-L, MultiChip Modules Laminates, MCM-C, MultiChip Modules Ceramics, cost reduction, RTD, Research and Technology Development

Abstract: The opportunity for mutual benefit across Europe to develop low-cost MCM technologies arose from recognition of the scientific skills and design and prototyping capabilities in organic and inorganic circuits in countries of Central Europe. As a results, the leading research institutions and small/medium-size enterprises of Hungary, Romania and Slovenia together with relevant institutions of the United Kingdom and Belgium proposed and received approval for an European Union INCO-COPERNICUS project (IC15-CT96-0743) "Establishment of Fast Prototyping Low Cost Multichip Module Technology Facilities in Eastern Europe for the Benefit of European Industry" (Cheap MultiChip Modules) to establish fast prototyping low cost multichip module (MCM) technology facilities. The project commenced in May 1997.

MCM Technologies include the design, manufacturing, assembling and testing phases. The tasks of the Project are divided among the participants in accordance with these technological phases and conforming to their interest and capability in the field.

Design is the task of the Rumanian Partners. They have installed CAD systems and developed circuit designs and simulations to determine the design rules and preferences for MCMs. Manufacturing is the task of the Hungarian and Slovenian Partners. They are focusing their laminate and ceramics capabilities towards MCM-L and MCM-C manufacturing and upgrading test technologies up to a level to fulfill the low cost, fast prototyping requirements of the participating Central European Countries (and later Europe-wide). The Hungarian Partner is also establishing mounting and bonding facilities for assembling MCMs in collaboration with the UK and Belgian Partners, exploiting their high level experience in the fields of microjoining and test technologies. The final test of demonstration modules is also the task of the Belgian Partner. The evaluation of the results in accordance with the manufacturing, application and economic aspects will be the task of all Partners with the leadership of the Hungarian Partner.

The Project is carried out in close co-operation of all Partners. In order to disseminate information for and about the Project, the Partnership participates in conferences, organizes seminars and training courses for themselves and for small and medium size enterprises who show interest in the prototyping technology of MCMs.

Considerable progress has been made in the design facilities by the Rumanian Partner, and in the refinement of the printed circuit board (PCB) technology at Budapest, including laser patterning of MCM-Ls. Diffusion patterning and ceramics technology skills in Slovenia are enabling MCM-C prototyping to be demonstrated and further developed.

Poceni multichip moduli

Ključne besede: MCM moduli multichip, MCM tehnologija modulov multichip, moduli ceneni, MCM-L moduli multichip laminati, MCM-C moduli multichip keramika, zmanjšanje stroškov, RTD razvoj raziskovanja in tehnologije

Povzetek: Vodilni raziskovalni inštituti in majhna oziroma srednje velika podjetja Madžarske, Romunije in Slovenije so hkrati z ustreznimi inštitucijami Velike Britanije in Belgije predlagali Evropski uniji INCO-COPERNICUS projekt »Poceni Multichip moduli«. Namen projekta, ki je bil sprejet in je začel teči maja 1997, je omogočiti hitro izdelavo prototipov poceni multichip modulov (MCM).

MCM tehnologije obsegajo design, izdelavo, sestavljanje in testiranje prototipov. Naloge projekta so razdeljene med partnerje glede na njihovo tehnološko usposobljenost. Design je naloga romunskih partnerjev. Instalirali so CAD sistem in bodo s pomočjo testnih vezij in simulacij določili pravila načrtovanja. Izdelava prototipov je naloga madžarskih in slovenskih partnerjev. Madžarski partnerji se bodo koncentrirali na MCM-L (tehnologija tiskanih vezij), slovenski pa na MCM-C (Keramični MCM, v tem primeru večplastna debeloplastna vezja). Madžarski partner bo hkrati z angleškim in belgijskim odgovoren tudi za bondiranje golih silicijevih tabletk in sestavljanje oziroma montažo prototipov MCM. Končno testiranje demonstracijskih vezij je naloga belgijskega partnerja. Evaluacija rezultatov je naloga vseh partnerjev pod vodstvom madžarskega partnerja, ki je tudi koordinator projekta.

V projektu vsi partnerji tesno sodelujejo. Da bi razširili znanja tako o projektu kot o tehnologijah in možnostih načrtovanja, partnerji sodelujejo na konferencah, objavljajo v odprti literaturi in sodelujejo pri organizaciji seminarjev in tečajev za mala in srednje velika podjetja, ki se zanimajo za poceni prototipe MCM ali za izdelavo MCM v tehnologiji tiskanih vezij ali večplastnih debeloplastnih vezij.

Opazen napredek je bil dosežen s strani romunskega partnerja na področju designa, s strani madžarskega partnerja na področju tiskanih vezij in laserskega oblikovanja ter slovenskega partnerja na področju tehnologije difuzijskega oblikovanjanja večplastnih debeloplastnih vezij.

V prispevku je opisana struktura projekta in podana tista bibligrafija sodelavcev, ki se nanaša na projekt.

INTRODUCTION

The success of most electronic instruments and systems, regarding both their performance and marketing issues, depends to a great extent on the ability to use the most advanced technology that is cost-effectively possible. However, the performance of today's electronics is primarily limited by the interconnections between components and subsystems, and not by the high-speed, very large scale integrated (VLSI) circuits from which the systems are built up. Thus, to achieve high performance and high reliability at a reasonably low cost, it is imperative to use the most appropriate interconnection and packaging technology accompanied by advanced design, manufacturing, assembly, and testing expertise.

Regarding the interrelationships between the various products of electronics and between the interconnection and packaging system-technologies used for them, three levels of the products can be distinguished: components (or basic products), circuit modules (or assemblies) and equipment (or electronic systems). The usual physical construction of a personal computer (PC) is a good illustration of the hierarchy of electronics products (Figure 1). This construction points out the importance of interconnection and packaging technologies, mainly realized by the different types of circuit modules. Moreover it presents a characteristic example for the use of interconnection technology, that is to create connections and communication routes between the signal processing chips and large systems, as well as, human beings.

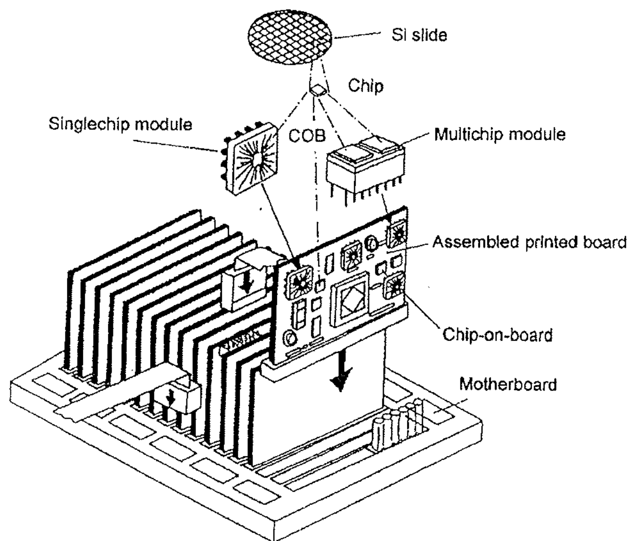


Fig. 1. The hierarchy of electronics products and packaging technologies

Electronic Packaging Driving Forces toward Multichip Modules

In the design and manufacturing of each level of interconnection of any electronic system, the driving forces are to lower cost and to improve performance /1,2/. From these points of view the followings are of great importance:

- **The decrease of the distance between chips** in order to achieve faster operation. This requirement can be fulfilled by increasing the functional density and integration level of the applied very large scale integrated (VLSI) circuits and/or increasing the density of the interconnection system.
- **The reduction of the cost per connection** in order to reduce cost. The most cost-effective solution can be achieved by increasing the integration levels of both the chips and the interconnection systems, thus making more connections simultaneously, reducing the use of materials and processing, which results in the reduction of the cost per connection. From this a general rule can be formulated, that the cost per connection is the higher the farther the connection from the center of the chip is.
- **The use of catalogue devices.** The customization on the chip level is very expensive unless large quantities are to be used. The use of less application specific integrated circuits together with custom designed interconnection system can minimize the duration of the design-manufacturing-test cycle, and can result in a cost-effective complex solution.
- **The optimum partitioning of the circuitry** in order to improve thermal performance by using materials with high thermal conductivity, instead of using more complicated and expensive heat-transfer mechanisms.
- **The exploitation of the existing design, manufacturing, assembly, and testing technology** in the field of interconnection and packaging.

At present time, the multichip module (MCM) approach is considered the most advanced circuit module technology. MCM technology is an advanced extension of bare-chip hybrid technology, offering at least an order-of-magnitude improvement over earlier packaging approaches regarding electric performance, packaging density and reliability as well. Among the criteria beyond which a circuit is considered to be a multichip module there are the followings:

- the application of bare-chips or chip-size packages, and compatible chip attachment and bonding technologies, in the majority of cases,
- the application of multilayer and high-density interconnect substrate, and
- the advanced thermal design of the complete package.

Objectives of the Cheap MultiChip Modules Project

The title of the Project that was proposed and received approval for support from the European Commission in the frame of INCO-COPERNICUS Programme is "Establishment of Fast Prototyping Low Cost Multichip Module Technology Facilities in Eastern Europe for the Benefit of European Industry". The short form of the title is "Cheap MultiChip Modules" or CM^2. The project commenced in May 1997, and now it is over its half-time

period. The project is the cooperation of nine Partners given by the institutions of the co-authors of the present paper.

On the basis of the trends in electronics discussed in the Introduction, and taking into account the forces which drive electronic packaging technology toward multichip modules, the Project was initiated with the following important research and development objectives:

- improvement of the technological facilities of the Rumanian, Hungarian and Slovenian Partners in order to be capable for
- prototyping low cost, high performance electronic circuit modules by increasing functional and interconnection density with the
- application of integrated interconnection substrates instead of the extremely expensive on-chip customization.

Multichip module technology, utilizing and/or uniting the advantages of ceramic (C) and laminating (L) techniques, is a promising solution of the requirements. The results are higher reliability, increased yield, reduced use of materials and processing, faster prototyping and shorter production period.

In addition, the RTD Project is intended to

- strengthen the relationship between research institutions of Central-Eastern Europe and their EU Partners in order to enhance research and technological capacities in some Countries of Central Europe,
- establish links with the small and medium-size enterprises responsible for product development and distribution, and
- safeguard and stabilize the research and technology development (RTD) potential of Central-Eastern European Countries by means of training and seminars for researchers working on the Project.

Technology of multichip modules includes the design (1), substrate manufacturing (2), assembling (3) and testing (4) phases. The tasks of the Project were divided among the participants in accordance with these technological phases and conformable to their interest and previous activity in the field. The distribution of the tasks can be summarized as follows:

1. The Rumanian Partners select a suitable CAD system, install it for the use of themselves and for the other Partners, and organize training courses.
2. Manufacturing MCM-L and MCM-C substrates is the task of the Hungarian and the Slovenian Partners, respectively. They have to improve their facilities, manufacturing and test technologies up to a level to fulfill the low cost, fast prototyping requirements. Quantitatively, the aim is to realize 300 μm diameter plated-through holes/vias with 125 μm wide lines and spacings, for laminated and ceramic based MCM technologies.
3. The Hungarian Partners' task is the establishment of mounting and bonding facility for the assembling of MCMs with the promotion of the English and Belgian Partners, exploiting their high level experience in the fields of microjoining and test technology. The aim is to handle 150 μm pitch medium size VLSI chips.
4. The material test and performance evaluation of the test patterns and demonstration modules is the task of all Rumanian, Hungarian and Slovenian Partners directed and controlled by the Belgian Partner.

The evaluation of the results in accordance with the manufacturing, application and economic aspects is the task of all Partners with the leadership of the Hungarian Partner.

The Project is carried out in close co-operation of all Partners. In order to gather and to disseminate information for and about the Project, they participate in conferences, organize seminars and training courses for themselves, for small/medium-size enterprises and research institutions in the Central-Eastern European Countries, who show interest in the application of the established low cost fast prototyping MCM technology.

Contributions of Partners to Project 'Cheap MultiChip Modules'

Considerable progress has been made in the first part of the Project. The present state of the work packages, the activity of the Partners and the most important results are characterized shortly in the followings.

In WP1:T1 University POLITEHNICA Bucharest and Ramelectro Ltd., Romania (UPB.RO and SCR.RO) collected requirements for the design of PCBs and MCM-Ls to help the selection of the CAD System. As the most suitable software, the CADSTAR for Windows made by Zuken Redac, with an additional module dedicated to EMC analysis, was selected. UPB.RO's experience using previous DOS and Windows CADSTAR versions has proved that this is a suitable software tool, which is oriented towards both electrical and technological aspects and contains many options like virtual costs estimation, powerful editing of routes, EMC-analyzer, field solver, thick- and thin-film design, various post-processing tools etc. Another reason for choosing CADSTAR system was that dedicated MCM programs were very expensive in comparison with the budget of the Project and could be run on very expensive workstations only. In WP1:T2 UPB.RO obtained the specified CADSTAR system and installed it into three PCs. SCR.RO has also obtained and installed a version of CADSTAR with the purpose to accommodate with it.

The Rumanian and Hungarian Partners carried out very fruitful discussions on what kind of MCM-L structure and technology, and what circuit should be chosen for demonstration of the use of the CADSTAR system and the manufacturing facilities, respectively. On the basis of consultations with TWI.GB and the other Partners, having also analyzed the different solutions published in the literature (e.g. in /3/, see Figure 2), a combined MCM/BGA structure (Figure 3) was pointed out for a simple transmitter circuit as a pilot demonstration (Figure 4). More details of the analyses of the structure and resulting design considerations are presented by the Rumanian Partners /22/, and the technological aspects of the problem are given later in this paper where the Hungarian Partners' activity is presented.

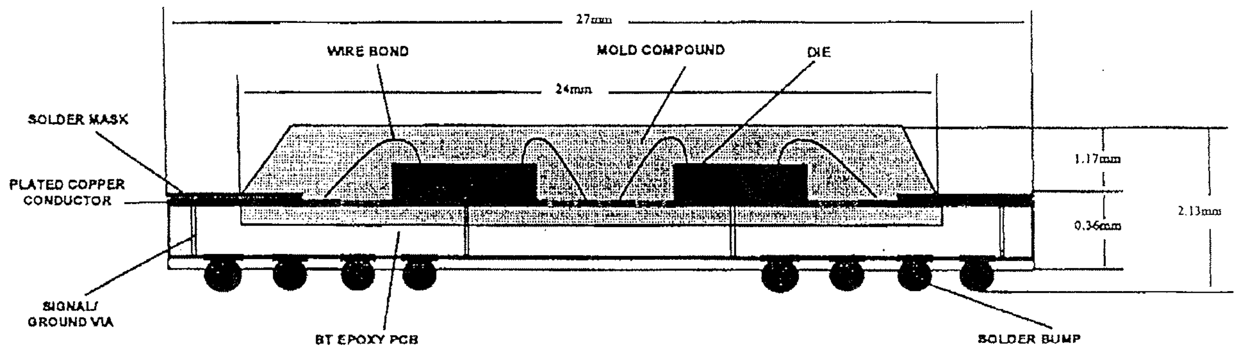


Fig. 2 A typical MCM-L structure combined with PBGA package /3/

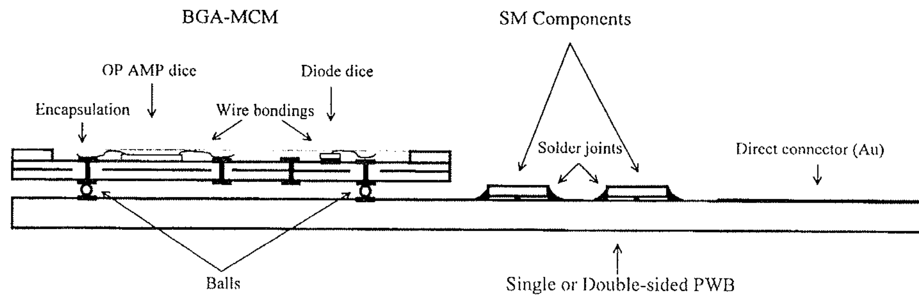
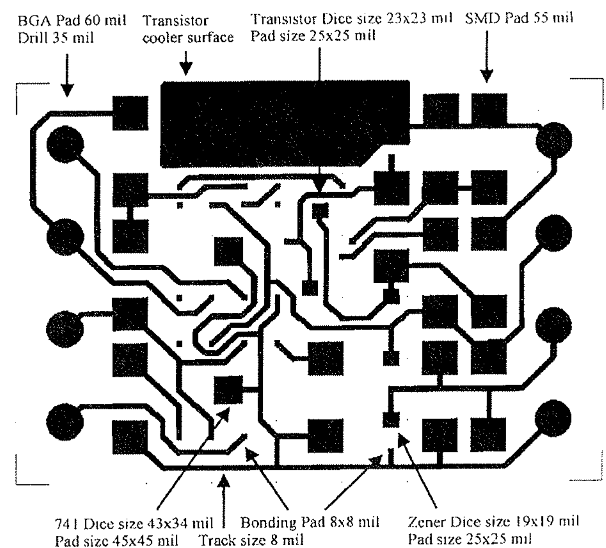


Fig. 3 Principle of the MCM/SMT modul

Technical University of Budapest and Elektroprint Ltd., Hungary (TUB.HU & EP.HU) in WP1:T1 and WP1:T2 collected requirements for the manufacturing facilities of MCM-Ls and selected suitable equipment to improve the resolution of the laminates and to decrease the turn-around time. For this purpose a drilling and direct patterning laser system was specified. TUB.HU had a unique opportunity to apply for a support from the Hungarian Research Ministry (OMFB) to purchase a "large research equipment". At last a support of ca ECU 63.000 was allotted, which sum together with ECU 10.000 from the INCO Project and ECU 23.000 from other incomes of the Hungarian Partners was spent to buy the specified Direct Exposure Laser System for MCM-Ls. In this way the investment for this purpose was about ten times higher than it had been originally planned in the INCO Proposal. The system was installed and is applied for drilling and image transfer /55/. With the professional and financial support of the EP.HU a more advanced etching system and a more suitable grinding machine were also installed.

In WP2:T3 TUB.HU upgrades processing technology of MCM-Ls. Pilot investigations have been carried out for this purpose to combine the laser imaging and wet chemical etching/electroplating processes in order to improve the resolution of the laminates. By the installation of the direct exposure laser system the possibility of the development of this new image transfer technology has been improved /26,38,45,51,53,55/. In addition, the application of the newest Shipley chemical products and the installation of the more advanced equipment provide possibilities for the processing technology upgrading. For this activity suitable test patterns and sample circuits are designed and used.



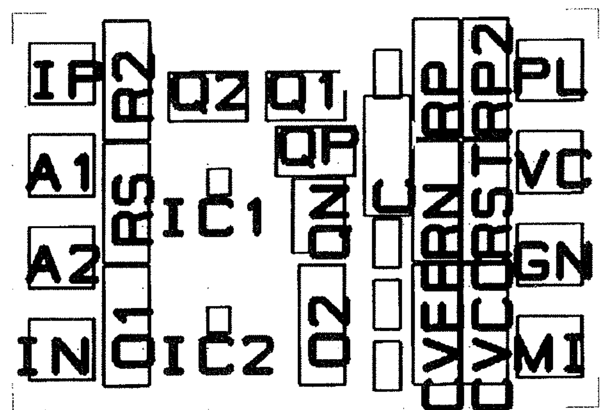


Fig. 4 Layouts of a transmitter for combined MCM-SMT-BGA realization

In WP4:T1 TUB.HU collected requirements for the assembling facility of MCMs. The main question was to decide what type of chip assembling technology, i.e. chip-and-wire, flip chip or TAB, would be used. With the help of the expertise of TWI.GB and IMEC.BE, it was decided that TUB would upgrade the chip-and-wire facility, and later would obtain and install flip-chip assembly equipment. The specification was discussed with JSI.SI at the 1st Project Meeting, and with IMEC.BE, WD.GB and TWI.GB during a visit paid to Gent and Abington, respectively.

In WP4:T2 TUB.HU installed an ultrasonic bonder to study the possibilities of chip-and-wire technology. A new handling table was designed and implemented to the ultrasonic bonder. Applying this bonder the bonding parameters were optimized for different type of substrates, such as thick- and thin-film structures as well as PWB laminates. To check the bonding parameters a new digital pull-up tester was developed. In order to obtain expertise for flip-chips, ball-grid-arrays were studied: a new type of BGA package was developed based on PWB laminates. This BGA version enables higher pitch density using specially positioned balls and filled vias. The new BGA version requires the application of DuPont ink materials. The requirements of ISO 9001 were studied concerning the MCM-L technology (partly as a preparation for WP5). Concerning the reliability and quality questions of the assembling technology a short visit was paid to the TWI.GB.

In WP3:T1 Josef Stefan Institute and HIPOT Hybrid Ltd., Slovenia (JSI.SI & HIPOT.SI) had to upgrade the analyzing and test facilities of integrated substrates for MCM-Cs. Equipment for Complex Impedance Analysis was selected and ordered. The price of the equipment with software was around ECU 38.000. Only a part of this (ECU 8.650) was covered from this INCO Project. The equipment was installed at Josef Stefan Institute in the summer of 1998.

In order to upgrade processing technology for MCM-Cs in WP3:T3, JSI.SI and HIPOT.SI decided to use thick-film multilayer technology to obtain the required MCM-C devices. A relatively novel technique for producing more dense thick film multilayer structures, i.e. the Diffusion Patterning (Diffusion Patterning™ is a trademark of DuPont) is used. Unlike standard via construction with screen-printing, Diffusion Pattering vias do not use any extra substrate space. Typical vias dimensions, obtainable in production, are around 400μm for screen-printing and 200μm for diffusion patterning. The dimensions of diffusion patterned vias are therefore similar to the width of conductor. It is estimated that complex hybrids can be build on 20% to 40% smaller substrates, and hence more complex and cost effective solutions are possible.

On this topic JSI.SI and HIPOT.SI paid a visit in Du Pont facilities in Bristol, England. The aim of the visit was to get acquainted with diffusion patterning technology and processing. Materials and processing equipment needed for the successful application of this technology for multilayer thick-film hybrids production was discussed. In the DuPont laboratory practical demonstration of technology was presented. To apply the above-defined technology, the necessary materials were specified and ordered. More details of the results are given in /61/.

The technical activities of IMEC, Belgium (IMEC.BE) are in connection with WP3, WP4 and WP5, and also IMEC.BE is the financial coordinator of the Project. First of all, IMEC.BE set up an automatic measurement system for measurements on substrates with test structures. The system consists of a switching matrix, 3 source-measurement units (SMUs), and an RLC impedance measurement unit. The devices under test are contacted using needle probes, or by insertion of the substrate in a special socket with 84 contact points. With the system measurements can be performed on passive test structures delivered by the Partners. In this way, the developed technologies can be validated.

For example, three identical test substrates were sent for measurements from TUB.HU. These substrates are square 50 mm x 50 mm FR4 boards, fitting into the test insertion socket. They carry a double-sided Cu metallization with Au finish. Tracks on front and backside of the substrate are connected by plated-through holes. On each substrate two test structures are present, namely daisy chains, consisting of a series interconnection of 200 plated-through holes. In one structure, small holes (A = 250μm), on the other, large size holes (A = 350μm) are used. The yield and resistance of the whole structure and parts of the structure were measured using a 4-point method. The results of the measurements on these interconnection substrates are used for the design and realization of test modules at UPB.RO and TUB.HU, and the test structures on these modules will then be measured at IMEC.BE.

The Welding Institute, United Kingdom (TWI.GB) is not Responsible Partner in any Work Packages, however, the contribution of TWI.GB and the activity of Prof. Nihal Sinnadurai as a consultant are very important to the success of the Project. During the first half of the Project TWI.GB

- attended inaugural meeting in Bled Slovenia, and helped set the direction for the project;
- hosted advisory meeting with WD.GB and provided guidance on scope for William Dennehy's activities;
- provided advice on MCM technologies;
- hosted meeting and discussion with TUB.HU on technology evaluation activities to be undertaken in the project;
- provided guidance to project consortium members on suitable equipment acquisition;
- hosted visit by TUB.HU to provide advice on reliability evaluation and training on wire bonding equipment;
- provided ongoing advice to WD.GB on MCM publications;
- provided on-line interactive advice and comments to UPB.RO on the choice of prototype designs and design approach for MCM-L;
- contributed in the work of Project Meetings and gave papers in the joint seminars /63-65/;
- last but not least, encouraged all Partners to participate in this European Conference on Multichip Modules /22,54,55,61/.

The general objective of William Dennehy Ltd., United Kingdom (WD.GB) in the first part of the Project has been to travel a steep learning curve in this subject area in order to apply its technical and statistical expertise in the improvement of the quality of processes used to produce fast prototyping low-cost MCM technology facilities in Eastern Europe for the benefit of European industry. Some success has been achieved in this objective with the significant assistance of Prof. Nihal Sinnadurai of TWI.GB and Prof. Zsolt Illyefalvi-Vitéz, and their teams. He presented a joint paper entitled "Analysis of a Multi-Stage Double-Sided Printed Circuit Board Production" written by L. Várnai of TUB.HU /67/. WD.GB also intends to analyze the design facilities in Romania and the ceramics and thick-film facilities in Slovenia.

Conclusions

Considerable progress has been made in the Project during its first half-time period. New software and equipment were installed and process technologies were upgraded to improve the design facilities at the Rumanian Partner, the printed circuit board (PCB) technology for MCM-Ls at Budapest, and ceramics technology skills for MCM-C in Slovenia. All Partners took part in seminars, conferences, exhibitions and published papers to obtain and disseminate information and knowledge about MCMs and other microelectronics technologies /4-67/. This also helps to safeguard and stabilize intellectual RTD potential of RO, HU and SI.

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STIKALNI MOČNOSTNI TONSKI OJAČEVALNIK

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Ključne besede: ojačevalniki močnostni stikalni tonski, D-razred ojačevalniki, ojačevalniki močnostni, način delovanja stikalni, ojačevalniki tonski, modulatorji pulzno širinski, pretvorniki stikalni, pretvorniki navzdol, sita nizkoprepustna, MOSFET elementi stikalni, pretvorniki mostični, pretvorniki močnostni, sheme blokovne, vezja električna

Povzetek: Članek opisuje izvedbo tonskega ojačevalnika v stikalni tehniki za ojačenje signalov v nizkofrekvenčnem področju od 10 do1000 Hz. Tako izvedbo ojačevalnika označujemo kot D razred delovanja, ki vsbuje štiri ločene stopnje: analogno vhodno stopnjo, pulzno širinski modulator, močnostnostikalno stopnjo in nizkoprepustno sito. Posebni povdarek je bil podan pri izvedbi močnostne izhodne stopnje, ki jo predstavlja mostični DC-DC pretvornik. Zanj smo uporabili študijo dinamičnega obnašanja z metodo povprečenja v prostoru stanj. Na podlagi te metode je ocenjena frekvenčna karakteristika izhodne stopnje ki jo predstavljata mostično DC-DC pretvorniško vezje ter sito z bremenom.

Switching Type Audio Power Amplifier

Keywords: switching type audio power amplifiers, Class-D amplifiers, power amplifiers, switching mode of operation, audio amplifiers, pulse width modulators, switching converters, down converters, lowpass filters, MOSFET switching elements, bridge converters, power converters, block diagrams, electrical circuits

Abstract: A Class-D amplifier which amplifies an analog input signal in the low frequency range from 10Hz to 1000Hz through pulse width modulation techniques is presented in this article. This frequency range which is only one part of audio frequency range is selected with active frequency switch. Class D amplifier can be easily explained in four stages; analog input stage, audio modulation stage, pulse width modulation power stage and low pass filtering stage. The audio modulation stage changes the analog input signal to a constant frequency, varying duty cycle. This operation is accomplished with integrated circuit SN3524. For power stage amplifier realization the experiences with DC-DC converters are used and for pulse width gain stage the DC-DC Buck converter with continuous input current in bridge configuration is used. The mode of operation is very similar to switch mode power suppliers. The main goal for this decision is better power efficiency over Class-AB power amplifiers and its reduction in heat dissipation. This is in audio power amplifiers of great importance just at low frequencies. Design requirements are as follows; output voltage 28 V on the load resistance of 8 Ohms and the switching frequency is 150 kHz. The simulation and experimental results of frequency response are presented. In the expected frequency range the output power of 100 W is obtained at total harmonic distortion of 2,3% and power efficiency of 87%. The increasing of the output power up to 1000 W is possible without difficulties.

1. Uvod

Klasični tonski ojačevalniki izdelani v analogni tehniki v A oziroma AB razredu imajo relativno male izkoristke. Posebej je to prisotno pri malih izkrmiljenjih. Glede na lastnosti tonskega signala lahko tudi pri izvedbi tonskih ojačevalnikov uporabimo stikalni način delovanja za doseganje večje moči na izhodu. Zato analogni signal s pomočjo pulzno širinskega modulatorja preoblikujemo v diskretni signal, ki ga neposredno ojačimo s stikalno izhodno stopnjo /2/. Izhodna stopnja z nizkoprepustnim sitom in zvočnik pa poskrbita za pretvorbo digitalnega signala spet v analogno obliko. Stikalni tonski ojačevalniki, ki jih označujemo tudi kot ojačevalnike moči v D razredu, omogočajo delovanje z zelo visokim izkoristkom tudi pri malih signalih, kar je njihova velika prednost /9/, /10/.

Iz izkušenj je znano, da je 80% moči tonskega signala prisotno v nizko frekvenčnem delu. Če z aktivno kretnico razdelimo celotni tonski signal že v predojačevalniku na področja nizko frekvenčnih, srednje frekvenčnih in visoko frekvenčnih signalov, bomo lahko posamezne signale ojačevali s posebnimi ojačevalniki. Srednje in visoke tone ojačujemo z manjšima tonskima ojačevalnikoma, narejenima v linearni, analogni tehniki. Nizke tone pa preko kretnice vodimo na stikalni tonski ojačevalnik.

V članku je opisan stikalni tonski ojačevalnik za ojačenje nizkofrekvenčnega tonskega področja med 10 Hz in 1 kHz. Sestavljen je iz štirih stopenj: analogne vhodne stopnje, pulzno širinskega modulatorja, močnostne izhodne stopnje in nizkoprepustnega sita. Močnostno izhodno stopnjo smo izvedli z mostičnim DC-DC pretvornikom, ki se sicer uporablja v pretvorniške in napajalne namene. Načrtali smo jo tako, da je imela izhodno moč 100 W, brez večjih težav pa bi izhodno moč lahko povečali do 1000 W. Za frekvenco delovanja stikalnega ojačevalnika smo izbrali 150 kHz, kar je najbolj uporabljana in priporočena frekvenca delovanja pulznoširinskih modulatorjev stikalnega ojačevalnika glede na pasovno širino /2/, /10/. Ker je bila uporabljena mostična izhodna stopnja, je bilo mogoče za dinamično analizo uporabiti metodo povprečenja v prostoru stanj. S tem smo delovanje mostičnega stikalnega pretvornika lahko opisali z delovanjem pretvornika navzdol /1/, /3/, /4/, /5/.

Delovanje pretvornika navzdol in njegova povezava z mostičnim stikalnim pretvornikom sta prikazani v drugem poglavju /1/. Projektiranje polprevodniških komponent izhodne stikalne stopnje je obdelano v tretjem poglavju. Obdelan je problem izbire močnostnih stikalnih elementov ter problem galvanske ločitve krmilnega signala od izhodne stikalne stopnje /6/, /8/. V četrtem poglavju smo analizirali frekvenčne odzive izhodnega sita, ki bistveno vpliva na frekvenčno mejo ojačevalnika in frekvenčni odziv celotnega ojačevalnika ter primerjali dobljene rezultate z obstoječimi standardi /7/.

Glede na funkcijo in uporabo ločimo dve vrsti ojačevalnikov v D-razredu. V prvo skupino sodijo ozkopasovni

ojačevalniki /11/, ki ojačujejo le vhodno napetost določene frekvence. Vhodno stopnjo imajo v obliki omejevalnika signala, ki vhodni signal pretvori le v pravokotno obliko.V drugo skupino sodijo širokopasovni ojačevalniki, njihovo delovanje je v blokovni obliki prikazano na sliki 1.1. Vhodni analogni signal vodimo na pulzno širinski modulator, ki nam ga pretvori v pravokotni signal. Tako dobljene napetostne impulze pravokotne oblike peljemo na stikalni ojačevalnik. Med ojačevalnikom in bremenom imamo nizkopasovno sito, ki nam izloči koristen signal iz pulznoširinskega močnostnega signala.

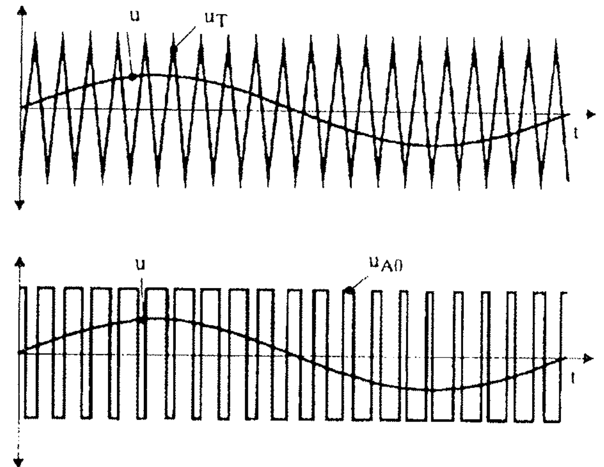
Slika 1.1: Širokopasovni ojačevalnik v D razredu

2. Vhodna stopnja

Vhodnastopnja je v bločni strukturi prikazana na sliki 2.1.

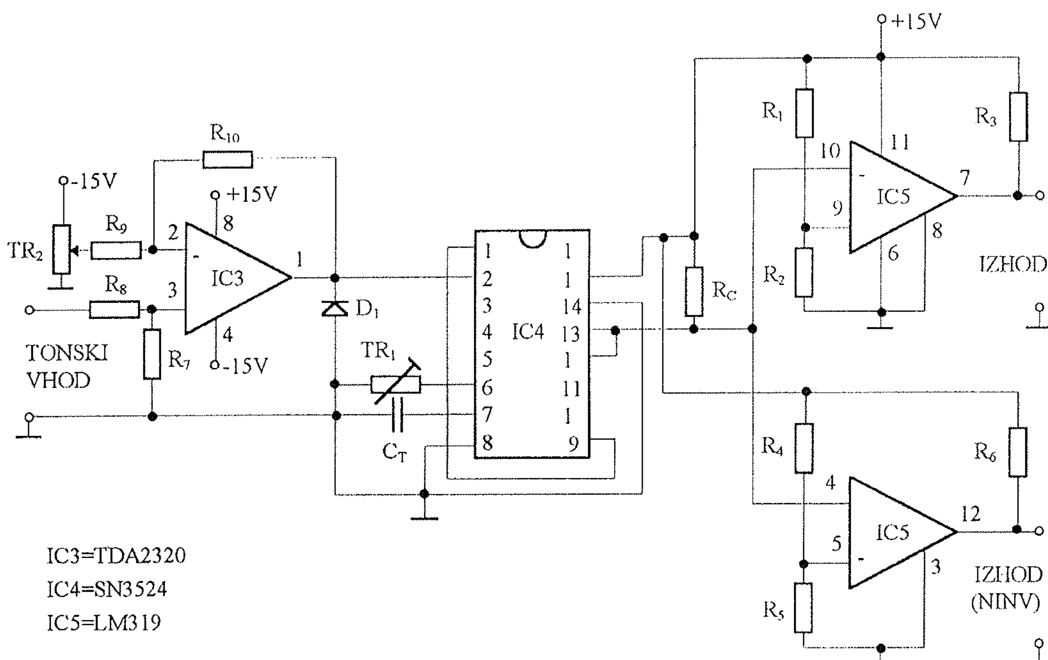
Slika 2.1: Blokovna shema vhodnega dela

Premik nivoja tonskega signala je potreben zaradi prilagoditve signala iz predojačevalnika na PŠM vezje. Prilagodilno vezje za krmiljenje prožilne stopnje je zgrajeno iz diskretnih elementov in nam signal fazno zamakne za 180°. Pomembno je, da so elementi zelo kvalitetni, saj je kvaliteta celotnega ojačevalnika močno odvisna od vhodnega dela. Celotna shema vhodnega dela je prikazana na sliki 2.2.



Slika 2.3: Princip PŠM
a) vhodni signal primerjamo s signalom trikotne napetosti
b) vhodni signal in izhodni pravokotni signal, ki se mu spreminja širina v odvisnosti od vhodnega

Jedro vhodnega dela predstavlja pulzno širinski modulator, ki spremeni analogni vhodni signal v digitalno obliko s konstantno frekvenco, pri čemer se spreminja prevajalno razmerje d. V osnovi je sestavljen iz primerjalnika, ki primerja posebej generirano trikotno vhodno napetost in vhodni analogni signal. Na izhodu primerjalnika dobimo impulze, katerih širina je linearno odvisna od vhodne napetosti. Princip pulzno širinske modulacije je prikazan na sliki 2.3.

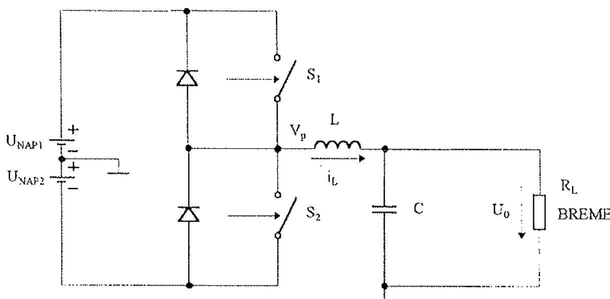


Slika 2.2: Vhodni del vezja

PŠM smo izvedli z integriranim vezjem SN3524 /8/, ki vsebuje poleg PŠM-ja še operacijski ojačevalnik na vhodu, ki se uporablja kot ojačevalnik pogreška, tokovni senzor, ki izklopi PŠM ob morebitni prekoračitvi nastavljenega toka, ter poseben priključek za prenapetostno zaščito. Vgrajen ima oscilator trikotnih impulzov, katerih frekvenco določimo z zunanjimi elementi in jo kasneje med delovanjem več ne spreminjamo. Operacijski ojačevalnik, ki služi kot tokovni senzor, ima na svojem invertirajočem vhodu termično stabilen izvor napetosti 200mV. Kadar padec napetosti zaradi toka, ki ga merimo kot napetost na znanem uporu R_S, prekorači to vrednost napetosti, PŠM preneha delovati. Slaba stran integriranega vezja je v tem, da je vhodno napetostno območje premaknjeno v pozitivno področje med 0,8V in 3,5V. Pri vhodni napetosti 0,8V je prevajalno razmerje d= 0%, pri vhodni napetosti 3,5V pa je d= 45%. Na izhodu integriranega vezja imamo še dva tranzistorja, ki imata dve funkciji. Prva je močnostno ojačenje z dovolj velikim izhodnim tokom, I=50mA, za krmiljenje enostavne izhodne stopnje druga pa invertiranje izhodnega signala iz PŠM. Ker je vhodna napetost našega ojačevalnika izmenična z amplitudo 2V, smo za pravilno krmiljenje PŠM izdelali ojačevalno vezje za premik napetostnega nivoja.

3. Močnostna izhodna stopnja

Za ojačenje pulzno širinskega moduliranega signala iz vhodne stopnje smo uporabili mostično izhodno stopnjo, ki je bila izvedena z dvema DC-DC pretvorniškima vezjema. Pretvorniško vezje deluje po principu pretorbe navzdol v področju zveznega toka in je prikazan na sliki 3.1. V izhodni mostični močnostni stopnji smo breme vezali na protifazna izhoda pretvornikov.



Slika 3.1: Pretvornik navzdol

Krmiljenje stikal S_1 in S_2 je izvedeno s stopnjo, ki ima en izhod invertiran. Preklapljanje je izvedeno s konstantno frekvenco f_S, spreminja se le prevajalno razmerje d. Izhodno napetost U_0 izračunamo z izrazom

$$U_0 = \frac{t_{ON}}{T_S} U_{NAP} = dU_{NAP} \quad (3.1)$$

kjer je U_0 izhodna napetost, t_{ON} je čas, ko je stikalo v sklenjenem položaju, T_S je čas trajanja periode in U_{NAP} je napajalna napetost. S spreminjanjem prevajalnega razmerja vplivamo na izhodno napetost. Ko je sklenjeno stikalo S_1, se energija pretaka iz izvora proti bremenu, ko pa je sklenjeno stikalo S_2, se breme napaja z energijo, ki je ostala shranjena v dušilki in kondenzatorju.Zaradi lastnosti stikalnih komponent v pretvorniku navzdol ločimo pri njem dva načina delovanja:

- zvezno področje delovanja, ko trenutna vrednost toka skozi tuljavo v periodi delovanja nikoli ne doseže vrednosti nič;
- nezvezno področje delovanja, področje trganega toka, trenutna vrednost toka skozi tuljavo v periodi delovanja doseže vrednost nič.

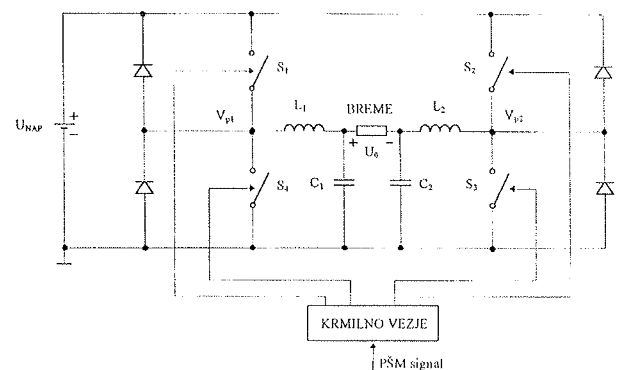
V primeru ojačevalnika v D razredu želimo zvezni način delovanja. Zanj je značilno, da tok skozi tuljavo izpolnjuje pogoj $i_L(t)>0$. Zvezno področje delovanja pretvornika navzdol se konča na meji med zveznim in nezveznim tokom. Mejo nezveznosti toka dosežemo, ko doseže tok tuljave ničelno vrednost natanko ob koncu periode. Temensko vrednost toka $\hat{i}_L$ lahko izrazimo s srednjo vrednostjo toka na meji zveznosti, ki jo bomo označili z I_{LM} /1/:

$$I_{LM} = \frac{1}{2}\hat{i}_L = \frac{1}{2}\frac{t_{ON}}{L}(U_{NAP} - U_0) = \frac{dT_S}{2L}(U_{NAP} - U_0) \quad (3.2)$$

V primeru, ko se izhodna napetost spreminja v mejah od 0V do U_{NAP}, I_{LM} vseeno pade na vrednost nič.

3.1 Mostična močnostna izhodna stopnja

Slika 3.2 kaže mostično močnostno izhodno stopnjo z bremenom in LC sitom. Mostični pretvornik in nizkoprepustni siti sta vezani simetrično. Izhodna napetost $U_p = V_{p1} - V_{p2}$ je plavajoča napetost. V praksi je $V_{p1} - V_{p2}$ visokofrekvenčni signal impulzne oblike. Siti izločita visokofrekvenčni signal s stikalno frekvenco.

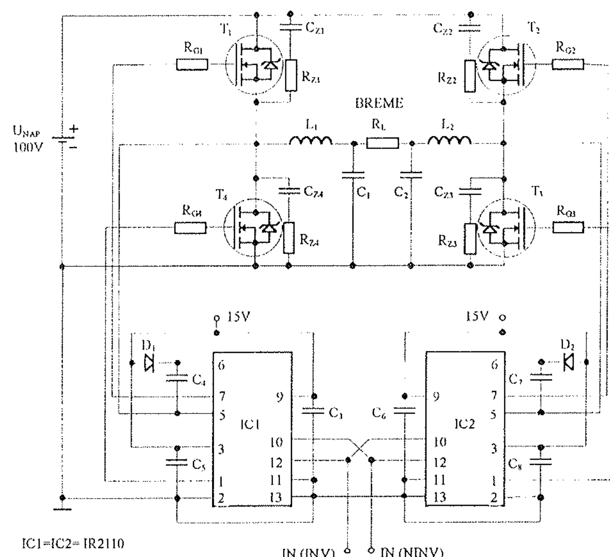


Slika 3.2: Mostični pretvornik

Mostična stopnja ima dve stanji: v prvem stanju sta stikali S_1 in S_3 sklenjeni, S_2 in S_4 pa razklenjeni. Potencial V_{p1} je enak U_{NAP}, V_{p2} pa je enak 0, v drugem stanju sta sklenjeni stikali S_2 in S_4, S_1 in S_3 pa ne. Potencial V_{p2} je enak U_{NAP}, medtem ko je V_{p1} enaka 0. Efektivni izhodni signal na bremenu dobimo s pomočjo izraza

$$U_0(t) = \frac{1}{T_S}\left(\int_0^{dT_S} U_{NAP}dt - \int_{dT_S}^{T_S} U_{NAP}dt \right) \quad (3.3)$$

Končno izvedbo mostične močnostne ojačevalne stopnje prikazuje slika 3.3. Močnostni del ojačevalnika je sestavljen iz dveh delov. V prvem delu imamo močnostne tranzistorje, ki so vezani v mostič. Ob vsakem tranzistorju imamo zaščitno razbremenilno vezje. Na plavajoče sponke mostiča imamo simetrično vezana izhodni siti. V drugem delu imamo integrirani vezji IC1 in IC2, ki služita za krmiljenje stikalnih tranzistorjev s tokom do 2A. Krmilna stopnja je izvedena z vezjem IR2110. To je visokonapetostno, zelo hitro MOS močnostno vezje z galvansko ločenim visokim in nizkim prožilnim izhodom. Logični vhodi so kompatibilni z standardnimi CMOS izhodi ali z LSTTL izhodi z uporabo dvižnih uporov. Izhodni gonilniki so nizkoohmski za kratkočasne tokovne konice. Plavajoči kanal je lahko uporabljen za proženje N-kanalnih močnostnih MOSFET ali IGBT. Pri tako izbrani prožilni stopnji, vezje IR 2110 dovoljuje tudi 500V priključene napetosti na tranzistorje. Med izhodom integriranih vezij in vrati tranzistorjev imamo vezane upore, ki nam omejijo trenutne tokove ob vklopu in zmanjšajo možnost uničenja integriranega vezja v času prehodnih pojavov.



Slika 3.3: Shema močnostnega dela ojačevalnika

Pri preklapljanju induktivnih tokokrogov pride do pojava, ko kljub izklopljenemu tranzistorju ni možna nenadna sprememba toka. Ta pojav nam povzroča dodatne stikalne izgube na tranzistorjih. S pomočjo preprostega kriterija /3/

$$t_{ON} + t_{OFF} \leq \frac{T}{10} \qquad (3.4)$$

smo določili najkrajši čas periode in s tem najvišjo dovoljeno frekvenco preklopov. Morda je kriterij (3.3) na prvi pogled nekoliko prestrog, vendar se moramo zavedati, da na stikalnem elementu nastajajo stikalne izgube, ki so lahko tudi večje od prevodnih izgub. Pri tranzistorjih, ki smo jih uporabili pri našem ojačevalniku, je bila vrednost vsote časov vklopa in izklopa 465ns, kar določa najvišjo frekvenco delovanja stikalnega vezja 215kHz.

Za izboljšanje lastnosti D-razreda ojačevalnika (nelinearna popačenja, popačenj zaradi PŠM) bi morala biti stikalna frekvenca 150 krat večja od najvišje frekvence želene pasovne širine signala /10/. Za Hi-Fi tonske ojačevalnike, ki imajo zgornjo frekvenčno mejo pri 20kHz bi to pomenilo, da bi bila stikalna frekvenca D-razreda ojačevalnika v tem primeru 3MHz. Za takšen ojačevalnik pa je težko najti tranzistorje, ali pa so ti zelo dragi. Pri izvedbi našega ojačevalnika, ki ojačuje le frekvenčni pas od 10Hz do 1kHz smo izbrali frekvenco 150kHz, saj smo pri pregledu literature /2/ ugotovili, da tudi drugi avtorji uporabljajo takšne vrednosti.

Za stikalne elemente smo uporabili MOSFET tranzistorje. Prednost MOSFET močnostnih tranzistorjev pred bipolarnimi je predvsem v področju višjih stikalnih frekvenc. Izvedba krmiljenja je dokaj preprosta. Krmilimo jih v bistvu napetostno, vendar ne smemo pozabit tudi na polnjenje parazitnih kondenzatorjev C_{GS}, ki so prisotni med vrati (G) in izvori (S). Za manjše stikalne čase je potreben večji krmilni tok. Iz enačbe (3.4) lahko izračunamo amplitudo toka, ki je potrebna ob vklopu tranzistorjev /5/

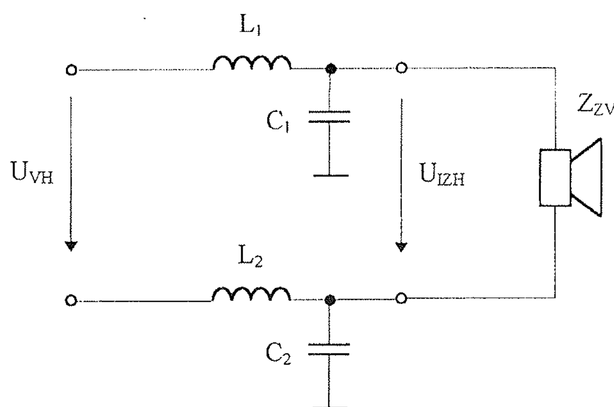
$$U_{GS} C_{GS} = I_K t_{vk} \qquad (3.5)$$

4. Nizko prepustno sito

Nizko prepustno sito predstavlja obenem vezje za digitalno analogno pretvorbo pulzno moduliranega visokofrekenčnega signala. Običajno se uporablja Butterworthovo sito druge stopnje z L in C elementom. Prenosno funkcijo sita nam podaja izraz

$$\frac{U_{IZH}}{U_{VH}} = \frac{1}{s^2 + \sqrt{2}s + 1} \qquad (4.1)$$

Zaradi mostične vezave izhodne stopnje sito ustrezno razdelimo kot je prikazano na sliki 4.1. Vrednosti za posamezni tuljavi in kondenzatorja dobimo s primerjavo prenosne funkcije vsakega posameznega vezja in izraza (4.1).



Slika 4.1: Izhodno sito polnomostičnega ojačevalnika

Izbira tuljave in kondenzatorja predstavlja kompromis tudi glede na dovoljeno valovitost /1/. Valovitost napetosti izračunamo iz

$$\frac{\Delta U_0}{U_0} = \frac{\pi^2}{2}(1-d)\left(\frac{f_0}{f_s}\right)^2 \quad (4.2)$$

kjer je

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \quad (4.3)$$

Tuljavi L_1 in L_2 sta prvi energijski posodi v izhodnem situ. Njeni induktivnosti morata biti čim večji, to pomeni manjšo valovitost izhodnega toka okrog želene vrednosti; shraniti morata toliko energije, kolikor jo potrebuje breme v eni periodi; njune fizične dimenzije morajo biti čim manjše, ker to pomeni prihranek prostora in denarja, linearni del histerezne zanke mora biti dovolj velik, da med delovanjem ne bi zašli v nasičenje.

Kondenzatorja C_1 in C_2 sta druga od elementov, ki sta sposobna skladiščiti energijo. Vendar pa v naši aplikaciji nimata tako velikega pomena kot dušilka. Kondenzator skrbi bolj za glajenje izhodne napetosti. Kapacitivnosti ne smemo večati v nedogled, saj s tem nižamo zgornjo frekvenčno mejo. Pri izbiri želenega kondenzatorja smo se srečali še z enim problemom. Zraven omejitve, da mora ustrezati napetostnim zahtevam, imajo kondenzatorji, ki so namenjeni za stikalno uporabo, tudi podatek o maksimalni dopustni spremembi napetosti na njem, du/dt. Iz enačbe

$$i_C = C\frac{du_C}{dt} \quad (4.4)$$

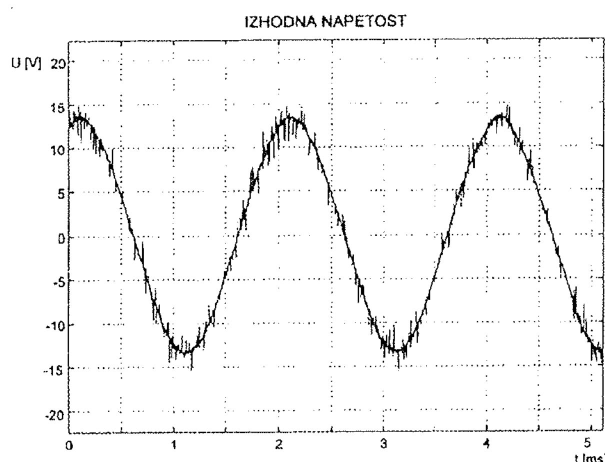
vidimo, da nam ta podatek podaja maksimalni tok, s katerim lahko polnimo kondenzator. Seveda je to za nas pomembno, saj polnimo kondenzator v zelo kratkih intervalih in so tokovne konice lahko precej visoke. Zato smo izbirali le med kondenzatorji, ki so namenjeni za stikalne namene, saj imajo le-ti du/dt bistveno večji od običajnih kondenzatorjev.

5. Rezultati

Prenosna funkcija pretvornika je podana z /1/

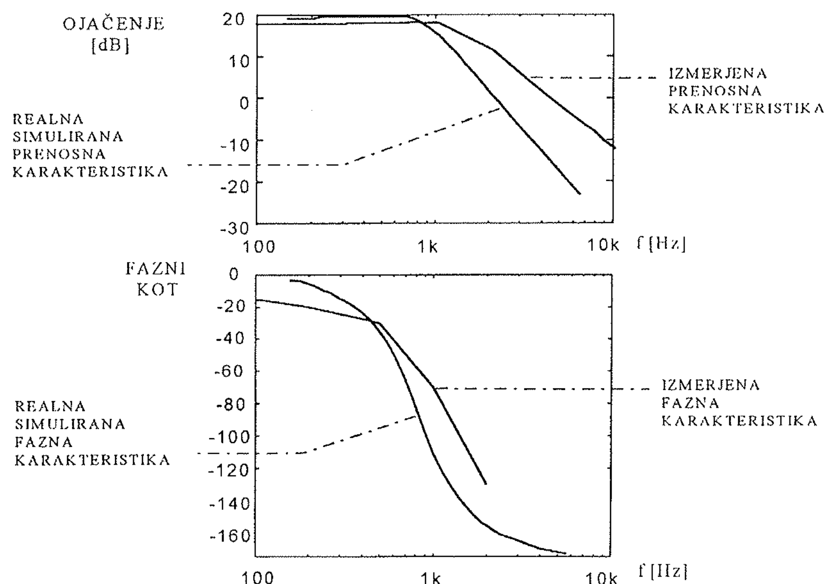
$$\frac{U_0(s)}{d(s)} = \frac{dU_{NAP}}{s^2LC + s\frac{L}{R} + 1} \quad (5.1)$$

Na sliki 5.1 je prikazan simulirani in izmerjeni amplitudni in fazni frekvenčni odziv celotnega vezja.



Slika 5.2: Časovna oblika izhodnega signala s frekvenco 500Hz na bremenu

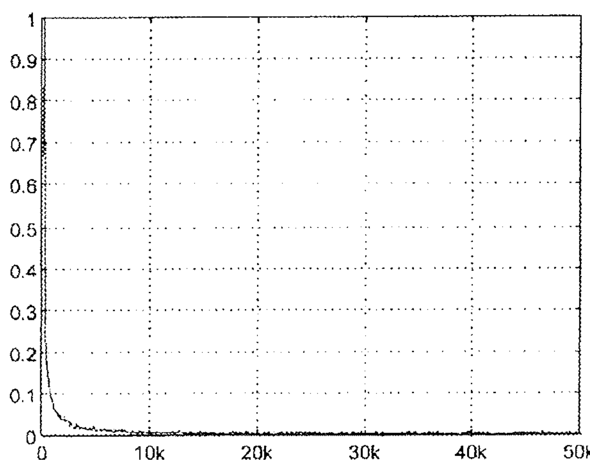
Če primerjamo izmerjeno in simulirano prenosno karakteristiko vidimo, da se dokaj dobro ujemata.



Slika 5.1: Frekvenčna in fazna karakteristika

Razlika je v strmini upadanja ojačenja in faze. Pri simulaciji prenosne karakteristike je upoštevana še serijska izgubna upornost tuljave in kondenzatorja.

Rezultati meritev izhodnega signala so prikazani na naslednjih dveh slikah. Na sliki 5.2 je izrisana časovna oblika signala na bremenu, ki ima frekvenco 500Hz, na sliki 5.3 pa je izrisan normirani frekvenčni spekter. Iz njega vidimo razmerje med osnovno harmonsko komponento in višjimi harmonskimi komponentami, ki s frekvenco močno upadajo.



Slika 5.3: Normirani frekvenčni spekter izhodnega signala

6. Zaključek

V članku je opisano načrtovanje in izdelava nizkofrekvenčnega tonskega ojačevalnika v stikalni izvedbi za izhodno moč 100 W. Pri impedanci bremena 8Ω smo imeli izhodno napetost 28V, tok skozi stikalno stopnjo je bil 3.6A. Stikalno frekvenco smo izbrali 150 kHz. Pri delu smo uporabili izkušnje s pretvorniškimi vezji in za izhodno močnostno stopnjo uporabili mostično vezavo dveh DC-DC pretvornikov. Z ojačevalnikom v stikalni izvedbi dosežemo boljši izkoristek vezja, brez večjih problemov pa bi lahko izdelali ojačevalnik z močjo do 1000 W. Izmerjeni rezultati kažejo zaenkrat še določeno slabost v razmeroma velikem nelinearnem popačenju, izmerjeni faktor popačenja THD je znašal 2.3%, ter v povzročanju stikalnih visokofrekvenčnih motenj. Izmerjena frekvenčna karakteristika se lepo ujema s postavljenimi zahtevami, spodnja frekvenčna meja je pod 10Hz, zgornja frekvenčna meja pa je 1kHz. Izkoristek smo izmerili pri polovični koristni moči na izhodu in znaša 87%. Zaradi male potrošnje moči na tranzistorjih so lahko hladilna telesa tranzistorjev majhnih dimenzij. To je prav tako pomembna prednost stikalnega delovanja ojačevalnika.

Posebnost stikalnega načina delovanja mostičnega stikalnega pretvornika s plavajočim izhodom je tudi v tem, da je valovitost napajalnega izvora precej izločena iz izhodnega signala in v običajnih primerih zato ni potrebna posebna stabilizacija enosmernega izvora. To nam omogoča dodatno zmanjšanje izgub, velikosti, kompleksnosti in cene ojačevalnika.

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CONSIDERATIONS OF IEEE 1149.4 STANDARD IN ANALOG DESIGN

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Keywords: IEEE standards, IEEE 1149.4 standards, boundary-scan tests, DFT, Design For Testability, analog circuits, digital circuits, mixed circuits, mixed-signal tests, analog/digital circuit tests, interconnect tests, parametric tests, internal tests, ATE, Automatic Test Equipment, JTAG, Joint Test Action Group, TAP, Test Access Port, TCK, Test ClocK, ABM, Analog Boundary Modules, TBIC, Test, Bus Interface Circuit, ATAP, Analog Test Access Port

Abstract: The paper gives a brief introduction to the emerging Standard for Mixed-Signal Test Bus described by the P1149.4/D25 draft. The aim is to provide standardized approaches to interconnect test, parametric test and internal test of a printed circuit board including mixed-signal devices. In the paper, the main features of the proposed standard are described and the results of an experimental case study using the IEEE 1149.4 KLIC Test Chip are summarized.

Upoštevanje standarda IEEE 1149.4 pri načrtovanju analognih vezij

Ključne besede: IEEE standardi, IEEE 1149.4 standardi, preskusi robni, DFT snovanje na preskusljivost, vezja analogna, vezja digitalna, vezja mešana, preskusi parametrični, preskusi notranji, ATE oprema za preskuse avtomatska, JTAG skupina delovna za preskušanje spojev, TAP vrata dostopna preskusa, TCK ura preskusna, ABM moduli robni analogni, TBIC vezje vmesniško vodila preskusnega, ATAP vrata za preskus analogni

Povzetek: Članek podaja kratek uvod v nastajajoči Standard testnega vodila mešanih digitalno/analognih vezij predstavljenega v delovni dokumentaciji P1149.4/D25. Cilj predlaganega standarda je ponuditi standardiziran pristop k izvedbi testiranja povezav, parametričnega testa in notranjega testa tiskanine opremljene z digitalno/analognimi integriranimi vezji. Opisane so glavne značilnosti predlaganega standarda in povzeti rezultati eksperimentalne študije uporabe testnega integriranega vezja IEEE 1149.4 KLIC.

1. Introduction

Increasing complexity and greater miniaturization are rapidly reducing the ability to test printed circuit boards effectively. Traditional in-circuit test techniques utilize a bed-of-nails to make contact to each individual lead on a printed circuit board. With the introduction of surface mounted devices, small pitch packaging becomes prevalent which makes the access to the test points on the board either impossible or at least very costly. Furthermore, as device and board functionality grow, the test process is becoming more difficult.

The need for an alternative access approach gave the idea of somehow building the test probe directly into the silicon chip. In other words, the proposed solution was to build parts of the test equipment into the actual circuits. The effort of a group of ATE makers and EDA tool suppliers organized as the Joint Test Action Group (JTAG) resulted in a boundary-scan test technique for digital circuits and systems. In 1990 it was approved by the IEEE as standard 1149.1, /1/. The standard is now widely supported by major manufacturers of ICs and ASIC vendors.

Boundary scan was developed first for digital components and boards. This was due to the fact that the problem is more tractable in digital than analog or mixed-signal domain. In contrast to the digital circuits, analog components are specified by a continuous range of parameters rather than two discrete logical values 0 and 1. Besides, their interconnections may comprise networks of other analog components rather than simple wires. In order to tackle the problem, the development of analog boundary-scan has started in 1991. The work is coming to a close after the second ballot in March 1999. It is realistic to expect that the current Draft Standard for a Mixed-Signal Test Bus P1149.4/D25 /2/ will be approved by the IEEE as standard 1149.4 in the following months.

In this article we first briefly describe the main idea of the IEEE 1149.1 standard. Next, we summarize the basic features of P1149.4 Mixed-Signal Test Bus and point to some useful references related to this document. In the second part, experiments with IEEE 1149.4 KLIC Test Chip are reported. At the end, some concluding remarks are drawn.

2. IEEE 1149.1 Standard

The principle of the boundary-scan technique is to place a shift register boundary-scan cell adjacent to each component pin and to interconnect the boundary-scan cells in order to form a chain around the border of the chip logic design. During the test mode, boundary-scan cells are used to control the status or read the states of the pins, while during the normal mode the cells are transparent. Components of a board that are fitted with the test structure of the IEEE 1149.1 standard are interconnected by way of the standard interface with the 4-wire test bus providing serial input data, serial output data, clock and mode select line. Addition of the boundary-scan logic has the following principal tasks: it allows normal circuit operation, it allows data to be shifted in or test results to be shifted out, and it provides a number of circuit tests. The following test modes are normally supported:

- external test (i.e., test of interconnections of the board),
- sample test (i.e., a snapshot of the states of boundary-scan supported pins during the normal operation of the board),

- bypass (i.e., a shortcut of a boundary-scan path of the board),
- built-in self-test at the chip level.

In addition, IC manufacturers usually provide more testing facilities by offering the user a set of non-mandatory boundary-scan operations.

The IEEE 1149.1 Standard defines the following basic hardware elements:
- the Test Access Port (TAP),
- the TAP Controller,
- the Instruction Register,
- different Test Data Registers.

An IC compliant with IEEE Std 1149.1 must include TAP, TAP Controller, IR and the mandatory Test Data Registers: Boundary-Scan Register and Bypass Register, as shown in Figure 1.

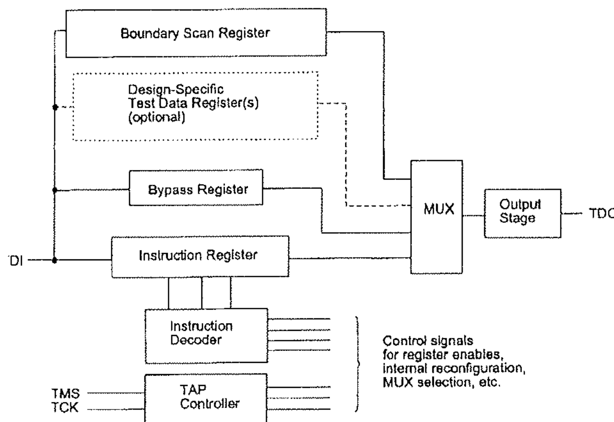

Figure 1: The standard boundary-scan architecture

The TAP Controller is a sequential circuit, its operation is controlled by the signals through the TAP. TAP consists of four mandatory connections (Test Clock Input, Test Mode Select Input, Test Data Input and Test Data Output) and one optional (Test Reset Input). Thus, any IC conforming with IEEE Std 1149.1 has at least four additional pins.

The TAP Controller generates clock and control signals required for the operation of the Instruction Register and the Test Data Registers in order to:
- provide signals for loading the instructions into the Instruction Register,
- provide signals for shifting data into and out of the Test Data Registers,
- perform test actions (i.e., capture data, shift data, update data).

The operation of the TAP Controller is given by the state diagram which defines the test protocol. IEEE Std 1149.1 prescribes three mandatory instructions: Bypass, Sample/Preload and Extest.

The purpose of the Bypass instruction is to shorten the scan path through the boundary-scan architecture when scan access of the test data registers is not required.

The Sample/Preload instruction is used to scan the Boundary-Scan Register during the normal circuit operation (i.e., not in the test mode!). Its execution does not interfere with circuit's normal operation, hence this option may be very useful for system debugging.

The Extest instruction allows test of board interconnections (i.e., test of opens, shorts or bridging faults).

In addition, a number of non-mandatory instructions may also be provided. Some typical representatives are: Runbist (which runs a built-in self-test of a circuit), Idcode (which allows reading of the circuit's identification code and thus permits blind interrogation of the assembled components on a board), Intest (which allows slow speed testing of the core of a circuit), etc.

Limited space prevents us to go further into details. The reader can find a good introduction to the boundary-scan test technique and the associated standard in /3/.

3. Emerging IEEE 1149.4 Standard

The aim of the proposed standard for a Mixed-Signal Test Bus described in the P1149.4 document is to provide standardized approaches to interconnect test, parametric test and internal test. For the first objective, the aim is to provide facilities that allow to detect opens in the interconnections between integrated circuits, and to detect and localize bridging faults. The test structure should allow interconnect testing in full compatibility with IEEE 1149.1 Std. The second objective refers to the problem of measuring the values of discrete components such as pull-up resistors, filter capacitors, etc., that are often interposed between integrated circuits on a board. The third objective relates to the ability to perform internal test of a component. An internal test of a complex component mounted on a board may result in a rather costly testing procedure, hence this option of the proposed standard is not mandatory.

As a whole, P1149.4 can be regarded as an extension of IEEE 1149.1 Std. The 1149.4 extensions are analog boundary modules (ABMs) on every analog functional pin and optionally on other functional pins. Functional pins with ABMs can be accessed via internal analog test bus consisting of 2 lines (AB1, AB2). The bus is connected to the Analog Test Access Port (AT1, AT2) through the Test Bus Interface Circuit (TBIC).

The boundary modules associated with the digital pins are identical to the boundary cells as specified in IEEE 1149.1 Std.

The test register structure is essentially identical to the one defined in IEEE 1149.1 Std. The only difference concerns the boundary-scan register which in the case of P1149.4 contains additional shift-register stages for the control of ABMs and TBIC.

The structure of a basic 1149.4 chip is shown in Fig. 2.

The functional schematic of the ABM module, connected to each analog function pin, is shown in Figure 3. The ABM module consists of six conceptual switches SB1, SB2, SH, SL, SG and SD. (A conceptual switch is defined as a circuit feature that allows two circuit nodes to be electrically connected or disconnected. The conceptual switch is controlled by a digital control signal.)

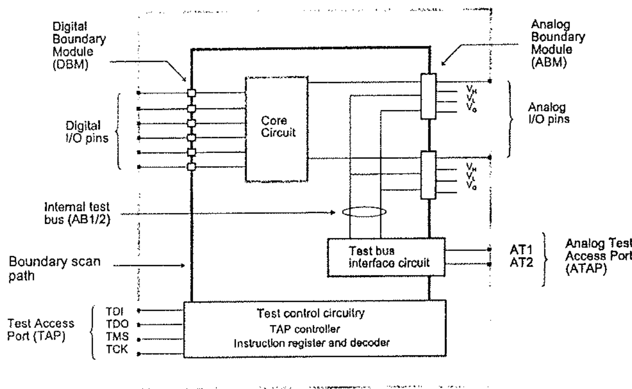

Figure 2: The structure of a basic 1149.4 chip

SB1 and SB2 are used to connect the pin to the internal analog test bus lines AB1 and AB2. In this way, Analog Test Access Port lines AT1 and/or AT2 can be connected to any component pin without the need of physical probing. (The above stated goal of somehow building the test probe directly into the silicon chip is thus achieved by the "virtual probe" feature provided by the ABM framework.) This structure is used to perform component measurements.

A digitizer with a threshold voltage VTH is included in the ABM. It is used to interpret voltages on the pin as digital ones and zeros. This feature can be used for the detection of bridging faults in the interconnect test.

SH and SL are used to set either of two voltage levels (VH or VL) on the pin. This feature allows simple interconnect testing on analog pins to take place at the same time, and using the same methods, as digital interconnect testing.

SG is provided to allow the pin to be connected to the reference quality voltage VG. This feature is used for measurements of board components connected between function pins supported by the AMS modules.

The fifth switch, labeled CD is the core disconnect facility. It provides a controllable mechanism for disconnecting the analog core from the analog function pin while external testing is taking place. From the implementation point of view, it is imperative that the additional series impedance due to the CD is still acceptable for the circuit normal operation.

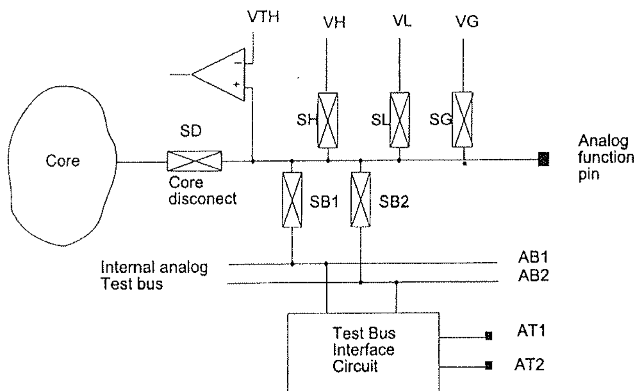

Figure 3: ABM switching structure

Each component conforming to P1149.4 must provide the mandatory instruction: Probe. This instruction allows analog pins to be monitored on AB2, and/or stimulated from AB1 during the normal operation. In order to provide the compatibility with IEEE 1149.1 Std, the mandatory instructions Bypass, Sample/Preload and Extest are also included. The proposed standard allows optional user-defined instructions as well as optional instructions defined in IEEE 1149.1 Std.

P1149.4 document also covers the aspects of measurement methodology. The principles of simple interconnect testing (i.e., testing of open circuits and bridging faults), extended interconnect testing (i.e., measurements of individual analog components) and simple network measurements (when more general networks are connected between the 1149.4 compliant components) are described. For more complicated cases, a special metrology has been developed by Parker et al /4/.

It should be mentioned that P1149.4 also defines differential analog boundary-modules for analog differential pins. However, detailed description of this subject and the associated testing principles are beyond the scope of the paper. Furthermore, analog parametric limits are discussed in the P1149.4 document, including switch limitations, problems associated with incorporation of electrostatic protection, measuring performance and calibration.

For experimental purposes, a series IEEE 1149.4 test chips have been manufactured and distributed by the working group to the interested parties. The samples granted to Jožef Stefan Institute were used for the experimental case study of the possible application of the emerging IEEE 1149.4 Std in the products of Hipot Hyb, /5/. In the following we summarize some experimental results.

4. Experiments with IEEE 1149.4 KLIC Test Chip

Experiments have been performed using the IEEE 1149.4 KLIC Test Chip /6/ in an active RC filter implemented in thick-film hybrid technology. The goal was to analyze the influence of IEEE 1149.4 ABMs on the circuit performance. For the case study we have chosen an active RC notch filter (as a part of a thick-film hybrid circuit for a telecommunication application) with quite exacting characteristics. The impact of non-ideal opamp on pole and zero locations is considered in the early design phase and finally compensated by trimming the resistor(s) in the production process. The introduced ABMs have additional impact on filter characteristics. The question is, how much do they actually influence circuit performance, and if it is possible to compensate their impact in practice. In our case we inserted ABMs in the circuit as shown in Figure 4 and measured amplitude and phase characteristics. Since the characteristics depend on the amplitude of the input signal, we made measurements at two different input signals (Vin = 20 mV and 100 mV).

In the case when only ABM1 was inserted, the central frequency f0 shifted towards higher frequencies and the gain at f0 increased. For the input signal Vin = 100 mV,

the frequency shift of f0 was 0.3%, and the gain has increased for 2.12 dB. At the lower input signal Vin = 20 mV, the frequency shift was a little smaller (about 0.01%), and the gain at f0 changed for 2.37 dB. The changes are due to the capacitive effect of the inserted ABM1, while the serial resistance of the ABM1 module can be neglected.

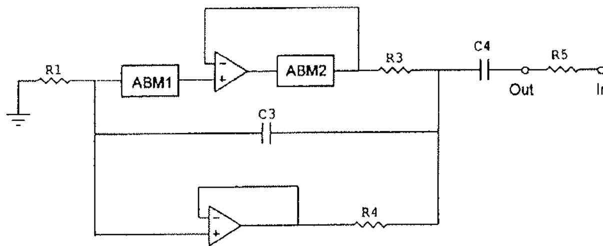

Figure 4: active RC notch filter with inserted ABMs

In the case when only ABM2 was inserted, the central frequency f0 slightly shifted towards higher frequencies and the gain at f0 decreased. The changes are due to the on-resistance of the ABM2, while its capacitive effect can be neglected.

Figure 5 depicts situation when both ABM1 and ABM2 were inserted and Vin = 20 mV. Note that the change of circuit characteristic was smaller than in the cases when only ABM1 or ABM2 were employed. This is due to the fact that the impact of ABM1 and ABM2 on the filter quality partially compensate.

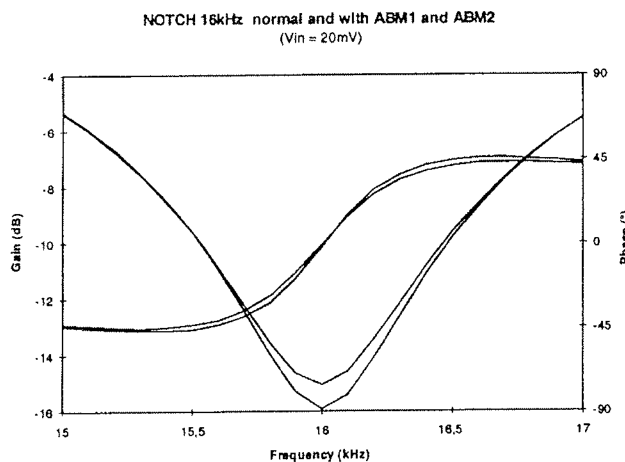

Figure 5: Measured frequency and gain when both ABM1 and ABM2 were inserted

In our case, the resulting changes of the central frequency f0 are not critical since they can be easily adjusted. Hence the application of IEEE 1149.4 in this particular case is feasible.More efforts would be needed to achieve the required quality in the case of high performance circuits (narrow tolerance ranges).

Conclusion

Boundary-Scan has proved to be an effective test technique for digital circuits and systems and its standard IEEE 1149.1 has been widely accepted in practice. Likewise, we can expect a similar success of the emerging IEEE 1149.4 in the area of mixed-signal circuits. The costs of implementing include 1149.1 TAP controller (resulting in area overhead), extra pins (at least 4 for compatibility with IEEE 1149.1 plus 2 for the analog test bus) and some inevitable performance degradation due to the additional capacitance and resistance of individual parts of ABMs, /7/. On the other hand, the benefits of increased testing facilities and diagnosability are likely to outweigh the costs and P1149.4 is likely to become essential solution for automatic test of mixed-signal circuits and systems. Let us conclude this brief introduction to P1149.4 with a daring idea stated at the International Test Conference 1997 by Steve Sunter, one of the members of the 1149.4 working group: "Just as the Internet evolved into the World Wide Web, and high performance sound, graphic, and programming were developed for the medium, we can expect to see dramatically better design and test solutions developed to fit into the P1149.4 framework. The Internet and 1149.4 might eventually link together!" /8/.

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VPLIV DOPANTOV NA MAGNETNE LASTNOSTI MnZn FERITOV

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Ključne besede: keramika magnetna, Mn-Zn feriti, dopanti, CaO oksidi kalcijevi dopanti, lastnosti magnetne, lastnosti električne, mikrostrukture, meje med zrni, materiali sintrani, atmosfera kisikova, tokovi vrtinčni, zrna feritna, prostor med zrni, rezultati eksperimentalni

Povzetek: Raziskali smo mikrostrukturne parametre in magnetne lastnosti Mn-Zn feritov, dopiranih z različnimi vsebnostmi CaO ter sintranih v atmosferah z različno vsebnostjo kisika. Rezultati kažejo, da so količine CaO na mejah med zrni, vsebnost kisika v atmosferi sintranja, povprečna velikost feritnih zrn in elektromagnetni parametri feritnih materialov močno soodvisni. CaO, ki se vgrajuje v meje med zrni med procesom sintranja, bistveno vpliva na razvoj mikrostrukture, magnetno permeabilnost in močnostne izgube Mn-Zn ferita.

Effect of Dopants on the Magnetic Properties of MnZn Ferrites

Key words: magnetic ceramic, Mn-Zn ferrites, dopants, CaO dopants, magnetic properties, electrical properties, microstructures, grain boundaries, sintered materials, oxygen atmosphere, eddy currents, ferrite grains, intergranular volume, experimental results

Abstract: The microstructal development and magnetic properties of Mn-Zn ferrites doped with various amounts of CaO sintered in an atmosphere containing various oxygen concentrations was investigated. The results indicate a strong link between the amount of CaO segregated in the grain boundary, the oxygen concentration during sintering, average grain size and the properties of the Mn-Zn ferrites. The CaO which segregates in the grain boundary during sintering governs the microstructal development and consequently the magnetic permeability and power loss of Mn-Zn ferrites.

1. Uvod

Feriti so keramični materiali, ki poleg osnovnih lastnosti keramike izkazujejo tudi specifične elektromagnetne lastnosti. Mikrostruktura in sestava mej med zrni bistveno vplivata na fizikalne in elektromagnetne parametre Mn-Zn feritov. Nizkoizgubni koeficienti feritnih materialov v primerjavi s klasičnimi kovinskimi lameliranimi jedri omogočajo njihovo vgradnjo tudi v različne visokofrekvenčne aplikacije, kjer klasična kovinska jedra zaradi visokih izgub niso več uporabna. Z vidika trendov na področju elektronske industrije, predvsem na področju videoteleinformatike, prenosne telefonije, satelitskih komunikacij, računalniške industrije, so nizkoizgubni močnostni Mn-Zn feriti tržno najbolj perspektivni materiali, zato je v zadnjem obdobju velik poudarek na razvoju novih nizkoizgubnih Mn-Zn feritov za visoko-frekvenčna področja.

Upornost mej med zrni zmanjšuje izgube na račun vrtinčnih tokov. Ta efekt je posebno pomemben, ko prehajamo v višja frekvenčna področja. Analize sestave feritnih zrn med procesom sintranja so pokazale, da se CaO vgrajuje na meje med zrni in tako bistveno zmanjšuje vrtinčne tokove (1). Vzporedni dodatki CaO in SiO_2 so pokazali še večjo učinkovitost večanja upornosti, ki je posledica vgrajevanja $CaSiO_3$ na meje med zrni (2,3). Neustrezna koncentracija CaO in SiO_2 in nepravilni atmosferski in temperaturni pogoji v fazi ohlajanja povzročajo prekomerno rast zrn, nižjo električno upornost ferita, ob enem pa se zvišajo močnostne izgube. V literaturi je objavljenih nekaj prispevkov o vgrajevanju Ca^{2+} na meje med zrni, povezanih z magnetnimi lastnostmi, kot sta magnetna permeabilnost (7) in upornost mej med zrni (4, 5, 6). V predhodnih raziskavah (10) in testiranjih smo ugotovili, da je gradient koncentracije Ca^{2+} po prostornini ferita občutljiv na procent kisika v atmosferskih pogojih sintranja, katerega merilo je tudi delež FeO v sintranem Mn-Zn feritu (8).

Magnetne izgube Mn-Zn feritov dopiranih s CaO so v literaturi delno že obdelane. Malo pa je znanega o povezavi pogojev priprave ferita, razvoja mikrostrukture, sestave mej med zrni in močnostnih izgubah visokofrekvenčnih Mn-Zn feritov.

Namen dela je bil zato ugotoviti pomembne mikrostrukturne parametre pri razvoju nove kvalitete močnostnega Mn-Zn ferita dopiranega s CaO v kombinaciji z dodatki TiO_2 in SnO_2 ter sovpliv med lastnostmi mej med zrni in končnimi izgubami.

2. Eksperimentalni del

Pripravljeni so bili vzorci z osnovno sestavo $Mn_{0,66}Zn_{0,27}Fe_{2,07}O_4$ dopirani z 0,3 mol. % SnO_2; 0,2 mol. % TiO_2 ter različnimi vsebnostmi CaO. Vhodne surovine Fe_2O_3, Mn_3O_4 in ZnO smo suho homogenizirali in kalcinirali pri temperaturi 1000 °C. CaO je bil dodan v fazo mletja. Vzorec 1, ki je vseboval 0,14 ut. % CaO smo mleli v vodovodni vodi, vzorec 2, ki je vseboval 0,14 ut. % CaO smo mleli v destilirani vodi, vzorca 3 in 4, katerim nismo dodali CaO pa smo mleli v vodovodni in destilirani vodi. Povprečne velikost zrn ferita po mletju je bila 1,1 μm (Granulometer HR 850 - CILAS). Feritno suspenzijo smo posušili s kombinacijo organskega vezivnega sistema PVA / PEG. Končno vsebnost CaO v sintranem Mn-Zn feritu smo določili s pomočjo ICP - AES. Določene vsebnosti so bile 0,14 ut. % (vzorec 1), 0,123 ut. % (vzorec 2), 0,021 ut. % (vzorec 3) in 0,0098 ut. % (vzorec 4). Koncentracija CaO v vodovodni vodi je znašala $1,5*10^{-3}$ g/l .

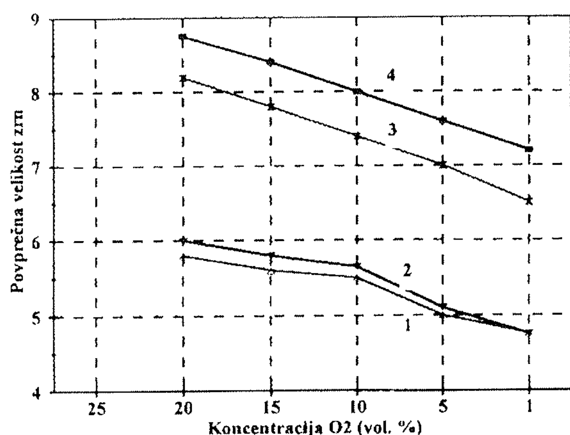
Toroidalno feritno jedro z izmerami zunanjega premera 22, notranjega premera 14 in višino 7 mm smo sintrali v računalniško vodeni peči pri temperaturi 1280 °C in pri različnih koncentracijah kisika in sicer: 21 vol. %, 10 vol. %, 5 vol. % in 1 vol. %. Sintranim vzorcem smo določili gostoto s pomočjo Hg - volumetra, vsebnost FeO s kemijsko analizo, mikrostrukturne parametre s pomočjo mikrofotografske analize jedkanih feritnih površin. Povprečna velikost zrn je bila določena z modelom za polavtomatsko kvantitativno ocenjevanje fotografij.

Gradient koncentracije Ca^{2+} v mejah med zrni smo določili z analizo intergranularnih površin z metodo Auger-spektroskopije. Analizirane feritne površine smo obsevali z argonovimi ioni in posneli atomske absorbcijske spektre. Hitrost snemanja je bila 1 nm/min.

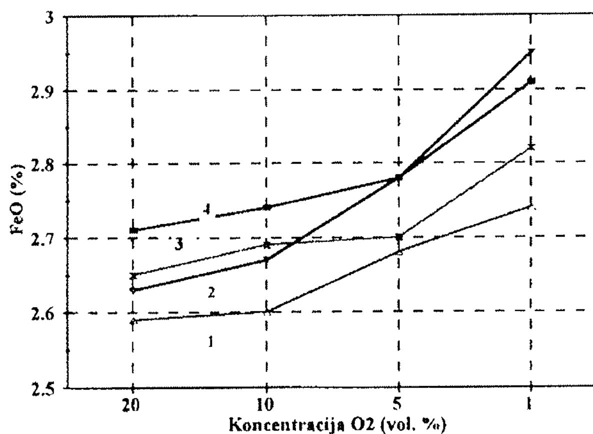
Močnostne izgube sintranih toroidov smo izmerili z inštrumentom Clarke & Hess 258 W pri frekvencah 200, 300, 400, 500 in 700 kHz (B = 50 mT) in T = 80 °C.

3. Rezultati in diskusija

Kombinacija dodatkov CaO in reduktivne atmosfere zmanjšuje končno velikost zrn feritnega izdelka (sl.1), ob enem pa z reduktivnimi pogoji sintranja vplivamo na končno koncentracijo FeO.



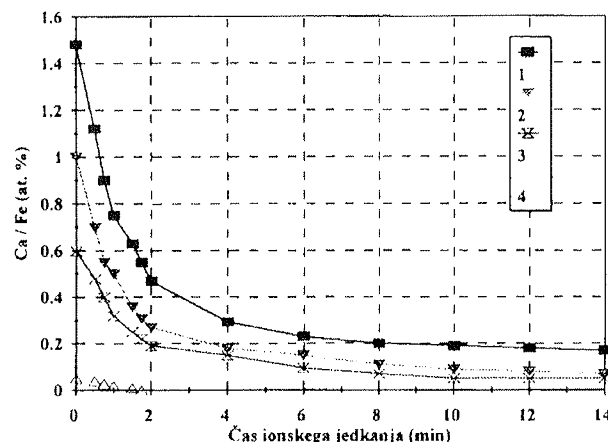
Sl. 1 Velikost zrn vzorcev 1, 2, 3 in 4 v odvisnosti od atm. pogojev sintranja



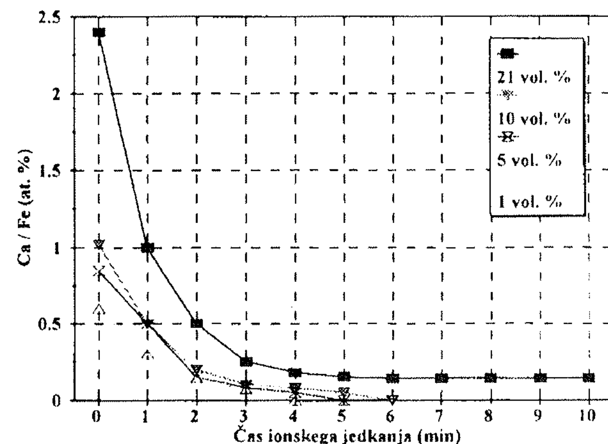
Sl. 2 Koncentracija FeO vzorcev 1, 2, 3 in 4 v odvisnosti od atm. pogojev sintranja

Kemijska sestava mej med zrni v odvisnosti od vsebnosti CaO in atmosferskih pogojev sintranja je bila določena s pomočjo AES. Sl. 3a prikazuje tipični koncentracijski gradient po globini vzorcev ferita 1, 2, 3 in 4, sintranih v atmosferi z 21% O_2. AES intragranularno lomljenih površin kaže, da se pri večjih vsebnostih CaO vgrajuje več dopanta na meje med zrni. Sl. 3b prikazuje globinski gradient koncentracij CaO na mejah med zrni vzorca 1, v odvisnosti od atmosferskih pogojev sintranja.

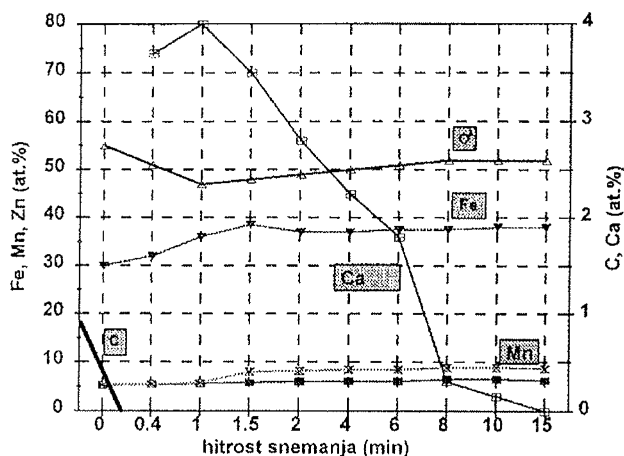
CaO se nalaga na mejah med zrni, kjer manjša mobilnost mej in vpliva na končno velikost zrn. Mehanizem vpliva dodatkov CaO lahko razložimo kot efekt difuzije topljenca (9). Nečistoče, ki se nalagajo na mejah med zrni, zavirajo premike mej in s tem rast zrn. Velikost in naboj dopanta določata energetsko področje na mejah med zrni, kjer se bo dopant vgrajeval. Med potekom rasti zrn ioni dopanta difundirajo sočasno s premiki mej med zrni. Hitrost premikanja je obratnosorazmerna širini področja, kjer dopant reagira z mejo med zrni. V našem primeru lahko obravnavamo koncentracijski gradient CaO, ki se nahaja po širini δ kot področje kjer dopant reagira z mejo. Hitrost premikov meje med zrni je sorazmerna $1/\delta$. Pri večjih koncentracijah in prodiranju CaO v globino MnZn ferita (sl.3a) bo difuzija topljenca povečana, rezultat pa je manjša povprečna velikost zrn (sl.1).



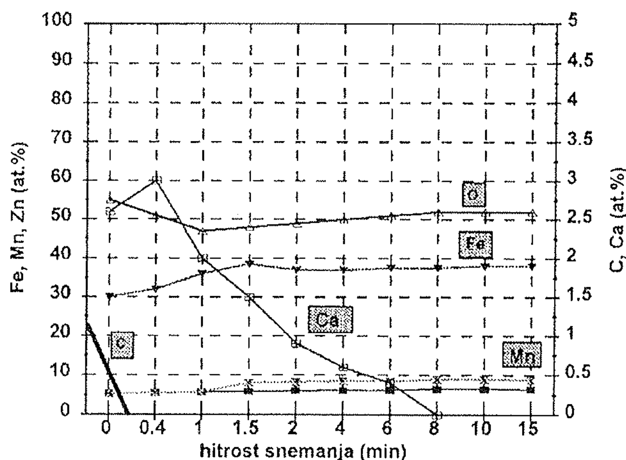
Sl. 3a Koncetr. gradient CaO v vzorcih 1, 2, 3, in 4



Sl. 3b Koncentr. gradient CaO v vzorcu 1 v odvisnosti od atm. pogojev sintranja



Sl. 3c AES koncentracijski gradient vzorca 1, sintranega pri koncentraciji 10 vol.% O_2



Sl. 3d AES koncentracijski gradient vzorca 1, sintranega pri koncentraciji 1 vol.% O_2

Po drugi strani pa reduktivna atmosfera poveča vsebnost FeO kar ima za posledico izrivanje Ca^{2+} iona iz meje in s tem bistveno manjši globinski koncentracijski gradient (sl. 3b, 3c, 3d). Vsled temu je bilo moč pričakovati prekomerno rast zrn, izkazalo pa se je, da prihaja do zaviranja rasti zrn, ki je posledica prodiranje por skozi meje med zrni (sl.1).

Če primerjamo upornost mej med zrni in ustrezni globinski koncentracijski gradient Ca^{2+} (sl. 3b), opazimo korelacijo med globino koncentracijskega gradienta Ca^{2+} na mejah med zrni (δ) in upornostjo meje (Rm.). Po drugi strani pa je upornost vzorcev sintranih v različnih parcialnih tlakih O_2 znotraj zrn konstantna kljub temu, da koncentracija Fe^{2+}narašča (sl. 2). Vzrok je v prisotnosti Ti^{4+} in Sn^{4+} ionov v kristalni mreži, ki tvorijo stabilne pare Fe^{2+} - Ti^{4+} (Sn^{4+}), ki preprečujejo preskok elektronov in s tem padec električne upornosti ferita (8).

V vzorcih z najvišjo vsebnostjo FeO so močnostne izgube najvišje, kljub dejstvu, da je tu povprečna velikost zrn najmanjša. Iz AES koncentracijskih gradientov se vidi, da imajo vzorci z največ Fe^{2+} najožje notranje meje med zrni tj. ozek koncentracijski gradient (sl. 3d). Po drugi strani pa visoke vsebnosti Fe^{2+} ionov v notranjosti feritnih zrn kot tudi na mejah med njimi povečajo število prebitnih elektronov, ki z relativno majhnim dodatkom energije preskočijo na drug mrežni položaj in posledično povečajo prevodnost feritov. Iz rezultatov torej lahko vidimo, da je v vzorcih z visoko vsebnostjo Fe^{2+} ionov debelina mej med zrni ključnega pomena za velikost visokofrekvenčnih vrtinčnih izgub. Pri načrtovanju in razvoju visokofrekvenčnih parametrov MnZn feritov so torej ključnega pomena mikrostrukturni parametri in lastnosti mej med zrni, ker bistveno vplivajo na končne elektromagnetne in uporabne lastnosti močnostnih MnZn feritov za visoka frekvenčna področja. Da bi izboljšali magnetne lastnosti močnostnih MnZn feritov z nizkim povprečnim premerom zrn in visoko vsebnostjo FeO, smo že izvedli prve preliminarne študije vpliva dodatne termične obdelave sintranih vzorcev pri temperaturnih (1100 °C) in atmosferskih pogojih (0.7 vol% kisika) oz. pri spremenjenih atmosferskih in temperaturnih pogojih sintranja z vpeljavo homogenizacije v fazi ohlajanja pri ravnotežnih pogojih, kjer poteče reoksidacija mej med zrni in segregacija večvalentnih ionov. Proces poteče brez mikrostrukturnih sprememb zaradi nizke temperature sintranja. Prvi rezultati dodatne termične obdelave pri spremenjenih atmosferskih in temperaturnih pogojih kažejo znižanje močnostnih izgub pri vzorcih dopiranih s CaO v povprečju za 20 do 30 %.

Koliko dodatna termična obdelava sintranih vzorcev dopiranih z CaO oz. spremenjeni atmosferski in temperaturni pogoji v fazi sintranja (z uvedbo faze homo-

Tabela 1: Upornost mej med zrni ($R_{m.z.}$) in upornost zrn (R_z) vzorcev 1, 2, 3 in 4

Vzorec	1		2		3		4	
vol. % O_2	R_z [Ω]	$R_{m.z.}$ [Ω]	R_z [Ω]	$R_{m.z.}$ [Ω]	R_z [Ω]	$R_{m.z.}$ [Ω]	R_z [Ω]	$R_{m.z.}$ [Ω]
21	10	2800	10	2250	7	100	8	15
10	10	2500	10	2000	9	90	9	17
5	10	2100	10	1900	9	72	8	19
1	10	2100	10	1700	9	60	12	17

Tabela 2: Močnostne izgube (P - celotne, P_H - histerezne; P_E - vrtinčne) Mn-Zn feritnih vzorcev 1, 2, 3 in 4 v (mW/cm^3) merjene pri T = 80 °C, B = 50 mT in f = 700 kHz, sintranih pri 21, 10, 5 in 1 vol. % kisika

Vzorec	1			2			3			4		
vol. % O_2	P_H	P_E	P	P_H	P_E	P	P_H	P_E	P	P_H	P_E	P
21	28	462	490	25	490	515	25	585	610	46	857	903
10	17	306	323	17	323	340	19	347	366	37	681	718
5	13	251	264	14	264	278	23	426	449	40	759	799
1	17	301	318	17	318	335	36	661	697	55	1024	1079

genizacije pri ravnotežnih pogojih) dejansko znižajo celokupne izgube pa je tema obstoječih raziskav pri študiju in razvoju nove generacije močnostnih MnZn feritov za frekvenčna področja f > 1 MHz.

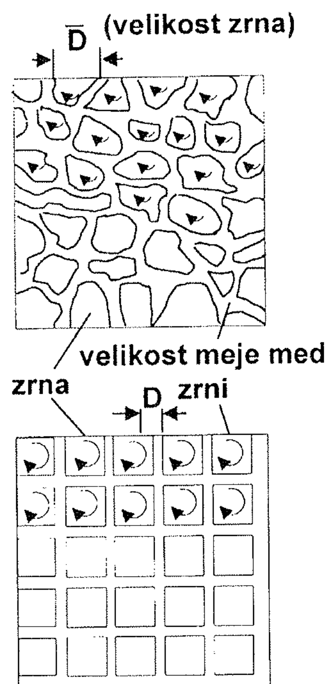
Z višanjem frekvenčnega območja uporabe MnZn feritnih materialov postaja delež vrtinčnih izgub vse večji in začne postopoma prevladovati nad histereznimi izgubami, katerih delež se drastično zmanjša. Pri obravnavanju vrtinčnih izgub je potrebno upoštevati dva ključna modela:

– v prvem modelu so magnetna zrna med seboj izolirana, vrtinčni tokovi pa se pojavljajo le znotraj zrn (slika 4). Vsako zrno prispeva k celokupnim vrtinčnim izgubam. V mejnem primeru, ko so meje med zrni dovolj debele in se bistveno zniža njihova električna kapacitivnost oz. postane frekvenčna odvisnost impedance zanemarljiva, lahko opišemo mikrostrukturni model ferita z ekvivalentnim vezjem, kjer prevladuje čista omska upornost. V tem primeru se da pokazati (10), da so močnostne izgube sorazmerne s kvadratom povprečne velikosti zrn:

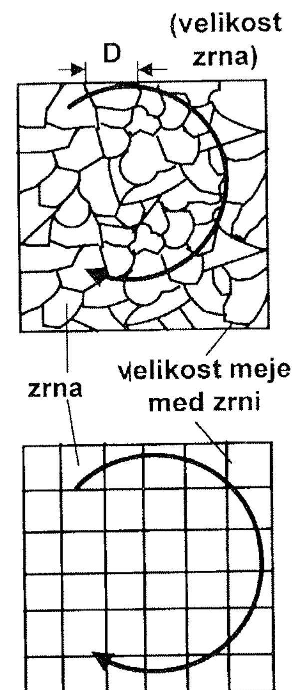
$$P_E = \frac{c\overline{D^2}}{\rho} B_m^2 f^2$$

B_m je maksimalna gostota magnetnega pretoka, f je frekvenca, ρ je električna upornost, $\overline{D}$ povprečna velikost zrn in c koeficient vrtinčnih izgub

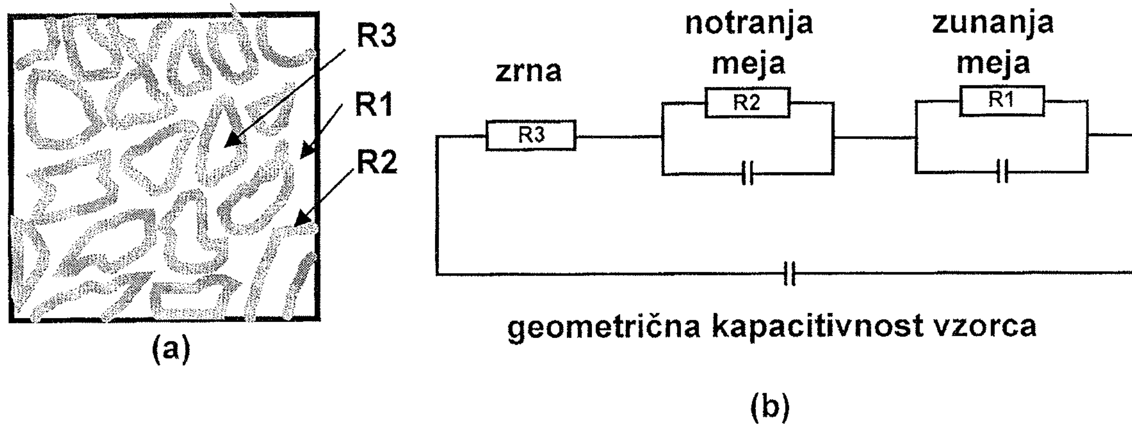
– v drugem primeru so meje med zrni prepustne za vrtinčne tokove (slika 5) in se po kemijski sestavi razlikujejo od notranjosti zrn. Za takšen material, ki ga sestavljajo polprevodna zrna in visoko omsko uporne meje je nadomestno električno vezje sestavljeno iz vzporedno vezane uporovne in kapacitivne komponente.



Slika 4: Shema dejanske in idealne strukture materiala z izoliranimi magnetnimi zrni



Slika 5: Shema dejanske in idealne mikrostrukture materiala z mejami med zrni, prevodnimi za vrtinčne tokove



Slika 6: Shematski model mikrostrukture, ki ustreza nadomestnemu električnemu vezju, sestavljenem iz vzporedno vezane uporovne in kapacitivne komponente
a) Shema polikristaličnega MnZn ferita (R_1 - upornost neferomagnetne meje med zrni, R_2 - upornost ferimagnetne notranje meje zrna in R_3 - feromagnetnih prevodnih zrn)
b) Shema nadomestnega vezja

Impedanca vzporednih R_iC_i elementov, ki običajno predstavljajo nadomestno vezje MnZn feritne keramike, je $Z = Z' - jZ''$, kjer je

$$Z' = \sum R_i / \left[1 + (\omega R_i C_i)^2\right]$$

in

$$Z'' = \sum R_i \left[\omega R_i C_i / (1 + \omega R_i C_i)^2\right]$$

Impedanca

$$Z = \sqrt{Z'^2 + Z''^2} \quad \text{za } \omega RC << 1,$$

kjer je $\omega = 2\pi f$, bo približno enaka omski upornosti $Z \rightarrow R$. V primerih $\omega RC >> 1$ in posledično $Z \rightarrow 1/\omega C$ je kapacitivnost mej med zrni zelo pomembna v MnZn feritih.

Z namenom, da razložimo odvisnost močnostnih izgub od povprečne velikosti zrn, smo uporabili za MnZn ferit modelno mikrostrukturo imenovano "Brick Wall Model" (BWM). Model sestavljajo kocke MnZn ferita, ki so izolirane z neprevodnimi plastmi debeline δ_{meje}. Te plasti so usmerjene pravokotno in vzporedno na glavno os, ki je hkrati tudi smer električnega polja. Meje med zrni, ki so vzporedno z glavno osjo, električno niso aktivne. Po drugi strani pa meje med zrni, ki so pravokotne na smer električnega polja, predstavljajo visoko omske uporovne plasti, pravokotne na glavno os.

Kadar je upornost materiala mnogo manjša od upornosti mej med zrni, lahko vsako plast predstavimo z nadomestnim vezjem, ki ga tvorijo vzporedno vezani omska in kapacitivna upornost R - C parov.

Z uporabo tega modela lahko makroskopsko upornost, ki jo lahko določimo iz impedančnega spektra, izrazimo kot

$$R^{mak}_{meje} = R^{mik}_{meje} L / (D + \delta_{meje})$$

kjer je $L/(D+\delta_{meje}) \cong L/D$ število mej med zrni v vzorcu, ki so pravokotne na električno polje. δ_{meje} je debelina meje med zrni.

$R^{mak}_{meje} = \rho^{mik}_{meje} L / A$ je makroskopska upornost, dobljena iz diagramov kompleksne impedance, L/A pa je razmerje med dolžino in površino vzorca.

Pri nizkih frekvencah, kjer velja za $\omega RC << 1$, lahko pokažemo, da so vrtinčne izgube sorazmerne s povprečno velikostjo zrn in obratno sorazmerne z upornostjo mej med zrni R^{mik}_{meje}. Po drugi strani pa pri visokih frekvencah ($\omega RC >> 1$ in $Z \rightarrow 1/\omega C$), če spet uporabimo model "opečnaste stene" (BWM), kjer je vsak presek meje med zrni pravokoten na električno polje, velja zveza $C^{mik.} = \varepsilon_0 \varepsilon_{meje}(A/\delta_{meje})$. Pri tem pomeni C^{mik} kapacitivnost posamezne meje. Če predpostavimo, da je število mej med zrni $\cong L/D$, dobimo izraz $1/C^{mak.} = (L/D)\ 1/C^{mik.}$, kjer je $C^{mak.} = \varepsilon_0 \varepsilon_{meje}(D/\delta_{meje})A/L$ enaka kapacitivnosti celega vzorca, ki jo lahko izmerimo. Ko vstavimo izraz za impedanco v splošno enačbo za vrtinčne izgube, dobimo sledečo zvezo:

$$P_E \cong cAB_m^2 f^2 \omega C^{mak.} \propto \varepsilon_{meje} D / \delta_{meja}$$

Iz vsega navedenega lahko sklepamo, da pri pogoju $\omega RC >> 1$ določajo vrtinčne izgube povprečna velikost zrn, debelina mej med zrni in njihova dielektrična propustnost. Najpomembnejša ugotovitev pa je dejstvo, da je povprečna velikost zrn dominantni mikrostrukturni parameter v celotnem področju frekvenc, ki določa vrtinčne izgube (10).

Zaključki:

- večanje vsebnosti CaO in zniževanje parcialnega tlaka bistveno vplivata na razvoj mikrostrukture MnZn ferita
- nizek parcialni tlak kisika veča vsebnost FeO, tanjša meje med zrni, krajša globinski koncentracijski profil Ca^{2+} in povzroča padec upornosti mej med zrni.

- močnostne izgube Mn-Zn feritov se z dodatkom CaO znižujejo, obenem pa se poveča upornost in širina frekvenčnega področja uporabnostni feritnega materiala.
- povprečna velikost zrn, debelina mej med zrni in dielektrična prepustnost so dominantni parametri vrtinčnih izgub
- razvita je nova kvaliteta visokofrekvenčnega močnostnega Mn-Zn ferita, ki je prenešena v redni proizvodni proces in se že uspešno trži na zahtevnem svetovnem tržišču..

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POROČILA S KONFERENC
CONFERENCE REPORTS

5th European Conference on Multi-Chip Module EC-MCM´99

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V dneh od 1. do 2. februarja 1999 je bila v Londonu konferenca z naslovom "5th European Conference on Multi-Chip Module" EC-MCM´99. Organizirala jo je, kot vsa leta doslej, angleška sekcija IMAPS (International Microelectronics and Packaging Society). Ob konferenci je bila tudi razstava proizvajalcev opreme in materialov za hibridno mikroelektroniko. V okviru konference je bila tudi sekcija oziroma delavnica z naslovom "GOOD-DIE for GOOD MCM". Pripomba; v tekstu bo za Multi Chip Module večinoma uporabljana okrajšava MCM.

Poleg konference smo imeli še projektni sestanek projekta "Cheap Multi-Chip Module" iz sklopa INCO/Copernicus. V poročilu je na kratko opisana vsebina nekaterih zanimivejših predavanj, na razpolago pa je zbornik referatov na Odseku za keramiko na Institutu Jožef Stefan.

Konferenca EC- MCM´99se je odvijala v okviru sledečih sekcij:

- MCM aplikacije
- MCM tehnologije in načrtovanje
- Povezovanje
- Zanesljivo dobre tabletke za dobre Multi-Chip Module (GOOD-DIE for GOOD MCM)

Poleg tega so uvedli še zanimivo novost; razstavljalci opreme in materialov so pred začetkom sekcije vsak v nekaj minutah na kratko predstavili, kaj razstavljajo.

Najprej ponovimo nekaj definicij. Multi Chip Moduli (MCM) so komponente, podsistemi ali sistemi z zelo visokim številom funkcij. Narejeni so na večplastnih substratih, na katerih so pritrjene ali gole polprevodne tabletke ali pa tabletke v Chip Sized Package (CSP), ki so samo okrog 20% večje kot gole tabletke. V večplastnem substratu in na njegovi površini so prevodne linije. Vezje je navadno hermetično zaprto. V glavnem ločijo tri tipe MCM, ki so izdelani v različnih tehnologijah, to je tankoplastni, debeloplastni (keramika) in v tehnologiji tiskanih vezij. Oznake so MCM-L (laminate - tiskana vezja), MCM-C (keramika) in MCM-D (deposited - tanki filmi). Tu omenimo, da so se leta na konferencah prijateljsko "prepirali" o tem, kako definirati, kaj je MCM in kaj ni. Sedaj kaže, da je prevladala nekakšna minimalistična definicija. Multi Chip Modul mora biti vsaj dvoplasten in imeti vsaj dve goli silicijevi tabletki, ali tabletki v CSP.

MCM-L so zahtevna večplastna tiskana vezja z linijami čim manjše širine. Ta tip MCM je najcenejši. Prevodnik je baker, dielektrik pa polimer. Glaven problem pri MCM-L je neujemanje temperaturnih razteznostnih koeficientov med silicijevimi tabletkami in organskim substratom. MCM-C so "keramični" hibridi visoke gostote, navadno večplastni keramični substrati ali pa kompleksna debeloplastna večplastna vezja. Debeloplastne izvedbe so ali "običajna" večplastna vezja ali pa vezja, narejena z novimi materiali, ki omogočajo večjo gostoto vezij, kot na primer difuzijsko oblikovanje ali foto postopki. MCM-D imajo nanešene tankoplastne večplastne kovinske povezave, ločene predvsem s polimernim ali včasih napršenim tankoplastnim dielektrikom. Kot substrat za MCM se običajno uporablja Al_2O_3 ali silicij. V primeru silicija se del elektronike izdela lahko že na substratu.

Razlogi za uvajanje MCM so predvsem miniaturizacija sistemov, boljše in hitrejše delovanje in zniževanje teže in porabe energije. Velikokrat je boljša in predvsem hitrejša rešitev MCM, "sestavljen" iz že obstoječih integriranih vezij (IC), kot razvoj novega ASIC-a (Application Specific Integrated Circuit) za isto funkcijo.

Referat z naslovom »Use of MCM technology to produce a bendpassing pipeline inspection vehicle« (N. Rice, British Gass Technology) je obravnaval konkretno uporabo MCM tehnologije pri izdelavi naprave za preverjanje kvaliteto oz. poškodovanosti cevi mestnega plinovoda. Pri omenjeni aplikaciji je MCM tehnologija omogočila miniaturizacijo elektronskega in senzorskega vezja, tako da se naprava lahko giblje po zavitih ceveh plinovoda. Predavanje je začel z dramatično sliko hiše, ki jo je porušila eksplozija plina, ki je uhajal pod njo. Referat »MCM packaging for sensors, actuators and microsystems« (J. M. Wilkinson, Techno-logy for Industry LTD, Anglija) je bil pregleden referat o MCM tehnologiji na področju senzorjev, aktuatorjev in mikrosistemov. Predavatelj je omenil sledeče:

Na področju avtomobilske elektronike so proizvajalci SensNor (N), VTI Hamlin (FIN), Bosch (D), Temic (D) in Sagem (F). Izdelki so predvsem senzorji pospeška (delajo jih vsi našteti), senzorji pretoka zraka in senzor pomika. MCM tehnologijo na osnovi debeloplastne tehnologije na keramičnem substratu imata firmi Bosch in Temic.

Na področju pisarniške opreme so proizvajalci Xaar (UK), Olivetti (I) in OCEA (D). Izdelki so namenjeni za

tiskalnike. MCM tehnologijo na osnovi debeloplastne tehnologije na keramičnem substratu ima le firma OCEA, ki izdeluje "glave" za termične tiskalnike.

Na področju medicinske elektronike so proizvajalci Dyconex (UK) - slušni aparat (fleksibilni PCB), Fadi (S) - katetrski senzor, FhG-IBMT (D) - katetrski senzor tlaka (silicijev senzor bondiran z žičko na fleksibilni PCB), Philips (D) - implant (MCM na keramiki), in IMT (CH) - analizator krvi (COB).

Na področju "pametnih" kartic in varovalnih naprav so proizvajalci Gemplus (F) - "pametne" kartice (TAB na plastiki), Siemens(D) - senzor prstnega odtisa (TAB na plastiki), SGS Thomson (F) - senzor prstnega odtisa (COB) in VLS Vision (UK) - cenena kamera (LCC na keramiki).

Prispevek »Low cost high density multilayer circuits for MCM-C« (I. Born in sodelavci, C-MAC Electromag, Belgija) je prikazal tehnološko in cenovno primerjavo cenenih MCM v tehnologiji difuzijskega oblikovanja (Diffusion Patterning) za izdelavo odprtin (vias) v dielektriku in optičnega oblikovanja (Fodel) za izdelavo 50 μm širokih prevodnih linij napram klasični debeloplastni tehnologiji in LTCC (low temperature cofired ceramics) tehnologiji. Omenjeni tehnologiji sta primerni pri manjšem številu prevodnih plasti (do 4) in zahtevani večji gostoti, ki jo klasična debeloplastna tehnologija ne omogoča.

Referat "MCM technology enables the world smallest GSP receiver" (C. Habinger, U-Blox AG, Švica) je predstavil razvoj in izdelavo najmanjšega GPS spre-jemnika na svetu v MCM tehnologiji. Majhna švicarska firma μ-Blox v sklopu EUROPRACTICE deluje na področju razvoja MCM-L na tiskanih vezjih. Startali so s sistemskim, elektronskim in tehnološkim znanjem, kar je zelo skrajšalo čas, potreben za razvoj. Njihov del projekta je trajal 6 tednov, celoten projekt pa 12 tednov. Predavatelj je posebej poudaril pomembnost dobavitelja komponent in dobro dolgoročno sode-lovanje s proizvajalcem.

V sekciji "MCM tehnologije in načrtovanje" so bili predstavljeni referati partnerjev INCO-COPERNICUS projekta. Najprej bomo podali nekaj osnovnih podatkov o projektu; projekt INCO-COPERNICUS z naslovom **"Establishment of Fast Prototyping Low Cost Multichip Module Technology Facilities in Eastern Europe for the Benefit of European Industry"** oziroma s "kratico" **Cheap Multi Chip Modules** traja tri leta, od 1. maja 1997 do 30. aprila 2000. Administrativni koordinator projekta je prof. dr. Zsolt Illyefalvi-Vitez iz Tehnične Univerze v Budimpešti, Madžarska. V okviru projekta sodeluje devet partnerjev. Partnerji so razisko-valni inštituti in majhna oziroma srednje velika podjetja Madžarske, Romunije, Slovenije, Velike Britanije in Belgije. Slovenska partnerja pri projektu sta Institut Jožef Stefan, Ljubljana in HIPOT HYB., Šentjernej. Cilj projekta je doseči možnost razmeroma poceni projek-tiranja, izdelave in testiranja predvsem prototipov Multi Chip Modulov (MCM). Naloge projekta so razdeljene med partnerje glede na njihovo tehnološko usposobljenost. Design je naloga romunskih partnerjev. Ti so instalirali CAD sistem in bodo s pomočjo testnih vezij in simulacij določili pravila načrtovanja. Izdelava prototipov je naloga madžarskih in slovenskih partnerjev. Madžarski partnerji se bodo koncentrirali na MCM-L (tehnologija tiskanih vezij), slovenski pa na MCM-C (keramični MCM, v tem primeru večplastna debeloplastna vezja). Madžarski partner bo hkrati z angleškim in belgijskim odgovoren tudi za bondiranje golih silicijevih tabletk in sestavljanje oziroma montažo prototipov MCM. Končno testiranje demonstracijskih vezij je naloga belgijskega partnerja. Evaluacija rezultatov je naloga vseh partnerjev pod vodstvom madžarskega partnerja, ki je tudi koordinator projekta.

Pregledni referat v tej sekciji z naslovom »The European INCO-COPERNICUS project« (Z. Illyefalvi-Vitez, koordinator projekta, Madžarska, in sodelavci) je predstavil planirano in izvedeno delo na projektu "Cheap Multi-Chip Module" iz sklopa INCO/Copernicus. Podrobno so razdelane naloge in dosežki partnejev projekta in podana tista bibligrafija sodelavcev, ki se nanaša na projekt. Referat »Simulation of multichip module structures« (P. Svasta in sodelavci, Univerza v Bukarešti, Romunija) je bil posvečen elektronskim simulacijam (frekvenčnim odvisnostim in tokovne gostote) posameznim strukturam, ki se uporabljajo v MCM. Simulirali in analizirali so »obnašanje« štirih tipičnih elementov MCM struktur, in sicer prehod skozi dielektrik (via), 200 μm širiko prevodno linijo in simetričen ter nesimetričen bond z zlato žičko. Elektromagnetna simulacija je bila narejena za širok spekter frekvenc od 1 MHz do 1 GHz. Z. Illyefalvi-Vitez (Tehnična univerza v Budimpešti, Madžarska) je govoril o uporabi YAG laserja pri izdelavi kompliciranih prototipov MCM v tehnologiji tiskanih vezij, to je predvsem oblikovanje in izdelavo tiskanin s kombinirano metodo laserskega odstranjevanja bakrene plasti in kemičnega jedkanja bakrene plasti. V obsežnem in zanimivem uvodu je najprej predstavil osnove laserja in možna področja uporabe pri tehnologijah za elek-troniko. Laser se lahko uporablja tako za vrtanje lukenj (vias) v ploščah tiskanih vezij kot za direktno »risanje« prevodnih linij na vezju.

V tej sekciji je bil tudi naš referat z naslovom »Thick film materials for diffusion patterning technology« (avtorji D. Belavič in M. Pavlin, HIPOT, Šentjernej in M. Hrovat, Institut Jožef Stefan, Ljubljana). Predstavili smo materiale (izolacijske-dielektrik, prevodne, in uporovne) za izdelavo MCM s tehnologijo difuzijskega oblikovanja. Difuzijsko oblikovanje je način izdelave večplastnih debeloplastnih vezij, ki omogoča doseganje večje gostote vezij z obstoječo tehnologijo sitotiska in žganja. Večplastno vezje, narejeno s to tehnologijo, je pri isti kompleksnosti 20% do 40% manjše od "navadnega" debeloplastnega večplastnega vezja. Načrtali smo testna vezja, s katerimi smo meje oziroma tolerance izdelave ozkih prevodnih linij in odprtin v dielektriku večplastnih vezij. Predstavili smo tudi preliminarne rezultate preiskav karakteristik debeloplastnih uporov, žganih v dielektrični strukturi, kar bi lahko še povečalo gostoto večplastnih vezij.

Referat »Mixed component integration in advanced printed wiring boards« (S. O´Reilly in koavtorji, PEI Technologies, Irska, Alcatel Bell in OMRC-INTEC, Belgija ter Kam Circuits, Anglija) je predstavil integriranje pasivnih komponent v MCM-L. Integrirane upore izdelajo s pomočjo komercialno dobavljivih uporovnih folij OHMEGA-PLY. Folije imajo plastno upornost od 25 do 500 (1000) Ohm/kv. Upore oblikujejo z jedkanjem folije.

Kondenzatorje in induktivne komponente izdelu-jejo z jedkanjem bakrene folije. Delo je del Brite EuRam projekta z imenom COMPRISE.

Zanimiv referat z razmeroma dolgim naslovom, ki že sam pove skoraj vse, je bil »The development of a novel, low stress, non-pocorning, glob-top and encapsulant«. Avtoji so bili iz Multicore Solders Ltd. (Anglija), ki je razvijal ta nov polimerni encapsulat za vezja oziroma komponente na vezjih ter iz DERA (prav tako Anglija), ki so materiale testirali na velikih keramičnih hibridnih vezjih. Zahteve oziroma želje, katerim karakteristikam naj bi organske zaščite ustrezale, so jasne, čeprav se nekatere med sabo izključujejo. Poleg običajnih karakteristik, to so na primer nizka dielektričnist, dobra adhezija in temperaturni razteznostni koeficienti, ki se ujemajo z vezjem in komponentami, sta si predvsem dve nasprotni; zaščita naj bi bila »trda«, da dobro ščiti pred zunanjimi vplivi in »mehka«, da ne povzroča mehanskih stresov. »Trde« zaščite so epoksiji, ki imajo temperaturo prehoda T_g (glass transition temperature) okrog 150°C, mehke pa silikoni s T_g okrog -50°C. Razvili so nov dvokomponentni organski enkapsulant na osnovi poliuretana, ki je dovolj prožen, da ne vnaša stresov in hkrati dovolj trd, da dobro ščiti tako komponente, recimo bondirane tabletke, kot cela vezja. Polimerizira pri 100°C, kar je dovolj nizka temperatura. T_g je pri -50°C, razteznostni koeficient pa je 100×10^{-6}/K. Obsežna testiranja so pokazala, da je material primeren tako za zaščito komponent kot tiskanih vezij. Cilj je uporaba v avtomobilski industriji, kjer mora elektronika delati pod zelo zahtevnimi pogoji.

Referat o evropskem projektu Europractice MCM (R. Doyle, NMRC, Irska) je prikazal dogajanje na evropskem trgu MCM in funkcijo organizacije Europractice pri povezovanju ponudbe in povpraševanja. Cilj projekta je, da bi preko tako imenovanih lokalnih centrov, lociranih po raznih krajih Evrope, povezoval proizvajalce MCM (uporabnike) s proizvajalci polprevodnih tabletk, materialov in opreme. Uporabniku naj bi pomagal pri izbiri primerne tehnologije in designa za zaželjene aplikacije. Uporabnik večkrat nima dovolj izkušenj, da bi izbiral med ponujenimi opcijami, zato mu Europractice MCM lahko pomaga pri odločitvi. Namen projekta torej ni razvoj tehnologij, ampak izbor in uporaba razpoložljivih tehnologij.

Delavnica z naslovom "GOOD-DIE for GOOD MCM" s štirimi temami je bila organizirana v sklopu evropskega ESPRIT projekta "GOOD-DIE".

Predstavitev projekta (Mike Roughton)

Evropski ESPRIT projekt "GOOD-DIE" je organiziran v sedmih delovnih paketih.

- v prvem proučujejo in uvajajo novosti, procedure in standarde (Philips),
- v drugem organizirajo in izvajajo delavnice ter izdajajo revijo in spletno stran (IMEC),
- v tretjem analizirajo trg in razvijajo CSP tehnologijo (Siemens),
- v četrtem se ukvarjajo s testiranjem (Alcatel Microelectronics),
- v petem pripravljajo pravila in postopke za rokovanje in dobavljanje tabletk, rezin in CSP (Eltek),
- v šestem organizirajo predavanja, tečaje in vadbe ter promovirajo in podpirajo uporabo standardov (CODUS),
- v sedmem pripravljajo in uvajajo načrtovalske postopke in orodja (Rood Technology).

Razvoj CSP tehnologije (John Myers)

Predavatelj je predstavil razvoj Chip Scale Package (CSP) tehnologije v smer μBGA (zaščitna znamka za miniaturne Ball Grid Array firme Tessera, Inc.). Klasična CSP tehnologija je konkurenčna "Flip čip" tehnologiji. Vendar μBGA izkorišča prednosti CSP in SMD tehnologij. Njihova μBGA ohišja so velika od 4 mm do 21 mm. Pri μBGA orjejo ledino na področju standardnih razmakov priključkov ("pitch"). Odločili so se za razmak 0,5 mm z mnogokratniki. Standardni razmak je tudi diagonala kvadrata s stranico 0,5 mm (ali mnogokratnik). Vezja v μBGA ohišjih so testirali pri povišani temperaturi (1000 ur na 150°C), na temperaturno cikliranje (1000 ciklov -50°C/+125°C oziroma 1000 ciklov -65°C/+150°C), temperaturne šoke (500 ciklov -65°C/+150°C), testiranje v vlagi in testiranje na povišani temperaturi in povišanem tlaku.

Cenena Flip Chip tehnologija (Joachim Kloester)

Predavatelj iz FhG-IZM, Berlin je predstavil razvoj cenenega flip-chip ohišja. Pri cenenih aplikacijah (mobilni sistemi, telekomunikacije, avtomatiziran trg, ...) je velik pritisk na znižanje cene in na vzdrževanje kvalitete. Njihov odgovor je ceneno flip-čip ohišje. Postopek izdelave cenenega flip-čipa je sledeč. Na bondirno blazinico (na tabletki) iz aluminija se nanese plast niklja in preko nje še tanka plast zlata. Oba nanosa skupaj sta debela od 3 μm do 5 μm. Na tako pripravljeno blazinico se natiska pastozno spajko, ki se jo pretali in na ta način formira kroglico. Pastozna spajka mora imeti delce spajke manjše od 45 μm. Oni uporabljajo pastozno spajko firme Heraeus 95/5 oz. 63/37 (Pb/Sn) z velikostjo delcev od 15 do 25 μm oz. od 5 do15 μm. Za uporabo flip-čipa uporabljajo standardno pretalje-valno tehnologijo kakor za SMD tehnologijo. Dodaten postopek je uporaba in polimerizacija polnila pod flip-čipom.

Testiranja rezin (Samuel Declercq)

Predavatelj je prikazal način in postopke funkcionalnega testiranja integriranih vezij na nivoju rezine. Testiranje izvajajo spiralno od sredine proti robu rezine in označujejo slaba vezja. Postopki so namenjeni zmanjševanju izmeta pri nadaljnji uporabi tabletk kot KGD s ciljem 0 ppm.

PREDSTAVLJAMO PODJETJE Z NASLOVNICE
REPRESENT OF THE COMPANY FROM FRONT PAGE

ISKRA FERITI d. o. o.

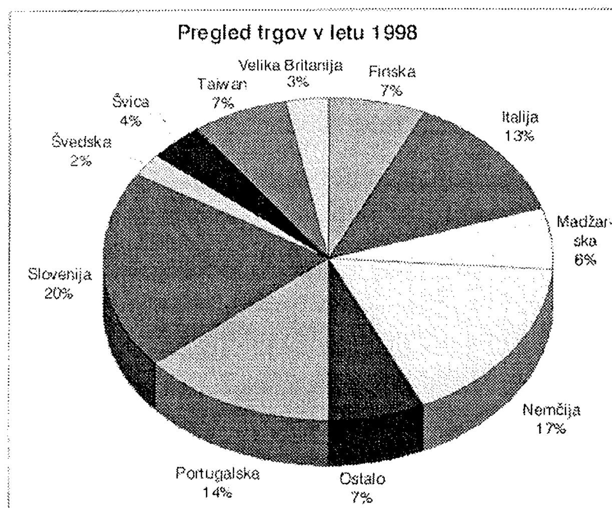
1. Uvod

Iskra Feriti, d. o. o. že več kot 40 let proizvaja feritne materiale in feritna jedra za celotni spekter elektronike. Proizvodnji program je bil zasnovan v letu 1954 v okviru Electronics Research Institute in Ljubljana. Proizvodnja feritnih materialov in izdelkov je stekla v letu 1957. Na sedanji lokaciji imamo proizvodnjo feritnih materialov in izdelkov od leta 1966. V letu 1973 pa smo na Ljubnem ob Savinji ustanovili podružnico Iskra Feriti za navite komponente. Na tej lokaciji je še vedno zaposlenih 120 ljudi, v Ljubljani pa okrog 288.

Manjši del proizvodnje navitih komponent vzdržujemo tudi v Ljubljani. Tu lahko izdelamo manjše serije navitih komponent in sestavljanje večjih količin RM6 transformatorjev za telekomunikacije. Za proizvodnjo RM6 transformatorjev imamo avtomatsko linijo, ki je ena najmodernejših v Evropi. Njena zmogljivost je 900 RM6 transformatorjev na uro. Linija sestavi, izmeri, žigosa in pakira omenjene transformatorje brez posluževalcev.

Razvoj, tehnologija in skupne službe so za oba programa v Ljubljani. Program je plod domačega znanja in ni licenčno obremenjen. Že vsa leta uspešno in tesno sodelujemo, na področju razvoja novih feritnih materialov z Inštitutom Jožef Stefan, Odsek za keramiko, ki ga sedaj vodi dr. Marija Kosec, dipl. ing. Na področju navitih komponent pa z Fakulteto za elktrotehniko, Laboratorijem za močnostno elektroniko, ki ga vodi prof. dr. Janez Nastran, dipl. ing. Rezultati uspešnega dela so tudi podeljene patentne listine, ki smo jih prejeli na obeh področjih dela.

Na slovenskem trgu prodamo okrog petino naših proizvodov, zlasti na področju telekomunikacij, avtomobilske industrije in široke potrošnje. Dobrih 80% proizvodnje pa prodamo na zahodnoevropskih trgih, od katerih ima Nemčija še vedno največji delež. Bolj podrobni podatki so razvidni iz frekvenčnega kolača, ki je na sliki 1. V zadnjih dveh letih prodiramo na Ameriški trg, kjer so velike priložnosti za kakovostna feritna jedra in navite komponente za telekomunikacije.



Slika 1. Pregled trgov v letu 1998

2. Naš program

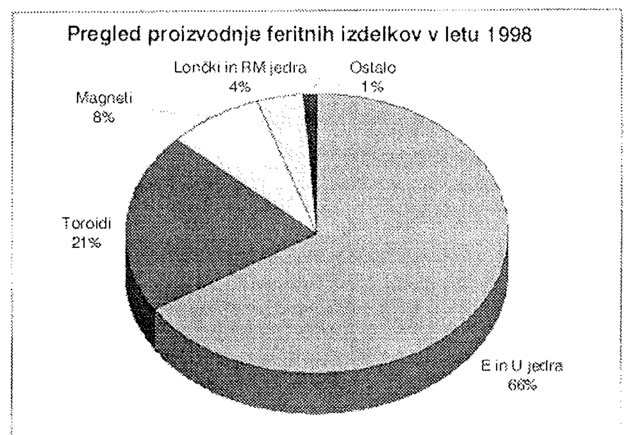
- Mehki feriti
- Trdi feriti
- Navite komponente

2.1. Mehki feriti

Vseh feritnih materialov proizvedemo okrog 800 ton. Od tega proizvedemo okrog 700 ton Mn-Zn feritov, 100 ton trdih feritov in okrog 50 ton Ni-Zn feritov. Za nas so najpomembnejši Mn-Zn feriti, ki so namenjeni za področje telekomunikacij, napajalnikov, filtrov, senzorjev in dušilk. Mehke feritne materiale delimo še na nizkoizgubne, močnostne in visokopermeabilne. Vsak od teh materialov je namenjen specifičnim aplikacijam v področju elektrotehnike.

Iz Mn-Zn materialov oblikujemo različne oblike feritnih jeder s suhim stiskanjem. Zahtevne oblike feritnih jeder pa tudi brizgamo s pomočjo posebnih vezivnih materialov. V obeh primerih je potreben vezivni material, ki ga je potrebno pred sintranjem izgnati oziroma izpareti. V drugem primeru je vezivnega materiala bistveno več kot v prvem.

Tipične oblike feritnih jeder, ki jih oblikujemo iz Mn-Zn materialov so: RM jedra, Toroidi, E jedra, U jedra, ETD, EFD, EI14-EI38, cevke in palčke ter ostalo. Naše nove oblike feritnih jeder so planarna jedra, ki jih imamo pet različnih vrst v kombinacijah EI in EE. Planarna jedra se



Slika 2. Pregled proizvodnje feritnih izdelkov v letu 1998

uporabljajo v modernih DC/DC konverterjih, zlasti za področje telekomunikacij.

Na sliki 2 so razvidni deleži posameznih oblik feritnih jeder, ki smo jih proizvedli v letu 1998.

2.2. Trdi feriti

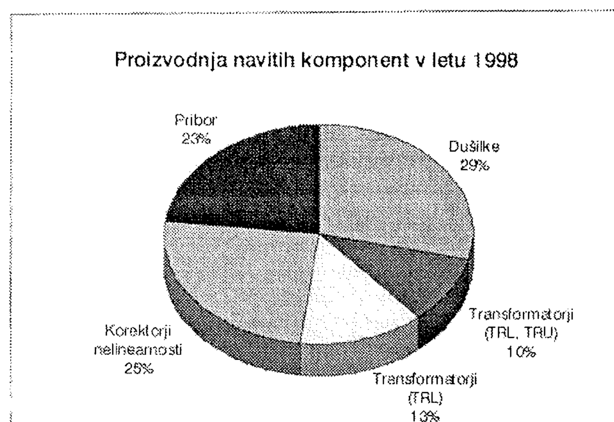
Sestavine trdih feritnih materialov so precej drugačne. Njihove elektromagnetne lastnosti so tipične lastnostim trajnim magnetom. Feritni magneti so lahko anizotropni in izotropni. Anizotropni imajo višje magnetne gostote in koercitivnosti hkrati. Oblikujejo se tako, da med procesom stiskanja s pomočjo zunanjega magnetnega polja vpliva na orientacijo notranjih magnetnih domen. Izotropni magneti se suho stiskajo. Brez zunanje orienatacije domen imajo nižjo magnetno gostoto in koercitivno poljsko jakost.

Odlikujejo jih večja ohmska upornost in manjše histerezne izgube napram kovinskim magnetom, zato jih lahko uporabljamo v aplikacijah do precej visokih frekvenc, kjer bi se kovinski magnet močno grel, zaradi vrtinčnih in histereznih izgub.

Izdelujemo jih v okroglih in ploščatih oblikah. Uporabljamo jih tudi v navitih komponentah pri korektorjih nelinearnosti. Pogosto jih srečamo v motorski in avtomobilski industriji ter v široki potrošnji.

2.3. Navite komponente

Na sliki 3 so razvidni deleži posameznih navitih komponent, ki smo jih proizvedli v letu 1998. Največ smo izdelali raznih dušilk na DTM in DAM jedrih, sledijo korektorji nelinearnosti in RM transformatorji za telekomunikacije.



Slika 3. Pregled proizvodnje navitih komponent v letu 1998

Specializirani smo za proizvodnjo RM transformatorjev za ISDN telefonijo, senzorjev za približevalna stikala, različne električne filtre in korektorje nelinearnosti. V letu 1998 smo proizvedli okrog 20 milijonov različnih navitih komponent. Naše navite komponente konstruiramo na osnovi domačega feritnega jedra. Naš cilj je povečati delež vgradnje lastnih feritov in jih tržiti skozi navito komponento.

3. Novi proizvodi

3.1. Planarni transformatorji

Izgled planarnega transformatorja je na naslovnici. Je nov proizvodni program in plod lastnega razvoja. Planarni transformatorji so izdelani iz zelo sploščenega mehko magnetnega feritnega jedra in večslojnega tiskanega vezja, ki predstavlja navitje. Večslojno tiskano vezje je stisnjeno in lepljeno pod velikim pritiskom in temperaturo. Vsi zračni mehurčki in vlaga so iztisnjeni. Mehanske dimenzije paketa so konstantne. Vsled tega imajo lastnosti v ozkih tolerančnih mejah. Odlikujejo jih nizka stresana induktivnost, visoka prebojna trdnost, majhen volumen, visok izkoristek in dolga življenska doba. Edina slaba stran je nekoliko višja cena, ki je povezana z drago tehnologijo izdelave večslojnega tiskanega vezja.

Ravno cena je bila odločilna, da so se planarni transformatorji pojavili najprej na področju telekomunikacij, kjer so predvsem napajalniki oziroma DC/DC konverterji v različnih topoloških vezavah: flyback, forward, halfbridge in fullbridge converters.

3.2. Korektorji nelinearnosti

S pomočjo teh komponent je možno izboljšati horizontalno nelinearnost slike pri TV sprejemnikih in monitorjih, ki uporabljajo CRT cevi, v širokem spektru horizontalnih frekvenc. Pri TV sprejemnikih delajo običajno na osnovni horizontalni frekvenci 15.625Hz. Pri računalniških monitorjih pa med 32,5kHz in 120kHz.

Za monitorske aplikacije smo razvili specialni korektor, ki pokrije navedene zahteve in samodejno prilagaja delovno točko horizontalne končne stopnje velikosti računalniške slikovne resolucije. Slika je v celotnem spektru nelinearna znotraj 5%.

Za področje TV sprejemnikov in monitorjev smo razvili korektor z minimalnimi sestavnimi deli. Trajni magnet smo nadomestili s plastomagnetom. Ta korektor odlikuje nižja cena.

3.3. Nov feritni material 75G

Za področje modernih močnostnih aplikacij razvijamo nov Mn-Zn material, ki bo uporaben do 1,5MHz. Uporaben bo predvsem za področje DC/DC konverterjev. Iz njega bomo izdelovali različne oblike feritnih jeder: RM, EI14-EI38, EFD in razna toroidna jedra.

3.4. Multilayer chip dušilke

Poleg klasičnih dušilk se vedno bolj uveljavljajo večslojne dušilke na osnovi večplastnega feritnega jedra. Osnova teh dušilk so nizkotemperaturni Ni-Zn materiali 5C do 9C, ki smo jih že razvili. Navitje je izvedeno s pomočjo srebro-paladijeve paste. Induktivnost je odvisna od števila plasti. Te dušilke odlikujejo zaprti magnetni krog in manjša občutljivost na elektromagnetne motnje. Proizvodnja bo mogoča s pomočjo druge slovenske firme, ki že ima tehnologijo večslojnega oblikovanja komponent.

Leopold Knez, dipl. ing.
ISKRA FERITI, d. o. o.
Stegne 29, 1521 Ljubljana

VESTI - NEWS

In this issue of Informacije MIDEM we are bringing to you some highlights from 1998 reports of three European institutions/companies:
- IMEC, Belgium
- National Microelectronics Research Centre, Ireland and
- Austria Mikro Systeme Intl. AG, Austria

Copies of full reports are available at the MIDEM headquarters.

IMEC

Introduction

I. Preface

Microelectronics continues to be one of the most rapidly evolving generic technologies. Future technology generations require enormous efforts in basic and long-term research related to new materials and interfaces between different materials, new lithography, interconnect and device concepts. It becomes an enormous challenge to further reduce dimensions, to master the new production processes and to bring them to high yield, and to reduce the waste in order to decrease costs and environmental effects.

The developments in microelectronics also lead to the rapidly expanding field of microsystems with interesting applications in medicine, pharmacology, automotive, space,... We see a need for new packaging techniques for chips with large pin-count and for circuits using the multi-chip module concept. The merge of the consumer, communication and computer worlds has created complete systems-on-a-chip requiring the development of new design methodologies.

The R&D underlying these developments is multidisciplinary and is a mixture between long- and short-term research. The cost increases substantially, with every new generation. It requires an excellent collaboration between industry, independent laboratories and academia. The interaction has to be built on a good intellectual property ruling.

IMEC stands out as an independent R&D laboratory. It is known for its broad coverage of microelectronic technologies, its balance between basic research and application-oriented research, its unique infrastructure and its well-developed IPR policy. IMEC is carrying out R&D with many companies all over the world, next to more than 60 companies in Flanders. Up till today,15 spin-off companies have been started up. The microelectronics industry in Flanders is gaining importance through the creation of DSP Valley through the efforts of IMEC in training, transfer of technology, creation of spin-offs, but also due to the many initiatives and incentives from the Flemish government.

This scientific report describes the results of our research in 1998. Our strategy is discussed in the introduction of the various research domains. It also gives the results of the research done at the Flemish universities in collaboration with IMEC. Next to this scientific report, IMEC also publishes a general annual report with a short description of our activities and with financial data. A copy of this annual report can be obtained on request.

II. History and organization

IMEC is an Interuniversity Microelectronics Center, setup in 1984 by the Flemish government in Belgium as part of a comprehensive program in the field of microelectronics.

The laboratory houses over 3,900 m^2 ultra clean processing area, 6,710 m^2 computer room and utilities,10,400 m^2 offices and supporting laboratory space and 810 m^2 cafeteria and training facilities. The R&D facilities include:

- a 200 mm pilot line for deep submicron CMOS processing
- a pilot line for multi-chip modules
- a microsystems laboratory
- research facilities for new materials and devices
- a pilot line for crystalline silicon solar cells
- a physico-chemical analysis laboratory
- a VLSI design methodology laboratory
- automatic device and circuit measurements
- packaging and testing equipment
- equipment for device reliability studies

In September 1998 construction started for the expansion of the clean room facilities. This will increase the capacities for clean room air exhaust and production of DI water. For the future, IMEC will have the possibilities to expand the clean room with an extra 1,200 m^2.

One of the important issues in a R&D environment is quality insurance. On February 12, 1998 the ISO9001 certificate was granted to IMEC by SGS. This certificate covers the total IMEC organization: training, design, research, development, integration and characterisation of processes, systems and software in the field of microelectronics and related technologies. The introduction ol the quality system was phazed over the different groups and resulted in a first certificate in 1994 for the pilot processing activities.

IMEC's annual budget is close to 3.0 billion BF (75 million EURO).

Associate Vice-Presidents are:
- R. De Keersmaecker, reporting to the President and in charge of key projects. In 1997 he was seconded to FFIO (Flander's Foreign Investment Office) in order to coordinate and manage investments in IC fabs in Flanders. In 1999, he will continue this assignment;

- P. Six, reporting to I. Bolsens are responsible for the design methodology transfer to external users.
- L. Deferm, reporting to H. Maes and responsible for CMOS integration;
- A. Hermans, reporting to R. Mertens and responsible for Microsystems;
- H. Lebon, Fab Manager and reporting to L. Van den hove.

Several staff members of IMEC have a part-time teaching appointment at one of the universities.

Professors at the K.U.Leuven (University of Leuven) are: S. Borghs, F. Catthoor, L. Claesen, C. Claeys, G. Declerck, R. De Keersmaecker, H. De Man (full-time), K. De Meyer, H.. Maes, K. Maex, R. Mertens, J. Nijs, W. Vandervorst, R. Van Overstraeten and M. Van Rossum.

Members of the Patent Review Board are:

- DESICS Division: I. Bolsens - H. De Man - M. Engels
- SPT / SDTI / MCP Divisions: L. Deferm - L. Hermans - M. Heyns - H. Maes - R. Mertens - J. Poortmans - M. Van Rossum - I. Van den hove
- BDU Divison: K. Meuwis - V. Ryckaert - R. Vanoppen - K. Wuyts

III. Interaction with educational research laboratories and institutions

It is IMEC's mission to contribute to the strengthening of the research potential of the Flemish universities in microelectronics and related fields. As one could expect, the closest collaboration has been established with the Electronics Department of the three Flemish universities offering a degree in electronic engineering: the K.U. Leuven (University of Leuven), RUG (University of Gent) and the VUB (Universitv of Brussel).

The following facilities are made available to these institutions:

- state-of-the-art software and hardware for the design of integrated circuits;
- prototyping of semi-custom and full-custom semiconductor devices, including sensors;
- equipment and personnel for complementary research at the laboratories.

IMEC also encourages university students to do research in preparation of their Master's or Ph.D. thesis. In 1998 they represented a group of more than 120 persons. The research includes signal processing, optoelectronics, MMICs, reliability, computer architectures, sensors, image processing, new semiconductor structures and devices,...

Through the INVOMEC division, state-of-the-art design software and hardware is also made available to the 13 Flemish higher polytechnical schools.

The R&D activities of the INTEC (department of Information Technology) laboratory of the RUG and those of the ETRO (Electronic and Digital Signal Processing) laboratory of the VUB are fully coordinated with IMEC's activities. INTEC's research eflorts are directed towards broadband communication, including optoelectronics and high-speed/high-frequency cir-cuits. ETRO's activities concentrate on hardware architectures for image compression, on optoelectronic and optical components and systems for communication. Full account of these R&D activities is given in part II of this report. The R&D activities of the microelectronics group of the Katholieke Hogeschool Brugge-Oostende and the related contract research are also fully coordinated with IMEC.

Other university research groups are included in a growing number of collaborative research programs. The most important projects are:

- with the LUC (Universitv of Limburg) on reliability of electronic material systems and electronic components; on precursor preparation for ferroelectric nonvolatile memory research, on LASIMS analysis;
- with the UIA (University of Antwerpen) on electrical transport in low-dimensional semiconductor structures, on ultra-fast switching and relaxation processes in III-V heterostructures and devices, on concentration-depth profiles of semiconductor structures, on organic semiconductors and light-emitting semiconductors; on TEM and TOF-SIMS analysis methods;
- with the Physics and Chemistry department of the K.U. Leuven (University of Leuven). Topics include high-Tc superconductors, atomic force microscopy (AFM), silicides, X-ray diffraction (XRD), Raman spectroscopy. The collaboration with the Electrical Engineering department focuses on mm-wave and microwave circuits and systems, on parallel VLSI architectures for non-linear diffusion for front-end vision, on DSP algorithms and architectures for digital communication systems, on design methods for microsystems, software environment for real-time emulation of complex DSP;
- with the RUG (University of Gent) on massive parallel information processing based on hybrid Si and III-V optoelectronic components;
- in 1998, a new phase of the Information Technology Action Program has been launched by the Flemish government. Within this framework IMEC performs research in close collaboration with all Flemish universities concerning:
  - design and control of broadband networks for multimedia applications;
  - integration, management and processing of images for high-end applications;
  - integrating signal processing systems;
- the second edition of the Teleclassing course on Telecommunications was started in September 1998. The course is a joint initiative of IMEC, the Flemish universites and industry. Lectures are broadcasted from the IMEC site to several university and industry locations. Over 500 students have already registered for this course.

In collaboration with the K.U. Leuven (University of Leuven), IMEC organizes graduate level courses on the physics and technology of microelectronics and related materials sciences. These courses are part of the curriculum of the Faculty of Engineering and/or the Faculty of Sciences.

The main topics are:

- solid-state physics (fundamentals, optical properties, metastable and amorphous materials, modulated structures);
- thermodynamics, kinetics and related topics in materials science;
- physics of advanced microdevices;
- fundamentals of defects in materials;
- physics of beam-solid interactions;
- materials characterization techniques;
- continuum modeling of material properties;
- basics of VLSI processing;
- design and analysis of experiments.

In the European Union, IMEC is also involved in a number of Networks of Excellence. These networks help in coordinating and focusing academic research in Europe.

Through the Large Scale Facility Program of the European Commission, IMEC provides access to its prototype silicon compiler software available, developed at IMEC, to several users, allowing them to make designs of advanced real-time digital signal processing chips. On the technology side, the EURACESS project, introduced jointly by LETI and IMEC, has been approved by the European Commission. This project will open major parts of the technological infrastructure of both institutes to interested research groups throughout the European Union.

Besides these actions supported by the European Commission, IMEC continues to collaborate with foreign research centers on large projects, beyond the scope of one single laboratory or on projects where the complementary, nature of the laboratories can lead to synergetic effects.

IV. Doctoral research at IMEC

As an interuniversity research center IMEC conceives as its important mission the integration of graduate education and research in a strong collaboration with the academic community in Belgium. Study and research at the graduate level have always held a prominent place at IMEC. Ph.D. students have important roles in wide-ranging research activities; this participation is vital to the educational experience of students and to the success of the research itself. The universities associated with IMEC award doctoral degrees in engineering, physical sciences, and chemistry and graduate students at IMEC are registered also at the universities of Leuven, Gent or Brussel. Financial aid is arranged through IMEC and is sufficient to cover all living expenses, housing, health insurance and registration as a student. To be admitted as a regular graduate student, an applicant for physical sciences and chemistry must have received a bachelor's degree or its equivalent from a college, university, or technical school of acceptable standing. Applicants for doctoral degrees in engineering must have successfully followed a five-years program leading to the equivalent of a master degree.

The doctor's degree requires four years beyond a baccalaureate or masters in the same field. The requirements include amongst others completion of an acceptable thesis prepared at IMEC, unless special permission is granted for part of the thesis work to be done elsewhere. Students normally start research in October.

V. Interaction with industry and with other research institutions

An important funding is coming from the government of Flanders. This allows IMEC to perform strategic, own internal research and to build valuable background information (BI). Such BI constitutes an excellent and attractive basis for cooperation with industrial partners, allowing them to reduce, by using IMEC's BI, both the complementary costs needed for dedicated joint R&D projects (foreground information, FI) and, more importantly reduce time-to-market.

During its fourteen years of existence, IMEC has built up a proven ability to understand and to meet industrial needs and requirements in a quickly evolving and highly competitive environment. As such, IMEC stands out as a major independent research resource for industry. IMEC has developed a variety of specific formulas of interaction as a strategic technology partner for industry, in which flexibility, quality of research and an in-depth knowledge of the industrial roadmaps are crucial factors of its success.

Within its overall microelectronics R&D strategy; IMEC concentrates on a number of R&D areas, as discussed in more detail hereafter. The major drive is to build an internationally accepted leading edge competence, leading to industrial applications.

As part of its strategy, IMEC is cooperating very closely with a worldwide network of industrial top performers to interact with them on strategically important topics in an early stage of research.

Furthermore, as IMEC's background information portfolio (with own industrial property rights (IPR)) has grown substantially over the years, more and more application-oriented research is being conducted with both local and international industrial partners. The interaction with industrial partners also constitutes an essential complementary funding, as the costs for deep-submicron microelectronics research are increasing rapidly, allowing IMEC to maintain its leading edge position.

IMEC interacts with industry in several ways, such as:

1. IMEC's Annual Research Review Meeting (ARRM). Industrial partners enrolling for IMEC's ARRM do not only get acquainted with IMEC's strategic R&D orientation at an early stage, they are also automatically informed about major IMEC scientific breakthroughs through its annual reports, scientific report, newsletters, articles,... Furthermore IMEC organizes about 130 topical seminars per year to which such industrial partner (enrolled for the ARRM) is entitled to participate free of charge.

   IMEC's ARRM has grown over the past 8 years to become a very dynamic and high level platform

gathering more than 130 topmanagers from all over the world. The ARRM 1999 is scheduled for October 27-28. Subscription is also possible through Internet at IMEC's homepage (http://www.imec.be) under the heading Industrial Window.

2. IMEC's Industrial Affiliation Program (IIAP) is a real R&D cooperation scheme, which has grown into a very popular way of cooperation. IMEC's IIAPs allow for collaboration between industrial researchers and an IMEC research team focused on a specific topic or technology area. As part of this collaboration, the relevant technology owned by IMEC (IMEC's background information) in this specific area, before the start of such an IIAP project, can also be transferred to the industrial partner.

   IMEC has selected a limited number of research areas in which it has built up a considerable BI. Based upon this BI, IMEC is setting up research programs involving an important core of IMEC researchers.

Industrial partners are invited to join such IIAP research program, in a well-defined research area, on a bilateral basis. This means that IMEC and the industrial partner define together, on a bilateral basis, a project fitting in IMEC's overall IIAP research program but allowing the industrial partner to tune the bilateral project to some of its particular needs. Once such bilateral technical scope is being agreed upon between the industrial partner and IMEC, the project results (deliverables) are being defined as well.

Each industrial partner joining IMEC's IIAP program is invited to delegate a specialist to IMEC's site (industrial resident). Such industrial resident is executing, at IMEC's site, the project in close cooperation with IMEC's research team in that Field. If a full time residentship is not feasible, a solution for a smaller period of residentship can be allowed. Experience shows that a presence of at least 6 months per year is contributing to a higher and more intense transfer of IMEC BI to the industrial partner, further increasing the benefits for the industrial partner.

With respect to intellectual property rights (IPR) on the additional project results (FI), and for each bilateral project, the results are labeled as follows:
- more generic or methodological type of results which are also based upon IMEC's background information are co-owned by both IMEC and the industrial partner, without any accounting to each other. This means that each party can freely use such results. The results are also shared with other industrial partners, joining up IMEC's IIAP program and are labeled in the agreement as R_1 results;
- company specific data or confidential information: such results are labeled as R_2 results and are the exclusive ownership of the industrial partner;
- for some contract types IMEC introduces the notion of intellectual property owned solely by IMEC (R_0 results). The industrial partner however is guaranteed to have a license on these results, providing full user rights for the industrial partner. This R_0 type of intellectual property complements the intellectual property that is co-owned with the industrial partner (R_1 results) and the IPR that is exclusively owned by the company (R_2 results). In a more general definition, R_0 results relate to fundamental, generic methodologies.

The IPR labeling of the deliverables (as R_0, R_1 and R_2 results) is done before the project starts and forms part of the agreement (technical annex of the agreement including the deliverables and IPR labeling).

The industrial partner furthermore gets access to both:
- IMEC's background information in the research domain specific to the IIAP;
- the R_0 and R_1 results of the other industrial partners being active in the same IIAP.

The IIAP formula is offering a multitude of advantages to the industrial partner such as:
- access to strategic IMEC background information at an early stage;
- access to other R_0 and R_1 (shared)-results from other partners in the same IIAP;
- the industrial researcher is taken up into the IMEC mixed research team to execute the IIAP project. This intensifies the process of transfer of technology and shortens the learning curve;
- flexible interaction between the research team at IMEC (including the industrial researcher) and the industrial headquarters;
- each IIAP contract is conducted on a bilateral basis, allowing for tuning and confidential information (exclusive R_2 results) as agreed upon;
- each IIAP contract is standard as well as the corresponding prices.

The IIAP approach is offering a number of leverage effects:
- pricing leverage: through the cost-sharing principle of R_0 and R_1 results;
- information leverage: each industrial partner gets access to much more information (project information, IMEC background information, R_0 and R_1 results of other program partners) than its financial commitment;
- cross-fertilization leverage: through the sharing of R_0 and R_1 results and through a good combination by IMEC of leading edge partners, also coming from complementary fields (e.g. foundries, equipment manufactures, material suppliers) but interested in the same research topic a rich cross-fertilization effect is being generated;
- time-to-market leverage: through the IIAP mechanisms, an industrial partner is getting a competitive advantage in both strategic results and rapid time-to-market.

IMEC currently, has IIAPs in the following areas:
- optical lithography (248 nm and 193 nm lithography);

- cleaning technologies and environmental, safety and health issues:
- silicide technologies;
- interconnection technologies; composed of three sub-programs:
  - advanced metallization (Al and Cu);
  - low-k dielectrics (for both Al and Cu);
  - chemical mechanical polishing, including Cu;
- advanced silicon materials and devices (<0.1 μm);
- integrated ferroelectrics;
- multimedia image compression (MPEG-4);
- integrated tranceivers for broadband wireless multimedia communication
- SoC++, object-oriented system-on-a-chip design.

3. The Industrial Residentship (IR) formula allows an industrial partner to make use of the available IMEC state-of-the-art infrastructure and/or expertise and background information to perform more application-oriented R&D, at IMECs premises. Hence, this type of cooperation is more application-driven. Apart from a hosting fee, a background information fee (royalty) is being charged for the use of such IMEC background information (if applicable).

   The industrial resident performs his project at IMEC (duration depending on the nature/complexity of the project) being assisted by IMEC. experts (including appropriate training and access to IMEC's BI, if necessary).

4. Cooperative projects (straightforward contract research), either bilateral or multilateral (e.g. through R&D programs of the European Commission), can be conducted in the various research domains of IMEC's R&D strategy, based upon clearly defined and agreed upon technical specifications and contractual terms.

5. Training courses covering the whole spectrum from VLSI design to process technology are organized. INVOMEC provides a coherent training program on hands-on design technologies, EDA (electronic design automation) and tools and methods for designing embedded systems. Custom training is offered to companies and special training course are regularly organized on deep-UV lithography for ASML and its customers.

   No less than 540 students enrolled in the Interuniversity Postgraduate Course on Telecommunication, which can be followed throughout Europe by videoconferencing.

   In 1999, a new microelectronics training center will be set up to give basic and advanced training in process technology and IC design.

   IMEC is also recognized by the European Commission as a Large Installation Program (LIP) site for design technologies.

6. An increasing variety of well proven, IMEC owned. complete processing technologies (photovoltaics, CMOS (0.7 μm, 0.5 μm, 0.35 μm, 0.25 μm and 0.18 μm), a flash EEPROM non-volatile memory HIMOS (0.7 μm and 0.35 μm) and BiCMOS (0.5 μm and 0.35 μm) are offered to industry through appropriate licensing agree-ments, associated technology transfer and training actions. All dedicated process modules can be transferred.

In 1998 IMEC collaborated with a wide variety of companies and research institutions from the following countries:
Austria (6), Australia (1), Belgium (110), Brazil (2), Canada (7), China (2), Czech Republic (6), Denmark (7). Finland (7), France (70), Germany (98), Greece (7), Hungary (5), India (1), Ireland (9), Israel (4), Italy (36), Japan (5), Korea (1), Lithuania (2), Mexico (1), Moldavia (1), Norway (7), Poland (9), Portugal (8), Romania (2), Russia (5), Singapore (2), Slovakia (6), Spain (22), Sweden (17), Switzerland (18), Taiwan (1), Thailand (1), The Netherlands (31), Ukraine (3), United Kingdom (74), United States (32), White Russia (1), Zaire (2)

For more detailed information about IMEC's collaboration partners and figures, see our annual report which is available on request at the Public Relations department.

In 1998, IMEC carried out research contracts for 1561 million Belgian Francs (39 million EURO), which represents a further growth as compared to 1997 of 10%.

Besides the numerous bilateral contracts IMEC was also involved in 135 R&D contracts with the European Commission. One of the key projects was Advanced CMOS in Europe (ACE), in which the development of 0.18 μm CMOS front-end & back-end technology was done. IMEC is also contributing extensively to several projects run by MEDEA, the European industrial consortium coordinating large projects in the area of semiconductor Technology, equipment and applications. IMEC's involment in R&D projects for the European Space Agency (ESA) was comparable (in absolute terms) to 1997.

Interaction with the Flemish industry

1998 was also characterized by a further interaction with the Flemish industry. This interaction, both in terms of contract research income (492 million Belgian Francs or 12.3 million EURO) and the number of industrial partners (65 different contract partners in 1998) is further underpinning the economic dynamics in the Flanders region.

IMEC expresses its gratitude to IWT (Institute for the Promotion of Scientific and Technological Research in the Industry) who has been acting as an important catalyst through its cofunding policy.

VI. Flanders, an attractive and dynamic location for new IT-driven industrial activities

The internationally recognized expertise of IMEC and its close collaboration with the highly, reputed Flemish universities, is creating new industrial dynamics in the field of Information Technology (IT) around a number of complementary axes:

I. Design oriented activities

Together with a number of other partners, IMEC created the DSP Valley initiative in 1994. DSP Valley is regrouping a unique concentration of close to 450 DSP experts in the Leuven area alone and is enhancing a fast growing use of DSP in innovative new applications. Up to now already, 13 companies and research institutions have been clustering together in a dynamic and complementary way. Further rapid expansion being expected in 1999.

P Simkens, Managing Director DSP Valley;
Tel. +32 16 281225, Fax +32 16 281779,
peter.simkens@dspvalley.com.

Next to a fast growing number of existing, fabless systems design oriented cornpanies - both small start ups and multinational companies - also a new joint (K.U.Leuven/IMEC) spin-off company in the field of analog design has been created early 1998.

DSP Valley is being recognized as a cluster by the Flemish government in 1996 and is teaming up with the Flanders Language Valley initiative, which concentrates on speech processing activities. Flanders is indeed offering a world class expertise in this field with leading edge companies.

Furthermore, an increasing number of foreign systems design oriented companies have selected Flanders to settle down around IMEC and to become a member of DSP Valley. The major drive was both availability of leading edge know-how and experienced workforce. DSP Valley is offering, together with the universities and with IMEC, both access to well-trained talent and to streamlined training initiatives in the field of DSP and ITC.

2. IC manufacturing

Over the past years IMEC has been establishing a truly international network of process technology, partnerships with a wide variety of IC manufacturers all over the world (such as amongst others Alcatel Microelectronics, AMD, Cypress, EM Microelectronics-Marin, IBM, Intel, Micronas-Freiburg, Mitel Semiconductors, Motorola, National Semiconductor Corporation, Philips, ST Microelectronics, Siemens, Sony, Thesys/AMS, TI, Tower,...), with equipment suppliers (Applied Materials, ASM International, ASM-L, Balzers, Steag Pokorny, TEL, Semitool...) and with material suppliers (such as Ashland, BOC, JSR, Olin, Wacker). New investments in these fields are underway in 1999.

Based upon this unique concentration of very advanced semiconductor processing technology expertise, the government of Flauders took an important decision in 1996 to start a focused action, with a view to attract IC fabs to Flanders in the coming years.

The Flemish region is indeed a very attractive location for many reasons:

- a unique availability of excellent expertise in IC process technology and other related R&D expertise at IMEC;
- a well established education system tailored towards IT;
- rapidly growing system oriented, fabless design industry and a take-off of an advanced IC packaging industry (both advanced IC assembly lines and IC packaging inspection systems);
- 10 IC fab units and a widespread IC fab support industry available within an one-hour drive;
- very attractive sites for IC fabs, approved for IC manufacturing activity, next to dedicated science parks for more design oriented, fabless activities;
- very competitive conditions for large-volume consumption of water and electricity:
- very high-standard of working ethics and productivity;
- multilingual quality of the labour force;
- central location towards the customers of IC fabs (UK, France, Germany, The Netherlands, Switzerland, Austria, ...) and very close to Brussel, the HQ of the European Union;
- attractive incentive packages and opportunities for cofunding of strategic R&D;
- high quality of life.

A site suitability analysis of two locations in the province of Limburg has been completed, including air, water and soil quality, vibrations and geotechnical conditions. Both sites of over 40 ha (100 acres) received the label "excellent" from the German engineering and construction company MW-Zander (formely Meissner+ Wurst), a member of the Jenoptik group. Presently, we have received the environmental permit for the first site. This pro-active attitude of the regional development authority will shorten the time-to-market for any, interested investor.

In a joint effort with Flanders' Foreign Investment Office (FFIO), MW-Zander, is considering several new business models that would make it much more cost attractive for semiconductor companies to locate their business in Flanders. One of the models is to form a consortium to finance the building of the complex and the facilities and provide them on a lease basis to one or more semiconductor manufacturers. This model represents an innovative form of partnership and would result in a smaller cash lay-out for the semiconductor company. Also, having a turn-key contractor run and maintain a centralized complex, including a co-generation plant, the ultra-pure water distribution, the chemical and gas management, the waste treatment and safety systems, will also result in a considerable increase in efficiency and thus an overall cost reduction and reduction in environmental impact. The facility financing, installation and management could also include the processing equipment. The preliminary design provided by the A.M.A. architects group for the "science park" style facility not only provides room for a Technology Center, which would house centralized training facilities, but also e.g. equipment development labs and office space for design and fabless companies.

For any further inquiry, on these opportunities for setting up in Flanders, please do not hesitate to contact Dr. Roger De Keersmaecker, who has been seconded from IMEC to FFIO in order to coordinate and to manage such foreign, inward investments towards Flanders.

Dr. R. De Keersmaecker can be contacted at
tel. +32 2 2275311, fax +32 2 2275310,
e-mail: Flanders@ffio.be

3. Packaging industry

Based upon a new plastic stud grid array (PSGA) technology, jointly developed by IMEC and Siemens, a commercial launching of this new IC packaging technology has been taken in 1998 by Siemens, who has exclusive rights on this technology. This PSGA IC packaging technology offers unique advantages (both in terms of price per pin-count and of performance) for complex chips with medium and high pin-counts.

In 1998, CS2, a new semiconductor assembly foundry company active in advanced packaging technologies has been setup. CS2 will focus on area-array technologies, such as BGA, flex-based area arrays, CSP and multi-chip modules.

Also in the field of MCM-D a new industrial activity is being prepared.

4. Microsystems

Finally; based upon IMEC's expertise and technology, in the field of microsystems, a number of new industrial initiatives (based on smartpen technology, image CMOS sensors, ...) have been created. Other initiatives and new investments are being prepared for 1999.

5. Venture capital and infrastructure

In conclusion, we can state that the Flanders region is preparing a strong growth in 4 complementary fields, being:

- design oriented activities;
- IC manufacturing;
- packaging activities;
- microsystems;

based upon a world leading technology expertise supported by IMEC and the Flemish universities.

To support this evolution, two new science parks, as well as fully equipped sites for IC production facilities, are being prepared.

In addition, an independent IT venture capital fund IT-Partners, 75M$ (1,859 million EURO), has been setup end of 1997, as an initiative of IMEC. The availability of such fund, specialized in ICT, shall further boost the IT-driven industrial activities in the region.

VII. Logistics

IMEC has the following different departments which play an important role in supporting the research activities:

- **Technical Support and Computer Logistics department with the following activities**

Director: W. Fluit
Members: K. Adams, G. Alaerts, F Arcq, F Bangels, E. Bergans, W Blommaert, G. Bollen, H. Camps, H. Ceustermans, B. Charliers, A. Claes, M. Clarysse, J. Darche, A. Debie, M. De Becker, H. De Vadder, I. De Waelhevns, B. De Winter, E. Denruyter, N. Dewaele, L. Doclot., M. Elsen, E. Engels, V Fonderie, M. Frooninckx, C. Gevens, N. Gillemot, F Hendrickx, G. Hennau, L. Huysmans, B. Jaecques, A. Joutear, J. Klykens, S. Konings, F Lens, L. Marent, H. Meulemans, T. Meulemans. I. Nijskens, A. Opdebeeck, A. Pardon, C. Paridaens, L. Pauwels, F. Poppe, D. Roelants, J. Sevens, R. Severyns, E. Sledsens, N. Sleeubus, G. Stoops. P Swevers, J. Van den Berge, M. Van den Bergh, L. Van Dromme, L. Van Even, R. Van Eylen, R. Van langenhoven, K. Van Ranst, P Vandeloo, J. Vandenbroeck, A. Vanhelmont, E. Vanlee, E. Verbee.men, K. Verbraeken, K. Verhaege, H. Verhaeghe, G. Verstraeten, W. Voets. C. Wils, D. Wouters, D. Wouters

- to exploit the different buildings using proper technical infrastructure; to take care of the installation of processing equipment;
- to organize and run the purchasing department including warehousing, safety and environmental aspects as well as quality approval (QA);
- to build up and exploit the electronic test equipment, necessary for characterization of submicron technology

- **Business Development Unit with the following major tasks**

Director: J. Van Helleputte

Members: I. Boerenkamp, R. Cartuyvels, K. Deneffe, J. De Wachter, R. Graulus, B. Grietens, B. Haven, O. Marzouk, K. Meuwis, R. Moons, K. Pollefeyt, L. Rottiers, V Ryckaert, J. Siffert, M. Sroczynski, R. Vanoppen, M. Van den Broeck, K. Van de Voorde, C. Vanherck, F. Vanheusden, C. Van Houtven, J. Wauters, K. Wuyts

- cost calculation and legal aspects of all contract research activities;
- IPR management: patents, licenses, .. ,
- marketing sales support for technology transfer;
- manage several databases (sales database, IPR database, project database, patent database)
- stimulation of the interaction with the Flemish industry;
- assistance for the creation of spin-off companies;
- collaboration with existing organizations to attract foreign investors in the field of ICT;
- the topics covered by the public relations department are:
  - IMEC publications (Annual report, Scientific report, IMEC newsletter, Inter-Connect, Internet information)
  - press contacts (both local & international)
  - organization and logistic support for in-house happenings (Annual Research Review Meeting, exhibits, ...) as well as for participation in international technology fairs (FTI, DAC, Semicon West, ...).

- **Personnel Department**

Director: E. Daenen

Members: R. Azza, L. Decneut, N. Geuens, T. Gouverneur, P. Snoeks. K. Sporen, D. Stinissen, M. Van Tichelen, D. Velaers

The Personnel department is responsible for the management of human resources. It covers the full range of functions, from recruiting up to remuneration and performance management.

- **Budget & Finances department**

Director: A. Vinck

Members: I. Augustynen, I. Bogaerts, S. Callebert, P De Baets, P Dupon, V Gille, P. Herinckx, P. Paepen, R. Reynders. L. Timmermans

- fiscal, financial and legal reporting (internal and external);
- contract reporting;
- financial follow-up of licenses and royalties;
- financial audits and controls;
- treasury, accounts payable and receivable;
- budgets and monthly follow-up;
- (accounting) services and logistic support to spin-off companies.

- **Interuniversity relations**

Responsible: R. Mertens, M. Van Rossum

As an interuniversity center, IMEC works closely together with the Flemish universities: Universiteit Gent, K.U.Leuven, Vrije Universiteit Brussel, Universiteit Antwerpen, Limburgs Universitair Centrum and with the higher polytechnical schools. Ways of collaboration:

- the INVOMEC network;
- bilaterial collaboration with research groups at the universities;
- joint investments in the field of advanced analysis equipment

- **Library**

Responsible: G. Vanhoof

Member: G. Op de Beeck

- **Administrative personnel of the scientific divisions and logistics**
- Silicon Process Technology (SPT): C. Declerck, A. Distelmans, N. Van Turnhout, V Wijns
- Silicon Technology & Device Integration (STDI): H. Derdin, C. Declerck, L Vanmeerbeek
- Microsystems, Components & Packaging (MCP): Ch. Deboes
- Industrial Training INVOMEC: W. Fannes, I. La Riviere
- Design Technology for Integrated Information & Communication Systems (DESICS): K. Discart, A. Stas
- General Management (AA): C. Claes, C. Declerck, L. Vanmeerbeek, V Vranckx

National Microelectronics Research Centre, Ireland

1998 was an outstanding year of growth and achievement at the *NMRC.*

Total research income at over £6m was the highest ever achieved and represented a 18% increase over last year's figure, which itself was a record.

The increased contribution to our activities from the Department of Enterprise and Employment, at over £2m, was not only very welcome but was also the highest ever and represents a progressive recognition by the Department of the strategic role that the NMRC plays in maintaining and up-grading the technological capabilities of the electronics industry in Ireland.

In addition, it was very gratifying to hear the presence of NMRC being cited by both Motorola and Cypress Semiconductor industry leaders in their respective fields, as being the reason for establishing integrated circuit design centres in Cork during 1998.

I am very glad to be able to announce that the Steering Committee of the European Solid State Devices Conference (ESSDERC) have decided to hold their meeting in the year 2000 in Cork. This extremely prestigious meeting, the largest of its kind in Europe, at which 400 plus of the world's leading solid state researchers gather to discuss progress in the area of microelectronics technology is held annually at a different location in Europe. This is the first occasion it is being held in Ireland, and will be an extremely important event which the NMRC will organise. The General Chairman is Mr. Frank McCabe, Managing Director, Intel Ireland Ltd., and a member of the NMRC Industry Committee, while the Technical Chairman is Dr. Alan Mathewson, Assistant Director Technology, Characterisation & Modelling, NMRC.

A new Environmental Services Laboratory was successfully commissioned during 1998 and has already completed analysis projects for companies such as Motorola, Analog Devices, Artesyn Technologies and EMC. Other NMRC activities in this area, of growing importance to society and to the electronics industry, were the filing of a patent for a toxic metal sensor developed by our Silicon Technology Group in collaboration with a local multinational company, and a large project on the reliability of lead-free solders.

Examples of other initiatives of direct relevance to industry which commenced during 1998, were the development of advanced process reliability investigations tailor made for specific products, and the development of a unit to deal with design evaluation of Smart Card products. Given the growing importance of e-commerce, the Smart Card initiative is considered a very timely support service for industries such as banks, telephone companies etc., who will be concerned about the integrity of their Smart Card Services.

1998 also saw the continuation of a project on advanced flip-chip technology with Intel. The objective of this basic research programme is to investigate the development of low cost chip bumping processes.1999

will see the continuation of the excellent progress made in this project last year.

The expansion of NMRC's second Silicon Fabrication Unit, dedicated to non-CMOS compatible processes and microsystems technology, was completed during 1998. Non-CMOS compatible process steps can be carried out in this area, and last year it allowed NMRC to develop novel-micro-inductors and transformers for an Irish customer and micro-optical benches for a large UK industrial customer.

During 1998 we continued with our policy initiated two years ago of an increased involvement in longer term basic technological research. A further 6 post doctoral fellows were hired, bringing the total number of PhDs now working at the Centre, to 48. Examples of areas of advanced research undertaken during 1998 were at the interface of the biological sciences and microelectronics; the development of biological sensors, as well as the development of biological based self-assembly of microelectronic components. In addition, further progress was made in the development of optical devices for inter and intra chip communication.

In the final round of the Fourth EU Framework Programme we had major success in both the ESPRIT Advanced Research Initiative and the Industrial Materials Programme, with a total of 12 projects commencing towards the end of 1998.1999 sees the beginning of the Fifth Framework Programme and NMRC researchers will be very active to ensure that our level of involvement in this important EU Programme remains at least as high as it has been in the past.

During the last academic year, the number of our postgraduate students increased from 89 to 108, including 43 studying for the PhD Degree, an increase of 10 from last year's figure. This was an impressive growth given the many job opportunities available for good students in the Irish economy today.

In 1998 an Innovation office was set up in the NMRC, staffed by a Group Manager and two Commercial Project Managers. The aim of this initiative is to focus on the development of new business and the promotion of NMRC services. It will also provide a technological foresight service covering market trends, and a greater level of support for the protection and commercialisation of intellectual property within NMRC. Following a period of about a year's familiarisation with the various technology teams within NMRC, it is planned that the Innovation Services function be privatised so that it can operate with a real commercial ethos and be the customer interface for NMRC industrial services and our intellectual property portfolio.

During the year we had 8 new patent applications with 5 patents being granted, our highest ever number. For the first time, we also exhibited the range of technological services we offer at two major European electronics exhibitions, Semicon (Geneva) and Electronica (Munich).

Finally, in this my last NMRC Annual Report, I would like to pay a special tribute to all of the staff and students I have worked with at the Centre over the last 18 years. It has been for me truly a wonderful privilege to work with such dedicated, committed and enthusiastic people. Long may the NMRC be so fortunate that it can continue to be of service to industry, education and research in the years ahead.

Prof. G.T. Wrixon,
January 1999

AMS

Company Profile

For over 17 years Austria Mikro Systeme International AG has specialised in developing and producing application-specific integrated circuits - ASIC's - and application-specific standard products -ASSP's- and offers a broad range of customer solutions for the automotive. communications and industrial sectors. The Company is one of the few European semiconductor manufacturers and one of Europe's market leaders in the field of mixed digital/analog ASICs. Its headquarters are located at Unterpremstätten near Graz where all the departments necessary for ASIC and ASSP production, such as R&D, design, mask lithography, wafer production, assembly and testing, are situated under one roof.

The Company is organised into three distinct market and customer oriented business units: automotive, communications and industry. Each business unit is managed as a separate profit centre, with complete responsibility for sales, marketing and design, taking its lead from clearly defined core corporate targets.

Austria Mikro Systeme International has been listed on the Vienna Stock Exchange since June 1993. 100% of the shares are free float.

The Unterpremstätten site has a complete production facility producing CMOS and BiCMOS technologies with structural widths down to 0.6 μm. All quality assurance measures are based on ISO 9000 and ISO 14001 standards. Austria Mikro Systeme International also has the CECC 90000 certificate and has been awarded the STACK Technical Approval for advanced quality management by STACK organisation, a group of well known international firms in the telecommunications and computer industry. Within the framework of the joint ESPRIT research project of the European Union, the Company is working and researching intensively with the world's leading semiconductor companies. This gives Austria Mikro Systeme International's 100 highly qualified design engineers access to the latest research technologies. Austria Mikro Systeme International maintains design centres in Unterpremstätten, Dresden and Budapest and has sales offices in Paris, Milan, Stockholm, London, Munich, Hamburg, Stuttgart, Düsseldorf, Bad Camberg, Budapest, Barcelona, Hong Kong, San Jose/California and Yokohama/Japan.

Positive forecasts for the semiconductor industry at the start of 1998 proved incorrect. Substantial over capacity and a fall in demand in certain market segments resulted in a 9% decline in total market sales. Because of our high level of specialisation, Austria Mikro Systeme International did not experience the same reduction in prices that high-volume products were susceptible to. Nevertheless, a change in customer ordering habits,

difficulties in marketing the spare manufacturing capacity at Thesys and the phasing out of some key products resulted in a 2.2% reduction in our sales revenue. The erosion of market share experienced in previous years, however, was halted and the 9% increase in new projects and the resulting 14% rise in engineering sales were clear indications that Austria Mikro Systeme International exploited all new market opportunities. I am confident that we now have a solid foundation for continued growth.

In April 1998 I resumed overall responsibility for the Austria Mikro Systeme Group. Working closely with a well known, international technology management consultant, we developed a new platform for Austria Mikro Systeme International's corporate strategy. Going forward, we will build upon our existing expertise in the development and production of application-specific mixed analog-digital integrated circuits (ASIC's). We will increasingly focus on the more specialised applications of our technology. We shall continue to offer special skills in accelerator and magnetic sensor technology, high frequency applications for the automotive and communications industry, security engineering in the automotive sector and system developments for measuring instruments. Co-operating closely with our customers, we will develop application-specific standard products (ASSP) in order to permit substantially wider marketing of our technology than is currently possible in the case of ASICs. The range of circuit design products we supply, will be enhanced by our COT-service (Customer Own Tooling). We aim to capitalise on our position as the leading European COT player by moving into international markets. A first step has already been achieved with our increased presence in the USA.

The new corporate structure of Austria Mikro Systeme International will also help us achieve our business objectives. With the creation of three strategic business units with complete P&L responsibility we shall be in a much stronger position to service our customers in the automotive, communications and industrial markets. The specialised departments of COT Engineering, Design Technology and Corporate Marketing will provide support for these business units. I am pleased to report that these departments will be managed by a team consisting of both experienced staff and newly recruited managers.

During recent months substantial efforts have been made to address the unsatisfying situation with our subsidiary, Thesys. We have agreed with the Free State of Thuringia, which owns 48.75% of Thesys, to build a new basis on which the two companies can co-operate. The close co-operation on production will continue as before. but in future we shall be able to act independently out in the market. Our shares in Thesys will be transferred back to the Free State of Thuringia subject to the outstanding approvals.

The availability of a state-of-the-art fabrication facility for "deep submicron" technology has been the main focus of comprehensive planning works of last year. Plans for the construction of a 200 mm wafer fabrication plant have progressed substantially and I expect final decision for it within the forthcoming months.

1998 was an important and challenging year for our Group. I would like to thank all my colleagues for their efforts which in future will justify our shareholders' confidence in Austria Mikro Systeme International.

Hans Jörg Kaltenbrunner
(President and Chief Executive Officer)

Research and Development

As in previous years, the development of new products and process technologies was given a high priority. ATS 261.8 million, or 16.3% of the entire sales revenue, was invested in R&D in 1998; the highest R&D investment Austria Mikro Systeme International has made since the Company was founded. One of the core strengths of the Company is the diversity of its leading-edge technologies leading to technically and economically optimized system solutions.

In addition Austria Mikro Systeme International's service package (software for circuit design, design rules, libraries, production support) focuses on offering every customer a solution optimised for his or her requirements. Based on a modern range of technologies and its considerable experience in mixed analog/digital circuits, Austria Mikro Systeme International is concentrating on product developments for information technology, industrial controls and automotive electronics. Building on its successful developments in integrated, customer specific circuits (ASICs), more application-specific standard products (ASSPs) will be offered in these sectors.

As a result of its technical expertise Austria Mikro Systeme International is involved in both national and international R&D cooperation projects. The Company also collaborates with well known firms in the field of microelectronics in order to cover peak demand and to buy in production modules which cannot be manufactured internally.

Austria Mikro Systeme International has the technical expertise and the necessary facilities for all development and manufacturing stages in the production of integrated circuits. This is the prerequisite for successful cooperation with prestigious partners in the research sector. At a national level, existing projects and cooperation projects with specialised university institutes and research institutions are being continued. These include the activities with Christian Doppler Forschungsgesellschaft and the Institute for Microelectronics of the Technical University of Vienna in the areas of process and componentry simulation.

As development costs and technology complexity rise, research cooperation projects are becoming increasingly important. In response to this Austria Mikro Systeme International is placing a special emphasis on the strategic European research programmes in which it is involved.

Several ESPRIT and MEDEA projects were successfully completed (CICDIP, IMPROVE, APPLE, PROMYMA) in collaboration with well known international semiconductor firms.

The PROMPT 2, MagIC, HIPOKRAT, SADE and TTA projects were continued as planned; HECTOR 300, ASTERIS, BC3 and APPEAL were successfully started.

The above projects focus on both the new and further development of semiconductor technologies and the other advanced themes in the field of circuit and system development, as well as the commercially successful implementation of new technologies.

Process Technology

The continual further development of mainstream CMOS process technologies forms the prerequisite for production of ever more complex circuits with increased specifications. Austria Mikro Systeme International has responded to this trend with corresponding developments in the "deep submicron" field. As a result, the competitiveness of the products manufactured at the Company has been significantly enhanced.

After successful completion of the project supported by FFF, the research promotion fund of the industrial sector, for the development of the 0.6 μm / 0.5μm technology generation, the development of a mixed analog-digital 0.35 μm process technology began. This process will form the technical and economic base for future entry into the 0.25 μm and 0.18 μm CMOS technologies, essential technologies for the production of ever more powerful systems of silicon. Additional FFF projects focus on the examination of new interconnect structures for components and the development of a technology with extremely low power consumption.

An important element of the research lay in the field of BICMOS (mixed bipolar CMOS) technology. Because of its internationally recognised expertise in this field, a cooperation agreement was made with the Canadian firm, SiGe-Microsystems Inc., for the implementation of an innovative and highly advanced technology for the production of integrated circuits for high frequency applications. High-speed hetro bipolar transistors (HBTs) made of silicon/germanium layers are inserted into an existing BiCMOS process platform. Products for a frequency range of up to 10 Gigahertz can be realised using this process. Mobile phones, satellite navigation and safety systems for cars are applications for this process.

Circuit Design

Building on Austria Mikro Systeme International's existing expertise in mixed analog-digital circuits, more advanced work was carried out in high-frequency and high-voltage applications as well as energy management circuits for mobile electronic systems. Additionally, technology in the fields of sensorics and system integration was substantially developed.

As a result of agreements lasting several years with leading CAD suppliers, Austria Mikro Systeme International now has access to most advanced circuit design systems.

For the newly developed processes (e.g. SiGe-BiCMOS technology) Design Kits consisting of library elements, component models, process-specific parameters and interface files for the CAD software are created. These Design Kits are used by internal development groups as well as by more than 500 customers throughout the world.

Further work on the design system, in particular in the "deep submicron" field, was concentrated on the integration of entire systems in one chip, made possible through the high digital component packing density which these new process generations permit. In each case the optimal combination of analog and digital processing of the signals is sought. High speed data converters (analog-digital and digital-analog converters) and processing units (signal processors) are needed to fulfill the demanding requirements.

Products

Based on Austria Mikro Systeme International technologies and its design bases, the following products have been successfully realised and launched on the market during the year:

- Single chip telephone with integrated hands-free function, dialler function and serial interface
- Transmitter/receiver circuit for electronic car keys in the ISM band (433 MHz)
- Drive circuits with high dielectric strength for industrial measuring technology (bus systems)
- Three-dimensional magnetic field sensor for precise position measurements in industrial and automotive electronics
- Analog/digital converter modules for speech signals (CODECs) for use in conventional and mobile phones
- Power line modem for transmitting data via conventional power lines
- Circuit for an airbag system

Production

As an ASIC manufacturer, Austria Mikro Systeme International focuses on providing customers who have the most varied requirements with a broad range of wafer fabrication processes. The specific expertise invested in the production operation is the ability to integrate this diversity into an economically optimised global process. Depending on the requirements, internal and external production facilities are involved.

In the course of a continuos improvement program yield, employee productivity and throughput time continued to increase. For example, the throughput time for wafer production was reduced by about 40% during the year under review.

In assembly, the diversity of packages, optimised for particular applications, is remarkable. In the reporting period, two new types were introduced: a package for magnetic sensors and a "Ball Grid Array" package, which is increasingly used for very complex circuits with a high pin count.

Austria Mikro Systeme International has an excellently equipped test department and many years of experience; it has an international reputation particularly in the field of testing mixed analog/digital circuits. Through hundreds of complex projects it has been possible to

gain a solid technical expertise base which when testing circuits for automotive, industrial and telecommunications applications gives Austria Mikro Systeme International a clear competitive advantage. During the past years special emphasis was given to the test of high frequency circuits that are used for example in mobile radio, GPS receivers and electronic car keys.

Due to the capital-intensive equipment, the optimisation of test procedures has a significant effect on chip costs. An expert system has been developed which continuously compares the test results with standard figures and supports the operator.

Looking forward to system integration in the future, Austria Mikro Systeme International has already ordered high performance testers of the newest generation for coping flexibly with expected new challenges.

One of the most important projects in the production field is the introduction of a new integrated production control system, which naturally also has to be Year 2000 compliant. The increasing complexity of our products demands the automatic flow of all stages of production. The high demands on quality of our products require ever better cleanroom conditions and the full documentation of each step of the process. The requirement for ever shorter delivery times and exact adherence to agreed deadlines forces us towards ever more accurate allocation of our resources.

The new Manufacturing Execution System PROMIS, which is highly regarded in the sector, has been integrated into the Company IT system at the Company's headquarters and fulfils all the requirements set out above. The diversity of processes and products typical for Austria Mikro Systeme International necessitates high expenditure on implementation; besides a large number of standard PROMIS modules, a series of company-specific adaptations is necessary. The entire application in its scope and complexity can therefore be seen as leading edge within the semiconductor industry.

COT Projects

Projects from the COT sector (Customer Own Tooling) are responsible for a significant part of the turnover of our Company. These projects involve the customer carrying out the design of the circuit, whilst Austria Mikro Systeme International provides the "Design Kits" for this. Design Kits consist of library elements, component models, process-specific parameters and interface files for the CAD software, all for very diverse design platforms. Austria Mikro Systeme International then manufactures the product. Depending on customer requirements the COT service package is completed by support in evaluation and ramp up of production. For these projects, customers have a broad range of high performance processes available. For example, a successful COT project was carried out early in 1999 with the American aircraft building company Boeing for the Mars Mission of NASA. The special features and quality characteristics of the high-voltage CMOS process developed by Austria Mikro Systeme International was crucial in the selection of the Company as a partner.

A special service is provided to customers through the supply of so-called MPWs (Multi-Product Waferruns). By combining several different chips on a wafer, the customer is offered a cheap entry to modern microelectronics. This is also of extreme interest to universities and research laboratories because it means they can try out the most advanced process technologies (e.g. SiGe-BiCMOS) at an early stage in their development.

KOLEDAR PRIREDITEV - CALENDAR OF EVENTS

MAY

MAY 6,1999

UK MICROSYSTEMS TECHNOLOGY CONFERENCE, RUTHERFORD APPLETON LABORATORY OXFORDSHIRE, UK

Based on survey of R&D in microsystems technology in the UK.

Contact David Topham, UKMSTS

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e-mail: dt@artscience.scotborders.co.uk

web: www.summit.rl.ac.uk

MAY 17-19,1999

CABLE & SATELLITE MEDIACAST LONDON, UK

Speakers include STMicroelectronics European marketing director Dr Bernard Beit and ARM multimedia business development and manager Noel Hurley (both on May 17).

Contact Neil Stinchcombe, Eskenzi PR

Tel: +44181449 8292

Fax: +44181440 4449

e-mail: Neil@ eskenzi.demon.co.uk

web: www.cabsat.co.uk

MAY 17-23,1999
SIXTH SEMI CIS EXECUTIVE MISSION AND EXHIBIT ZELENOGRAD, RUSSIA
Includes market seminars, symposiums, tours.
Contact Alla Famitskaya, SEMI Moscow
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JUNE

JUNE 1-4, 1999
49TH COMPONENTS & TECHNOLOGY CONFERENCE, SAN DIEGO CA, USA
Coutses covering BGA, LBGA, chip-scale and wafer-scale packaging. Contact Electronic Industries Alliance
Tel: +1703 907 7536
Fax: +1703 907 7549
e-mail: margieballinger@kemet.com

JUNE 7-9, 1999
12TH EUROPEAN MICROELECTRONICS CONFERENCE AND EXHIBITION, HARROWGATE, UK
Contact International Electronics and Packaging Society (IMAPS).
Tel: +1703 7581060
Fax: +1703 7581066
e-mail: abell@imaps.org
web: www.imaps.org

JUNE 22-24, 1999
EUROPEAN SMART CARD EXHIBITION & CONFERENCE, ZURICH, SWITZERLAND
Contact Martin Scott, Turret RAI
Tel: +441895 454438
Fax: +441895 454588
e-mail: 100730@ compuserve.com

FUTURE COMMUNICATION NETWORKS - Trends and Tradeoffs Twisted Pair, Coax Cable, Fiber Optics, Satellite and Wireless
St. Moritz Hotel, NYC June 21- 23,1999
Don Brown, MMRC Program Chair
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Email: donbrown@iwpc.org

1999 MCM Applications Workshop
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IEEE CPMT Staff Contact: Marsha Tickman, Executive Director IMAPS Staff Contact: Janet Kingston

If there are questions, or you desire more information (when available),

contact: Jack Balde at balde@webtv.net or Evan Davidson at davidsoe@us.ibm.com

JULY

JULY 5-9, 1999
ICNS3, MONTPELLIER, FRANCE
Third International Conference on Nitride Semiconductors. Contact Pierre Lefebvre, Secretary ICNS3
Tel: +33 4 6714 37 56
Fax: +33 4 67 14 37 60
e-mail: lefebvre@ges.univ-montp2.fr

JULY 12-16, 1999
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