REAL TIME DECODER FOR CODED SIGNALS MIXED WITH NOISE

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Key words: smart card, identification card, contact less integrated circuit, reader, recognition circuit, antenna, bit-stream, data rate, time window.

Abstract: An approach to decoding of serial data bit-stream is described. This approach is based on moving the time window, which makes an average number of received pulses in real time. The average value of the number of pulses is compared on the comparator with a hysteresis and its output shows decoded logic state. Such technique eliminates same spurious and some missing pulses in the incoming data bit-stream and increases the range of communicating devices.

Sprotno dekodiranje s šumom pomešanih signalov

Ključne besede: pametna kartica, identifikacijska kartica, brezkontaktno integrirano vezje, čitalnik, razpoznavno vezje, antena, tok podatkov, podatkovna hitrost, časovno okno.

Izvleček: V članku je opisan način za dekodiranje niza serijskih podatkov. Zasnovan je na premikajočem časovnem oknu, ki povprečuje v realnem času število sprejetih impulzov. Komparator s histerezo primerja povprečno vrednost števila impulzov in na izhodu se pojavi dekodirana logična vrednost. S takšno tehniko uspešno izločamo nekatere lažne in nekatere manjkajoče impulze v podatkovnem nizu, ki prihaja na vhod vezja ter s tem povečujemo razdaljo na kateri lahko uspešno komunicirata identifikacijska kartica in čitalnik.

1. Introduction

There are several methods to decode signals described in ISO standard /1/. Many systems use microprocessors and it is possible to save a part of input data bit-stream and recognize the coded information using this complex hardware. The goal of this work was to develop the minimized hardware, which is able to decode the input signal in real time, because the application requires the integration for high volume production where the reduction of cost is an important parameter.

The developed hardware is located on the chip, which is called reader and receives the signals from the smart card. The distance between smart card and antenna of the reader defines the quality of the received signal. If the smart card is very close to the antenna of the reader, the received signal is very strong and correctly detected in the analog part of the reader chip. This demodulated signal is used as input signal to the described recognition circuit, which decodes incoming bit-stream into the logic data. But increasing distance between smart card and antenna of the reader decreases demodulated signal and pushes it into the noise. The influence of this noise is shown on the demodulated bit-stream as a spurious and missing pulses. The described recognition circuit counts pulses in the moving window. This numbers are compared on the comparator and its output is high, if there is a group of pulses and is low, if there are not pulses or there are only a few spurious pulses. Signal from the comparator is synchronized and formed in the last block. Serial data on the output are decoded and corresponded bit_clock is shifted regarding to the upper mentioned signal.

2. Coded signals

Signal transmitted from the smart card to the reader is coded. This code is defined in ISO standard /1/ and can be used for two data rates. This design is performed for higher data rate (26.48kb/s) and all definitions for logic signals and preambles are valid for this speed of communication. Four times lower data rate has the same definitions. The number of pulses shall be multiplied by four and also all other times will increase by this factor. Increased number of pulses for logic definitions decreases the data rate, but increases the reliability of communication.

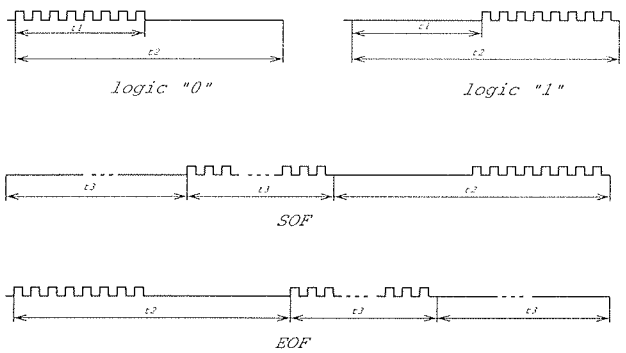

Fig. 1. Definition of coded signals using ISO standard /1/.

Code definitions for high data rate are shown on the figure 1. All definitions use the same sub-carrier frequency. Logic "0" starts with 8 pulses and then follows unmodulated signal with the same duration as is duration of 8 pulses. Unmodulated signal with duration "t1" and additional 8 pulses define logic "1".

The successful protocol with serial coded data requires two additional definitions:

- signal defining beginning of data: start of frame or SOF.
- signal defining end of data: so-called end of frame or EOF.

These signals are also shown on the fig. 1. SOF is defined with unmodulated signal of duration "t3" and then followed by 24 pulses of the same duration "t3" and a coded logic "1". The SOF is required for the synchronization of described recognition circuit. The correct received SOF starts the timing of recognition circuit. After this signal immediately starts decoding of incoming signals and bit clock is also generated. The last important definition is EOF. This signal tells the reader that the transmission of the data is concluded. EOF consists of logic "0" and followed by 24 pulses and an unmodulated signal with the same duration as the duration of 24 pulses. After an EOF is decoded, the receiver is reset and waits the next SOF.

3. Description of the recognition circuit

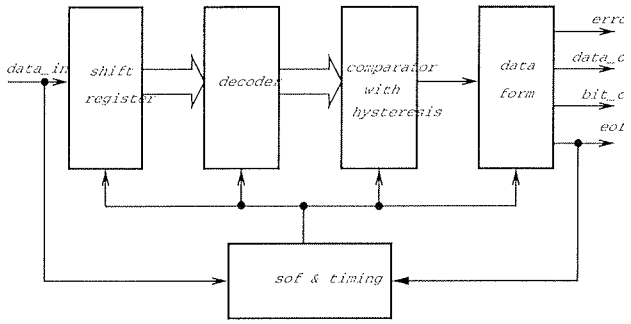

Fig. 2. Block diagram of recognition circuit

Block diagram of the recognition circuit is shown in the fig. 2. Demodulated signal from analog front end is connected to the input of this recognition circuit. Data are checked and after receiving SOF the complete recognition circuit starts with the appropriate timing. Serial data are shifted in the shift register and on its parallel outputs are connected to the inputs of decoder. This block check the numbers of "1" and decodes this number in a binary sequence. These signals are checked on the comparator. Output of comparator goes high, if the number on the inputs is changed from 4 [100] to 5 [101] and goes low, if the number is changed from 4 [100] to 3 [011]. Output from comparator is connected to the data form block where output signals are formed. This block generates output data bit-stream, bit clock and EOF. Bit clock is slightly shifted regarding the data bit-stream. Decoded EOF stops the operation of the complete circuit and the system is now waiting for the next input bit-stream with correct SOF.

3. Principle of operation

The most important signals are shown on the fig. 3., which explain developed algorithm and its realization in the recognition circuit. Upper part of the fig. 3. shows ideal signals. Data bit-stream on the input "data_in" shows "1", "0" and "1" and this shifted and decoded signal is present on the input of comparator as a number of pulses. Shift register creates time window where only eight possible pulses are visible at each time. Hysteresis is built in the comparator. Its output signal is connected to the data form block where this signal is formed and synchronized with the bit clock. Incoming pulses mixed with the noise are shown on the lower part of the fig. 3. There are some missing pulses in the group of pulses and a few additional pulses in unmodulated region of received bit-stream. This inconvenience decrease the span of received numbers at the input

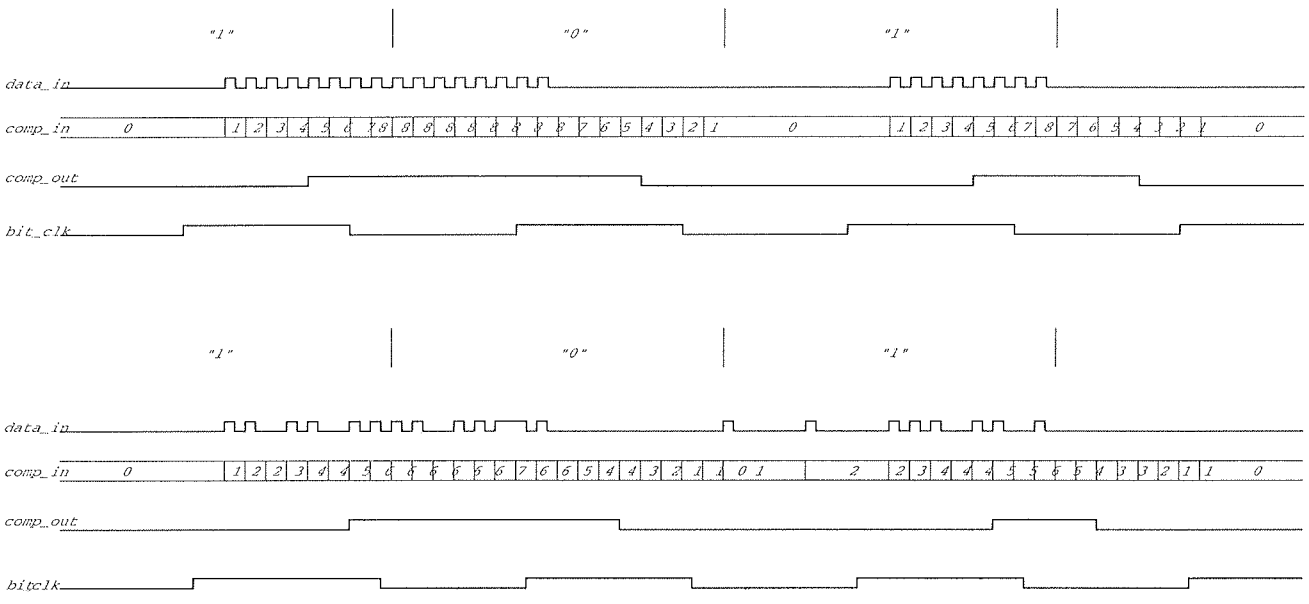

Fig. 3. Main signals of the circuit

Fig. 4. Simulation with correctly decoded output

of the comparator. That means the moving window of selected numbers makes an average of received pulses. The comparator produces logic signal from these numbers, but this signal is now shifted and its duration varies compared to the signal with ideal conditions in the upper part of the figure 3. Shift of the comparator output and its duration are taken into account when bit clock signal is generated. The result of this approach is signals with the jitter. If the noise in the incoming "data_in" signal is to high, this signal is to much corrupted and of course recognition circuit can not decode these signals correctly. In this case the signal "error" goes high.

4. Results

Many simulations were made with ideal and corrupted signals. The fig. 4 shows simulation with corrupted signal and its correct response. Input signal "data_in" mixed with the strong noise is shown on the fig. 5. This signal is too corrupted and comparator can not correctly decode it and "error" goes high.

5. Conclusion

Digital block is designed, which decodes signals from the smart card. The distance from smart card to the antenna of reader defines the quality of received signal. Correct decoding of corrupted incoming data bit-stream increase the reading distance between smart card and reader. The data protocol used corresponds to international standard.

References

/1/ ISO/IEC 15693-2 Identification cards - Contactless integrated circuit(s) cards -Vicinity cards - Part 2: Air interface and initialization, INTERNATIONAL STANDARD.

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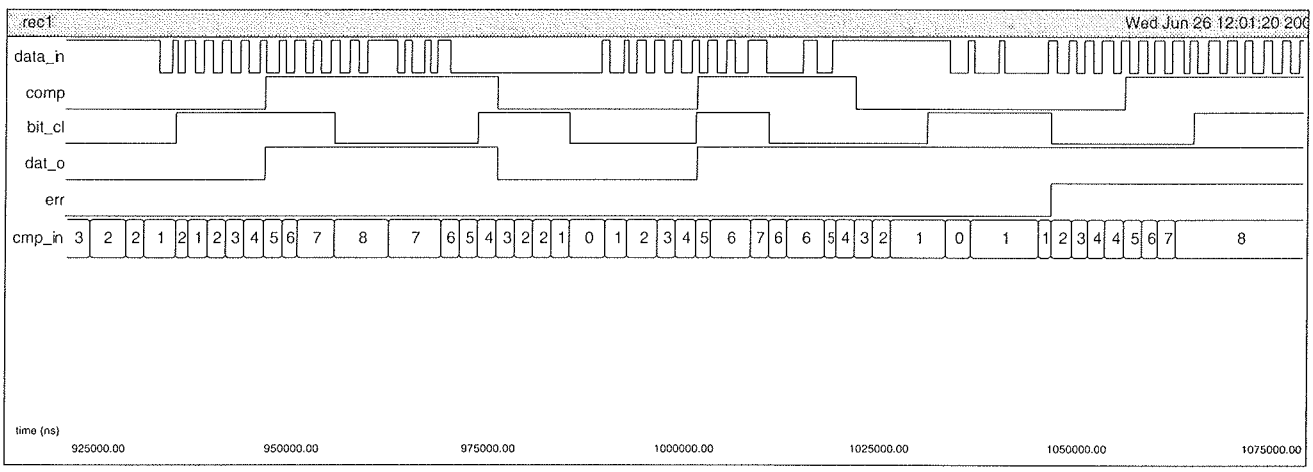

Fig. 5. Noisy signal on the "data_in" and corrupted output