UDK 621.3:(53+54+621+66)(05)(497.1)=00 ISSN 0352-9045

INFORMACIJE MIDEM 2·2001

Strokovno društvo za mikroelektroniko elektronske sestavne dele in materiale

Strokovna revija za mikroelektroniko, elektronske sestavne dele in materiale
Journal of Microelectronics, Electronic Components and Materials

INFORMACIJE MIDEM, LETNIK 31, ŠT. 2(98), LJUBLJANA, junij 2001

UDK 621.3:(53+54+621+66)(05)(497.1)=00 ISSN 0352-9045

INFORMACIJE MIDEM 2 ○ 2001

INFORMACIJE MIDEM LETNIK 31, ŠT. 2(98), LJUBLJANA, JUNIJ 2001

INFORMACIJE MIDEM VOLUME 31, NO. 2(98), LJUBLJANA, JUNE 2001

Revija izhaja trimesečno (marec, junij, september, december). Izdaja strokovno društvo za mikroelektroniko, elektronske sestavne dele in materiale - MIDEM.
Published quarterly (march, june, september, december) by Society for Microelectronics, Electronic Components and Materials - MIDEM.

Naslov uredništva
Headquarters
Uredništvo Informacije MIDEM
Elektrotehniška zveza Slovenije
Dunajska 10, 1000 Ljubljana, Slovenija
tel.: + 386 (0)1 51 12 221
fax: + 386 (0)1 51 12 217
e-mail: Iztok.Sorli@guest.arnes.si
http://paris.fe.uni-lj.si/midem/

Letna naročnina znaša 12.000,00 SIT, cena posamezne številke je 3000,00 SIT. Člani in sponzorji MIDEM prejemajo Informacije MIDEM brezplačno.
Annual subscription rate is DEM 200, separate issue is DEM 50. MIDEM members and Society sponsors receive Informacije MIDEM for free.

Znanstveni svet za tehnične vede I je podal pozitivno mnenje o reviji kot znanstveno strokovni reviji za mikroelektroniko, elektronske sestavne dele in materiale. Izdajo revije sofinanci rajo Ministrstvo za znanost in tehnologijo in sponzorji društva.
Scientific Council for Technical Sciences of Slovene Ministry of Science and Technology has recognized Informacije MIDEM as scientific Journal for microelectronics, electronic components and materials.
Publishing of the Journal is financed by Slovene Ministry of Science and Technology and by Society sponsors.

Znanstveno strokovne prispevke objavljene v Informacijah MIDEM zajemamo v podatkovne baze COBISS in INSPEC.

Prispevke iz revije zajema ISI® v naslednje svoje produkte: Sci Search®, Research Alert® in Materials Science Citation Index™

Scientific and professional papers published in Informacije MIDEM are assessed into COBISS and INSPEC databases.

The Journal is indexed by ISI® for Sci Search®, Research Alert® and Material Science Citation Index™

Po mnenju Ministrstva za informiranje št.23/300-92 šteje glasilo Informacije MIDEM med proizvode informativnega značaja.

Grafična priprava in tisk
Printed by
BIRO M, Ljubljana

Naklada
Circulation
1000 izvodov
1000 issues

Poštnina plačana pri pošti 1102 Ljubljana
Slovenia Taxe Percue

UDK621.3:(53+54+621+66), ISSN0352-9045 Informacije MIDEM 31(2001)2, Ljubljana

37th INTERNATIONAL CONFERENCE ON MICROELECTRONICS, DEVICES AND MATERIALS

and the WORKSHOP on

OPTOELECTRONIC DEVICES AND APPLICATIONS

October 10. - 12. 2001
Bohinj, SLOVENIA

PRELIMINARY PROGRAMME

http://paris.fe.uni-lj.si/midem/conf2001/

Elektrotehniška Zveza Slovenije

IEEE Slovenia Section

PWM DC MOTOR REGULATOR IC WITH EXCELLENT EMC BEHAVIOR

W.Marks, S.Ritz
AMS, Austria Mikro Systeme International AG, Graz, Austria

Key words: electric motors, DC motors, Direct Current motors, motor control, motor regulation, PWM regulators, Pulse Width Modulated regulators, AS8410 IC Integrated Circuits, EMC, ElectroMagnetic Compatibility, single chip solutions, high voltage technologies

Abstract: This is an introduction to the AS8410 control IC and associated device modules for PWM DC motor control. This IC enables equipment manufacturers to combine two features of electronically controlled DC motors, which were previously considered incompatible: High power efficiency (>95 %) and minimal electromagnetic radiation, to include the high frequency range (RF emission significantly below VDE0871, VDE0875, VDE0879 standards) with high PWM frequencies.

Extensive load failure diagnosis and error processing routine, as well as easily programmable operating modes, provide secure and low-cost application over a spectrum of DC motor control application.

Integrirano vezje za PWM regulacijo DC motorja z izvrstno EMC skladnostjo

Ključne besede: motorji električni, DC motorji na tok enosmerni, krmiljenje motorjev, regulacija motorjev, PWM regulatorji modulirani impulzno širinsko, AS8410 IC vezja integrirana, EMC kompatibilnost elektromagnetna, izvedbe na enem chip-u, tehnologije visokonapetostne

Izvleček: V prispevku je predstavljeno integrirano vezje AS8410 proizvajalca AMS za PWM regulacijo DC motorja. To integrirano vezje omogoča uporabnikom kombinacijo dveh lastnosti, ki sta pri elektronsko krmiljenih motorjih do sedaj bili nekompatibilni: visok izkoristek moči (>95%) in minimalno elektromagnetno sevanje zlasti na področju visokih frekvenc (RF sevanje občutno pod standardi VDE0871, VDE0875 in VDE0879).

Možnost nadzora in analize odpovedi bremena, rutina za obdelavo napak, lahko programljivi načini dela omogočajo varno in ceneno uporabo tega integriranega vezja v široki paleti regulacijskih elektronik za krmiljenje DC motorjev.

Motivation

The principle of DC motor speed or power/torque control and regulation through a pulse-width modulated electronic switch is not new. Such switch operation produced the desired motor speed-torque control, but caused electromagnetic emission of significant amplitudes in a wide, mainly high frequency range, making an obstacle to its wide application. It also prevented application in EMC-sensitive environments (e.g. automotive applications near other interference-sensitive electronic systems like car radio, airbag, etc.) or required additional, economically questionable shielding procedures. In such cases, exclusive analog motor control has been used, which holds the great disadvantage of poor power efficiency (high dissipation in the power regulating transistor).

The tremendous demand for energy-saving, convenient, environment-friendly (low-noise, EMC-conform) and cost-effective devices for electric motors with variable (controlled) speed and/or speed-torque has resulted in world-wide R&D activities of considerable expenditure.

These developments match the increasing use of brushless, electronically commutated motors. To reach a broad, low-cost electronic control systems are absolutely necessary for these motors.

We developed our standard product AS8410 and the associated modules for DC motor regulators (voltage regulators) with PWM control. On one hand, this allows the advantage of pulse control without the disadvantage of high interference emission, and on the other hand, provides a low-cost device for a broad application spectrum (for motors power-rated from a few watts to several kilowatts in different operating modes with comprehensive load diagnosis and error processing mechanisms).

The AS8410 realization was also designed to generally enable PWM control of inductive loads and/or inductance-affected loads (e.g. switch regulators) with very good EMC behavior. Since automotive field application was planned from the very beginning, all requirements for 12V or 24V direct system operation had to be met (load dump, burst and surge impulses on the battery supply, EMC susceptibility, minimal RF emission, broad supply voltage range, low current consumption, automatic sleep mode, etc.)

System solution and EMC- conform operation

The AS8410 is made with analog/digital CMOS (BiCMOS) high-voltage technology (2) and delivered in a standard SOIC16 package. The system concept realizes an ana-

log/digital (mixed signal) IC with primary analog functions. It contains a complete load regulator loop. Additionally, comprehensive load diagnosis and failure processing procedures, temperature and supply voltage monitoring and protection are integrated.

The AS8410 operates in a supply voltage range of V_{min} = 6V to V_{max} = 34 V (or 44V) enabling direct application to 12V or 24V automotive power supply. Operating temperature range: -40 °C to +125 °C.

The remarkable feature for achieving this good EMC behavior is the power (switch) transistor drive method. The power FET driver unit consists of fast current and voltage controlled current sources, and the control of these current sources through the instantaneous value of the on-load (motor) voltage (slew rate regulation). Finally, the motor performance rating (rated load current) is selected through the current control of these current sources (externally programmable), and the voltage control realizes the EMC-conform operation. With this application, the gate of an external power FET and the motor voltage time variation during the PWM motor voltage rise and drop is controlled by the motor voltage instantaneous value. In this way, the electromagnetic emissions of the entire control module are minimized and almost totally dissipate in the high-frequency range (Fig. 1). The exceptionally low emission levels, particularly in the high-frequency range, are clearly seen in Fig.1.

The motor regulator application does not require any filter devices.

The AS8410 system concept

The AS8410 forms a complete PWM DC motor regulator loop and consists of the following sub-blocks:

Set value input signal processing, generating the characteristic curve of the regulator (see Fig. 2), feedback value measurement (load detection at the high side of the motor), and a PWM generator (controlled by the set value and the actual motor current value) as well as the power FET gate driver. The control of the external power FET is effected by the special current controlled feedback sources described above. The control voltage is generated by an internal charge pump and is 10 V higher than the system power supply. The AS8410 requires only one supply voltage, which usually is the same as the motor supply, and ranges from 6V to 34V (V_{max} = 40V). Regarding the security concept, load failure detection circuits (over current, motor blocking, no load of the motor, or open wire, commutator and power FET short circuits) as well as over temperature and over or under voltage detection, are integrated. Additionally, a special circuit protects the power FET in generator mode of the motor (coast-down of motor due to mechanical inertia).

Sequence control is performed by a logic block, detecting systems status (failures, operating modes) and translating them into internal control signals and an external failure feedback signal (operating modus 1). See Fig. 2 for AS8410 system schematic.

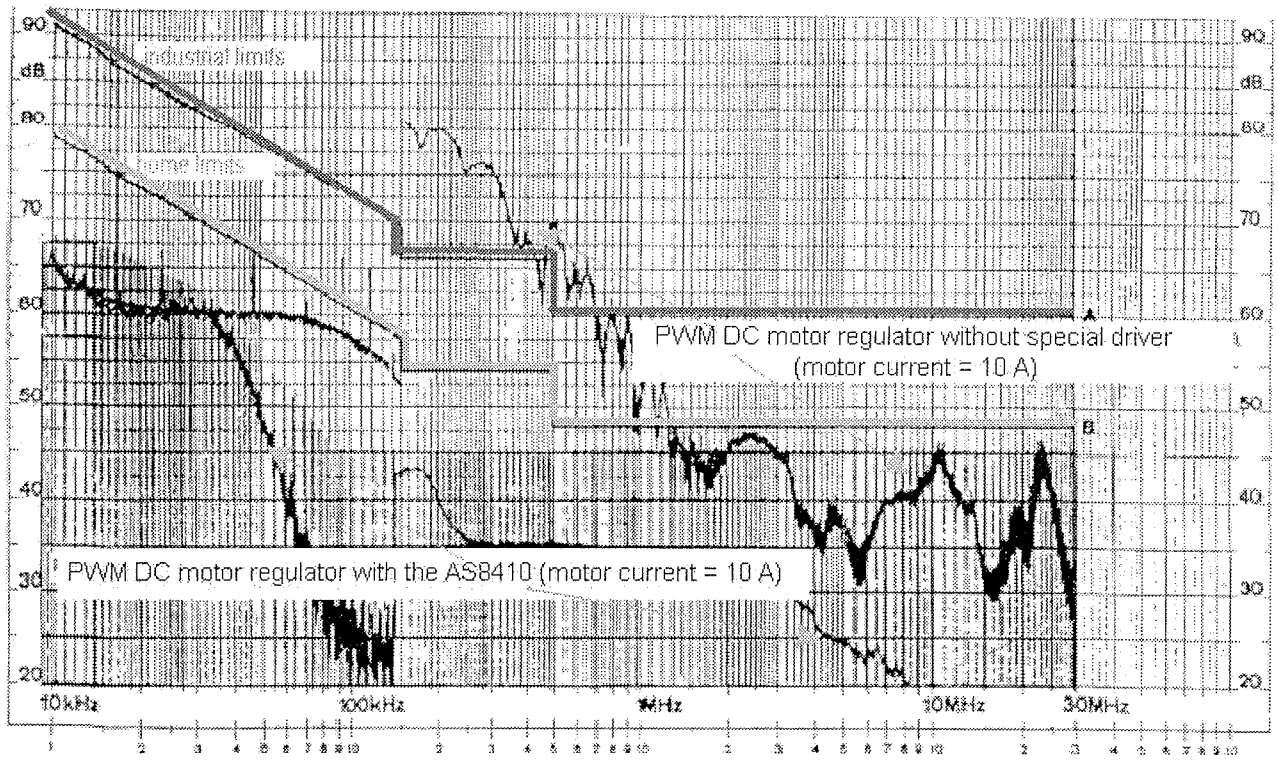


Fig. 1 Emission spectrum comparison - AS8410 controlled motor regulator versus a commercially available solution, showing much lower RF emission using a 10A rated motor current.

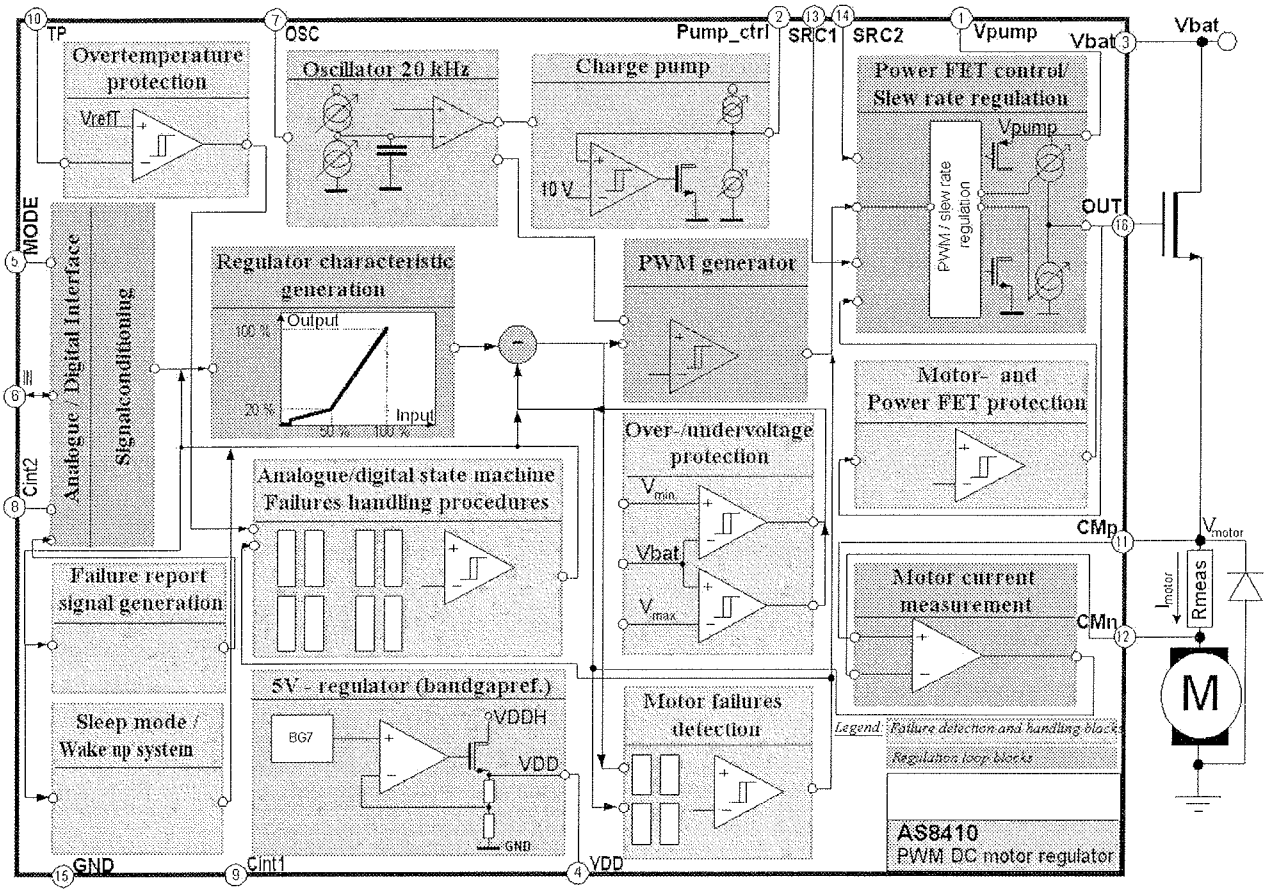


Fig. 2 Block diagram – AS8410 PWM DC Motor Regulator Circuit

Security concept

Another significant aspect in the system design of AS8410 was comprehensive failure diagnosis in the load circuitry (DC motor and power switch) and AS8410 self-controlled failure processing procedures (relieving the IC-controlling MP or IC application in systems without MPs). The AS8410 detects and treats various failure states of the power load circuit, returns a failure report signal to the set value pin, and performs an analog/digital failure processing procedure according to the type of failure.

Load circuit monitoring is performed by analog motor current measurement at the high side of the motor, and motor voltage mean measurement.

The following specified failures are diagnosed by the AS8410 in operating mode 1, and processed with analog/digital procedures by the IC itself:

1. Over current or short circuit of the motor.
2. No load of the motor (e.g. torn belt) or open wire.
3. Short-circuited power switch (power FET).
4. Mechanically blocked motor.
5. Short-circuited commutator (carbon brush clogging).
6. Protective function for the power FET and the AS8410 itself, when motor is in generator mode (during coast-down due to mechanical inertia).
7. Over or under voltage (supply voltage).
8. Over temperature.

Fig. 4 gives an example of some sequences of AS8410 internal events during an analog/digital failure processing procedure.

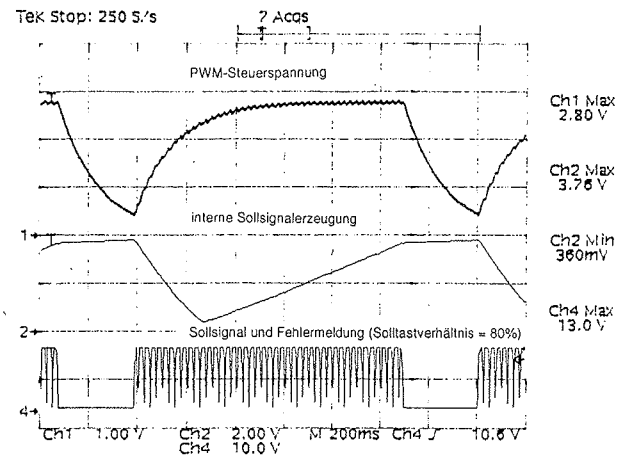


Fig. 4 Example of an AS8410 motor failure processing procedure.

The wide application range and main application properties

An additional aspect in the development of theAS8410 was its wide application scope. The following functional and parametric properties can be customized by simple programming with external devices:

1. Adapting to different DC motor power ratings is effected by programming the control currents at two analog pins. With this, control currents to the gate of the power FET-switch up to 300 mA can be delivered on chip, so that even high-performance FET's (or parallel power FET's for rated load currents in the >100A range) with effective gate source capacities of 10nF switching time down to 150 ns are possible (slew rate > 100 V/ms). Even with these short switching times, good EMC behavior is achieved by the edge-controlled drive. The short switching times allow relatively high PWM frequencies (presently 20kHz are realized) with a power efficiency of > 95 %. At the other end of the motor performance ratings, motors with rated currents in the mA range can be driven with the same properties.
2. The programming of different functional properties is realized by two additional pins (a digital pin and an analog pin):
   2.1. Set value input mode and temperature monitoring are set with the digital pin as follows:
      a) Operating mode 1: The set value (motor current or speed) is given as duty ratio of a low frequency PWM signal. The frequency of this signal is optional within a wide range (e.g. 10Hz, like the PWM output signal of many microprocessors).
      b) Operating mode 2: The set value is given as analog voltage in the range 0 - 5V at the same set value input pin.
      c) Temperature monitoring by an excess-temperature threshold, which is externally and analog programmable, with two different control modes in the case of over temperature:

      Operating mode 1 brings the motor current (motor speed) to 100 % of the rated value, if the temperature threshold is exceeded. This protects a system where dissipation is not produced by the controlled DC motor (e.g. overheated combustion engine fan-cooled by the DC motor).
      Operating mode 2 regulates the load circuitry for the system temperature not to exceed the threshold value (comparable to a thermostat). This protects a system where dissipation is produced by the controlled DC motor (or the switching transistor itself). In this case the motor output is brought down - independent from the set value - to a predefined temperature threshold value (this might even lead to a total DC motor shut-down).
      A special control was planned for cooling an overheated combustion engine (heat accumulation in a parked automobile): The DC motor regulator control is switched over from mode 1 to mode 2 with the ignition key. If the engine was overheated, the DC motor (cooling fan) starts operating in mode 2 after shut off with 100% PWM repetition rate, until the permissible temperature is reached.
   2.2. Within a wide option range, the regulator time constant can be set by the analog pin using a capacitor. A time constant in the seconds range, for example, enables soft regulating behavior, i.e. relatively slow motor speed increase or decrease toward the programmed set value.
3. In operating mode 2 the ASIC is automatically put in power-down mode through set values of < 4 % of the rated current (nominal speed). Current drawing is approx. 300 mA.

Despite its extensive programmability, the AS8410 has only 16 pins and is delivered in a standard SOIC16 package. This standard product is a successful, cost-effective bulk product.

The application circuitry in operating mode 1 and 2 is shown in Fig. 3.

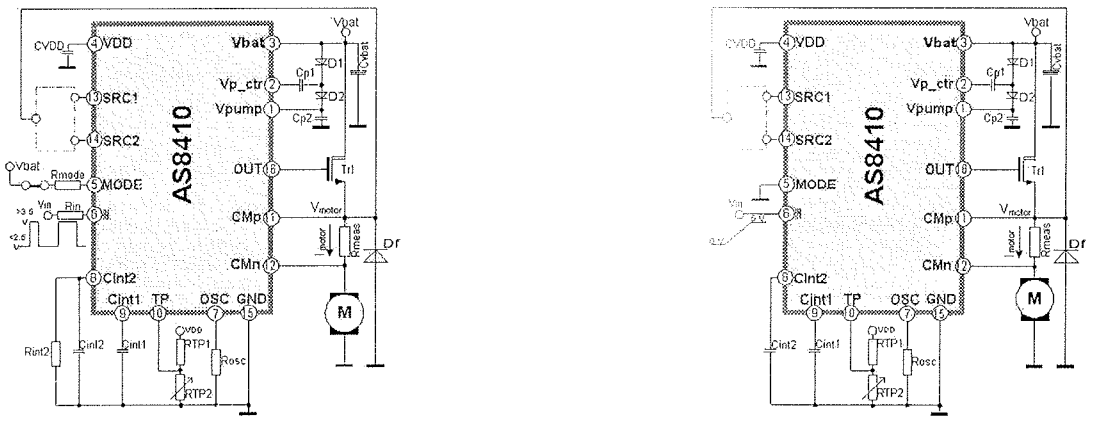


Fig. 3 Application circuits of the DC Motor regulator in operating mode 1 (left) and operating mode 2 (right)

The most remarkable property of DC motor regulator modules associated with the presented AS8410 is certainly the nearly RF emission-free (EMC complying) operation combined with high efficiency (>95 %) and relatively high PWM frequency (approx. 20kHz, which is beyond the audible range). This enables compliance with EMC regulations and application of PWM controlled DC motor regulators in electromagnetic sensitive environments (e.g. automotive field).

The low radiation susceptibility (> 300 mV) and the reliability of the control modules proved successful in their multiple automotive industry application.

The simple programmability for various rated DC motors, the entire security concept, and the operating modes have opened large application fields to the AS8410.

A glimpse of the future

The AS8410 in PWM DC motor regulators can now already be applied, wherever the described properties result in significant, cost-effective inherent utility increase, and favorable EMC behavior of DC motor-operated equipment (e.g. do-it-yourself machines, household appliances, automotive applications, variable speed and actuating drive units in automation systems, etc.). With this PWM control, DC-DC converters can also be applied (good EMC behavior).

Advance developments on the basis of the AS8410 deal with the system concept (e.g. brushless motor control, effective speed control, etc.), single system components, and motor control/regulator ICs with convenient µP interface and, on the other hand, control/regulator ICs that provide a single chip solution to the mass market of controlled DC motors.

Literature

/1/ Maurice, Bruno: *Mit dem richtigen Dreh in Schwung kommen.* Elektronik 24/1996, Pages 76 - 87

/2/ Austria Mikro Systeme International AG, CMOS-Hochvolt-Technologien

/3/ Kupris, Gerald: *Mehr als eine Vernuftehe.* Elektronik 24/2000, Pages 62 - 68

/4/ Murari, Bruno: *Verknüpfung von Leistung und Intelligenz.* Elektronik 15/1996, Pages 30 - 36

W.Marks, S.Ritz
AMS, Austria Mikro Systeme International AG
Schloss Premstaetten
A-1841 Unterpremstaetten, AUSTRIA
Tel.+43 3136 500 5449, fax.+43 3136 500 5420
Further information can also be found on Internet
web-page: www.amsint.com

Prispelo (Arrived): 03.04.2001 *Sprejeto (Accepted): 01.06.2001*

PWM LESS CURRENT CONTROL AT VSI-IM DRIVE

Žarko Čučej, Peter Cafuta, and Rajko Svečko
University of Maribor, Slovenia

Keywords: electric motors, IM, Induction Motors, FOC, Field Oriented Control, current control, PWM inverters, Pulse Width Modulated inverters, VSI, Voltage Source Inverters, VSC, Variable Structure Control, BLSC, Boundary Layer Switching Controllers, SCC, Switching Current Control, time-discrete switching variable structure control, optimized mappings

Abstract: This paper discusses time-discrete field oriented variable structure current control of induction motor - voltage source inverter system without use of a pulse-width modulator. The controller is supplemented by feedforward selection of optimized mapping of controllers into voltage source inverter states. This proposed approach of direct inverter control depends on the boundary layer control, and the sign, nominal value and maximal values of the back e.m.f. estimate. It lessens back e.m.f. influence on chattering and makes it possible to extend the field angular velocity range of constant rotor field. Boundary layer control separates variable structure control modes. Supporting preassigned switching order and control objectives is assigned to each attraction domain.

Tokovna regulacija skupka napetostno izvorni pretvornik - izmenični motor brez uporabe modulatorja

Ključne besede: motorji električni, IM motorji indukcijski, FOC krmiljenje v orientaciji polja, krmiljenje tokovno, PWM inverterji modulirani impulzno širinsko, VSI inverterji napetostno izvorni, VSC krmiljenje s strukturo spremenljivo, BLSC, krmilniki komutacijski plasti mejnih, SCC krmiljenje toka komutirajočega, krmiljenje s strukturo spremenljivo časovno-diskretno, preslikave optimirane

Povzetek: Članek obravnava časovno diskretno tokovno regulacijo s spremenljivo strukturo v poljskih koordinatah skupka asinhronski motor - napetostno izvorni pretvornik brez uporabe modulatorja. Regulator je izpopolnjen s predkrmiljenjem izbiranja optimalne preslikave stanj v stanja pretvornika. Ta predlog direktnega krmiljenja pretvornikov je odvisna od režima regulacije in predznaka, minimalne ter maksimalne inducirane napetosti v motorju. Z njo se v veliki meri kompenzira vpliv inducirane napetosti motorja na drhtenje. V primerjavi z običajnimi rešitvami omogoči tudi razširitev vrtne hitrosti pri konstantnem rotorskem polju. Pasovni regulator razmeji režime regulacije s spremenljivo strukturo. Vsakemu režimu predpiše atrakcijsko domeno, ki omogoča predpisano zaporedje preklapljanja in kriterije kvalitete regulacije.

1 Introduction

For an Induction Motor (IM) the Pulse-Width Modulation (PWM) of the Voltage Source Inverter (VSI) plays an important role in the control system, since not only the level but also the phase of input signal must be controlled. These occur as certain disadvantages of PWM inverters because they are determined by the characteristics of PWM and are not addressable by controllers /1/. These drawbacks can be eliminated by switching the variable structure (which has a direct control VSI - IM system) constructed by signals as the position, velocity, and currents, which contain information about disturbances and parameter variation, consequently the entire control system is completely accessible to control and can be optimized in a Variable Structure Control (VSC) design.

Unfortunately, time-discrete implementation of switching type VSC causes chattering, degrading all the benefits of direct switching control. In /2/,/3/ we describe chattering reduction using hysteresis controllers and in /4/ using finite automaton. The recent article /5/ proposes quasi VSC implemented with a first order deadbeat controller and a space-vector PWM. Regardless of the fact that the obtained average current error is smaller than at direct switching control, this solution has some serious limitations. Disturbances should be smooth and limited, control robustness depends on the disturbance estimator used, and PWM properties are uncontrollable.

In this paper we present the Boundary Layer Switching Controller (BLSC) used in Field Oriented Control (FOC) adapted with a feedforward steering selection for mapping of the controllers states into VSI states. Using BLSC the fixed order switching is determined, and to each of its phases mapping is optimized in regard to the following control objectives:

- sliding mode reaching time,
- average current error offset,
- chattering,
- VSI switching losses.

Mapping optimization compared to /6/ involves zero voltage vectors. This introduced feedforward selection is similar to predictive current control /7/, except that: (i) the control is still VSC, and (ii) instead of back e.m.f., only information about the field velocity sign, and minimal and maximal values of back e.m.f. estimates are used.

This work was supported in part by the Slovene Research Ministry under Grant J2-1644-0796-99.

This article is organized as follows. Problem presentation with description of VSI, IM model and a summary of VSC is contained in section 2. In section 3 the proposed control with compensation of back e.m.f., feedforward steering and design of ST is given. Results of simulations are collected in section 4. This article ends with conclusions and appendices containing derivation of zero dynamics, IM model and analysis of stability for use of zero voltages.

2. Problem presentation

IM is feed by a 3-leg bridge VSI supplied by DC voltage *E* and direct controlled by current switching controllers in the inner loop of FOC. VSI has eight states, which determine six active voltage vectors $\boldsymbol{u}_k, k = 1,\ldots 6$ with constant amplitude $u_k = 2E/3$ and two zero voltage vectors $\boldsymbol{u}_k \in \{\boldsymbol{u}_0, \boldsymbol{u}_7\}$ (Fig. 1).

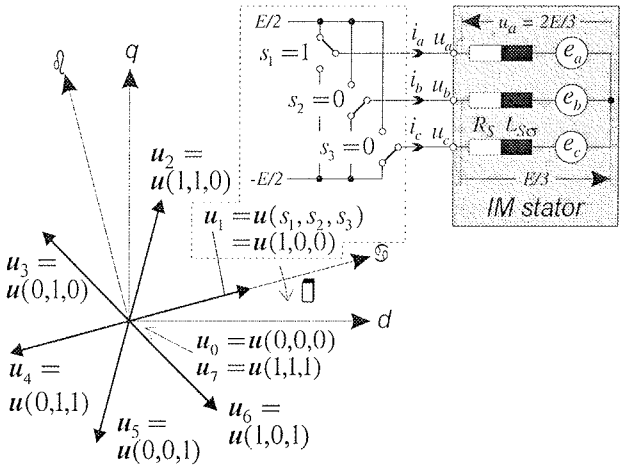


Fig. 1: Voltage vector representation from the d-q frame perspective, inverter, and load circuit.

A symmetrical, 3-phase IM with Y stator windings with a galvanic isolated central tap is considered. Its voltage model in *d-q* frame is described by the following MIMO system:

$$u_\Diamond = Ri_S + L_{S\sigma} p i_{S\Diamond} + e_\Diamond \,, \Diamond \in \{d, q\}, \qquad (1)$$

where $\boldsymbol{u} = [d\ q]^T$ is stator voltage vector, R_S and $L_{S\Diamond}$ are rotor resistance and rotor leakage inductance respectively, $e_\Diamond$ is sum of back e.m.f. and crosscoupled voltages ($e_d = e_{dq} + e_{di}$, $e_q = e_{qd} + e_{qi}$), and $pi = di/dt$. Latter, in the design we use a simple modified model:

$$L_{S\sigma} p i_{S\Diamond} = u_{k\Diamond} - e_\Diamond \,, \qquad (2)$$

which is derived in Appendix C.

2.1 FOC

We assumed that FOC has a multi-loop structure and is sampled every T_S seconds, i.e. algorithms are implementable in the digital signal processor. Outer loops contain state controllers and estimators for the load torque T_L, rotor magnetization current i_{mR}, and angle ϑ. They are responsible for the tracking of drive kinematics variables and the regulation of i_{mR}. Field weakening is not considered. The selection of design coefficients c_1, c_2, and c_3 (elaborated in Appendix A and Appendix B) of outer control loops should guarantee stable *zero dynamics* with a stationary point: $\tilde{\varphi} = \dot{\tilde{\varphi}} = \psi_R = 0$ and $\dot{\tilde{\varphi}} = \ddot{\tilde{\varphi}} = \dot{\psi}_R = 0$. Outputs from outer loops i_{Sq}^{REF} and i_{Sd}^{REF} serve as command values for inner current control loops.

2.2 Current variable structure control

The control problem being considered is a determination of sequence and the duration of VSI states, so that by tracking i_{Sq}^{REF} and i_{Sd}^{REF} the drive FOC is satisfied:

$$\boldsymbol{s} = \left[s_d\ s_q\right]^T = \boldsymbol{i}_S^{REF} - \boldsymbol{i}_S = 0 \,, \qquad (3)$$

i.e. VSC is established in stator currents error space $\square^2$ where $s_\Diamond = 0$, $\Diamond \in d, q$ are switching subspaces. This formulation embraces the control of stator currents and modulation of VSI outputs as one problem, which is solved by a MIMO VSC.

It is well known /9/, /10/, that the design of VSC can be done by satisfying a reaching condition. In FOC the torque and magnetization control are decoupled, meaning that the MIMO current control is designed by two independent controllers, which fulfill reaching conditions written in compact form as:

$$S_D : \dot{s}_d s_d < 0 \qquad (4a)$$

$$S_Q : \dot{s}_q s_q < 0 \qquad (4b)$$

$$S_0 : S_D \cap S_Q \qquad (4c)$$

by discontinuous control:

$$v_\Diamond = \begin{cases} v_\Diamond^- & \text{if } s_\Diamond > 0 \\ v_\Diamond^+ & \text{if } s_\Diamond < 0 \end{cases} \qquad (5)$$

with discontinuity on the switching subspaces S_i. The set of control vectors $\boldsymbol{v} = \left[v_d\ v_q\right]^T \in \boldsymbol{v}_j$, $j = 1,\ldots 4$ is present-

ed in Fig. 2a. Control (5) ensuring (in ideal circumstances, when switching frequency is infinite) or sliding on S_D with reaching to S_0, or sliding on S_Q with reaching to S_D either sliding on S_0. Only in the last case is the request (1) completely satisfied.

The PWM's less mapping between control vector ***v*** and stator voltage vector ***u*** gives IM stator voltage equation (2). Combining (4a), (4b) and (1) gives:

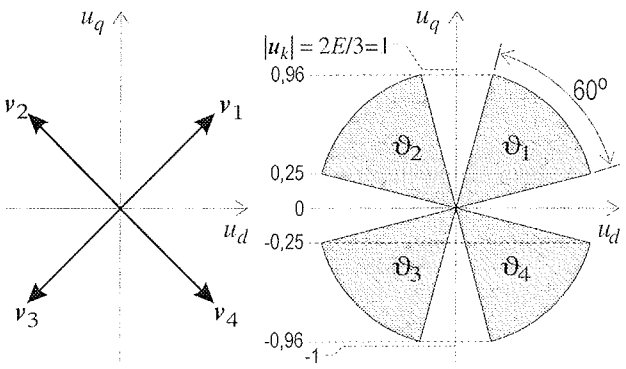


Fig 2: Presentation of control vectors (a) and mapping range (b).

$$\left[\frac{1}{L_{S\sigma}}\left(u_{k\Diamond}-e_{\Diamond}\right)\right]s_{\Diamond}<0\rightarrow\begin{matrix}s_{\Diamond}<0\,,\,u_{k\Diamond}>e_{\Diamond}\\ s_{\Diamond}>0\,,\,u_{k\Diamond}<e_{\Diamond}\end{matrix}\qquad(6)$$

If VSC, for control robustness is designed at $\max|e_{\Diamond}|$, for mapping $v\rightarrow u$ from (6) it follows:

$$v_{\Diamond}=u_{k\Diamond}(\rho)=\begin{cases}v_{\Diamond}^{-} & \text{when}\quad u_{k\Diamond}<-\max|e_{\Diamond}|\\ v_{\Diamond}^{+} & \text{when}\quad u_{k\Diamond}>\max|e_{\Diamond}|\end{cases}\qquad(7)$$

Due to the rotation of the active voltage vectors and their angular displacement at 60^0, the mapping $v\rightarrow u$ links control vectors $\{v_j\}$ with four angular sectors $\{\vartheta_j\}$ in *d-q* frame containing voltage vectors $\{u_k\}$ involved in mapping.

The sectors placements depend on terms $e_{\Diamond}$ (or $d_{\Diamond}$, see (31) in Appendix C), but in the case of (7) only on their maximal amplitude. Therefore angle sectors are placed symmetrically as are the symmetrical control vectors v_j (Fig. 2b).

2.3 Implementation of decoupled switching current control

This described current control is named decoupled Switching Current Control (SCC). It is of simple structure (Fig. 3) and can be simply implemented using digital signal processors. ST performs mapping where selection of columns addressed by ρ quantizer performs an inverse transformation from *d-q* to *abc* space.

Time discrete implementation of the decoupled SCC causes inverter outputs to have a finite pulse such as pulse width modulation. Their duration is equal to one sample interval and occasionally to an integer multiple of T_s. Therefore the decoupled SCC is never in SM. Consequently difference in control vector amplitudes, i.e. $|\overline{v_{\Diamond}^{-}}|-|\overline{v_{\Diamond}^{+}}|=|\overline{e_{\Diamond}}|$ cause offset in $|\overline{e_{\Diamond}}|$ and subharmonic oscillation (in regard to frequency $1/T_s$) of local average of $|\overline{e_{\Diamond}}|$ (determined by stator time constant) causing torque chattering.

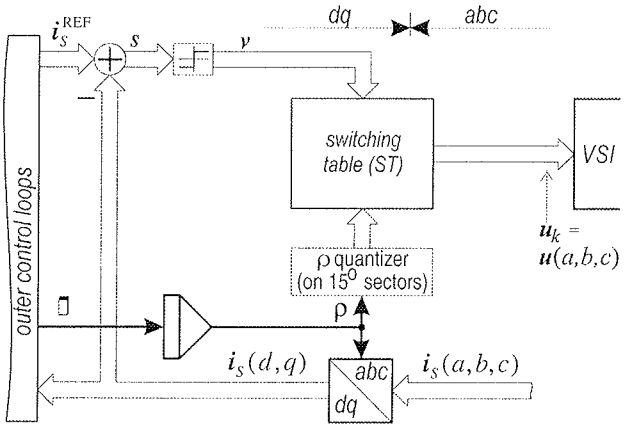


Fig. 3: Realization of decoupled SCC.

The other important drawbacks of mapping (7) are: (i) zero vector voltages are uninvolved, and (ii) for components of the selected voltage vector the following holds

$$\max|u_d|=\max|u_q|\quad\text{and}\quad\min|u_d|=\min|u_q|,\qquad(8)$$

which limits the velocity range of nominal magnetization to:

$$\max e_{\Diamond}\le 0{,}25\left(2E/3\right)\qquad(9)$$

Absence of zero voltages cause high total switching frequency of VSI (at least twice that of $1/T_s$), consequently VSI switching losses are very high.

3 Proposed switching current control

Decoupled SCC performances are well enhanced with Fixed-order sliding mode switching scheme /10/, where the sliding mode takes its place in a preassigned order while state is traversing the state space:

- moving along S_D only in initialization phase during the establishment of nominal rotor magnetization;
- in regular control it mode moves in order

$$S_Q \rightarrow S_0 \tag{10}$$

and then maintaining limit cycle around S_0. Mappings supporting (10), should adopt attraction to VSC modes. For S_Q the minimal S_0 reaching time is requested, after reaching S_0 it is desirable to maintain the limit cycle around ***s***-origin so, that the current ripple is redirected from torque into magnetization control (where it is well dumped by large rotor lag) and in VSI switching sequences the minimal number of switches is involved. This is achieved by deliberate use of zero voltage vectors in mapping.

3.1 Boundary Layer Switching Control

The fixed-order sliding mode switching scheme is made possible by the Boundary Layer Switching Control (BLSC), which separates the associated VSC modes. According to above description it has to differentiate between three VSC modes:

- mode of moving along S_Q
- mode of limit cycle at S_0, which has two phases:
  - phase of obeying (4b).
  - phase of obeying (4c).

These modes besides the mapping range presented in Fig. 2b, which accommodates attraction domain A_{DQ}, need two further domains:

- domain A_0 belonging S_0, where v_q^-, v_d^+ are mapped into ***u*** with minimal amplitudes of u_{kq} fulfilling (6), and v_d^-, v_d^+ into ***u*** with maximal amplitudes of u_{kq},
- domain A_Q belonging S_Q where mapping requests are opposite to requests for domain A_0.

BLSC, which fulfills the above requirements, has three layers of coaxial arrangement with a center in ***s***-plane origin (Fig. 4).

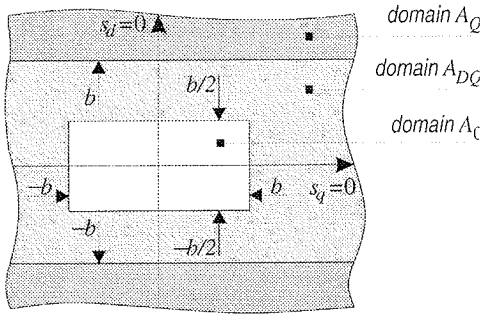


Fig. 4: Borders and discrete VSC modes.

The borders between attraction domains are determined by the current error caused by maximal voltage amplitude, which arises in a stationary condition in one sampling interval. Using the estimation of $\dot{s}_q$ with difference $\Delta s_q / T_s$ for border between A_Q and A_{DQ} we can state:

$$|b| = \frac{\|\boldsymbol{u}\|}{L_{S\sigma}} T_s \,. \tag{11}$$

For inner border (between A_{DQ} and A_0) we consider in (11) maximal allowed back e.m.f.. Because

$$\frac{\|\boldsymbol{u}\|}{\max|e_q|} \geq 2 \tag{12}$$

it follows, that in *q* direction the inner border is $b/2$. Boundaries in *d* direction we settled to $\pm b$. This choice is based on a consideration that in the limit cycle around the error plane origin ($s = 0$) a sequence of voltage vectors could be formed, where zero voltage vectors follow each active vector. In this case the border in *d* direction should be at least so far from the origin of ***s***-plane that s_d, i.e. current error in *d* direction can be zeroed by $\max|u_d|$. Thus borders in *d* direction should be calculated similarly to borders in *q* direction, i.e. by (11) with consideration for adequate voltages in *d* direction. Because $\max|u_d| = \max|u_q|$ and $\max|e_d| \leq \max|e_q|$ we justify aforementioned choice of $\pm b$ for *d* direction.

Note, the boundaries are tied to the sampling interval T_S, and their size actually determines the duration of sampling interval. In many IM control designs, the value of the sampling interval T_S is influenced more by desired rotor field angular accuracy, the rms value of stator current chattering, and inverter volume power density than by IM dynamic requests. One of this project's goals was to make the sampling interval as short as possible in regard to the limitations of the used digital signal processor. The target value was 25 μs.

3.2 Compensation of e_q

Use of zero voltage vectors $\boldsymbol{u}_0, \boldsymbol{u}_7$ in mapping during limit cycle reduces offset and chatter of $s_\Diamond$ local average (in interval determined by the motor's time constants respectively), but for dump these phenomena, $e_\Diamond$ should be compensated.

Due to switching controllers they cannot be compensated by subtraction of $e_\Diamond$ as is done for predictive controllers /

/7/. Rather, the slowly-occurring magnetization offset (caused by e_d) is minimized by rotor magnetization control (see Appendix B), and oscillation of local average of s_q causing torque chattering, is effectively minimized by mapping with property

$$\overline{|v_q^+|} = \overline{|v_q^-|} \,. \tag{13}$$

From (7) at $e_q > 0$ follows $v_q^- = u_q^- + e_q$ and $v_q^+ = u_q^- - e_q$ where u_q^-, u_q^+ denotes voltages to which v_q^- and v_q^+ are mapped, consequently the above equation can only be fulfilled if at least the sign, min and max of e_q is known. By rough linearization of $u_q = \|\boldsymbol{u}\| \sin\rho$, considering $e_q > 0$ and limit $\min\left(v_q^+\right) = \max\left(e_q\right)$, after a short calculation we obtain:

$$\min\left|u_q^-\right| = -\min\left|e_q\right| \,. \tag{14}$$

This suboptimal solution enables a simple construction of the angular sectors distributions. Moreover, exact calculation in the case of $\min\left(e_q\right)$ is by (7) limited to (14).

Mapping, considering (13) and (14) and the preassigned switching order is then:

$$u_{kd}(\rho) - e_d \rightarrow \begin{cases} v_d^- & \text{when} \quad s_d > 0 \\ v_d^+ & \text{when} \quad s_d < 0 \end{cases} \tag{15a}$$

$$u_{kq}(\rho) - e_q \rightarrow \begin{cases} v_q^- & \text{when} \quad u_{kq} > -\min\left|e_q\right| \\ v_q^+ & \text{when} \quad u_{kq} < \max\left|e_q\right| \end{cases} \tag{15b}$$

$$u_{kq}(\rho) + e_q \rightarrow \begin{cases} v_q^- & \text{when} \quad u_{kq} < \min\left|e_q\right| \\ v_q^+ & \text{when} \quad u_{kq} > -\max\left|e_q\right| \end{cases} \tag{15c}$$

where (15b) and (15c) are valid for positive and negative e_q respectively.

The position of angular sectors θ_j, containing vectors $\boldsymbol{u}_k$ is determined by the geometric relationship between $|u_q|$ and $|\boldsymbol{u}(\rho)|$ at ρ_{jB} and ρ_{jE}, where angles ρ_{jB} and ρ_{jE} denote the beginning and end of angular sector ϑ_j (Fig.5). At $\rho > 0$ for odd sectors ρ_{1B} and ρ_{1E} can be generally written as:

$$\sin\rho_{1B} \geq \frac{\min e_q}{\|\boldsymbol{u}\|} \quad , \quad \sin\rho_{3B} \geq \frac{\min e_q}{\|\boldsymbol{u}\|} \,. \tag{16}$$

Sector ϑ_1 is placed in $\rho_{1B} \leq \rho \leq \rho_{1B} + \frac{\pi}{3}$ and similarly for sector ϑ_3 hold $\rho_{3B} \leq \rho \leq \rho_{3B} + \frac{\pi}{3}$. When hold $\dot{\rho} < 0$, then we obtain:

$$\sin\rho_{1B} \geq \frac{\min e_q}{\|\boldsymbol{u}\|} \quad , \quad \sin\rho_{3B} \leq \frac{\min e_q}{\|\boldsymbol{u}\|} \,. \tag{17}$$

The position of even sectors ϑ_2 and ϑ_4 are symmetrically over q-axe to position of ϑ_1 and ϑ_2 respectively.

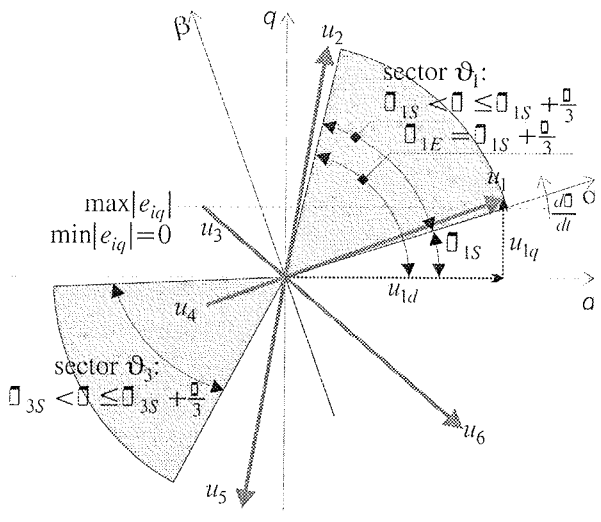
Zero voltage vectors take place in A_0 domain only and their selections is independent of field angle ρ. They are applied according to:

$$\begin{aligned} &\texttt{if } \boldsymbol{u}\left[(n-1)\mathrm{T_s}\right] = \boldsymbol{u}_7 \vee \boldsymbol{u}_2 \vee \boldsymbol{u}_4 \vee \boldsymbol{u}_6 \\ &\quad \texttt{then } \boldsymbol{u}\left(n\mathrm{T_s}\right) = \boldsymbol{u}_7 \\ &\quad \texttt{else } \boldsymbol{u}\left(n\mathrm{T_s}\right) = \boldsymbol{u}_0 \end{aligned} \tag{18}$$

where nT_S is the sampling instant. This selection gives minimal VSI over-switching at the voltage vectors change [2]. As this is excellent for VSI and enables good compensation of e_q, it should be noted that at zero vector voltage the IM is effectively allowed to coast. Control seems to be lost during this time, but stability is still preserved because besides conditions (33) and (10) the following condition

$$\operatorname{sign} s_q = \operatorname{sign} e_q \tag{19}$$

is also fulfilled (see stability analysis in Appendix D).



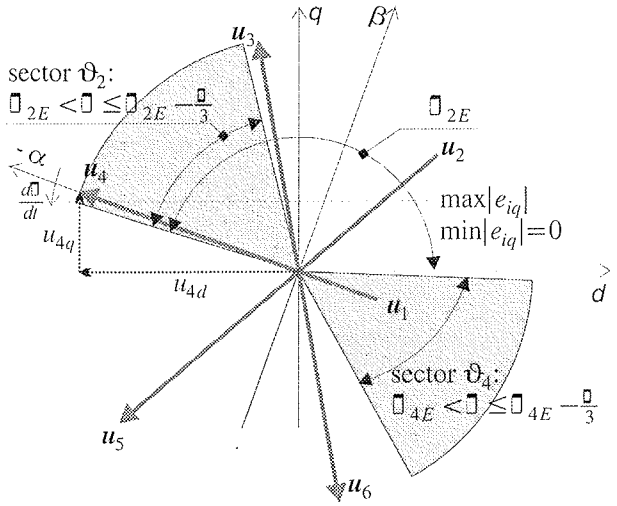


Fig. 5: Determination of ρ_{jB} and ρ_{jE} in nominal field angular velocity range.

3.3 Implementation of proposed current control

The structure of the proposed current switching control is shown in Fig. 6. BLSC is implemented by a 2-dimensional 4-level quantizer separating the attractors domains A_0, A_{DQ} and A_Q. Switching table ST is result of logic superposition of angular sectors determined in subsections 3.1 and 3.2 respectively. Feedforwarded $\dot{\rho}$ is quantized by a four-level quantizer. It determines max and min value of back e.m.f. (because $e_q = e_{iq} + e_{dq}$, whereas constant field is proportional to $\dot{\rho}$ and e_{dq} varies according to $\dot{\rho}$ and fast i_{Sd}, it is simple to evaluate $\max e_q$ and $\min e_q$ for positive and negative angular velocity range of $\dot{\rho}$). In the case, where distinguishing between A_{DQ} and A_Q domains is less important than maximal $\dot{\rho}$ with constant rotor field, the voltage range for A_Q can be exploited in A_{DQ} domain. This in comparison to decoupled SCC enables to doubling of the $\dot{\rho}$ range of the constant rotor field, Table 1.

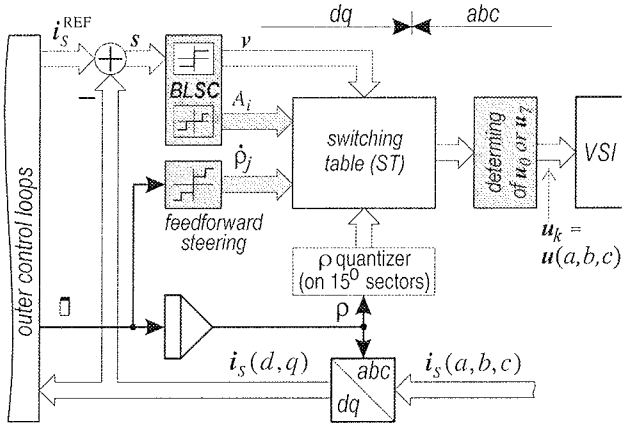


Fig. 6: Proposed control with mapping and feedforward steering.

Table 1: Pairs $\max e_q$ - $\min e_q$ in nominal and extended velocity ranges. $\dot{\rho}_{SCC}$ is maximal $\dot{\rho}$ range of SCC.

velocity range	$\max e_q$	$\min e_q$
$\dot{\rho}_{SCC} \geq \rho \geq 0$	0,25(2E/3)	0
$0 \geq \rho \geq -\dot{\rho}_{SCC}$	0	– 0,25(2E/3)
$2\dot{\rho}_{SCC} \geq \rho \geq \dot{\rho}_{SCC}$	0,5(2E/3)	0,25(2E/3)
$-\dot{\rho}_{SCC} \geq \rho \geq -2\dot{\rho}_{SCC}$	-0,25(2E/3)	– 0,5(2E/3)

ST consists of 9 subtables, see Table 2. They are addressed by attractors domains A_i and angular velocity range ρ_j. The rows in the subtable are determined by the signum functions of BLSC. Columns are addressed by ρ quantizer determining 24 angular quants θ_c. The inverse transformation from *d-q* to *abc* frame is the domain of columns. Determination of zero voltage vectors according to (18) follows ST.

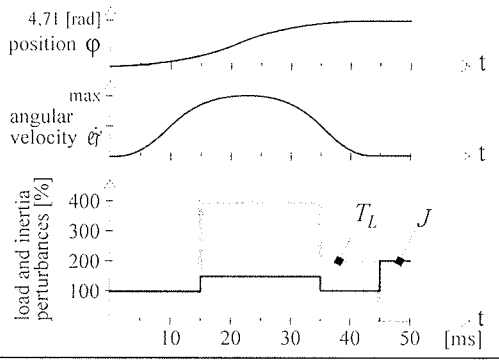
Table 2: Switching table (ST). The VSI switches states are denoted by the corresponding voltage vectors.

	θ_1 : $0 \geq \rho \geq -\frac{\pi}{12}$											
v	$\cdots$	$\theta_{2'}$	θ_1	θ_2	θ_3	θ_4	θ_5	θ_6	θ_7	θ_8	θ_9	$\cdots$
	subtable #1: A_{DQ} ; $\dot{\rho}_{SCC} > \dot{\rho} > -\dot{\rho}_{SCC}$											
v_1	$\cdots$	u_5	u_5	u_5	u_5	u_6	u_6	u_6	u_6	u_1	u_1	$\cdots$
v_2	$\cdots$	u_6	u_6	u_1	u_1	u_1	u_1	u_2	u_2	u_2	u_2	$\cdots$
v_3	$\cdots$	u_2	u_2	u_2	u_2	u_3	u_3	u_3	u_3	u_4	u_4	$\cdots$
v_4	$\cdots$	u_3	u_3	u_4	u_4	u_4	u_4	u_5	u_5	u_5	u_5	$\cdots$
	subtable #2: A_Q ; $\dot{\rho}_{SCC} > \dot{\rho} > 0$											
v_1	$\cdots$	u_3	u_4	u_4	u_4	u_4	u_5	u_5	u_5	u_5	u_6	$\cdots$
v_2	$\cdots$	u_6	u_1	u_1	u_1	u_1	u_2	u_2	u_2	u_2	u_3	$\cdots$
v_3	$\cdots$	u_2	u_2	u_2	u_3	u_3	u_3	u_3	u_4	u_4	u_4	$\cdots$
v_4	$\cdots$	u_3	u_3	u_3	u_4	u_4	u_4	u_4	u_5	u_5	u_5	$\cdots$
	subtable #3: A_Q ; $0 > \dot{\rho} > -\dot{\rho}_{SCC}$											
v_1	$\cdots$	u_5	u_5	u_5	u_6	u_6	u_6	u_6	u_1	u_1	u_1	$\cdots$
v_2	$\cdots$	u_6	u_6	u_6	u_1	u_1	u_1	u_1	u_2	u_2	u_2	$\cdots$
v_3	$\cdots$	u_1	u_2	u_2	u_2	u_2	u_3	u_3	u_3	u_3	u_4	$\cdots$
v_4	$\cdots$	u_3	u_4	u_4	u_4	u_4	u_5	u_5	u_5	u_5	u_6	$\cdots$
	subtable #4: A_0 ; $\dot{\rho}_{SCC} > \dot{\rho} > 0$											
v_1	$\cdots$	u_5	u_5	u_5	u_6	u_6	u_6	u_6	u_1	u_1	u_1	$\cdots$
v_2	$\cdots$	u_6	u_6	u_6	u_1	u_1	u_1	u_1	u_2	u_2	u_2	$\cdots$
v_3, v_4	zero voltage vectors, determined by (18)											
	subtable #5: A_0 ; $0 > \dot{\rho} > -\dot{\rho}_{SCC}$											
v_1, v_2	zero voltage vectors, determined by (18)											
v_3	$\cdots$	u_1	u_2	u_2	u_2	u_2	u_3	u_3	u_3	u_3	u_4	$\cdots$
v_4	$\cdots$	u_3	u_4	u_4	u_4	u_4	u_5	u_5	u_5	u_5	u_6	$\cdots$
	subtable #6: A_{DQ} , A_Q ; $\dot{\rho} > \dot{\rho}_{SCC}$											
v_1	$\cdots$	u_3	u_4	u_4	u_4	u_4	u_5	u_5	u_5	u_5	u_6	$\cdots$
v_2	$\cdots$	u_6	u_1	u_1	u_1	u_1	u_2	u_2	u_2	u_2	u_3	$\cdots$
v_3	$\cdots$	u_2	u_2	u_2	u_3	u_3	u_3	u_3	u_4	u_4	u_4	$\cdots$
v_4	$\cdots$	u_3	u_3	u_3	u_4	u_4	u_4	u_4	u_5	u_5	u_5	$\cdots$
	subtable #7: A_{DQ} , A_Q ; $-\dot{\rho}_{SCC} > \dot{\rho}$											
v_1	$\cdots$	u_5	u_5	u_5	u_6	u_6	u_6	u_6	u_1	u_1	u_1	$\cdots$
v_2	$\cdots$	u_6	u_6	u_6	u_1	u_1	u_1	u_1	u_2	u_2	u_2	$\cdots$
v_3	$\cdots$	u_1	u_2	u_2	u_2	u_2	u_3	u_3	u_3	u_3	u_4	$\cdots$
v_4	$\cdots$	u_3	u_4	u_4	u_4	u_4	u_5	u_5	u_5	u_5	u_6	$\cdots$
	subtable #8: A_0 ; $\dot{\rho} > \dot{\rho}_{SCC}$											
v_1	$\cdots$	u_3	u_4	u_4	u_4	u_4	u_5	u_5	u_5	u_5	u_6	$\cdots$
v_2	$\cdots$	u_6	u_1	u_1	u_1	u_1	u_2	u_2	u_2	u_2	u_3	$\cdots$
v_3, v_4	zero voltage vectors, determined by (18)											
	subtable #9: A_0 ; $-\dot{\rho}_{SCC} > \dot{\rho}$											
v_1, v_2	zero voltage vectors, determined by (18)											
v_3	$\cdots$	u_1	u_2	u_2	u_2	u_2	u_3	u_3	u_3	u_3	u_4	$\cdots$
v_4	$\cdots$	u_3	u_4	u_4	u_4	u_4	u_5	u_5	u_5	u_5	u_6	$\cdots$

4. Simulation

A property of the proposed control with feedforward steering of optimized mappings has been evaluated by simulation. Data for IM, VSI, controllers, and perturbed tracking task considered in simulations are collected in Table 3.

Table 3: Motor, inverter, controllers, and task data.

Motor:	four pole, 1480 rpm, Y connected stator windings with isolated central tap		
Parameters:	$R_S = 0,65\,\Omega$	$L_S = 1,65$ mH	$T_e = 4$ Nm
	$\tau_R = 0,12$ s	$J = 0,000656$ kgm^2	
Inverter:	3-phase bridge, supply voltage $E = 310$		
Control:		SCC	proposed
	BLSC border: b	-	3 A
	magnetization reference i_{mR}^{REF}	4,75 A	4,75 A
Kinematics:	$c_1 = 70000$, $c_2 = 1000$, $c_3 = 100$		
Perturbed tracking task:			

The chosen task enables testing of the proposed mapping in all VSC modes. Simulation starts by initialization, where the nominal rotor magnetic field is established, then A_Q and A_{DQ} follow, which are disturbed in 15^{th} milliseconds with a change of the load torque. It pushes VSC into RM. The perturbation of the inertia J is used for evaluation of the robustness against IM parameter variation.

To show the properties of the proposed mapping, a comparison to SCC (characterized by Fig. 2b and presented in Fig. 3) has been made. The significant simulation results are collected in Table 4, and shown in Fig. 7.

From these results it follows that the proposed mapping with optimized voltage patterns has several advantages in comparison to SCC:

- the number of switches involved in voltage vector switch-over and the number of voltage vector changes are reduced by 60 % and 40 % respectively,
- chattering of i_{sq} is reduced by 40 %,
- reduction of $(i_S)_{rms}$ 1,73 % slightly reduces motor losses,
- the angular velocity range of the constant rotor field is doubled,
- tracking of kinematics variable is slightly improved.

Table 4: Simulation results.

parameter		SCC	proposed
$\max(i_{Sq}) - \min(i_{Sq})$	[A]	20,26	10,83
$\overline{i_{Sq}}$	[A]	12,51	12,62
$(i_{Sq})_{rms}$	[A]	13,39	12,97
$\overline{\max(i_{Sq}) - \min(i_{Sq})}\Big/\overline{i_{Sq}}$		1,62	0,87
$\max(i_{Sd}) - \min(i_{Sd})$	[A]	4,92	5,96
$\overline{i_{Sq}}$	[A]	0,93	0,57
$(i_{Sq})_{rms}$	[A]	1,98	2,17
$(i_S)_{rms}$	[A]	13,39	13,15
u changes frequency	[Hz]	19800	11400
total switch-over freq.	[Hz]	48200	18800
end position error $\Delta\varphi$	[rad]	-0,087	-0,066

The complexity of the algorithms and the target sampling interval was tested by implementation of algorithms on the floating point digital signal processor AT\&T C32 using a 40 MHz clock. The following results were achieved:

- the boundary layer controller with feedforward steering needs about 4 μs, and
- the measurement of i_{Sd} and i_{Sq}, and the calculation of ρ need about 14 μs.

From the above it can be concluded that the sampling interval of $T_s = 25\,\mu s$ at IM servo-drive system with proposed current control can be easily achieved.

5. Conclusion

The presented PWM less switched field oriented control with feedforward selection of subtable with optimized mapping has been investigated analytically and evaluated by simulations. The obtained results show that the proposed switching current control significantly reduces the drawbacks of decoupled SCC, i.e. chattering, offsets and inverter switching losses. The achieved improvements are based on the deliberate use of the reaching condition resulting in of preassigned switching order, time scale sepa-

reference solution:
de-coupled SCC
from Fig. 3

proposed solution

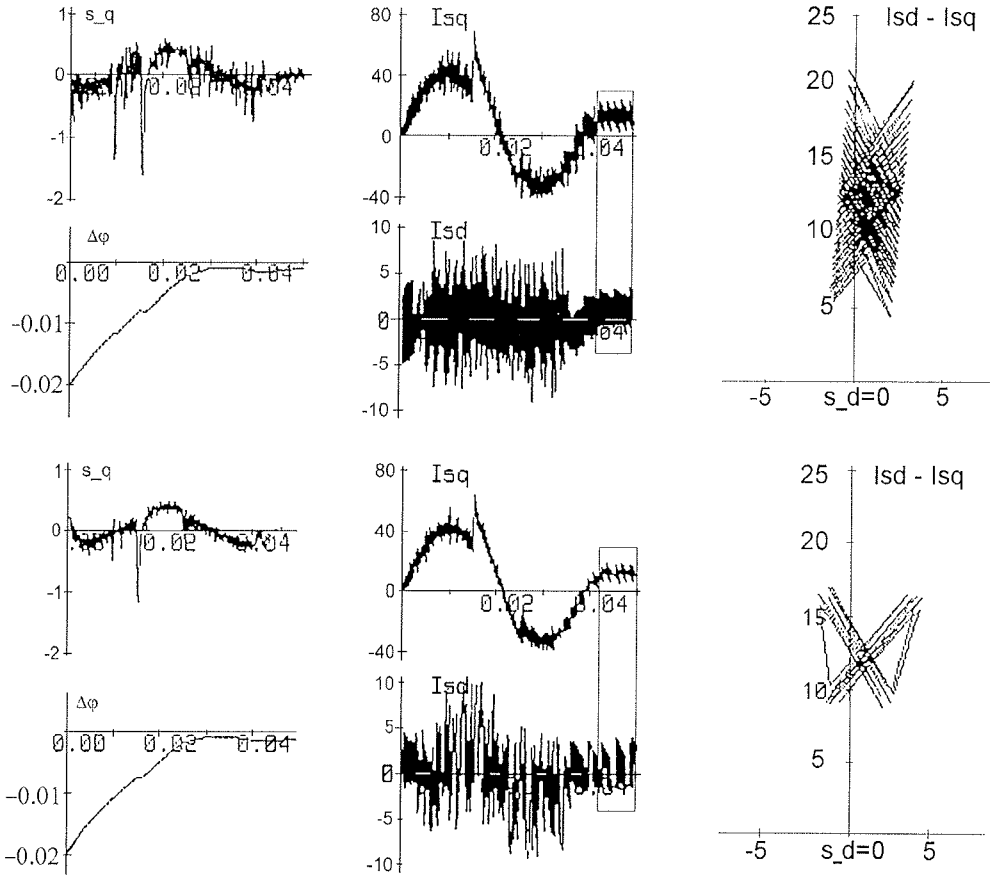


Fig. 7. Tracking the disturbed task simulation results for SCC (top), and BLSC (bottom). $T_s = 25\,\mu s$, [A] $\Delta\varphi = \varphi^{REF} - \varphi$ [rad], s_d and s_q are s_d and s_q respectively. Trajectories of i_S are at $\varphi = 4,75$ [rad] at the indicated 5 ms intervals.

ration of FOC and the use of feedforwarded $\dot{\rho}$ Using these measures, more current ripples are directed into magnetization (where it is well dampened by rotor lag) than to torque generation.

Preassigned switching order also enables the employment of zero-voltage vectors. Their use reduces deviation of the **s** local average at S_0, thus reducing the chattering, as well as the total inverter switching frequency. With feedforwarding $\dot{\rho}$ becomes possible the compensation for deviation of the local average s_q at active voltage vectors and also it enables extension of $\dot{\rho}$ with nominal rotor field.

Finally, it is worth mentioning that despite to all refinements, current control still has a relatively simple structure, which can be efficiently implemented in digital signal processors. The proposed VSC with voltage mapping is also implementable in all symmetric 3-phase motor types.

Biblography

/1/ F. Hashimoto, H. Yamamoto, S. Yaganisava: Brushless servomotor control using variable structure approach. *IEEE tarns. IA.*, vol IA24, pp 160–170, 1988

/2/ Ž. Čučej, P. Cafuta: Current controllrd pulse-width modulations for output voltage of inverters feeding AC motors, part 3: sliding mode control. *Elektrotechnical review*, ISSN 0013-5852 Vol. 66, No. 1, pp. 58–66, 1999

/3/ Ž. Čučej, P. Cafuta: *Optimization of the supply voltage pattern in the sliding mode controlled induction motor drive.* ISIE'99 Bled Slovenia, Proceeding Vol. 1, pp. 7–13, 1999

/4/ P. Cafuta: *Determination of inverter switching by intermodulation: sliding mode controlled IM drive*. Invited presentation on University Johanes Kepler, Linz, Avstrija, 1999

/5/ W.C. Su, S.V. Drakunov, Ü. Özzgüner: An $O(T^2)$ Bounary Layer in Sliding Mode for Sampled data System. *IEEE Trans. on Automatic Control*, Vol. 45. No. 3. pp. 482–485, 2000

/6/ N. Šabanović-Behlilović, A. Šabanović, T. Ninomiya, *PWM in three-phase switching conwerters - sliding mode soluton.* Conference PESC'94, Taipeh, Proceedings, pp. 560–565, 1994.

/7/ J. Holtz, S. Stadtfeld, Pulsewidth modulation for electric power conversion. *Proceedings of IEEE*, Vol. 82, No. 8. pp. 1194–1214, 1994.

/8/ W. Leonhard, 30 years space vectors, 20 years field orientation, 10 years digital signal processing with controled AC drives. *EPE Journal*, Vol. 1 and Vol. 2, 1991.

/9/ V.I. Utkin, Sliding mode control design principle and applications to electric drives. *IEEE Trans. on Ind. Electronics*, Vol. 40, No. 1, pp. 23–35, 1993.

/10/ W. Gao, J. C. Hung, Variable structure control of nonlinear systems: a new approach. *IEEE Trans. on Ind. App.*, Vol. 40, No. 1, pp. 45–55, 1993.

/11/ C. Rossi, A. Tonielli, Robust current controller for three-phase inverter using finite-state automaton. *IEEE Trans. on Ind. Electronics*, Vol. 42, No. 2, pp. 169–178, 1995.

Appendices

A. Kinematic tracking

The drive dynamics is described with

$$J\dot{\omega} = T_e - T_L, \tag{20}$$

where $\omega = \dot{\varphi}$ is rotor angular velocity and *J* is drive inertia constant or variable as load torque T_L. By tracking, kinematics' variables $\dot{\varphi}^{REF}$ (speed) and φ^{REF} (rotor position) are prescribed functions. IM delivers electrical torque decoupled from magnetization by FOC:

$$T_e = \frac{2}{3}\frac{P}{2}\frac{L_m}{L_S L_R} i_{mR} i_{Sq} = k_m i_{Sq}, \tag{21}$$

where *P* is number of the machine poles, L_m, L_R and L_S are mutual, rotor and stator inductances respectively, i_{mR} present rotor magnetization current /8/. The rotor field angle:

$$\rho = \int \dot{\rho}\, dt = \int \left\{ P\omega + \frac{2}{P}\frac{i_{Sq}}{i_{mR}} \right\} dt \tag{22}$$

is determined according to the rotor lag τ_R. If an error of position, angular speed and acceleration forms a linear combination, then the control task can be determined as:

$$c_1 e + c_2 \dot{e} + \ddot{e} = 0 \tag{23}$$

where $e = \varphi - \varphi^{REF}$, $\dot{e} = \dot{\varphi} - \dot{\varphi}^{REF}$ and $\ddot{e} = \ddot{\varphi} - \ddot{\varphi}^{REF}$ are the position, angular speed and acceleration error respectively, and c_1 and c_2 are positive constants. From (23) follows

$$\ddot{e} = \ddot{\varphi}^{REF} - \ddot{\varphi} = c_1 e - c_2 \dot{e} \tag{24}$$

and considering (20) and (4) the current reference is given as:

$$i_{Sq}^{REF} = \left(c_1 e + c_2 \dot{e} + \ddot{\varphi}\right)\frac{J}{k_m} - \frac{\hat{T}_L}{k_m} \tag{25}$$

where $\hat{T}_L$ is estimated value of T_L. From (25) follows, that e, $\dot{e}$, and $\ddot{e}$ are projected on a current error plane as current error in *q*-axis direction of FOC. Maximal ratio between them and $\| s \|_2$ is bounded by the selection of constants c_1 and c_2 regarding stability and robustness of the controlled system.

B. Rotor magnetization control

If the rotor magnetization is represented by the rotor magnetization current i_{mR} /8/, then the magnetization model is determined by:

$$\tau_R \, pi_{mR} + i_{mR} = i_{Sd} . \tag{26}$$

Magnetization due to FOC is a slow process, in relation to torque production; thus, the offset caused by e_d can be minimized by a suitably designed magnetization current control. Using the same reasoning as kinematics tracking, the magnetization current error is expressed as

$$e_m = i_{mR}^{REF} - \hat{i}_{mR} \tag{27}$$

where $\hat{i}_{mR}$ is an estimate. The current reference is:

$$i_{Sd}^{REF} = c_3 \varepsilon_m + \left(pi_{mR}^{REF} - \frac{\hat{i}_{mR}}{\tau_R} \right) \frac{L_m}{R_R} . \tag{28}$$

C. Modified induction motor model

After calculating $i_{S\Diamond}$ from (4), the equation (3) rewritten in the error form /11/ becomes:

$$u_{k\Diamond}(\rho) = R_S i_{S\Diamond}^{REF} - R_S s_\Diamond + L_{S\sigma} \, pi_{S\Diamond}^{REF} - L_{S\sigma} \dot{s}_\Diamond + e_\Diamond \tag{29}$$

and when rearranged is

$$L_{S\sigma} \, \dot{s}_\Diamond = u_{k\Diamond}(\rho) - R_S s_\Diamond - d_\Diamond . \tag{30}$$

The term

$$d_\Diamond = L_{S\sigma} \, pi_{S\Diamond}^{REF} - R_S i_{S\Diamond}^{REF} - e_\Diamond \tag{31}$$

collects all the disturbances (exogenous and endogenous) acting on the system. It is known that the current tracking problem (3) is equivalent to the stabilization of (30). Because $L_{S\sigma}$ and R_S are semipositive values, the term $-R_S s_\Diamond$ is always stabilizing, i.e. any feedback that stabilized (31) with $R_S = 0$ also stabilizes it with $R_S > 0$. Moreover, the stator windings resistance in IM is usually low, and the term $-R_S s_\Diamond$ can be neglected. Furthermore, considering that i_{Sq}^{REF} during the sampling interval is constant, its derivation is zero. From (31) it follows that $d_\Diamond = e_\Diamond$. Hence, the simplified model

$$L_{S\sigma} s_\Diamond(\rho) = u_{k\Diamond}(\rho) - e_\Diamond \tag{32}$$

is assumed in presented design.

D. Stability analysis

For attraction domain A_0 the reaching condition is derived by second Lyapunov method /9/ from quadratic form $\frac{1}{2} ss^T$, $V \geq 0$ as:

$$\dot{V} = \dot{s}_d s_d + \dot{s}_q s_q \leq 0 . \tag{33}$$

Considering simplified IM model (2) at constant rotor field, where $pi_{mR} = 0$ and consequently $e_{id} = 0$, condition (33) can be written as:

$$\dot{V} = \frac{s_d}{L_{S\sigma}} \left[u_{kd}(\rho) - e_{dq} \right] + \frac{s_q}{L_{S\sigma}} \left[u_{kq}(\rho) - e_{iq} - e_{dq} \right] \leq 0 \tag{34}$$

In the case of selected zero voltage vectors (34) becomes:

$$\dot{V} = \frac{s_d}{L_{S\sigma}} \left[-e_{dq} \right] - \frac{s_q}{L_{S\sigma}} \left[e_{iq} + e_{dq} \right] \leq 0 \tag{35}$$

and it is also evident that it is negative as long as $\dot{\rho} \neq 0$ and the condition (19) for selecting of zero voltage vectors is fulfilled.

In the case of $\dot{\rho} = 0$, (34) is equal to zero, meaning that the system is at a standstill. But there is an assumption for neglecting the influence of R_S for simplified IM model is not valid anymore, consequently full IM model had to be considered in (33). Assuming selection of zero voltage and that during sample interval i_S^{REF} is constant, (35) becomes:

$$\dot{V} = -\frac{s_d}{L_{S\sigma}} R_S i_{Sd} - \frac{s_q}{L_{S\sigma}} R_S i_{Sq} \tag{36}$$

which is negative until the condition (10) is satisfied, since according to (19) signs of s_q and e_q are reciprocal. Those facts can serve as proof of the following theorem:

Theorem: Zero voltage maintains sliding along switching lines, or limit cycle around the error plane origin, if and only if their use satisfies the conditions of (10) and (19).

Žarko Čučej,
Peter Cafuta, and
Rajko Svečko
University of Maribor, Slovenia
e-mail: zarko.cucej@uni-mb.s

Prispelo (Arrived): 24.03.2001 *Sprejeto (Accepted): 01.06.2001*

TESTABILITY ISSUES OF SYSTEM-ON-CHIP DESIGN

Franc Novak
Institut "Jožef Stefan", Ljubljana, Slovenia

Keywords: microelectronics, SOC, System-On-Chip, SECT IEEE P1500, Standards for Embedded Core Test, design, testability, IC, integrated circuits, embedded cores, core wrapper, computer languages, CTL, Core Test Languages, testing strategies, TAM, Test Access Mechanisms, STAM, Serial Test Access Mechanisms, Automatic Test Equipment, BIST, Built-In Self-Test, STIL IEEE P1450, Standards Test Interface Language IEEE P1450, WIP, Wrapper Interface Port, WIR, Wrapper Instruction Registers, WBR, Wrapper Boundary Registers

Abstract: The paper describes current trends in standardisation of design-for-testability approaches for complex circuits with embedded cores also referred to as system-on-chip. The concept of core wrapper and the corresponding core test language, the main two issues of the forthcoming IEEE P1500 Standard, are briefly introduced. Possible strategies for test integration of cores conforming to the standard are discussed. References to the available IEEE P1500 Standard documents and papers are given. The goal of the paper was to enlighten the issues that may be of most interest to a potential user/designer in the applications of our national electronic industry.

Upoštevanje zmožnosti testiranja pri načrtovanju sistema-v-čipu

Ključne besede: mikroelektronika, SOC sistem-v-chip-u, SECT IEEE P1500 standardi za preskušanje jeder vgrajeno, snovanje, preskusljivost, IC vezja integrirana, jedra namenska, ovoj jedra testni, jeziki računalniški, CTL jeziki za opis preskušanja jeder, strategije preskušanja, TAM mehanizmi dostopa za testiranje, STAM mehanizmi dostopa za preskušanje serijski, ATE oprema za preskuse avtomatska, BIST preskušanje vgrajeno vase, STIL IEEE P1450 standardi za jezik preskuševalni vmesniški, WIP vrata ovoja vmesnika, WIR registri ovoja inštrukcijski, WBR registri ovoja mejni

Povzetek: V članku opisujemo sedanje smeri razvoja standardizacije postopkov načrtovanja zmožnosti testiranja kompleksnih vezij z vgrajenimi namenskimi jedri, imenovanih tudi sistem-v-čipu. Na kratko sta opisana zasnova testnega ovoja jedra in jezik za opis testiranja jeder, ki predstavljata glavni značilnosti prihajajočega standarda IEEE P1500. Opisane so strategije povezovanja jeder, ki ustrezajo standardu, v sistem, ki ga bo možno učinkovito testirati. Navedene so reference na dokumente o standardu IEEE P1500 dosegljive preko spletne strani delovne skupine ter objavljene članke in referate. Cilj prispevka je osvetliti tiste vidike standarda, ki bi bili najzanimivejši za potencialnega uporabnika/načrtovalca v aplikacijah domače elektronske industrije.

1 Introduction

Recent technology advances allow to integrate functions that have been traditionally implemented on one or more complex printed circuit boards into one single IC, often referred to as system-on-chip (SOC). The development of this new class of ICs is based on the design technique which integrates large reusable blocks (i.e. cores) that have been designed and verified in earlier applications in practice, /1/. A core may be soft, firm or hard, /1/-/4/. A *soft* core is a synthesizable register-transfer level code of a logic block. It allows much flexibility to the designer and can be realised by different technological processes. A *hard* core consists of a technology-dependent layout and lacks flexibility since it has been optimised for a given performance requirements. A *firm* core contains a gate-level netlist that is ready for placement and routing and thus represents a compromise between the two. Embedded cores provide a wide range of functions, like CPUs, DSPs, interfaces, controllers, memories, and others. The advantage of embedding reusable cores in the design of a new product is a shortened design cycle resulting in reduced time-to-market and reduced cost.

The design of a complex system-on-chip normally requires expertise in different technology areas which is difficult to find in a single design house. Consequently, embedded-core design involves two parties: *core providers* and *core users*. In most cases, the core user (i.e., system integrator) does not have the knowledge about the design of the building blocks (cores). It is neither the interest of core providers to reveal design and implementation details in order to protect their intellectual property. However, the core user is responsible for manufacturing and testing the whole system-on-chip including cores, interconnect logic and possible additional user-designed logic. Complexity of the design and limited knowledge about implementation of cores make the problem of SOC testing rather challenging to the core user. The problem could only be adequately handled by involving both core providers and core users in a joint effort to develop efficient test solutions. In order to provide an independent openly defined design-for-testability method for integrated circuits containing embedded cores, an initiative to develop a standard has been taken by the IEEE P1500 Working Group, /6/.

2 Testing of core-based chips

The SOC designer (core user) has limited knowledge about the adopted cores and he cannot develop adequate tests for them. The core providers need to provide tests for the cores and all the necessary information (i.e., test patterns, timing and protocol description). A SOC normally consists

of cores from different providers and the integration of different core tests into a composite SOC test may become a difficult job because of the diversity of descriptions and test implementation details. Core internal tests need to be described in a commonly accepted way. The forthcoming IEEE P1500 standard defines standard format (i.e., Core Test Language) for the description of core test /6/.

Conventional production test of assembled boards consists of a sequence of separate component tests, bare board test, static test of assembled board (detecting shorts and opens) and dynamic functional test (detecting timing faults). In the case of testing SOC, all the above tests are merged into one composite test instance. Furthermore, in most cases direct access to the core terminals is not provided which makes it difficult to run internal tests of deeply embedded cores. The principle of embedded core testing is presented in terms of conceptual test architecture /3/ consisting of *test pattern source* and *sink*, *test access mechanism* (TAM) and *core test wrapper* (Figure 1). In order to test a core, a test source (i.e., test pattern generator) generating test stimuli and a test sink (i.e., response compactors, current monitors, etc.) collecting the test responses must be provided. Test access mechanism transports test patterns from the source to the core and test responses from the core to the test sink. Finally, the core test wrapper, a thin shell around the core, provides interface between the embedded core and its environment. It connects the terminals of the core to the rest of SOC (in the normal mode) and to the test access mechanism (in the test mode). The IEEE P1500 Standard defines the structure and the operation of the test wrapper /6/.

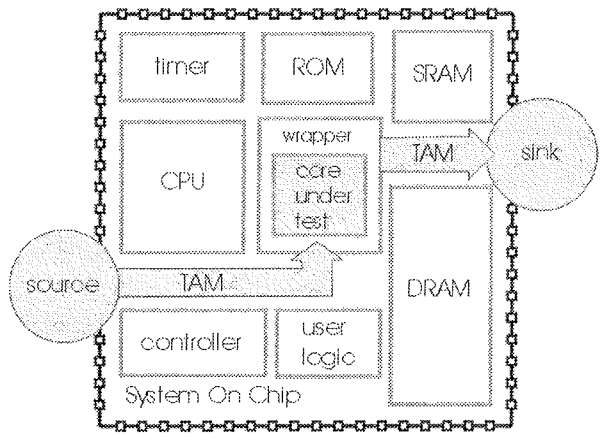


Figure 1: Embedded core testing involves source, sink, TAM and wrapper

The described test architecture is implemented in various ways depending on the type of the core (i.e., logic, memory, analog or mixed-signal), type of pre-defined tests provided by the core vendor, and required test quality. For example, test patterns can be generated by external automatic-test-equipment (ATE) or built-in self-test (BIST) logic implemented in SOC. Likewise, test results can be evaluated by external ATE or compressed to a signature and compared to a reference value by the BIST logic on SOC. More details on this are given in Zorian *et al.* /3/.

3 IEEE P1500 Standard for Embedded Core Test (SECT)

Activities on IEEE P1500 SECT started in 1995, and have been officially approved by the IEEE Standards Activities Board in 1997. The work currently focuses on a standard for testing digital logic and memory cores, future extensions will include also analog and mixed-signal cores. The mission statement defines the following scope /6/:

"This project will develop a standard test method for Integrated Circuits containing embedded cores, i.e. reusable megacells. This method will be independent of the underlying functionality of the Integrated Circuit or its individual embedded cores. The method will create the necessary testability requirements for detection and diagnosis of such integrated Circuits, while allowing for ease of interoperability of cores originated from distinct sources. This method will be usable for all classes of digital cores including hierarchical ones."

The two primary issues are to provide means for (1) efficient core test knowledge transfer, and (2) the test access to the embedded cores. Accordingly, the standard defines (1) a language for the description of the test-related information for the cores embedded in the SOC, and (2) the test wrapper architecture of the embedded core. The work on the standard has progressed to the draft version IEEE P1500/D0.3 and aims to be ready for ballot in 2001 /6/.

3.1 Core test language

IEEE P1500 SECT defines the Core Test Language (CTL) in order to facilitate the transfer of the core test-related information from the core provider to the core user. CTL uses the syntax of IEEE 1450, Standard Test Interface Language (STIL), /7/, and describes test information including test data, test methodology, core configurations and necessary connectivity information for system integration. The objective is to provide all the necessary information for the implementation of core wrapper including the description of core signals, timing, electrical characteristics, core external connections, protocol for applying test patterns to the core terminals, etc. Detailed description of CTL is beyond the scope of this paper. Interested readers can find more information on this subject together with an illustrative example describing the way of transforming a bare core into a 1500-compliant core in /4/.

3.2 Core test wrapper

Test wrapper is a thin shell around the core and serves as an interface between the core and the test access mechanism(s). During normal operation, wrapper connects core inputs and outputs to SOC functional wires. For testing purposes, wrapper has modes in which core inputs

and outputs are connected to a mandatory serial TAM (one-bit wide) and optional scalable parallel TAMs which provide access for core-internal and core-external tests. Wrapper operation is controlled by a set of control and clock signals provided at the Wrapper Interface Port (WIP). WIP also includes serial scan terminals WSI and WSO which are used to shift-in and shift-out serial test data. (The function of WSI and WSO is similar to TDI and TDO terminals of IEEE 1149.1, digital boundary-scan architecture /8/). Test wrapper contains the following mandatory registers:

- *wrapper instruction register* (WIR) which is similar to IEEE 1149.1 instruction register and controls the operation of the wrapper. WIR receives instructions via wrapper serial input WSI.
- *wrapper boundary register* (WBR) to which the core functional terminals are connected. It is a serial shift register similar to the IEEE 1149.1 boundary-scan register.
- One-bit *bypass register* which is similar to IEEE 1149.1 bypass register. It is used to bypass the WBR. In a single scan path configuration, where WSI and WSO terminals of cores are connected in series, it may become inconvenient to shift data through the entire sequence of WBRs. Bypass registers enable to skip out the WBRs of the cores that are not being tested.

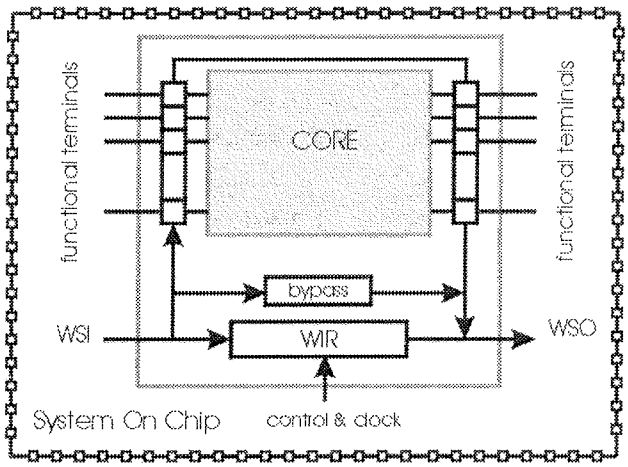


Figure 2: Test wrapper structure

Serial TAM and (if available) parallel TAMs provide means for performing core-internal and core-external tests. Core-internal test is based on the test information that the core user gets from the core provider. It may consist of the application of test patterns within a specified test protocol, or of initiation of a built-in self-test of the core. Core-external test checks external connections between the cores and additional glue logic designed by the SOC integrator.

For the core-internal tests, test stimuli are provided via TAM to wrapper boundary at the core input terminals and test results are read via TAM from the wrapper boundary at the core output terminals. For the core-external tests, initial logical values are set-up via TAM at the wrapper boundary at the core output terminals and results are observed at the wrapper boundary at the core input terminals.

4 Possible test configurations

From the conceptual point of view one may notice several points of similarity between IEEE P1500 SECT and IEEE 1149.1. For example, wrapper registers WIR, WBR and bypass have similar role as instruction, boundary-scan and bypass register in IEEE 1149.1. Furthermore, as mentioned above, the function of WSI and WSO is similar to TDI and TDO in digital boundary-scan architecture. But there are also substantial differences: the operation of the TAP Controller which is the "heart" of the IEEE 1149.1 compliant circuit is given by the state diagram which unambiguously defines the test protocol - on the other hand, IEEE P1500 SECT does not define the operation of the test wrapper by a state diagram, and allows the designer of a test wrapper a lot of freedom.

SOC integrator can choose different strategies of implementing STAM and parallel TAMs of individual wrappers depending on the complexity of core-internal tests, the amount of additional user defined logic, overall complexity of the SOC and on the conditions imposed by the available ATE that will be used in production test. For example, for a core with a built-in self-test it may be sufficient to provide test wrapper only with STAM. On the other hand, some other core may need extensive amount of test patterns that can only be transferred in reasonable time via parallel TAM. Wrappers can be connected in different configurations (i.e., multiplexing, daisychain, etc.) differing in test time, wiring and SOC performance. Besides, possible implementation of boundary-scan at the level of individual cores and requirements for its implementation at the level of SOC will impact the selection of wrapper test features and system level core configurations. Effective combination of IEEE 1149.1 and IEEE P1500 SECT infrastructure in SOC test is an interesting problem in practice.

5 Conclusion

SOC testing is one of the current hot topics in the field of electronic test. Several papers and vivid discussions at recent European Test Conference /9/ confirm the importance of providing efficient solutions to the problem of testing embedded cores integrated in a complex SOC. In the paper, the basic approach to testing SOC formalised in IEEE P1500 SECT is described. Another issue concerns intellectual property of core providers. Due to the opposite interests of core providers and core users regarding the level of the core implementation details that should be revealed to the user (making SOC testing easier) the problem of information transfer remains a challenge for both participating parties. Here again, IEEE P1500 SECT offers means that may help them in achieving a reasonable solution.

Finally one could ask: what consequences will the forthcoming IEEE P1500 SECT have to those users that do not produce complex SOC but rather use them in their products? We can expect from the SOCs producers to provide some information related to testing embedded cores in a SOC for the purpose of debugging and for performing system functional test. Besides, cores including scalable test wrapper are likely to become a standard product on the market, ready for integration as well in simple electronic systems (e.g., intelligent sensors) which makes the IEEE P1500 SECT interesting to a broader group of potential users.

Literature

/1/ R.K.Gupta, Y.Zorian, "Introducing core-based system design", IEEE Design and Test of Computers, Vol. 14, No. 4, October-December 1997, pp. 15-25.

/2/ Y.Zorian, "Test requirements for embedded core-based systems and IEEE P1500", Proc. International Test Conference, Washington, DC, November 1-6, 1997, pp. 191-199.

/3/ Y.Zorian, E.J.Marinissen, S.Dey, "Testing embedded-core based system chips", Proc. International Test Conference, Washington, DC, October 18-23, 1998, pp. 130-143.

/4/ E.J.Marinissen, Y.Zorian, R.Kapur, T.Taylor, L.Whetsel, "Towards a standard for embedded core test: an example", Proc. International Test Conference, Atlantic City, NJ, September 28-30, 1999, paper 24.1.

/5/ E.J.Marinissen, R.Kapur, Y.Zorian, "On using IEEE P1500 SECT for test plug-n-play", Proc. International Test Conference, Atlantic City, NJ, October 1-5, 2000, paper 24.1.

/6/ IEEE P1500 Standard for Embedded Core Test: http://www.manta.ieee.org/groups/1500/

/7/ T.Taylor, G.Maston, "Standard Test Interface Language (STIL): A new language for Patterns and waveforms", Proc. International Test Conference, Washington, DC, October 20-25, 1996, pp. 565-570.

/8/ IEEE Std 1149.1-1990: IEEE Standard Test Access Port and Boundary-Scan Architecture.

/9/ Proceedings of European Test Workshop ETW2001, Stockholm, May 29 - June1, 2001.

Franc Novak
Institut "Jožef Stefan"
Jamova 39, 1000 Ljubljana, Slovenia
tel. +386 1 4773 386
fax. +386 1 2519 385
Email: franc.novak@ijs.si

Prispelo (Arrived): 18.05.01 *Sprejeto (Accepted): 01.06.01*

DODATNI PRIMERJALNI TESTI ZA SIMULATORJE SPICE

Tomaž Dogša
Fakulteta za elektrotehniko, računalništvo in informatiko, Univerza v Mariboru

Ključne besede: SPICE orodja računalniška, testi primerjalni, simulatorji računalniški, točke delovne, DC analize enosmerne, testiranja avtomatska, avtomatizacija testiranja, vezja naključna

Povzetek: Dosedanji primerjalni testi, s katerimi lahko primerjamo kakovost simulatorjev, temeljijo na posebej izbrani majhni množici vezij. V prispevku predlagamo dodatne skupine primerjalnih statističnih testov in kriterije, s katerim bi lahko na objektiven način primerjali kakovost simulatorjev električnih vezij. Vsa vezja, ki so vključena v dodatno množico testov imajo naključno tvorjeno strukturo in naključno izbrane elemente in parametre. Ker lahko s posebnim generatorjem vezij tvorimo poljubno število takih vezij, je možno podajati statistično ovrednotena kvantitivna merila glede kakovosti simulatorjev.

Additional Benchmark Tests for SPICE Simulators

Keywords: SPICE computer tools, Simulation Program with Integrated Circuit Emphasis computer tools, benchmarks, comparative tests, computer simulators, biases, operating points, DC analyses, Direct Current analyses, automatic testing, test automation, random circuits

Abstract: The purpose of benchmark test is to compare the quality attributes of circuits simulators. Existing benchmark tests are based on selected small set of electronic circuits. In this paper we propose additional sets of statistically based benchmark tests and corresponding criteria that enable unbiased comparison. All test circuits that form additional benchmark sets have randomly generated structure, randomly chosen elements and their parameters. Statistically quantization of quality attributes is now possible, since high number of circuits can be generated by the special software tool.

1. Uvod

Načrtovanje elektronskih vezij brez pomoči računalnika je danes praktično neizvedljivo. Vse večja kompleksnost vezij in nelinearnost elektronskih elementov v večini primerov onemogočajo analitični pristop. Načrtovalci si v takih primerih pomagajo s simulatorji elektronskih vezij. Simulatorji so zelo kompleksni programski paketi, ki se neprestano spreminjajo: izboljšujejo se uporabljeni algoritmi in modeli ter dodaja se nova funkcionalnost. Eden izmed glavnih namenov simulatorja je napovedovanje obnašanja realnega vezja. Kljub relativni zrelosti simulatorjev, se dogaja, da dajejo napačne rezultate (glej npr. /PERŠIČ,1995/). Na tržišču obstaja več vrst simulatorjev, ki se med seboj razlikujejo po funkcionalnosti, uporabljenih algoritmih in modelih, ceni in drugih atributov kakovosti. Njihova medsebojna primerjava temelji na določenih primerjalnih testih (benchmark). Kaj je primerjalni test? Davidson in Harlow v svojem uvodniku /DAVIDSON,2000/ ponujata delno prirejeno definicijo, ki jo lahko najdemo v leksikonu Merriam-Webster Collegiate Dictionary: "Primerjalni test je standardiziran problem (vezje ali del vezja), ki ga uporabljamo za primerjavo zmogljivosti (hitrost, učinkovitost, kakovost rezultata) različnih orodij in algoritmov".

Namen primerjalnih testov ni samo primerjanje izbranih karakteristik (npr. hitrosti) ampak širši vpogled v kakovost simulatorja. Zaradi tega so tudi zanimivi za načrtovalce in preverjevalce EDA (Electronic Design Automation) programske opreme. S primerjalnimi testi lahko testirajo simulatorje ali pa jih uporabijo za merjenje uspešnosti novih ali izboljšanih algoritmov. Vsak primerjalni test mora biti sestavljen iz opisa postopka, opisa testnih primerov in kriterijev za vrednotenje primerjave. Testne primere tvorijo vhodni podatki in pričakovani rezultati oziroma pričakovano obnašanje.

Primerjalni testi naj bi predstavljali reprezentativne primerke iz posameznih problemskih razredov. Npr. zelo znana zbirka 58 vezij, ki so jo leta 1990 predlagali na eni izmed delavnic na MCNC (Microelectronic Center of North Carolina. (http://www.cbl.ncsu.edu/), je sestavljena in petih skupin. Te skupine lahko glede kompleksnosti vezij razdelimo v dve grupi: skupina majhnih (približno do 500 elementov) in skupina obširnejših (nad približno 1000 elementov) vezij. Vezja so tako izbrana, da pokrivajo celotno problemsko domeno.

Slabost sedanjih primerjalnih testov oziroma metod kritizira tudi F. Brglez /BRGLEZ,2000/. Zavzema se za znanstveni pristop na področju eksperimentiranja, kar pomeni, da se ne oziramo na nekaj izbranih testnih vezij ampak na množico. S statistično analizo nato ovrednotimo rezultate eskperimenta oziroma primerjalne analize. Zato predlagamo, da se obstoječemu nizu primerjalnih testov dodajo še tri skupine. Tako bi za potrebe primerjalne analize in testiranja uporabljali naslednje skupine:

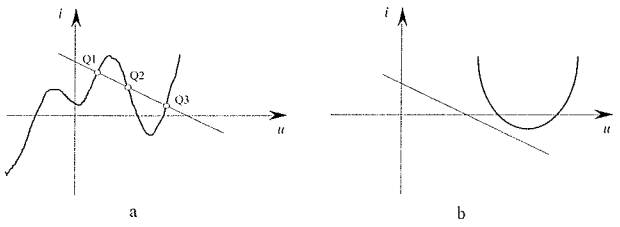
1. skupina: izbor posameznih konkretnih vezij (obstoječa skupina),
2. skupina: množica naključno generiranih topološko pravilnih vezij,
3. skupina: izbor posameznih topološko nepravilnih vezij,
4. skupina: množica naključno generiranih topološko nepravilnih vezij.

Vključitev skupine s topološko nepravilnimi vezji je smiselna zaradi tega, ker pri takih vezjih rešitev (niti teoretična) ne more obstajati in nas mora o tem simulator obvestiti. V pris-

pevku bomo najprej opisali določeno problematiko, ki je povezana z nakljućnim generiranjem vezij. Kljub temu, da se bomo omejili, le na simulatorje analognih vezij to še ne pomeni, da predlaganih idej ni možno posplošiti na digitalna in analogno-digitalna vezja. Vsak simulator nudi uporabniku več vrst analiz. Najbolj osnovna je vsekakor analiza delovne točke. Ker predstavlja izhodišče za skoraj vse druge analize, smo se osredotočili samo na njo. Torej, zanimali nas bodo primerjalni testi, s katerimi bi lahko ovrednotili uspešnost algoritmov za analizo delovne točke. Najprej bomo na kratko opisali probleme, ki se utegnejo pojaviti pri analizi delovne točke nato pa problematiko generiranja nakljućnih vezij. Za ilustracijo bomo prikazali tudi konkretne rezultate primerjalne analize za tri simulatorje: SPICE2G6 (verzija Intusoft IS SPICE 1.41 12/12/87, PSPICE (verzija 3.01, januar 1987) in SPICE3F4 (verzija 18. februar 1999). Izbor je bil povezan predvsem z njihovo dosegljivostjo. Če bi uporabili najnovejše verzije, bi zagotovo dobili drugačne rezultate.

2. Delovna točka

Delovna točka je niz takšnih parov enosmernih tokov in napetosti, ki hkrati zadoščajo karakteristiki elementov in obema Kirchhoffovima zakonoma. Ker gre za enosmerno analizo, simulator najprej pretvori vezje v rezistivno varianto in nato izvede simulacijo. Vsi algoritmi, ki jih uporabljajo simulatorji analognih vezij za analizo delovne točke, temeljijo na določenih iterativnih metodah, ki jih omejimo s številom iteracij in zahtevano natančnostjo rezultata. Pri analitičnem ali grafičnem izračunu vidimo, da lahko obstaja ena, več ali pa nobena rešitev (slika 1 a in b).



Slika 1 Zgled grafične analize dveh vezij, ki sta sestavljeni iz baterije, upora in nelinernega elementa.Vezje (a) tri teoretične rešitve, vezje (b) nima teoretične rešitve

Več rešitev več ne moremo interpretirati kot rezultat enosmerne analize, ampak kot stacionarno stanje prehodnega pojava električnega vezja. Rešitev torej ni odvisna samo od vezja in nastavitev parametrov, s katerimi vplivamo na algoritem, ampak tudi od začetnih pogojev. Ena izmed slabosti tipičnih simulatorjev analognih vezih (npr. SPICE) je ta, da izračunajo samo eno delovno točko, kljub temu, da obstaja več rešitev. Obstajajo tudi simulatorji, ki z uporabo popolnoma drugačnih algoritmov, izračunajo vse delovne točke oziroma ravnotežna stanja. Najbolj znani metodi sta: iterativna odsekoma-linearna kombinacijska analiza /CHUA, 1975/ in homotopna metoda /TRAJKOVIC,1991/. Slednja je tudi implementirana v simulatorju HomSPICE /TRAJKOVIC,1998/, ki pa ga nismo uspeli preizkusiti.

Eden izmed pogojev, da bo simulator poiskal delovno točko, je obstoj teoretične rešitve. Neobstoj teoretične rešitve se lahko pojavlja samo pri vezjih, ki vsebujejo enega ali več nerealno modeliranih elementov. Glede oblike enosmernih karakteristik modelov ni nobenih omejitev razen za vrednosti toka oziroma napetosti, ko le-ta limitira proti neskončnosti. Ker vedno obstaja neka delovna točka, pri kateri postane vezje totalno pasivno, pomeni, da se morajo karakteristike dvopolnih elementov začeti v prvem in končati v tretjem kvadrantu. Takoj vidimo, da idealni napetostni in tokovni vir te zahteve ne izpolnjujeta. Ta problem lahko simulator reši z dodajanjem ustreznega upora k vsakemu napetostnemu ali/in tokovnemu viru in z dodatnimi zahtevami glede topologije (npr. zanka iz samih napetostnih virov je prepovedana). Če karakteristika vsakega elementa zadosti prej omenjenemu kriteriju, potem vedno obstaja teoretična rešitev. Če vsaj en element tega kriterija ne izpolnjuje, se lahko zgodi, da teoretična rešitev ne obstaja (slika 1 b).

Vsa pravkar opisana problematika se uporabniku kaže v neuspešnosti analize, ki se večinoma navzven pokaže kot nekonvergiranje rešitve. Problem konvergence je možno reševati na več načinov:

1. Simulatorju pomagamo s podatkom o približni rešitvi (stavek .NODESET).
2. Spremenimo modele - uporabimo realnejše modele.
3. Spreminjamo razne parametre, s katerimi vplivamo na potek reševanja (npr. povečamo največje število iteracij).
4. Uporabimo počasi naraščajoče napetostne vire (source-stepping algorithms).
5. V vsako vozlišče dodamo parazitno prevodnost, ki jo počasi manjšamo (Gmin -stepping).
6. Z dodanimi parazitnimi reaktivnimi elementi pretvorimo vezje v dinamično in simuliramo vklop vezja (pseudo-transient analysis).
7. Izberemo drugačen algoritem za analizo delovne točke (uporabimo npr. odsekoma-linearno kombinacijsko analizo ali homotopno metodo).

Pravilnost izračuna delovne točke je odvisna od pravilnosti uporabljenih modelov in pravilnosti ter učinkovitosti algoritma. Pri sodobnih simulatorjih je lahko vzrok za napačen izračun delovne točke tudi v napačnem delovanju postprocesorja. V tem primeru jedro simulatorja izračuna pravilno vrednost, grafični postprocesor jo pa izpiše napačno.

3. Odpoved simulatorja pri izračunu delovne točke

Izračun delovne točke je ena izmed temeljnih analiz, ki jih izvaja simulator. Nepravilnosti pri izračunu delovne točke vplivajo na pravilnost večine analiz (npr. .AC, .TF, .DC, .TRAN). Potem, ko smo sprožili zahtevo za analizo delovne točke, lahko simulator preide v naslednja stanja:

1. Delovna točka je izračunana in **se nahaja** znotraj dovoljenih odstopanj pričakovane vrednosti.
2. Delovna točka je izračunana vendar se **ne nahaja** znotraj dovoljenih odstopanj pričakovane vrednosti. V tem primeru gre za alternativno delovno točko oziroma za vezje, ki ima več delovnih točk. Možno je tudi, da simulator deluje nepravilno.
3. Delovna točka **ni izračunana**, kljub temu da ima vezje pravilno topološko strukturo (npr. rešitev ne konvergira ali pa nastopi popolna odpoved simulatorja)
4. Delovna točka ni izračunana, ker ima vezje nepravilno topološko strukturo (npr. zanka iz samih napetostnih virov).

Stanje številka 3 bomo klasificirali kot odpoved. Popolna odpoved simulatorja se pojavi takrat, ko delovanje programa nasilno ustavi operacijski sistem. Za firmo, ki je izdelala simulator je to sicer zelo neprijetna odpoved, za uporabnika pa zgolj moteča in hkrati nenevarna, saj je le-ta z odpovedjo seznanjen. Kritične oziroma fatalne so lahko tiste odpovedi, katerih uporabnik ne opazi. To se lahko zgodi, če ne razpolaga s pričakovano vrednostjo oziroma je interval, v katerem pričakuje rezultat, prevelik.

4. Naključno analogno vezje

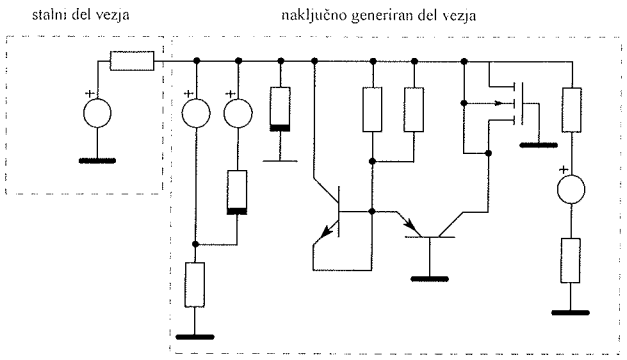
Naključna vezja lahko generiramo na dva načina. Postavimo nek splošen model, ki ustreza neki skupini vezij in nato s spreminjanjem parametrov in nekaterih delov strukture tvorimo množico naključnih vezij. Zgled za to metodo bi lahko bil npr. splošen model enostopenjskega diferenčnega ojačevalnika, ki vključuje tudi nekaj variant. Pri drugi metodi naključno generiramo graf vezja in nato elemente. S to metodo lahko v bistvu nastane katerokoli možno vezje, pri prvi pa smo omejeni z izbranim splošnim modelom.

Za generiranje naključnih vezij smo izdelali poseben program (generator naključnih vezij), ki delno združuje oba pristopa. Naključno vezje, ki ga tvori generator, je sestavljeno iz stalnega in naključnega dela. Najpomembnejši podatki, ki vplivajo na strukturo naključnih vezij in vrednosti parametrov, so:

1. Deleži posameznih elementov in njihovi parametri (R, L, C, E, G, I, V, D, NMOS, PMOS, QN, QP). E in G sta polinomska vira, ki ju uporabljamo za modeliranje krmiljenih virov oziroma nelinearnih dvopolov. Parametri so: največja in najmanjša vrednost ter vrsta porazdelitve. Trenutna verzija ne omogoča naključni izbor parametrov v .MODEL stavkih.
2. Kompleksnost vezja (število vozlišč, število elementov).
3. Odločitev o generiranju topološko pravilnih ali nepravilnih strukturah.
4. Izbor porazdelitvene funkcije po kateri se vrši izbor naključnih entitet (Gaussova, konstantna ali kaotična porazdelitev).
5. Statistična privilegiranost dveh vozlišč. Pri večini realnih vezij lahko vidimo, da incidenčna matrika ni enakomerno napolnjena oziroma nekatera vozlišča izrazito odstopajo glede števila priključenih elementov. To sta vozlišči, kamor je priključena napajalna napetost in masa (glej sliko 3).

Na videz je funkcija generatorja podobna tisti, ki se uporablja pri Monte Carlo analizi. Razlika je v tem, da tukaj naključno spreminjamo strukturo vezja, elemente in parametre, medtem ko pri Monte Carlo analizi samo vrednosti parametrov.

Glede na izbor podatkov, ki so vhod v generator, lahko generirarmo zelo pestro množico vezij. Z nelinearnimi upori, ki so implementirani z G viri (za SPICE3 se uporablja B element), generator simulira uporabo zunanjih vedenjskih modelov. Z izborom lihe oziroma sode stopnje polinoma generiramo teoretično nemogoče (npr. element na sliki 1 b) oziroma mogoče nelinearne upore (npr. element na sliki 1 a). S temi upori lahko tudi spreminjamo nelinearnost vezja. Zgled naključno generiranega vezja prikazujeta sliki 2 in 3.



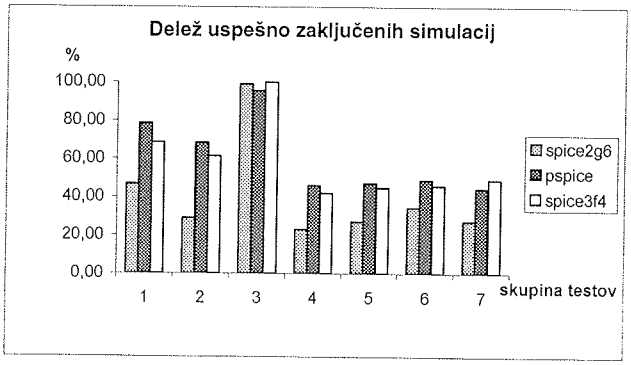
Slika 3 Shema naključno generiranega analognega vezja narisanega na podlagi opisa iz slike 2. Stalni del vezja je enak za vsa generirana vezja.

5. Rezultati primerjalnega testiranja

Vsako testiranje izvajamo po naslednjih korakih: tvorjenje testnih vzorcev, tvorjenje pričakovih vrednosti, izvedba analize in vrednotenje rezultatov. Vse korake razen drugega je relativno enostavno avtomatizirati. Za avtomatizacijo drugega koraka moramo napraviti zahteven program za sintezo vezja. V primeru testiranja več simulatorjev imamo tudi možnost, da enega izberemo za referenčnega. Glede na predlagane skupine vezij namenjenih primerjalnemu testiranju, smo izvedli samo testiranje z množico naključno generiranih topološko pravilnih vezij.

Tabela 1 Opis testnih vezij

Testna garnitura	število vezij	opis
1	169	vsi elementi, brez nelinearnih uporov
2	200	samo NMOS, PMOS, D, R in napajalni viri
3	199	samo QN, QP, D, R in napajalni viri
4	169	vsi elementi, nelinearnost uporov do 4.stop.
5	169	vsi elementi, nelinearnost uporov do 3.stop.
6	168	vsi elementi, nelinearnost uporov do 2.stop.
7	106	brez polprevodnih elementov, nelinearnost uporov do 4.stop



Slika 4 Delež uspešno zaključenih simulacij

Ker bi opis in diskusija rezultatov za vse primerjalne teste presegala dovoljen obseg prispevka, se bomo osredotočili le na sedmo garnituro testov, v kateri ni nobenih polprevodnih elementov. S tem smo izločili morebiten vpliv kakovosti

```
VEZ117.cir
*SPICE_NET
*Stevilka vezja:
*117
*Datum nastanka:   4.4.2001 Generator vezij:V5.0 2.4.2001
*Konfiguracijska datoteka: k4g2k1.dat
*Nastanek konfiguracijske datoteke: 4.4.2001  12:32:24
*Verzija opisovanja nel. elementov:2 Stevilo vozlisc: 6 Stevilo el.: 14
*Nacin generiranja vezja: nakljucno
*Statisticno poudarjeno vozlisce: 0 20.00%
*Statisticno poudarjeno vozlisce: 1 20.00%

R1 0 5  1.04222864689678E+0004
R2 1 3  1.64998529084921E+0004
R3 2 0  7.76117287476063E+0004
V4 3 2 -9.63017179630697E+0000
R5 4 1  5.58461088487506E+0003
E6 5 1 POLY(1) (4 6)  3.88584041036665E-0001 -4.95419465005398E-0002
+  -1.17212752811611E-0001 -5.41528668254614E-0002
+  -6.52682286687195E-0001
G7 6 5 POLY(1) (6 5) -1.81034177541733E-0001
+    -4.58973378874362E-0001 + 2.83149098977447E-0001
QN8 4 0 1 QN
R9 1 4  3.21886612679362E+0004
E10 6 1 POLY(1) (2 1) -3.01108809188008E-0001
+   -5.59775688685477E-0001 + 4.59779966622591E-0001
QP11 1 3 3 QP
G12 0 1 POLY(1) (0 1) -6.98641702532768E-0001  5.45442000962794E-0001
+   8.75892678275704E-0001 -1.84644504450262E-0001 -7.96733874827623E-0001
MP13 1 0 1 1 PENH L=8U W=7U
QN14 1 2 2 QN
.OP
* ======= Dodana datoteka : MOD_VSI.MOD  ================
* Posebej dodamo nap. vir zato, da bo vedno prisoten vsaj en
VDD 5000 0 5
RG  5000 1 1
.OPTIONS NOMOD

**********************************************************************
**                      ( MODEL M8CN-290)                           **
**      MCNC 0.8 CMOS PROCESS   PISCES                              **
**      ( NOMINAL )     FEBRUARY 1990                               **
**      SOURCE: CIRCUITSIM90 BENCHMARK CIRCUITS FILE MODELS.NOM     **
**********************************************************************
```

Slika 2 Zgled naključno generiranega analognega vezja

notranjih modelov in se osredotočili predvsem na učinkovitost algoritma za izračun delovne točke. Statistična porazdelitev elementov je bila naslednja: R (40%), V (10%), I (10%), G (20%), E (20%). Z napetostno krmiljenimi tokovnimi viri (G) smo realizirali nelinearne upore, katerih naključno generirana karakteristika je definirana s polinomom. Največja stopnja polinoma je bila 4. Podobno velja za krmiljen nelinearni napetostni vir E. Za vrednotenje primerjalnega testa smo postavili tri merila: merilo uspešnosti, merilo podobnosti in merilo ekskluzivnosti.

Merilo uspešnosti je delež uspešno zaključenih simulacij. Za učinkovito primerjalno testiranje morajo biti testna vezja tako izbrana, da je uspešnost vedno manjša od 100%, sicer nastopi pojav nasičenja (merilo več ne zaznava sprememb). Če se uspešnost začne približevati 100%, je potrebno povečati število vezij oziroma stopnjo nelinearnosti.

Zanimiva sta tudi atributa *skupna napaka* in število *alternativnih rešitev.* Razliko med referenčno in dejansko vrednostjo delovne točke vrednotimo s povprečnim kvadratičnim pogreškom. Če je bil ta večji od nekega izbranega praga (5V), potem smo izračunano delovno točko vezja kvalificirali kot alternativno. Skupna napaka je vsota vseh napak vezij, ki so bila uspešno simulirana (izvzeta so bile alternativne delovne točke). To merilo je seveda problematično, saj je za naključno vezje težko podati enoten kriterij, ki bi omogočal identifikacijo alternativnih točk.

Tabela 2 Podrobni rezultati za sedmo garnituro testov.

	SPICE2G6	PSPICE	SPICE3F4
število neuspešnih simulacij	73%	56%	51%
število uspešnih simulacij	27%	44%	49%
skupna napaka	27V	31V	-
štev. altern. rešitev	2%	9%	-

Merilo podobnosti: s to metriko vrednotimo podobnost v obnašanju simulatorjev. Izračunamo ga kot kvocient med številom enakih stanj, v katero prideta dva simulatorja in številom testov. Če je podobnost med dvema simulatorjema enaka 1, pomeni, da sta bila uspešna in neuspešna pri enakih testnih primerih (vezjih). Pri testni garnituri številka 7 sta se SPICE3F4 in PSPICE v 87% testov obnašala enako (tabela 3).

Tabela 3 Merilo podobnosti za sedmo garnituro testov.

	spice2g6	pspice	spice3f4
spice2g6	1	0,83	0,76
pspice	0,83	1	0,87
spice3f4	0,76	0,87	1

Merilo ekskluzivnosti: To merilo se nanaša na uspešnost tistih vezij, pri katerih je določen simulator odpovedal. Npr. SPICE2G6 je odpovedal pri 77 vezjih (tabela 4) in v množici teh vezij je PSPICE uspešno simuliral 23% vezij, SPICE3F4 pa 30%. Hkrati tudi vidimo, da vsa vezja, ki so povzročila odpoved simulatorja SPICE3F4, so tudi povzročila odpovedi ostalih simulatorjev. Ali z drugimi besedami, tam kjer SPICE3F4 ni uspel, nista uspela tudi ostala simulatorja.

Z drugimi skupinami testov smo ugotovili, da to vedno ne velja. Npr. pri testni garnituri štev. 2 (tabela 5), je PSPICE uspel poiskati rešitev za 37% vezij, za katere je bil SPICE3F4 neuspešen. Kljub temu lahko glede na vrednost ekskluzivnosti, še vedno lahko sklepamo, da je SPICE3F4 najboljši.

Tabela 4 Merilo ekskluzivnosti za sedmo garnituro testov.

	spice2g6	pspice	spice3f4
spice2g6	77 (100%)	18 (23%)	23 (30%)
pspice	0 (0%)	59 (100%)	5 (9%)
spice3f4	0 (0%)	0 (0%)	54 (100%)

Tabela 5 Merilo ekskluzivnosti za drugo garnituro testov.

	spice2g6	pspice	spice3f4
spice2g6	142 (100%)	84 (59%)	66 (46%)
pspice	5 (8%)	63 (100%)	15 (24%)
spice3f4	1 (1%)	29 (37%)	77 (100%)

7. Sklep

Tradicionalno primerjalno testiranje temelji na izbrani majhni množici tipičnih vezij. Ker vezja niso izbrana naključno in ker jih je premalo, ni možno uporabiti statističnih meril. Predlagamo, da se k obstoječi skupini dodajo še naključno generirana vezja. V tem primeru lahko uporabimo tri nova merila: merilo uspešnosti, podobnosti in ekskluzivnosti. Dva simulatorja sta enako kakovostna, če imata enako uspešnost, podobnost in ekskluzivnost. Pokazali smo, da predlagana merila in postopek testiranja večata objektivnost primerjalnega testiranja.

Največji problem, ki nastopa pri testiranju, je določitev pričakovanih rezultatov (v našem primeru so to potenciali vseh vozlišč). Za vsako vezje bi bilo potrebno izračunati brez uporabe simulatorja delovno točko. Ker gre za naključna nelinearna vezja, ki niso vedno zaporedno-vzporedna, bi izračun delovne točke za npr. 1000 vezij predstavljal izredno naporno delo.

Ta problem bomo skušali rešiti z nadgradnjo obstoječega generatorja naključnih vezij, ki lahko tvori naključna vezja tako, da si najprej izbere naključno vrednost delovne točke in nato napravi sintezo vezja. Zaradi težav pri sintezi, zanekrat niso vključeni polprevodni elementi, ampak samo linearni R, I, V in nelinearni G in E.

8. Literatura

/BRGLEZ,2000/ Franc Brglez *"The Scientific Method and Design and Test"*, IEEE Design & Test of Computers, julij-september, 2000, str. 144,142,143.

/CHUA,1975/ Leon O. Chua, Pen-Min Lin: *" Computer-aided analysis of electronic circuits"*, Prentice-Hall, Englewood Cliffs, New Jersey, 1975.

/CHUA,1976/ L. O. Chua and A. Ushida: *"A switching-parameter algorithm for finding multiple solutions of nonlinear resistive circuits,"* IEEE Trans. Circuit Theory, Vol. CT-19, No. 4, str. 215-239, 1976.

/DAVIDSON,2000/ S. Davidson, J. Harlow: *"Guest Editors' Introduction: Benchmarking for Design and Test"*, IEEE Design & Test of Computers, julij-september, 2000, str. 12-14.

/PERŠIČ,1995/ Boštjan Peršič: *"Primer napačnega delovanja numerične integracije simulatorja SPICE"*, Elektrotehniški vestnik 62(2):117-125, 1995.

/TRAJKOVIC,1991/ Lj. Trajkovic, R. C. Melville and S. C. Fang, *"Finding dc operating points of transistor circuits using homotopy methods"*, Proc. IEEE Int. Symp. Circuits and Systems, Singapore, junij 1991, str. 758-761. (glej tudi http://divine.eecs.berkeley.edu/~ljilja/).

/TRAJKOVIC,1998/ Lj. Trajkovic, E. Fung, and S. Sanders, *"HomSPICE: Simulator with homotopy algorithms for finding dc and steady state solutions of nonlinear circuits"*,Proc. IEEE Int. Symp. Circuits and Systems, Monterey, CA, June 1998, TPA 10-2.

Dr. Tomaž Dogša,
Fakulteta za elektrotehniko, računalništvo in informatiko v Mariboru
Smetanova 17
2000 Maribor, Slovenija
Tel. (02) 220 7231
E- pošta: tdogsa@uni-mb.si

Prispelo (Arrived): 25.04.01 *Sprejeto (Accepted): 01.06.01*

POWER ELECTRONIC BUILDING BLOCKS: A SURVEY

Žarko ČUČEJ
Univerza v Mariboru, Fakulteta za elektrotehniko, računalništvo in informatiko

Key words: power electronics, PEBB, Power Electronics Building Blocks, development results, circuit topologies, electronic circuits, THD, Total Harmonic Distortion, PWM switches, Pulse Width Modulation switches, ZVT, Zero-Voltage Transition, ZCT, Zero-Current Transition, ZVS, Zero-Voltage Switching, ZCS, Zero-Current Switching, ARCP, Auxiliary Resonant Commutated Pole, inverters, converters, LMARC, Load Modulated Auxiliary Resonant Current, MCT, Metal-oxide silicon Controlled Thyristors, HM controllers, Hardware Manager controllers, AM controllers, Application Manager controllers, CI, Coordinated Interconnect, control, thermal losses

Abstract: The PEBB program, sponsored by the Office of Naval Research, seeks to develop a general-purpose power controller capable of performing numerous electrical power conversion functions simply through software reconfiguration.

Gradniki močnostne elektronike: pregled

Ključne besede: elektronika močnostna, PEBB gradniki elektronike močnostne, rezultati razvoja, topologije vezij, vezja elektronska, THD popačenje harmonsko totalno, PWM stikala z modulacijo širine impulzov, ZVT prehod pri napetosti nič, ZCT prehod pri toku nič, ZVS preklapljanje pri napetosti nič, ZCS preklapljanje pri toku nič, ARCP pol komutirani z resonanco pomožno, inverterji, pretvorniki, LMARC tok pomožni resonančni moduliran z bremenom, MCT MOS kovina-oksid silicij tiristorji krmiljeni, HM krmilniki kot vodje hardware-ski, AM krmilniki kot vodje aplikacijski, CI povezave medsebojne koordinirane, krmiljenje, izgube termične

Povzetek: V članku je podan kratek pregled rezultatov razvoja gradnikov močnostne elektronike, ki ga je inicializiral Urad za raziskave pri ameriški vojni mornarici (ONR: Office of Naval Research). Za cilj so si zastavili razvoj pretvornikov, ki jih zgradimo s preprosto, standardizirano povezavo standardnih elementov podobni gradnji z lego kockami, katerih funkcionalnost določimo z vpisom ustreznega algoritma delovanja. Iniciativa sicer zrcali potrebe in načrte ameriške vojne mornarice, kot je program »more electric ship« in drugi, vendar je njegov cilj mnogo širši: razviti novo filozofijo načrtovanja, razvoja, gradnje, proizvodnje in uporabe naprav močnostne elektronike, kot tudi distribucije električne energije v raznih avtonomnih sistemih. Program sicer še ni sprožil serijske proizvodnje gradnikov, ne vzpostavil novih standardov na področju močnostne elektronike, je pa že prinesel nove elemente kot so MOS krmiljeni tiristorji, nova paradigma v krmiljenju močnostnih stikal, ki vključuje tudi digitalni komunikacijski sistem, pametne senzorje in digitalno obdelavo signalov.

1. Introduction

The power building block (PEBB), initiated by Office of Naval Research (ONR), is promising enabling technology which will promote future electrical power systems. A PEBB is concept of building a larger power processing system from relatively small number of standardized units which have high degree of intelligence and control autonomy, and which are themselves built from smaller standardized units with some, but less intelligence and autonomy, which in turn also can be but by even smaller, elementary blocks and so on /1-4/. Therefore a PEBB is not some specific block, but rather a building block concept. It starts from the smallest block, i.e. smart switches, smart sensors, etc, which are used to build smart power processing units, e.g. inverters, rectifiers, motor drivers, solid-state circuits breakers, etc. These power-processing units are combined to provide more complex function, or a single function but with higher power rating than each individual unit.

At any level, a PEBB module has form depicted in Fig. 1. This concept makes difference to classical design of power processing devices in following:

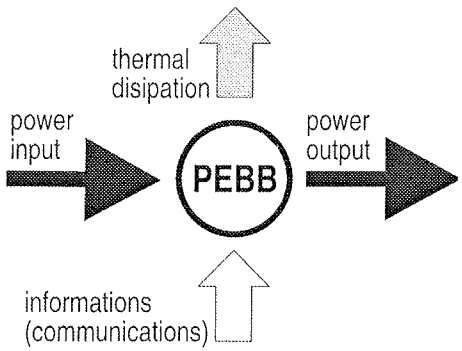


Fig. 1: PEBB module interfaces

1. Every, even the simplest module has some intelligence and includes some communications capability,
2. Physical properties at each of the four interfaces (connectors, screws, surfaces, etc) are standardized for each PEBB power level. Planed are three power ranges:
   a. Low Power 10 kW to 100 kW
   b. Medium Power 100 kW to 500 kW
   c. High Power 500 kW to 10 MW
3. Electrical properties at each interface should be standardized,
4. Compatibility of all modules that connect at the some interface is guaranteed a priory.

The initial intent of the PEBB program was to development or fosters the development of a family of power electronic modules that can be used in 80% of the power conversion and power control applications in the commercial and military world. The technical goals for the PEBB were as follows:

1. Size and packaging, for example, a 250 kW single-phase PEBB module should be fit in a volume roughly the size of a shoebox without the output filter circuits but with built-in provision for thermal management.
2. Power conversion efficiency greater than 98%.
3. Output power quality less than 5% Total Harmonic Distortion (THD).
4. Electromagnetic Interference (EMI) levels below those specified in Mil Std 46.

It is the objective of the PEBB program to promote innovative development of a family of power electronic devices that satisfy the PEBB goals. Furthermore, this program likes to stimulate and support competing ideas in order to advance the state of the art and produce the best possible PEBB modules /5,6/. Of course, main goal is to have PEBB modules produced in the US by US manufacturers.

2. Topology

For electric power conversion a different kind of switching converters are employed. Their switches are implemented by one of three basic switch topologies (Fig. 2), which together with switching control must guarantee the elementary safety operation: no shorted voltage source, no open current source. Analysis of power converters topologies show, that medium and high power converters are built up from different interconnected half-bridges (Fig. 3). Further, the control of switches in half bridge is very tied: if one is in on state, the other one has to be in off state.

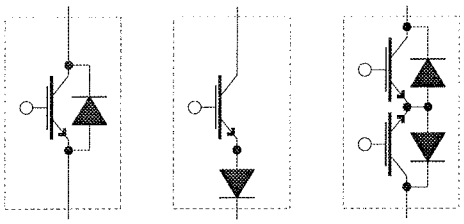


Fig. 2: Basic switches topologies. From left to right: voltage unidirectional, current unidirectional and bi-directional.

2.1. Impact of soft switching techniques

Reduction of thermal dissipation is very important issue in integration of PEBB elements into compact peace of hardware. Meanwhile the contribution of static losses is reducible only by inventing a new semiconductor switches, the switching losses can be reduced also with appropriate modulation techniques as well as with use of soft switching. So far, many soft switching topologies have been proposed to reduce the switching loss and improve the performance of converters. All have been evolved from resonant converters, quasi-resonant converters, multi-resonant converters, soft switching PWM converters including zero-voltage transition (ZVT) and zero-current transition (ZCT). They can be classified be classified into two categories: zero voltage switching (ZVS) and zero-current switching

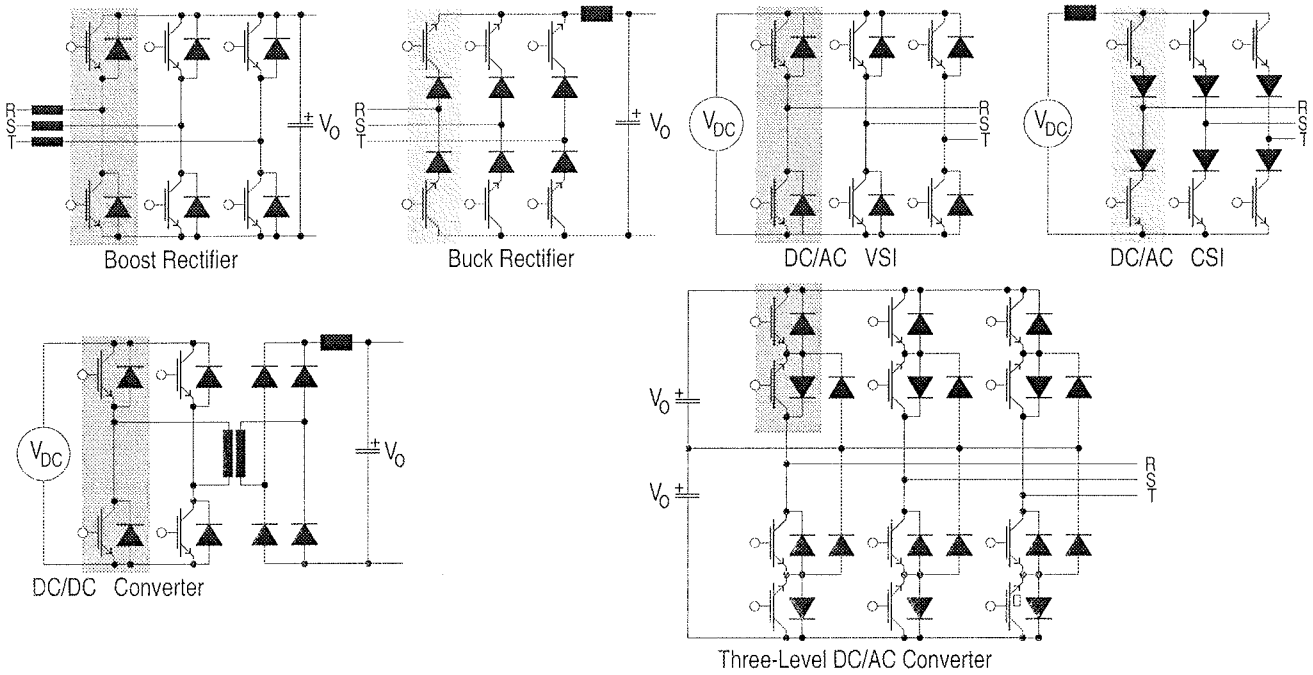


Fig. 3: Identification of a PEBB Switching cell: The commonality in the power converters is presented as the shaded block

(ZCS). ZVS reduces the switch turn-on loss by forcing the switch voltage to zero prior to its current flowing, while ZCS reduces the turn-off loss by forcing the switch current to zero before its collector-emitter voltage increases from zero to turn-off static value. For medium to high power applications, ZVT and ZCT are more suitable than other soft switching techniques, since they combine the advantages of PWM control (i.e. minimum switch static voltage/current dynamic and minimum circulating energy), and the advantages of soft switching techniques, i.e. low switching loss and low dynamic transition.

2.1.1. ARCP inverter

The ARCP (Auxiliary Resonant Commutated Pole) inverter belongs to ZVS family of soft switching inverters /6/. In its topology (Fig. 4), the voltage across each phase switch (S_1 and S_2) is driven to zero just prior to its turn on. This is accomplished by generating a resonant current pulse that drives the voltage across the switch to zero. The resonant pulse is formed when auxiliary switch (AC) consisting from switches A_1 or A_2 is turned on just prior to turning off a phase switch.

A detailed description of ARCP operation can be found in reference /7/. Briefly its operation can be described as follows. When the AC switch is gated on, a current begins to rise linearly through the resonant inductor L_R in the conducting phase switch. When the phase switch is turned off, the current resonates based on the resonant component values and then falls back to zero. The peak resonant current depends on the following (see Fig. 6):

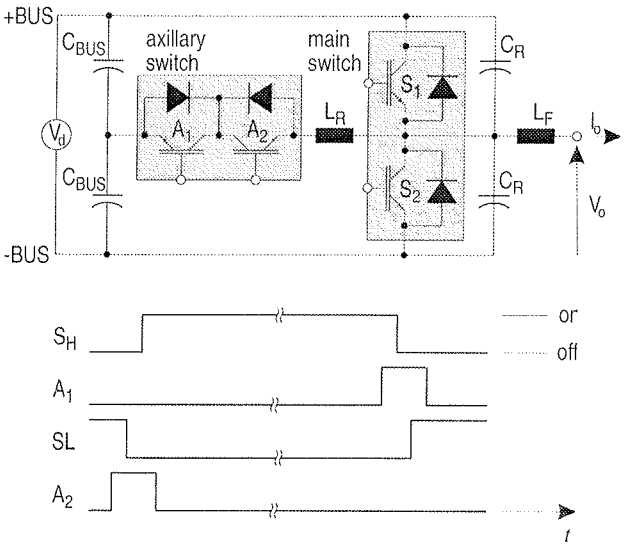


Fig. 4: ARCP schematic and switching timing

- Length of time that both the AC and the phase switch are turn-on simultaneously (overlap time)
- Input bus voltage
- Resonant component values (L_R and C_R)

For AC switches in ARCP inverters the MCT (MOS Controlled Thyristors) have been developed and provided under the ONR PEBB development program. These devices can withstand high dv/dt and di/dt stresses making them ideal candidates for use as AC in the ARCP topology.

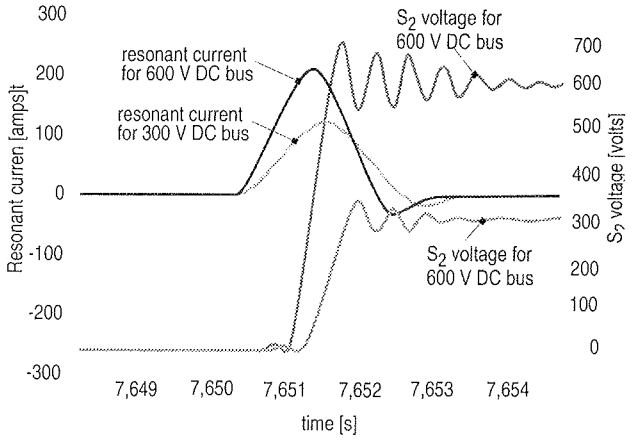


Fig. 5: ARCP Resonant Transitions.

Efficiency of ARCP inverters strongly depends on resonant pulse control. Minimization of resonant energy required for soft switching can be achieved by introducing of a smart control with self-tuning the overlap time to the actual input DC bus voltage and actual load current. Example of smart control is LMARC (Load Modulated Auxiliary Resonant Current) control algorithm reported in reference /6/. LMARC determines overlap time according to the instantaneous load currents. To insure zero voltage transitions the adequate safety margins, i.e. more resonant energy than what is theoretically needed is maintained. LMARC also considers the facts that the magnitude and direction of the instantaneous load current flowing through a main switch or diode can help or hindrance of resonant transitions.

2.1.2. ZCT converters

A ZCT PEBB can be regarded as the combination of two soft switching cells. One of them is shown within the shaded area in Fig. 6. The relationship between the main switch and its corresponding auxiliary switch in one PEBB topology is diagonal. This means the timing control of A_L is related to S_H. On the other hand, A_H is related to S_L. The key waveforms and the control timings are shown in Fig. 7, analysis of improved ZCT can be found for example in /8,9/. Let be emphases, that ZCT only help the switching transition, so the power converters with ZCT operates according to PWM rather than switching transition. So the controller design is almost the same as at the hard switching converters.

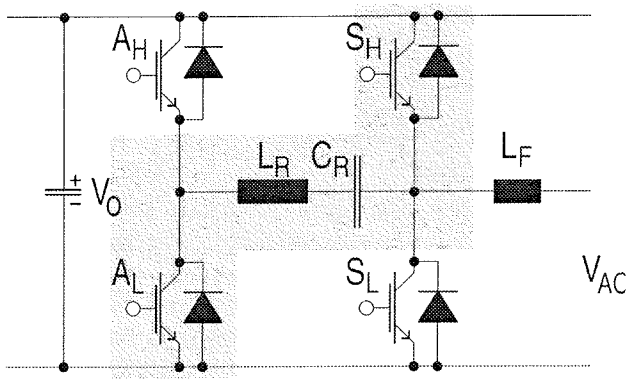


Fig. 6: Topology of one ZCT PEBB power stage for boost rectifier

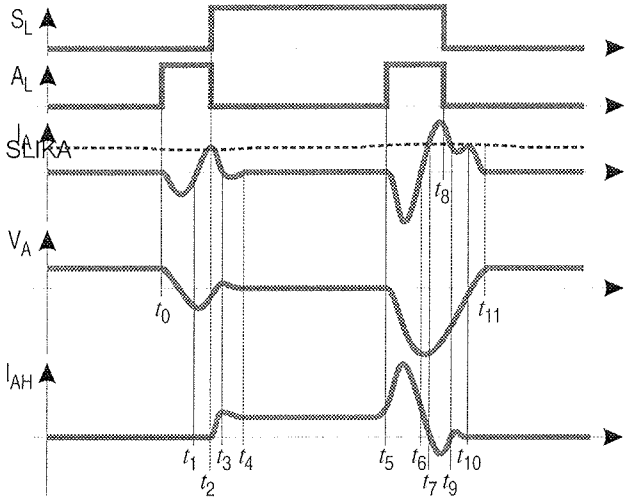


Fig. 7: Operation waveforms for the improved ZCT

3. Control and communication isues

The control of PEBB is divided into two parts:

1. Controller of power stage of PEBB, which was named *Hardware Manager* (HM), and
2. Controller of PEBB's applications, which was named *Application Manager* (AM).

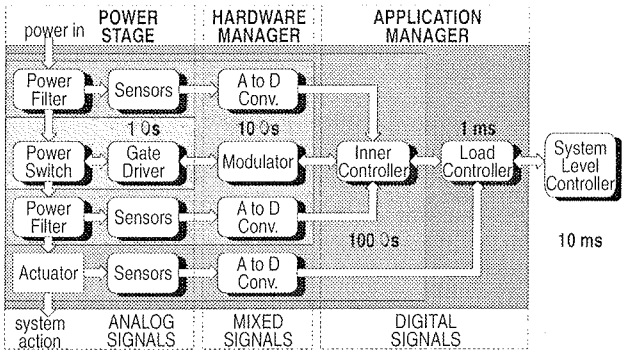


Fig. 8: PEBB module interfaces

In the beginning to HM belongs pulse-width modulator and analog-to-digital converters preparing data for AM (Fig. 8). For AM has been proposed cascade controller structure. The concerns of inner loop are electric variables like input/output voltages and currents, the outer loops concern are load variables, for example motor torque and angular velocity. This solution needs numerous noise sensitive signal lines between HM and elements of PEBB. This was eliminated by further development of PEBB concepts where in PEBB control was introduced smart sensors generating data instead of signals and smart gate drivers capable converting digital commands into adequate drive signals. In this concept modulator and AM vas merged into universal controller (Fig. 9), HM and AM communicate over fast serial bus interface (Fig. 10).

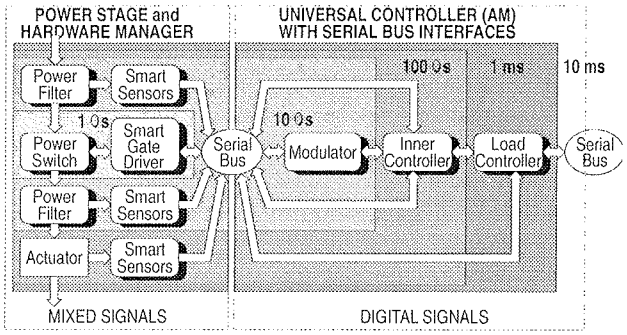


FIG. 9: Universal controller with serial bus interfaces

Serial communication between HM and AM has specifics not found in existed industrial communication systems. As it is on one hand very simple and mostly performs cyclic traffics, on another hand it had to be very fast, has very low synchronization jitter and should be reliable.

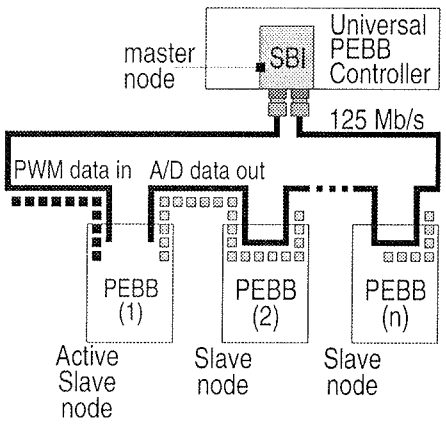


Fig. 10: Inter PEBB and UPC communication

4. Interconnections

Interconnection of a PEBB's components into compact device is one of a major issue of PEBB initiative. There arise lot of problems because only in rare cases it is possi-

ble to connect one component directly to the adjacent component. The stray inductance and capacitance of the interconnection, which are often impossible to determine in advance, consequently accurately modeling of the converter is not possible. This leads to a lot of unnecessary laboratory experimentation during the interconnect development. Furthermore, components are not mechanically interchangeable, requiring sole sourcing of many components. One of solutions for above problems is proposition for a system called *Coordinated Interconnect* (CI) /10-11/, which by a change in component terminations philosophy can greatly improve converter design and construction. New philosophy emphases the component terminations should not govern the interconnect design, rather the interconnect design should govern the component terminations. Proposed CI eliminates the wiring harness and busses typical of present-day converters. The concept of CI is to integrate a section of laminated bus, or at least a bus-like structure into each component. The bus is terminated with a bus edge connector which mates directly to the bus edge connector of the adjoining component. Consequently all interconnect stray elements are included with the components and are characterized as part of the component data sheets. Therefore modeling of the converter prior to construction is greatly simplified. Furthermore, components of various types are mechanically interchangeable with each other. Finally the concept of CI allows replacement of a single component without disturbing other components or connections.

Designing CI the selection of the number of layers is a key decision. Since CI should be carried throughout the converter, both the ac and dc sections of the converter should use CI. In the dc section buses often require a "+" layer, a "-" layer, and a midpoint or "0" layer. Coincidentally, the ac section of a three-phase converter requires three layers for phases *a*, *b*, and *c*. Therefore was proposed a three-layer system, which could easily be reduced to a two-layer or enhanced to four or more layers. As shown in Fig. 11, a vertical tab terminates each of the three horizontal bus layers. Each tab occupies a width W and is isolated from its neighbor by separation S. The bus thickness determines the tabthickness T. The bus thickness depends on component design and can be different for different components. All tabs must extend above the baseplate by a uniform elevation E. Therefore; the tab height H actually can vary depending on the distance between the bus layers and the baseplate. The contact area between the two tabs is the product of W and H. Three-tab bus edge connector has not centerline axis symmetry. Lack of symmetry introduces in the converter layout certain constraints like orientation in component placing. The symmetry is achievable by five-tab bus edge connector (Fig. 12), but requires five connections between adjacent components. Beside of increased it has a total of 4S separation between tabs compared to a total of 2S separation between tabs for the three-tab design. The additional separation reduces the contact area and could be a limiting factor if S is large.

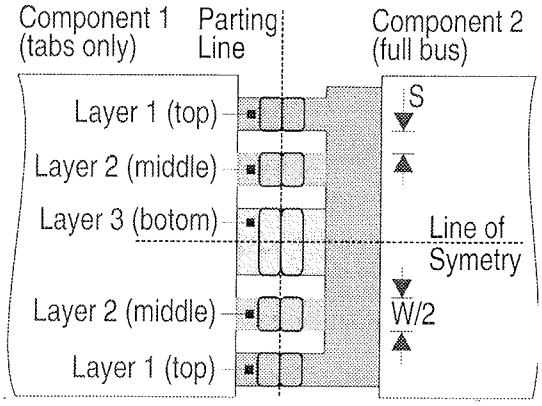


Fig. 12: Five-tab bus edge connector for three-layer bus.

Many different techniques could be used to fasten the tabs to each other. Fig. 13 shows three example methods. Traditional bolt, washers, and nut (Fig. 13a) are not convenient for mounting, more convenient is use of a spring steel clip, which can be inserted from above with minimum clearance on either side (Fig. 13b). Similarly is with the screw-driven wedge (Fig. 13c). By it is possible to connect multiple tabs simultaneously. Those connections can be made and unmade. Permanent connections such as crimping are also easily envisioned.

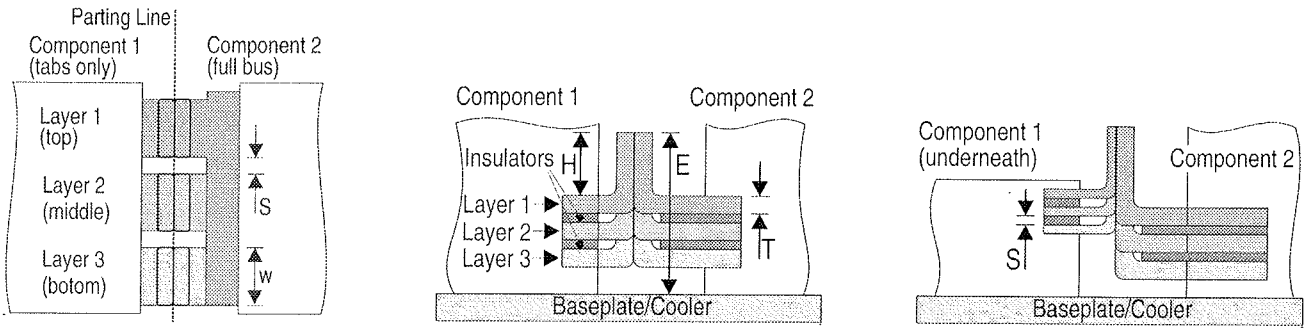


Fig. 11: Three-tab bus edge connector for three-layer bus: (a) top view, (b) edge view with coplanar bus layers, (c) alternate edge view with non-coplanar bus layers and buses of differing thickness.

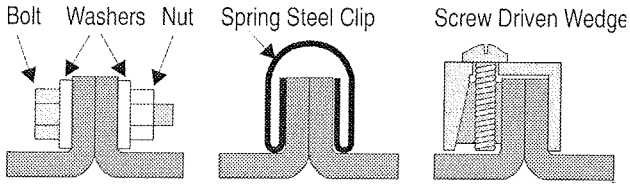


Fig. 13: Methods to fasten tabs of bus edge connector.

For wide acceptance of CI sine qua non condition is standardization of CI. At least should be standardized measures E, S, H_{min}, W and position of holes in edge connectors. It can be expected that those measurements will be grouped in power classes like PEBB's. Since no currently available components use CI, it would be developed in phases with various components making the transition when possible. Advanced technology components would use CI as an integral part of the component design, for others adapters would be used to make the transition however. Example of it for electrolytic capacitor is illustrated in Fig. 14.

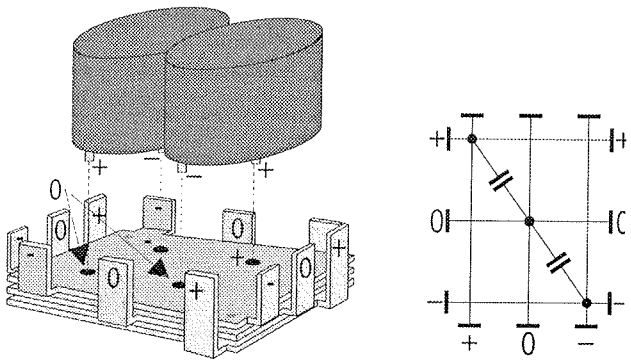


Fig. 14: Three layer bus adapter for electrolytic capacitor. Terminals allow the capacitor to connect to either "+" and "0" layers or "–" and "0" layers.

5. Packaging Issues from a Thermal Perspective

Integration of PEBB's components, determined by circuit topology, into compact device depends very much on voltage, current and the amount of waste heat generated. By CI the problems with voltage and currents influence on package is seems to be efficiently solved, but for wasted heat is likely that the common methods of cooling have already reached their limit. To improve performance the waste heat has to be taken out more efficiently. The sketches below outline the various topologies that can be considered for packaging a power electronic switch. Each of the following drawings is laid out in the same basic manner to emphasize the similarities and differences of the topology. Each is shown with a generic heat sink (heat exchanger, fluid link and final heat exchanger).

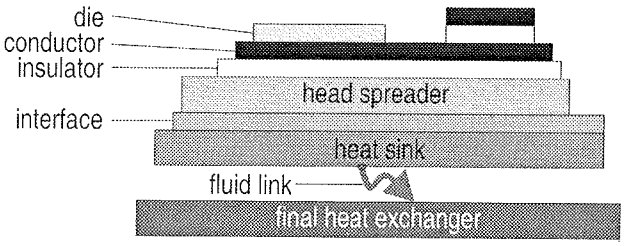


Fig. 15: Conventional heat sink

Fig. 3.1 shows a conventional heat sink topology. It is the most common because of its flexibility. With this topology, the worst is the field interface (on the sketch assigned as interface). Even under the best of circumstances it acts as a thermal barrier. Because of material performance limitations and manufacturing techniques the overall package has a lot of layers in the 'stack', each interface providing a thermo-mechanical problem.

The attached and integral heat sink topology (Fig. 16) are compromise that has been tried a number of times for both single and double side-cooled packages. At integral heat sink the insulator is part of the mechanical structure and overtake the heat spreader functionality, so minimal thermal path from die to heat exchanger seems to make this a near ideal heat management system. Pool and flow boiling as well as spray and impingement using Fluorocarbons all appear to promise very real performance boosts and would be worth development. Therefore the integral heat sink topology is a basis for the temporary phases of PEBB program.

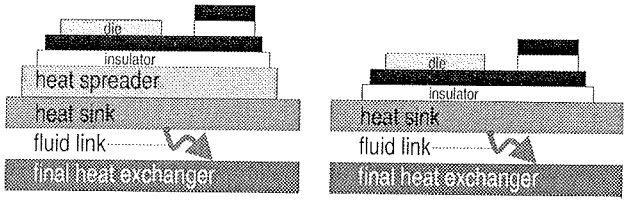


Fig. 16: Attached (left), and integral (right) heat sink.

The double side cooled topologies are complex layout (Fig. 17). They have similar properties as one side cooled counterparts, but with important benefits, that in comparison to them have halved thermal resistance. Unfortunately, those topologies require a new way of connecting the package to the outside world. Fundamental changes in package form, power interface and control connection is required. In thermal sense the best possible thermal performance is feasible by integral liquid cooling (Fig. 18) where the heat exchange liquid is right at the die. Further advantage is that the package does not need to use the expensive ceramics and engineered metals used in conventional high performance module designs. The package can be designed as one large heat exchanger operating at a high temperature. It can be cooled efficiently with forced air. However the performance and size advantages seem to outweigh the need to use special liquids. For future high-

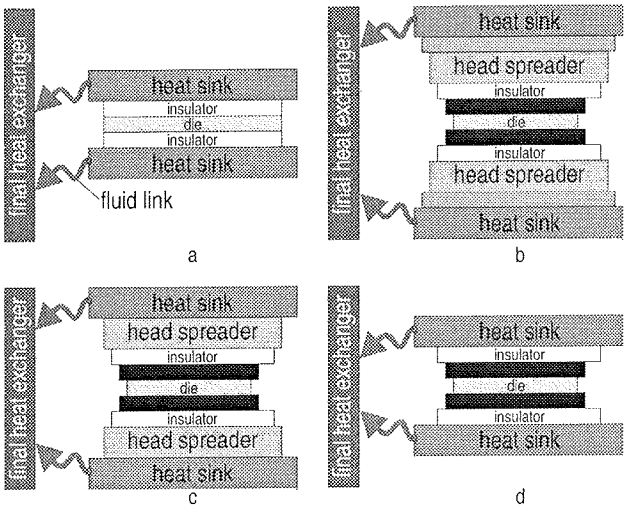


Fig. 17: Double side cooled packages, a: Hockey puck or press pack, b: conventional, c: attached heat sink), d: integral heat sink.

power-density PEBB's this certainly seems to be a promising approach.

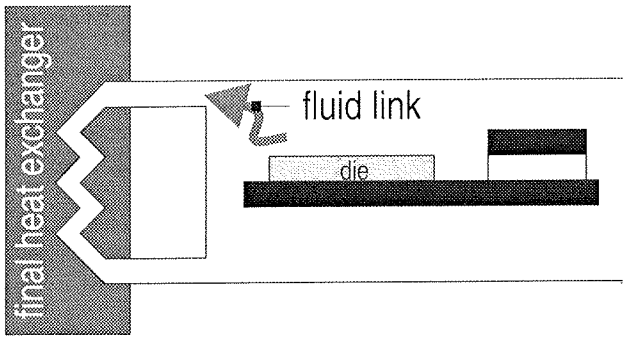


Fig. 18: Integral liquid cooling

Chart in Fig. 19 shows an analysis of efficiency of different cooling systems. In analysis it is assumed that all layers

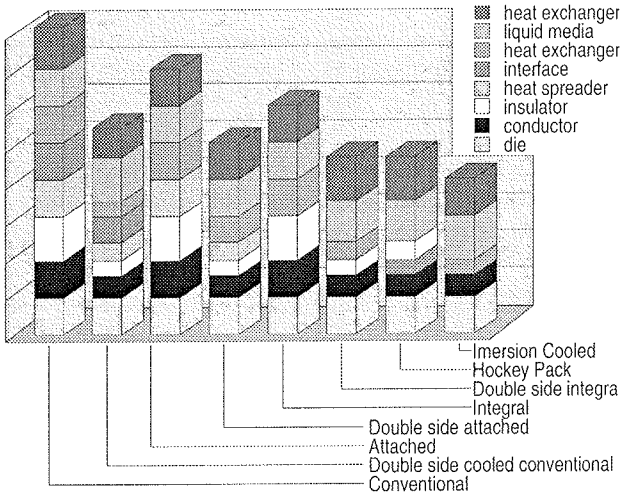


Fig. 19: Comparative Thermal Resistance

have approximately equal thermal resistances. Each single layer in package has full height; doubled layers are half height since they would approximately halve the thermal resistance. This illustration has a lot of simplifying assumptions but hopefully it shows why the 'advanced' module designs are of such interest. This analysis probably understates the performance gains of the more 'advanced' packaging styles. The pivot in packing development is development of packaging materials. For them are many performance parameters of importance, however the primary areas of interest to the PEBB program are thermal issues relating to coefficients, reliability and performance. For reliability the primary driving force is the mismatch of Thermal Coefficients of Expansion (TCE) between layers in a packaging stack. Thermal Conductivity (TC) measured in W/mK reflects the thermal performance/power dissipation. A list of packaging electronic materials with their TCE and TC considering in PEBB program is in Table 1.

Table 1: Electronic materials

	TCE	TC [W/mK]	Type
Thermal grease	~	1	I
Diamond	1	>2300	I
Si_3N_4	2	270	I
BN	4	600	I
CuGrpht MMC	~4	~250	C
AlN	4	180	I
Si	4	160	S
SiC	4	270	S/I
CuMoCu	7	200	C
Al_2O_3	7	23	I
BeO	8	240	I
Cu	18	395	C
Al	24	205	C
Circuit Board	130	0,24	I
AlSiC	180	180	C
Solder (Sn/Pb)	210	36	C/A
Thermal Epoxies	<700	1	I/A

Type codes: I - Insulator, C: Conductor;
S - Semiconductor, A - Attach

All numbers are approximate

Conductors have to be directly bonded to the die at least on one face. Electrical conductivity is a prime parameter but because of the close proximity to the die, their TCE needs to be as closely matched as possible. Electrical insulators are relatively good thermal conductors, but the less expensive ones are generally poor performers in this area. Most ceramics insulators have relatively small TCE's while organics have high TCE's. The cheap organic insulators can be inexpensively formed into complex shapes while

the ceramics are all expensive to form into anything beside flat plates.

Attachment materials are solders and organics. The most common solders are tin/lead alloys and although other mixtures are used fairly frequently, they have somewhat similar characteristics. Organic attachment materials are electrical and thermal insulators; though they can be 'loaded' with other materials that can modify either or both the electrical and thermal properties. Organics can be made to adhere to just about any surface and are generally processed at low temperatures that give them a great deal of process flexibility.

Heat spreaders are the relatively thick, flat base-plates of power modules that provide a stable base on which the components are mounted in conventional modules. They are generally made of copper, provide a good path for heat dissipation, and form a "thermal capacitor" to absorb heat spikes and protect the device when a short-term overload situation occurs. Heat sink/heat exchangers are usually just extruded or machined aluminum. The term heat exchanger is generally used for active devices where hot a low temperature and usually different fluid flowing on the other side cool flowing fluid on one side of an interface. Most heat exchangers are made of aluminum.

6. Conclusions

This paper demonstrates the progression in development of PEBB concept and philosophy. From past research and development can be concluded that PEBB will not have unique topology. Regard to application the hard switch and ZVT or ZVT soft switch versions will be available.

The control of power electronics in future will be split into part integrated into PEBB, which in collaboration with smart sensors and gate drivers will control PEBB behavior and will be through fast serial digital communication linked with application control. This communication will have the same importance as have I^2C in connections of chips.

The power electronics would benefit enormously if the industry of elements used in power electronics will accept system of Coordinated Interconnect just as the computer and other digital industries benefited from the dual inline package (DIP) and subsequent surface mount devices. But that this will happen many important challenges must be met.

Thermal aspects of PEBB's packaging give insight in problems of integrating PEBB into compact device. From brief overview of packing technologies can be concluded, that integral heat sink technology is basis of temporary phases of PEBB program. In future, when high temperature devices like SiC elements will be available at reasonable cost, it seems that integral liquid cooling will prevail. For this cooling a long way of searching for materials with appropriate TCE is still to be passed.

7. References

/1/ D. Boroyevich: Some control, communications, and modeling Issues for PEBB based power distribution systems. White paper as part of the Control and intelligence systems control of ONR PEBB control technology workshop, 1995

/2/ K. Drew, "PEBB technology development and cost assessments benchmark as of October 9, 1998, ONR, code 36 (http://pebb.onr.navy.mil)

/3/ G. S. Thaudi: *Modeling, control and stability analysis of a PEBB based DC distribution power system.* M.Sc. thesis, VPI&SU Blacksburg, Va., 1997

/4/ T. Ericson, A. Tucker, D. Hamilton, G. Campisi, C. Whitcomb, J. Borraccini, W. Jacobsen: *Standardized power switch system modules (power Electronics Building Blocks).* Power systems world '97, 1997 (http://pebb.onr.navy.mil)

/5/ J. Borraccini, W. Ruby, T. Duong, D. Cochran, E. Roth, D. McLaughlin, T. Ericsen: *Demonstration of Power Electronic Building Block (PEBB1) Function, and Plans for PEBB2 and PEBB3.* Report (http://pebb.onr.navy.mil).

/6/ W. Ruby, R. Cooley, J. Borraccini, M. Cannell, J. Sullivan, J. Baker, R. Sigethy, G. McKibben: *Power Electronic Building Block design and hardware demonstrator - results from December 1996 through May 1998.* (http://pebb.onr.navy.mil)

/7/ R. W. DeDonker: "Resonant Pole Converters". EPE-93, Ch. 4, p 4-1 through 4-44, 1993

/8/ J. Mayer: *Analysis of Zero-Current Switching Topologies and Strategies for the Power Electronic Building Block.* Final Technical Report for Naval Surface Warfare Center, February 1998

/9/ A. W. Kelley, M. Harris, D. Hartzell, and D. Darcy, "Coordi-nated Interconnect: A Philosophical Change in the Design and Construction of Power Electronic Converters, 33rd IAS Annual Meeting, 1998, St. Louis, Missouri, USA, pp. 1105-1110.

/10/ A. Kelley, M. Harris, J. Cavaroc, M. Jones, R. Linkous, D. Hartzell, D. Darcy: "Bus connector for coordinated interconnect laboratory measurement and finite element simulation" APEC, Dallas, Texas, 1999, pp. 325-331.

/11/ W. A. Stinnett: *Thermal management of power electronic building blocks. M.Sc, thesis,* VPI&SU Blacksburg, Va., USA, 1999.

/12/ J. Borraccini, W. Ruby, R. Cooly, M. Cannel: *Calculation of power density of PEBB 1.5 based ARCP electrical power converter.* 1998 (http://pebb.onr.navy.mil).

/13/ P. N. Harrison, R. W. Garman, "PEBB Thermal Baseline Study Test Plan," A&T Engineering Technologies, VECTOR Research Division (July 8, 1998).

/14/ P. N. Harrison, R. W. Garman, "PEBB Thermal Management Final Report," A&T Engineering Technologies, VECTOR Research Division (May 1999).

/15/ Jia Wu, Heping Dai, Kung Xing, Fred C. Lee and Dushan Boroyevich: Implementation of a ZCT soft switching technique in a 100 kW PEBB based Three-phase PFC rectifier, IEEE conference PESC'99, reprinted in 1999 *Annual Power electronic seminar, Virginia Tech, Blacksburg, USA*

Žarko ČUČEJ
Univerza v Mariboru
Fakulteta za elektrotehniko, računalništvo in informatiko
Smetanova 17, 2000 Maribor-SI
e-mail: zarko.cucej@uni-mb.si

Prispelo (Arrived): 24.03.01 *Sprejeto (Accepted): 01.06.01*

A STUDY OF THE LIMITS OF SPIN-ON-GLASS PLANARIZATION PROCESS

R. Osredkar
Faculty of Computer Sciences and Faculty of Electrical Eng.,
University of Ljubljana, Slovenia

Keywords: semiconductors, microelectronics, IC, Integrated Circuits, topography planarization, SOG films, Spin-On Glass FILMS, production, process modeling, PECVD, Plasma-Enhanced Chemical Vapour Depositions

Abstract: Results presented in this paper demonstrate that global planarization with a SOG planarization process can not be achieved. However, local planarization on a predetermined site on a patterned wafer is possible, with a planarization factors of 0.81 for a single step process, 0.86 for a double step process, and 0.90 for a triple step process. Such planarization involves repeating the deposition and densification steps of the SOG material several times, and can be accurately modeled by a simple model described.

Študija omejitev planarizacijske tehnike s tanko plastjo tekočega stekla (SOG)

Ključne besede: polprevodniki, mikroelektronika, IC vezja integrirana, planarizacija topografije, SOG plasti tanke stekla tekočega nanesenega centrifugalno, proizvodnja, modeliranje procesov, PECVD nanosi kemični s paro plazemsko izboljšani

Povzetek: Rezultati predstavljenih meritev kažejo, da je globalna planarizacija topografije na silicijevi rezini izven dosega metode planarizacije s tanko plastjo tekočega stekla (SOG). Vendar pa se z metodo, na določenem mestu na rezini, da doseči lokalno planarizacijo, s planarizacijskimi faktoji 0.81 za enostopenjski proces, 0.86 za dvostopenjskega in 0.90 za tristopenjskega. Takšen večstopenjski planarizacijski postopek zahteva večkratno, zaporedno nanašanje in utrjevanje SOG planarizacijskega materiala in ga je možno natančno opisati s preprostim modelom planarizacije, ki je tudi opisan.

Introduction

Device planarization, i.e. reduction of distances between topography and reduction of the side wall slopes in order to facilitate subsequent processing steps, is an important consideration in IC fabrication technologies where circuit features are scaled to submicron dimensions. It is most critical during the final steps of fabrication, when several metallization and dielectric layers are deposited, and is used primarily to enhance step coverage of these layers. Often only partial planarization (smoothing of topography), with limited step heights reduction is sought /1,2/. However, sometimes complete local planarization is required, and even complete global planarization, where the surface of the wafer is completely planarized over arbitrary topography. The latter requirement arises e.g. in LCD technologies where the globally planarized wafer surface is the lower electrode of a LC display /3/ or in ferroelectric memory devices /4/.

There are several planarization techniques used in IC processing /5/. Physical methods include polishing, which is usually applied where complete and global planarization is required, and different techniques where planarization of existing dielectric layers is attempted by film reflow, etch-back of sacrificial layers etc. Fluidic planarization techniques utilize low viscosity of certain materials, e.g. photoresists, polyimides and spin on glasses (SOG), which can fill the trenches in wafer topography. These methods are simple to apply and usually require low processing temperatures (below 400 °C). However, compatibility of the fluidic materials with the standard dielectric materials is a serious concern, and, as a rule, only limited planarization can be achieved by such methods. In this contribution the limits of the SOG planarization methods are studied and described.

Experimental

Planarizing characteristics of the Allied Chemicals Accuglass series 204 SOG material were studied. SOG films were deposited on 4" wafers on a Semiconductor Systems Inc. System One modular coater with an on-line drying oven, at 3000 r.p.m. and the deposited film dried at 100 °C for 60 sec. Resulting film was 315 nm thick, with better than 1 % ($\pm 1\sigma$) wafer to wafer repeatability in uniformity. Densifications were performed in a Blue M, model IGF 206B-3 furnace, in a nitrogen atmosphere. A Semix Tazmo model TR 6132U (D) coater, with 3 ovens, was also used at later stages of the work, eliminating the need of a separate oven for low temperature (305 °C) densification. High temperature densification (900 °C) was performed in the Blue M oven in all cases. The results of planarization processing were photographed on a Hitachi model 405 scanning electron microscope and photographs analyzed.

The patterned wafer topography was simulated by a pattern of 10 parallel aluminum lines on field oxide. The lines were 2.5 μm wide, 0.35 μm thick (i.e. step heights 0.35 μm) spaced 1.5 μm apart (i.e. at 4.0 μm pitch), 3 μm, 4.5 μm, 6 μm, and 7.5 μm apart. All planarization factor data presented are an average of 5 measurements on 5 different wafers, with 2 % (± 1σ).

Results and discussion

Rapid evaporation of the solvent from the SOG material during the deposition process challenges detailed analysis and prediction of the degree of planarization possible with such a process. A quantitative measure of the step-height reduction, referred to as the planarization factor β, is given by

$$\beta = 1 - (t^f_{step}/t^i_{step}) \quad (1)$$

where t^f_{step} and t^i_{step} are the final and the initial step heights, respectively. In complete planarization β = 1 and 0 if no planarization exists.

The rheological (fludic) deposition model, which is often used in analysis of the spin-on processes and is based on the Navier–Stokes equations /5/, suggests that covering a patterned wafer with a fluid film (SOG, photoresist or polyimide) results in a completely flat top surface of the film, which remains flat until a considerable amount of solvent is removed from the material. After the removal of the solvent only non-volatile components of the film material remain on the wafer surface. If the proportion of the non-volatile components in the SOG material is k, the planarization factor achieved during the evaporation of the solvents is simply β = k, regardless of the thickness of the deposited planarizing film and the resulting partially planarized wafer topography still reflects the underlying topography. In case of Accuglass 204 SOG material, which contains 10 % of nonvolatile components (as specified by the producer), a maximal planarization factor of β_{id} = 0.1 could thus be expected, as a result of drying of the material. However, this would only be true if during evaporation of the solvents no gross transport of the planarizing material, driven by the surface tension, occurred. This is clearly not the case: in dense topography we have been able to achieve β as high as 0.83 (depending on the details of the wafer topography), and less than 0.1 on isolated lines or lines separated by more than 4 to 5 μm. This indicates that the transport of the planarizing material during evaporation of the solvents plays an important role in the SOG planarization process.

The quality of the surface underlying the planarization film also effects the planarization process and is also not predicted by the rheological model. A SOG film deposited on a bare, flat silicon wafer is not uniform across the wafer: it is generally 1.2 % thicker on the wafer center than on its edge. The situation is reversed on films deposited on wafers covered with a 1.3 μm thick PECVD oxide film, which also has a flat surface: in this case the SOG film is 2.7 % thinner in the center of the wafer. Also, at identical coating conditions, average thickness is 3,5 % less than on the bare wafers. SOG films deposited on patterned wafers (patterned aluminum on field oxide) simultaneously exhibit surface and topography effects: their thickness similar to those on PECVD oxide, with a 8.8 % reduction of thickness in the center. These effects are quite reproducible and are several times larger than the pertaining standard deviations of the film thickness as measured at standard positions on the wafers /6/. We conclude that both the surface quality and its structure have important influence on the local thickness of the deposited SOG films, precluding total global planarization with such a process. However, locally the topography effects prevail, which makes partial, local planarization possible.

Another difficulty in analyzing in detail the SOG planarization process arises from the rapid drying (evaporation of the solvents) and the associated thinning of the SOG film at 100 °C, the recommended temperature for this stage of processing. No further thinning due to evaporation of the solvents can be observed after only 60 sec, which makes it difficult to measure the original film thickness, unless depositions and thickness measurements are performed in an atmosphere saturated by the solvents. Such measurements have been attempted with inconclusive results: they suggest an as-deposited film thickness of 4μm, which can be compared to 5.6 μm, the result of a calculation based on the rheological model, material and the deposition parameters.

As a consequence of the high volatility of the solvent system used the SOG material, the amount of solvent evaporating during the spinning and the formation of the film is considerable, thereby rapidly and locally changing the surface tension and viscosity of the spun-on material. The surface diffusion model of the planarization process, which is often used to model planarization by reflow of doped glass and is conveniently accessible in different simulation packages (e.g. SAMPLE), is therefore unsuitable for simulations of the SOG planarization process. Detailed modeling of the planarizing properties of the liquid SOG material is therefore difficult and only semi-empirical attempts in this direction have been published /7/.

After initial drying the behavior of the SOG film becomes well predictable /6/. During densification at 305 °C initially some further expulsion of the solvents from the pores of the film is observed, resulting in thinning of the film in an exponential manner, with a characteristic time of 0.50 hours. After this initial thinning, densification proper of the film can be observed; it also follows an exponential curve, with characteristic time of 1.3 hours. After 3.5 hours of baking at 305 °C the SOG film thickness does not decrease further appreciably. The quality of the deposited film is determined exclusively by the second stage of the densification and results in a porous film. Further heat treatment at a higher temperature reduces the porosity /8/, however if the planarization is applied at a stage where a

metal (aluminum) film is present on the wafer, the possibility of densification at elevated temperatures is strictly limited. Densification at 900 °C removes all traces of silanols and H_2O from the film, as has been demonstrated by IR spectroscopy /9/, but still does not eliminate porosity completely. This is illustrated by our rehydration experiments in which freshly densified films at this temperature were exposed to an atmosphere saturated with water and from which the films can reversibly adsorb H_2O. The degree of water adsorption has been monitored by measurements of the dielectric constant of the SOG film, which ranges from 4.6 in a dry film densified at 900 °C to 8.3 in a rehydrated film. These results closely correspond to those reported previously /10/ and indicate that moisture content (and possibly silanol content) in SOG films can be, due to possible reactions of the moisture from the film with the aluminum, potentially a serious source of quality degradation problems /11/.

In modeling of the planarization factor of the two stage densification process at 305 °C, the initial thinning due to expulsion of the solvents from the film can be, without appreciable loss of accuracy, neglected, and only the characteristic thinning time of the second stage considered. This is due to the relatively small change in the film thickness during the initial stage and the long densification times of the second one. The planarization factor for the densification step only, at specified temperature, is $\beta_d = 0.90$. Thus the compound planarization factor for the initial drying and densification is

$$\beta = \beta_{id}\, \beta_d$$

and depends strongly, as described above, on the topography: it is 0.09 for isolated lines and 0.81 in case of 0.35 μm step heights of 2.5 μm wide lines with 4.0 μm pitch.

Attempts at panarization with 2 subsequent SOG depositions revealed that a SOG film dried at 100 °C is readily attacked by the solvents in the SOG material itself and is partially removed during the second deposition. This is demonstrated by the compound thickness after drying which increases by only 50 %, and a resulting β_{id}, which is, in case of isolated lines, not significantly different than that of one deposition only. The influence of the substrate topography on the double film planarization factor is even greater than in single film case, probably due to the fact, that the material in the trenches between the lines is less accessible to the solvent than the more exposed material. However, no regularity in the planarization factors could be observed for such a process and we therefore conclude that this is not a viable planarization procedure.

Deposition of a second film after densification of the first one (at 305 °C) resulted in doubling of the compound film thickness and an increase in the planarization factor β from 0.81 to 0.86, an increase of 6.2 %. This increase can be modeled by replacing k, the proportion of the non-volatile components in the SOG material, in the expression for β, by a related empirical parameter f. This characterizes the dynamic drying-out and densification processes by their end results, i.e. the thinning of the planarizing film at a particular site on the wafer, and thus takes account of all the effects governing the film thinning process at the site. f has to be determined experimentally. If the ratio of the f parameters, describing the reduction of the deposited SOG film thickness under and on a step of initial thickness t^i_{step}, is taken to be proportional to the step heights:

$$r = f_{under}/f_{on} = a \,.\, t^i_{step} + 1$$

where a depends on the details of the topography to be planarized, the resulting planartization factor of a multiple-step planarization process can be predicted for a predetermined site on the wafer. In case of parallel lines of the above mentioned dimensions, and for the Accuglass 204 SOG material, a = 7.1 and the model predicts a planarization factor β = 0.86 for a double deposition of the SOG planarization material, and 0.90 for a triple deposition. Both values agree well with our experimental data. Reasults are summarized in Table 1. However, such an empirical model can only be used for determining β on a predetermined site on the wafer, with specified topography. It is of little value for estimating the degree of global panarization across the wafer. Further, multiple-step planarization is a process of diminishing returns and total planarization, even locally at a predetermined site, may not be a realistic goal of such a multi-step process.

Conclusion

A detailed understanding of the planarization process is required to design a planarization process which results in the required degree of planarization of a production wafer. Our results demonstrate that global planarization with a SOG process is extremely difficult, if not impossible, to achieve, but local planarization with a planarization factor of 0.9 is certainly within its reach. Such a process involves repeating the deposition and densification steps of the SOG material several times, and can be, for a predetermined site on a patterned wafer, quite accurately modeled by the simple model described.

Acknowledgements

The use of IMP (San Jose, Ca., USA) facilities for some of the experimental work is gratefully acknowledged. The study has been supported by a grant from the Ministry of Science and Technology of the Republic of Slovenia.

Table 1. Planarization factors after different stages of SOG planarization process

Planarization stage	planarization factor
deposition (including evaporation of solvents at 100 °C, β_{id}): isolated lines	0.09
deposition (including evaporation of solvents at 100 °C, β_{id}): dense topography	0.9
double deposition with no densification: isolated lines	~ 0.1
double deposition with no densification: dense topography	~ 0.8, not repeatable
densification (β_d)	0.9
compound ($\beta_{id} \cdot \beta_d$): dense topography	0.81
double planarization: dense topography	0.86
triple planarization: dense topography	0.90

References

/1/ S. Wolf, Silicon Processing for the VLSI Era, Vol. 2 - Process integration, Lattice Press, Sunset Beach, Ca. USA, 1990, p. 191

/2/ P. B. Johnson and P. Sethna, Semiconductor Int., Oct. 1997, p. 80

/3/ J. Pirš, IJS, private communication, 2000

/4/ Suk-Kyoung Hong et al., Intermetal Dielectric Process Using SOG for Ferroelectric Memory Devices having $SrBi_2Ta_2O_9$ Capacitors, J. Mater. Res., Vol. 12, No. 1, 1997

/5/ B. Gspan, Ph.D. Thesis, Faculty of Electrical Eng., University of Ljubljana, 1995

/6/ R. Osredkar, Spin-on-Glass Material Curing and Etching, Micrelectron. Reliab., Vol. 34, No. 7, 1994, p. 1265

/7/ L. K. White, Approximating Spun-on, Thin Film Planarization Properties on Complex Topography, J. Electrochem Soc. Solid State Science and Technology, Vol. 132, No. 2, 1985, p. 169

/8/ J. D. Romero et al., Outgasing Behavior of SOG, J. Mater. Res., Vol. 11, No. 9, 1996, p.1996

/9/ S. K. Gupta, Spin-on-glass for Dielectric Planarization, Microelectron. Manuf. Test., Vol. 12, No. 5, p. 10, April 1989

/10/ S. K. Gupta and R. L. Chin, ACS Symp. Ser., 295, 1986, p. 349

/11/ R. Osredkar, SOG Planarization of Device Topography, MIDEM, No. 3, 1995, p. 107

Radko Osredkar
FRI in FE Univerze v Ljubljani
Tržaška 25
SI 1000, Ljubljana
Slovenia
e-mail: radko.osredkar@fri.uni-lj.si

Prispelo (arrived): 24.05.01 *Sprejeto (Accepted): 01.06.01*

ELECTRONIC BRACE FOR THE MEASUREMENTS AND ELICITING OF MUSCLE CONTRACTIONS IN A DOG'S ANKLE

Matjaž Bunc and [1]Janez Rozman
School of Medicine, Institute of Pathophysiology, [1]ITIS d. o. o.
Centre for Implantable Technology and Sensors, Ljubljana, Republic of Slovenia

Keywords: medicine, physiology, physiologic measurements, dogs, electronic braces, ankle rotation, muscle contraction, spontaneous muscle contraction, stimulated muscle contraction, isometric muscle contraction, isotonic muscle contraction

Abstract: An experimental electronic brace, which is able to evaluate torque in the ankle joint of a dog elicited by spontaneous or stimulated muscle contraction, has been developed. The brace is also able to impose electrically controlled passive movements on the dog leg. Precise-passive movements, as passive external, electrically-controlled flexion or extension of the ankle of a dog leg, are defined in as speed and angle of rotation/movement. On the other hand, switching in a certain working mode, the brace, equipped with force transducers and a goniometer, could serve for measurements of isometric (*locked mode*) or isotonic contractions (*active mode* and *passive mode*) of a dog leg.

A range of the rotation around the ankle joint is limited between -40 and +55 degrees according to the neutral position. The calculated endurance moment of the brace is 2.41×10^{-4} kg m^2 s^{-1}, while the speed of electronically controlled movement of the brace in the *passive* mode is up to 78 degrees/second, respectively. In the *active* mode the brace is able to rotate synchronously with the dog ankle joint with a speed of up to 400 degrees/second. The maximum frequency, on activation of the *tibialis anterior* muscle current, when the amplitude of flexion was 50 degrees, was 7/min. In the *locked* mode the brace is able to measure the amplitude of force of a dog leg isometric contraction elicited by electrical stimulation. The force transducer with a natural frequency of 8 Hz and compliance of 0.4 μm/g represents a very linear dependence of the output voltage upon the load with a transducer sensibility of 0,5 mV/mN at a bridge excitation voltage of 5V. The nominal range of each transducer is 0-70 N.

Elektronska opornica za pasivno gibanje pasje noge in meritev kontrakcije v pasjem kolenskem sklepu

Ključne besede: medicina, fiziologija, merjenja fiziološka, psi, opornice elektronske, rotacija gležnja, krčenje mišic, krčenje mišic spontano,krčenje mišic stimulirano, krčenje mišic izometrično, krčenje mišic izotonično

Povzetek: Izdelali smo elektronsko opornico za pasjo nogo, s katere je moč meriti momente v pasjem gležnju, ki ji izzovejo mišice ob spontanem ali stimuliranem krčenju. Poleg tega je mogoče z opornico izzvati v naprej predvidene pasivne gibe pasje noge z natančno določeno hitrostjo krčenja ali raztegovanja in kotom premika opornice ter s tem na njo pritrjene pasje okončine. Razen tega lahko opornico priredimo za meritve izometrične kontrakcije (locked mode) ali pa izotonične kontrakcije (active mode) ter za prej omenjena programirana gibanja opornice (passive mode).

Kot za katerega se lahko zavrti opornica opornice glede na nevtralno lego, določeno z nevtralno lego pasjega gležnja, je od -40 do 55 stopinj. Izračunani vztrajnostni moment opornice je 2.41×10^{-4} kg m^2 s^{-1}. Pri pasivnem, programiranem gibanju opornice je moč nastaviti hitrost rotacije v območju od nekaj stopinj/sek do največ 78 stopinj/sek. V aktivnem načinu pa se opornica lahko zavrti, skupaj z stimulirano pasjo nogo, s hitrostjo tudi do 400 stopinj/sek. Največja frekvenca draženja mišice tibialis anterior, pri kateri je bilo moč izvajati meritve v aktivnem načinu brez popačenja (amplitudi zasuka opornice 50 stopinj) je bila 7/min. Na opornico je bil vgrajen tudi senzor sile, katerega resonančna frekvenca je bila 8Hz, podajnost (compliance) 0.4 μm/g in občutljivos 0.5 mV/mN (napajanje 5V). Občutljivost je bila pri napajanju s 5V v pričakovanem področju merjenih sil (0-70 N), povsem linearna.

Introduction

In physiological studies of muscle contraction and contemporary nerve activity it is suitable to have special equipment for eliciting controlled mechanical contractions of different muscles. The aim of this work was to develop a mechanical system that would be able either to measure or to impose movements of a dog ankle. Therefore, the aim of our work was to develop a special electronic brace for the dog leg. The brace should be able to elicit precisely defined (angle and speed) passive movements of a dog leg. On the other hand, the characteristics of both, isometric and isotonic contractions of a dog ankle muscle, caused by electrical stimulation, should be measured.

Materials and Methods

The brace

The brace consists of a mechanical joint that could be attached to the ankle of a dog. Such a fixed mechanical joint (ankle) turns around together with the ankle of a dog continuously. The artificial mechanical joint is a construction of one fixed part, artificial ankle and a rotate-able fine bearing, which, fixed on a dog leg, forms common axes with the joint of a dog (Fig. 1). The joint is connected to the actuator by mechanical transmission with a hysteresis angle of ±0.5 degree. The system measures the angle of rotation and the torque induced by the ankle of the dog either due to electrically powered passive rotation of the mechanical joint or electrical stimulation of the dog muscles. The rotate-able artificial ankle has the function of a force transducer at the same time. The brace is construct-

ed in such a way that it could be used for experiments either on the left or on the right leg. It just has to be turned around on the white or black plate (see Fig. 1).

tions divided by angles of rotation and is equal to 2.66:1. The mechanical transmission was selected on the basis of the specified requirements of acceleration and velocity in

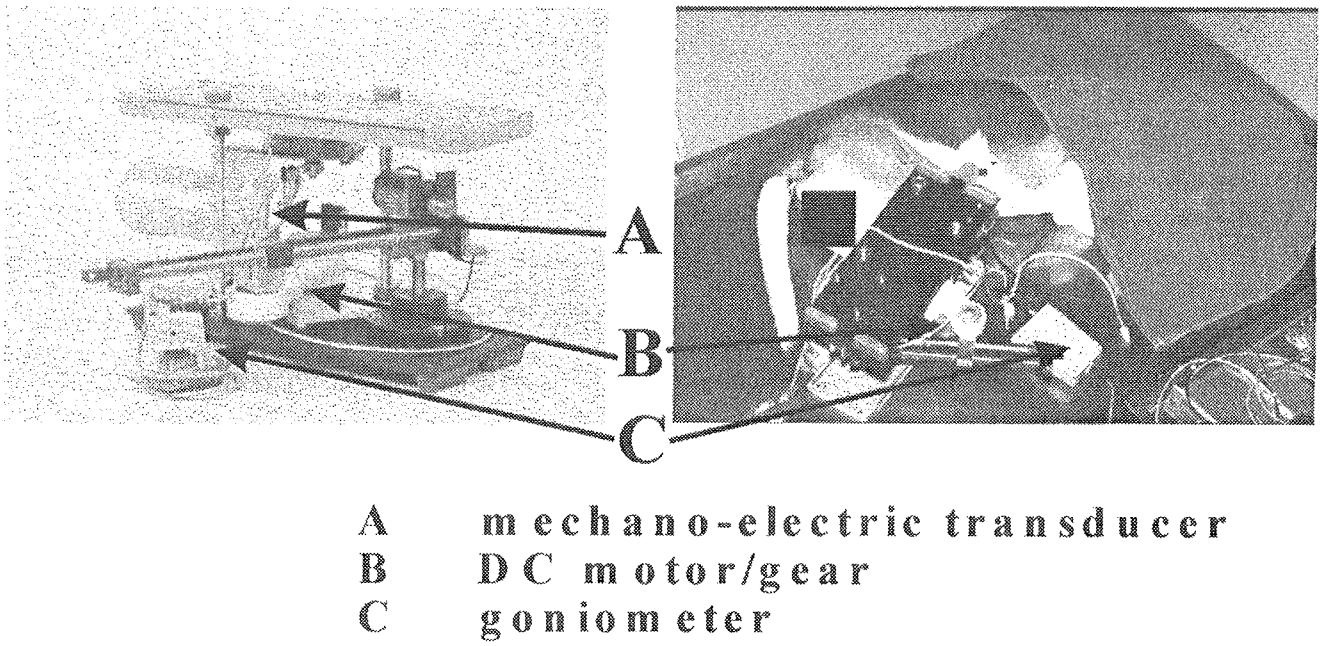


Fig 1. ***The brace.*** *The bear brace is shown on the left of the picture, the positioning of the dog leg into the brace is shown on the right. A) position of force transducer, B) DC motor/gear, C) goniometer.*

Description of the sensors

Mechano-electric transducer

The force transducers were made up of a full Wheatstone bridge composed of four semi-conductor strain gauges /1/ bonded on the artificial ankle (Fig.1.). The voltage signal, produced by a deformation of the semi-conductor strain gauges, is amplified by a precision strain gauge amplifier (Linear Technology, LT 1101).

Sensor of angle rotation – a custom designed goniometer

In order to measure and control an angle in the joint a custom designed goniometer manufactured from a precision potentiometer with a resolution of 0.1 degree (*ITIS d.o.o.*, Ljubljana) is mounted at common axes with the rotate-able artificial ankle (Fig. 1).

Mechanical part of the brace

Passive movements of a dog ankle are elicited electrically by powered motor movements of the artificial ankle brace transmission (Fig. 1).

Actuator system

The complete actuator system is mounted on an aluminum plate, the base of the brace. It is possible to regulate the motor speed and number of revolutions by the PC controller. The ratio of transmission is defined by motor revolu-

the passive mode with respect to the friction of transmission. The chosen system comprises a direct current (DC) motor within grounded iron cage to minimize electromagnetic artifacts.

Motor control

An actuator system involving the aforementioned DC motor/gear system (Fig.1) is mechanically connected to the mechanical joint, and joint thus transferring the torque to the dog joint. By position feedback obtained through measuring an angle in the mechanical joint, the motor is regulated in such a way that it rotates at a chosen speed for any angle according to the neutral position of the ankle. The mechanical system is able to operate in three modes: *passive, locked* and *active* mode. In the *passive* mode the brace is able to rotate the ankle by a predefined angle at a different predefined speed. Therefore, in this mode a rotation from the actuator is transferred to the ankle joint, thus imposing a stretch of a dog ankle extensors or flexors. The common friction, expressed as the certain amount of torque in the *passive* mode, is composed of friction of the potentiometer, four fine bearings and the transmission. In the *locked* mode, the position of the motor and artificial ankle is locked at a desired angle in order to measure the isometric torque elicited by electrical stimulation of the muscles or muscle group under investigation. The force transducers, described above, measure the torque of contrac-

tion through deformation of the sensors. In order to achieve a dynamic range of measurement in the *active* mode, the system is able to follow the ankle joint rotation with fast cadence elicited by electrical stimulation of a nerve or muscle.

Measurements of passive and dynamic characteristics of the brace

Passive characteristics of the brace

The maximum speed of the ankle movement was determined by goniometric measurement of an angle speed of the spare brace rotation at the highest DC motor performance.

Brace friction

The common friction of the brace was defined by feeding a known DC to the motor and measuring the mechanical energy output. The difference of the input and output energies reveals the friction of the system.

Dynamic characteristic of the brace

The dog muscle contraction was elicited by electrical stimulation of the sciatic nerve using stimuli with frequencies ranging from 0 to 20 min^{-1}. Since contractions of the leg were detected by the brace, we could determine the frequencies where the response of the brace is linear. This means that the ratio of stimulus/contraction detected without artifacts due to the brace friction or endurance is 1.

Endurance moment of the artificial ankle

The endurance moment of the brace was calculated considering the dimensions (14 x 3.3x 1 cm), shape and material (aluminium) of the artificial ankle.

Selective stimulation of fibers in the sciatic nerve of a dog with a 33-electrode stimulating and recording spiral cuff

The cuff was made by bonding two 0.1 mm thick silicone sheets together /2-5/. One sheet stretched and fixed in that position was covered by a layer of adhesive material (NuSil, MED-1511). A second unstretched one was placed on the adhesive and the composite was compressed to a thickness of 0.3 mm. When released, the composite curled into a spiral tube as the stretched sheet contracted to its natural length. 33 electrodes (0.6 x 1.5) mm made of 0.05 mm thick platinum ribbon connected to lead wires were mounted on the third silicone sheet. They were arranged in three parallel spiral groups each containing 11 electrodes at a distance of 0.5 mm. The distance between the spiral groups was 6 mm. Electrodes of the central group were connected to lead wires individually, while the corresponding outer electrodes were shunted to each other and then connected to lead wires. The silicone sheet with electrodes was bonded on the inner side of the cuff. The cuff with an inner diameter of 2.5 mm was trimmed to a length of 20 mm. The lead wires were connected to the connector to be implanted within the lateral subcutaneous tissue for the time between stimulation. Rectangular, bi-phasic, charge balanced, current pulses with a frequency of 20 Hz and amplitude of up to 1 mA were delivered on the central electrode of each GTE within the cuff. As a neutral electrode a hypodermic needle was inserted in the subcutaneous tissue of the thigh, slightly proximal to the cuff.

Selective recording of electro-neurogram (ENG) from the sciatic nerve of a dog

The cuff already described above was used also for the selective recording of the ENG from a dog nerve after passive or active dog leg movements. ENGs are recorded differentially and selectively with the spiral cuff (see above) from two superficial regions of the sciatic nerve innervating mostly the aforementioned muscles /6-7/. Since the motor system has to operate simultaneously with noise-sensitive ENG measurements, the electromagnetic noise of the motor system was reduced by using a RFI filter and ferrite cores on the supply connections. Shielded wires and the motor and proper ground connection were implemented throughout the entire electrical circuit.

Results

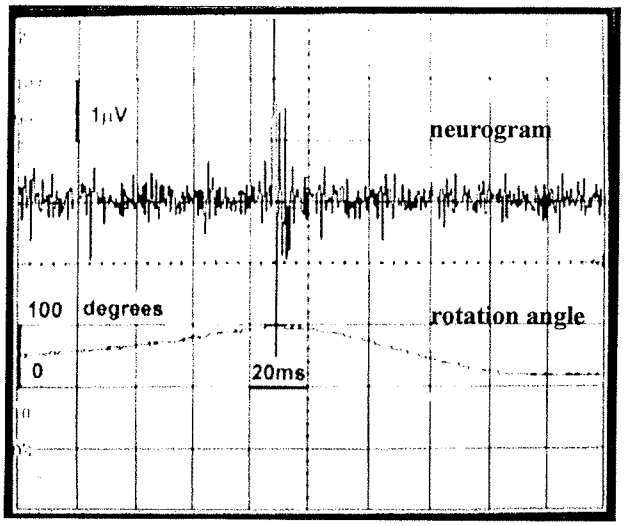


Fig 2. ***Detection of the contraction of the dog ankle in the*** **passive** ***mode of the brace.*** *The upper trace shows a neurogram recorded from the sciatic nerve after rotation of the brace and the dog leg with a DC motor system at 50 degrees.*

In the *passive* mode (Fig. 2) the brace is able to rotate to a maximum extension of 45 degrees and of maximum flexion of 55 degrees, according to the neutral position of the ankle. The DC motor/gear system is able to perform movement of the artificial ankle with a speed of up to 78 degrees/second. However, practically we could not exceed 7 passive movements with maximum amplitude of flexion and extension of a dog ankle per minute during the experiments because of the combination of endurance and fric-

tion of the complete system and resistance of the dog ankle.

The friction of the system presents less than 2% of the input electric force. In the *active* mode the brace is able to measure reliably the parameters of a dog ankle contraction elicited by the electrical stimulation of a nerve. In order to follow the ankle joint without resisting the movement, the brace is able to perform an ankle rotation of up to 400 degrees/second synchronously with a dog ankle. The calculated endurance moment of the brace is 2.41×10^{-4} kg $m^2 s^{-1}$. The maximum frequency at which the ratio stimulation/contraction is lower than 1 depends on the amplitude of the brace movement due to the dog's leg contraction. In our experiment, at an amplitude of 50 degree of flexion and sciatic nerve stimulation current of 1.4 mA, the maximal frequency of stimulation was 10/min. Above this, we could not measure the contraction parameters of a dog ankle at the maximum amplitude of flexion and extension without artifact any more.

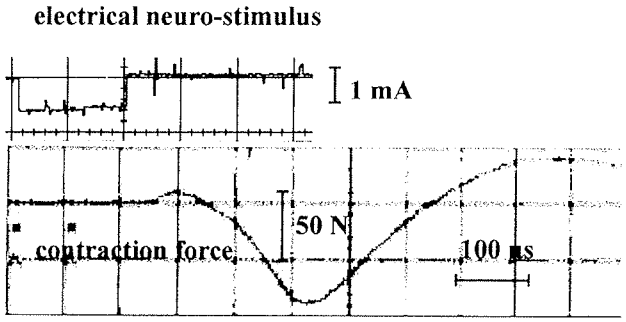


Fig 3. ***Detection of the force of contraction of the dog ankle in the*** **locked** ***mode of the brace.*** *The upper trace shows the neuro-stimulus applied to the sciatic nerve. The lower trace shows force of the dog leg developed after nerve stimulation.*

In the *locked* mode (Fig. 3) the brace is able to measure the amplitude of force of the dog ankle contraction elicited by electrical stimulation. The transducers with a natural frequency of 8 Hz and compliance of 0.4 μm/g represent a very linear dependence of the output voltage upon the load with the sensibility of transducers being 0.5 mV/mN at a bridge excitation voltage of 5V. The nominal range of each transducer is 0-70 N.

Discussion

According to the aims of the brace construction determined in the introduction, we can conclude that all of the aforementioned requirements were met. The brace is a suitable tool for the study of contractions of different muscles or muscle groups of a dog leg as a result of selective stimulation of a peripheral nerve. On the other hand, nerve activity from a peripheral nerve, describing the torque and angle of rotation in the ankle joint as a consequence of flexion or extension elicited by the brace or by passive movements of the leg, could be recorded. The limitation of the transducer is that it has a relatively high endurance that could not be easily diminished. It enables recordings of muscle contraction parameters at higher frequencies of nerve stimulation. On the other hand, the brace, due to its low friction, permits the recording of isotonic forces of contraction. When using the *locked* brace mode, measurements of isometric muscle are also possible. The brace is a suitable and low price research tool. Its construction could be easily adapted to the experiments on animal legs of different sizes and force of contraction.

Acknowledgement

This work was financed by Research Grant Nos. J2-7042-1326 and J3-2389-0381-00 from the Ministry of Science and Technology, Ljubljana, Republic of Slovenia.

References

/1/ Bunc, M., Šuput, D., Rozman, J., 1999, Force transducer for measurements of isolated muscle contractions. J Med Eng Technol, **23**, 222-225.

/2/ McNeal, DR., Bowman, BR., 1985, Selective activation of muscles using peripheral nerve electrodes. Medical & Biological Engineering & Computing, **23**, 249-253.

/3/ Sweeney, JD., Ksienski, DA., Mortimer, JT., 1990, A nerve cuff technique for selective excitation of peripheral nerve trunk regions. IEEE Transactions on Biomedical Engineering, **37**, 706-715.

/4/ Lefurge, T., Goodall, E., Horch, K., 1991 Chronically implanted intrafascicular recording electrodes. Annals of Biomedical Engineering, **19**, 197-207.

/5/ Rozman, J., Sovinec, B., Trlep, M., Zorko, B., 1993, Multielectrode spiral cuff for ordered and reversed activation of nerve fibres. Journal of Biomedical Engineering, **15**, 113-120.

/6/ Rozman, J., Zorko, B., Seliškar, A., Bunc, M., 2000, Selective recording of ENG from peripherial nerve. Pflüg Arch-Eur J Ph (suppl), 440, 157-159.

/7/ Rozman, J., Zorko, B., Bunc, M., 2000, Selective recording the sciatic nerve of a dog with multi-electrode spiral cuffs. Jpn J Physiol., 50, 509-514.

Matjaž Bunc
School of Medicine
Institute of Pathophysiology
Zaloška 4, 1000 Ljubljana, Slovenia
e-mail: Bunc@ibmi.mf.uni-lj.si
fax: 386 61 443 898.

Janez Rozman
ITIS d. o. o. Ljubljana
Centre for Implantable Technology and Sensors
Lepi pot 11, 1001 Ljubljana, Slovenia
Tel.: 17 01 913, Fax.: 17 01 939

Prispelo (Arrived): 28.03.01 *Sprejeto (Accepted): 01.06.01*

APLIKACIJSKI ČLANKI
APPLICATION ARTICLES

TANTALUM CAPACITOR REPLACEMENT WITH CERAMIC CAPACITOR

Iztok Šorli, MIKROIKS, Ljubljana

High Capacitance MLCC

For several years we have been facing periodic variations of availability and price of Tantalum capacitors. In the past this behaviour was due to political and economical strategies.

Today it is the poor supply of Tantalum raw material that drives the Tantalum capacitor crisis. At present we see a price growth of 50% (from 0.2 USD to 1.0 USD) for normal Tantalum capacitors; the forecast is for a further hike in the next year. Murata can help to solve this problem by offering many ceramic capacitors that directly replace electrolytic and Tantalum types.

Before we discuss about electrical characteristics, part numbers etc., let us briefly summarize some basic concepts of high capacitance usage. Figure 1 shows principal circuits that need high capacitance values.

Smoothing

The function of C1 and C2 is to smooth ripple and voltage fluctuations at the input and output of the LDO (Low Drop Out Regulator). C2`s ESR and ESL are most important because they are responsible for the purity of the output voltage. In the past high value Ta capacitors were used; now it is possible to use ceramic capacitors at 1/2 to 1/10 of the Ta values used.

Bypassing

C3 creates a "virtual" ground for the transistor which "believes" it is working at ideal conditions. The static and dynamic parameters are satisfied and the active device is properly used. Also in this case the ESL of the capacitor is of the most importance since a low value avoids self - oscillation problems.

Coupling

In order to link two stages (for example pre amp to power amp) C4 is basic. This capacitor transfers only the signal and does not modify the DC parameters. For the example mentioned, it is the most important that the capacitor is not polarized in order to avoid signal distortion. What better solution than a ceramic capacitor?

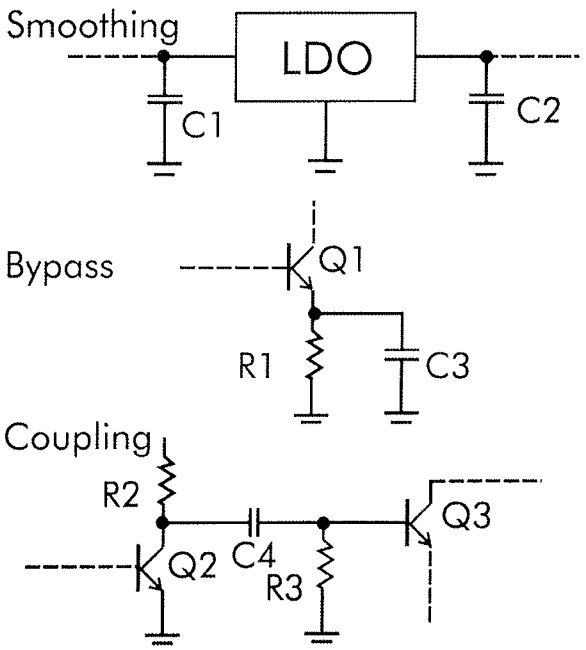


Figure 1: Examples of principal circuits where capacitors with high capacitance values are mostly used

Technical Aspects of Multi Layer Ceramic Capacitors

Despite the simple construction, monolithic ceramic capacitor provides both high-speed response and an excellent high-frequency characteristics; the capacitance range has generally reached just approximately 1μF until now. However, with recent advancements in the thin-layer/multilayer forming technology for dielectrics, as well as the technology for using base metal for internal electrodes, the capacitance range now exceeds 1μF. Moreover, capacitors with capacitance of up to 100μF have been developed and are now being used.

Multilayer Ceramic Capacitors (MLCC) are built as a kind of "sandwich", composed of conductive layers separated by a dielectric (ceramic). Two conductive terminations are added to provide solderability, figure 2.

The mathematical formula that relates all the mechanical and electrical parameters to the capacitance values is as follows:

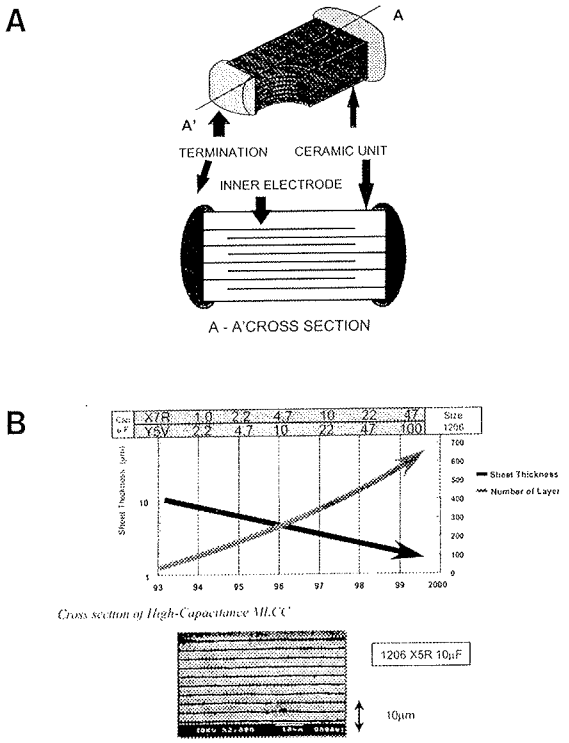
$$C = \frac{\varepsilon \times \varepsilon_0 \times S \times n}{d}$$

where

* ε_0: dielectric constant of vacuum
* ε: dielectric constant of ceramics
* S: active area per layer
* n: number of ceramic layers
* d: thickness of a layer

With this equation in mind, the means of obtaining high value multilayer ceramic chip capacitors are:

* thinner dielectric layers
* increased number of dielectric layers
* increased active area
* increased dielectric constant



Fugure 2: Structure of a ceramic capacitor

A) device cross section

B) physical cross section as seen on electron microscope; the graph is showing how higher capacitances of X7R and Y5V ceramic capacitors can be obtained by thinning dielectric layers and by increasing their number

The most important parameter that can enable an increase in the capacitance of monolithic ceramic capacitors is the thickness of the dielectric element. Year by year, the dielectric element thickness becomes ever smaller. Currently, products with a dielectric element of 2 ~ 3 μm thick are on the market, and recent products with dielectric elements only 2μm thick or less have been developed. The core technologies for supporting thin-layer products include technologies for ultra-fine graining and low-temperature firing of ceramics, non-reduction material technology, and technologies for graining and dispersing the electrode material, as well as using base metal for the electrode material. These technologies are much advanced compared to more conventional ones.

Consequently, the delicacy of a MLCC design is clear. A good capacitor is the result of a good balance between materials, thickness and dimensions.

This demonstrates the difficulties to be overcome in order to obtain small, high value capacitors with good temperature performance and high working voltages.

Reliability Superiority of Ceramics over Tantalum

Breakdown voltage

In figure 3 there are two important points that must be observed:

* considerably higher actual breakdown voltage of ceramic capacitors compared to tantalums
* enormous safety factor between stated working voltage and actual breakdown voltage of ceramic capacitors

This only means that the ceramic capacitor is more reliable and that can safely operate at the stated working voltage; it would also seldom fail due to overvoltage spikes which would kill tantalum capacitor.

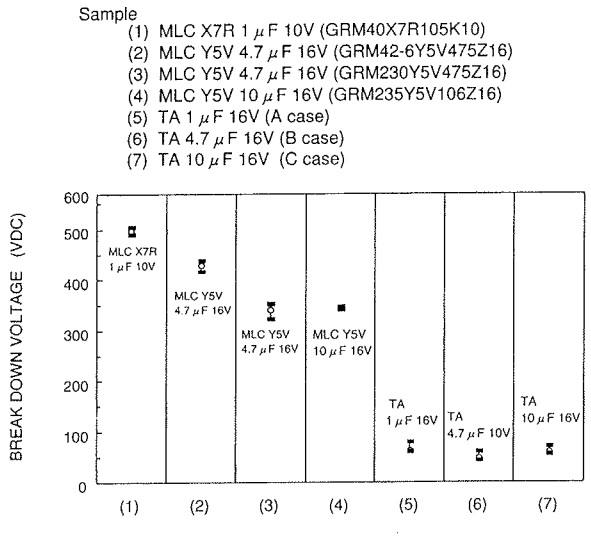


Figure 3: Comparison among measured breakdown voltages of ceramic and tantalum capacitors

ESL & ESR vs Frequency

Unique features of ceramic capacitors are their low Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL) especially at high frequencies. This is clearly demonstrated in figure 4 where differences among two types of ceramic (X5R and Y5V) capacitors and tantalum capacitors are shown.

The superior performance of the ceramic is extremely clear, allowing optimization of final circuit. Because of this effect, in most cases it is even possible to reduce the capacitance values of ceramic capacitor compared to tantalum, while filtering very effectively.

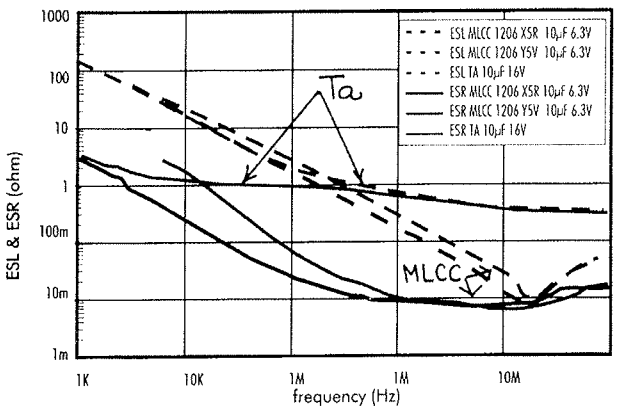


Figure 4: ESL and ESR of ceramic versus tantalum capacitors

Allowable Power

The low ESR is the feature of MLCC that allows high peak current. This guarantees very fast response to high speed current transients.

The low ESR (at medium/high frequencies) also causes low self-heating when ceramic capacitor is under stress at high frequencies and under high voltage.

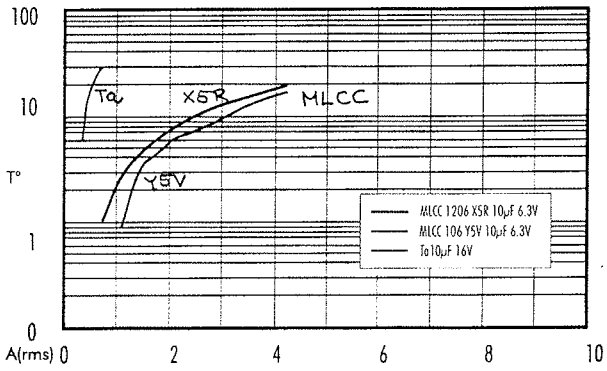


Figure 5: Temperature rise of different capacitors working at 100 kHz

Attention

When designing circuitry with ceramic capacitors two important things must be taken into consideration: capacitance versus temperature behaviour of different ceramics, as well as capacitance versus bias voltage dependence, as summarized in figures 6 and 7. In these two specific cases only the performance of X7R ceramics is comparable to tantalum, while Y5V is inferior.

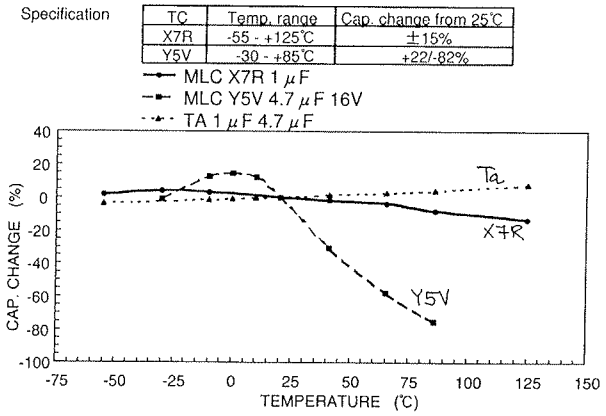


Figure 6: Capacitance versus temperature behaviour of different capacitors

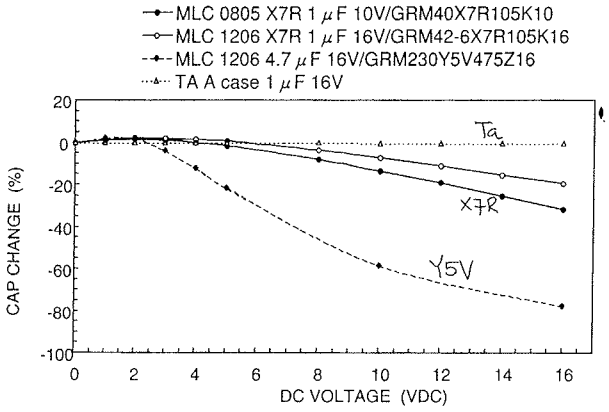


Figure 7: Capacitance versus DC voltage behaviour of different capacitors

Measurement results

Figures 8, 9 and 10 present some measurement results from which we can compare performance of ceramic to Ta/Al capacitors in pulse response, noise absorption and smoothing applications.

This data shows clearly that in noise bypass applications the value of MLCC capacitance can be 1/2 to 1/10 of the tantalum for the same bypass effect. This is due to lower ESR and ESL of MLCC compared to tantalum capacitor.

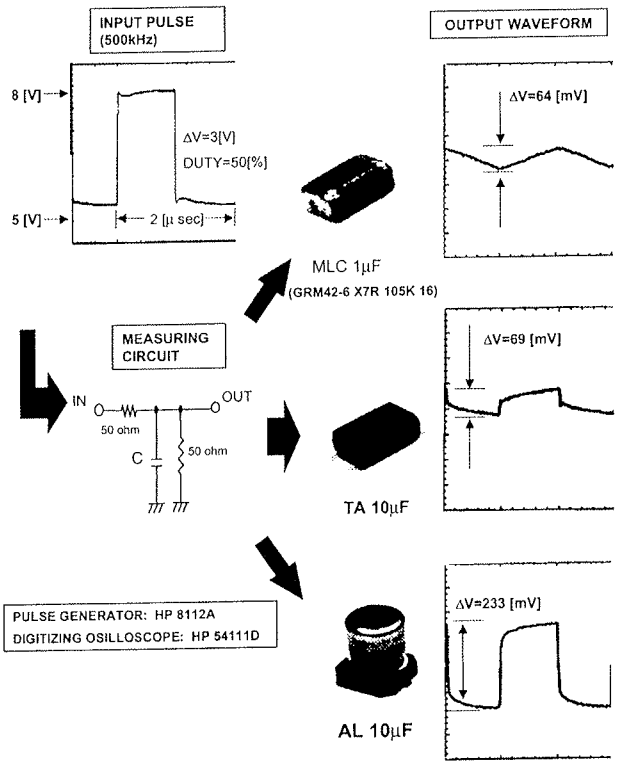


Figure 8: Pulse response of MLCC versus Ta/Al capacitors

Input Pulse Freq	Input Pulse Voltage	Output ripple voltage (mV)		
		AL	TA	MLCC
10kHz	2V	534	204	196
100kHz		336	64	16
500kHz		346	38	12
1MHz		332	30	3

FFT Analysis result shows MLCC's superiority in terms of noise absorption in High Frequency range.

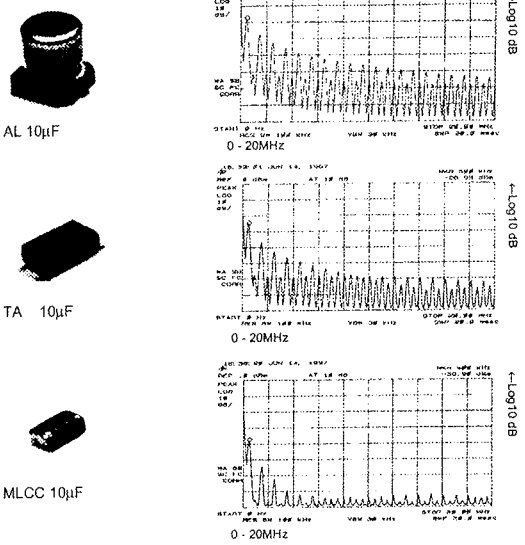


Figure 9: General noise absorption comparison data

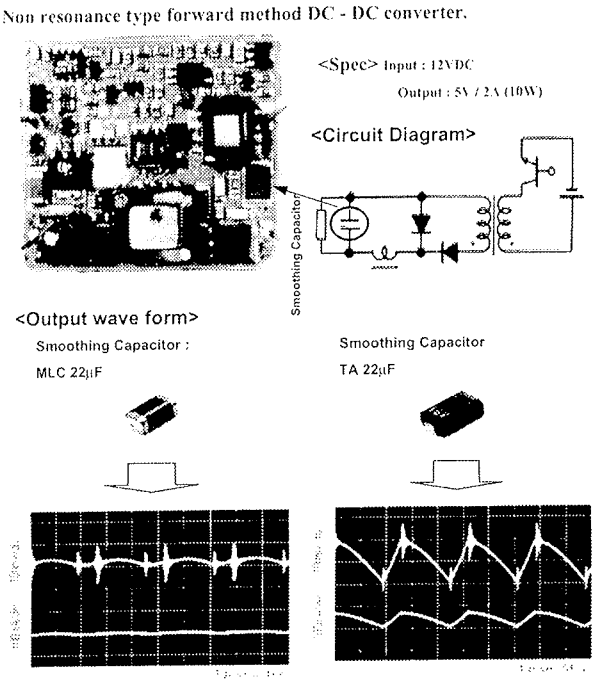


Figure 10: Example of Ta/Al replacement in smoothing application

Table I: performance comparison among MLCC, tantalum and aluminum capacitors

		MLCC		TA	AL
Hihg freq.	Capacitance - frequency	Exelent		Fair	Poor
	Imedance - frequency	Exelent		Fair	Poor
Reliability	Break down Voltage	Exelent		Fair	Fair
	Life	Exelent		Fair	Fair
	Temp. rise	Exelent		Fair	Poor
Other	Noise absorption	Exelent		Fair	Poor
	Polarity	Exelent		Poor	Poor
	Size	Exelent		Good	Fair
	Temp. Capacitance	X7R X5R	Y5V	Good	Fair
		Good	Fair		
	Voltage Capacitance	X7R X5R	Y5V	Good	Good
		Fair	Fair		

The Murata answer

In figure 11 you will find the most important values of MLCC that Murata is able to supply. The dielectric types, the capacitance values, the working voltages and the sizes of capacitors currently in production are shown. Please, note that this list is being constantly updated as new capacitor types are being added on the regular basis.

As well, figure 12 allows you to find the right MLCC size to match the existing land pattern of the Ta being replaced. On the left there are the most common Ta pad designs for reflow soldering, on the right there are basic MLCC sizes for those pads. To find equivalent size of MLCC just drag its symbol over the Ta land pattern.

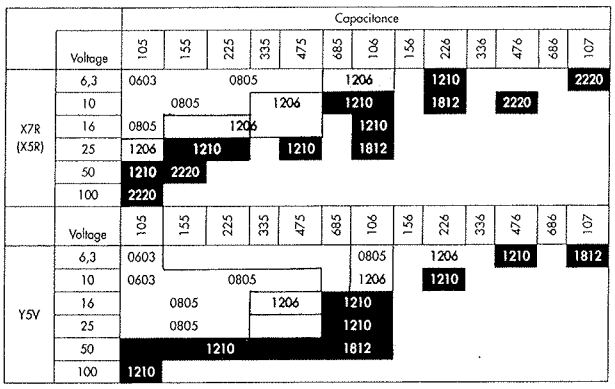


Figure 11: List of high capacitance MLCC that can be supplied by muRata

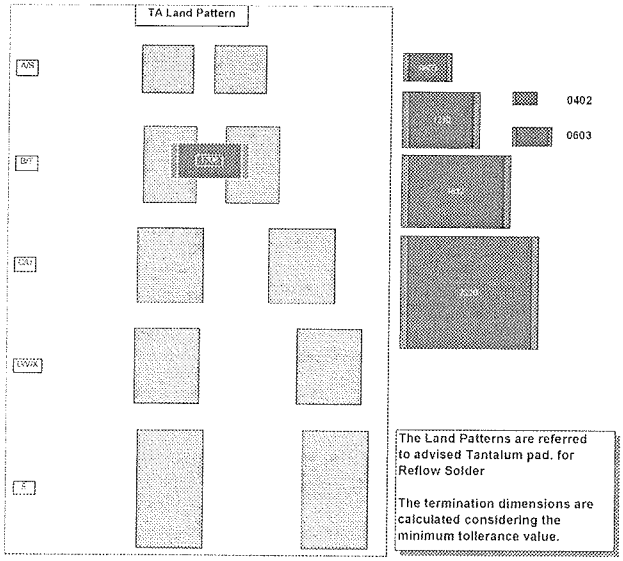


Figure 12 . MLCC to Ta matching sizes

Continued development will see continued decreases in the thickness of the dielectric element. Using thin-layer forming technology allows ceramic capacitors to be further reduced. With increased semiconductor density, semiconductor components use lower voltages. Accordingly, electric and electronic circuits are driven at lower voltages. If a ceramic capacitor appears with a rated voltage of 4 V or 2.5 V, there is a great possibility that applications will be found for it. The current situation is favorable especially for thin-layer monolithic ceramic capacitors.

Likewise, the technology has grown enough to meet the needs for products with more than 100 μF, 220 μF, or higher capacitance.

In addition, low-profiled products that can be used in thinner equipment are available. Step by step, product thickness of 1.35 mm or more will be reduced to 1.35 mm or less (1.25±0.1 mm), to 0.95 mm or less (0.85 mm±0.1 mm), and then to 0.7 mm or less (0.6 mm±0.1 mm).

As described above, it is expected that high-capacitance monolithic ceramic capacitors will be further developed in a variety of directions – through downsizing, upsizing, capacitance increase, rated voltage increase, and more – all based on the ceramic thin-layer forming technology.

REFERENCES

/1/ MURATA mail, no.4, spring 2001
/2/ muRata internal communication
/3/ Denpa Shinbun, Part 2, High Technology, Aug. 21, 2000

Iztok Šorli
MIKROIKS d.o.o.
Stegne 11, 1521 Ljubljana
Tel.01 5112 221, fax.01 5112 217

POROČILA S KONFERENCE
CONFERENCE REPORTS

Konferenca MicroTech 2001, London, 29. do 31. januar 2001R

Marko Hrovat
Institut Jožef Stefan, Jamova 39, 1000 Ljubljana

V dneh od 29. do 31. januarja 2001 je bila v Londonu konferenca "MicroTech 2001" (to je skrajšano za Micro Technologies), ki je bila formalno v treh delih; "Seventh European Conference on High density Packaging", "European Conference on Wireless Technologies" in "Second European Conference on Microsystems Packaging", vendar so se teme vseh treh prepletale. Organizirala jo je angleška sekcija IMAPS (International Microelectronics and Packaging Society). Ob konferenci je bila tudi razstava proizvajalcev opreme in materialov za hibridno mikroelektroniko. Registriranih je bilo nekaj nad 80 delegatov.

Ker bodo v tekstu nekajkrat omenjeni flip chip tabletke in Multi Chip Moduli, bom na kratko ponovil nekaj definicij. Flip-chip so tabletke, ki se pritrdijo "z obrazom navzdol". Na površini tabletke so na kontaktih izdelane kroglice spajke (bumps), ki se s pretaljevanjem pritrdijo na substrat. Zanimivo je, da je flip chip tehnologija "stara" že skoraj 40 let (IBM je pričel izdelovati flip-chipe leta 1962), vendar se jih do pred nekaj leti ni veliko uporabljalo. Pri tabletkah, ki so pritrjene kot flip-chip, je onemogočena vizualna kontrola, ker so kroglice spajke skrite med tabletko in substratom. Flip-chip tabletke so že po definiciji vedno dražje od tistih, ki so namenjena za bondiranje z žičko, ker so potrebni dodatni tehnološki postopki, da se izdelajo kroglice spajke. Prednost tabletk v flip chip izvedbi je, da v vezju zasedejo tudi do 60% manj prostora kot tabletke, bondirane z žičko. Zato njihova uporaba, predvsem v MCM, strmo narašča s stopnjo okrog 28% letno. Ocenjujejo, da bo leta 2002 na trgu 2 in pol miljarde chipov v flip-chip izvedbi.

Multi Chip Moduli (MCM) so komponente, podsistemi ali sistemi z zelo visokim številom funkcij. Narejeni so na večplastnih substratih, na katerih so pritrjene ali gole polprevodne tabletke ali pa tabletke v Chip Sized Package (CSP), ki so samo okrog 20% večje kot gole tabletke. V večplastnem substratu in na njegovi površini so prevodne linije. Vezje je navadno hermetično zaprto. V glavnem ločijo tri tipe MCM, ki so izdelani v različnih tehnologijah, to je tankoplastni, debeloplastni (keramika) in v tehnologiji tiskanih vezij. Oznake so MCM-L (laminates - tiskana vezja), MCM-C (ceramics - keramika) in MCM-D (deposited - tanki filmi). MCM-C so "keramični" hibridi visoke gostote, navadno večplastni keramični substrati ali pa kompleksna debeloplastna večplastna vezja. Večplastni keramični substrati so narejeni iz zelenih folij, potiskanih s prevodnimi linijami in so lahko na osnovi Al_2O_3 ali AlN z višjo toplotno prevodnostjo (MCM-C z visoko temperaturo žganja) ali pa na osnovi kristalizirajočih stekel (MCM-C z nizko temperaturo žganja). Po nekaterih ocenah pripada keramičnim multi chip modulom preko 50% tržišča. MCM-D imajo nanešene tankoplastne večplastne kovinske povezave, ločene predvsem s polimernim ali včasih napršenim tankoplastnim dielektrikom. Kot substrat za MCM-D se običajno uporablja Al_2O_3 ali silicij. MCM-L so zahtevna večplastna tiskana vezja z linijami čim manjše širine. Ta tip MCM je navadno tudi najcenejši. Seveda so multi chip moduli v večini primerov dražji kot bolj "klasične" izvedbe, njihova prednost pa je, da so manjši. Zmanjševanje modulov in vedno večjo gostoto komponent zahteva razvoj telekomunikacij, na primer prenosnih telefonov, modemov, daljinskih upravljalcev itd. Skratka, elektronskih naprav, ki združujejo vedno več funkcij, še vedno pa morajo biti tako majhne, da jih lahko držimo v roki.

H. Quinones (Asymtek, Carlsbad, California) je v referatu z naslovom "Encapsulation of large, densely populated die with small gap" predstavil probleme pri pritrjevanje silicijevih tabletk na tiskana vezja, predvsem tabletk v flip-chip izvedbi. Po spajkanju flip-chipa zapolnijo prostor med tabletko in substratom s polimernim tekočim "podpolnilom" (ta izraz je precej okoren in dobeseden prevod izraza "underfill"). Podpolnilo nanesejo ob enem ali dveh robovih tabletk s dispenzerjem, podobnim injekcijski igli. Tekoč material steče pod tabletko v ozkem prostoru med tabletko in med med prispajkanimi kroglicami. Ko podpolnilo polimerizirajo, se malo skrči in pritiska na spajkalne krogljice. S tem nekoliko kompenzira različne temperaturne razteznostne koeficiente (TEC) med tabletko in substratom. Z naraščajočim številom funkcij in z naraščajočo gostoto funkcij postajajo tabletke večje, hkrati pa narašča gostota priključkov in se manjšajo dimenzije posameznega priključka. Raster - velikost spajkalnih krogljic in razmak med njimi - se je zmanjšal že do 25 μm. Podpolnilo ne teče z laminarnim

tokom, ampak zaradi kapilarnih sil. Avtorji so testirali vrsto materialov, tako tistih z nizko vsebnostjo polnila in nižjo viskoznostjo kot "klasičnih", pri katerih so znižali viskoznost s povišano temperaturo. Druga možnost je, da je podpolnilo netekoč film na substratu, v katerega "vtisnejo" tabletko s spajkalnimi kroglicami in nato pri povišani temperaturi hkrati polimerizirajo material in pretalijo spajko. Problem pri tem je, da so pri tem načinu prevodne blazinice na substratu pokrite in jih je težje "zadeti" s spajkalnimi kroglicami. Predavatelj je pokazal tudi video posnetke, ki so pri povečavi kazali, kako podpolnilo teče pod flip-chipom. Za te preiskave so uporabili steklene ploščice s spajkalnimi kroglicami z rastrom in v velikosti testiranih tabletk, tako da so lahko snemali skozi prozorno ploščico.

P. Moran (Advanced Interconnection Technology, Manchester, Anglija) je v referatu "Advances in interconnection technologies using selective electroplating" predstavil način izdelovanja bakrenih prevodnih linij na različnih substratih, to je na keramiki, fleksibilnih polimerih ali na tiskanem vezju. Baker je zaradi dobre prevodnosti in razmeroma nizke cene skoraj idealen prevodnik. Na substrat najprej nanesejo "začetno plast" (initial coating). Debelina te plasti, ki je osnovi zmesi plemenitih kovin, tako da se lahko procesira na zraku, je po toplotni obdelavi del mikrometra. Ker prevaja kasneje nanešen prevodnik, upornost same začetne plasti ni pomembna. Mora pa imeti dobro adhezijo tako na substrat kot na prevodnik. Nato substrat pokrijejo s foto resistom, ki ga razvijejo z ultavijolično svetlobo skozi primerne maske, da dobijo odprtine tam, kjer bo nanešen prevodnik. Prevodnik - baker - nato izdelajo z elektrolitskim nanašanjem. Hitrost rasti prevodnika je okrog 0,5 μm/min. Najmanjša širina prevodnika je okrog 20 μm, debelina, ki je odvisna od časa nanašanja, pa je lahko, odvisno od zahtev, do 100 um ali več. za nekatere aplikacije nato prevodnik pokrijejo s tanko plastjo niklja in preko tega zlata za boljše spajkanje ali bondiranje. Ko je prevodnik nanešen, odstranijo foto resist in med prevodnimi linijami odjedkajo začetno plast. Pri tem je pomembno, da je sestava materiala začetne plasti različna od prevodnika, tako da se lahko selektivno odjedka, ne da bi se jedkal tudi baker. Na vprašanja, kakšen je material za začetno plast, predavatelj seveda ni hotel odgovoriti. Povedal je le, da ga nanašajo kot tekočino, debelina plasti po nanosu je okrog 4 μm (spiniranje?) in da je njegova sestava različna, odvisno od tipa substrata.

Več referatov je bilo posvečenih materialom oziroma vezjem na osnovi keramike z nizko temperaturo žganja (LTCC - Low Temperature Co-fired Ceramics). Ti materiali so na osnovi zmesi stekla in keramike ali pa kristalizirajočih stekel in so po sestavi podobni debeloplastnim dielektrikom za večplastna vezja. Žgejo se običajno pri temperaturah okrog 850°C. Zelene folije so debele od 25 μm do 100 μm in več. Na folije natiskajo posamezne nivoje večplastnega vezja, jih razsekajo in "prebijejo" majhne odprtine (vias). Odprtine zapolnijo s prevodnikom, zelo pogosto s srebrno pasto. Nato folije natančno zložijo ("zadeti" morajo zelo majhne odprtine (vias) v posameznih plasteh), stisnejo skupaj, razplinijo pri temperaturah sto ali nekaj sto stopinj Celzija in žgejo, da se zasintrajo v tri dimenzionalno strukturo. V nasprotju z običajnimi debeloplastnimi hibridnimi vezji, kjer je temperatura žganja okrog 10 min, se ti LTCC sendviči žgejo tudi neka ur. Na površini sintranega sendviča lahko izdelajo debeloplastne upore in pritrdijo komponente. Že pred skoraj desetimi leti so vsi večji proizvajalci debeloplastnih materialov začeli izdelovati pod različnimi komercialnimi imeni folije za LTCC tehnologijo. Nekaj let nazaj je kazalo, da se MCM, predvsem MCM-C, vrtijo v začaranem krogu in se kar ne "premaknejo" naprej. Zaradi majnega povpraševanja in s tem povezanih majhnih serij so bile MCM izvedbe drage. Ker so bile drage, to ni spodbudilo povpraševanja, ki bi lahko znižalo ceno. V zadnjem času so se stvari optimistično "premaknile". Za razmah LTCC tehnologije izdelave multi chip modulov sta bili, zanimivo, dve gonilni sili; v Evropi avtomobilska elektronika, v ZDA pa disketni pogoni v računalnikih.

Barnwell s sodelavci (Heraeus Circuit Materials Division in Middleesex University) je v referatu z naslovom "LTCC systems for low frequencies - a study of the critical properties and their measurement techniques" predstavil preiskave LTCC materialov, razvitih pri Heraeus-u in načine meritve zaželjenih karakteristik pri visokih frerkvencah. (Same tehnike meritve sta bolj podrobno opisala dva koavtorja tega referata (C. Free, Z. Tian) v prispevku "Micro technology measurement techniques for the evaluation of thick-film materials used in wireless applications"). Mikrovalovne aplikacije so po uporabi frekvenc razdeljene grobo v dve skupini, nižje frekvence med 1 in 6 GHz in višje frekvence od 20 GHz naprej. LTCC keramika je hkrati z debeloplastno tehnologijo nanašanja komponent že preverjeno uporabna za nižje frekvenčne aplikacije. Omogoča izdelavo struktur s pokopanimi komponentami, na primer upori ali kondenzatorji. Ločljivost linij je pri sitotisku do 75 μm, s foto občutljivimi dbeloplastnimi materiali pa do 50 μm, novi materiali pa naj bi omogočili ločljivost do 25 μm. Velikost odprtin (vias), ki povezujejo prevodne nivoje, je 100 μm. Njena prednost je predvsem relativno nizka cena, čeprav je na enoto površine še vedno dražja kot tiskana vezja (MCM-L izvedbe). Cena LTCC folij seveda pada z naraščajočim volumnom uporabe. Tu je treba omeniti, da so MCM-C, narejeni s tehnologijo LTCC, bolj gosti kot tiskana vezja , kar po mnenju avtorjev že sedaj "prevaga" nekoliko višjo ceno. Druga velika prednost je paralelno procesiranje; vse folije se najprej potiskajo in nato zložijo in zapečejo v večplastne strukture.

Nekatere aplikacije, ki delujejo na področju nižje frekvenčnih mikrovalov in ki so tržno zelo pomembna, so:
Prenosni telefoni delajo v območju 0,9 do 2 GHz. Njihovo število naj bi leta 2003 ali celo prej doseglo miljardo.
GPS (Global Positionining System) dela pri frekvenci 1,6 GHz. Nova zakonodaja bo vsaj v Angliji zahtevala vgraditev GPS v vse prenosne telefone.
Brezžična tehnologija kratkega dosega (Bluetooth) dela pri frekvenci 2,4 GHz in ima doseg okrog 10 m. Povezuje prenosne telefone z računalniki, računalnike med seboj, računalnik s tiskalnikom, senzorje s "pametnimi" karticami

itd. Ta tehnologija ponuja standard, ki ga bo verjetno osvojila večina proizvajalcev naprav. Zato je predviden obseg proizvodnje še večji kot pri prenosnih telefonih. Zanimivo je, kako je dobila ime Bluetooth (modri zob). Razvijati so jo začeli pri skandinavski firmi Ericsson in so jo imenovali po danskem vikinškem kralju Haroldu Modrozobem, ki je vladal od 950 do 986. Kralj naj bi bil znan po tem, da je znal prepričati sprte ljudi, da so sedli skupaj in se pogovorili, namesto da bi se vojskovali. Torej, komuniciranje na kratke razdalje.

Zahteve za LTCC folije, ki se uporabljajo v mikrovalovnih aplikacijah, so: dielektrična konstanta med 8 in 10, nizki izgubni koti, temperaturna stabilnost dielektrične konstante oziroma centralne frekvence in zelo enakomerna debelina folije. Pri Heraeusu so razvili material z oznako CT2000, za katerega upajo, da bo postal industrijski standard. Dielektrična konstanta 9,1 je višja od večine primerljivih materialov in ravno v sredi zaželjenega "okna" vrednosti, frekvenčni temperaturni koeficient je pod $10x10^{-6}/K$ in ponovljivost debeline folije po žganju je +/- 2%. Za primerjavo omenimo, da je zajamčena toleranca debeline Al_2O_3 substratov, ki jih proizvajalci v zelo velikih količinah izdelujejo za debeloplastno hibridno tehnologijo, precej širša, do 10%. Zraven so razvili še srebrne paste, ki s sitotiskom (100 μm linije) ali foto postopkom (50 μm linije) omogočajo izdelavo prevodnikov z nizko upornostjo in predvsem z zelo ostro definiranimi robovi.

L. Davlin s kolegi (Plextek Ltd. in C-MAC, obe firmi iz Anglije) je v referatu z naslovom "Low cost RF and microwave components in LTCC" predstavil preiskave in analizo LTCC struktur pri frekvencah do 28 GHz. V uvodi je povedal, da so pri izdelavi MCM-C s temi materiali glavni problemi s skrčki zloženih folij med žganjem, ki so med 12% in 16% v "X" in "Y" smeri in celo več v "Z" smeri. Nekateri proizvajalci razvijajo materiale za folije, ki se med žganjem ne bi krčile (zero-shrink). Ne on ne prej omenjeni predavatelj pa nista hotela komentirati, kako so ti materiali narejeni. Testirali so tako organske polimerne materiale za tiskana vezja kot LTCC folije različnih proizvajalcev (Heraeus, Du Pont, EMCA, Ferro). Organski kompoziti imajo dielektrične konstante med 2 in 4 ter izgube med $4x10^{-4}$ in $27x10^{-4}$. Dielektrične konstante LTCC materialov so med 6 in 8, izgube pa med $5x10^{-4}$ in $40x10^{-4}$. Za primerjavo, 99,6% Al_2O_3, ki je skoraj univerzalni substrat za hibridna debeloplastna vezja, ima dielektrično konstanto 9,9 in zelo nizek izgubni kot, $4x10^{-4}$. Uporaba zlatih in srebrnih debeloplastnih prevodnikov v različnih testnih strukturah je pripeljala do podobnih rezultatov. S srebrom so bile izgube nižje zaradi višje specifične prevodnosti. Seveda pa toleranca sitotiska oziroma ponovljivost geometrije prevodnih linij (širina +/- 10 μm in debelina +/-1 μm) določa do neke mere toleranco izgub.

B. Bober (Wroclaw University of Technology, Poljska) je v referatu z naslovom "Investigations of assembly properties of conductive layers in LTCC circuits" predstavila testiranje kombinacij LTCC folij (trije materiali) in debeloplastnih prevodnikov (dva na osnovi Ag in eden na osnovi Pd/Ag) različnih proizvajalcev. Vseh devet LTCC struktur je bilo žganih najprej nekaj ur na 400°C (razplinjevanje) in nato 10 do 20 min pri 850°C. Mikrostrukture prevodnikov so pokazale, da se nekatere kombinacije srebra in LTCC folij ne "ujamejo". Prevodnik je bil slabo zasintran in/ali pokrit s stekleno fazo, kar je otežilo ali onemogočilo tako spajkanje kot bondiranje z Au ali Al žičko. Zanimivo je, da do teh problemov ni prihajalo pri kombinacijah s Pd/Ag prevodnikom. Različna mikrostruktura istega prevodnika na različnih folijah je bila pripisana ralzličnim profilom žganja. Predavateljica zaenkrat ne ve, ali steklena faza na površini Ag prevodnika izhaja iz prevodnika ali pa je med žganjem difundirala iz LTCC keramike v prevodnik.

P. Barrett (Kingston University, Anglija) je imel referat z naslovom "Narow bandwidth, high frequency, band pass filter using thin film and thick film technology". V prispevku je predstavil delo študentov na njihovi univerzi. Tu omenim, da sodelavci univerze vsako leto na tej konferenci predstavijo zaključen študentski projekt. Naloga je bila, da študenti izračunajo in načrtajo mikrovalovni pasovni filter s centralno frekvenco 9,75 GHz in širino pasu 0,1 GHz, ki ga že izdelujejo v tankoplastni tehnologiji (Thomson Racal Defence Ltd). Filter so izdelali v debeloplastni tehnologiji z metodo foto oblikovanja, ki omogoča zelo dobro definicijo robu prevodnih linij. Fotoobčutljive debeloplastne paste po tiskanju in sušenju osvetlijo skozi maske z ultravijolično svetlobo, ki sproži polimerizacijo v organskem materialu. Nepolimerizirane dele natiskane plasti nato sperejo z vodo. Nadaljni postopki so isti kot pri izdelavi debeloplastnih hibridnih vezij. To je tehnologija, ki uspešno kombinira zrel način debeloplastne tehnologije z natančnostjo fotolitografije. Dosegljive ločljivosti tako odprtin za povezovanje (vias) kot širine prevodnih linij so nekaj deset mikrometrov. Metoda omogoča dobro definicijo linij, je pa razmeroma draga, ker se "zavrže" nepolimeriziran material. Primerjali so električne karakteristike tenkoplastnega filtra, izdelanega v Thomson Racal Defence na 99,6% Al_2O_3 in debeloplastnega filtra na običajni 96% Al_2O_3 keramiki. Karakteristike obeh so bile primerljive, majhen premik centralne frekvence proti višjim vrednostim za debeloplastni filter pa so pripisali različnim dilektričnim konstantam obeh keramik. V diskusiji je bilo omenjeno, da je eden problemov foto oblikovanja to, da se med žganjem rob prevodne linije včasih zvije stran od substrata.

Dva referata sta obravnavala mikrosisteme za "laboratorij na chipu" (Lab.on-a-chip). Referat "Modular integrated microsystems" (devet avtorjev iz šestih angleških laboratorijev oziroma podjetij) je poročal o integriranih senzorjih za analizo krvi. Na plastičnih substrati so izdelali 200 μm kanale in 300 μm odprtine, po katerih bo tekla tekočina, z mehanskim rezanjem. Na te substrate nato "z obrazom navzdol" pritrdijo chipe z mikrosenzorji. Avtorji iz National Microelectronic Research Cente, Irska, pa so v referatu z naslovom "Lab-on-a-chip; materials, processing, componet integration, assemly and packaging issues" poročali o novih tehnologijah in predvsem problemih pri izdelavi mikrostruk-

tur. Fotoobčutljivi materiali, na primer polimeri ali Li_2O/SiO_2 stekla, omogočajo izdelavo mikro kanalov precej ceneje kot mehanična obdelava. Laserske diode in detektorji se izdelajo v samih chipih za uporabo kot senzorji fluorescence. Predavatelji pa so poudarili, da je zaenkrat le malo laboratorijev-na-chipu na tržišču. Eden glavnih razlogov je "konzervativnost" medicine. Vsako stvar, najsi bo to novo zdravilo ali naprava, morajo preiskusiti in odobriti "odgovorna telesa". Navadno to traja pet ali več let, ker se precejšen čas porabi tudi za klinične teste, ki morajo potrditi, da so predlagane mikro naprave neškodljive in kompatibilne z zahtevami medicine.

J. Kowal (Applied Microengineering, Oxford, Anglija) je predstavil osnove anodnega bondiranja. Anodno bondiranjeje je kakih trideset let stara tehnologija, ki se je sprva uporabljala za tvorbo vezi med steklom in kovino. Steklo z dovolj visoko koncetracijo alkalnih ionov, v glavnem Na^+, pritisnejo na silicijevo rezino. Sendvič segrejejo na nekaj 100 stopinj Celzija, običajno na 300°C do 400°C. Pri tej temperaturi postane steklo ionski prevodnik (Na^+ ioni) in upornost mu pade do sedem velikostnih razredov. Na sendvič pritisnejo električno napetost med 100 V in 1000 V. Čas trajanja bondiranja je okrog pol ure; 15 do 20 min za segrevanje sendviča in okrog 5 min za visoko napetostno bondiranje. Natrijevi ioni difundirajo proti katodi (negativna napetost) in negativno nabiti kisikovi ioni proti anodi (pozitivna napetost). Na stiku med steklom in silicijem nastane okrog 1 μm debela plast, osiromašena na Na^+ ionih in zato s precej višjo upornostjo. Večina padca napetosti je sedaj preko tega tankega sloja. Kisikovi ioni so močno povlečeni k stiku, tako da nastane SiO_2 in s tem preko Si-SiO_2-steklo stika tvorijo vez med steklom in rezino silicija. Vez Si/SiO_2/steklo je močnejša od mehanske trdnosti stekla. Tu je vredno omeniti, da pri teh temperaturah steklo še ne "teče" viskozno, vendar ta elektrostatski privlak "zravna" možne površinske neenakomernosti silicija ali stekla, tako da stik postane intimen. Zaradi razmeroma visokih temperatur mora biti temperaturni razteznostni koeficient (TEC) stekla blizu TEC silicija, da pri ohlajanju struktura ne ukrivi. Drugi mehanizem, ki lahko pripelje do krivljenja sendviča, je difuzija Na^+ ionov stran od stika. Zato se steklo, obogačeno z Na^+, bolj raztegne kot "osiromašeno" steklo ob stiku. Če so na stiku med silicijevo rezino in steklom zaprti kanali, lahko zaradi kisika, ki izstopa iz stekla, naraste pritisk v njih tudi do nekaj 100 Barov, kar lahko raztrga stik. Če so že zapreti kanali ali "votline", naj bi bili čim globlji, da se minimizira ta učinek (približno pravilo je, da je varno 1 Bar na 1 um globine). Zanimivo je, da ta tehnika dela ne samo na siliciju, ampak tudi na SiO_2, silicijevem nitridu ali tantalovem nitridu (tankoplastni kondenzatorji). Če pa se steklo pritrjuje preko običajneja prevodnika na chipoh, to je napršen aluminij, pa se lahko ta oksidira v Al_2O_3 in prekine prevodne sledi.

V precej živahni diskusiji po referatu se je videlo, da ta tehnologija, ki "dela" že trideset let, še vedno ni dobro razumljena. Nekateri problemi so; če se na stiku silicij / steklo izloča mulekularni kisik, bi se na površini stekla moral izločati elementarni natrij, kar pa niso opazili. Prav tako ni znano, ali je meja ned Si in steklom ostra, to je, ali na atomskem nivoju preide iz kovinskega silicija v SiO_2 ali pa je ta prehod bolj difuzen preko vmesne plasti. Tudi mehanizem bondiranja na silicijevem ali tantalovem nitridu ni znan.

V našem referatu z naslovom "Diffusion-patterning technology and materials for thick-film ceramic MCMs" (avtorji M. Hrovat, Institut Jožef Stefan, Ljubljana in D. Belavič ter M. Pavlin, HIPOT, Šentjernej) smo predstavili pregled debeloplastnih materialov za difuzijsko oblikovanje. Difuzijsko oblikovanje je način izdelave večplastnih debeloplastnih vezij (MCM-C), ki omogoča doseganje večje gostote vezij z obstoječo tehnologijo sitotiska in žganja. Večplastno vezje, narejeno s to tehnologijo, je pri isti kompleksnosti 20% do 40% manjše od "navadnega" debeloplastnega večplastnega vezja. Podali smo rezultate karakterizacij materialov (dielektrikov, prevodnikov in uporov). Predstavili smo testna vezja in miniaturiziran senzor pritiska (MCM-C s štirimi prevodnimi ravninami), ki je bil izdelan s to tehnologijo. Omenimo, da so bile preiskave difuzijskega oblikovanja del triletnega projekta COPERNICUS "Cheap Multi Chip Modules" (Projekt N°: IC15-CT96-0743, DG 12-SNRD).

Naslednja konferenca "MicroTech 2002" bo konec januarja 2002 v Angliji.

PRIKAZ MAGISTRSKIH DEL IN DOKTORATOV V LETU 2000
M. S. and Ph. D. ABSTRACTS, YEAR 2000

MAGISTRSKA DELA

Naslov naloge: **Generator za sintezo govornega signala**

Avtor: **Damjan Šonc**

Mentor: **prof. Dr. Dušan Kodek univ.dipl.ing.**

Univerza v Ljubljani, Fakulteta za računalništvo in informatiko

V nalogi je opisan visoko kakovostni generator govornega signala, ki sloni na sinusnem govornem modelu. V tem modelu je govorni signal predstavljen z vsoto sinusnih sestavin poljubnih frekvenc, amplitud in faz.

Potrebne vrednosti frekvenc, amplitud in faz za krmiljenje generatroja v sestavnem delu sistema smo pridobili z analizo naravnega govornega signala. Pri analizi smo uporabili različne nabore KEO filtrov, katerih značilnosti podaja tabela 1 v poglavju 3.1.2. Vse signale smo, razen tam, kjer je to posebej označeno, vzročili s frekvenco 16kHz in jih kvantizirali na 16 bitov natančno. Izhode iz nabora KEO filtrov smo v raznih preizkusih računali v časovnih razmikih od 5 do 50ms. Te izhodne vrednosti so predstavljale množico parametrov analiznega okvirja. V nalogi smo obdelali tudi metode za interpolacijo parametrov med posameznimi analiznimi okvirji. Za ujemanje frekvenc med okvirji smo uporabili poseben ujemalni algoritem (poglavje 2.3.1), amplitude smo interpolirali z linearno interpolacijo (poglavje 2.3.2.1), fazne prehode pa smo interpolirali s kubičnimi polinomi (poglavje 2.3.2.2).

Namesto frekvenčnih vrhov spektrograma kot v [4], smo kot merilo za izbor frekvenc izbrali vsoto energijskih prispevkov η najmočnejših frekvenčnih sestavin, s čimer smo dosegli pomembno izboljšanje kvalitete umetno sestavljenega govora. Vrednost za η se je gibala v intervalu $0.5 \leq \eta \leq 0.99$. Z vrednostmi amplitud in faz, dobljenimi pri analizi naravnega govornega signala smo krmili sinusni generator podan z enačbo (9).

Kakovost govornega signala, ki smo jo lahko dosegli z generatorjem govornega signala slonečem na sinusnem govornem modelu, je bila skoraj enaka kakovosti naravnega govornega signala. Rezultati so pokazali, da je pri naboru 393 filtrov, časovnem razmiku med okvirji t = 5ms, vrednostjo η = 0.95 ter pri časovnem razmiku med okvirji t = 10ms in vrednostjo η = 0.99 , poslušalec šele pri pazljivem poslušanju delno razločeval med naravnim in umetno sestavljenim govorom, pri istem naboru filtrov, časovnem razmiku med okvirji t = 5ms in vrednostjo η = 0.99 , pa ni več ločil naravnega in umetno sestavljenega govora.

S testi smo preizkusili tudi uporabnost generatorja na različnih signalih. Prepričali smo se, da je generator primeren tudi za umetno sestavo širše skupine signalov, ki jih lahko predstavimo kot vsoto sinusnih sestavin, in ki zajemajo na primer: govor skupine ljudi, razne živalske glasove in glasbo. Z njim lahko dobro modeliramo omejene signale tudi, če je v njih prisoten šum.

Glavna pomanjkljivost generatorja in zaradi tega tudi najpomembnejši problem, ki je naloga nadaljnjih raziskav, je zmanjšanje števila potrebnih parametrov za enako kvaliteto umetnega govornega signala. O grobi oceni, ki izhaja iz števila glasniških parov slovenskega govora, povprečnega števila parametrov pri sestavi ter povprečne dolžine glasnikov, bi za hranjenje parametrov generatorja za visoko kvalitetno sestavo (razmik med okvirji 5ms, nabor 393 filtrov, energijski prispevek η = 0.99) umetnega govora s pomočjo metode lepljenja potrebovali 130MB pomnilniškega prostora. Če bi namesto glasniških parov uporabljali glasniške trojke, bi se zahteve po prostoru povečale na 3.6GB.

Kljub večji računski in prostorski zahtevnosti od drugih znanih metod (PSOLA, LPC), je generator zaradi izredne kakovosti umetno sestavljenega signala in enostavnosti zelo primeren za nizko-nivojski del sistema za sestavo umetnega govora iz besedil, posebno za sistem, ki lepi in preoblikuje vnaprej posnete delčke naravnega govora. V teh sistemih lahko popolnoma izrabimo metode interpolacije parametrov med okvirji opisane v poglavju 2.3, ki zagotavljajo kakovostno izvedene prehode med odseki, brez umetnih dodatkov kot so poki, zvenenje in drugi.

Naslov naloge: **Digitalni števec električne energije**

Avtor: **Simon Balanč**

Mentor: **Doc.dr.Franc Bergelj**

Univerza v Ljubljani, Fakulteta za elektrotehniko

Magistrsko delo obravnava merjenje električne energije na digitalen način. Cilj dela je izdelati števec električne energije razred 2.0, izmeriti rezultate števca in izračunati negotovost meritve.

V uvodu sem nakazal, kako je sploh prišlo do ideje o izdelavi popoloma digitalnega števca in kakšni so bili predhodni poskusi.

V glavnem delu sem najprej pokazal, kako so električno energijo merili še takrat, ko je bila distribucija in poraba še v povojih. Nato sem opisal različne elektronske načine merjenja energije, ki so trenutno v uporabi ali so bili vsaj raziskani kot možni načini.

Nato sem opravil analizo trga, kjer že nekaj let poskušajo prodreti najrazličnejše firme z lastnimi integriranimi vezji za merjenje energije. Zbral sem jih v tabeli in primerjal glede merjenih funkcij.

Največji in najpomembnejši del je opis števca električne energije ED500. Najprej so podani gradniki sistema, kot je procesor in AD pretvornika kot najpomembnejši členi. Nato so opisani še merilni vhodi, pa čelna plošča, izhodni kanali in tako naprej. Z meritvami sem pokazal, da je možno narediti števec, ki bo merilno ustrezal standardu za statične števce razreda 0.2. Hkrati sem podal tudi primerjavo s simulacijami v MathCadu. Preveril sem samo obremenilno krivuljo pa tudi občutljivost na vplivne veličine kot so napajalna napetost, sprememba omrežne frekvence, po drugi strani pa tudi zmožnost merjenja z različnimi resolucijami AD pretvornikov in frekvencami vzročenja. Izkaže se, da je 14 bitni AD pretvornik ravno še dovolj za tokovno dinamiko 1:600.

Na koncu sem opisal še sledljivost enote za električno energijo in primerjavo enot enkrat na svetovnem in enkrat na evropskem nivoju in pokazal, kako se izračuna negotovost števca in kam v merilno piramido je pripet etalon TEMP-100, s katerim sem ED500 meril.

Naslov naloge: **Avtomatska impedančna merilna priprava za nadzor parametrov kondenzatorjev v proizvodnji**

Avtor: **Dušan HABE, univ. dipl. inž. el.**

Mentor: **prof. dr. Anton JEGLIČ**

Univerza v Ljubljani, Fakulteta za elektrotehniko

V magisterskem delu je obravnavan način reševanja ozko namenske merilne priprave za merjenje kapacitivnosti faktorja kondenzatorjev. Uporaba in lastnosti merilne priprave so strogo podrejene zahtevam serijske proizvodnje visokokvalitetnih kondenzatorjev. Osnovne zahteve za merilno pripravo so podane z zahtevano točnostjo, postavljeno končno ceno in uporabo v merilnih avtomatih. Pri tem nastopita kot kritična parametra zelo nizka vrednost izgubnega faktorja, ki ga moramo meriti in potrebna dovolj visoka hitrost merjenja. Postavljene meje za meritve izgubnega faktorja in zahtevana točnost segajo do skrajnih možnosti današnje merilne tehnike.

Tematsko ima naloga dva dela. V prvem delu po pregledu profesionalnih impedančnih merlinikov sledi obravnava novejše strokovne literature iz tematike merjenja kapacitivnosti in izgubnega faktorja kondenzatorjev. V nadaljevanju sledi analiza primernih merilnih metod. Njihovo ovrednotenje je podano s pomočjo simulacij in z izdelavo prototipnih rešitev merilnih priprav.

Ob določitvi merilne metode so opravljene še ostale ustrezne analize. Te določajo pogoje za izbiro potrebne aparaturne opreme. Delovanje merilne priprave omogoča močna programska podpora, izvedena na osnovi najnovejših programskih orodij.

V drugem delu je nakazana dokončna rešitev za izdelavo merilne priprave. Uporabljene so večnamenske vstavne kartice v osebnem računalniku. Ta osnovi skrbi za delovanje merilnega avtomata. S tem, ko je računalniku dodana še funkcija merjenja, to prispeva k znižanju cene merilnega avtomata v primerjavi z vgrajenim samostojnim merilnikom.

Naslov naloge: **Integrirani nadzorni in krmilni mikrosistem**

Avtor: **Uroš BIZJAK, univ. dipl. Inž. el.**

Mentor: **prof. dr. Baldomir ZAJC**

Univerza v Ljubljani, Fakulteta za elektrotehniko

Namen magistrske naloge je izdelava nadzornega in krmilnega vezja vključenega mikrosistema. Sistem bo izveden v hibridni softversko-hardverski arhitekturi, sestavljen pa bo iz programabilnega mikroprocesorskega jedra in optimiziranih hardverskih podsklopov, s katerimi razbremenimo delovanje mikroprocesorja.

V prvem delu naloge je predstavljen sistemski model, sledi pa analiza sistemskih procesov s pomočjo data-flow grafov. Glede na omejitve, ki jih postavlja delovanje procesov v realnem času, funkcionalnost sistema razdelimo na softverske in hardverske komponente.

Rezultati sistemske analize in simulacij procesov nam služijo kot vodilo pri načrtovanju posameznih komponent; izvedene optimizirane hardverske podsklope z nizkonivojskim V/I gonilnimi rutinami povežemo v funkcionalno celoto. Želimo, da je celoten sistem izveden na kar najmanjši končni geometriji, delovanje V/I rutin pa naj kar najmanj obremenjuje integrirano mikrojedro.

Funkcionalnost celotnega sistema je združena na enem integriranem vezju, hardverski del je načrtan z uporabo načrtovalskega paketa Cadence/Verilog, softverske rutine pa so bile razvite s pomočjo GNU Compiler Collection paketa in prevedene z razvojnim sistemom winuSim za MTC-8308 mikrojedro.

Naslov naloge: **Razpoznavanje oseb na osnovi analize vzorcev šarenice človeškega očesa**

Avtor: **Marko Knez, univ. dipl. inž. el.**

Mentor: **Prof.dr.Stanislav Kovačič, dipl.ing.**

Univerza v Ljubljani, Fakulteta za elektrotehniko

Pričujoče magistrsko delo obravnava širšo problematiko biometrike in biometričnih metod. Najprej je podan zgodovinski pregled in razvoj omenjenega področja. V nadaljevanju so podane temeljne lastnosti in zahteve, ki jih morajo izpolnjevati vse biometrične metode ter našteti in razloženi osnovni pojmi ter nekatere definicije, nujno potrebne za razumevanje področja. Sledi predstavitev ter nekoliko podrobnejši opis posameznih biometričnih metod z njihovimi prednostmi in slabostmi ter samim postopkom, ki je specifičen za vsako od njih. Na koncu predstavitvenega dela bio-

metričnih metod, je podan primerjalni pregled metod glede na posamezne pomembnejše lastnosti. Na podlagi opisa je moč hitro ugotoviti primernost določenega postopka gede na zahteve za izbrano okolje in pogoje, v katerih bo sistem deloval ter predvsem primernost glede na zahteve po zanesljivosti in varnosti. Podane so tudi matematične osnove za objektivno vrednotenje in primerjanje biometričnih metod.

Osrednji del pričujočega dela natančneje obravnava tematiko identifikacije oseb na osnovi določanja, razpoznavanja in vrednotenja vzorcev ter značilnosti šarenice človeškega očesa. V celoti je opisan avtomatski postopek razpoznavanja oseb vse od zajema vhodne slike do rezultata razpoznave. Opisani sistem je v laboratorijskem okolju tudi praktično realiziran in delujoč. Predstavljeni so testi, rezultati ter ugotovitve, do katerih smo prišli tekom izdelave sistema in obravnavanja tematike identifikacije.

Naslov naloge: **Nadgradnja magnetometra na principu jedrske magnetne resonance**

Avtor: **Janez HUMAR, univ. dipl. inž. el.**

Mentor: **Prof. dr. Dušan FEFER**

Univerza v Ljubljani, Fakulteta za elektrotehniko

Vsaka merska enota ima svojo definicijo, realizacijo in predstavitev. Definicija je idealna vrednost, ki je ponavadi vključena v Mednarodni Sistem Enot SI. Realizacija je dosežena s poskusi, katerih rezultat naj se čim bolj skladajo z definicijo. Bolj ko se rezultati uporabljene metode skladajo z definicijo, višje se ta metoda nahaja v metrološki hiearhični piramidi.

Na področju merjenja nizkih gostot enosmernega magnetnega pretoka se uporablja kar nekaj različnih metod (Hallov senzor, fluxgate metoda, resonančne metode,...). Največje točnosti dosegamo z resonančnimi metodami, se pravi z metodami, ki izkoriščajo princip jedrske magnetne resonance (JMR). Pojav jedrske magnetne resonance je sicer že star vendar pa vse bolj prodirajoča digitalna tehnika omogoča nove rešitve za izdelavo tovrstnih magnetometrov. Prednosti je pričakovati predvsem pri povečanju hitrosti izvajanja meritev, lažjemu shranjevanju merilnih rezultatov in nenazadnje miniaturizaciji samega merilnega sistema.

V grobem gre pri uporabi jedrske magnetne resonance za zaznavanje pojava resonance med precesirajočimi jedri v snovi (voda) ter zunanjim vzbujajočim izmeničnim magnetnim poljem. Frekvenca zunanjega izmeničnega vzbujajočega polja pri kateri pride do resonance je premo-sorazmerna z merjeno gostoto statičnega magnetnega pretoka. Na ta način merjenje gostote magnetnega pretoka prevedemo na merjenje frekvence, ki pa jo znamo meriti zelo točno. Signali, ki jih dobimo pri postopku zaznave resonance (v nadaljevanju jih bomo imenovali signali JMR), so pri majhnih gostotah merjenega magnetnega pretoka zelo šibki in dobro skriti v zelo močnem šumnem ozadju. To pa je tudi največja omejitev pri merjenju majhnih gostot magnetnega pretoka.

Z analogno tehniko se da izvesti le malo metod za izločanje koristnega signala iz šuma pa še te zahtevajo zelo komplicirana vezja. Drugačna zgodba je, ko se spustimo na področje digitalne tehnike. Matematične operacije, ki so zelo uporabne za izločanje koristnega signala iz močnega šumnega ozadja, so veliko laže izvedljive z digitalnimi podatki ,kot pa z analognimi signali. Metode kot so konvolucija, korelacija, fouierjeva analiza,... je v analogni tehniki skoraj nemogoče realizirati, v digitalni tehniki pa so to čisto vsakdanje stvari.

Preden pa signale začnemo digitalno obdelovati, jih je potrebno pretvoriti v digitalno obliko. Ta del naloge je zelo pomemben, saj še tako dobre metode obdelave digitalnih signalov nič ne pomagajo, če je pretvorba iz analognega v digitalni svet popačena.

V uvodnem delu magistrske naloge so predstavljene fizikalne osnove jedrske magnetne resonance. Temeljni lastnosti atomskih jeder, kotni moment ali spin I in magnetni moment μ, definirata giromagnetno razmerje γ_p, kot temeljno konstanto eksperimentov jedrske magnetne resonance.

Delovanje JMR magnetometrov temelji na fizikalnem principu jedrske magnetne resonance. Vzorec, ki je del sonde JMR magnetometra, vsebuje atomska jedra. Ko vzorec postavimo v enosmerno merjeno magnetno polje, se magnetni dipoli nekaterih jeder postavijo v smeri tega polja, nekateri v obratni smeri. V novi smeri magnetni dipoli atomskih jeder precesirajo, pravimo, da imajo spin.

Teorija jedrske magnetne resonance pravi, da je frekvenca recesiranja ali vrtenja okoli nove smeri odvisna samo od vrste jedra in od gostote enosmernega magnetnega pretoka zunanjega polja B_0. Do pojava jedrske magnetne resonance pride, ko vzorcu dovajamo energijo v obliki izmeničnega magnetnega polja enake frekvence, kot je frekvenca precesiranja magnetnih dipolov atomskih jeder. Izmenično magnetno polje generiramo s pomočjo zunanjega visokofrekvenčnega sinusnega generatorja. Frekvenca precesiranja magnetnih dipolov atomskih jeder se imenuje tudi Larmorjeva frekvenca ω_L. Najpomembnejša enačba $\omega_L = \gamma \cdot B_0$ linearno povezuje dve snovni veličini, gostoto magnetnega pretoka ter frekvenco, preko temeljne konstante jedrske magnetne resonance γ, ki se imenuje Giromagnetno razmerje. Giromagnetno razmerje je razmerje med jedrskim kotnim momentom (spinom) in jedrskim magnetnim momentom in prestavlja snovno konstanto, oz. osnovno fizikalno konstanto, ki je značilna za atome določenih kemičnih elementov. Neznano magnetno polje gostote magnetnega pretoka B_0 tako lahko merimo z merjenjem Larmorjeve frekvence ω_L, pri čemer moramo poznati konstanto γ.

V nadaljevanju dela je nazorno prikazan merilni postopek pri uporabi magnetometra na principu jedrske magnetne

resonance. Podrobno razumevanje delovanja magnetometra je pomembno za njegovo kasnejšo nadgradnjo ter izboljšavo. Predstavljeni so značilni signali JMR ter način, kako do njih pridemo. Prikazane so značilnosti ter s tem meritve naslanja na obdelavo teh signalov, je njihovo poznavanje zelo pomembno. V ta namen je v tem delu prikazan postopek določitve trenutka nastopa resonance.

Opisano je delovanje fazno-občutljivega ojačevalnika. Z njegovo pomočjo iz signalov JMR izločimo podatke o nastopu resonance. Izhod iz fazno-občutljivega ojačevalnika nam namreč da informacijo o tem, kako blizu resonance se nahajamo. Poleg tega pa poskrbi tudi za izločitev koristnega signala iz šuma. To pomeni, da z njim močno popravimo razmerje signal/šum.

Z modeliranjem omenjenih signalov lahko simuliramo postopek zaznave resonance. Pri tem imamo opraviti z diskretnimi signali. Glede na to, da je naloga tega magistrskega dela digitalna obdelava signalov JMR, je delo z diskretnimi signali zelo nazorna simulacija realnega dela. Do signalov JMR pridemo s pomočjo množenja (modulacije) sinusnega (modulacijskega) signala preko absorpcijske (resonančne) krivulje, ki jo v okolici resonančne krivulje opišemo z Lorentzovo krivuljo. Značilna zvonasta oblika Loerntzove krivulje predstavlje množino energije, ki jo vzorec absorbira v odvisnosti od bližine frekvence ω zunanjega vzbujajočega izmeničnega magnetnega polja, Larmorjevi frekvenci ω_L.

S pomočjo simulacije lahko študiramo vplive naključnega šuma, izmeničnih parazitnih signalov (npr. Motnje omrežne napetosti) in vplive sprememb statičnega magnetnega polja (bližina kovin, bližina močnostnih vodnikov) na obdelavo signala JMR ter tako točnost meritev.

V nadaljevanju simulacije, bomo uporabili realen povzročen signal, katerega bomo vzročili s pomočjo VXI sistema (platforma VXI-1500 ter 10MHz vzročevalnik HP 1430A). Za programsko podporo zajema signala smo izbrali programski paket LabView. Diskretne vrednosti povzročenega signala smo nato, podobno kot prej, obdelali v okolju MIT-LAB, kjer smo dobili koristne informacije za nadaljnje delo.

Prikazana je še ena možna oblika zaznavanja resonance s pomočjo signala JMR. In sicer uporaba spektralne analize. S pomočjo Fourierove transformacije se da določiti kdaj nastopi resonanca, vendar zaenkrat le pri sorazmerno močnih signalih, ki jih dobimo pri merjenju večjih gostot magnetnega pretoka. Vendar pa je metoda obetavna in ji bomo v prihodnosti posvetili več pozornosti.

Prva naloga pri nadgradnji obstoječega magnetometra je pretvorba analognega signala JMR v digitalno obliko. Vzročenje, oziroma zajemanje signala v diskretnih časovnih razmakih je osnova za realno-časovno signalno procesiranje. Veliko pozornosti je namenjeno zgradbi analognega filtra, s katerim je pred vzorčenjem potrebno izločiti tisti del neželenega spektra, ki bi povzročil prekrivanje spektra vzročnega signala (aliasing) znotraj pasovne širine koristnega signala. Tu nam prav pride poznavanje lastnosti signala JMR. Nato je prikazan sistem za analogno/digitalno pretvorbo, pri kateri smo uporabili analogno/digitalni pretvorik proizvajalca Burr Brown, DSP101, ki je prirejen za delo z digitalnimi signalnimi procesorji. Podani so pomembni napotki za sestavo takega sistema, ki je zelo občutljiv na vrsto dejavnikov (priključitev mas ter napajanja, filtriranje napajanja, način ločitve analognega ter digitalnega dela,...).

Cilj magistrske naloge je bilo določiti trenutek nastopa resonance s pomočjo digitalne obdelave signalov jedrske magnetne resonance. V ta namen smo uporabili DSP razvojni sistem (Aplication Development Module) proizvajalca Motorola, ADM 96000, ki vsebuje 96-bitni IEEE Floating-Point digitalni signalni procesor DSP96002. Prikazana je izvedba posameznih modulov potrebnih za delovanje sistema ter delovanje programa, ki podpira delovanje celotnega sistema.

Na koncu bodo podani rezultati dela, primerjava novega sistema z obstoječim ter razvojne smernice k nadaljnjim izpopolnitvam magnetometra. Nadaljevanje raziskovalnega dela na področju nadgradnje magnetometra bo temeljilo pretežno na izpopolnjevanju digitalne obdelave signalov JMR. Potrebno bo izvesti rutine kot so filtriranje, fouierova analiza,..., s katerimi bomo omogočili razširitev merilnega območja magnetometra ter izboljšanje njegovih metroloških lastnosti. Najpomembnejši del bo predstavljal algoritem, ki bo ob sorazmerno hitrem preletu resonančne krivulje z veliko točnostjo zaznal, v katerem trenutku nastopi resonanca. Poleg tega bo potrebno izvesti način za zajem merilnih podatkov ter njihovo analizo.

Naslov naloge: **Izpostavljenost in zaščita ljudi in naprav v okolju električnih magnetnih polj elektroenergetskih omrežij**

Avtor: **Marko Istenič, univ. dipl. inž. el.**

Mentor: **prof.dr. Peter Žunko**

Somentor: **doc.dr. Peter Kokelj**

Univerza v Ljubljani, Fakulteta za elektrotehniko

Naše bivalno in delovno okolje se pogosto nahaja v bližini elektroenergetskih omrežij. Elementi elektroenergetskih omrežij v prostor oddajajo elektromagnetno valovanje frekvence 50/60 Hz, ki predstavlja del elektromagnetnega frekvenčnega spektra neioniziranih sevanj. Primeri iz prakse kažejo, da lahko elektromagnetno valovanje, ki ga oddajajo elementi elektroenergetskih omrežij, povzroča motnje v delovanju nekaterih električnih naprav ali pri prenosu informacij (telekomunikacijski kabli). Od začetka sedemdesetih let pa se veliko raziskav posveča tudi morebitnim škodljivim vplivom elektromagnetnih polj na biološke organizme. Eden izmed najpomembnejših načinov za smotrno reševanje teh problemov je zaščita pred elektromagnetnim sevanjem. Poznamo več vrst zaščite, ki skušajo na učinkovit in sprejemljiv način zmanjšati vpliv med virom sevanja in prostorom oziroma objektom, ki ga hočemo ščititi.

Določanje izpostavljenosti elektromagnetnemu polju v bivanjskem ali delovnem okolju ljudi je osnovni pogoj za vse nadaljnje raziskave (epidemiološke raziskave, raziskave na prostovoljcih in laboratorijske študije), načrtovanje zaščite, določanje dopustnih mejnih vrednosti ter tudi oceno zdravstvenega tveganja. Za določanje izpostavljenosti elektromagnetnemu polju elementov elektroenergetskih omrežij smo definirali matematični model, ki smo ga uporabili pri analizi izpostavljenosti elektromagnetnemu polju med kmetijskimi opravili. Glavni vzrok za raziskave izpostavljenosti kmetovalcev je bila njihova specifična narava dela (na prostem, tudi v okolju daljnovodov) ter relativno velik delež te poklicne skupine v splošni populaciji (v Sloveniji okrog 12% prebivalstva). V analizi izpostavljenosti smo uporabili eksperimentalno določene faktorje dejavnosti ter faktorje obremenjenosti posameznih prenosnih daljnovodov, ki jih zbira Elektrogospodarstvo Slovenije. Oceno izpostavljenosti smo izračunali iz statističnih podatkov, ki jih zbirajo na Statističnem uradu Republike Slovenije, ter iz geografskih podatkov o prenosnih daljnovodih v Sloveniji.

Reševanja naloge oblikovanja zaščite smo se lotili z metodo digitalne simulacije, ki je pri raziskavah in razvoju delovanja in vplivov elektroenergetskih omrežij eno največkrat uporabljenih orodij. Ob uporabi te metode se moramo nenehno zavedati, da je natančnost rezultatov digitalnih simulacij neposredno odvisna od ustreznosti modelov, s katerimi predstavimo elemente sistema. Načrtali smo več različnih modelov zaščite za zmanjševanje magnetnega polja transformatorske postaje, ki so namenjeni za uporabo v programskem orodju EMAS.

Če želimo z digitalno simulacijo, ki temelji na metodi končnih elementov, opazovati razporeditev magnetnega polja v okolici transformatorske postaje, moramo pri načrtovanju modela postaje prispevke posameznih elementov pravilno ovrednotiti, saj bi bil detajlni model celotne postaje zelo zapleten. V našem primeru, ko nas zanima razporeditev magnetnega polja zunaj transformatorske postaje, je dovolj, če za vir magnetnega polja upoštevamo le vodnike, ki vodijo od sekundarja transformatojra do nizko-napetostne omare. Pri simulacijah se je izkazalo, da ob znatno enostavnejšem modelu, ki bistveno skrajša simulacijski čas, ne izgubimo nobene pomembne informacije o razporeditvi magnetnega polja v okolici transformatorske postaje, tudi pri načrtovanju zaščite.

Naslov naloge: **Visokonivojska sinteza vezij z genetskimi algoritmi**

Avtor: **Gregor Papa, univ. dipl. inž. el.**

Mentor: **prof. dr. Franc Bratkovič**

Univerza v Ljubljani, Fakulteta za elektrotehniko

V nalogi je predstavljen postopek načrtovanja digitalnih vezij z visokonivojsko sintezo. Poudarek je na osrednjem delu načrtovanja, ki ga sestavljata razvrščevanje in dodeljevanje. V ta namen je bil izdelan nov optimizacijski algoritem, ki vsebuje nekaj bistvenih prednosti drugih obstoječih algoritmov. Predvsem so tu izpostavljene hitrost, vsestranskost in robustnost.

V uvodnem poglavju so podani nekateri osnovni pojmi razvrščanja in dodeljevanja v visokonivojski sintezi ter optimizacije, ki so potrebni za razumevanje delovanja novega algoritma in njegovih posameznih funkcij. V tej nalogi sta zaradi svoje pomembnosti pri načrtovanju obravnavana in obširneje predstavljena procesa razvščanja in dodeljevanja.

Drugo poglavje ponuja nekaj bistvenih značilnosti algoritmov za razvrščanje ter njihovo razvrstitev. Prestavljeni so tudi nekateri pomembnejši algoritmi, ki se pojavljajo v literaturi in so v tej nalogi tudi uporabljeni. Ob tem so izpostavljene prednosti posameznih algoritmov ter njihovih različic. Nakazana je tudi prednost naključnosti algoritma.

Tretje poglavje vsebuje opis genetskih algoritmov. Predstavljen je njihov izvor, njihove funkcije ter načini njihovega delovanja. Glede na različne izvedbe posameznih funkcij obstaja tudi več vrst genetskih algoritmov, ki pa se med seboj razlikujejo le v izvedbi teh funkcij, medtem ko ostaja način delovanja enak - evolucijski.

Celotno četrto poglavje je posvečeno primerjavam in ocenam posameznih algoritmov. Preko primerjalnih opisov v tabelah in grafih je nakazan vzrok za izgradnjo novega algoritma na temelju genetskih algoritmov, saj so se izkazali za učinkovite tako na področju izrabe gradnikov kakor tudi pri računski zahtevnosti algoritma.

Peto poglavje vsebuje podroben opis novega algoritma MOGS. Ta večkriterijski algoritem za razvrščanje upošteva pri delu posamezna pravila, s katerimi dosega rezultate, primerne za proces dodeljevanja. Podrobno so predstavljene tudi posamezne funkcije, način njihove izvedbe ter vzroki in posledice izbire teh funkcij oziroma načinov njihovega delovanja. Glede na podobne obstoječe algoritme ima opisani algoritem spremenjeno cenovno funkcijo, saj pri delu upošteva tudi tiste gradnike vezja, ki na razvrščanje nimajo neposrednega vpliva (registri, vodila).

V šestem poglavju je algoritem MOGS ovrednoten s stališča hitrosti, učinkovitosti in primernosti za uporabo pri načrtovanju digitalnih vezij. V ta namen je bilo sestavljenih nekaj testnih vezij, ki preskušajo delovanje algoritma ter preverjajo njegove zmožnosti. Algoritem MOGS se je v primerjavi z drugimi algoritmi izkazal za uspešnega na vseh preskusnih področjih.

V zadnjem poglavju so podane ocene novega algoritma s stališča drugih postopkov v okviru visokonivojske sinteze ter nekatere pomembnejše smernice za iskanje novih poti pri razširitvi ter dodelavi predstavljenega algoritma.

Naslov naloge: **Sledenje in kodiranje oblike video objektov**

Avtor: **Janez Zaletelj, univ. dipl. inž. el.**

Mentor: **prof. dr. Jurij F. Tasič**

Univerza v Ljubljani, Fakulteta za elektrotehniko

Cilj standardov digitalnega kodiranja avdiovizualnih podatkov je doseganje čim višjih stopenj zgoščevanja podatkov, ki naj ob enaki ali izboljšani kvaliteti slike in zvoka glede na analogni prenos omogočijo sprejem slike in zvoka preko različnih vrst komunikacijskih kanalov. S pojavom večpredstavnih podatkovnih baz, videa na zahtevo, interaktivne televizije ter čedalje širše uporabe ne samo avdio, pač pa tudi vizualnih komunikacij, pa se postavljajo nove zahteve glede funkcionalnosti, ki naj jih standardi za kodiranje omogočajo, saj želimo imeti možnost vsebinskega dostopa do podatkov.

Najnovejši standard na področju digitalnega kodiranja videa vpeljuje nov semantični model video podatkov. Video ne predstavlja več preprostega zaporedja slik, ampak vsoto posameznih avdiovizualnih objektov. Takšen model omogoča npr. učinkovitejše urejanje video posnetkov, pa tudi iskanje po večpredstavnih podatkovnih bazah na osnovi vsebinskih značilnosti posameznih objektov. Pri tem je potrebno rešiti problema izločanja (segmentacije) video objektov iz slike ter učinkovitega kodiranja dodatne informacije, ki jo predstavlja oblika objektov.

Koncept magistrske naloge s področja digitalnega kodiranja videa na osnovi vizualih objektov lahko strnem v naslednje točke:

1. predstavitev obstoječih standardov s področja digitalnega kodiranja videa in njihovih omejitev glede vsebinskega dostopa do video podatkov,
2. opis modelov slike, ki omogočajo kodiranje slike kot vsote posameznih vizualnih objektov,
3. opis modelov gibanja objektov, s pomočjo katerih je možno slediti gibanju objekta skozi zaporedje slik ter na ta način ločiti objekt od ozadja,
4. definiranje načina predstavitve oblike objektov ter njenega spreminjanja s časom, ker je poudarek na aproksimaciji oblike s parametričnimi zlepljenimi krivuljami, ki omogočajo naravno predstavitev oblik z minimalnimi popačenji,
5. učinkovito kodiranje oblike in gibanja video objektov aproksimiranih z zlepljenimi krivuljami, ob iskanju optimalnega kompromisa med popačenji oblike ter potrebno bitno hitrostjo prenosa.

Naštete točke združimo v izdelavi sistema za hkratno segmentacijo gibajočih slik na posamezne objekte s pomočjo tehnik sledenja objektov ter kodiranja njihovega gibanja in oblike. Pri tem uporabimo model gibanja objektov, na osnovi katerega ocenimo vektorje gibanja objektov, z njihovo pomočjo pa potem projiciramo obliko objekta v naslednjo sliko zaporedja. Tehnike obdelave slik uporabimo za zaznavanje robov objektov, katere potem aproksimiramo s parametričnimi krivuljami s pomočjo tehnik numerične optimizacije. Končno zaporedje kontrolnih točk krivulje kodiramo z entropijskim kodiranjem. Opisan sistem predlaga rešitve za nekatere od opisanih problemov ter omogoča ponazoritev prednosti objektno orientiranega pristopa h kodiranju digitalnih video signalov.

Naslov naloge: **Pretvorniki valovne dolžine v optičnem transportnem omrežju**

Avtor: **Boštjan Batagelj, univ. dipl. inž. el.**

Mentor: **doc. Dr. Matjaž Vidmar, univ. dipl. inž. el.**

Univerza v Ljubljani, Fakulteta za elektrotehniko

Potreba po pretvornikih valovne dolžine je nastala v samem optičnem omrežju zaradi razširitvenih potreb, ki rastejo sorazmerno z naraščajočim telekomunikacijskim prometom. Pretvorniki valovne dolžine so naprave, ki imajo sposobnost pretvarjati oziroma spreminjati valovno dolžino (frekvenco) optičnega signala, ki vstopa vanje. Poznane so različne tehnike pretvorbe valovne dolžine, ki so osnovane na najrazličnejših fizikalnih prinicpih. Eden od namenov tega dela je ustvariti pregled sprememb in izboljšav pri tehnikah pretvorbe, ki so jih osnovne raziskave prinesle v zadnjih letih.

V uvodnem delu so opisani posamezni parametri pretvornikov valovne dolžine, ki jih ovrednotijo in omogočijo njihovo kasnejšo medsebojno primerjavo.

Delo je sestavljeno iz dveh delov. V prvem delu so opisane možnosti uporabe pretvornikov valovne dolžine v popolnoma optičnem omrežju. Za posamezno možnost uporabe so zbrane lastnosti, ki naj bi jih imel pretvornik valovne dolžine. Poleg pretvorbe so še posebej poudarjene naslednje lastnosti: transparentnost, regeneracija in kompenzacija disperzije.

V drugem delu so proučene različne fizikalne metode popolnoma optične in optoelektrične pretvorbe valovne dolžine. Razvrščene so glede na telekomunikacijske zahteve popolnoma optičnega omrežja v koherentne in nekoherentne tehnike pretvorbe. Analizirani so mehanizmi pretvorbe valovne dolžine, ki so primerni za uporabo v telekomunikacijskem optičnem omrežju. Podrobneje sta teoretično opisana pretvornika, ki delujeta na principu štirivalovnega mešanja in križne fazne modulacije v optičnem vlaknu. Prikazana je praktična realizacija obeh pretvornikov in podani so njeni rezultati. Analizirana je uporaba teh dveh pretvornikov v optičnem WDM transportnem omrežju.

V sklepu so zbrani razultati primerjalnih lastnosti in možnost uporabe pretvornikov v dveh preglednih tabelah, ki operaterju omrežja jasno prikažejo, kateri pretvornik valovne dolžine je primeren za želeno aplikacijo. Razvidno je, da je pri izbiri pretvornika valovne dolžine potrebno upoštevati tudi ostale uporabne lastnosti, ki spremljajo samo pretvorbo. S tem se funkcionalnost popolnoma optičnega omrežja še dodatno poveča.

Naslov naloge: **Določanje prozodičnih lastnosti z analizo besedil**

Avtor: **Janez STERGAR, univ. dipl. inž. el.**

Univerza v Mariboru, Fakulteta za elektrotehniko, računalništvo in informatiko

V magistrskem delu je predstavljen pristop določanja prozodičnih značilnosti v besedilih na simboličnem nivoju. Odločili smo se za podatkovno vodeni pristop pri resevanju problema s ciljem hitrega snovanja modelov in podpore večjezičnosti. Izdelali smo orodje za polavtomatsko napovedovanje oz. označevanje in klasifikacijo prozodičnih mej in pomozno orodje za označevanje jakostnih izrazitosti v povedi. Dopolnili smo besedilne zbirke z označitvijo besednih vrst celotne zbirke in označili besedilno zbirko s prozodičnimi mejami. V nadaljevanju smo poskusali napovedovati in klasificirati prozodične meje glede na besedilne zbirke, ki smo jih pripravili. Uporabili smo pristop učenja z nevronskimi mrezami, modul napovedovanja pa smo realizirali z večnivojskimi perceptroni.

Preskusili smo različne algoritme učenja in nekatere nadgradnje osnovne strukture večnivojskega perceptrona in realizirali strukturo za napovedovanje prozodičnih mej.

Naslov naloge: **Komprimiranje dvodimenzionalnih signalov po metodi drevesa ničel**

Avtor: **Dušan GLEICH, univ. dipl. inž. el.**

Univerza v Mariboru, Fakulteta za elektrotehniko, računalništvo in informatiko

V magistrskem delu so opisane transformacijsko izgubne metode za komprimiranje dvodimenzionalnih signalov. Za transformacijo metode uporabljajo diskretno transformacijo wavelet. Metode se med seboj razlikujejo po kvantizaciji. Poudarek je na metodah, ki temeljijo na t.i. algoritmu drevesa ničel. To so metoda dreves ničel, delitev niza pri hierarhičnih drevesih in prostorsko frekvenčna kvantizacija. Izgubne metode za komprimiranje dvodimenzionalnih signalov so testirane nad testnimi optičnimi slikami in SAR sliko.

Naslov naloge: **Primerjava signalizacij v ISDN vmesnikih**

Avtor: **Rado SLATINEK, univ. dipl. inž. el.**

Univerza v Mariboru, Fakulteta za elektrotehniko, računalništvo in informatiko

Magistrsko delo obravnava signalizacijske protokole tretje plasti vmesnika med uporabnikom in digitalnim omrežjem z integriranimi storitvami. V delu je prikazano funkcijsko obnašanje vmesnika z vsemi funkcijskimi grupami, ki krmilijo pretok signalizacijskih sporočil. Osnovnim funkcijam vmesnika med terminalsko opremo in končnikom centrale smo dodali funkcije zasebnega in dostopovnega omrežja. Signalizacije, ki se uporabljajo v tako razširjenem vmesniku, so podrobneje obdelane, prikazan pa je tudi način njihove izvedbe. Primerjava med signalizacijskimi protokoli v vmesniku ISDN temelji na studiju standardov ETSI ter na rešitvah, ki smo jih uporabili pri zasnovi in izdelavi programske opreme. Posebej sta bili obdelani signalizaciji DSS1 in QSIG ter protokoli vmesnika V5.2 s signalizacijo PSTN. Primerjava upošteva zahtevane in ponujene komunikacijske storitve za prenos signalizacijskih sporočil, stanja osebkov protokolov ter vsebino in zgradbo sporočil. V primerjavi je delno upostevan tudi protokol DECT, ki pa ni bil realiziran.

Naslov naloge: **Večkanalni sprejemnik za CDMA z uporabo digitalnega signalnega procesorja in vezij FPGA**

Avtor: **Filip Samo BALAN, univ. dipl. inž. el.**

Univerza v Mariboru, Fakulteta za elektrotehniko, računalništvo in informatiko

V magistrskem delu je predstavljena praktična izvedba komunikacijskega sistema z večkanalnim sprejemnikom s kodnim sodostopom. Sistem tako omogoča sočasno oddajanje in sprejemanje podatkov najrazličnejsih izvorov.

Posamezni oddajniki so narejeni s pomočjo RISC mikrokrmilnikov in omogočajo tvorjenje poljubnih psevdonaključnih zaporedij z nastavljivo hitrostjo. V sprejemnem delu vhodni signal najprej digitaliziramo s hitrimi A/D pretvorniki. Strojna oprema za tvorjenje lokalnih PN zaporedij, korelacija z vhodnim signalom ter komunikacija s procesorjem je opisana v jeziku VHDL ter izvedena v vezju FPGA. Vsa druga potrebna opravila naredi digitalni signalni procesor, rezultati pa se prenesejo na osebni računalnik. Podanih je tudi nekaj eksperimentalnih rezultatov.

Naslov naloge: **Problematika izobraževanja elektromagnetne skladnosti**

Avtor: **Marko VALANT, univ. dipl. inž. el.**

Univerza v Mariboru, Fakulteta za elektrotehniko, računalništvo in informatiko

Delo predstavlja prepoznavanje potreb po specifičnem znanju elektromagnetne skladnosti (EMC) , ki je v univerzitetnih študijskih programih delno zanemarjeno, je pa prepotrebno za slovensko industrijo. Namen dela je postavitev temeljev in strokovno podkrepljena umestitev tega znanja v predmetno področje elektrotehnike. Tako bodo študentje, kot bodoči načrtovalci elektronskih naprav in sistemov, osvojili veščine elektromagnetne skladnosti, ki so nujne pri nastajanju funkcionalnega izdelka, da bo le-ta izpolnjeval vse zahteve evropske smernice EEC/336/89.

Poudarek je na pripravi praktičnega urjenja, ki bo nadgradilo teoretično znanje. V uvodu opozorimo na temeljne težave, ki izhajajo iz elektromagnetne neskladnosti različnih elektronskih naprav in sistemov.

Drugo poglavje predstavlja področje EMC. Tretje poglavje zajema zahtevane meritve, ki jih narekuje evropska smernica glede EMC, četrto poglavje pa se ukvarja s študijo izobraževalnih konceptov v tujini. Peto poglavje predstavlja cilj našega dela. Osredotočimo se na zasnovo laboratorijskih eksperimentov pri samostojnem učnem predmetu Elektromagnetna skladnost.

Eksperimenti ponazarjajo osnovne principe EMC. Podan je tudi predlog opreme sodobnega laboratorija, ki bo poleg pedagoških namenov lahko rabil za izvajanje tovrstnih storitev.

DOKTORSKE DISERTACIJE

Naslov naloge: **Polprevodniške strukture za detekcijo sevanj**

Avtor: **Danilo Vrtačnik**

Mentor: **Prof. dr. Slavko Amon**

Univerza v Ljubljani, Fakulteta za elektrotehniko

V predloženem doktorskem delu smo raziskali osnovne lastnosti detektorja mehkih x-žarkov, izdelanega na visokoohmskem in zelo čistem silicijevem kristalu. Obravnavali smo interakcijo elektromagnetnega sevanja s silicijevo strukturo. Ugotovili smo, da se mehki x-žarki absorbirajo v siliciju primarno s fotoelektrično absorpcijo, pri čemer je z absorpcijo generirano število prostih nosilcev odvisno od energije vpadnega sevanja.

Osnovna celica predlaganega pasovnega detektorja, ki smo ga v delu imenovali kar strip detektor, je p-i-n (PIN) diodna struktura. Teoretična obravnava PIN strukture je vsebovala analizo senzorskega izgubnega toka, življenjske dobe nosilcev, energijsko ločljivost in šumne izvore. Ugotovili smo, da celotni izgubni tok v detektorju izvira iz termičnih generacij treh področij: površine, osiromašenega področja in neosiromašenega (navidezno nevtralnega) področja. V normalnem režimu delovanja, to je pri popolnem osiromašenju substrata, največji prispevek k celotnemu izgubnemu toku prispevajo termične generacije v osiromašenem področju.

Zmožnost detektorja, kako natančno meri energijo vpadnega sevanja, je izražena z njegovo energijsko ločljivostjo in je v detektorski strukturi določajo trije glavni izvori šuma: statistično odstopanje v številu generiranih nosilcev ter statistično odstopanje v izgubnem toku detektorja in elektronskega vezja, na katerega je priključen detektor.

Raziskali smo tudi vpliv vpadnega sevanja na generiranje poškodb v detektorski strukturi. Ugotovili smo, da mehki x-žarki povzročajo predvsem poškodbe v silicijevih oksidnih plasteh in na meji Si/SiO2. Te poškodbe imajo za posledico premike v pragovni napetosti MOS struktur (v našem primeru pomembno za FOXFET strukture) in v lokalnem povečanju električnega polja in s tem izgubnega toka na kritičnih mestih v PIN strukturi.

Začrtana in izdelana je bila nova struktura silicijevega strip detektorja za stransko osvetljevanje z x-žarki. Zaradi izboljšanja stabilnosti delovanja detektorja in zaradi izbranega delovanja detektorja v načinu posameznega štetja fotonov (single-counting mode), smo se odločili za izmenično (AC) priključitev detektorja na predojačevalno vezje.

Bremenski upor smo realizirali z izkoriščanjem upornosti tako imenovanega punch-through efekta, ki smo ga dodatno dogradili s tem, da smo na to strukturo dodali še kovinsko elektrodo vrat na osnovni oksid. Takšno strukturo, ki je poznana kot FOXFET struktura, smo proučevali tudi s pomočjo numeričnega 2D modeliranja. Na podlagi omenjenih modeliranj smo ugotovili, da vgrajeni naboj v oksidu in izgubni tok detektorja pomembno vplivata na delovanje FOXFET uporovne strukture.

Izboljšali smo strukturo ločilnega kondenzatorja s tem, da smo namesto ene same oksidne plasti uporabili sendvič-strukturo iz silicijevega oksida in nitrida. Pri tem smo ugotovili, da imajo pomembno vlogo pri preboju dielektrika debeline posameznih plasti kakor tudi njihovo razmerje in ugotovili vrednosti kritičnih parametrov.

Podrobno so bili raziskani nekateri kritični tehnološki koraki pri izdelavi detektorske strukture. Za izdelavo strip detektorja smo uporabili standardni planarni proces, prirejen za procesiranje na visokoohmskih in zelo čistih silicijevih rezinah. Ključno vlogo pri procesiranju detektorja je odigrala čistost procesa in postopki getranja.

Raziskali smo različne postopke mokrega čiščenja, pri čemer smo za osnovo izbrali standardno RCA čiščenje. Rezultati so pokazali, da ni univerzalnega čiščenja, ki bi bil enako učinkovit za vse faze čiščenja v postopku izdelave detektorja.

Ugotovili smo, da je najboljši proces getranja tisti, ki vsebuje hkratno getranje nečistoč z difuzijo fosforja in depozicijo polisilicija na zadnji strani rezine. Pri tem je pomembno, da je depozicija fosforja napravljena takoj po začetni oksidaciji, na zmerni temperaturi okrog 1000°C. Eksperimenti so tudi pokazali velik vpliv segregacijskega napuščanja na izgubni tok detektorja.

Električne meritve na izdelanih detektorjih so pokazale dobro, v nekaterih segmentih pa odlično ujemanje z napovedanimi teoretičnimi pričakovanji. Električne meritve so pokazale na upravičenost začrtanega varovalnega obroča detektorja, ker rezultati kažejo, da površinska komponenta izgubnega toka ni nezanemarljiva.

Predlagana nova, izvirna merilna metoda meritve izgubnega toka posameznega stripa, je opravičila uporabo predlaganega pristopa.

Poleg potrditve simulacijskih rezultatov z meritvami glede dinamične upornosti FOXFET bremenskega upora, zlasti glede njene odvisnosti od izgubnega toka in vgrajenega akumuliranega naboja v kanalu FOXFET-a, so rezultati meritev tudi pokazali, da je dinamična upornost funkcija geometrije FOXFET strukture.

Izmerjen detektorjev odziv na x-žarke je pokazal, da je detektor sposoben zaznavati energije višje od 12keV. Izmerjeni ekvivalentni šumni naboj detektorja priključenega na CASTOR elektroniko je znašal 690_e (elektronov).

Naslov naloge: **Mikroobdelava silicija za senzorske in aktuatorske strukture**

Avtor: **Drago Resnik**

Mentor: **prof. dr. Slavko Amon, univ. dipl. inž.**

Univerza v Ljubljani, Fakulteta za elektrotehniko

V predloženem doktorskem delu smo raziskali nekatere pomembne vitalne tehnologije mikroobdelave (micromachining) silicijevih ploščic orientacije <100>, ki se danes največ uporabljajo pri realizaciji silicijevih senzorskih in aktuatorskih mikrostruktur. Delo je sestavljeno iz štirih osnovnih sklopov, ki obravnavajo podrobno fizikalna ozadja jedkalnih procesov pri izdelavi mikrostruktur, eksperimentalne rezultate in njihovo analizo ter prinašajo ustrezne nove rešitve.

Prvi sklop sistematično obravnava moderne tehnologije, ki se danes uporabljajo pri mikroobdelavi silicija. Posebna pozornost je namenjena anizotropnemu mokremu jedkanju silicijevih struktur.

Drugi sklop predstavlja raziskave spodjedkavanja in kompenzacije konveksnih vogalov pri realizaciji mikrostruktur s pomočjo mokrega jedkanja.

V tretjem delu obravnavamo novejše področje tvorbe stranskih {311} silicijevih ravnin, ki omejujejo silicijeve strukture pri anizotropnem mokrem jedkanju in omogočajo realizacijo večnivojske mikroobdelave z minimalnim naborom fotomask.

V četrtem delu smo se ukvarjali z raziskavo tehnike nizkotemperaturnega bondiranja silicijevih ploščic, ene od osnovnih tehnologij pri realizaciji kompleksnih senzorskih elementov in mikrosistemov.

Razvoj senzorjev in aktuatorjev na siliciju je poleg tehnologij za izdelavo vezij za zajemanje in obdelave signalov neposredno pogojen tudi z razvojem mikroobdelave silicija. Mikroobdelava pomeni način preoblikovanja silicijevega substrata kot osnovnega materiala v primerne oblike in dimenzije z odvzemanjem (globinska mikroobdelava) ali dodajanjem materiala (površinska mikroobdelava). Pri mikroobdelavi silicija se poslužujemo orodij, ki so na voljo v mikroelektronski industriji, kot tudi novih ali izpopolnjenih tehnik, specifičnih za področje mikroobdelave. Vse te dodatne tehnike morajo biti združljive z mikroelektronskimi procesi, saj se izvajajo v istih okoljih in na kompatibilnih materialih.

Tri osnovne lastnosti, ki omogočajo mikroobdelavo silicija, so: i) anizotropno obnašanje različnih kristalnih ravnin, ii) selektivnost jedkanja silicija glede na maskirne materiale ter iii) samoustavitvene tehnike jedkanja.

Za mikroobdelavo je posebej primeren silicij orientacije <100>, predvsem zaradi primernih anizotropnih lastnosti, saj se ravnine (100) jedkajo znatno hitreje od ostalih, poleg tega pa se standardno uporablja tudi v mikroelektronskih tehnologijah za izdelavo integriranih vezij.

Pri anizotropnem jedkanju pravokotnih oblik silicijevih 3D struktur, paralelnih ali pravokotnih z [110] smerjo, so pri (100) siliciju stranske mejne {111} ravnine definirane s točno določenimi medsebojnimi koti (70,53°).

Pri strukturah kot je na primer prisekana piramida, ali takoimenovanih »mesa« strukturah, se izkaže, da bodo izpostavljeni konveksni vogali prisekani pod določenimi koti z dvema ali celo kombinacijo več ravnin višjih indeksov. Ker je ta pojav pri izdelavi tridimenzionalnih silicijevih struktur nezaželen, ga je potrebno eliminirati ali vsaj zmanjšati.

Raziskali smo vpliv spodjedkavanja konveksnih vogalov v različnih anizotropnih jedkalih: KOH, KOH-IPA, TMAH in TMAH-IPA. Na podlagi teh rezultatov smo določili, katere ravnine povzročajo hitrejše spodjedkavanje. Zakasnitev jedkanja na konveksnem vogalu dosežemo z uporabo mask s kompenzacijskimi liki, definiranimi na mestu konveksnega vogala. Pri zahtevani globini se mora vogalna superpozicija spodjedkati le do pravilnega presečišča {111} ravnin. Takrat je stopnja kompenzacije največja.

Analizirani so bili pristopi raznih avtorjev, ki so prišli do različnih rezultatov glede kristalnih ravnin na konveksnem vogalu, s tem pa tudi do različnih rešitev za realizacijo kompenzacijskih mask.

Uspešne kompenzacijske strukture vključujejo trikotnike, kvadrate, pasove v smeri <100> in asimetrične podaljške v smeri <110>. Cilj je ob najmanjši porabi lateralnega prostora priti do čimbolj popolne kompenzacije.

Na podlagi eksperimentalnega dela in analize rezultatov, smo načrtali več različnih kompenzacijskih struktur ter jih preizkusili v štirih različnih jedkalnih sistemih. Na podlagi teh rezultatov smo določili osnovne zakonitosti spodjedkavanja in izvedli relacije za dimenzioniranje kompenzacijskih struktur s superponiranim kvadratom in superponiranim trikotnikom na mestu konveksnega vogala. Pri tem smo si pomagali z analizami optične in elektronske vrstične mikroskopije (SEM).

Z namenom razširiti možnost uporabe mikroobdelave tudi na druge ravnine, ki sekajo površino (100) pod drugimi koti, smo raziskali možnosti, ki jih nudi anizotropno jedkanje v različnih jedkalih. Zanimiv nov fenomen, ki je bil odkrit pri našem delu, je dejstvo, da je možno iz obstoječih struktur z {111} mejnimi ravninami realizirati tudi ravnine {311} in sicer

tako, da se po maskirnem jedkanju v prvi fazi odstrani masko z (100) ravnine na definiranem področju. To imenujemo v delu anizotropno brezmaskirno jedkanje, saj na tem področju poteka sedaj jedkanje brez maske. Podrobneje je bil ta fenomen raziskan za KOH, medtem ko za TMAH jedkalo rezultati omenjenega pristopa še niso bili analizirani v literaturi. Raziskave so potekale primerjalno v omenjenih jedkalih.

Prednost našega pristopa je v tem, da že na začetku ustvarimo na površini silicijeve ploščice dve maskirni plasti. Najprej zraste na površini silicija termični silicijev oksid SiO_2 nakar deponiramo z LPCVD metodo nanašanja še plast silicijevega nitrida Si3N4. Zatem z dvema zaporednima fotolitografskima postopkoma definiramo dve področji jedkanja. V prvi fazi jedkamo anizotropno preko oksidne maske, ki jo nato pred začetkom drugega jedkanja odstranimo. Predhodno ustvarjene {111} ravnine se zvezno pretvorijo po določenem času v {311} ravnine. Ugotovljeno je bilo, da se anizotropija močno zmanjša, kar moramo upoštevati že pri načrtovanju mikrostruktur.

Predstavljena je analiza karakteristik takega načina jedkanja, vključujoč morfološke lastnosti novih ravnin kot posledice temperaturne odvisnosti jedkalnega procesa. Posebna pozornost je bila usmerjena tudi na obnašanje konveksnih in konkavnih vogalov pri spremenjenih pogojih anizotropije, saj se v primeru mikrostruktur, omejenih s {311} ravninami, zaradi spremenjene anizotropije močno spremenijo razmere tudi na vogalu. Na podlagi opravljenega eksperimentalnega dela smo pokazali, da lahko z izbiro globine mikrostrukture v maskiranem jedkanju ter naknadnega brezmaskiranega jedkanja dosežemo samokompenzacijo struktur. Obenem z izboljšanjem razmer na konveksnih vogalih smo ugotovili v brezmaskiranem načinu popačenje konkavnih vogalov, kar v maskiranem načinu jedkanja ni bilo opaziti. Ugotovljena je bila večja zaobljenost konkavnih vogalov v brezmaskiranem načinu jedkanja, ki je bolj poudarjena v KOH jedkalu v primerjavi s TMAH jedkalom.

Zaradi potencialne uporabe {311} ravnin kot optičnih odbojnih površin, smo raziskali vpliv različnih jedkal, temperature kopeli, koncentracije raztopine jedkala in mešanja jedkal na hrapavost dobljenih {311} ravnin. Znižanje hrapavosti smo dosegli z izbiro jedkala in optimiranjem jedkalnih parametrov. Predlagana in izvedena je bila tudi možnost realizacije mikrostruktur s kombinacijo dveh mejnih ravnin, v našem primeru {111} in {311} ravnin.

Bondiranje je važen postopek pri izdelavi silicijevih senzorskih in aktuatorskih struktur, saj nam omogoča spajanje komplementarnih delov delno izdelanih mikrostruktur, ki tako dobijo funkcionalno vrednost in jih ni možno realizirati s tehnološkimi prijemi na eni sami silicijevi ploščici. Omogoča tudi pritrditev občutljive, aktivne senzorske ali aktuatorske mikrostrukture na pasivno podlago, ki daje mehansko trdnost, potrebno za nadaljnjo montažo v ohišje.

Pri direktnem nizkotemperaturnem bondiranju dveh silicijevih rezin s hidrofilno zaključeno površino je privlačnost pri sobni temperaturi posledica Van der Waalsovih sil, s temperaturnim napuščanjem pa jih nadomestijo kovalentne vezi.

Raziskava bondiranja je bila izvedena z namenom razumevanja fenomenov, ki se pojavljajo ob pripravi površin in med bondiranjem samim, kot tudi praktičnim aplikacijam. Predstavljene so osnovne lastnosti hidrofilnih in hidrofobnih površin silicija in silicijevega oksida ter kemijsko-fizikalni načini povezav med površinama ob medsebojnem stiku.

Raziskani so bili osnovni parametri, ki vplivajo na kvaliteto bonda. To so predvsem priprava silicijeve površine, začetna topografija površine, ambient pri bondiranju ter vpliv orientacije silicijevih ploščic na porušitveno trdnost bonda.

Delo je osredotočeno predvsem na bondiranje silicijevih ploščic orientacij <111> in <100> v temperaturnem obsegu 80-400°C v treh različnih ambientih, prisotnih pri termičnem napuščanju: v kisiku, dušiku in nizkem vakuumu. Cilj tega dela je bil poiskati primerjavo med bondirnimi energijami, doseženimi pri teh danih pogojih, najti optimum in možne fizikalne razlage k doseženim eksperimentalnim rezultatom.

Zaradi tvorbe praznin na stiku pride do nepopolnega spajanja površin. Podani so vzroki za nastanek le-teh kot tudi rešitve, ki doprinesejo k zmanjšanju števila in velikosti praznin, ter v končni fazi do njihove eliminacije.

Prikazane so metode za ovrednotenje bonda ter obdelane deformacije v siliciju kot posledica prilagajanja realnih površin, ki so posledica hrapavosti posameznih spojnih površin.

Karakterizacija kvalitete bonda je bila izvedena s trgalnimi testi, ki podajajo porušitveno trdnost bonda. V rezultatih so podane odvisnosti natezne trdnosti bonda od valovitosti in hrapavosti površin in vpliv kemijskega čiščenja površine silicija na topografijo, nadalje odvisnost natezne trdnosti od ambienta, prisotnega pri termičnem napuščanju, od temperature napuščanja bondirnih vzorcev, od orientacije silicija ter zaključitve površine posamezne stične površine. Kvalitativna karakterizacija bonda je bila izvedena tudi s termovizijsko kamero.

Predstavljeni so obstoječi fizikalni modeli in dopolnitev teh modelov na osnovi ugotovitev našega eksperimentalnega dela. Opravljeno raziskovalno delo podpira vrsto predstavljenih modelov ter prinaša nekatere nove bistvene ugotovitve v fizikalnih dogajanjih pri bondiranju hidrofilnih silicijevih površin, ki sloni predvsem na vplivu orientacije kristala, priprave površin in ambientu napuščanja.

Naslov naloge: **Optimizacije vezij v programskem okolju *SPICE***

Avtor: **Janez Puhan**

Mentor: **prof. Franc Bratkovič, univ. dipl. inž.**

Univerza v Ljubljani, Fakulteta za elektrotehniko

Optimizacija elektronskih vezij je zelo obširen pojem, ki zajema različne vrste optimizacijskih postopkov. V ožjem pomenu besede pomeni načrtno spreminjanje poljubnih parametrov danega vezja z namenom iskanja odziva in lastnosti vezja, ki bi bile čimbolj podobne želenim. Načrtovalec pri tem uporablja inženirsko znanje iz analize in sinteze vezij, ter svoje dragocene izkušnje. Že znane rešitve poskuša prikrojiti potrebam načrtovanega vezja. Optimizacijsko orodje mu je lahko v veliko pomoč. Razkriva mu nove poglede na določeno vezje in odpira nove rešitve, ki niso omejene z načrtovalskimi kalupi, ali pa potrjuje optimalno zgradbo nekega vezja.

Da lahko optimizacijski postopek opravi svoje delo, potrebuje temelj, na katerem lahko gradi. To je primeren analizator elektronskih vezij, ki se je že dokazal s svojo numerično stabilnostjo in točnostjo rezultatov, ter je hkrati primeren za nadgradnjo. Takšen temelj predstavlja programsko okolje *SPICE*. Programsko okolje *SPICE* je zadnjih nekaj let nedvoumno industrijski standard na področju računalniške analize integriranih in diskretnih analognih, ter deloma tudi digitalnih elektronskih vezij. Na njem je, zaradi javnosti originalne Berkeleyeve izvorne kode, mogoča poljubna vrsta nadgradnje.

Med študijem teorije optimizacijskih metod so bili izoblikovani praktični numerični postopki konkretne implementacije le teh v programskem okolju *SPICE*. Tako je v delu podrobneje opisanih enajst implementiranih optimizacijskih metod s stališča praktične izvedbe. Pri tem so pri nekaterih metodah podani tudi izkustveni popravki algoritmov znanih iz teorije, ki se izkažejo pri delu z realnimi primeri.

V okviru nadgradnje programskega okolja *SPICE* s splošno optimizacijsko zanko je bil potreben tudi poglobljen študij originalne Berkeleyeve izvorne kode. Tako je podrobneje opisana tudi sama implementacija optimizacijske zanke, ter stične točke (podatkovne strukture in posamezne funkcije) med osnovno kodo in kodo optimizacijske zanke. Kot rezultat teh prizadevanj je nastalo povsem splošno računalniško optimizacijsko orodje z enajstimi vgrajenimi optimizacijskimi metodami. Le to omogoča optimizacijo poljubnega vezja, s poljubno definirano kriterijsko funkcijo. Prav tako lahko uporabnik kot parametre optimizacije izbere poljubne spremenljive parametre vezja, ter jih eksplicitno ali implicitno omeji.

Uspeh posamezne optimizacijske metode je v veliki meri odvisen od primernosti začetnega poskusa. V več optimizacijskih tekih nad isto kriterijsko funkcijo je zato smiselno preiskovanje vedno drugega dela parametrskega prostora. Tako naj se začetni poskus novega optimizacijskega teka nahaja vedno tam, kjer do tedaj parametrski prostor še ni bil preiskan. Z vsakim naslednjim optimizacijskim tekom je na ta način pridobljenih več informacij o kriterijski funkciji, ki je glavna neznanka vsakega optimizacijskega postopka. Tako je klasičen optimizacijski postopek preoblikovan v več optimizacijskih tekov, ki so med seboj povezani z vsakokratno ustrezno izbiro začetnega poskusa.

V delu je raziskan problem določevanja novega začetnega poskusa posameznega optimizacijskega teka. V enodimenzionalnem prostoru je pokazana relacija med verjetnostjo nizke vrednosti kriterijske funkcije v neki točki, ter gostoto že določenih točk in vrednostjo kriterijske funkcije v njih. Ob predpostavki, da je kriterijska funkcija v okolici že določenih točk realizacija limitiranega naključnega korakanja, je izpeljana povezava, ki podaja najboljšo izbiro novega začetnega poskusa v odvisnosti od oddaljenosti od že znane točke in vrednostjo kriterijske funkcije o njej. Odvisnost velja bližini vsake izmed že znanih točk. Sklepa, ki ju navaja izpeljana odvisnost, sta posplošena na večdimenzionalen prostor. Verjetnost nizke vrednosti kriterijske funkcije je tem večja, čim večja je oddaljenost od že znanih točk, ter je večja v bližini točk z nižjo vrednostjo kriterijske funkcije. Na njuni podlagi je dalje razvit hevrističen postopek za določevanje novega začetnega poskusa naslednjega optimizacijskega teka. Pri tem so upoštevane vse informacije o poteku kriterijske funkcije pridobljene s predhodnimi optimizacijskimi teki. Razvit postopek v povezavi z več optimizacijskimi teki najde več lokalnih minimumov, če jih kriterijska funkcija ima.

Vse implementirane metode, in tudi samo optimizacijsko orodje, so bile preizkušene na primerih, tako na matematičnih, kot na povsem realnih vezjih. Do tega trenutka, zaradi neobstoja splošnega optimizacijskega orodja, v literaturi ni zaslediti praktičnih primerov optimizacije elektronskih vezij, ki niso rešljivi analitično, ali so več kot le nekaj dimenzionalni. V primerih, navedenih v tem delu, so v realnem svetu med seboj primerjane različne optimizacijske metode. Uspešnost posamezne metode se ne meri le v številu potrebnih iteracij za rešitev, oziroma v hitrosti konvergence, ampak tudi v robustnosti posameznega postopka. Tako se izkaže, da kriterijske funkcije v realnih primerih niso več lepe zvezne. V najboljšem primeru so posejane z rahlim numeričnim šumom, ki je posledica postopkov računalniške analize vezja, ter izračunavanja kriterijske funkcije. V takšnih okoliščinah se je izkazalo, da hitri gradientni postopki navadno odpovedo, medtem ko direktni postopki dajejo boljše rezultate. Na primerih se je tudi pokazalo, da ima najboljše latnosti med implementiranimi postopki metoda omejenih simpleksov.

Naslov naloge: **Optimizacija konfiguracij dinamično programirljivih vezij**

Avtor: **Hubert Fröhlich**

Mentor: **prof. dr. Baldomir Zajc, univ. dipl. el.**

Univerza v Ljubljani, Fakulteta za elektrotehniko

Tehnologija vezij FPGA je zelo uspešno prodrla na vsa področja načrtovanja digitalnih sistemov. Vse odkar se je pojavil nov pristop pri načrtovanju z vezji FPGA, ki ga imenujemo dinamično reprogramiranje, se vedno več raziskovalcev in inženirjev ukvarja z načrtovanjem sistemov z dinamično reprogramirljivimi vezji.

Medtem ko so prednosti dinamičnega reprogramiranja, še posebno ob uporabi delne reprogramirljivosti, že znane, pa smo še precej daleč od tega, da bi načrtovanje dinamočno reprogramirljivih sistemov postalo rutina. Tu sta pomanjkljivi predvsem metodologija načrtovanja in programska podpora. Vsi objavljeni rezultati s tega področja opisujejo delo ročnega načrtovanja konfiguracij. To je zelo zapleteno, še posebno če uporabljamo delno reprogramirljivost.

Dinamična reprogramirljivost ima veliko prednost pri realizaciji vezij. Najpomembnejše so fleksibilnost na nivoju arhitekture, cenejša izvedba sistema in v določenih primerih hitrejše delovanje. Vendar vse te predanosti niso brez cene. Cena, ki jo plačamo, je čas rekonfiguriranja programirljivih vezij, ki lahko, če je predolg, naredi cel sistem neuporaben. Zato je eden od velikih problemov pri načrtovanju dinamično reprogramirljivih sistemov prav rekonfiguracijski čas.

Čas rekonfiguracije lahko skrajšamo na nivoju vezij FPGA (hitrejša vezja, boljša arhitektura) ali pa na nivoju načrtovanega vezja (rekonfiguriramo čim manjši del vezja). Pri drugem načinu moramo izrabiti delno programirljivost vezij.

Namen te disertacije je razviti metodo za minimizacijo rekonfiguracijskega časa na nivoju vezja. To pomeni avtomatsko odkrivanje čim večjih skupin delov vezij, kar lahko načrtovalec s pridom uporabi pri snovanju sistema, saj je ta postopek naporen, dolgotrajen in zelo podvržen napakam. Z avtomatizacijo bi ga skrajšali in močno razbremenili načrtovalca.

Če želimo razviti metodo za iskanje največjih skupnih delov vezij, moramo ta vezja predstaviti v obliki, ki bo primerna za obdelavo z računalnikom. Najbolj naravna predstavitev vezij je z usmerjenimi grafi. Tudi mi smo uporabili to predstavitev. Problem predstavitve digitalnih vezij z usmerjenimi grafi pa je ta, da lahko vezje predstavimo samo na nivoju logičnih vrat, kar pa ni dobro, če vemo, da bodo taka vezja realizirana v vezjih FPGA. Če iščemo skupne dele vezij, bi pri predstavitvi na nivoju logičnih vrat lahko prišlo do rešitev, ki jih ne moremo realizirati, saj bi skupni del vezja lahko vseboval del nekega vezja, ki je v vezju FPGA nedeljiva celota. Take rešitve torej ni mogoče realizirati. Primer takega nedeljivega bloka je statična pomnilniška celica (D-flip flop), ki ga v grafu predstavimo na nivoju logičnih vrat.

Da bi rešili problem predstavitve vezij z usmerjenimi grafi za vezja FPGA, smo uvedli nov tip vozlišč, ki jih imenujemo virtualna vozlišča, saj v resnici ne predstavljajo dejanskega vezja pač pa samo vhode, funkcijo in izhode določenega podvezja, ki pri realizaciji z vezjem FPGA ni deljivo. Izkazalo se je, da taka predstavitev vezja prinaša še eno prednost. Ta je, da lahko v predstavitev vezja z grafom vnesemo hierarhijo. Tako lahko podvezja, za katera vemo, da so si v obeh vezjih enaka (na primer seštevalniki, množilniki), predstavimo kot nedeljive celote in jih optimiziramo. S tem zmanjšamo število vozlišč grafa in tako pohitrimo optimizacijo.

Iskanje največjih skupnih delov vezij pomeni iskanje največjega skupnega podgrafa. To pa je problem, ki je NP-poln, kar pomeni, da zanj ni znan algoritem, ki bi rešitev dal v polinomskem času. Zato moramo iskati rešitve na drugačen način, z nedeterminističnimi metodami, ki so se že do sedaj zelo obnesle pri reševanju problemov, katerih računska zahtevnost je eksponentna ali celo super eksponentna. Za reševanje problema iskanja največjega skupnega podgrafa smo uporabili genetski algoritem.

Genetski algoritem je samo predpis, kako iskati rešitev. Pri uporabi genetskega algoritma je naloga uporabnika, da razvije ustrezno kodiranje rešitev, zasnuje genetske operatorje in kriterijsko funkcijo. Največji problem pri tem predstavljata kodiranje in križanje, saj morata izpolnjevati posebne pogoje, da bo genetski algoritem dobro deloval.

Uvedli smo kodiranje, ki vsako rešitev zapiše z nizom, ki je dolg toliko, kot ima vozlišč manjši od grafov, ki ju preiskujemo. S tem smo močno zmanjšali zahteve po velikosti pomnilnika, saj bi bila predstavitev z matrikami precej bolj požrešna. Tudi operator križanja in kriterijsko funkcijo smo zasnovali tako, da je časovna zahtevnost algoritmov s katerimi so realizirani, polinomska.

Pri testiranju s testnimi grafi se je pokazalo, da dobimo 80 - 85% skupnega podgrafa zelo hitro, za boljše rešitve pa je potrebno daljše izvajanje algoritma. Rezultati so močno odvisni tudi od velikosti populacije, kar pripisujemo kombinatorični naravi problema in dejstvu, da je optimizacijski prostor ogromen.

Vsi rezultati so bili dobljen na računalniku PC s procesorjem Pentium III - 450 MHz, 128 MB RAM, Windows 95. Program je bil napisan v programskem jeziku *C + +*.

V uvodu najprej opišemo trenutno stanje področja in predstavimo dinamično reprogramirljivost, ter njene prednosti. V drugem poglavju nato podamo teoretično ozadje, potrebno za opis rešitve problema iskanja največjih skupnih podgrafov. V tretjem poglavju opišemo metodo za iskanje največjih skupnih podgrafov in uporabo genetskega algoritma v ta namen. V tem poglavju podamo tudi rezultate, ki prikazujejo odvisnost delovanja genetskega algoritma od ključnih parametrov. V četrtem poglavju pokažemo, kako je mogoče metodo iskanja najkrajšega časa rekonfiguracije prevesti na metodo iskanja skupnega podgrafa, v petem poglavju pa opišemo programsko orodje razvito za iskanje največjega skupnega podgrafa in podamo rezultate.

Naslov naloge: **Grafi AND/OR za računalniško načrtovanje in testiranje integriranih vezij**

Avtor: **Alenka Žužek**

Mentor: **prof. dr. Baldomir Zajc**

Univerza v Ljubljani, Fakulteta za elektrotehniko

Načrtovanje digitalnih vezij je področje, ki se zelo hitro razvija in spreminja. V zadnjih dvajsetih letih se je število tranzistorjev na čip povzpelo iz tisoč na več deset milijonov. To postavlja stalno nove zahteve za orodja računalniškega načrtovanja (CAD) integriranih vezij (IC) v tehnologiji izdelave integriranih vezij VLSI.

Reševanje problemov načrtovanja v tehniki VLSI zahteva ustrezno podatkovno strukturo. V zadnjih letih so se, tudi v industrijskih aplikacijah, uveljavile metode, ki rešujejo probleme računalniškega načrtovanja in testiranja integriranih vezij z binarnimi odločitvenimi grafi (BDD). Med temi so bile najuspešnejše strukture urejenih binarnih odločitvenih grafov (OBDD). Za metode z odločitvenimi grafi načeloma velja, da probleme rešujejo učinkovito in enostavno, če je le možno zgraditi odločitveni graf. Enostavnost reševanja je posledica kanonične predstavitve logičnih funkcij z odločitvenimi grafi.

Probleme verifikacije, logične sinteze in testiranja lahko preslikamo na problem Boolove izpolnljivosti. Ker je ta problem s pristopom odločitvenih grafov učinkovito rešljiv in ker se Boolove operacije s temi grafi izvajajo preprosto, so te metode vgrajene v številne algoritme za računalniško načrtovanje integriranih vezij. Pristop z odločitvenimi grafi pa ima dve poglavitni slabosti, in sicer občutljivost na vrstni red spremenljivk ter velika kompleksnost predstavitve določenih pomembnih funkcij, kot so na primer množilniki. Zato je potrebno iskati nove poti za reševanje problemov v CAD VLSI.

V zadnjem času se kot alternativni pristop za reševanje logične sinteze, verifikacije in testiranja z odločitvenimi grafi vse bolj uveljavlja strukturni pristop z grafi AND/OR. Grafi AND/OR ne predstavljajo Boolove funkcije kanonično, temveč hranijo strukturo vezja (implementacijo) z Boolovim sklepanjem. Ti grafi so se do sedaj pretežno uporabljali na področju umetne inteligence, sedaj pa lahko uspešno rešujemo tudi mnoge probleme računalniškega načrtovanja in testiranja vezij.

V pričujočem delu bomo podali natančno primerjavo metod z grafi AND/OR in odločitvenimi grafi. Primerjava BDD-jev in grafov AND/OR v načinu preiskovanja kaže na naslednjo pomembno razliko: odločitveni grafi temeljijo samo na preiskovanju OR, medtem ko nova podatkovna struktura uporablja preiskovanje AND/OR. Problem Boolove izpolnljivosti lahko prav tako predstavimo z grafi AND/OR. Za razliko od BDD-jev grafi AND/OR ne predstavljajo funkcije kanonično, vsebujejo pa informacijo o strukturi vezja, kar je za mnoge aplikacije lahko zelo dobrodošlo.

Razvili smo dve novi statični metodi za določanje urejenosti binarnih odločitvenih grafov. Na podlagi analize grafa AND/OR določita vrstni red spremenljivk, s katerim dosežemo oz. celo presežemo rezultate, dobljene z dinamičnimi metodami.

V doktorskem delu smo raziskovali tudi druge zmožnosti grafov AND/OR za reševanje problemov na področju CAD IC. Spektralni pristop je uporaben za mnoge probleme pri reševanju sinteze, verifikacije in generiranje testih vzorcev. Z grafi AND/OR lahko predstavimo funkcije v CAD, iz grafov AND/OR izluščimo izhodno verjetnost, s katero lahko izračunamo spektralno informacijo. Prednost tega načina je, da se lahko hranijo tudi nepopolne funkcije.

V doktorskem delu obravnavamo še tretjo in najdalj uveljavljeno uporabnost grafov AND/OR na področju CAD IC. Znani algoritmi s področja umetne inteligence za delo z graf AND/OR se zadnje desetletje uspešno uporabljajo za optimizacijo sekvenčnega diagnosticiranja. V okviru doktorskega dela smo problem posplošili na večizidne in asimetrične teste. Pristop pa smo uporabili za model funkcionalnega diagnosticiranja sinhronih sekvenčnih vezij. Za celovito predstavitev uporabe grafov AND/OR na področju CAD VLSI IC pa v pričujočem delu opisujemo tudi reševanje optimizacije vezij na fizičnem nivoju.

Pričujoče doktorsko delo je raziskava področja računalniškega načrtovanja in testiranja integriranih vezij z grafi AND/OR. S poznavanjem obstoječih metod in razvojem lastnih smo postavili temelje za implementacijo celovite rešitve za delo z grafi AND/OR za potrebe reševanja različnih problemov na tem področju.

Naslov naloge: **Študij procesov na fazni meji kovina/polprevodnik in raziskave vpliva na električne karakteristike Schottkyjevih struktur v sistemu AgAu/Si(111)**

Avtor: **Janez KOVAČ**

Univerza v Mariboru, Fakulteta za elektrotehniko, računalništvo in informatiko

Delo, opisano v tej disertaciji, je nastalo z namenom, da bi prispeval k razumevanju mikroskopskih vplivov morfologije na nastanek fazne meje kovina/polprevodnik in na elektronske lastnosti na meji. V ta namen sem na modelu fazne meje preiskal interakcije med naparjenimi kovinskimi plastmi Au in Ag ter različnimi morfološkimi fazami na faznih mejah Ag/Si(111) in Au/Si(111), ki nastanejo pri povišanih temperaturah. Iz fotoelektronskih spektrov Si 2p, Ag 3d in Au 4f, dobljenih z novim fotoelektronskim mikroskopom na sinhrotonu Elettra, sem sklepal na sestavo, kemijsko stanje in masni transport ter iz premika spektra Si 2p in valenčnega pasu na elektronske lastnosti različnih faz. Njihovo strukturo sem določil z uklonom nizkoenergijskih elektronov. Ugotovil sem, da na faznih mejah Ag/Si(111) in Au/Si(111) pri temperaturi nad 400 in 600°C nastanejo 2D-faza in 3-D faze, ki vsebujejo kovino in so prekrite z zreagirano plas-

tjo kovina-Si. Pri interakciji naparjenih plasti Au in Ag z različnimi morfološkimi fazami na faznih mejah Ag/Si(111) in Au/Si(111) sem ugotovil, da so pomembni procesi: vgradnja atomov Au v urejeno 2D-fazo Ag/Si, zamenjava atomov Ag vezanih z Si v zreagirani plasti Ag-Si z atomi Au, masni transport med 2D- in 3D-fazami in mešanje atomov ali tvorba kovinske zlitine v 3D-fazah. Potek teh procesov je odvisen od strukture in sestave posamezne faze, jakosti kemijske vezi med Au, Ag in Si, prisotnosti nezreagirane kovine in prostorske omejenosti kovinskih plasti. Elektronske lastnosti valenčnega pasu 2D-faze Ag/Si imajo polprevodniški značaj, medtem ko imajo 2D faza Au/Si in 3D faze kovinskega. Na fazni meji AgAu/Si(111) se elektronske lastnosti spreminjajo skladno s sestavo in strukturo posameznih faz. Na 2D-fazah Au/Si in Ag/Si sem določil višino Schottkyjeve pregrade. Med eksperimentalnim delom sem sodeloval tudi pri postavitvi vrstičnega fotoelektronskega mikroskopa na sinhotronskem pospeševalniku Elettra, ki ga tudi opišem v tej disertaciji. Mikroskop fokusira s krožnim Fresnelovim uklonskim elementom svetlobo z energijo 200-1000 eV. Njegova lateralna in energijska ločljivost sta 150 nm in 0,3 eV in deluje pri tlaku okoli $5x10^{-10}$ mbar. Obravnaval sem stranske pojave, ki sem jih srečal pri svojem delu in so povezani z veliko gostoto svetlobnega toka v gorišču mikroskopa kot so: lokalno segrevanje in električno nabijanje površine, fotoinducirana redukcija oksidov in kontaminacija površine z ogljikom. Predstavljen je postopek korekcije dobljenih slik v mikroskopu zaradi vpliva topografije na neravni površini. V delu je podano tudi fizikalno ozadje sinhotronskega sevanja, ki kaže na njegove lastnosti, ki smo jih uporabili pri postavitvi fotoelektronskega mikroskopa.

Naslov naloge: **Izboljšanje elektromagnetne združljivosti naključno moduliranega usmernika s korekcijo faktorja moči**

Avtor: **Franc MIHALIČ**

Univerza v Mariboru, Fakulteta za elektrotehniko, računalništvo in informatiko

Z uporabo vezij za korekcijo faktorja moči (pretvornik navzgor) lahko v enofaznih usmernikih dosežemo faktor moči blizu 1. Po dugi strani pa zaradi visoke stikalne frekvence pretvornika navzgor nastajajo elektromegnetne motnje (electromagnetic inference - EMI) tudi v radijskem frekvenčnem področju. V tej disertaciji je opravljena široka frekvenčna analiza usmernika s korekcijo faktorja moči krmiljenega z običajno (deterministično) in naključno pulzno širinsko modulacijo (PSM). Meritve v nizkofrekvenčnem področju so pokazale, da je vpeljava naključne PSM prispevala k povečanju skupnega harmonskega popačenja (total harmonic distorion -THD) za manj kot 1%, medtem ko se faktor moči usmernika ni bistveno poslabšal (ostal je večji od 0.9981). Z uporabo teorije o naključnih procesih je bila izvedena estimacija spektra močnostne gostote (power spectral desnsity -PSD) vhodnega toka usmernika, da bi ugotovili vpliv naključne modulacije pri višjih frekvencah. Izveden je bil tudi optimizacijski postopek parametrov v Matlabu za Welch-evo metodo estimacije (ocentive) PSD. Verifikacija ocenjenih rezultatov z meritvami je potrdila v začetku postavljeno tezo o izboljšanju elektromagnetne združljivosti usmernika z uporabo naključne PSM. Končno potrditev teze je prineslo merjenje prevodnih motenj z industrijskim merilnim instrumentom. ki je potrdil skladnost usmernika s predpisanimi standardi in obenem ovrednotil prednost nakljune PSM pred običajno PSM. ta naloga ponuja enostavno in učinkovito (tudi cenovno) metodo ugotavljanja prevodnih elektromagnetnih motenj.

Naslov naloge: **Izmenični motorji kot servopogoni v mehatroniki**

Avtor: **Miran RODIČ**

Univerza v Mariboru, Fakulteta za elektrotehniko, računalništvo in informatiko

V delu je opisan nov pristop vodenja asinhronskega motorja po navoru in rotorskem fluksu brez uporabe senzorja hitrosti. Glavni prospevek dela je uporaba nove strukture observerja rotorskega fluksa, namenjenega delovanju brez senzorja hitrosti. Predlagani pristop se ukvarja s problemom servopogona z asinhronskim motorjem brez senzorja hitrosti, ki naj deluje pri nizkih in visokih hitrostih vrtenja z možnostjo hitrih sprememb hitrosti. Zamisel je realizirana z uporabo nelinearnega, od statorske frekvence odvisnega ojačanja, ki rotorskemu observerju omogoča delovanje pri visokih in nizkih hitrostih. Pri nizkih hitrostih preide observer v zaprtoznačni nelinearni sistem, ki za vhode uporablja statorski tok in napetost ter želeno vrednost rotorskega fluksa, pri visokih hitrostih pa v dobro znan napetostni model asinhronskega motorja s povratoznačno vezavo, ki izboljša lastnost observerja. Predstavljen je tudi algoritem za adaptacijo vrednosti statorske upornosti. Na ta način je observer nekoliko robustnejši na spreminjanje parametrov. Delovanje je proučeno in potrjeno s simulacijami in eksperimenti.

Pregled del sta pripravila R. Babič in I. Šorli