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A Power-On Reset Circuit for an Integrated Inductive Encoder

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Abstract. A power-on reset circuit (POR) with two threshold voltages $V_{TH,LOW}$ and $V_{TH,HIGH}$ separated with a hysteresis is designed. The circuit has an additional brown-out reset (BOR) functionality designed to detect outbursts with a minimum surface area of $100\,nVs$ and an ability to produce a startup prolonged reset pulse for the voltage rise times from $10^{-12}s$ to $10^{-8}s$. The circuit has a $34.66\,\mu A$ quiescent current and reaches a maximum current spike of $191.35\,\mu A$. Although the circuit is designed to operate at a power-supply rise and fall times in the ranges from $10\,\mu s$ to $20\,\mu s$, additional transient analyses are performed to define its response in the range of 12 decades (from $1\,ps$ to $1\,s$). Moreover, both the corner and Monte Carlo analysis at a $16\,\mu s$ supply rise time are performed. The area of the circuit implementation for the XFAB $350\,nm$ process is $300.450\,\mu m$ x $95.475\,\mu m$.

Keywords: application-specific integrated circuit, power-on reset, brown-out reset, integrated inductive encoder

Vezje za nastavitev ob vklopu napajanja (POR) za integrirani induktivni enkoder

Predstavljen je razvoj vezja za nastavitev ob vklopu napajanja POR (ang. power-on reset) z dvema pragovnima napetostima $V_{TH,LOW}$ in $V_{TH,HIGH}$, ločenima s histerezo. Vezju je dodana funkcionalnost ponastavitve ob napaki napajanja BOR (ang. brown-out reset) zasnovana za zaznavanje napajalnih izpadov z minimalno površino $100\,nVs$ in z zmožnostjo vzpostavitve zagonskega ponastavitvenega pulza za čase vzpona napajalne napetosti od $10^{-12}s$ do $10^{-8}s$. Vezje dosega delovni tok $34.66\,\mu A$ in maksimalni tok $191.35\,\mu A$. Kljub temu, da je vezje zasnovano za čase vzpona in padca napajalne napetosti od $10\,\mu s$ do $20\,\mu s$, so izvedene dodatne tranzientne analize za določitev odziva v območju 12 dekad (od $1\,ps$ do $1\,s$). Poleg tega so izvedene tudi analize corner in Monte Carlo pri času dviga napetosti napajanja $16\,\mu s$. Površina implementacije vezja za proces XFAB $350\,nm$ znaša $300.450\,\mu m$ x $95.475\,\mu m$.

1 INTRODUCTION

Analogue, digital and mixed-signal integrated circuits (ICs) are designed to function only in the determined supply voltage range. These are the operating voltage margins in which the circuit is designed to operate according to the specifications and are validated by performing simulations and measurements at wafer test. A successful simulation using power-supply variations ensures a deterministic behaviour of the fabricated device. However, other non-ideal characteristics of the voltage supply, such as the rise time of the voltage on power-up and possible errors in the power system, also have to be accounted for to preserve the deterministic behaviour despite the exceeded voltage tolerances. These conditions are usually met by an appropriate circuit design within IC which triggers a control pulse when the power-supply conditions are not suitable. An on-chip solution is used since the voltage from the off-chip supply voltage may vary substantially due to an unknown amount of the parasitic capacitance outside IC [2].

In the literature, the power-on reset (POR) signal is typically an output of a block which generates a signal of a certain duration on a specific voltage threshold during power-up. Its purpose is to hold digital and/or analogue blocks in reset for the settling time during power-on. On the other hand, a brown-out reset (BOR) generates a reset pulse when a certain threshold voltage is detected on a power line in case of a power-supply failure or at a power-off event. In some cases, both the duration and the magnitude of an event are determined in this circuit, therefore only a large current draw or an excessive supply noise can trigger a reset pulse in case of an error [1].

System [3] presents a novel method of a low-cost position encoder because both the integrated micro transformers as the sensing elements and analogue front-

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end electronics for signal processing and demodulation are fabricated in a conventional commercially-available four-metal $350 - nm$ CMOS process. The previous implementation of the system is reported to achieve a linear resolution of $20\,\mu m$ with a steel and copper scale.

2 System analysis

Although system [3] consists of an analogue oscillator, the designed POR circuit is configured to initialize the delay in terms of a prolonged pulse only for short power-supply voltage-rise times. This ensures a robust operation in case of either a power-on voltage with an unexpectedly short rise time which tends to be unstable even after reaching $3.3\ V$ or a sudden power-supply voltage outburst. In case of the latter, a reset pulse of a known duration ensures a sufficient reset of the system. In case of typical power-supply voltage-rise times, the function of the prolonged reset is later initialized in circuits needing it (such as the oscillator).

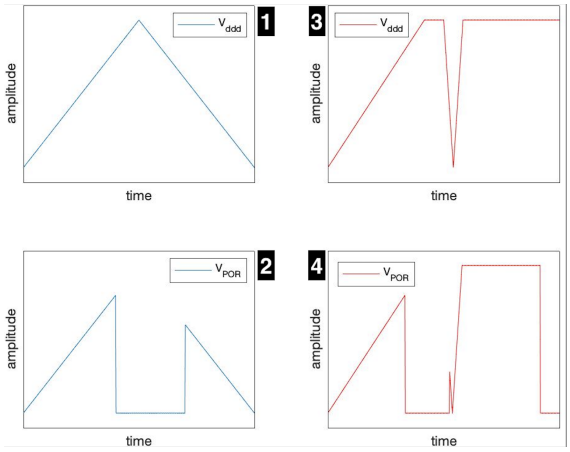

Figure 1. Superficial operation demonstration.

The POR and BOR functionality are initialized as a $V_{TH,HIGH}$ and $V_{TH,LOW}$ threshold-voltage detection. The voltages are set apart with a hysteresis. In Figure 1, $V_{TH,LOW}$ and $V_{TH,HIGH}$ are indicated on the ordinate axis plotted by the abscissa, showing the time domain. A superficial operating principle of the circuit is shown with an input power-supply voltage (marked as V_{ddd} in Section 2) and an output voltage (marked as V_{POR} in Section 1). Upon voltage-supply power-up, the voltage with a positive slope of a constant value is applied rising from $0\ V$ to $3.3\ V$. The output of the circuit follows the power-supply voltage until the value crosses $V_{TH,HIGH}$. At this point, the system is determined to be powered-up appropriately, therefore V_{POR} is set to $0\ V$ releasing the reset signal. The second part of the shown period represents a standard power-down case. In this case, the supply voltage drops with the same negative slope. Crossing $V_{TH,LOW}$ indicates unstable operating conditions, therefore the output follows the supply voltage conducting the reset procedure. This is the state of a nominal system operation where the slopes correspond to a typical power-supply rise time (typically $16\ \mu s$) which can vary from $10\ \mu s$ to $20\ \mu s$.

In Section 3, the power-on sequence is indifferent to the one in Section 1. However, an error occurrence is demonstrated after that. In this case, a voltage drop caused by a brief high-current drain will first trigger a POR output reset (demonstrated in Section 4) upon the power supply negative slope. After that, a prolonged reset will be triggered upon the power-supply voltage with a positive slope (assuming that the slope is steep enough).

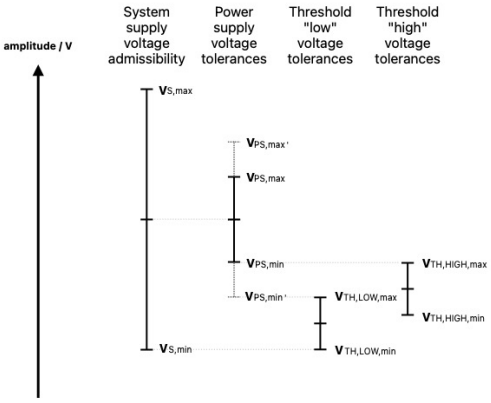

Figure 2. System tolerances.

The switching voltage points are set apart by a hysteresis which ensures two fundamental tasks. Firstly, oscillations of the output are prevented in a non-monotonic supply-voltage event. This may be caused either by the noise of the power supply or any sudden current drain. In such case, the purpose of the hysteresis is to allow the evaluation of a reset logic switch even in such non-ideal voltage-flow circumstances (a similar approach is taken in Power-On Reset and Related Supervisory Functions [4] but with only one threshold voltage).

Secondly, by considering both the voltage-source tolerances and nominal-system operating-voltage range when designing the hysteresis, both the wider voltage-source tolerances and additional precautions for abiding an erroneous system operation can be applied. Figure 2 examines the instance in which the hysteresis is set to perform the described operation. Both the system and power-supply tolerances are displayed besides the hysteresis tolerances of $V_{TH,LOW}$ and $V_{TH,HIGH}$.

The tolerance of $V_{TH,LOW}$ is set to the lowest value corresponding to the lowest value of the system-supply tolerance, guaranteeing a reset trigger for lower voltages. On the other hand, the upper limit at

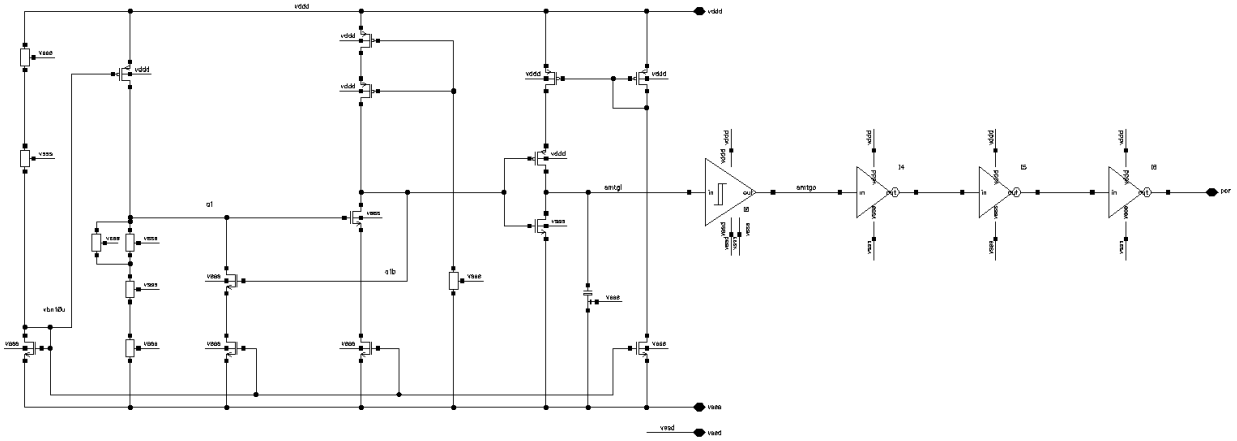

Figure 3. Proposed circuit.

$V_{TH,LOW}$ sets the minimum tolerances for the noise.

The $V_{TH,HIGH}$ tolerance is set to the highest edge, matching the lowest edge of the original power-supply tolerance, whereas clearing the reset on its lower edge still guarantees a stable operation.

3 PROPOSED CIRCUIT

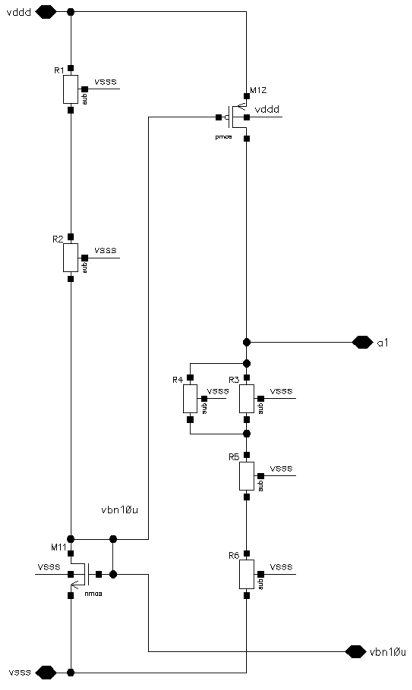

Figure 4. First segment.

The design of the proposed circuit is shown in Figure 3. The circuit is designed in the XFAB $350\,nm$ technology. The voltage detection and hysteresis are achieved by preventing the selected transistors from entering the saturation region. This is done by limiting either their U_{DS} and U_{GS} or I_D.

$$I_{DS,M11} = \frac{V_{ddd} - V_{GS,M11}}{R} \tag{1}$$

$$I_{DS} = \frac{\mu_0 C_{ox}}{2}\frac{W}{L} \\ (V_{GS} - V_{Tn})^2\Big[1 + \lambda(V_{DS} - (V_{GS} - V_{Tn}))\Big] \tag{2}$$

Firstly, the steady-state current is set with a simple current source consisting of an NMOS transistor in a diode configuration ($M11$) and two resistors ($R1$ and $R2$). At saturation, current I_{M11} is set by Eqs. (1) and (2) where R is the combined resistance of resistors R1 and R2, V_{Tn} is the threshold voltage, λ is the modulation of the transistor channel length and C_{ox} is the capacitance of the thin oxide. The diode voltage is then connected to the gate of the PMOS transistor with its drain connected to a resistor array (resistors from $R3$ to $R6$). Both circuits (Figure 4) are designed so that the current flows even when the supply voltage isn not high enough for the band gap source to work properly. Upon power-up, the diode voltage (marked as $vbn10u$) on $M11$ rises rapidly and settles, whereas the current rises linearly from its diode knee voltage. However, the PMOS only switches from the cutoff region to the saturation region when the difference between V_{ddd} and V_{vbn10u} (the U_{DS} of the PMOS) is high enough to act as a delayed voltage rise on $a1$. [7]

The next part acts as an inverter with a positive feedback loop (Figure 5). In theory, only $M7$ with a pull-up resistor could be used. To lower the layout area, the resistor can be replaced by a enhanced load device consisting of an NMOS in a diode configuration. However, in this design, two PMOS transistors ($M5$ and

$M6$) are used with their gates connected to the ground through a resistor ($R0$). The length of the two transistors is halved to ensure a greater fabrication repeatability. The described configuration of the elements around $M7$ gives an output with a voltage rise until the voltage on the $M7$ gate is high enough to slowly and continuously switch the output to $0V$. NMOS $M8$ is used to limit the current. The transistor acts as an NMOS current mirror connected to $M11$. The hysteresis is achieved by adding NMOS $M9$ which acts as a feedback loop and $M10$ current mirror for setting the feedback gain.

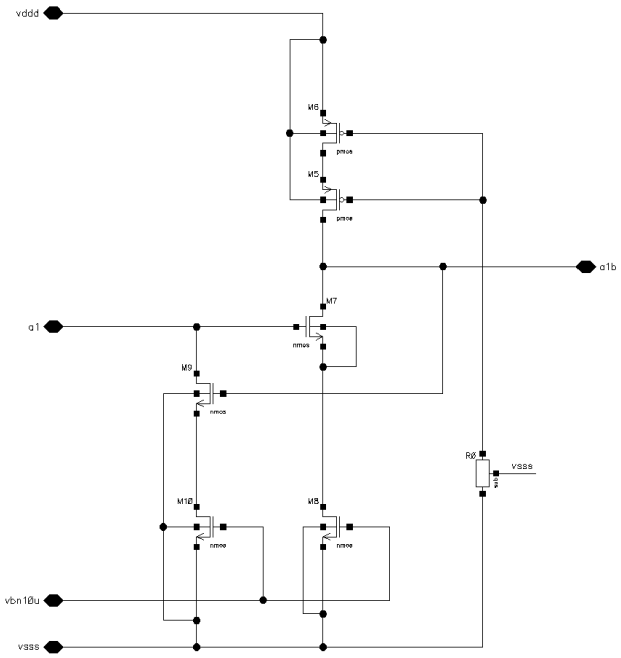

Figure 5. Second segment.

In saturation, transistors $M8$, $M10$, $M4$, $M0$ and $M1$ act as a voltage-driven current sources together with $M1$. The mirroring transistor pairs are of the same type to achieve the same threshold voltages, carrier mobility and channel modulation length. The same effective channel lengths (L) are used since the threshold voltages and channel length modulations are dependent on this parameter. The current is calculated by dividing the paired I_{DS} currents as this is done in Eq. (3) for transistors $M11$ and $M8$. The equation is further simplified by assuming that the transistor acts as an ideal current source. [7]

$$\begin{aligned} N &= \frac{I_{DS,M8}}{I_{DS,M11}} \\ &= \frac{W_8}{W_{11}} \frac{1+\lambda(V_{DS_8}-(V_{GS_8}-V_{Tn_8}))}{1+\lambda(V_{DS_{11}}-(V_{GS_{11}}-V_{Tn_{11}}))} \\ &= \frac{W_8}{W_{11}}. \end{aligned} \tag{3}$$

In the next stage, an inverter is implemented (transistors $M2$ and $M3$) with its output connected to a non-inverting Schmitt trigger (Figure 6). The inverter acts as a low-pass RC filter consisting of a capacitor ($C0$) and resistance which varies depending on the front of the signal. In case of $3.3\,V$ on the inverter input (the connection marked as $a1b$), only the resistance of NMOS $M3$ in saturation is applied (the resistance is set to the Kilo Ohms region). In case of $0\,V$ on the inverter input, the current is first set with NMOS current mirror from $M11$ to $M4$ connected to a PMOS current source $M0$ with a current mirror $M1$. In this case, the resistance is set to $500\,k\Omega$.

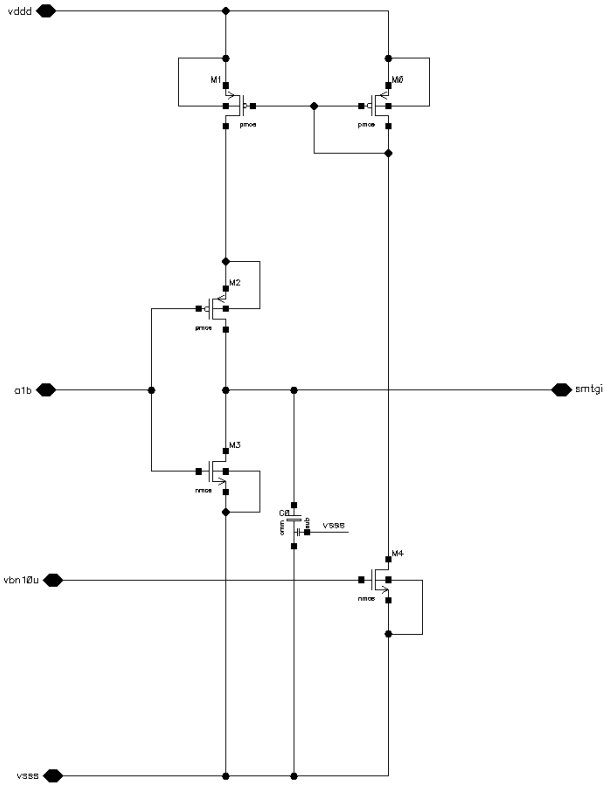

Figure 6. Third segment.

To a certain degree, the low-pass filter effects the hysteresis. Specifically, it shifts the $V_{TH,HIGH}$ threshold depending on its slope. Yet, the effect of the filter on $V_{TH,LOW}$ is less evident. This shortens the capacitor discharge times allowing the device both to respond to fast voltage drops and to properly set the circuit for the next power-on cycle (so that the capacitor does not store any charge from the previous cycle).

To match the design requirements for the BOR and POR threshold voltages and power supply outburst detection, the capacitance of the capacitor is chosen accordingly. By assuming the circuit operation shown in Figure 7 with continuously falling V_{ddd}, the cor-

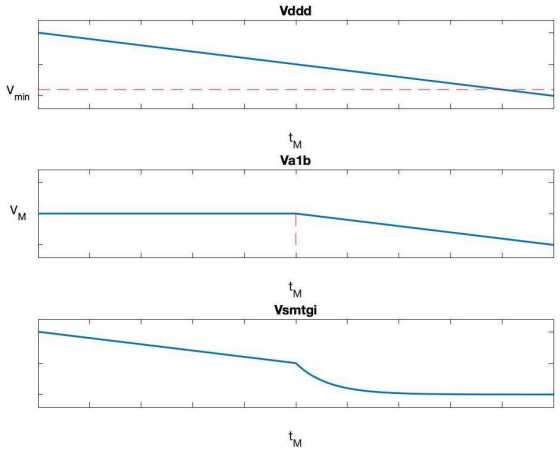

Figure 7. BOR analysis.

responding V_{a1b} and V_{smtgi} voltage courses are proposed and a mathematical model is set up. It is built as an RC circuit which approximates the large signal behaviour of the circuit around the capacitor $C0$. For the initial conditions at $t > t_M$, the voltage on the capacitor (V_{smtgi}) follows the supply voltage while V_{a1b} (representing V_{gs3}) is at V_M . At $t > t_M$, when M7 is expected to transit into the saturation region and assuming that $V_{a1b} = K * V_{ddd}$, the capacitor starts discharging. To analyze the borderline conditions for BOR, the linear differential equation of the first order (Eq. (4)) and its solution (Eq. (5)) are proposed. The drain-source resistance can be approximated either by Eq. (6) or used directly in a differential equation (in a form of $R = U_{DS}/I_{DS}$) in which case the equation is solved numerically. This is done in MATLAB® where the Euler method is implemented according to Eq. (7) with the differential equation rearranged in a form of $dy/dt = f(t, y)$. The solution is calculated by iteratively changing V_{ddd}. For each iteration, t_{int} is determined as the time at which $V_{smtgi}(t)$ crosses the lowest value at which an output switching is still possible ($V_{min} = V_{smtgi}(t_{init})$). Of all the solutions, the one corresponding to the steepest supply slope and meeting condition $V_{smtgi}(t_{init}) > V_{ddd}(t_{init})$ is determined as the BOR limit for a given capacitor value. POR and power supply outburst detection are determined by applying a similar analysis.

$$\frac{du_c}{dt} + \frac{1}{RC}u_c = 0 \tag{4}$$

$$u_c(t) = -V_M \cdot e^{-\frac{1}{\tau}} \cdot u(t) \tag{5}$$

$$R = \frac{1}{V_{Tn} - V_M} \int_{V_M}^{V_{Tn}} \frac{V_{DS}}{I_{DS}}\, dV_{DS} \tag{6}$$

$$y_{n+1} = y_n + \Delta t \cdot f(t_n, y_n) \tag{7}$$

For a typical power-on slope, $V_{TH,HIGH}$ is set at $3.1\ V$ and for a minimum slope, $V_{TH,HIGH}$ is set at $3.0\ V$. Steeper slopes activate higher $V_{TH,HIGH}$ voltages. Moreover, for the power-on rise times shorter than 11 us, the POR functionality is shifted to $3.3\ V$ and for all shorter rise times, logical 1 is held for an extended period of time allowing the system to sufficiently stabilize.

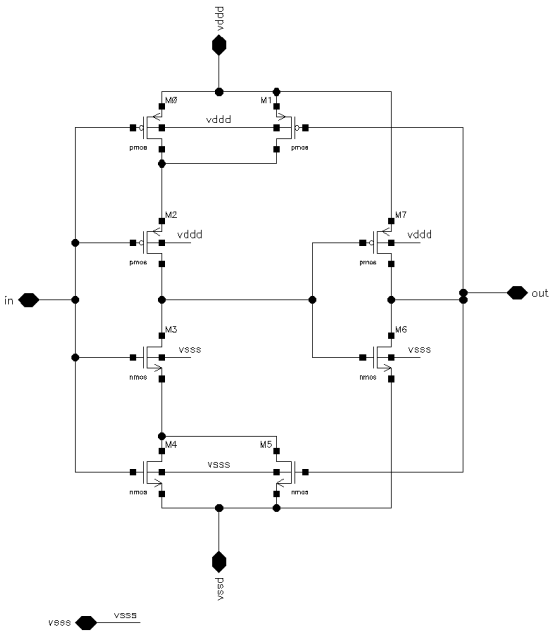

Figure 8. Schmitt trigger.

The function of the filter is also to hold the output state in case of a noise applied to the power-supply voltage in an instance where the DC component of the signal matches either switching point.

Between the filter and POR output, a signal-conditioning stage consisting of a Schmitt trigger and three inverters is implemented. The schematic of the non-inverting Schmitt trigger is shown in Figure 8. Its function is to set steep switching points. After that inverter $I1$ steepens the slope for the $V_{TH,LOW}$ switching point and $I2$ steepens it for the $V_{TH,HIGH}$ switching point. $I3$ acts both as a buffer and a phase correction circuit.

4 SIMULATIONS

The designed circuit is simulated with the Cadence® Virtuoso®Analog Design Environment XL (part of Cadence®Virtuoso®version $6.1.8 - 64b$). The transient, Corner and Monte Carlo analyses are performed in this step.

4.1 Transient analysis

First, an analysis of the current consumption is performed. After the reset output is released and the supply voltage stabilized at $3.3\ V$, the circuit consumes $34.96\ \mu A$. This is due to the high-voltage drops on resistors $R1$, $R2$, $R3$, $R4$, $R5$ and $R6$. To be specific, the current on $R1$ is $15.69\ \mu A$ and the current on the source connection of $M12$ is $14.34\,\mu A$. Other branches with a significant current consumption are $M6$ and $M0$ with their currents of $2.07\,\mu A$ and $2.86\,\mu A$, respectively.

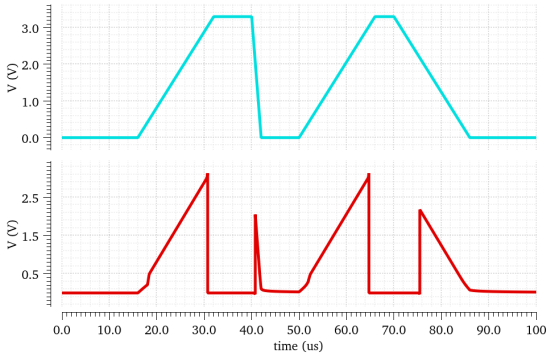

Figure 9. Transient analysis.

The highest current consumption occurs at the power-supply threshold values. With the power-supply spike of $191.35\ \mu A$ (at V_{ddd} being $V_{TH,HIGH}$), the highest current is consumed by the Schmitt trigger ($170.54\,\mu A$) and inverters $I2$ and $I3$.

Figure 9 shows the transient analysis results to validate the system activity. On both graphs, the time is plotted on the abscissa and the voltage amplitude on the ordinate. $3.3V$ supply voltage (the top graph in Figure 9) is applied with a rise time of $16\mu s$ demonstrating typical power-on conditions. The POR output (the bottom graph in Figure 9) follows the supply voltage until $V_{TH,HIGH}$ ($3.1V$) is reached. At $40\mu s$, the response to an erroneous power-supply operation instance is demonstrated. The supply voltage drops to $0\ V$ with a fall time of $2\ \mu s$ and BOR is triggered at $V_{TH,LOW'}$ ($2.0\,V$). After that, a typical power-on and power-off are shown. Upon a power-off sequence, BOR is triggered at $V_{TH,LOW}$ ($2.1\,V$) after which it follows the power-supply voltage.

With further transient analysis, threshold voltages $V_{TH,LOW}$ and $V_{TH,HIGH}$ and the delay feature occurrence are analyzed.

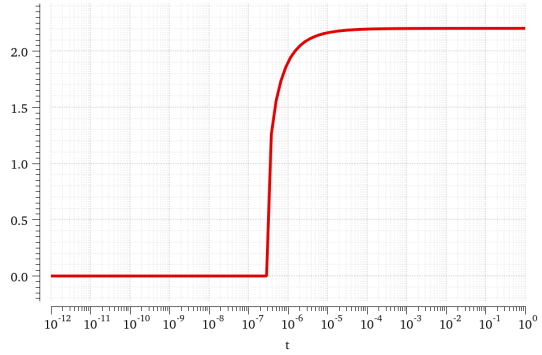

Figure 10. Low threshold voltage.

Firstly, the $V_{TH,LOW}$ threshold-voltage dependency on the power-supply voltage fall time is examined. Figure 10 shows the simulated $V_{TH,LOW}$ values of the transient sweep with fall times from $1\ ps$ to $1\ s$ with 100 automatic test points plotted on a logarithmic scale. Threshold voltage detection $V_{TH,LOW}$ activates at the power supply-voltage fall times longer than $354.5\ ns$ (where it activates the POR output at the threshold voltage of $685.86\,mV$). Longer fall times correspond to the higher $V_{TH,LOW}$ values with the limit at $2.204\,V$. With the power-supply voltage rise-time tolerances (described in Section 2), $V_{TH,LOW}$ reaches the values from $2.164V$ to $2.181\ V$.

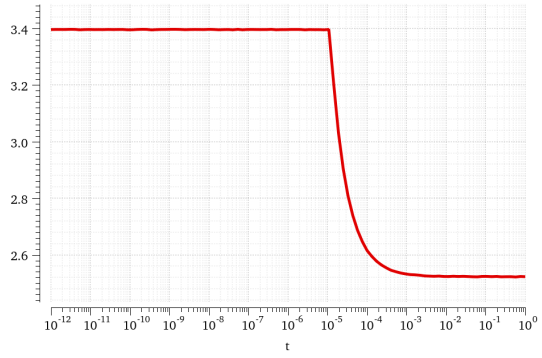

Figure 11. High threshold voltage.

Moreover, the BOR functionality is examined for the fall times shorter than $354.5ns$ was examined. Although the reset upon the power-supply voltage drop to $0\ V$ does not work, the BOR circuit still preserves part of its functionality. The capacitor is sufficiently discharged for the power-supply outbursts with the surface areas above $100\,nVs$. At the outbursts with the lower surface area, the POR functionality is therefore abolished.

Secondly, the $V_{TH,HIGH}$ threshold-voltage dependency on the power-supply voltage rise time is examined. Figure 11 shows the simulated $V_{TH,HIGH}$ values in the transient analysis sweep with the rise times from

$1\ ps$ to $1\ s$ with 100 automatic test points plotted on a logarithmic scale. By examining Figure 11 for the rise times above $11.0\,\mu s$, the $V_{TH,HIGH}$ logarithmically drops with its limit at $2.524\ V$. For the power-supply voltage fall time tolerances, $V_{TH,HIGH}$ reaches the values from $3.30\ V$ to $3.00\ V$.

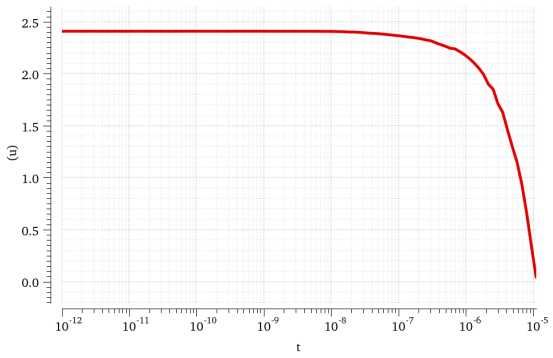

Figure 12. Prolonged pulse width.

Thirdly, the width and conditions for a prolonged reset pulse are determined with a simulation. The effects of this feature can be seen in Figure 11 where $V_{TH,HIGH}$ is at $3.3\ V$ for the power-supply voltage rise times less than $11.0\,\mu s$. Figure 12 shows an explicit presentation of this feature. A transient simulation with a sweep of the power-supply voltage rise times from $1.0\ ps$ to $11.0\ \mu s$ with 100 test points is made. The width of the prolonged reset is measured as an elapsed time from the point at which POR output reaches $3.3\ V$ upon power-up to the point at which POR passes $1.8\ V$ upon the end of the prolonged pulse. With the rising power-supply rise times, the width of the prolonged reset falls. For power-supply voltage fall time tolerances, the width reaches the values from $194.8\ ns$ to $0.0\ ns$.

Lastly, the noise immunity is measured. Two sets of the transient measurements are performed in which the supply voltage is set right below the threshold voltages $V_{TH,LOW}$ and $V_{TH,HIGH}$. At the DC voltages, a noise generator of $100\ MHz$ is used. For each analysis, a sweep of noise-generator amplitude V_{pp} is set, ranging from $0.1\,V$ to $3.3\,V$. For $V_{TH,LOW}$, the noise immunity up to the amplitudes of $1.75\ V_{pp}$ and for $V_{TH,HIGH}$ the noise immunity up to amplitudes of $0.4\ V_{pp}$ are confirmed.

4.2 *Corner analysis*

The corner analysis is performed for the power-supply voltage rise and fall times of 10 us, 16 us and 20 us. To achieve that, corner simulations are added to a transient analysis with the sweep of the power-supply voltage rise and fall times of $V_{TH,LOW}$, $V_{TH,HIGH}$ are measured.

The parameters for the analysis are provided by X-FAB. From the list of the model groups, tm, wp and ws are selected. The simulations are performed at temperatures $-30\,°C$, $27\,°C$ and $125\,°C$. Nine corners are performed on three transient sweep simulations.

Table 1. Threshold $V_{TH,LOW}$ corner analysis.

PS	normal	min	max
$10\ \mu s$	$2.164\ V$	$2.086\ V$	$2.212\ V$
$16\ \mu s$	$2.177\ V$	$2.099\ V$	$2.226\ V$
$20\ \mu s$	$2.181\ V$	$2.104\ V$	$2.230\ V$

Table 2. Threshold $V_{TH,HIGH}$ corner analysis.

PS	normal	min	max
$10\ \mu s$	$3.300\ V$	$3.172\ V$	$3.300\ V$
$16\ \mu s$	$3.127\ V$	$2.898\ V$	$3.300\ V$
$20\ \mu s$	$3.000\ V$	$2.809\ V$	$3.259\ V$

The simulation results are shown in Tables 1 and 2. They present the normal (with no corner analysis at $27\ °C$), minimum and maximum values for each measurement. Table 1 presents the $V_{TH,LOW}$ corner analysis results. Table 2 presents the $V_{TH,HIGH}$ corner analysis results.

4.3 *Monte Carlo analysis*

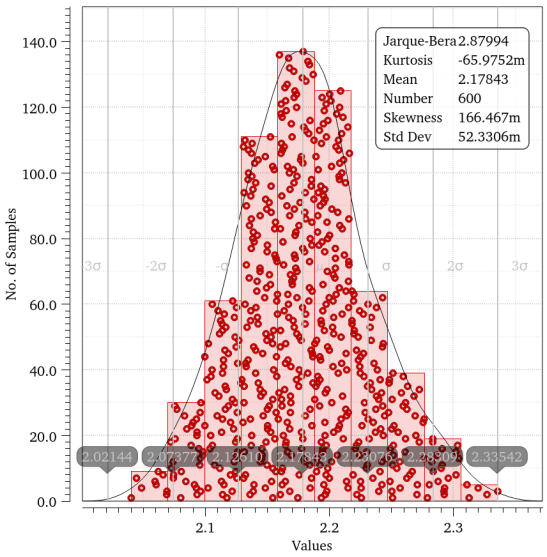

Figure 13. Gaussian Monte Carlo simulation.

A Monte Carlo analysis is performed to determine the circuit tolerance to the process variations and statistical mismatch for the supply-voltage rise and fall times of $16\ \mu s$. Six transient analyses are performed, all with randomly generated model parameters. A special set of the device models provided by XFAB are used [6].

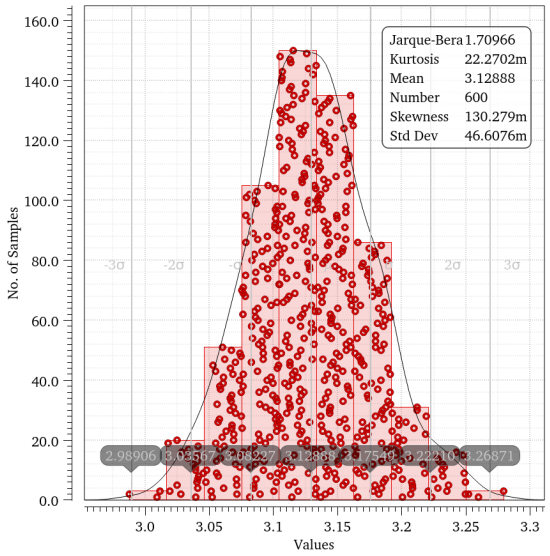

Figure 14. Gaussian Monte Carlo simulation.

Firstly, simulations of the process parameter variation are performed. In this step the Gaussian and uniform parameter distribution are applied for both threshold voltages. The low-discrepancy sequence sampling method at 600 points is set for each of the four described combinations.

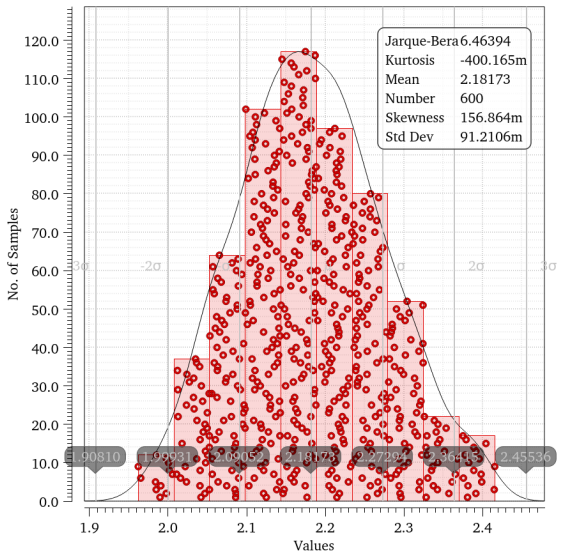

Figure 15. Uniform Monte Carlo simulation.

For the Gaussian parameter distributions at $\pm 3\ \sigma$ (Figure 13) of the $V_{TH,LOW}$ threshold voltage, the mean deviation of $2.17843\,V$ and standard deviation of $52.3306\,mV$ are achieved.

In Figure 14, the Gaussian parameter distribution at $\pm 3\ \sigma$ is shown for the $V_{TH,HIGH}$ threshold voltage. The mean and standard deviation are $3.12888\,V$ and $46.6076\,mV$ respectively.

For the uniform parameter distributions at $\pm 3\,\sigma$ (Figure 15) of the $V_{TH,LOW}$ threshold voltage, the mean and and standard deviation are $2.18173\,V$ and $91.2106\,mV$ respectively.

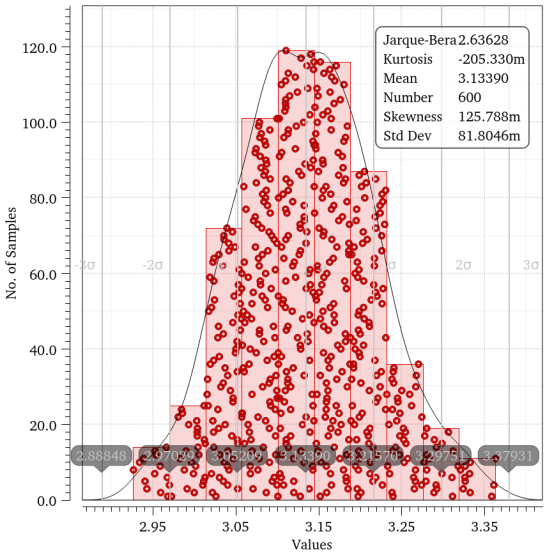

Figure 16. Uniform Monte Carlo simulation.

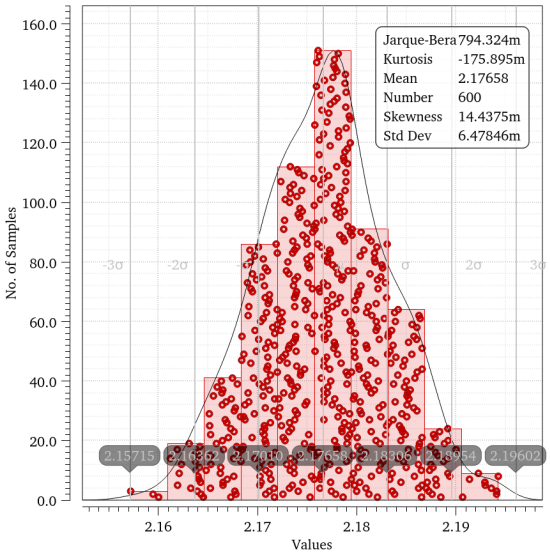

Figure 17. Gaussian Monte Carlo simulation.

In Figure 16, a uniform parameter distribution at $\pm 3\sigma$ is shown for the $V_{TH,HIGH}$ threshold voltage. The mean and standard deviation are $3.13390\,V$ and $81.8046\,mV$ respectively.

Secondly, a statistical device matching is performed. The matching parameters included in the models are de-

rived from real measurements and are always Gaussian-distributed. The results of the simulation are set to $\pm 3\sigma$ with the discrepancy sequence sampling method at 600 points [6].

Figure 17 shows the results of the simulation of the $V_{TH,LOW}$ threshold voltage. The mean and standard deviation are $2.17658\,V$ and $6.47846\,mV$ respectively.

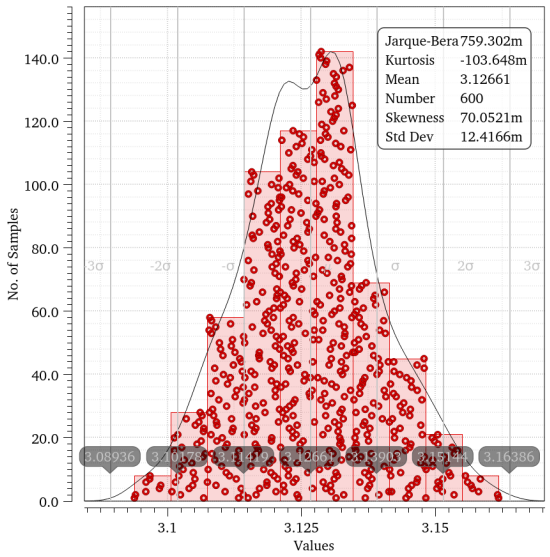

Figure 18. Gaussian Monte Carlo simulation.

Figure 18 shows the results of the simulation of the $V_{TH,HIGH}$ threshold voltage. The mean and standard deviation are $3.12661\,V$ and $12.4166\,mV$ respectively.

5 Layout

Figure 19 shows the implementation of the circuit for the XFAB $350nm$ process. In order to reduce the mismatch, the current mirrors are placed in a close proximity [5]. Furthermore, the devices of the same type are placed in a P-type or an N-type Guard Ring. The area of the circuit implementation is $300.450\,\mu m$ x $95.475\,\mu m$.

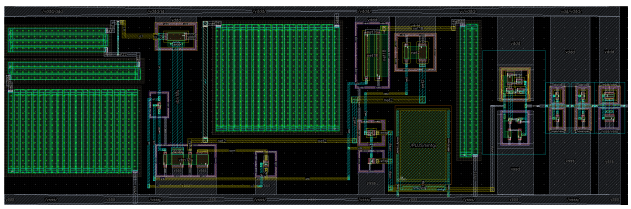

Figure 19. Layout of the circuit.

6 Conclusion

To assure a deterministic behaviour of the microelectronic systems, a circuit with a POR and BOR functionality is implemented. A circuit with such functionality used for an integrated inductive encoder [3] is analysed and designed for implementation in the XFAB $350\,nm$ process. During the development process, the literature on the topic is analyzed ([1], [2] and [4]) to optimize the circuit operation.

The designed circuit with a quiescent current of $34.66\,\mu A$ and peak consumption of $191.35\,\mu A$ has the two threshold voltages, i.e. $2.2\,V$ and $3.1\,V$, separated by a hysteresis. The BOR circuit detects the voltage outbursts with a surface area above $100\,nVs$. The BOR prolonged pulse is implemented (a reset lasting $2.4\,\mu s$ for the voltage rise time from $10^{-12}s$ to $10^{-8}s$).

The circuit optimally operates at the power-supply voltage rise and fall times from $10\,\mu s$ to $20\,\mu s$. The analysis is run for 12 decades of the power-supply transient conditions (from $1\,ps$ to $1\,s$). The corner analysis is preformed for the optimal power-supply transient conditions. The Monte Carlo analysis for the process tolerance variations and statistical mismatch is run for a single transient condition. The area of the circuit implementation for the XFAB $350\,nm$ process is $300.450\,\mu m$ x $95.475\,\mu m$.

The functionality of the circuit can be further developed to provide a BOR prolonged pulse with a longer period and precautions should be taken to reduce the size of the circuit.

7 Acknowledgment

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