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Low-pass filter for UWB system with the circuit for compensation of process induced on-chip capacitor variation

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Abstract: This paper describes the design and optimization of a Chebyshev 5th order low pass filter with included circuit for automatic process calibration and compensation. The filter is realized using lumped elements in 130 nm radio frequency (RF) CMOS process and is dedicated to cover lower sub-band (3.4 GHz – 4.8 GHz) of ultra-wideband (UWB) system. The proposed full on-chip calibration concept estimates MIM-Capacitor (Metal-Insulator-Metal) capacitance process-induced variation against more stable on-chip MOS capacitor reference. In order to estimate the capacitance value, a low frequency oscillator is designed, which uses both types of capacitors for generating the oscillations, one after another. The MIM capacitor value is determined in digital domain based on the ratio of two oscillation frequencies and its exact needed value is obtained using a compensation capacitor bank. Detailed mathematical optimization of the calibration method is presented.
All RF, analog and digital circuits have been integrated on a test chip and fabricated in 130 nm RF CMOS process. The produced ICs have been on-wafer measured and compared to simulation results. According to obtained results, the proposed calibration concept lowers process-induced filter transfer characteristic variation from approximately 5 dB to 0.6 dB at the critical frequency. The calibration needs to be applied just once at the beginning of circuit operation. The total area of implemented calibration circuit is less than 0.1 mm2. The same method and the compensation circuit can be employed for the calibration of all on-chip circuits whose performance is affected by MIM capacitance process variation.

Keywords: process variation; compensation; MIM capacitor; low-pass filter; UWB

Nizko pasovni filter za UWB system z vezjem za kompenzacijo procesno vzpodbujenega spreminjanja integriranega kondenzatorja

Izvleček: Članek opisuje optimizacijo Chebyshevega nizkopasovnega filtra petega reda, ki vključuje vezje za avtomatsko kalibracijo in kompenzacijo. Filter je realiziran z uporabo 130 nm CMOS procesa in je namenjen za podpas (3.4 GHz – 4.8 GHz) UWB sistema. Predlagan polno integriran koncept kalibracije ocenjuje spremembe kapacitivnosti MIM kondenzatorja v nasprotju s stabilnim referenčnim MOS kondenzatorjem. Za oceno kapacitivnosti je uporabljen nizkofrekvenčni oscilator. Opravljena je bila natančna matematična optimizacija kalibracijske metode.
RF, analogna in digitalna vezja so integrirana na testnem čipu v 1300 nm RF CMOS tehnologiji. Čipi so bili merjeni na rezini. Glede na rezultate predlagana kalibracija zmanjšuje procesno prožen prenos karakteristike sprememb za 0.6 do 5 dB pri kritični frekvenci. Ista metodologija se lahko uporabi za vsa vezja, ki so obremenjena s spremembami MIM kapacitivnosti.

Ključne besede: variacije procesa; kompenzacija; MIM kondenzator; nizkopasovni filter; UWB

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1 Introduction

Constant IC manufacturing technology scaling allows the device integration in ever smaller area. As an adverse effect, the size reduction causes degradation of the intrinsic precision of the manufactured components [1]. In order to satisfy extreme design constraints on the analog/RF circuits with given component tolerances, some method of digital calibration must be applied [1]. For the mass product solutions, it is very important that the calibration circuits take as small area on the silicon as possible. Since with the technology scaling the size of digital devices is reduced, it is possible to implement complex digital calibration circuits occupying very small on-chip area. Moreover, for consumer products, external references are not applicable, since the external component size is almost comparable to the chip size [2].

In this paper, the design of a passive, LC low-pass filter is described. The DC inductance value for on-chip inductors is mostly insensitive to process variations [2], but on-chip capacitors notably change their values due to the finite manufacturing accuracy. The Table 1 presents capacitor value variations for three types of capacitors, available in the used technology.

The MIM-capacitors are the most suitable for RF applications, since they are the most linear and have the highest Q-factor of all available on-chip capacitor types, so this type of the capacitor is chosen to be used in the design. In case of MIM-capacitors, the shift in capacitance occurs mostly due to the oxide thickness variation, rather than to the temperature-induced variation. Unfortunately, the shift in the capacitance value will degrade the final performance of circuits beyond allowed limitations, so an adequate calibration and compensation method must be applied. Presented calibration concept compensates MIM-capacitor variation and can be applied in any circuit which characteristics are deteriorated due to MIM cap process-induced variations.

Table 1: Tolerances of the available capacitors in the used technology

Capacitor type	Process and temperature (-40:125°C) tolerance
MIM	±15%
MOM	±15%
MOS	±4%

The Paper [3] has demonstrated a way to estimate and compensate capacitor values using an external reference. In [2], the calibration concept with the internal on-chip reference has been proposed, which makes calibration suitable for the small form factor solutions. The price is paid by limited accuracy of the reference, but at the other hand, the approach is insensitive to parasitic and systematic errors introduced by calibration circuit. This paper combines these two calibration approaches with additional optimizations, offering unique calibration solution, applicable for mass production. The proposed solution is applied on the low-pass filter calibration. The concept is verified through measurements.

The second section describes low-pass filter implementation. In the third section, the calibration concept is reviewed in detail. The experimental results are presented in the fourth section that is followed by conclusion in the fifth section.

2 Low-pass filter

2.1 Description

Ultra Wideband (UWB) systems are very suitable for low cost, low power or high data rate, short range communication. By using a large bandwidth, they are immune to narrow band interference and multipath fading. These systems are preferable in the applications that demand high security level, since transmitted signal is noise-like, and hence hard to intercept.

Filters are one of the key components in UWB systems. In transmitter, they control out-of-band radiation and suppress higher harmonics. In receiver, filters enable the suppression of unwanted signals and interferers. Proposed filter is designed for the lower band of UWB system according to 802.15.4a standard [4]. The filter can be applied in both, transmitter and receiver.

The specifications of the proposed 5th order Chebyshev low-pass filter are listed in Table 2. The specifications are chosen based on transmitter transmission power level and linearity and estimated levels of unwanted signals and interferers in image band on the receiver side. The Chebyshev filter has the best compromise between pass-band ripple, which degrades Error Vector Modulation (EVM) and selectivity, which limits out-of-band emission and reception.

Table 2: Filter specifications

Item	Value	Description
Zin	50Ω	
Zout	50Ω	
S11	<-10dB	

S22	<-10dB	
IL	<1 dB	Goal
Order	5	Chebyshev
Ripple	±0.5dB	
Fc	4.8GHz	3dB point
Selectivity	-15dB -30dB -40dB	@6.4GHz @8.53GHz @10.67GHz

The first filter implementation has been synthesized using ideal component values from [5]. Due to the low Q-factor of the on-chip passive components, optimization of component values under nominal conditions has been performed. The filter schematic and obtained S-parameter simulation results through all three process variation corners are presented in Figure 1 and Figure 2, respectively. The results are obtained on the schematic level and extracted parasitic effects after the circuit layout will introduce additional losses.

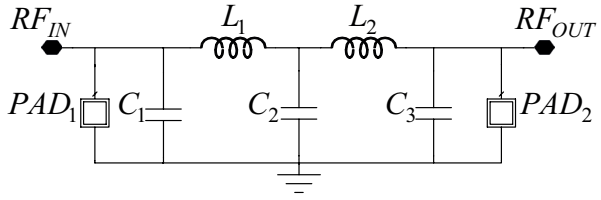


Figure 1: LPF- schematic

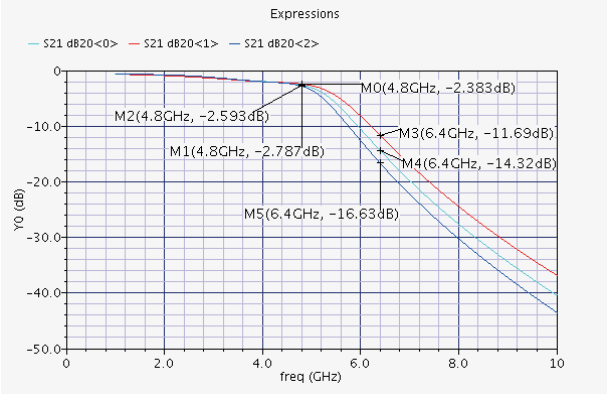


Figure 2: Filter transfer characteristic in slow(blue), typical(green) and fast(red) corner

As it can be seen from Table 2 and Figure 2, the specifications are not fulfilled under all process variations. One way to overcome this problem is to increase the order of the filter. That leads to overdesign at the price of larger chip area. Another solution is to apply a calibration and this solution is the preferred one.

3 Calibration

In this section, the calibration concept using internal reference is described in details.

The most suitable internal reference for on-chip capacitor calibration can be obtained using MOS capacitors. As it can be seen from the Table 1, the variation with a process and temperature is acceptable ±4%. But MOS capacitors are very nonlinear and can't be used in the circuits without appropriate polarization. For the purpose of the calibration, the reference MOS capacitor is polarized in the region where its nonlinear behavior is negligible.

3.1 Concept

Each of three capacitors from Figure 1 is replaced with a bank of one base and several tuning capacitors, used for the compensation. Depending on process variation effects on the capacitance value, the corresponding compensation capacitors are included or excluded from the circuit operation using RF switches, Figure 3. Thus, the effective capacitance is adjusted to the nominal value under all process variations. Control signals for the switches are generated from the circuits that estimate capacitor process variation.

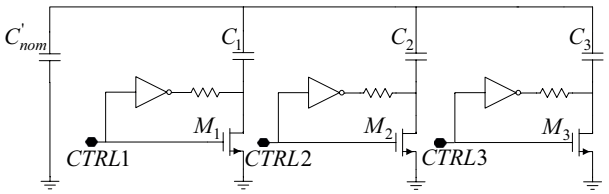


Figure 3: Capacitor bank

Figure 4 illustrates the concept of MIM-capacitor value estimation. The oscillator core generates oscillations on charge-pump principle using first the MIM and than the MOS capacitance. The MIM-capacitor value is calculated in digital domain by determining ratio of the oscillation frequencies which corresponds to inverse ratio of the MIM and MOS capacitor values.

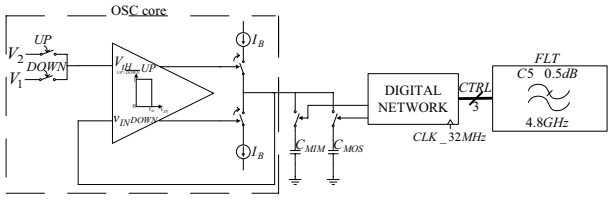


Figure 4: Calibration concept

The real advantage of the proposed approach is cancellation of PVT (Process, Voltage and Temperature)

variations for all components used for frequency ratio determination since the same oscillator core generates oscillations in both cases (with MIM and MOS capacitors).

Values of the capacitors in the cap bank and the process values at which they are included in the circuit operation are chosen according to the calculation derived in [3].

New value of the nominal capacitor is:

$$C'_{nom} = C_{nom}\frac{1+\varepsilon}{k_{\max}} \quad (1)$$

Where C_{nom} is the capacitor nominal value, ε is maximal acceptable error caused by discrete nature of compensation and k_{max} is maximal process value- k_{max}=1+3·σ, where σ is normalized standard process deviation for MIM-capacitors.

New, n-th compensation capacitor (2) is included in the circuit operation at the process value given by means of (3). It is assumed that C_{nom} is 1. Note, that at k_n process value, only C_n is included in the circuit operation.

$$C_n = \frac{\varepsilon\cdot(1+\varepsilon)}{1+3\cdot\sigma}\frac{2^n}{(1-\varepsilon)^n} \quad (2)$$

$$k_n = \frac{1-\varepsilon}{\frac{1+\varepsilon}{k_{\max}} + \sum_{i=1}^{n-1} C_i} \quad (3)$$

Satisfactory accuracy of up to ε=2% can be reached using three compensation capacitors. Normalized values of the compensation capacitors are presented in Table 3. All capacitor values are normalized to C_{nom}.

Table 3: Normalized values of the compensation capacitors in cap bank presented in Figure 3.

Capacitor name	Capacitor value
C'nom	0.8872
C_{C1}	0.0368
C_{C2}	0.0751
C_{C3}	0.1534

3.2 Switch design

Compensation capacitances are included in the circuit operation via RF switches as presented in the Figure 3. The switches are optimized so that the best compromise between insertion loss (when the switches are "on") and isolation (when the switches are "off") is obtained for the given application.

3.2.1 "On" state

When the switch is "on", the gate voltage corresponds to V_{DD}, while V_D= V_S=0. The impedance seen between drain and source terminals of the transistor is dominated by r_{ds} resistance, (4).

$$Z_{ON} \approx \frac{L}{W\cdot\mu\cdot C_{ox}\cdot(V_{DD}-V_{th})} \quad (4)$$

For the minimal transistor length and the fixed polarization we can assume that switch "on" resistance is approximately $R_{ON}\approx K_R/W$, where $K_R=\mu\cdot C_{0x}\cdot(V_{DD}-V_{th})/L$ is constant. This approximation is good enough in the observed case.

In order to calculate contribution of the switch "on" resistance to the filter insertion loss, we need to transform impedances (Figure 5).

$$R_P = R_S\cdot(Q^2+1), C_P = C_S\cdot\frac{Q^2}{Q^2+1}, Q = \frac{1}{\omega\cdot R_S\cdot C_S} \quad (5)$$

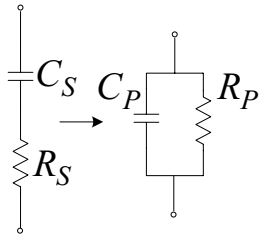


Figure 5: A series to parallel impedance transformation

For Q>10 we get:

$$R_P \approx R_S\cdot Q^2, C_P \approx C_S \quad (6)$$

Since we have three switches in the circuit, the total contribution of the switch "on" resistance to the node impedance can be expressed via equivalent parallel resistance, (7). Influence of the switch "on" resistance on filter performance is measured by means of Q-factor. Equivalent Q-factor of the observed node has the lowest value in the case when all three switches are "on". This case corresponds to the "fast" corner ($k=k_{min}$).

$$R_{eq} = R_1\cdot Q_1^2 \,||\, R_2\cdot Q_2^2 \,||\, R_3\cdot Q_3^2 \quad (7)$$

In that case, the equivalent Q-factor of each capacitor can be expressed by (8).

$$Q = \frac{r_0+r_1+r_2+r_3}{\omega\cdot k_{\min}\cdot C_{nom}\cdot K_R\cdot\left(\frac{r_1^2}{W_1}+\frac{r_2^2}{W_2}+\frac{r_3^2}{W_3}\right)} \quad (8)$$

Where r_i corresponds to C_{Ci}/C_{nom} ratio for i=1,2,3 and $r_0=C'_{nom}/C_{nom}$. These values are listed in Table 3. ω is angular frequency, k_{min} is minimal process value, C_{nom}

is nominal capacitor value, K_R is switch constant expressed above and W_i is width of the i-th switch which includes the compensation capacitors C_{Ci} into the circuit operation.

3.2.2 "Off" state

Figure 6 presents switch parasitic capacitors in "off" state. C_{gd} and C_{gs} are originating from overlap of the gate poly and drain/source areas and they can be approximately expressed via $C_{gd}=C_{gs}=C_{ov}=W\cdot L_{ov}\cdot C'_{ox}$. C_{db} and C_{sb} are junction capacitances between drain/source terminal and substrate. This capacitance is usually decomposed into bottom plate capacitance, associated with the bottom of the junction, C_j and sidewall capacitance due to the perimeter of the junction, C_{jsw}. C_j and C_{jsw} are capacitance per unit area and unit length, respectively, and both can be expressed as $C_j=C_{j0}/(1+V_R/\phi_B)^m$, where V_R is reverse voltage across junction. ϕ_B is the junction build-in potential and m is typically in the range of 0.3 and 0.4 [6]. In order to make these capacitances as low as possible, multi-finger structure is adopted and the drain is connected to the supply voltage in switch "off" state. The switch polarization, as presented in Figure 3, is done via inverter and a high value resistor. The resistor increases output inverter impedance since it appears in parallel with switch "off" impedance.

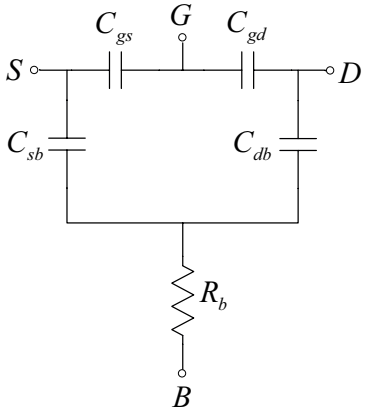


Figure 6: Switch in "off" state

R_{sub} models the substrate resistance from the junction to the substrate ground and in the given technology it depends on size and distance of the substrate contacts, the transistor size, the number of the gate fingers, and even of nearby circuit elements [7].

With the given polarization and multi-finger structure and with neglecting R_{sub} the impedance seen from the drain terminal is mainly capacitive and given by means of the following formula:

$$C_{drain} \approx C_{db} + \frac{C_{dg}\cdot C_{gs}}{C_{dg}+C_{gs}} \approx \frac{W}{2}\cdot E\cdot C_j + \\ + 2\cdot(\frac{W}{2}+E)\cdot C_{jsw} + \frac{W}{4}\cdot L_{ov}\cdot C'_{ox} \quad (9)$$

Where W is transistor width, E is width of the diffusion at drain terminal, L_{ov} is determined by the technology and represents length of an overlap area between gate poly and drain diffusion area, while C'_{ox} is oxide capacitance per unit area.

With the adopted polarization, we can approximately conclude that the drain capacitance is determined with the technology parameters and transistor width, $C_{drain}\approx K_C\cdot W$. Note that in the frequency range of interest (up to 10GHz) and with a good layout we can neglect R_{sub} in a given technology. Also W/2>>E is assumed.

Capacitor error (ε_p) due to the switch parasitic capacitance is largest when all switches are "off" and that occurs in slow process corner $k=k_{max}$.

$$\varepsilon_p = \frac{k_{max}\cdot r_1}{1+\frac{k_{max}\cdot r_1\cdot C_{nom}}{K_C\cdot W_1}} + \frac{k_{max}\cdot r_2}{1+\frac{k_{max}\cdot r_2\cdot C_{nom}}{K_C\cdot W_2}} + \\ + \frac{k_{max}\cdot r_3}{1+\frac{k_{max}\cdot r_3\cdot C_{nom}}{K_C\cdot W_3}} \quad (10)$$

3.2.3 Switch optimization

Without compensation, the IL (Insertion Loss) is determined by Q-factor of the inductors. With the compensation present, the switches can significantly degrade the IL. In order to prevent it, equivalent capacitor Q-factor has to be high enough at the frequency range of interest.

According to (8) equivalent capacitor Q-factor decreases with a frequency. Thus, insertion loss will be the most degraded at the highest frequency where it is important: at cutoff frequency ($f=f_c$=4.8GHz). Based on simulation results that consider degradation of IL due to equivalent capacitor Q-factor degradation, it is found that for capacitors having Q-factor above 40 at f_c, the degradation will be lower than 0.5dB.

From (8) we can observe that transistor width should be maximal in order to have high Q-factor. From the other side, the width should be minimal for the minimal error, (10) so, the optimal trade-off between insertion loss and capacitor error needs to be made. The calculation below gives the optimum ratio of switch width for a given Q-factor.

The goal is to minimize ε_p for a given Q. For the derivation we are going to use Jesen's inequality-

$$\forall x_1,x_2,x_3 : t_1 \cdot f(x_1)+t_2 \cdot f(x_2)+t_3 \cdot f(x_3) \geq f(t_1 \cdot x_1+t_2 \cdot x_2+t_3 \cdot x_3)$$

Where f is a convex function, x_1, x_2 and x_3 in its domain, t_1, t_2 and t_3 positive weights for which applies- $t_1+t_2+t_3=1$. Equality applies if and only if $x_1= x_2= x_3$ or f is linear. For $f(x)=1/x$, we can write:

$$\frac{r_1}{t} \cdot f\left(1+\frac{k_{\max} \cdot r_1 \cdot C_{nom}}{K_C \cdot W_1}\right)+\frac{r_2}{t} \cdot f\left(1+\frac{k_{\max} \cdot r_2 \cdot C_{nom}}{K_C \cdot W_2}\right)+ \\ +\frac{r_3}{t} \cdot f\left(1+\frac{k_{\max} \cdot r_3 \cdot C_{nom}}{K_C \cdot W_3}\right) \geq \\ f\left(\frac{r_1}{t} \cdot \left(1+\frac{k_{\max} \cdot r_1 \cdot C_{nom}}{K_C \cdot W_1}\right)+\frac{r_2}{t} \cdot \left(1+\frac{k_{\max} \cdot r_2 \cdot C_{nom}}{K_C \cdot W_2}\right)+\right. \\ \left.+\frac{r_3}{t} \cdot \left(1+\frac{k_{\max} \cdot r_3 \cdot C_{nom}}{K_C \cdot W_3}\right)\right) \quad (11)$$

$$\frac{r_1}{t}+\frac{r_2}{t}+\frac{r_3}{t}=1 \quad (12)$$

From (10), (11) and (12) we can obtain:

$$\frac{\varepsilon_p}{t} \geq k_{\max} \cdot \frac{1}{1+\frac{k_{\max} C_{nom}}{t \cdot K_C} \cdot \left(\frac{r_1^2}{W_1}+\frac{r_2^2}{W_2}+\frac{r_3^2}{W_3}\right)} \quad (13)$$

Using (8) we can rewrite (13):

$$\varepsilon_p \geq t \cdot k_{\max} \cdot \frac{1}{1+\frac{k_{\max}}{k_{\min}} \frac{1}{t \cdot K_C} \cdot \frac{r_0+r_1+r_2+r_3}{\omega \cdot K_R \cdot Q}} \quad (14)$$

For constant Q at f_c, the expression from the right side in (14) is constant. Note that the expression doesn't vary with the frequency, since it cancels out.

Minimal error can be obtained in the case when the left and the right side of (14) are equal. It will be the case if and only if:

$$1+\frac{k_{\max} \cdot r_1 \cdot C_{nom}}{K_C \cdot W_1}=1+\frac{k_{\max} \cdot r_2 \cdot C_{nom}}{K_C \cdot W_2}=1+\frac{k_{\max} \cdot r_3 \cdot C_{nom}}{K_C \cdot W_3} \quad (15)$$

We can than rewrite (15) into condition:

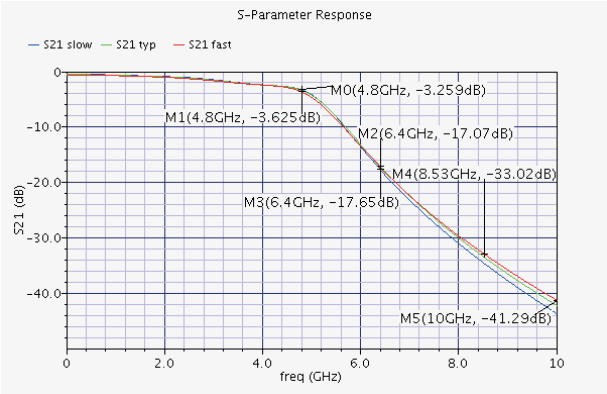
$$\frac{r_1}{W_1}=\frac{r_2}{W_2}=\frac{r_3}{W_3} \quad (16)$$

With specified Q-factor at f_c and (16) and (8) we can obtain the widths of the switches for all three capacitors.

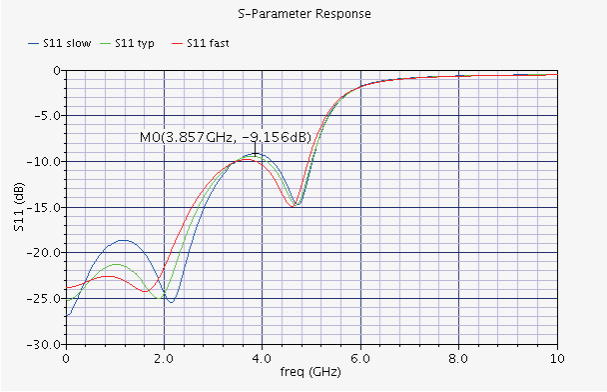
Note that with choosing Q-factor value at f_c, we determine the capacitor error, too. So if the error for chosen Q-factor is not satisfactory, one can decrease it at the cost of higher IL. For Q_C=40 we obtain maximal error of $\varepsilon_p \approx 2\%$ which is acceptable. For the capacitor C_2 the switches are sized for these values. For C_1 and C_3 we are restricted with the minimal size of switches in the used technology. In this case, Q_C=35 for $\varepsilon_p \approx 2\%$. Note that the worst IL degradation and maximum error arise in the case of different corners. For selected switch widths, the IL degradation at f_c is below 0.6 dB.

3.3 Compensated filter

The compensated filter is simulated on the extracted level through "fast", "typical" and "slow" corners and obtained S-parameter results are presented in Figure 7.



a)



b)

Figure 7: S-parameters of the compensated filter in slow (blue), typical (green) and fast (red) corner- a) S21 b) S11

If we compare the results with the ones obtained in the non compensated case, Figure 2, we can conclude that the filter transfer characteristic variation of 5 dB at the critical frequency 6.4 GHz is lowered to only 0.6 dB and the specifications are met under all process variations.

3.4 Capacitor value estimation

In this section, circuit that generates control bits for designed switches is described in detail.

3.4.1 Oscillator

The oscillator concept is presented in Figure 8 and is in detail described in [3]. Single-ended oscillator circuit generates oscillations on the charge-pump principle. Although the topology is more-less the same like in [3], the design optimization differs a lot. As noted, the design procedure in this work gains the benefits from using the internal reference, since the accuracy of the capacitor value estimation is insensitive to the temperature, power supply and process variations and on the parasitic influences of the line connections.

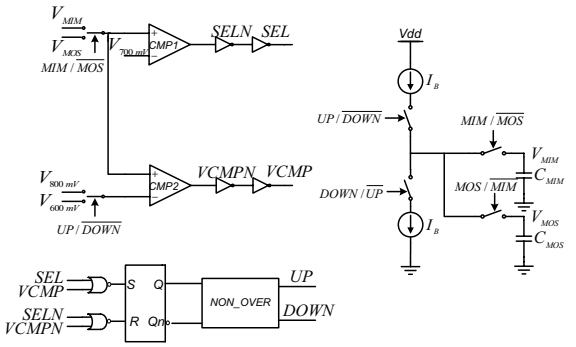


Figure 8: Oscillator- concept

Digital logic coordinates the oscillator. Digital signal *osc_enb* sets the oscillator in the initial state and enables its running. The *MIM / MOS* signal determineds weather the oscillation are generated with MIM or MOS capacitance. The signal *SEL* in the oscillator has the rectangular shape. Its frequency corresponds to the oscillation frequency and is measured in the digital domain.

The oscillation period is proportional to the value of the measured capacitance, (17).

$$T_{MIM/MOS} = \frac{2 \cdot C_{MIM/MOS} \cdot \Delta V_C}{I_B} = \frac{2 \cdot C_{MIM/MOS} \cdot (V_2 - V_1)}{I_B} \quad (17)$$

In digital domain, the oscillations using each of capacitors are counted within predefined measure time, $T_{measure}$.

$$COUNT_{MIM/MOS} = \frac{T_{measure}}{T_{MIM/MOS}} \quad (18)$$

$$\frac{COUNT_{MOS}}{COUNT_{MIM}} = \frac{T_{MIM\_ideal} \cdot (1+\alpha_{MIM})}{T_{MOS\_ideal} \cdot (1+\alpha_{MOS})} = \frac{C_{MIM}}{C_{MOS}} \cdot \frac{1+\alpha_{MIM}}{1+\alpha_{MOS}} \approx \frac{C_{MIM}}{C_{MOS}} \quad (19)$$

In (19) α_{MIM} and α_{MOS} model the oscillation period deviations from the nominal values caused by non-idealities; namely, inaccurate on-chip current source, non-ideal current mirroring, offset of operational amplifiers, V_1 and V_2 variations, parasitic capacitance and resistance of the connection lines. Since non-idealities are almost the same in both cases of oscillations due to the same oscillator core, follows that $\alpha_{MIM} \approx \alpha_{MOS}$.

Voltages V_1 and V_2 have to be high enough that nonlinear behavior of MOS capacitor does not affect the calibration accuracy. From the other side, these voltages have to be low enough, so the "P side" of current mirrors has high output impedance.

Proposed calculation shows the influence of V_1 and V_2 voltages on the estimation error caused by MOS cap non-linearity.

According to ACM (Advance Compact MOSFET) model, gate capacitance, for V_{DS}=0, can be expressed by means of (21) [9].

$$C_{gate} = C_{gs} + C_{gd} + C_{gb} \quad (20)$$

$$C_{gate} = \frac{n-1}{n} C_{0x} + \frac{1}{n} C_{0x} \frac{\sqrt{1+IF}-1}{\sqrt{1+IF}} \quad (21)$$

$$\frac{V_G - V_{T0}}{n} - V_{S,D} = \phi_t \left[\sqrt{1+IF} - 2 + \ln(\sqrt{1+IF} - 1) \right] \quad (22)$$

$$n = n(V_G), C_{ox} = W \cdot L \cdot C'_{0x}, \phi_t \approx 26mV (t^\circ = 27^\circ C) \quad (23)$$

In (21), C_{0x} is gate oxide capacitance, n is so-called slope factor and is a function of gate voltage, IF is inversion factor which can be calculated using (22). In (22), V_{T0} is threshold voltage, Φ_t is thermal voltage and V_G, V_S and V_D are transistor gate, source and drain voltages.

For the chosen value of MOS capacitor and high enough V_G, the C_{ox} is determined. Using the procedure described in [9] we can extract parameters V_{T0} and $n(V_G)$. For V_D=V_S=0 from (22), we can express IF and substitute it in (21). Now we are obtaining the gate capacitance as a function of gate voltage, C_{gate}= $C_{gate}(V_G)$. With this expression, we can calculate deviation of T_{MIM}/T_{MOS} ratio in nominal conditions from ideal (T_{MIM}/T_{MOS}=1) as a function of V_G.

Using (24) we can express voltage across MOS cap (gate voltage) as a function of time. We are assuming that capacitor charges from voltage V_1 with constant bias current, I_B.

$$I_B = C_{gate}(v_C) \frac{dv_C}{dt}, v_C(0) = V_1 \quad (24)$$

From (25) we can find time needed to charge observed cap from V_1 to V_2, namely $T_{MOS}(V_1,V_2)$.

$$v_C(t) = V_2 \rightarrow T_{MOS}(V_1, V_2) \quad (25)$$

In order to have ideal ratio $T_{MIM}/T_{MOS}=1$, we are choosing:

$$C_{MIM} = \frac{C_{gate}(V_1) + C_{gate}(V_2)}{2} \quad (26)$$

Combining (17) and (26) we can express $T_{MIM}=T_{MIM}(V_1, V_2)$. With that and (25), we can express error $(T_{MIM}/T_{MOS}-1)\cdot 100\%$ in respect to V_1 i V_2. The absolute error is depicted in Figure 9 as the function of V_1 for $V_2=V_1+0.1$ V, $V_2=V_1+0.2$ V and $V_2=V_1+0.3$ V.

As can be seen from the Figure 9 the error caused by MOS cap non linearity is negligible for $V_1>0.6$ V for $V_2-V_1\leq 0.2$ V.

In order to have constant current capacitor (de)charging, which is assumed during all calculations, current mirrors should have high output resistance. Furthermore, $T_{osc}/2$ should be larger than clock for digital logic under all PVT variations in order to synchronize and sense the oscillations in digital network. The nominal values of $C_{MIM/MOS}=30$ pF, $I_B=100$ µA, $V_1=0.6$ V and $V_2=0.8$ V allow these conditions to be realizable with the acceptable area of the oscillator.

The oscillator with the bias sources is fully implemented. Two current sources are designed, one for the comparators polarization, another for the purpose of charging and discharging the capacitors through current mirror. The sources are self-biased and operate using the positive feedback. For each source, Schmitt trigger is designed in order to provide certain start under all PVT variations.

Oscillation frequency for both, MOS and MIM capacitors, simulated through 81 different PVT combinations,

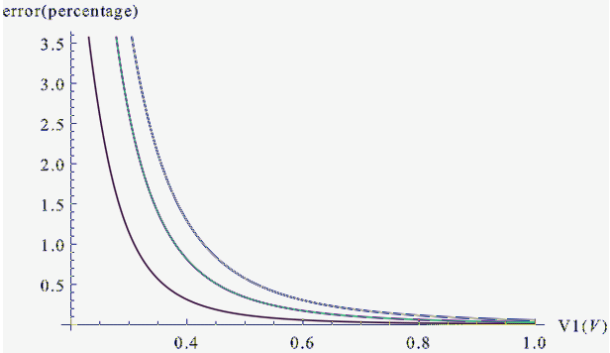


Figure 9: Error in MIM cap value estimation due to the finite MOS cap linearity versus V_1, for $V_2=V_1+0.1$ V (green), $V_2=V_1+0.2$ V (purple) and $V_2=V_1+0.3$ V (blue)

changes a lot, due to the full on-chip implementation. The obtained frequencies are in the range from 3.37MHz to 15.41MHz. Figure 10 presents time waveforms of the slowest, nominal and fastest oscillations that occur with MIM-capacitors.

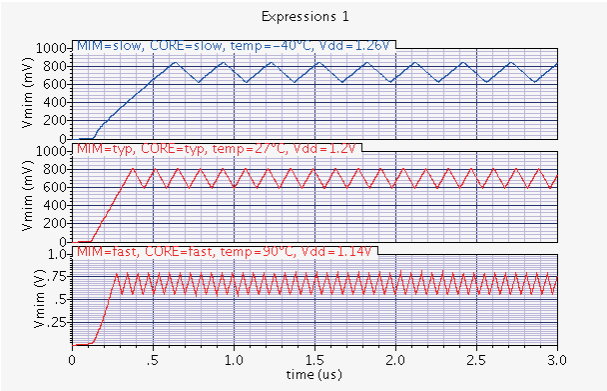


Figure 10: Oscillation waveforms in the slowest, nominal and fastest case

Table 4: C_{MIM}/C_{MOS} ratio for different PVT values on the extracted level

Item	Vdd=1.14V			Vdd=1.2V			Vdd=1.26V		
T [°C]	-40	27	90	-40	27	90	-40	27	90
CORE corner	MIM cap in slow corner (ideal=1.15)								
slow	1.17	1.17	1.18	1.16	1.17	1.17	1.16	1.16	1.17
typical	1.13	1.14	1.14	1.13	1.14	1.14	1.12	1.13	1.14
fast	1.10	1.11	1.11	1.09	1.10	1.11	1.09	1.10	1.10
MIM cap in typical corner (ideal=1)									
slow	1.03	1.04	1.04	1.02	1.03	1.04	1.00	1.03	1.04
typical	1.00	1.01	1.01	0.99	1.00	1.01	0.99	1.00	1.01
fast	0.97	0.98	0.99	0.97	0.98	0.98	0.96	0.97	0.98
MIM cap in fast corner (ideal=0.85)									
slow	0.89	0.90	0.91	0.89	0.90	0.90	0.88	0.89	0.90
typical	0.87	0.88	0.89	0.86	0.87	0.88	0.86	0.87	0.88
fast	0.84	0.85	0.86	0.84	0.85	0.86	0.83	0.84	0.86

Table 4 summarizes estimated values of MIM-capacitor through different corners, supply voltages and temperatures. Nine different combinations of temperature and supply voltage are considered- when all except C_{MIM} are in one corner, core corner, and C_{MIM} is in another, non-correlated corner. Estimation error is always smaller or equal to 6% (in 96.3% cases error is ≤5%).

3.4.2 Digital logic

Since the calibration process is being performed only once after power supply is applied, the speed and the low power consumption of the digital logic are not so important requirements. The area should be restricted, which is not a problem, due to low complexity and large level of integration of digital logic.

Block diagram of the digital logic is presented in Figure 11. The logic is synchronized with an external clock of 32 MHz.

Digital logic coordinates the oscillator running, determines the ratio of the oscillation frequencies and according to the ratio value, sets the control bits for the filter capacitor bank.

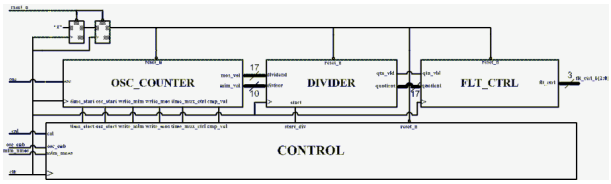


Figure 11: Digital network for generating filter control bits

External signal *reset_n* sets the initial state of the logic. All external signals are synchronized with the clock in order not to violate setup and hold times of used flip-flops, to avoid flip-flops to reach metastable state. Chosen oscillations that should be measured are presented at the input port *osc* of the digital network. Signal *cal* is external and it starts the calibration process again. Output signals *flt_ctrl_b[2:0]* control the switches in the filter adjustable capacitor bank.

Digital part of the design consists of the four main blocks described by Verilog code:

(1) *CONTROL BLOCK*, which is the core of the digital logic realized as the finite state machine, Figure 12;
(2) *OSC_COUNTER*, that counts oscillation in the predefined time period $T_{measure}$, equation (18);
(3) *DIVIDER*, which divides $COUNT_{MOS}$ and $COUNT_{MIM}$ equation (19);
(4) *FLT_CTRL* block, that generates filter control bits according to the division result.

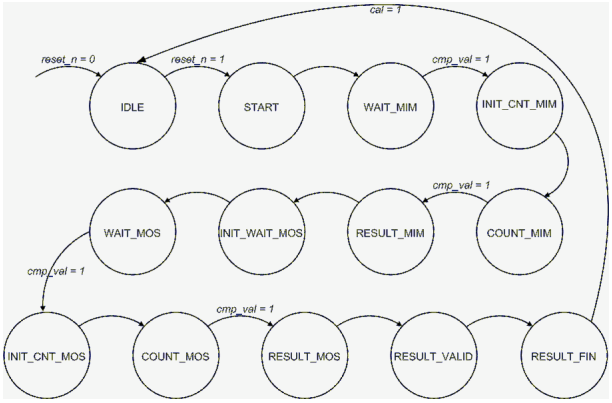


Figure 12: Control block- FSM (Finite State Machine)

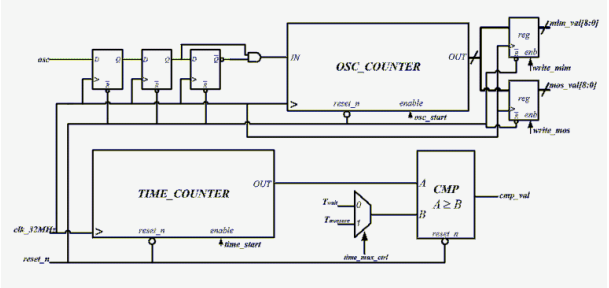


Figure 13: Counter of the oscillations and time counter

The listed digital blocks are described via Verilog code and are implemented in the silicon. Whole logic is implemented using 450 digital gates and takes the area of 114μm x 110μm. After synthesis and place-and-route, timing and functional checks were performed.

4 Experimental results- Measurements

The filter with its compensation capacitors, oscillator and digital network are designed and fully integrated. The layout of the whole design is presented in Figure 14. As it can be observed from the figure, the compensation capacitors are realized with multiple capacitors connected in series. This has been done due to the high minimal value of MIM capacitors in used technology. The effective area of the design is significantly smaller than the size of the entire chip. The reason for that and for layout aspect ratio is adjusting the design to available on-chip measurement equipment and integration of the test chip on the multi-project-wafer available area. It should be emphasized that, in order to have possibility of external calibration, an additional circuit is added. The circuit is composed of the three multiplexers controlled by signal *reset_n* which determines whether the calibration is internal or external. Also, shift register is implemented for writing three control bits via two external signals.

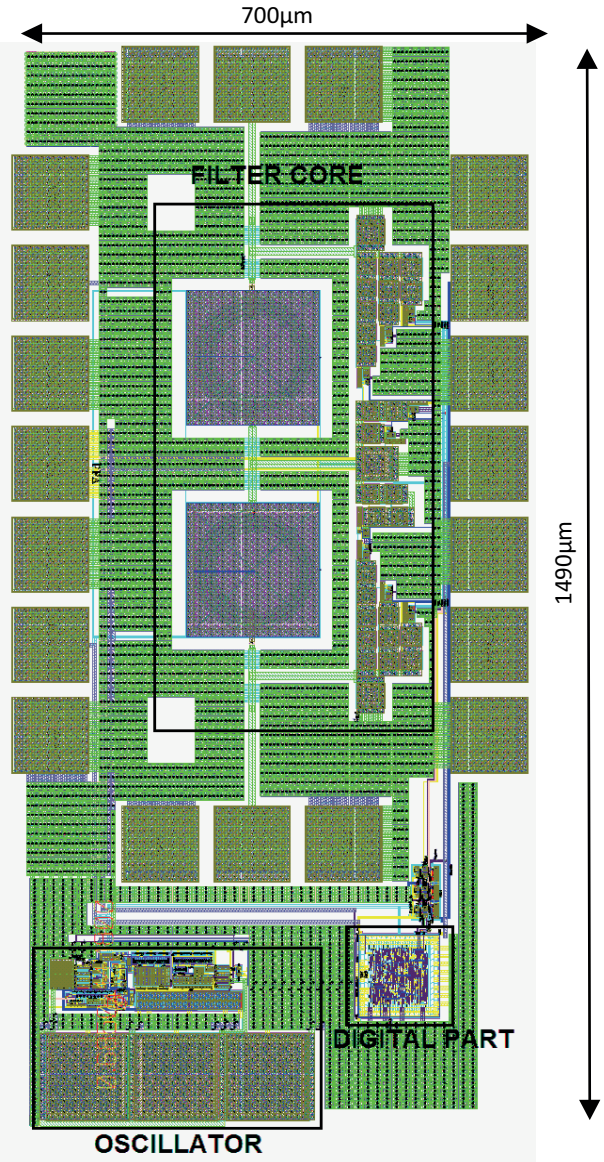
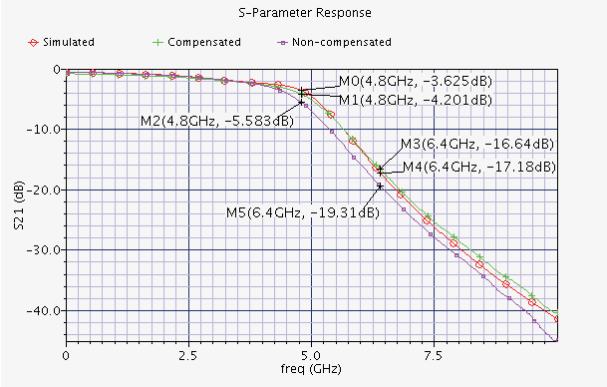


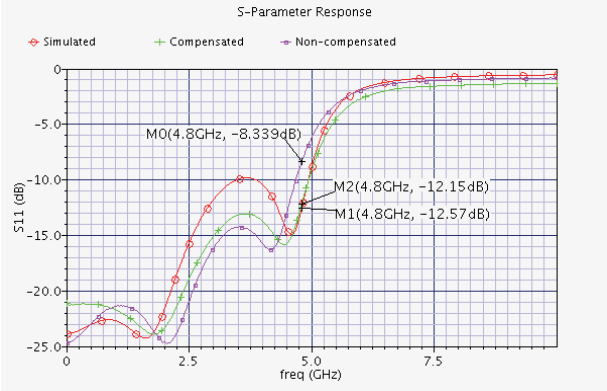
Figure 14: Integrated design- layout view

The Figure 15 shows the measurement results of the circuit using internal calibration procedure. Measurements are performed under nominal conditions - at the room temperature and nominal supply voltage. As it can be seen from the figure, the compensated filter transfer characteristic matches well with the simulated one - at the cutoff frequency the difference is 0.6 dB. Also, uncompensated filter characteristic is shown. In this case, control bits have random values. The difference between simulated and non-compensated case at cut-off frequency is unacceptable 2dB.

Figure 16 and Figure 17 present the photo of the IC die and the measurement set-up using the on-wafer probes.



a)



b)

Figure 15: Filter a) S21 and b) S11 parameters in compensated (green), simulated (red) and non-compensated case (purple)

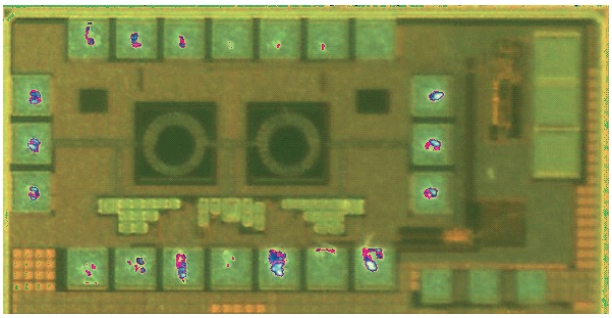


Figure 16: Die photo

5 Conclusion

This paper proposes one way of fully integrated on-chip calibration of MIM-capacitor process induced variation, utilizing more stable MOS capacitor as reference. The test circuit is designed and verified using standard 130 nm CMOS process. The concept is applied to low-pass filter design and is verified through simulations and measurements. After the calibration is applied, MIM capacitance variation is lowered from 15% to 8%.. Moreover, optimization of RF switches is proposed.

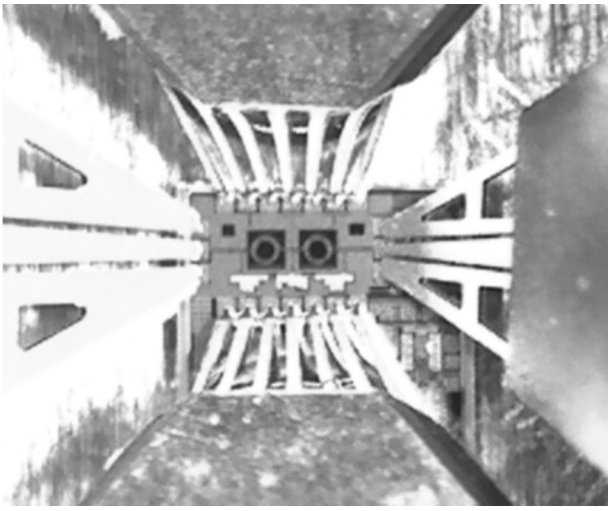


Figure 17: Die with probes

With adopted optimization, the switches increase filter insertion loss no more than 0.6 dB in "on" state, and introduce additional capacitor error below 2% when they are all "off".

The same method can be used for compensating the process variation in any other circuit type and in any other CMOS technology process.

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