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Impact of Downscaling on Analog/RF Performance of sub-100nm GS-DG MOSFET

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Abstract: This paper presents a systematic study to show the impact of channel length on the Analog/RF performances of gate stack (GS) silicon on insulator (SOI) architecture. The downscaling of channel length becomes the biggest challenge to maintain higher speed, low power and better electrostatic integrity for each generation. This investigation is done to find out the potential of the channel length in view of analog and RF performance measures of sub-100nm GS-double gate (DG) MOSFETs. The threshold voltage (V_{th}) is made constant by tuning the gate metal work function while downscale the channel length (L). The impact of channel length variation on subthreshold slope (SS), drain induced barrier lowering (DIBL), transconductance (g_m), output conductance (g_d), early voltage (V_{EA}), transconductance generation factor (TGF), intrinsic gain (A_V), cut-off frequency (f_T), transconductance frequency product (TFP), gain frequency product (GFP) and gain transconductance frequency product (GTFP) are rigorously examined. It is shown that gate stack design results in higher cut-off frequency along with a broader analog 'sweet spot' in nanoscale MOSFETs thus offering better possibilities for analog/RF scaling below 50nm. For shorter gate length devices (L=30nm), the design results in an impressive 69.10% improvement in f_T along with 36.31% enhancement in 'sweet spot' as compared to L=60 nm. The study generates an optimized channel length of L=40 nm for the designed device dimension in connection with the analog and RF performance for circuit design.

Keywords: Gate Stack (GS), DG-MOSFETs, Metal Gate Technology, Analog/RF FOMs, Sweet Spot

Vpliva pomanjševanja na analogne/RF lastnosti pod-100 nm GS-DG MOSFETa

Izvleček: V članku je predstavljana sistematična študija vpliva dolžine kanala na analogne RF lastnosti arhitekture večplastnih vrat (GS) silicija na izolatorju (SOI). Največji izziv pri krajšanju kanala je ohranjanje visoke hitrosti, nizke moči in boljše elektrostatične celote. Raziskava odkriva potenciale dolžine kanala pri analognih in RF lastnostih. MOSFET-ov z dvojnimi vrati. Konstantnost pragovne napetosti pri krajšanju kanala se je ohranjala s spreminjanjem delovne funkcije kovinskih vrat. Raziskan je vpliv krajšanja kanala na podpragovni naklon (SS), ponorno vzbujano nižanje bariere, transkonduktanco (g_m), izhodno prevodnost (g_d), zgodnjo napetost (V_{EA}), generacijski faktor transkonduktance (TGF), intrinsično ojačenje (A_V), frekvenco reza (f_T), produkt transconduktančne frekvence (TFP), produkt frekvence ojačenja (GFP) in produkt frekvenc ojačenja in transkonduktance (GTFP). Izkazalo se je, da večplastna vrata omogočajo višje frekvence reza skupaj s širšim območjem najboljšega delovanja v nanodimenzijskih MOSFET-ih, kar omogoča krčenje na 50 nm. Pri krajših dolžinah vrat (L=30nm) oblika izkazuje impresivno 69.10 % izboljšanje f_T in 36.31 % izboljšanje območja najboljšega izplena v primerjavi z L = 60 nm. Izkazalo se je, da je optimalna dolžina kanala 40 nm.

Ključne besede: večplastna vrata, DG-MOSFET, tehnologija kovinskih vrat, Analogni/RF FOM, območje najboljšega izplena

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1 Introduction

The use of low power and high frequency operated devices are having a high priority for future electronic applications. Silicon on Insulator (SOI) devices are excellent candidates as an alternative for the conventional bulk CMOS [1-2]. Advanced MOSFET structures such as ultra-thin body (UTB) SOI double gate (DG) MOSFET can be scaled more aggressively than bulk Si structure [3]. A double gate structure fabricated on SOI wafer has been utilized in CMOS technology due to their excellent scaling capability, outstanding Short Channel Effects (SCEs) immunity, high current drivability (I_{on}) and transconductance (g_m) and lower leakage current (I_{off}) as compared to the bulk MOSFETs [4-10]. Channel length scaling is limited by the ability to control off-

state leakage current due to quantum tunneling and thermionic emission between the source and drain.

The analog and RF circuits with a digital CMOS technology suffers from many challenges. More over the technology is optimized for digital design and the devices are characterized for current drive and gate delay. For System on Chip (SoC) and System in Package (SiP) applications, optimization of the devices becomes more challenging. SiP refers to a semiconductor device that incorporates multiple readily available chips into a single package; while SoC refers to a device that incorporates a system of differently functioning circuit blocks on a single silicon chip. So it is required to enhance the performance for digital and analog/RF circuit applications [11-18]. Major semiconductor companies such as IBM, RFMD, Honeywell, OKI, etc., have already produced several products for the telecommunication market based on SOI RF technologies.

In this work, a study has been made with designing different device cases by varying channel length (L) keeping all other process parameters constant for high-k/metal gate (HKMG) DG-MOSFETs. In our analysis, Analog/RF devices designed around the 'sweet spot' (compromise between power and speed performance, and linearity) signified by the peak of transconductance to current ratio (g_m/I_D) and cut-off frequency (f_T) product, typically characterized by a gate voltage of 0.35 V. The device performance is investigated keeping in view for analog and RF circuit application. For the analysis, the threshold voltage (V_{th}) is maintained at a constant value for all cases by tuning the gate metal work function between 4.6 eV to 4.7 eV. The V_{th} is achieved a constant value of 0.2V for all channel length device cases. Section 2 describes the device description that includes all the dimensions, materials and doping concentrations of HKMG DG-MOSFET. Section 3 analyses the physics of the device using device numerical simulations and models activated for simulation. In section 4, various performance metrics of the device including the short channel effects (SCEs) like SS, DIBL, and the important analog and RF FOMs such as g_m, g_d, TGF, V_{EA}, A_V, C_{gs}, C_{gd}, f_T, TFP, GFP, GTFP have been closely observed. Finally, the concluding remarks have been included in section 5.

2 Basic Structure

For the purpose of study a planar DG SOI n-channel transistor is considered. For the simulation a symmetric device structure model has been designed. Four different channel lengths (L= 60nm, 50nm, 40nm, and 30nm) are chosen for the device to analyze the device performance. The schematic simulated structure is shown in Fig. 1, where the silicon channel is surrounded above and below by two layer of oxide, SiO_2 and HfO_2. Metal gate technology is attractive because, it eliminates the poly-Si gate depletion effect and the associated degradation in transistor performance. To achieve a constant V_{th}, the work function of the metal gate is tuned in between 4.6 eV to 4.7 eV while varying the channel length of the device.The doping profile for channel (p-type 10^{16} cm^{-3}) and source, drain (n-type 10^{20} cm^{-3}) are set. For a better comparison of analog/RF FOMs, the V_{th} is maintained at a constant value 0.2 V while varying the metal gate work function at V_{DS}=0.1 V.

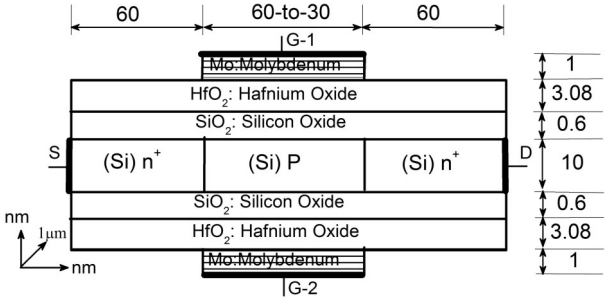


Figure 1: Schematic structure of Double Gate N-MOSFET

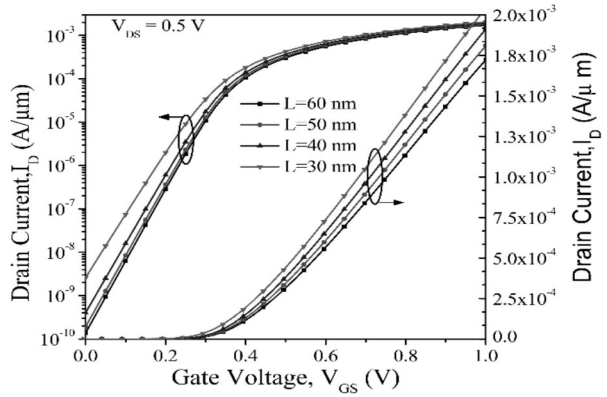
3 Device Simulation

The 2-D numerical device simulator ATLAS is employed to simulate the planner DG-MOSFET with high-k/metal gate. According to International Technology Roadmap for Semiconductors (ITRS), the drain bias has been fixed at V_{DD} = 1.0 V [19]. In order to study the analog performance, the simulation is performed with V_{DS} = 0.5 V (which is half of the supply voltage i.e., $V_{DD}/2$) [20-21] with variable V_{GS} = 0 V to 1.0 V. Threshold voltage (V_{th}) is extracted using constant current (I_D=10^{-6} A/μm) definition from the I_D-V_{GS} transfer characteristic at V_{DS}=0.1 V. The threshold voltage is used to find out the gate overdrive voltage (V_{GT}=V_{GS}-V_{th}). The gate over drive voltage is an important property of amplifier circuit as it decides the region of operation. The increment of V_{GT} increases drain current until saturation. Hence in our investigation all the analog and RF analysis has been done against V_{GT} [22- 23]. For more accuracy, it is essential to account for the mobility degradation inside the inversion layers. The degradation normally occurs as a result of higher surface scattering near the semiconductor to insulator interface. Hence, during simulation, the inversion-layer Lombardi constant voltage and temperature (CVT) mobility model has been considered. The Shockley–Read–Hall (SRH) generation and recombination parameters simulate the leakage currents existing due to thermal generation are incorporated in

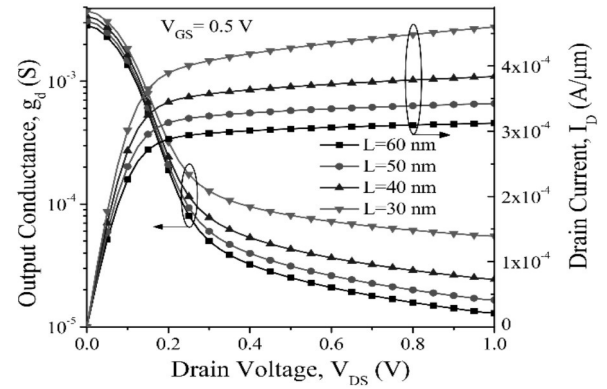
the simulation. At thermal equilibrium, a semiconductor lattice obeys Fermi-Dirac statistics. The use of Boltzmann statistics is normally justified in semiconductor device theory. However, Fermi-Dirac statistics are necessary to include for certain properties of very highly doped (degenerate) materials. The model Fermi-Dirac uses a Rational Chebyshev approximation that gives results close to the exact value. In the simulation all the junctions of the structure are considered to be of abrupt. Suitable empirical parameter β is selected to calibrate the drift diffusion transport model [20]. The biasing conditions are granted as per the room temperature T=25 °C. Furthermore, we have chosen two numerical techniques Gummel and Newton to obtain the solutions [24].

4 Results and Discussion

In order to analyze the impact of channel length of the device on the performance, simulation is done for four different channel lengths as 60 nm, 50 nm, 40 nm, and 30 nm.



(a)



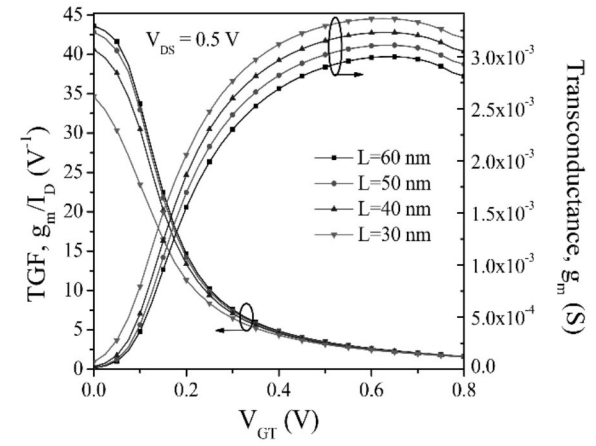
(b)

Figure 2: Drain current (I_D) in both linear and log scale as a function of gate to source voltage (V_{GS}) (b) Output conductance (g_d) and drain current (I_D) with respect to drain to source voltage (V_{DS}) for different channel lengths.

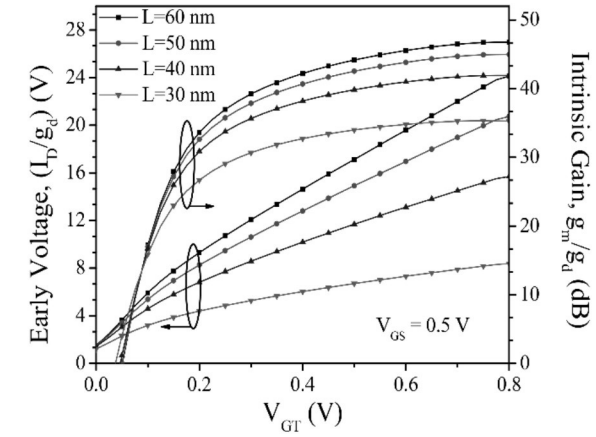
However, for analog and RF performance comparison among all the channel length cases, V_{th} kept constant (0.2 V) by adjusting the metal gate work function between 4.6 eV and 4.7 eV. The I_D-V_{GS} transfer characteristics both in linear and log scales have been shown in Fig. 2 (a) for different configurations at V_{DS}=0.5 V. The leakage current (I_{off}) is quit constant for three different channel length except L=30 nm. In the short channel device the I_{off} increases due to random motion of charge carriers. As channel length decreases, it gives rise to high drain current because of the relation $I_D \propto 1/L$. However, from the log scale, the leakage current is also prominent for lower channel lengths.Drain current (I_D) and output conductance (g_d) against drain to source voltage (V_{DS}) for different cases at V_{GS}=0.5 V are presented in Fig.2 (b). As per the Fig.2 (b), the drain current is increasing with decrease in channel length which in turn makes; the g_d high for lower L devices as $g_d=\partial I_D/\partial V_{DS}$. As we know from the literatures that gain and early voltage are inversely proportional to output conductance, so the device having lower L gives higher g_d which comprises lower gain and early voltage of the device.

Transconductance generation factor (TGF=g_m/I_D) and transconductance (g_m) as a function of gate over drive voltage ($V_{GT}=V_{GS}-V_{th}$) are presented in Fig.3 (a). From the figure, it is clear that as the channel length decreases the g_m value is increasing because of high drain current. The g_m/I_D ratio demonstrates how efficiently the current is used to achieve a certain value of transconductance. The advantage of high transconductance-to-drain ratio is the realization of circuits operating at low supply voltage. As shown in the figure, g_m/I_D is maximized towards the subthreshold region of device operation. From the Fig.3 (a), it is clear that the structure having channel length 60 nm shows higher g_m/I_D ratio as compare to others and it decreases as channel length decreases. Fig.3 (b) shows the variation of the early voltage (V_{EA}) and intrinsic gain (A_V) as a function of gate over drive voltage (V_{GT}) for different channel lengths. For better analog performance the V_{EA} and A_V should be as high as possible. An enormous improvement is observed in V_{EA} for channel length L=60 nm as compared to others.

The intrinsic gain of the device, which is a ratio of transconductance and output conductance for various channel lengths is plotted against gate voltage (V_{GS}) for V_{DS}=0.5 V is shown in Fig.3 (b). The intrinsic gain ($A_V=g_m/g_d$) is a valuable figure of merit for operational transconductance amplifier. From the figure, the device having channel length 60 nm gives highest gain from others and it decreases as the channel length decreases. Both the extracted values of SS and calculated values of DIBL for different channel lengths are tabulated in Table 1.



(a)



(b)

Figure 3: (a) Transconductance generation factor (TGF) and transconductance (g_m) (b) Early voltage (V_{EA}) and intrinsic gain (A_V) as a function of gate over drive voltage (V_{GT}) for different channel lengths.

The DIBL calculation is performed for V_{th} at V_{DS}=0.1 V and V_{DS}=1.0 V. From the table, it is clear that the SS value increases as channel length decreases and it is high for channel length 30 nm. Similarly, the DIBL value also increases as channel length decreases and it gives a maximum value for channel length of 30 nm. These two parameters are very important for short channel effects, which should be minimized. The maximum values for g_m, g_d, V_{EA}, A_V, TGF are also tabulated in Table 1. I_D increases for lower channel length devices which consequently increases g_m values for devices having lower value of L. However, because of high g_d, the V_{EA}, and A_V becomes lower as L decreases. Coming from L=60 nm to 30 nm, the DIBL and SS values are more prominent for lower channel length devices and also the TGF and Gain are decreases as L decreases.

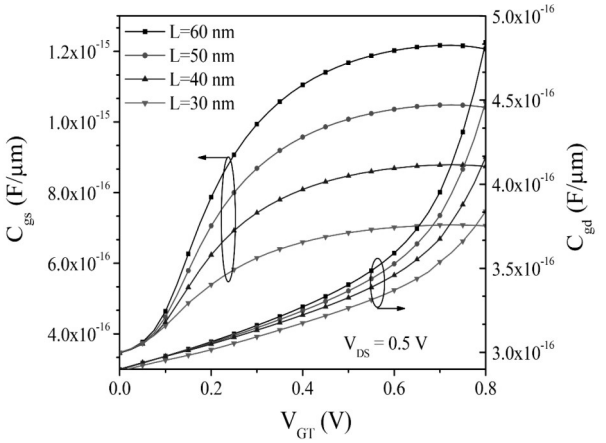


Figure 4: Gate to source capacitance (C_{gs}) and gate to drain capacitance (C_{gd}) as a function of gate over drive voltage (V_{GT}) for different channel lengths.

Fig. 4 shows the intrinsic capacitances (C_{gs} & C_{gd}) as a function of V_{GT}. As shown in figure, the intrinsic capacitance parameters increase swiftly in the super threshold region. This is because of the increase in the fringing field lines emanating from the gate edges. The device having channel length 60nm shows higher values of intrinsic capacitances (both C_{gs} & C_{gd}) and it decreases as channel length decreases. From Fig.5 (a), the variations of cut off frequency ($f_T=g_m/2\pi(C_{gs}+C_{gd})$) and gain transconductance frequency product ($GTFP=A_V*TGF*f_T$) can be observed with respect to V_{GT} for different values of channel lengths. Here, the value of f_T obtained for the device having low channel length is higher and it gradually decreases as the channel length decreases. f_T is inversely proportional to the intrinsic capacitances (C_{gs} & C_{gd}). So, f_T value is low due to high capacitance values for higher channel length devices. It is interesting to see that the device having

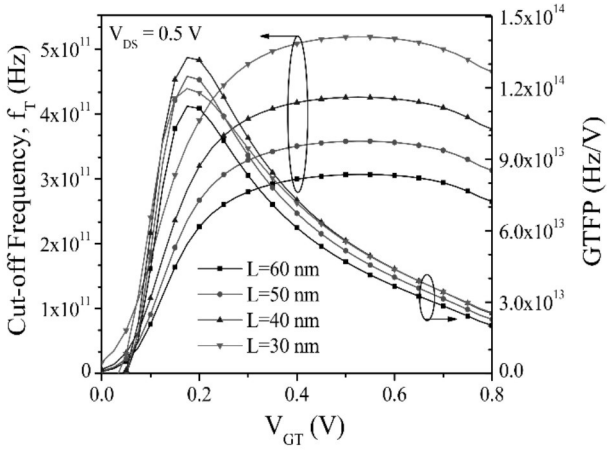
Table 1: Electrostatic & Analog performances for different values of channel lengths

Channel Length (nm)	DIBL (mV/V)	SS (mV/decade)	Transconductance, g_m (mS)	Output Conductance, g_d (μS)	Early Voltage, V_{EA} (V)	Gain, A_V (dB)	TGF (V^{-1})
		V_{DS}=0.5V					
L=60	20.71	62.31	2.81	12.94	24.130	46.742	43.637
L=50	21.12	63.12	2.93	16.57	20.737	44.969	42.840
L=40	37.24	65.95	3.05	24.53	15.787	41.921	40.639
L=30	49.88	68.35	3.18	54.84	8.499	35.458	34.669

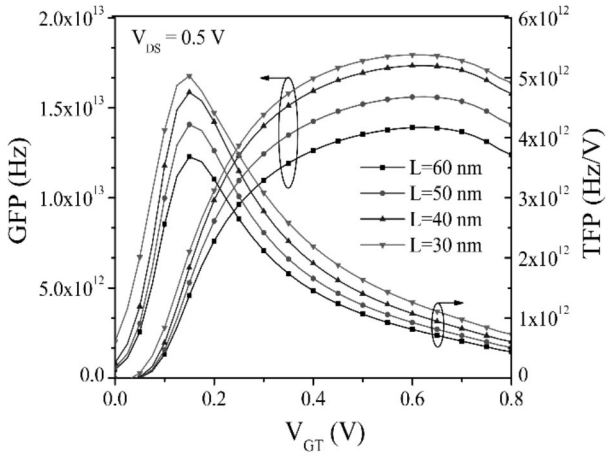
Table 2: RF performances for different values of channel lengths

Channel Length (nm)	C_{gs} (fF)	C_{gd} (fF)	f_t (GHz)	GFP (GHz)	TFP(GHz/V)	GTFP (GHz/V)
L=60	1.207	0.484	306.78	4.57*103	3.69*103	1.12*105
L=50	1.041	0.449	358.00	5.27*103	4.22*103	1.25*105
L=40	0.874	0.416	425.80	6.12*103	4.76*103	1.33*105
L=30	0.706	0.384	518.79	7.02*103	5.03*103	1.20*105

channel length L=40 nm shows a higher GTFP value as comparison to others. This is due to the reduction in peak electric field, lower output conductance of the device having channel length 40nm. The GTFP value is very low for L=30nm.



(a)



(b)

Figure 5: (a) Cut off frequency (f_T) and gain transconductance frequency product (GTFP) (b) Gain frequency product (GFP) and transconductance frequency product (TFP) as a function of gate over drive voltage (V_{GT}) for different channel lengths.

The product of g_m/I_D and f_T represents a trade-off between power and bandwidth and is utilized in moderate to high speed designs. Fig.5 (b) gives the gain frequency product ($GFP=A_V*f_T$) and TFP against gate over drive voltage (V_{GT}) for different values of channel lengths. From the figure, the value of GFP increases as channel length decreases and reaches utmost for the device having channel length 30nm. The same figure also shows transconductance frequency product (TFP) as a function of V_{GT} for different values of channel lengths. Where the bandwidth is flexible and part of the overall optimization process, it is important to consider the product of g_m/I_D and f_T as shown in Fig. 5 (b). This figure of merit exhibits a 'sweet spot' i.e., peak value for all device cases. Peak values for the product (TFP) increases from $3.69*10^3$ $GHzV^{-1}$ to $4.76*10^3$ $GHzV^{-1}$ when gate length (L) is reduced from 60nm to 30nm. The maximum values for TFP i.e., 'sweet point' is achieved at a gate voltage of 0.35 V which is 0.15 V more than from the threshold voltage. From the figure it is clear that the device having channel lengths 40nm and 30nm gives higher TFP values as comparison to others.

All the extracted values for analog/RF FOMs are plotted in Table 2 for different values of channel lengths. It is clear from the Table that, while the gate length is reduced the RF FOMs like f_T, GFP and TFP are also increased because of high drain current which results in higher g_m values for shorter gate length devices. However, the improvement in GTFP, which is a unique and major FOM, with L downscaling reduces below 40 nm due to short channel effects. From Table 1, the A_V values are obtained around 41.921 dB and 35.458 dB for 40nm and 30nm respectively whereas the g_m/I_D shifts lower to 34.669 V^{-1} for 30nm technology from 40.639 V^{-1} for 40nm technology. The GTFP is nothing but the product of three parameters i.e., TGF, gain and frequency, so the peak values are more for 40 nm technology as compare to 30 nm technology.

5 Conclusion

A detailed study on the analog/RF performance measure of GS-DG MOSFETs has been presented. It has been demonstrated that analog/RF performance metrics can be significantly enhanced by down scaling the channel length in terms of (a) analog 'sweet spot' and (b) compromise between gain and cut-off frequency i.e., GFP. However, the improvement in GTFP with L down scaling continues up till 40nm where a peak value of $1.33*10^5$ $GHzV^{-1}$ is attained. Beyond 40 nm, peak GTFP

value reduces to 1.20*10^5 $GHzV^{-1}$ in 30 nm GS-DG MOSFET due to short channel effects (peak g_m/I_D~34.669 V^{-1} and gain~35.458 dB, Table 1). So, from the results it is clear that all studied parameters are more sensitive to the channel length (L) of the device. The calculated and simulated results demonstrate that the optimized value of "L" will be 40 nm for the chosen device dimension. The values of the parameters like DIBL=37.24 mV/V, SS=65.95 mV/decade, I_{on}=1.912 mA, A_V=41.92 dB, f_T=425.80 GHz, GTFP=1.33*10^5 GHz/V are achieved for L=40 nm. The other device parameters could also be properly chosen for further downscaling of the transistor.

Due to lack of fabrication facilities, we can't validate our simulation results with the experimental results in literature. However, as our simulation is calibrated with experimental results, so we can give a formal assurance that degradation of studied parameters may not be expected when implementing MOSFETs in a real chip/ SoC.

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