DEVELOPMENT AND ANALYZIS OF FAST, POST-PROBE SILICON WAFER INKING ALGORITHMS

J. Trontelj Jr.

University of Ljubljana, Faculty of Electrical Enineering, Ljubljana, Slovenia

Key words: Wafer prober, inker, inking algorithm, wafer map.

Abstract: Wafer probing is essential process in the semiconductor manufacturing. While performing several electrical tests on chips within the silicon wafer, we can determine devices that don't comply with the predefined electrical parameters. Such devices are usually promptly marked with an ink dot. Sometimes inking can't be performed while testing. For example: when the inker presence disturbs sensitive sensors integrated on the tested device. For that purpose special algorithm for post-probe inking is required. Such algorithm is marking bad dies while reading error data from the wafer map file. Three different approaches for algorithms are presented to solve this problem.

Razvoj in analiza hitrih algoritmov za naknadno označevanje testiranja na silicijevih rezinah

Ključne besede: Testna naprava za silicijeve rezine, naprava za označevanje s črnilom, označevalni algoritem, grafična predstavitev napak na silicijevi rezini.

Izvleček: Končno testiranje silicijevih rezin je pomemben proces v izdelavi polprevodnikov. Tu s pomočjo elektronskega testiranja ugotavljamo količino dobrih čipov na rezini. Tiste mikrosisteme, ki ne ustrezajo vnaprej določenim kriterijem, pa običajno sproti označimo s kapljico črnila. Vendar pa to ni vedno mogoče. Včasih že sama naprava za označevanje s črnilom povzroči velike motnje na občutljivih senzorjih mikrosistemov. Torej potrebujemo poseben program za krmiljenje testne naprave za silicijeve rezine, ki omogoča naknadno označevanje s črnilom. Razvili smo tri različne algoritme za tak postopek.

1. Introduction

Wafer probing is important activity in the process of finalizing semiconductor products. The only way to find out, if a particular chip on silicon wafer is functional, is to perform several electrical tests. Such tests can be performed only after all wafer production steps are finished. However sometimes it happens, that measured electrical parameters are not within the predefined tolerances. When this is the case, bad device must be marked. Quite common approach for this task is to use a small drop of ink for the mark. The most convenient time for inking is a time bracket before moving wafer probe card to the next device. In some cases direct inking is not possible. Inking can only be performed after entire wafer probing is done. For that purpose we developed application specific algorithm for wafer prober control.

The device structures on the chip are getting smaller and smaller on the other hand, 200mm wafers are already standard. This means that we are usually testing several thousand chips per wafer. While optimizing time for the electrical measurements, the time necessary for applying probe card depends on the wafer prober speed and in general can't be optimized due to mechanical reasons. When the test time is short compared to the probe card move, several thousand moves use significant amount of time. Therefore it might happen, that inefficient post-probe inking algorithm actually doubles the test time per wafer.

Post-probe inking is mostly applicable when:

- Presence of the inker disturbs integrated sensors on tested device.
- Adopting multiple probe cards for simultaneous testing of several chips at the same time and there is no possibility to use several inkers.
- Delayed inking is not possible because probe card is preoccupied by test and measuring equipment.
- We are testing very little dies with several pads, which makes inker proper access to wafer surface impossible.

Therefore three different approaches for wafer inking algorithms are presented to solve listed problems and further implementations are proposed.

2. Description of the testing and inking process

Although wafer probing is an important step in the semiconductor production, it does not mean we should use a lot of time doing it. Therefore all wafer manipulation and electrical measurement routines should be optimized for speed. Since the electrical tests are the only way to find out, if certain chip on the silicon wafer is fully functional, we have to test all of them. Figure 1 presents test probe with inker.

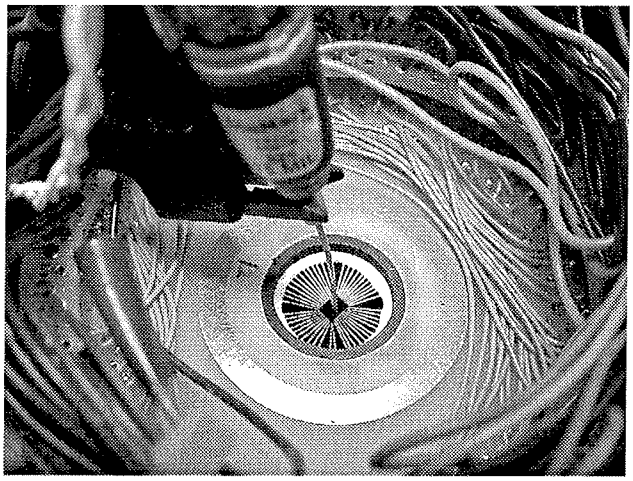

Figure1: Test probe with inker.

There are some methods to drastically increase testing speed. One is to test several chips at the same time. Drawback is, that we need very expensive test probes and several equivalent test stations. Due to high investment in expensive test stations economical aspect of this method is questionable. Another method is called consecutive fail monitoring. It is used to provide feedback information for determining problem areas. When they are determined we can test only the chips of the problem areas. However, such method is not very reliable and becomes quite unuseful, when additional trimming of chip parameters must be performed while testing.

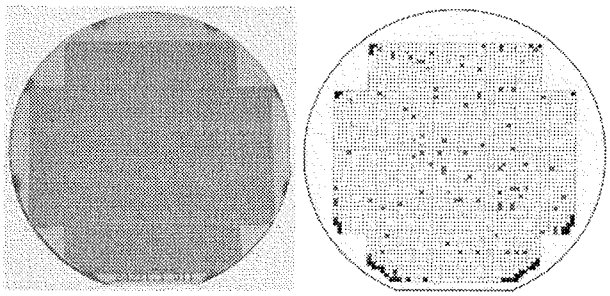

Figure 2: Silicon wafer and corresponding test wafer map.

Therefore it is reasonable to use simple, left to right and right to left test probe marching algorithm. It should be adopted to round shape and size of silicon wafers. Further it should also consider the pattern on the wafer (Figure 2). When we get to the end of the wafer, wafer test is completed and bad dies are inked. In case, when bad dies for some reason could not be inked directly we have three options:

- We can use a standard wafer map file for interface to the die-bonder. This method is called "inkless assembly". Drawback of this method is that it's not widely accepted as standard and that it has so called "first-die integrity" problem. It requires special marks on the wafer. These marks might be partially covered during wafer manufacturing and additional hardware and software is necessary to recognize such partially covered marks.
- We can use a special inking station outside the measuring wafer prober for offline inking, where the bad dies on the wafer are properly marked.
- We can use a standard wafer map file and slightly modified test probe marching algorithm with the same wafer prober setup data. This eliminates problems while matching physical locations on the wafer map file.

Last option can be used without any optimization. In this case, for N tested chips $2 \times N$ test positions must be selected per wafer. However, post-probe inking takes quite significant amount of time when chip test time becomes short, compared to time necessary for the test probe manipulation. And not at least, this method also significantly increases the mechanical wear of the expensive test equipment.

Usual yield per wafer varies from 60% to 90%. This fact offers some freedom for inking optimization since it is not necessary to ink every die on the wafer.

3. Inking process optimization

Inking process optimization is quite similar to the traveling salesman problem in which a salesman wishes to visit a number of cities and return to the starting point, while covering the minimum possible total distance on the way. Each city should be visited only once. If we represent testing algorithm from left to right and vice versa as a Hamiltonian graph (figure 3a), inking process might be introduced as a labeled spanning tree (Figure 3b). Vertices are presented as inked dies and we are trying to find an optimum spanning tree. Cayley's theorem says, that number of different labeled trees with n vertices is n^{n-2} and we usually have to ink a couple of hundred dies. However our problem is fortunately a little bit more specific.

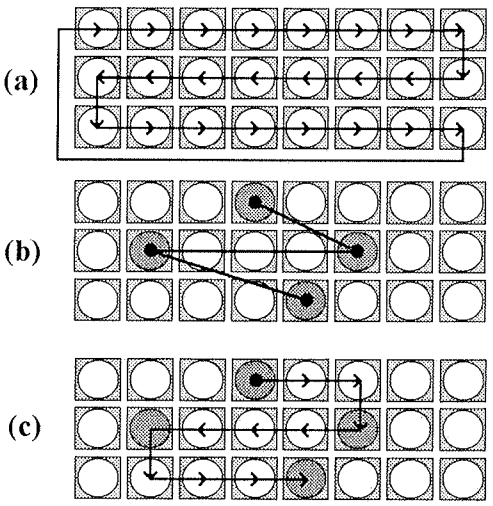

Figure 3: Wafer test probe marching description.

In other words, while inking we can actually decrease marching steps of the testing algorithm, by simply omitting some unnecessary traveling steps (figure 3c). Computer, that controls wafer prober input while inking, uses as input the same setup data as they are used for wafer prober while testing. The difference is, that optimized algorithm determines unnecessary marching steps and calculates appropriate offset moves to avoid unnecessary traveling. We will call this algorithm one pass inking optimization. In this case, time saving compared to $2 \times N$ marching algorithm, is considerable and compatibility with the marching algorithm for testing is preserved. This is, once again very important for achieving test and ink die integrity.

Figure 4 represents two typical wafer ink maps. Wafer ink map on the left actually represents best yield and wafer map on the right presents worst yield example. These two examples were chosen from several hundred tested wafers. We can see, that areas, requiring the most inking job are usually at the edge of the wafer. In the center of the silicon wafer, bad dies are more randomly distributed.

In worst yield case we can quickly realize, that our improved marching inking algorithm can't perform as well as in the best yield case. This is due to too many rows that need inking on the extreme left and right side. Therefore, the algorithm should be improved to perform better in such bad yield cases.

Adopting the feature, that areas requiring the most inking are actually on the edge of the wafer, we decided to ink the wafer in three phases. First phase is for inking dies on the left side, second on the middle and the third on the right side of the wafer. We will call this algorithm three passes inking optimization (figure 5).

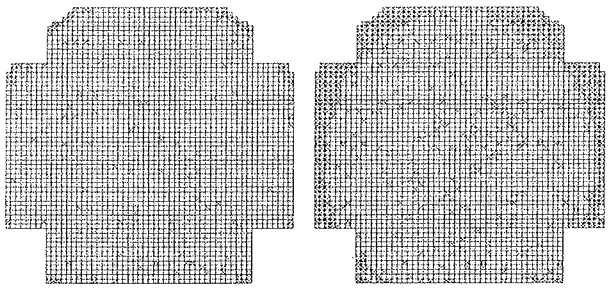

Figure 4: Best and worst-case inking wafer map.

Another problem that arises here is, how to efficiently group failed dies together? For that purpose we developed smart grouping and marking algorithms. Here we analyze three inking paths and use adoptable "near" and "far" functions. They are used to make a decision for grouping bad dies with questionable position. By questionable position we mean the position of all the dies that are geometrically between the two neighboring inking paths. It is quite evident, that when two dies are near each other, it is good to join them in the same group for post-probe inking. On the other hand, if two dies are far from each other, variable "far"

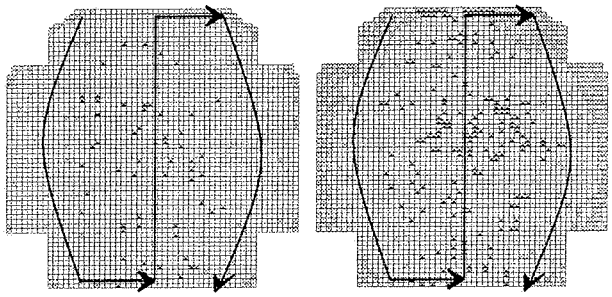

Figure 5: Best and worst-case inking wafer map for three passes inking algorithm.

actually represents our saved steps. "Near" and "far" parameters are variables, defined accordingly to the wafer size and number of dies to ink. This can be described with formulas (1), (2) and (3).

$$N = \frac{\pi r^2}{A} - \frac{2\pi r}{\sqrt{2A}} \quad (1)$$

$$N_b = (N * (1 - Y)) \quad (2)$$

$$Y = e^{-AD} \quad (3)$$

Where: N_b = number of dies to ink and N is number of dies per wafer,

$2r$ = wafer diameter,

Y = yield where A is die area and D is defect density.

Figure 5 presents such grouping for best and worst case yield from figure 4. Three different groups can be distinguished by different grayscales and different die patterns. The main direction of inker traveling is also indicated. Inker actually travels in steps left or right of main direction.

Both optimized inking algorithms are derived from wafer prober test setup files. Computer that controls wafer prober while inking uses HPIB communication protocol for test probe traveling and inker firing. However both algorithms were extensively tested for matching physical positions on wafer.

4. Inking process optimization evaluation

By using three passes inking algorithm we have additionally decreased extensive X marching for up to 66% in the best case. This algorithm is also efficient in previously mentioned worst-case condition, where we decreased inking time for 37%. Figure 6 presents timing diagrams for best and worst case times for all three inking algorithms. It is assumed, that worst-case $2 \times N$ inking algorithm takes 100% of time to finish.

The drawback is additional Y marching. However, additional Y steps are quickly annihilated by extensively decreased X

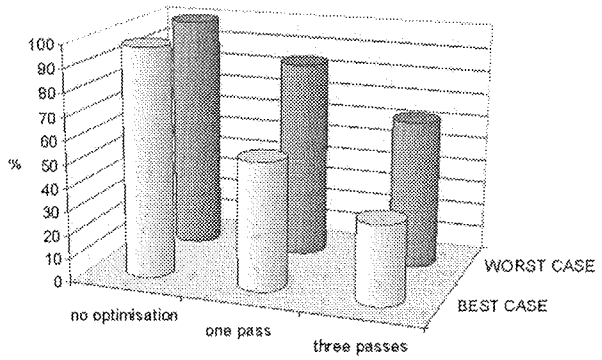

Figure 6: Timing diagram for all three different inking algorithms.

traveling. From mechanical wear of the wafer prober point of view, such algorithm is also much more convenient. This is because most of the job while testing and inking does the X-control machinery. So it's a good idea to increase load on the Y-control machinery while decreasing the load on the X-control machinery.

5. Conclusion

Post-probe inking of not functional chips is time consuming and increases maintenance cost of the expensive equipment. Therefore the effort for inkles testing is reasonable. Some test labs are already using wafer maps instead of ink drops for input to the die-bonders. Unfortunately this approach is probably several years away, to be a widely accepted standard.

There are approximately 20,000 wafer probers in the use worldwide. It is common, that almost every wafer prober has a different method for generating setup files, marking and marching algorithms. So, for achieving very important first-die integrity, old-fashioned inking is still quite common.

When inking for some reason can't be done promptly while testing, it is quite reasonable to use optimized wafer inking routines. When using three passes inking algorithm we can save up to 66% of inking time compared to $2 \times N$ inking algorithm. Beside faster wafer testing time we can also significantly decrease mechanical load on the expensive test equipment. As the wafer sizes grow, we may recommend further improvement to this algorithm by increasing the number of inking passes.

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dr. Janez Trontelj Jr.
Laboratory for Microelectronics, University of Ljubljana, Tržaška 25, SI 1000, Ljubljana, Slovenia
e-mail: jani@kalvarija.fe.uni-lj.si

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