UDK 621.3:(53+54+621+66)(05)(497.1)=00 ISSN 0352-9045

INFORMACIJE MIDEM 1·2004

Strokovno društvo za mikroelektroniko elektronske sestavne dele in materiale

Strokovna revija za mikroelektroniko, elektronske sestavne dele in materiale
Journal of Microelectronics, Electronic Components and Materials

INFORMACIJE MIDEM, LETNIK 34, ŠT. 1(109), LJUBLJANA, marec 2004

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INFORMACIJE MIDEM VOLUME 34, NO. 1(109), LJUBLJANA, MARCH 2004

Revija izhaja trimesečno (marec, junij, september, december). Izdaja strokovno društvo za mikroelektroniko, elektronske sestavne dele in materiale - MIDEM.
Published quarterly (march, june, september, december) by Society for Microelectronics, Electronic Components and Materials - MIDEM.

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Letna naročnina znaša 12.000,00 SIT, cena posamezne številke je 3000,00 SIT. Člani in sponzorji MIDEM prejemajo Informacije MIDEM brezplačno.
Annual subscription rate is EUR 100, separate issue is EUR 25. MIDEM members and Society sponsors receive Informacije MIDEM for free.

Znanstveni svet za tehnične vede I je podal pozitivno mnenje o reviji kot znanstveno strokovni reviji za mikroelektroniko, elektronske sestavne dele in materiale. Izdajo revije sofinanci rajo Ministrstvo za znanost in tehnologijo in sponzorji društva.
Scientific Council for Technical Sciences of Slovene Ministry of Science and Technology has recognized Informacije MIDEM as scientific Journal for microelectronics, electronic components and materials.
Publishing of the Journal is financed by Slovene Ministry of Science and Technology and by Society sponsors.

Znanstveno strokovne prispevke objavljene v Informacijah MIDEM zajemamo v podatkovne baze COBISS in INSPEC.

Prispevke iz revije zajema ISI® v naslednje svoje produkte: Sci Search®, Research Alert® in Materials Science Citation Index™

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The Journal is indexed by ISI® for Sci Search®, Research Alert® and Material Science Citation Index™

Po mnenju Ministrstva za informiranje št.23/300-92 šteje glasilo Informacije MIDEM med proizvode informativnega značaja.

Grafična priprava in tisk
Printed by
BIRO M, Ljubljana

Naklada
Circulation
1000 izvodov
1000 issues

Poštnina plačana pri pošti 1102 Ljubljana
Slovenia Taxe Percue

UDK621.3:(53+54+621+66), ISSN0352-9045 Informacije MIDEM 34(2004)1, Ljubljana

VSEBINA CONTENT

Obnovitev članstva v strokovnem društvu MIDEM in iz tega izhajajoče ugodnosti in obveznosti

Spoštovani,

V svojem več desetletij dolgem obstoju in delovanju smo si prizadevali narediti društvo privlačno in koristno vsem članom.Z delovanjem društva ste se srečali tudi vi in se odločili, da se v društvo včlanite. Življenske poti, zaposlitev in strokovno zanimanje pa se z leti spreminjajo, najrazličnejši dogodki, izzivi in odločitve so vas morda usmerili v povsem druga področja in vaš interes za delovanje ali članstvo v društvu se je z leti močno spremenil, morda izginil. Morda pa vas aktivnosti društva kljub temu še vedno zanimajo, če ne drugače, kot spomin na prijetne čase, ki smo jih skupaj preživeli. Spremenili so se tudi naslovi in način komuniciranja.

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MIDEM pri MIKROIKS

Stegne 11

1521 Ljubljana

Ljubljana, april 2003

Izvršilni odbor društva

NEW MnZn FERRITES AND THEIR APPLICATIONS

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Key words: magnetic ceramic, MnZn ferrites, magnetic properties, electrical properties, microstructures, applications

Abstract: MnZn ferrites, ceramic with special magnetic properties, are widely used as core materials for inductive components in electronics. The demands of future electronic systems require solutions that improve efficiency, reduce weight and not add pollution to the environment. The requirements for component design are a smaller size, weight reduction, performance increase and durability. This paper describes the applications and properties of new designed matireals12Gi, 27G, 55G, 75G and 65G.

Novi MnZn feriti in njihove aplikacije

Kjučne besede: magnetna keramika, MnZn feriti, magnetne lastnosti, električne lastnosti, mikrostruktura, aplikacije

Izvleček: MnZn feriti so keramični materiali z magnetnimi lastnostmi in sestavni deli induktivnih komponent namenjeni različnim aplikacijam v elektroniki. Trendi na področju elektronske industrije so usmerjeni v zmanjšanje teže osnovnih kompoment in izboljšanju osnovnih magnetnih lastnosti. Zahteve po zmanjšanju teže in prostornine novih induktivnih komponent narekujejo boljše lastnosti osnovnih materialov in večjo trajnost. V članku so predstavljene lastnosti novih materialov 12Gi, 27G, 55G, 75G in 65G ter njihova uporaba.

1. Introduction

Several improved materials will be discussed. It is important to select materials that are suited to specific applications. Some materials with their properties are listed:

1. EMI applications require a current compensated chokes which are very important to eliminate the disturbing interference sources. A ferrite material with a high initial permeability, high impedance over a broad frequency range and high operating temperature is required.
2. Splitter applications in ADSL applications required a plain old telephone system (POTS) splitter used to separate the high frequency data from low frequency voice signals. The core material must have a high reversible permeability at high magnetic field. In addition, a lower number of turns and smaller cores are required. This behavior can be achieved by high initial permeability and high saturation of the ferrite materials.
3. As electronic modules become smaller and lighter, the power supplies must likewise be reduced. The core losses, consisting of hysteresis losses, eddy current losses and residual losses, vary considerably with operating frequency and magnetic flux density. The losses can be reduced by a uniform microstructure and high material resistivity. But low mechanical stress, low magneto crystalline anisotropy and low magnetostriction are also required.
4. DSL applications require a fast data transfer without distortion. Inductive components are used in the customer^x^s premises modem and central office line transformers to realize a distortion free digital signal transmission along the copper wire of the conventional telephone network. The main target for the inductive cores is a long reach (higher than 5 km) at a high data distance.

2. Ferrite technology

The first step is the production of granulated ferrite powder. The weighed raw materials iron oxide, manganese oxide and zinc oxide are mixed and then palletized with a small amount of water. The red pellets with a pellet size of 3-5 mm are calcinated in a rotary kiln at about 1000^{0}C. Here the oxides react partly to the magnetic ferrite with spinel structure. After that the black pellets, water and some inorganic additives (amount from 0.01 - 0.1wt%) are added into an attritor for fine milling. The inorganic additives are necessary to improve the sintering behavior and/or the magnetic properties. The second part of the technology important to improve properties in associated with core shapes, sintering of them in the temperature range 1200 - 1400^{0}C and grinding of final cores.

3. Design principles

The performance of ferrites is not determined only by a high initial permeability. Other characteristics such as low losses, high saturation flux density, high sintered density and frequency characteristics are also important. In many cases, these requirements are not satisfied at the same time, so a compromise material has to be selected in such cases.

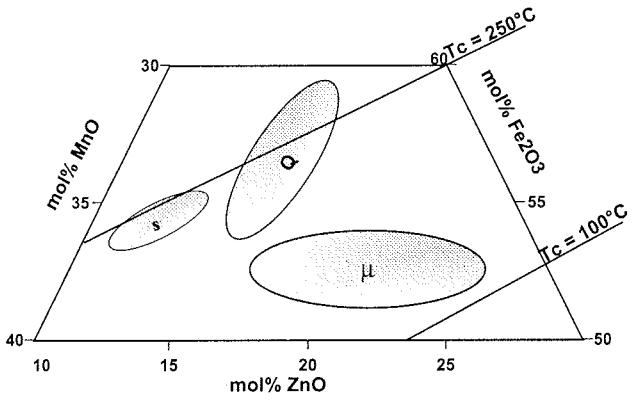

Fig. 1: Composition diagram for MnZn ferrites

The high initial permeability of materials depends to a large extent on the mobility of the Bloch's domain walls. To obtain high permeability it is important to lower the anisotropy and the magnetostriction. During the development of high-permeability MnZn ferrites much effort was devoted to the parameters which govern the bulk properties such as composition, microstructure and porosity /1/. To achieve a high permeability the composition of MnZn ferrite must be selected from a relatively narrow composition range, figure 1, region μ, where a zero crystalline anisotropy and a zero average magnetostriction can be expected. Studies of the grain-boundary chemistry in combination with grain-boundary structural analysis revealed that the grain boundaries are characterized by ZnO evaporation and the presence of a glassy phase and the segregation of various cations /2/. Firing conditions and additives are also important for achieving good properties. Well-adjusted sintering conditions support the development of the proper microstructure and the resulting magnetic properties. All these points have to be optimized in order to obtain desired magnetic properties.

Ferrites for power applications must be compositionally batched, figure 1 B_{sat} region, and processed for low losses. Low power loss MnZn ferrites should have uniformly sized grains and high saturation density. The use of additives, a well-controlled process and a suitable sintering profile must be selected to decrease the power loss of ferrites. Additives and impurities are responsible for the grain-boundary chemistry and have a remarkable effect on the grain boundaries properties, particularly on the grain-boundary resistance /3/. In order to obtain a sintered body of uniformly sized fine grains, which would be suitable for achieving low power losses, grain growth should be suppressed especially in the initial stage of sintering process /4,6/. The selection of high-grade raw materials, with a defined low level of impurities, is of special importance in the production of MnZn ferrites for optimized microstructure properties. Addition of Ca and Si are well known to control the micro structural properties. Both ions strongly influence the microstructure of MnZn ferrites. Furthermore, the total resistance of MnZn ferrites increases due to the precipitation of silicate phases at the grain boundaries. This has the advantage that CaO and SiO_2 are doped in a defined amount in the ferrite mixture and their effect can be optimized in order to control the grain size and resistivity. In addition to the concentration of impurities, the reactivity of raw materials is a fundamental importance to control and optimize the production process /5/.

The total usable flux, AC + DC, in single ended power supplies is becoming important. The usable flux of a ferrite material is closely connected with the saturation flux density B_s, which in turn depends on the composition and density of the ferrite. For practical purposes, the composition of a ferrite material has to be considered as a compromise between application temperature (the position of the secondary permeability maximum corresponding to the position of minimum core losses) and required saturation flux density (which falls as temperature rises). Detailed investigation of core loss mechanisms has made it possible to develop new ferrite materials for various applications.

High saturation power ferrite 55G

55G is intended for output chokes in power supplies. The requirement of a high saturation level to accommodate a high dc current is necessary to avoid saturating the core. The energy storage value of a choke is proportional to the square of peak flux density and determines the core volume required. Whenever space is limited, this is an important consideration. The new Iskra Feriti material 55G is usable to 500 kHz and above /8/.

***Table 1:** 55G Material characteristics*

Parameter	*measuring conditions*	*value*
μ_i []	25 °C, 10 kHz, 0.1 mT	1800 ± 20%
B_S [mT]	25 °C, 10 kHz, 1200 A/m	≥ 510
	100 °C, 10 kHz, 1200 A/m	≥ 430
	120 °C, 10 kHz, 1200 A/m	≥ 400
T_c [°C]		≥ 240

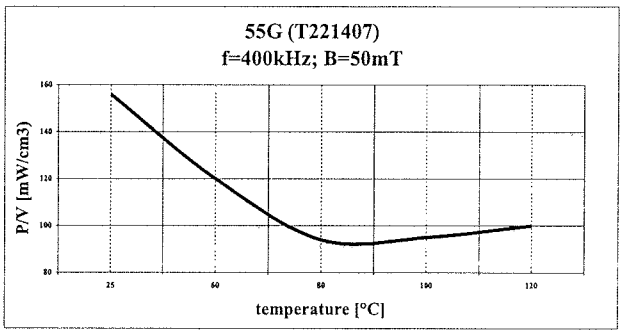

Fig. 2: Power losses versus temperature

Preferred applications are:

- High current output chokes - wherever space is at premium like a low profile converter modules, core volume can be reduced. The advantage increases with temperature.

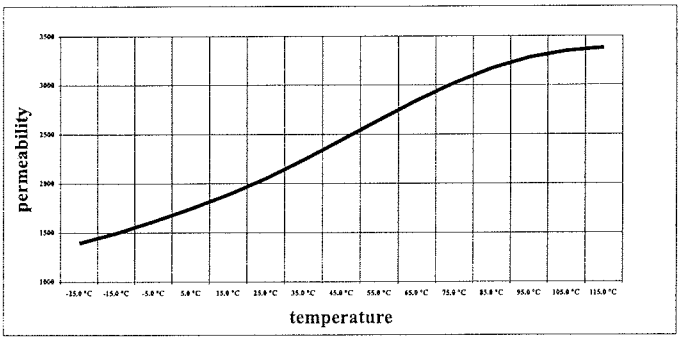

Fig.3: Initial permeability versus temperature

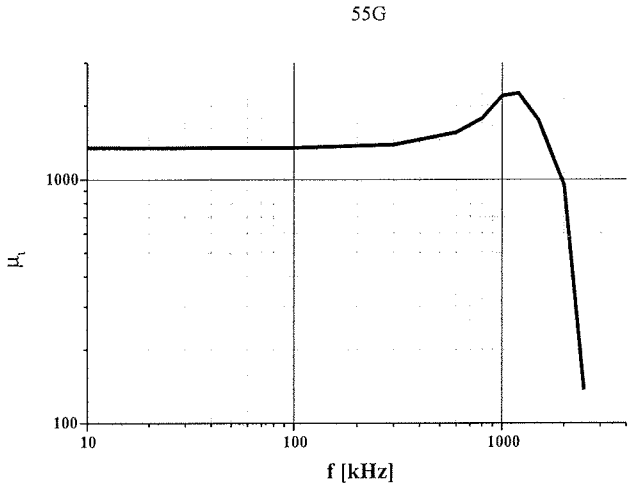

Fig. 4: Initial permeability versus frequency

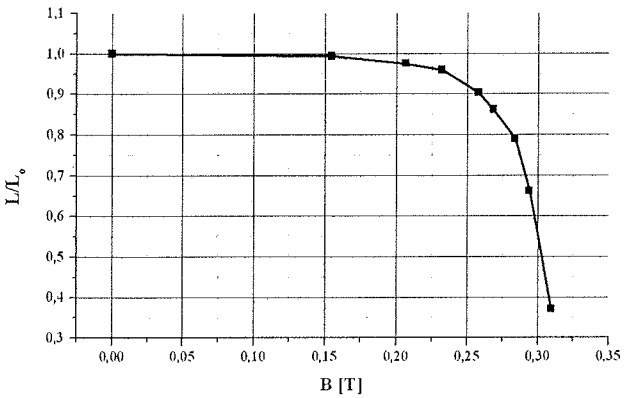

Fig. 5: Inductance as function of B_{pmax} at 120°C

- High voltage ignition transformers - for example in electronic lighting ballast where high flux density occurs during ignition, but losses have to be low during steady state operation.
- Gapped toroids where high-energy storage is required.

High frequency power ferrite 75G

The increase in electrical applications for the automotive market is stressing the 12 volt system. The way to solve the insufficient electrical power is to increase the 12V standard to a 42V standard. The additional requirement to reduce weight and change to a drive by wire concept opens the market for voltage converters. The operating frequency of these converters will be about 500 Hz to 1MHz. The right material is a high frequency power grade, like our 75G, Table2 and Figures 6 to 9. The ferrite components that will be needed for various applications could use 2 planar core sets, one for transformer and one for the output choke for the core solution.

***Table 2:** 75G Material characteristics*

Parameter	*measuring conditions*	*value*
μ_i []	25 °C, 10 kHz, 0.1 mT	1300 ± 20%
B_S [mT]	25 °C, 10 kHz, 1200 A/m	≥ 510
	100 °C, 10 kHz, 1200 A/m	≥ 430
	120 °C, 10 kHz, 1200 A/m	≥ 400
T_c [°C]		≥ 240

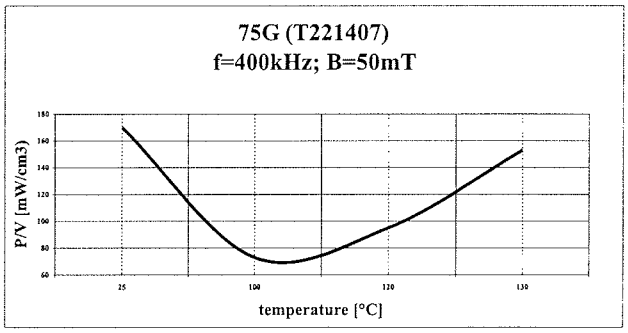

Fig. 6: Power loss versus temperature

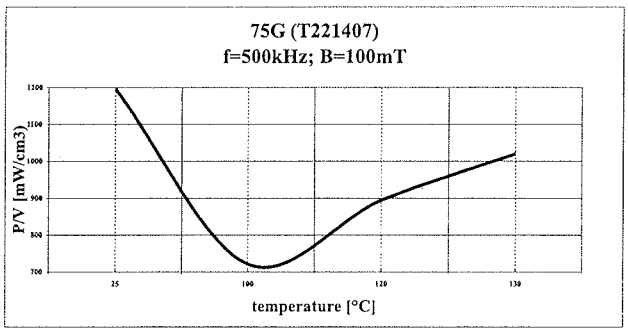

Fig. 7: Power loss versus temperature

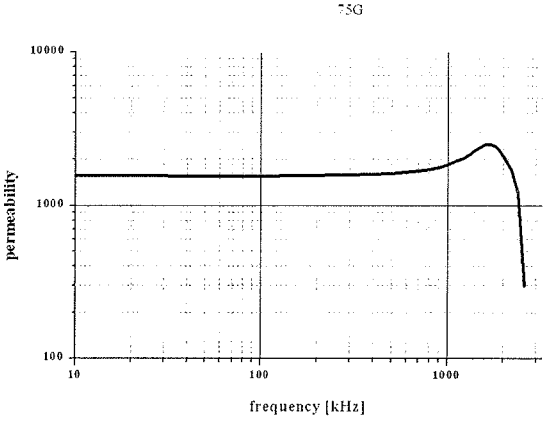

Fig. 8: Initial permeability versus frequency

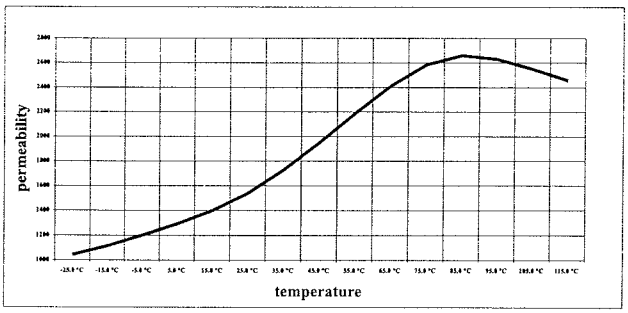

Fig. 9: Initial permeability versus temperature

Some potential applications under the 42V system are:

- Lighter, smaller and more efficient air conditioning
- Higher efficiency, longer life, water pump
- Faster starter, superior charging starter/alternator
- Mobile office: fax, PC,....

Power material 65G – new level of power density

The properties of 65G, a new high flux density power material suitable for frequency up to 400 kHz is shown in Table 3 and Figures 10 to 13. This material is primarily intended for output chokes in power supplies where a high saturation level is required to accommodate DC + AC currents at elevated temperatures. The energy storage volume of a choke is proportional to the square of peak flux density and determines the core volume required. When space is limited, this is an important consideration.

Table 3: *65G Material characteristics*

Parameter	*measuring conditions*	*value*
μ_i []	25 °C, 10 kHz, 0.1 mT	2300 ± 20%
B_S [mT]	25 °C, 10 kHz, 1200 A/m	≥ 510
	100 °C, 10 kHz, 1200 A/m	≥ 380
	120 °C, 10 kHz, 1200 A/m	≥ 360
T_c [°C]		≥ 210 °C

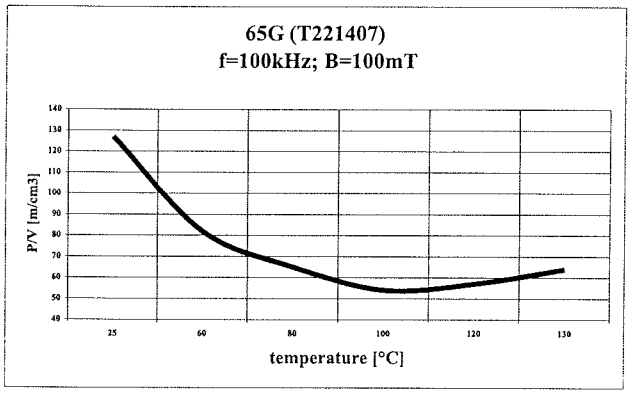

Fig. 10: Power losses versus temperature

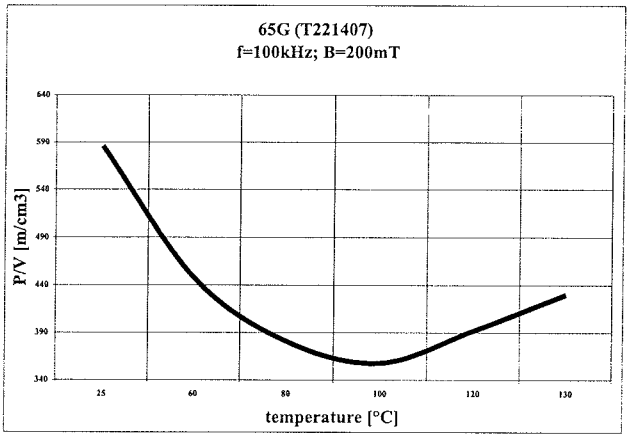

Fig. 11: Power losses versus temperature

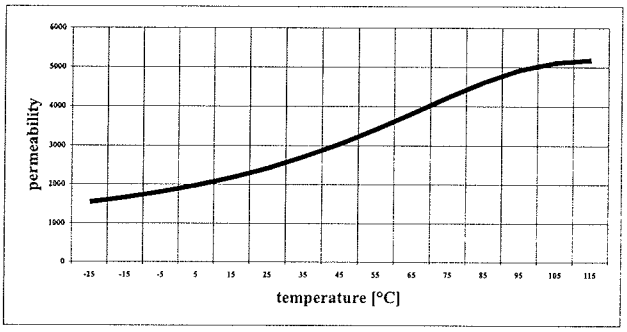

Fig. 12: Permeability versus temperature

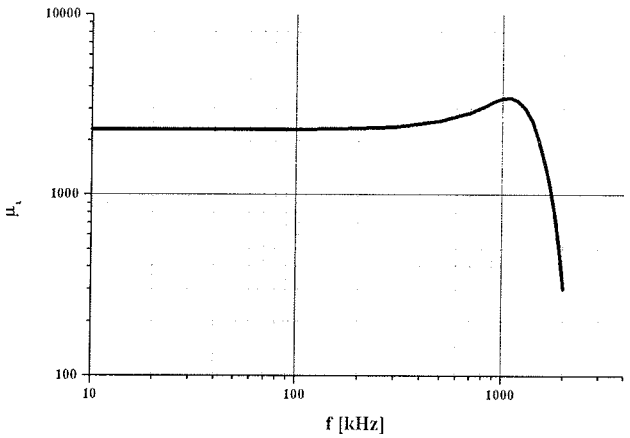

Fig. 13: Permeability versus frequency

Some potential applications are automotive electronics and electronic lighting ballasts.

Innovative material 12Gi for (A) XDSL interface transformers

The ferrite producer Iskra- Feriti has developed an improved 12i ferrite material optimized for (A) XDSL applications. In comparison with conventional 12G ferrite material, the new 12Gi, Table 4 and Figures 14 and 15, allows for increases in the data rate transfer and distance covered by (A)XDSL lines.

The THD, Total Harmonic Distortion, of a ferrite component should be low under operating conditions. THD is a function of flux density (B), frequency (f) and temperature (T). To evaluate the material quality with respect to THD an audio analyzer was used on toroid samples. The improved 12Gi is optimized by low impurity raw materials, the addition of additives and improved processing and sintering conditions.

Table 4: *12Gi Material characteristics*

Parameter	*measuring conditions*	*value*
μ_i []	10 kHz, 25 °C, 0.1 mT	10000 ± 20%
η_B [10^{-3}/T]	10 kHz, 25 °C, 1.5-3.0 mT	< 0.15
tgδ/μi [10-6]	10 kHz, 25 °C, 0.1 mT	≤ 7
	100 kHz, 25 °C, 0.1 mT	≤ 40
αF [106/K]	25 - 55 °C	-1 -+ 1
TC [°C]		≥ 130

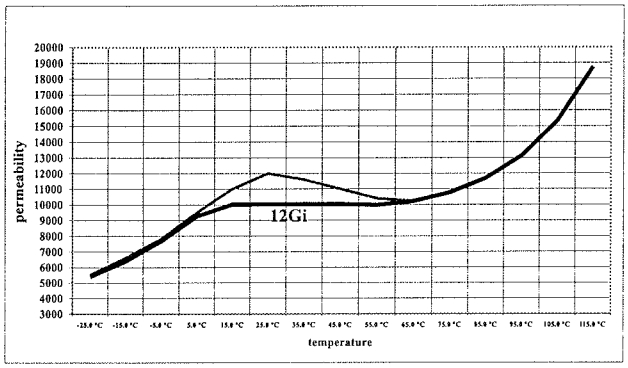

Fig. 14: Permeability versus temperature

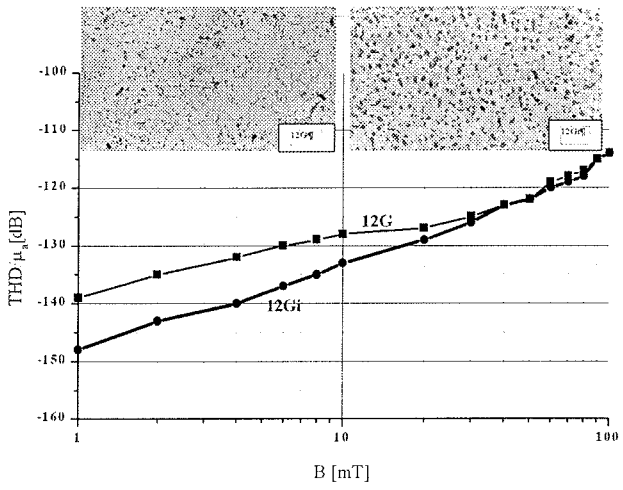

Fig.15: THD/μ_a versus B for 12G and new 12Gi at 20 kHz

New material 27G for splitter applications

27G material, Table 5 and Figures 16 to 18, replaces 25G material in splitter (POTS) applications. 27G material is the first MnZn-ferrite which is available in production and combines both a high permeability and high saturation,. Both the high permeability and the high saturation at room temperature lead to the improvement of the DC-bias behavior.

This innovative material will also be of interest for interference suppression in automotive electronics and in frequency converters for industrial applications.

Typical industrial applications are found in pumps, fans, conveyer belt drivers, textile machinery and printing presses.

Suppression of this interferences is now a statutory requirement and calls for filters that can cope with high power outputs. The high power outputs inevitably cause high operating and ambient temperatures. The filters therefore require ferrite materials with high initial permeability and high magnetic saturation. The new 27G material is particularly suitable for these extreme requirements.

Table 5: *27G Material characteristics*

Parameter	*measuring conditions*	*value*
μ_i []	25 °C, 10 kHz, 0.1 mT	3800 ± 20%
B_S [mT]	25 °C, 10 kHz, 1200 A/m	≥ 530
	100 °C, 10 kHz, 1200 A/m	≥ 410
	120 °C, 10 kHz, 1200 A/m	≥ 370
T_c [°C]		≥ 210

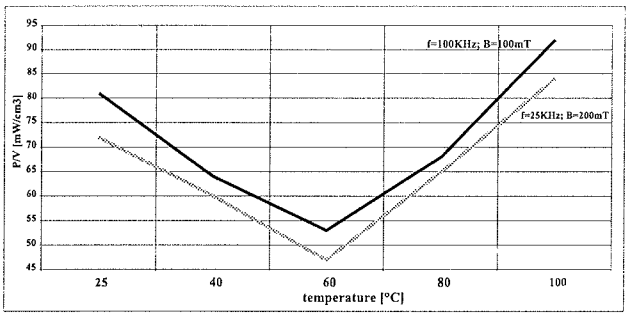

Fig. 16: Power loss versus temperature

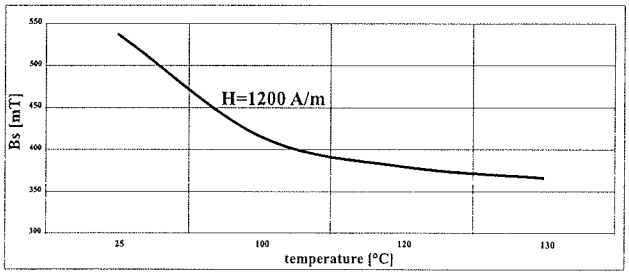

Fig. 17: Saturation flux density versus temperature

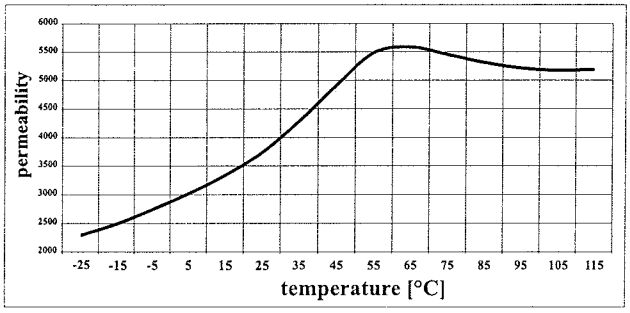

Fig. 18: Permeability versus temperature

All materials were successfully introduced on production and available in different core shapes.

3. Conclusion

The technical demand for improved soft ferrites has been growing. The technical department at Iskra - Feriti, has been busy developing and improving new ferrites to meet these demands. These materials meet the demands in both quantity and applications requirements that demand improved performance. Raw materials, the improvements in manufacturing technology and the ability to measure the results, play a decisive role in improving the quality and lowering the costs of ferrites. The results of these developments are expected to give new impulses for electrotechnical applications.

4. References

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Prispelo (Arrived): 11.12.2003 *Sprejeto (Accepted): 25.02.2004*

THE INTERACIONS OF CONDUCTIVE AND GLASS PHASE IN THICK-FILM RESISTORS DURING FIRING

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Key words: thick-film resistors, characterisation, ruthenium oxide, ruthenates, phase equilibria

Abstract: Some thick-film resistors based on RuO_2, ruthenates or a mixture of RuO_2 and ruthenates, were evaluated. The resistors were fired at different temperatures to determine the influence of firing temperature on the electrical and microstructural characteristics. The microstructures of the thick-film resistors were analysed with scanning electron microscopy and energy-dispersive X-ray analysis. The temperature coefficients of resistivity, noise indices and gauge factors were measured as a function of firing temperature. After a long term high temperature firing ruthenate based conductive phase transform into RuO_2 coinciding with a significant increase of the temperature coefficients of resistivity and decrease of the resistance. Glass phase in thick-film resistors was analysed by EDS. All glass compositions are rich in SiO_2 with the molar ratio SiO_2 / PbO between 2 and 2.5. Subsolidus equilibria in the RuO_2 - PbO - SiO_2 diagram were determined with the aim to verify the interactions between conductive phase (either ruthenium oxide or ruthenate) and silica-rich glasses. The tie line between RuO_2 and $PbSiO_3$ indicates that the lead ruthenats are not stable in the presence of the silica-rich glass phase.

Interakcije med prevodno in stekleno fazo v debeloplastnih uporih med procesom žganja

Kjučne besede: debeloplastni upori, karakterizacija, rutenijev oksid, rutenati, fazni diagrami

Izvleček: Karakterizirali smo nekatere debeloplastne uporovne materiale na osnovi RuO_2, rutenatov ali zmesi RuO_2 in rutenatov. Uporte smo žgali pri različnih temperaturah, da bi ugotovili vpliv temperature žganja na električne in mikrostrukturne karakteristike. Mikrostrukture debeloplastnih uporov so bile preiskane z elektronskim vrstičnim mikroskopom in rentgensko analizo. Izmerili smo temperaturne koeficiente upornosti, indekse tokovnega šuma in faktorje gauge v odvisnosti od temperature žganja. Ugotovili smo, da v debeloplastnih uporih, žganih dolgo časa pri povišanih temperaturah, rutenat preide v rutenijev oksid. Pri tem se zelo zniža plastna upornost in poviša temperaturni koeficient upornosti. Stekleno fazo v debeloplastnih uporih smo analizirali z EDS (Energy Disspersive X-ray Analysis). Ugotovili smo, da so vsa stekla bogata na SiO_2 z razmerjem SiO_2 / PbO med 2 in 2,5. Preiskali smo fazna ravnotežja v sistemu RuO_2 - SiO_2 - PbO. Rezultati so potrdili, da rutenat ni stabilen v prisotnosti stekel bogatih na SiO_2.

Introduction

Thick-film resistors consist basically of a conducting phase, a lead-borosilicate-based glass phase and an organic vehicle. The organic material is burned out during the high-temperature processing. The ratio between the conductive and the glass phases roughly determines the specific resistivity of the resistor. In most modern resistor compositions the conductive phase is either RuO_2 or ruthenates; mainly, as reported in the literature, lead or bismuth ruthenates. The main change during firing is the transition from a mixture of glass grains and, usually, much finer grains of the conductive phase in a thick-film paste, into conductive chains through the sintered glass in the fired resistor. During the firing cycle all the constituents of the resistor paste react with each other and the melted glass also interacts with the substrate The resistors are only a relatively short time (typically 10 min) at the highest temperature (typically 850°C). Because of this the reactions between the constituents of the resistor material do not reach equilibrium so that the required characteristics of fired materials (e.g long-term stability, low noise indices and a low temperature coefficient of resistivity) are, in a way, a compromise as a consequence of this frozen non-equilibrium /1-5/. The aim of this paper is to present the results on some thick film resistor material, fired either at the required 850°C for 10 min or at higher firing temperatures for significantly longer times. The aim was to gain some insight into the changes in the electrical and microstructural characteristics, and gauge factors if the resistors are fired long enough at the high temperature to allow the reactions within the resistor to reach the equilibrium. Thick-film resistors with a nominal resistivity of 10 kohm/sq. (Du Pont 8039 and 2041, and Heraeus 8241) were evaluated. The conductive phase in 8039, 2041 and 8241 resistors is based on $(Bi_{2-x}Pb_x)Ru_2O_{7-x/4}$, a mixture of RuO_2 and $Pb_2Ru_2O_{6.5}$, and RuO_2, respectively /6,7/. Data on the conductive phase and the qualitative results of an energy-dispersive X-ray analysis (EDS) of the glass composition of the thick-film resistors are summarized in Table 1. All glasses contain, as main elements, lead, silicon and aluminum oxides. Boron oxide, which is also present in the glass phase, cannot be detected in the EDS spectra because of the low relative boron weight fraction in the glass and the strong

absorption of the boron K_α line during EDS analysis in the glass matrix.

Table 1. Conductive phase and qualitative results of EDS microanalysis of elements detected in glass phase of thick-film resistors /17/.

Resistor	Conductive phase	Ma in elements	Other elements detected
8039	ruthenate	Si, Pb, Al	Zr
2041	RuO 2+ ruthenate	Si, Pb, Al	Mg, Zn, Ca, Ba
8241	RuO 2	Si, Pb, Al	Zn, Cu

The X-ray analysis of conductive phase in investigated thick film resistors will be given. The change of conductive phase (from ruthenate to the ruthenium oxide) at high firing temperatures, depending on the composition of glass phase will be discussed.

Experimental

Thick-film resistors with dimensions 1.6x1.6 mm^2 were printed on 96% alumina substrates and fired for10 min at 850°C and for 6 hours at 950°C. The resistors were terminated with a Pd/Ag conductor that was prefired at 850°C. Cold TCRs (from -25°C to 25°C) and hot TCRs (from 25°C to 125°C) were calculated from resistivity measurements at - 25°C, 25°C, and 125°C. Current noise was measured in dB on 100 mW loaded resistors by the Quan Tech method (Quan Tech Model 315-C). Gauge factors (GFs) were measured. The resistors were examined by X-ray powder-diffraction (XRD) analysis A JEOL JSM 5800 scanning electron microscope (SEM) equipped with an energy-dispersive X-ray analyser (EDS) was used for the microstructural analysis.

Results and discussion

Sheet resistivities, cold (-25°C to 25°C) and hot (25°C to 125°C) TCRs, noise indices and gauge factors of the investigated thick-film resistors that were 10 min at 850°C and 6 hours at 950°C are shown in Table 2.

After firing at 950°C for 6 hours, the resistivities of all the resistors significantly decreased to around 5% of the resistivities after firing at 850°C for the 2041 resistors, and to 1% or less for the 8039 and 8241 resistors. The GFs of all the resistors, as well as the sheet resistivities, decreased with increasing firing temperature. The TCR values of the resistors after firing at the "normal" temperature of 850°C are below $100x10^{-6}/K$. After firing for 6 hours at 950°C the absolute values of the TCRs of the 8039 and 8241 resistors increased significantly. The noise indices decrease with increased firing temperature. The 2041 resistor material has the lowest noise, around or under -20 dB, regardless of the firing temperature.

X-ray diffraction (XRD) spectra of ruthenate-based "equilibrated" resistors showed that at higher firing temperatures the ruthenate decomposes forming RuO_2, while the conductive phase in RuO_2-based resistors stays unchanged. This is shown in Figs. 1.a, 1.b and 1.c for 10 kohm/sq. Du Pont 8039 and 2041 thick film resistors, and Heraeus 8241 thick-film resistors, respectively /6/. As mentioned before, the 8241 resistor is based on RuO_2 and the 2041 material is based on a mixture of (mainly) ruthenate and RuO_2. The resistors were fired for 10 min at 850°C and for 6 hours at 950°C. After 6 hours of firing at 950°C the ruthenate peaks of the 8039 resistors disappear while the spectrum of RuO_2 based 8241 resistors remains unchanged. Presumably because of the interaction with the molten glass the ruthenate decomposes.

The decomposition of the ruthenate phase in the ruthenate-based 8039 resistor after high-temperature firing and the formation of RuO_2 was confirmed with SEM. Microstructures of the 8039 resistors that were fired for 10 min at 850°C and for 6 hours at 950°C are as an example in Figs. 2.a and 2.b. The microstructure of the 8039 resistor, fired at 850°C (Fig. 3.a) consists of light sub micrometer-sized particles of a conductive phase in a grey glass matrix. The dark particles are $SiZrO_4$. After 6 hours firing

Table 1: Sheet resistivities, cold and hot TCRs, noise indices and gauge factors of the thick-film resistors, fired 10 min at 850°C and 6 hours at 950°C

Resistor	T firing (°C)	Resistivity (ohm/sq.)	Cold TCR (10-6/K)	Hot TCR (10-6/K)	Noise (dB)	GF
8039	850	7,3 k	50	90	-14.3	11.0
	950, 6 h	37	1845	1810	-29.9	1.5
2041	850	6.6 k	-35	20	-23.3	11.0
	950, 6 h	280	-90	-85	-32.0	7.0
8241	850	5.4 k	20	60	-4.5	15.5
	950, 6 h	36	1950	1990	-25.5	2.0

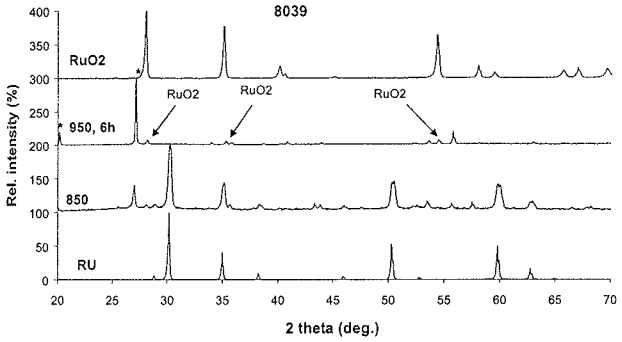

Fig. 1a: XRD spectra of 2039 thick-film resistor, fired for 10 min at 850°C and for 6 hours at 950°C. Spectra of ruthenate (RU) and of RuO_2 (RuO2) are also included.

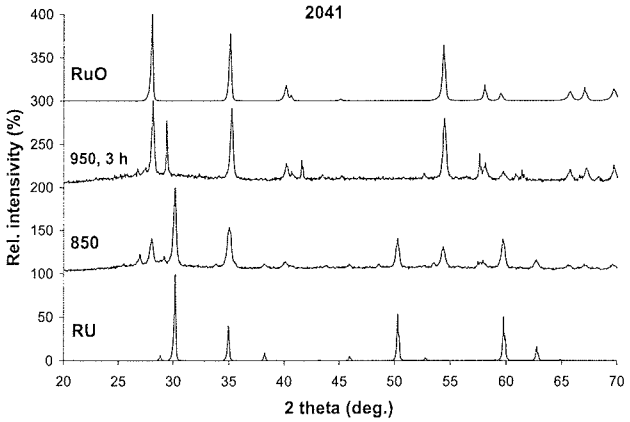

Fig. 1b: XRD spectra of 2041 thick-film resistor, fired for 10 min at 850°C and for 6 hours at 950°C. Spectra of ruthenate (RU) and of RuO_2 (RuO_2) are also included.

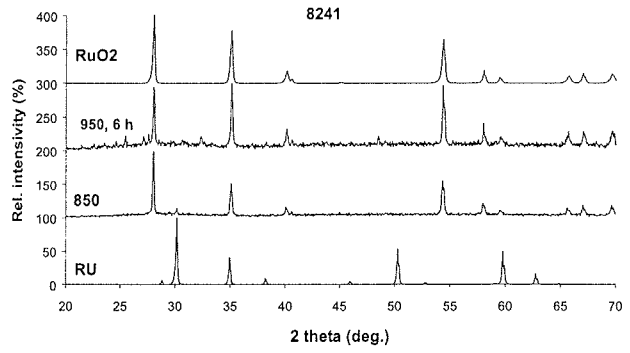

Fig. 1c: XRD spectra of 8541 thick-film resistor, fired for 10 min at 850°C and for 6 hours at 950°C. Spectra of ruthenate (RU) and of RuO_2 (RuO2) are also included.

at 950°C the ruthenate particles in the 8039 resistor have nearly all disappeared.

Adachi and Kuno /8,9/ studied high-temperature interactions between $PbO-B_2O_3-SiO_2$ glasses and $Pb_2Ru_2O_{6.5}$

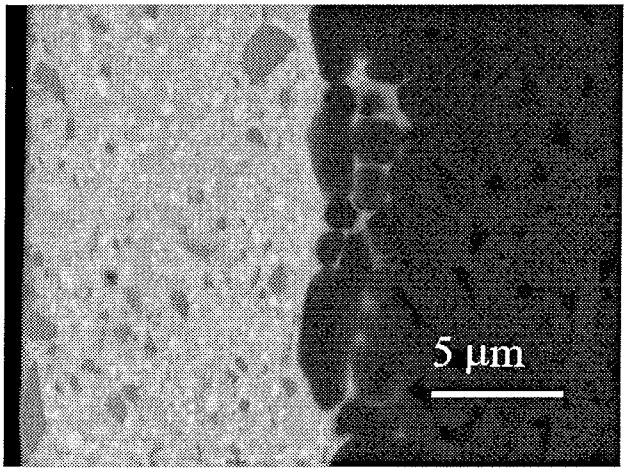

Fig.2a: Microstructure of a cross-section of the thick-film resistor 8039, fired for 10 min at 850°C. Alumina substrate is on the right. Light particles are conductive phase - $(Bi_{2-x}Pb_x)Ru_2O_{7-x/4}$.

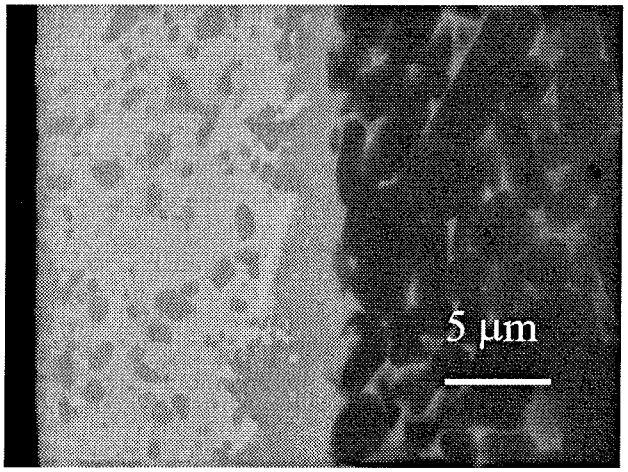

Fig. 2b: Microstructure of a cross-section of the thick-film resistor 8039, fired for 6 hours at 950°C. Alumina substrate is on the right. After firing at 950°C the ruthenate particles in the 8039 resistor have nearly all disappeared.

or RuO_2. They showed that in glasses poor in PbO the $Pb_2Ru_2O_{6.5}$ disappears and the RuO_2 is formed while for PbO-rich glasses the RuO_2 reacts with the PbO from the glass and forms $Pb_2Ru_2O_{6.5}$. Their results are summarised in Fig. 3. Three regions are marked in the $PbO-B_2O_3-SiO_2$ phase diagram. In the first region in the silica rich part of diagram ruthenates decomposes into RuO_2. In third region (PbO rich) ruthenates are stable while RuO_2 reacts with glass forming $Pb_2Ru_2O_{6.5}$. In glasses with roughly 1/1 SiO_2 / PbO ratio (second region) the RuO_2 and the ruthenate coexist.

To confirm these findings, the subsolidus ternary phase diagram of the RuO_2 - PbO - SiO_2.system was investigated. The glass phase in different commercial thick-film resistors was analysed by SEM and the PbO/SiO_2 ratio was

determined. All analysed glass compositions are rich in SiO_2 with the molar ratio SiO_2 / PbO between 2 and 2.5. The molar ratio SiO_2 / PbO in glass phases of thick-film resistors is also graphically shown as a short bold bar near SiO_2 in the PbO-poor part of the RuO_2 - PbO - SiO_2 system in Fig. 4. The PbO-rich part of phase diagram, which was not investigated, is shown with dotted lines. No ternary compound was found in the system. There is no binary compound between RuO_2 and SiO_2. The tie lines are between $Pb_2Ru_2O_{6.5}$ and $PbSiO_3$, and between RuO_2 and $PbSiO_3$. The results therefore indicate that the lead-ruthenate-based conductive phase in thick-film resistors is indeed unstable when in contact with the silica-rich glass phase, as shown by dashed lines in Fig. 4.

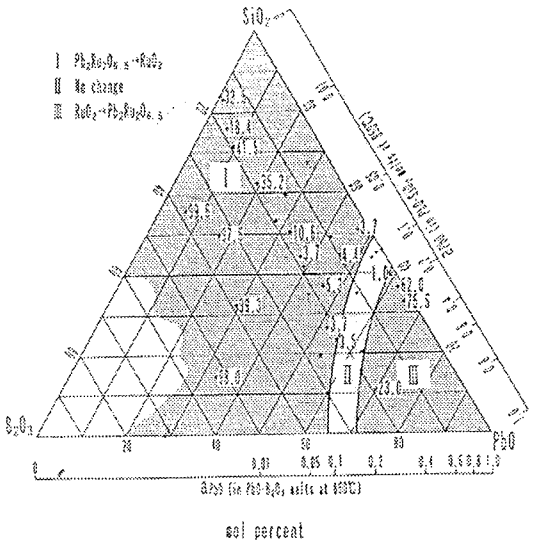

Fig. 3: The PbO-B_2O_3-SiO_2 system (after Adachi and Kuno /8/). Lead ruthenate is stable in the region III and unstable in the region I.

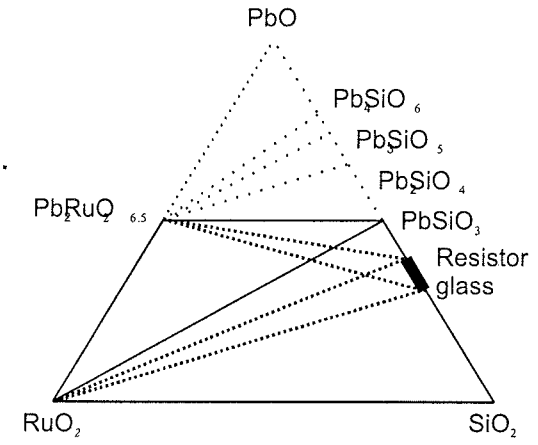

Fig. 4: The proposed subsolidus ternary phase diagram of the PbO-poor part of the RuO_2 - PbO - SiO_2. The molar ratio SiO_2 / PbO in glass phases of some thick-film resistors is shown as a short bold bar near SiO_2 in the PbO-SiO_2 system.

Acknowledgement

The financial support of the Ministry of Education, Science and Sport of the Republic of Slovenia is gratefully acknowledged.

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Prispelo (Arrived): 21.07.2003 *Sprejeto (Accepted):25.02.2004*

PROBLEM NEPONOVLJIVOSTI SIMULACIJ ELEKTRIČNIH VEZIJ

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Kjučne besede: simulatorji električnih vezij, benchmark testiranje, neponovljivost rezultatov, kaotična vezja, Chujev oscilator, nepravilnost.

Izvleček: Najkvalitetnejši simulatorji SPICE, kljub svoji relativni zrelosti, zmeraj ne zagotavljajo pravilnih rezultatov, na kar opozarjajo številni znanstveni prispevki /1/, /2/, /3/, /4/, /5/, /6/, /7/.

Naš prispevek opozarja na še eno kritično nepravilnost omenjenih simulatorjev - neponovljivost rezultatov simulacij. Ugotovili smo, da se lahko ta pojavi, kadar simuliramo vezje z istim simulatorjem, inštaliranim na platformah z različnimi procesorji. Zaradi tega je smiselno preveriti, ali današnji simulatorji zagotavljajo ponovljivost rezultatov in kvantitativno ovrednotiti njihovo morebitno neponovljivost. V ta namen smo predlagali primerno testno vezje in tri stopenjsko metriko za ocenjevanje neponovljivosti, ki jo je mogoče uporabiti tudi pri ocenjevanju kakovosti simulatorjev.

Problem of Non-repeatability of the Circuits Simulation

Key words: circuit simulators, benchmark testing, non-repeatability of results, chaotic circuits, Chua's oscillator, anomaly.

Abstract: SPICE circuit simulators are indispensable tools for integrated circuits design and for variety of scientific research activities. In spite of their mature age this simulators can give erroneous results /1/, /2/, /3/, /4/, /5/, /6/, /7/.

If we repeat the simulation on a different computer with the same simulator it is expected that results will not differ significantly. This property is called repeatability. There are a variety of situations where repeatability could be a problem. Repeated simulation can be performed with the same simulator on the same type of a computer, or with a different simulator on the same or on a different type of a computer, or with the same simulator installed on a different computer. We have focused on repeatability testing of different SPICE simulators installed on different platforms running transient analysis.

If the repeatability is not assured it is reasonable to evaluate the non-repeatability. Since deviations can occur between reference and repeated results in different ways, we have proposed three different non-repeatability measures. First order non-repeatability measure is used for the evaluation of time value deviations of time-domain waveforms. Second order non-repeatability measure evaluates dissimilarities of time-domain waveforms, and third order measure evaluates the deviation of global circuit behavior. To address this problem a functional testing of simulators were used.

Testing simulators with circuits of CircuitSim90 benchmark suite did not expose any repeatability problems. We have discovered that chaotic circuits are more efficient for the detection of non-repeatability because they are hypersensitive to the initial conditions. Chua's oscillator was selected as a representative member of chaotic circuits.

We have found out that some simulators did not ensure repeatability of results if they have been installed on different platforms. It was also discovered that the non-repeatability was most frequent if simulators were installed on the platforms with processors made by different manufactures. The consequences of non-repeatability were: significant time value deviations of time-domain waveforms and dissimilarities of their form. The type of processors however does not have significant influence on the circuit's global behavior.

The reasons for this anomaly and possibilities of its elimination were also addressed. The reason could be one or more errors in simulator's code or in the compiler, which allows different interpretations of the same processor instructions on different types of processors.

1. Uvod

Najkvalitetnejši simulator električnih vezij, ki se uporablja v industriji, različnih znanstveno-raziskovalnih in izobraževalnih institucijah, je simulator SPICE (Simulation Program with Integrated Circuit Emphasis). Njegovo jedro, ki je javna last, je bilo razvito med leti 1972 in 1992 na Kalifornijski Univerzi Berkeley, v sodelovanju z Bellovimi laboratoriji. Vgrajeno je v številne komercialne različice, katerih kakovost lahko primerjamo s pomočjo standardne benchmark zbirke *CircuitSim90* /8/. Najpogosteje primerjamo hitrosti simulatorjev in njihovo uspešnost pri reševanju konvergenčnih problemov /9/, /10/, /11/. Namen primerjalnih testov pa ni samo primerjanje izbranih karakteristik (npr. hitrosti, konvergence) ampak pridobiti širši vpogled v kakovost simulatorja. Primerjalni testi se lahko uporabijo tudi za merjenje uspešnosti novih in izboljšanih algoritmov /12/ ter za odkrivanje nepravilnosti simulatorjev, ki so še zmeraj prisotne.

V letu 1993 sta Angelo Brambilla in Dario D'Amore opozorila na nepravilne rezultate, ki se pojavijo z analizo prehodnega pojava pri zelo preprostih linearnih vezij. V prispevku /1/ ugotavljata, da je razlog za nepravilne rezultate hiba trapezne integracijske metode, nikakor pa ne njena implementacija ali topologija vezij ter uporabljeni modeli. Opozorila sta na frekvenčno popačenje časovnih odzivov in lažni prehodni pojav.

Velikokrat se zgodi, da rešitev ne konvergira, kar povzroči prekinitev simulacije. Ti problemi nastopijo zaradi iterativnega iskanja rešitev, predvsem pri enosmernih analizah in analizi prehodnega pojava. Charles Hymowitz v literaturi /4/ opisuje reševanje tovrstnih težav.

Avtorji prispevkov /5/ in /6/ opisujejo problematiko numeričnega integriranja na primeru vezja s pozitivno povratno vezavo. Analitično določen časovni odziv je neomejen, rezultat simulacije pa kaže, da je odziv omejen. Kot glavni vzrok nepravilnosti navajajo nepravilno izbran korak numeričnega integriranja, kar pa je mogoče odpraviti.

Posledica nepravilno izbranega koraka integriranja je lahko ne le frekvenčno popačenje /1/, ampak tudi lažno kaotično obnašanje vezij. Zaradi prevelikega dopustnega koraka numeričnega integriranja se lahko pojavi frekvenčno popačen odziv že pri preprostem linearnem LC vezju /2/, /3/. V primeru nelinearnega vezja (Colpittsovega oscilatorja) pa je odziv celo lažne kaotične narave.

Če ponovimo simulacijo, pričakujemo, da bomo dobili skoraj identične rezultate. To lastnost imenujemo ponovljivost simulacije. Ponovno simulacijo lahko izvedemo z istim simulatorjem na istem računalniku, z istim simulatorjem na drugem računalniku, ali s podobnim simulatorjem na istem ali drugem računalniku. V prispevku se bomo omejili na situacijo, ko ponovno simulacijo izvedemo z istim simulatorjem na drugem računalniku.

V tem prispevku se bomo ukvarjali s vprašanjem, ali današnji simulatorji električnih vezij zagotavljajo ponovljivost rezultatov simulacij. Problematika ponovljivosti rezultatov simulacij je opisana v drugem poglavju, v katerem je predlagana tri stopenjska metrika za kvantitativno ocenjevanje neponovljivosti rezultatov. V tretjem poglavju so opisani rezultati testiranja.

2. Neponovljivost simulacije

Predpostavimo, da s simulatorjem A simuliramo vezje. Rezultate te simulacije poimenujemo referenčni rezultati in jih označimo z A. Rezultate, ki jih dobimo s ponovno simulacijo istega vezja, označimo z B. Če se ti rezultati razlikujejo od referenčnih za manj kot dopuščamo, je ponovljivost zagotovljena. Kadar rezultati simulacij A in B odstopajo za več kot dopuščamo, govorimo o neponovljivosti rezultatov. Če primerjamo rezultate analize prehodnega pojava (TRAN), se odstopanja med A in B kažejo na tri načine:

1. Z različnimi vozliščnimi potenciali. Oblike časovnih potekov so identične. Bistvenih razlik v globalnem obnašanju testnega vezja ni.
2. Z različnimi vozliščnimi potenciali in različnimi oblikami časovnih potekov. Bistvenih razlik v globalnem obnašanju testnega vezja ni.
3. Z različnimi vozliščnimi potenciali, različnimi oblikami časovnih potekov in z različnim globalnim obnašanjem testnega vezja.

Z ozirom na navedene načine odstopanj, smo predlagali ti di kvantitativne ocene za: neponovljivost trenutnih vrednosti signalov - neponovljivost I. stopnje (*M1*), neponovljivost oblik signalov neponovljivost II. stopnje (*M2*) in neponovljivost globalnega obnašanja vezja - neponovljivost III. stopnje (*M3*). Naveden vrstni red ustreza stopnjevanju neponovljivosti rezultatov simulacij.

2.1 Mera za neponovljivost trenutnih vrednosti signalov

Rezultat analize prehodnega pojava je *m* časovnih potekov napetosti in tokov. Posamezni časovni potek je opisan z *n* trenutnimi vrednostmi. Časovne poteke napetosti in tokov, ki jih dobimo s simulacijo A, zapišimo z vrstičnimi vektorji v matriki **X**:

$$\mathbf{X}=\begin{bmatrix}\mathbf{x}_1\\ \mathbf{x}_2\\ \vdots\\ \mathbf{x}_m\end{bmatrix}=\begin{bmatrix}x_1(t_1) & x_1(t_2) & \cdots & x_1(t_n)\\ x_2(t_1) & x_2(t_2) & \cdots & x_2(t_n)\\ \vdots & \vdots & \ddots & \vdots\\ x_m(t_1) & x_m(t_2) & \cdots & x_m(t_n)\end{bmatrix}. \quad (1)$$

Z matriko **Y** na podoben način označimo rezultate simulatorja B. Namen ocene neponovljivost I. stopnje je ovrednotiti odstopanja trenutnih vrednosti časovnih potekov tokov in napetosti, ki jih dobimo pri simulaciji A in s ponovno simulacijo B. Odstopanja trenutnih vrednosti ovrednotimo s pomočjo razdalj med vrstičnimi vektorji matrik **X** in **Y**. Razdaljo med *k*-tima vrstičnima vektorjema $\mathbf{x_k}$ in $\mathbf{y_k}$ izračunamo s pomočjo enačbe:

$$d(\mathbf{x_k},\mathbf{y_k})=\sum_{i=1}^{n}\left|x_k(t_i)-y_k(t_i)\right|. \quad (2)$$

Komponente vektorja $\mathbf{x_k}$ naj bodo referenčne, komponente vektorja $\mathbf{y_k}$ pa tiste, ki jih z referenčnimi primerjamo. Vsaka komponenta vektorja $\mathbf{y_k}$ se sme razlikovati od komponente vektorja $\mathbf{x_k}$ za največ Δx. Če je Δx *dopustno odstopanje* komponent vektorja $\mathbf{y_k}$ od komponent vektorja $\mathbf{x_k}$ izraženo v odstotkih, je *dopustna razdalja* med *k*-tima vektorjema $\mathbf{x_k}$ in $\mathbf{y_k}$ določena z enačbo:

$$\varepsilon_k=\begin{cases}\dfrac{|\Delta x|}{100}\displaystyle\sum_{i=1}^{n}|\zeta| & ;x_k(t_i)=0 \quad i=1,2\ldots n\\ \dfrac{|\Delta x|}{100}\displaystyle\sum_{i=1}^{n}|x_k(t_i)| & ;sicer\end{cases}, \quad (3)$$

pri čemer je ζ minimalna, od nič različna, v računalniku predstavljiva, vrednost.

Privzemimo, da je dopustno odstopanje Δx za vse pare primerjanih vrstičnih vektorjev matrik **X** in **Y** enako. Rezultati simulacij A in B so *ponovljivi* le, če so razdalje med vsemi primerjanimi časovnimi poteki manjše ali enake dopustnim:

$$\varepsilon_1\geq d(\mathbf{x_1},\mathbf{y_1})\wedge\varepsilon_2\geq d(\mathbf{x_2},\mathbf{y_2})\wedge\ldots\wedge\varepsilon_m\geq d(\mathbf{x_m},\mathbf{y_m}). \quad (4)$$

Kadar ta pogoj ni izpolnjen, so rezultati simulacij *neponovljivi*. Za kvantitativno oceno neponovljivosti I. stopnje predlagamo naslednjo mero:

$$M1 = \sqrt{\sum_{k=1}^{m} d(\mathbf{x}_k, \mathbf{y}_k)^2} \quad (5)$$

Vrednost *M1* je tem večja, čim več je odstopanj med trenutnimi vrednostmi časovnih potekov in čim večja so. Če želimo primerjati neponovljivost, ki se pojavi pri različnih testnih vezij, moramo *M1* ustrezno normirati. Normiranje lahko izvedemo tako, da posamezno oceno *M1* normiramo z normo vektorja dopustnih razdalj:

$$M1^* = \sqrt{\sum_{k=1}^{m} \varepsilon_k^{\,2}} = \frac{|\Delta x|}{100} \sqrt{\sum_{k=1}^{m} \left(\sum_{i=1}^{n} |x_k(t_i)| \right)^2} . \quad (6)$$

Če izberemo zadostno majhen Δx in ne pride do neponovljivosti, potem bo tudi zagotovljena ponovljivost oblik in globalnega obnašanja.

2.2 Mera za neponovljivost oblik signalov

M2 se nanaša na obliko časovnih potekov napetosti oziroma tokov. Ker so lahko rezultati simulacij A in B oblikovno podobni tudi, če so vzorci trenutnih vrednosti primerjanih časovnih potekov med seboj nekoliko zamaknjeni, smo za ocenjevanje oblikovnega odstopanja uporabili maksimalno vrednost križnokorelacijskih funkcij $r_{xkyk(j)}$ vseh *m* časovnih potekov.

Časovna poteka $\mathbf{x_k}$ in $\mathbf{y_k}$ sta maksimalno korelirana, ko križnokorelacijska funkcija $r_{xkyk(j)}$ zavzame maksimalno ekstremno vrednost. Če je ta +1 obstaja med $\mathbf{x_k}$ in $\mathbf{y_k}$ popolna pozitivna koreliranost, če je ta vrednost -1, obstaja med njima popolna inverzna koreliranost, če pa je 0, med $\mathbf{x_k}$ in $\mathbf{y_k}$ ni linearne povezave.

Časovna poteka $\mathbf{x_k}$ in $\mathbf{y_k}$ sta oblikovno tem manj podobna, čimbolj je maksimalna vrednost križnokorelacijske funkcije $r_{xkyk(j)}$ oddaljena od vrednosti +1. Če je maksimalna vrednost križnokorelacijske funkcije $r_{xkyk(j)} \leq 0$, sta časovna poteka $\mathbf{x_k}$ in $\mathbf{y_k}$ oblikovno nepodobna.

Oblikovno nepodobnost primerjanih časovnih potekov lahko ocenimo s pomočjo naslednje mere:

$$M2 = 1 - \frac{1}{m} \sum_{k=1}^{m} r_k , \quad (7)$$

pri čemer je r_k maksimalna vrednost križnokorelacijske funkcije:

$$r_k = \begin{cases} \max\limits_j \left(r_{xkyk}(j) \right) & ; \max\limits_j \left(r_{xkyk}(j) \right) > 0 \\ 0 & ; \max\limits_j \left(r_{xkyk}(j) \right) \leq 0 \end{cases}$$

$$\text{za } j = -(n-1), -(n-2), \ldots, 0, 1, 2, \ldots (n-1). \quad (8)$$

Neponovljivost oblik signalov je tem večja, čim večja je vrednost *M2*, ki je lahko iz intervala [0,+1].

Primerjana časovna poteka $\mathbf{x_k}$ in $\mathbf{y_k}$ sta podobna, če je vrednost r_k večja ali enaka *minimalni dopustni vrednosti* r_{min}, ki lahko zavzame vrednosti iz intervala (0,+1]. Če to velja za vse primerjane časovne poteke:

$$r_{\min} \leq r_1 \wedge r_{\min} \leq r_2 \wedge \ldots \wedge r_{\min} \leq r_m , \quad (9)$$

se oblike napetosti oziroma tokov, dobljenih s ponovno simulacijo, bistveno ne razlikujejo od referenčnih.

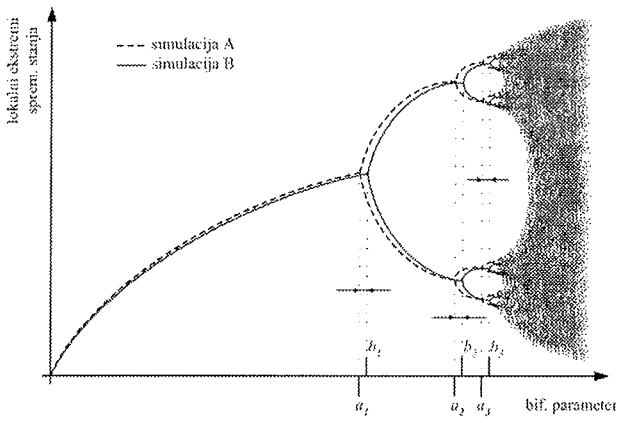
2.3 Mera za neponovljivost globalnega obnašanja

Namen ocenjevanja neponovljivosti III. stopnje je ovrednotiti odstopanja med globalnim obnašanjem testnega vezja pri referenčni simulaciji A in ponovni simulaciji B. Globalno obnašanje testnega vezja ocenimo na osnovi njegovih značilnih lastnosti - bistvenih lastnosti, s katerimi je mogoče okarakterizirati in oceniti njegovo obnašanje. Tipične značilne lastnosti so: pasovna širina, vhodna upornost, preklopna napetost, harmonska popačenja, frekvenca osciliranja itd.

Odstopanja med globalnim obnašanjem testnega vezja pri simulaciji A in ponovni simulaciji B bodo tem večja, čim večja bodo odstopanja med njegovimi istovrstnimi značilnimi lastnostmi. Ker imajo lahko različna vezja različne in različno število značilnih lastnosti, je mera za neponovljivosti III. stopnje odvisna od vrste vezja.

Ker smo pri testiranju ponovljivosti uporabili kaotična testna vezja, smo to mero natančno definirali za tovrstna vezja. Za značilno lastnost smo izbrali mejo med kaotičnim in ne kaotičnim režimom delovanja.

S pomočjo simulatorja A določimo *m* bifurkacijskih točk: $a_1, a_2, \ldots a_m$, ki nastopijo pri bifurkacijah s podvojitvijo periode in jih odčitamo iz bifurkacijskega diagrama (slika 1). Ta predstavlja odvisnost maksimalnih vrednosti izbrane spremenljivke stanja v vezju od bifurkacijskega parametra tj. parametra, s katerim lahko vplivamo na kvalitativne spremembe v obnašanju vezja.



Slika 1: Bifurkacijska diagrama, ki ju dobimo s pomočjo rezultatov simulacij A in B.

Mejo med kaotičnim in ne kaotičnim režimom /13/ določa enačba:

$$a_\infty = (a_2 - a_1)\cdot\left(\frac{1}{\delta_a - 1}\right) + a_2. \qquad (10)$$

Pri tem je δ_a Feigenbaumova konstanta, ki jo izračunamo s pomočjo izraza:

$$\delta_a = \lim_{k\to m} \frac{a_k - a_{k-1}}{a_{k+1} - a_k} \approx \frac{a_m - a_{m-1}}{a_{m+1} - a_m}. \qquad (11)$$

Na podoben način določimo mejo kaotičnosti b_∞, ki jo izračunamo iz podatkov, dobljenih s ponovno simulacijo.

Za oceno nepodobnosti med globalnim obnašanjem testnega vezja predlagamo naslednjo mero[1]:

$$M3 = \left|\frac{a_\infty - b_\infty}{a_\infty}\right| \cdot 100\ [\%]. \qquad (12)$$

Nepodobnost globalnega obnašanja testnega vezja je tem večja, čim večja so odstopanja med mejnima vrednostma $a\infty$ in $b\infty$.

Predpostavimo, da je globalno obnašanje testnega vezja, določeno s simulacijo B še podobno globalnemu obnašanju določenim s simulacijo A, če meja med kaotičnim in ne kaotičnim režimom delovanja vezja v obeh primerih ne odstopa za več kot Δ[%]:

$$a_\infty - \frac{a_\infty \cdot \Delta}{100} \le b_\infty \le a_\infty + \frac{a_\infty \cdot \Delta}{100}. \qquad (13)$$

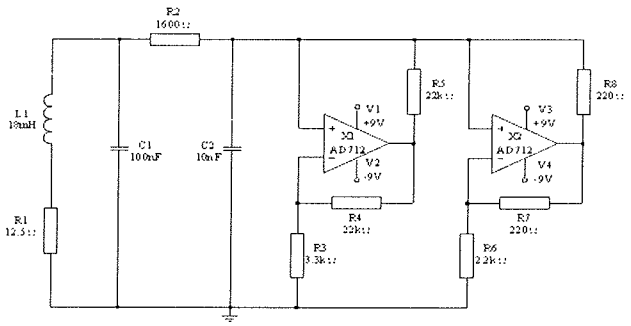
Če pogoj (13) ni izpolnjen, je globalno obnašanje testnega vezja popolnoma nepodobno kar pomeni, da so rezultati simulacij *totalno neponovljivi*.

3. Testiranje ponovljivosti rezultatov simulacij

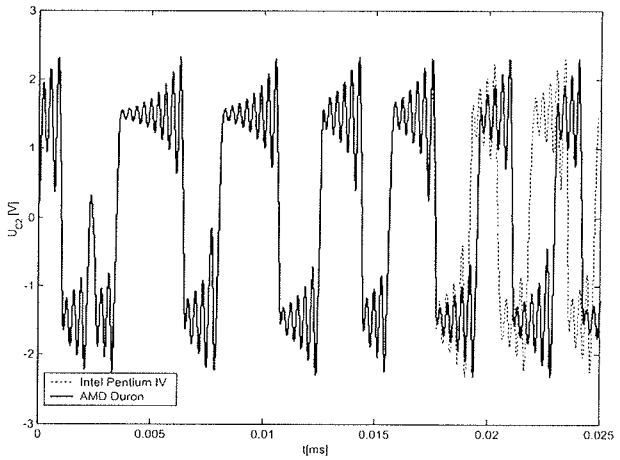
Testirali smo ponovljivost rezultatov simulatorja, ki je bil inštaliranih na platformah z različnimi procesorji. Ker je bila uporabljena ista izvršna koda, smo pričakovali, da bodo rezultati ponovnih simulacij popolnoma enaki referenčnim. Ugotovili smo, da vezja iz standardne benchmark zbirke *CircuitSim90* niso zaznala nobene neponovljivosti. Ker so kaotična vezja hiperobčutljiva na začetne pogoje, smo za testiranje ponovljivosti izbrali Chujev oscilator (slika 2).

Ugotovili smo, da je detekcija neponovljivosti uspešna le:
1. če je obnašanje testnega vezja kaotično in,
2. če je izbran dovolj velik čas trajanja analize prehodnega pojava.

Dejanska neponovljivost lahko ostane nezaznavna:
1. če je osciliranje Chujevega oscilatorja periodično, ali
2. če je kljub kaotičnemu režimu delovanja, izbran prekratek čas trajanja analize prehodnega pojava (glej sliko 3).



Slika 2: Chujev oscilator /14/ - testno vezje za testiranje ponovljivosti rezultatov simulacij.



Slika 3: Divergenca časovnih potekov napetosti na kondenzatorju C2 v Chujevem oscilatorju, (R2=1600Ω), simuliranem na platformi s procesorjem AMD Duron in Intel Pentium IV, je zelo očitna šele po približno 17.5ms.

Podobne rezultate smo dobili tudi z drugimi kaotičnimi vezji. Testiranje smo izvedli na raznih platformah in z različnimi verzijami simulatorja SPICE proizvajalcev: *Intusoft, OrCAD, PENZAR Development, Linear Technology Corporation, FERI Ljubljana* - skupina *CAD* in *Mentor Graphics*. Le pri nekaj simulatorjih se problem neponovljivosti ni pojavil.

3.1 Ocene neponovljivosti trenutnih vrednosti signalov

V poglavju 2.1 smo privzeli, da bodo rezultati simulacij ponovljivi, če nobena od razdalj med referenčnimi časovnimi poteki in časovnimi poteki, ki jih dobimo pri ponovnih simulacijah, ne presega dopustne. Pri testiranju smo privzeli, da je dopustno odstopanje trenutnih vrednosti primerjanih časovnih potekov Δx enako ±0.01%.

Ocene neponovljivosti rezultatov simulacij, ki smo jih dobili pri testiranju enega izmed simulatorjev SPICE, inštaliranega na platformah z različnimi procesorji, so zapisane v tabeli 1 in so podane v normirani obliki *M1/M1**.

1 *Ker v primeru predlaganega testnega vezja mejna vrednost bifurkacijskega parametra a_∞ ne more biti nič, smo M3 definirali kot relativna odstopanja med vrednostma a_∞ in b_∞.*

Tabela 1: Ocene M1/M1 za enega izmed simulatorjev SPICE, inštaliranega na platformah z različnimi procesorji.*

Referenčna platforma A s procesorjem	**Platforma B s procesorjem**						
	Cyrix (IBM) 6x86MX	*AMD Duron*	*AMD Athlon XP*	*Intel Pentium MMX*	*Intel Pentium III*	*Intel Celeron (Willamette)*	*Intel Pentium IV*
Cyrix (IBM) 6x86MX	-	12099.93	12099.93	11905.79	11905.79	11905.79	11905.79
AMD Duron	12082.59	-	0	11782.12	11782.12	11782.12	11782.12
AMD Athlon XP	12082.59	0	-	11782.12	11782.12	11782.12	11782.12
Intel Pentium MMX	11991.36	11883.84	11883.84	-	0	0	0
Intel Pentium III	11991.36	11883.84	11883.84	0	-	0	0
Intel Celeron (Willamette)	11991.36	11883.84	11883.84	0	0	-	0
Intel Pentium IV	11991.36	11883.84	11883.84	0	0	0	-

Ocene v tabeli 1 kažejo, da daje simulator:

1. neponovljive rezultate, če je inštaliran na platformah s procesorji različnih proizvajalcev;
2. ponovljive rezultate, če je inštaliran na platformah s procesorji istega proizvajalca - vrednosti *M1/M1** so enake nič.

3.2 Ocene neponovljivosti oblik signalov

Z ocenjevanjem neponovljivosti II. stopnje smo ocenili oblikovno nepodobnost primerjanih časovnih potekov. Ker postane morebitna divergenca primerjanih časovnih potekov očitna šele po približno 50ms smo privzeli, da sta dva časovna poteka od tedaj oblikovno podobna, če je maksimalna vrednost pripadajoče križnokorelacijske funkcije večja ali enaka 0.8. Če je pri tem pogoj (9) zmeraj izpolnjen, simulator zagotavlja oblikovno podobne časovne poteke.

V tabeli 2 so podane ocene neponovljivosti II. stopnje za enega izmed simulatorjev.

Glede na dobljene rezultate lahko zaključimo, da simulator zagotavlja oblikovno podobne časovne poteke napetosti in tokov v testnem vezju le, če je inštaliran na platformah z procesorjem istega proizvajalca. Vrednosti v tabeli 2 namreč kažejo, da je v teh primerih vrednost *M2* enaka nič, v ostalih primerih pa pogoj (9) ni izpolnjen.

3.3 Ocene neponovljivosti globalnega obnašanja

Ocena neponovljivosti III. stopnje vrednoti odstopanja v globalnem obnašanju testnega vezja. Po definiciji, opisani v poglavju 2.3, odstopanja ocenimo z odstopanjem meje med kaotičnim in ne kaotičnim režimom delovanja.

Pri ocenjevanju neponovljivosti III. stopnje smo se omejili na prve tri bifurkacijske točke. Za bifurkacijski parameter smo izbrali upornost R2, za opazovano spremenljivko stanja pa napetost kondenzatorju C2. Upornost R2 smo spreminjali na intervalu $1820\Omega \leq R2 \leq 1860\Omega$ po koraku 0.2Ω in v dobljenih časovnih potekih napetosti na kondenzatorju C2,

Tabela 2: Ocene neponovljivosti II. stopnje za enega izmed simulatorjev, inštaliranega na platformah z različnimi procesorji.

Referenčna platforma A s procesorjem	**Platforma B s procesorjem**						
	Cyrix (IBM) 6x86MX	*AMD Duron*	*AMD Athlon XP*	*Intel Pentium MMX*	*Intel Pentium III*	*Intel Celeron (Willamette)*	*Intel Pentium IV*
Cyrix (IBM) 6x86MX	-	0.8437	0.8437	0.8354	0.8354	0.8354	0.8354
AMD Duron	0.8437	-	0	0.8117	0.8117	0.8117	0.8117
AMD Athlon XP	0.8437	0	-	0.8117	0.8117	0.8117	0.8117
Intel Pentium MMX	0.8354	0.8117	0.8117	-	0	0	0
Intel Pentium III	0.8354	0.8117	0.8117	0	-	0	0
Intel Celeron (Willamette)	0.8354	0.8117	0.8117	0	0	-	0
Intel Pentium IV	0.8354	0.8117	0.8117	0	0	0	-

Tabela 3: Ocene neponovljivosti III. stopnje za enega izmed simulatorjev SPICE, inštaliranega na platformah z različnimi procesorji.

Referenčna platforma A s procesorjem	**Platforma B s procesorjem**						
	Cyrix (IBM) 6x86MX	*AMD Duron*	*AMD Athlon XP*	*Intel Pentium MMX*	*Intel Pentium III*	*Intel Celeron (Willamette)*	*Intel Pentium IV*
Cyrix (IBM) 6x86MX	-	$9.665\ 10^{-4}$	$9.665\ 10^{-4}$	$9.665\ 10^{-4}$	$9.665\ 10^{-4}$	$9.665\ 10^{-4}$	$9.665\ 10^{-4}$
AMD Duron	$9.665\ 10^{-4}$	-	0	0	0	0	0
AMD Athlon XP	$9.665\ 10^{-4}$	0	-	0	0	0	0
Intel Pentium MMX	$9.665\ 10^{-4}$	0	0	-	0	0	0
Intel Pentium III	$9.665\ 10^{-4}$	0	0	0	-	0	0
Intel Celeron (Willamette)	$9.665\ 10^{-4}$	0	0	0	0	-	0
Intel Pentium IV							

poiskali lokalne maksimume. Njihovo odvisnost od vrednosti upornosti R2 smo opisali z bifurkacijskim diagramom.

S pomočjo enačbe (12) smo ocenili neponovljivosti III. stopnje, ki so zapisane v tabeli 3. Z ozirom na pogoj, opisan z enačbo (13), smo predpostavili, da so rezultati, ki jih daje simulator na referenčni platformi A in platformi B totalno neponovljivi, če je odstopanje med mejno vrednostjo bifurkacijskega parametra a_∞ in b_∞ večje od $\Delta=\pm 10\%$.

Na osnovi rezultatov ocenjevanja neponovljivosti III. stopnje smo ugotovili, da simulator, inštaliran na platformah z obravnavanimi procesorji, ne daje totalno neponovljivih rezultatov, saj je pogoj (13) v vseh primerih izpolnjen.

4. Sklep

V prispevku smo se ukvarjali s vprašanjem: ali današnji simulatorji električnih vezij zagotavljajo ponovljivost rezultatov simulacij? Ponovljivost rezultatov simulacij je zagotovljena takrat, kadar dobimo pri ponovitvi simulacije rezultate, ki so znotraj dopustnih odstopanj. Odstopanja med referenčnimi rezultati in rezultati ponovne simulacije se kažejo v različnih trenutnih vrednosti, v različnih oblikah potekov napetosti oziroma tokov in v različnem globalnem obnašanju vezja. Za te tri primere smo definirali ustrezne metrike, s katerimi lahko tudi ocenjujemo morebitno stopnjo neponovljivosti.

V prispevku smo se omejili na situacijo, ko ponovno simulacijo izvedemo z istim simulatorjem na drugem računalniku. Računalnika sta se razlikovala samo v vrsti mikroprocesorja, uporabljala pa sta isto izvršno kodo simulatorja. Kljub tej razliki, ki naj ne bi vplivala na rezultate simulacije, smo ugotovili, da v nekaterih primerih prihaja do neponovljivosti rezultatov simulacij. Ugotovili smo, da z vezji iz benchmark zbirke *CircuitSim90* ni možno zaznati neponovljivosti. Le pri simulaciji kaotičnih vezij se je pojavila neponovljivost trenutnih vrednosti in oblik signalov.

Na osnovi rezultatov testiranja ponovljivosti lahko zaključimo, da nekateri današnji simulatorji električnih vezij, na platformah z določenimi procesorji, ne zagotavljajo ponovljivih rezultatov in, da je neponovljivost mogoče zaznati le s pomočjo hiperobčutljivih testnih vezij. Ker benchmark zbirka *CircuitSim90* tovrstnih vezij ne vsebuje, predlagamo njeno razširitev s kaotičnim vezjem.

Vzrok za neponovljivost rezultatov je lahko ena ali več napak v programu simulatorja ali prevajalniku programa, ki dopuščajo različno interpretacijo istih procesorskih ukazov na različnih procesorjih. To je mogoče, saj se proizvajalci današnjih procesorjev do potankosti ne držijo IEEE standardov za aritmetiko s plavajočo vejico. Zraven tega nekatere lastnosti te aritmetike niso natančno specificirane, kar dopušča različnost implementacij. Proizvajalci procesorjev v svoje izdelke vgrajujejo tudi lastne dodatke, ki jih trenutni standardi ne obravnavajo.

Obstoj neponovljivosti rezultatov simulatorjev SPICE predstavlja njihovo novo nepravilnost, ki pa v mnogih primerih ostaja uporabniku prikrita.

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Prispelo (Arrived): 13.11.2003 *Sprejeto (Accepted): 25.02.2004*

SEAMLESS HW/SW CO-DESIGN FLOW

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Key words: design space exploration, directed acyclic hyper-graph (DAG), HW/SW co-design, partitioning, scheduling

Abstract: Computing applications complexity has raised to the level where managing the design flow in the classical way, while satisfying various constraints, is becoming extremely hard to cope with. We see two main reasons for that. The first reason is partial consequence of Von Neumann architecture inheritance which imposes throughput restrictions /1/ with its imposed program sequentializing. The CS curriculum and rich set of tools are both suited to that model. Now, speedups are possible by providing additional HW components operating concurrently. We expect that the work will be done in the direction of a revised application development design flow approach which would trade the execution time for complexity. The second reason is the consequence of the IC manufacturing technology improvement with its increasing level of integration which enables a steep system level complexity increase in a wide range of applications. Many of them also face short time to market. CAD tools are not in pace with this increasing complexity, thus putting pressure onto design teams. The design cycle round time shortening is possible by different levels of modeling, where each of them features design decision estimations. This paper presents the HW/SW co-design architecture exploration space and gives an overview over the related methodologies. Based on the study of these methodologies and our experience with an ad-hoc approach, we present a seamless HW/SW co-design flow. The flow forms the basis for the development of a CAD tool helping designers to considerably benefit from the HW concurrency and offering an efficient system level approach.

Enovit načrtovalski potek sočasnega načrtovanja strojne in programske opreme

Kjučne besede: hkratno načrtovanje strojne in programske opreme, razmeščanje, razvrščanje, usmerjen graf vezja

Izvleček: Kompleksnost računalniško podprtih aplikacij je narasla do nivoja, ko je klasičen potek načrtovanja, ob hkratnem upoštevanju vseh omejitev, postal zelo težko obvladljiv. Tukaj vidimo dva glavna razloga. Prvi razlog je delna posledica Von Neumannove arhitekturne zapuščine, ki z vpeljano programsko sekvenčnostjo omejuje podatkovno pretočnost /1/. Računalniška veda in nabor orodij sta oba prilagojena temu modelu. Pohitritve so sedaj mogoče z dodajanjem vzporedno delujočih strojnih komponent. Nadaljnje delo vidimo v smeri predrugačenega načrtovalskega poteka razvijanja aplikacije, ki bi ceno povečane hitrosti izvajanja aplikacije plačal s povečanjem arhitekturne kompleksnosti. Drugi razlog je posledica tehnološke izboljšave izdelave integriranih vezij, ki z vse večjo integracijo omogoča eksponentno naraščanje sistemske kompleksnosti na širokem področju aplikacij. Dodaten pritisk pri razvoju aplikacije pa je lahko tudi kratek čas do trga. CAD razvojna orodja pa ne uspejo držati koraka v kompleksnosti, tako se povečujoče se breme prenaša na raziskovalno ekipo. Skrajšanje načrtovalskega razvojnega cikla je mogoče z modeliranjem na različnih nivojih, ki podpirajo možnost ocenitve načrtovalskih odločitev. Članek predstavi arhitekturni nabor primeren za hkratno načrtovanje strojne in programske opreme in poda pregled sorodnih metodologij. Na osnovi študije teh metodologij in izkušenj pridobljenih z ad-hoc pristopom predstavljamo enovit načrtovalski postopek sočasnega načrtovanja strojne in programske opreme. Načrtovalski potek vidimo kot osnovo za razvoj CAD orodja, ki bi načrtovalcem omogočil efektivno izkoristiti prednosti sočasnega delovanja strojne opreme in bi nudil efektivni sistemski pristop.

1 Introduction

Size and complexity of high performance signal, image and control processing algorithms is increasing tremendously. Classical SW approaches with traditional von Neumann-like architectures are far from being optimal. Their major strategy to overcome complexity and increase throughput is increasing the processor clock speed and SW optimization methods /1/, /2/. Moreover, the algorithm complexity and real-time constraints in reactive embedded systems can be so demanding that classical high end SW processor at a reasonable clock speed can no longer manage the task /3/. The only possible solution to the problem is a unified HW/SW co-design approach. Nevertheless, when studying HW/SW co-design, some other issues of similar importance arise. When partitioning between HW and SW, the following design metrics have to be accounted for: cost, size, performance, power, time-to-prototype, time-to-market, correctness, safety, and maintainability /5/. As some of these design metrics compete among themselves, managing the HW/SW co-design exploration space is even harder. In order to meet the optimization challenge, the designer must be comfortable with a vast variety of HW and SW implementation technologies enabling him/her to find an optimal solution for a given application and constraints. A rich expertise in both SW and HW domain is required for this purpose.

After the heterogeneity problem is solved, the next to be copped with is the system level complexity problem. The process of applying the application description onto architecture can be an extremely complex task when details are to be described in a non hierarchical way. Support for different level approaches has to be provided for. System level design decision choices should be available as late as possible within the design cycle, thus enabling the explore-propose-validate-refine process to achieve its best, while the accuracy of a model gradually increases. This is not the case in the classical approach where HW (processor) is designed in advance, hopefully powerful enough,

and SW (application) is adapted to it. Each designer involved with designing a fairly modest system, from the initial specification to the final implementation, has to deal with complexity when interconnecting heterogeneous components. The explore-propose-validate-refine process can be a very tedious work, especially when a variety of possible implementations should be explored to best satisfy design metrics. In the first approach aiming at lowering the designers' stress while simultaneously increasing productivity and the largest manageable system complexity, the design work is partitioned among multiple designers. Two problems arise. First, when partitioning work on smaller subsets, the designers specialize into a relatively narrow segment of the whole system. This gives rise to the problem of how developing individual parts of the system without having a clear idea of the overall system integrity. Second, adding system designers to the project does not work as expected. Believing that the designer's productivity is independent of the project team size is not in place. Simple man-month relations are not valid when the project team size increases. After some point, enlarging the number of designers working on the project does not contribute to the design cycle shortening/5/.

All these facts show the importance of research studies for guiding development of CAD tools to support the entire design flow based on heterogeneous architectures and to provide system level support. Such CAD tools are necessary to cope with the exponentially increasing system complexity. Already existing CAD tools provide a semi-automatic interactive environment where most important scheduling and partitioning decisions are the designer's choice. As seen currently, a fully automatic approach is impossible for the present.

The rest of the paper is organized as follows. Section 2 describes diverse architectures enabling efficient HW/SW co-design exploration. Analyzed are also their weaknesses and strengths. Section 3 presents some of the work related to HW/SW co-design approaches and methodologies. In section 4 we propose a seamless HW/SW design flow based on the study of these methodologies and our experience with ad-hoc approaches of application partitioning and system level integration /15/. In section 5 we introduce our ad-hoc application partitioning with which we acquired knowledge needed for mastering heterogeneous architectures and HW/SW partitioning. Section 6 concludes this paper.

2 HW/SW co-design exploration opportunities

HW/SW design deals with balancing the architecture resources of a digital system in the search for an optimal implementation. With the term architectural resources we denote all kinds of storage resources (memory, registers), programmable resources (FPGAs), partially programmable resources (application specific and general purpose SW processors), nonprogrammable resources (single purpose processors) and communication resources (interconnections, buses) which provide space for flexible exploration. All resources should be taken into account and trimmed carefully to achieve optimal design metrics. Design metrics that we are focusing on in our work are cost, time-to-prototype and performance improvement. Meeting these criteria leads us to some compromises that still permit us a level of flexibility large enough to explore a variety of implementation options. Some possible exploration environments that enable HW/SW co-design study are:

- FPGA-only HW environment with a processor implemented as a softcore. Microprocessor architectures implemented as a softcore (ARM, ARC, MIPS, PowerPC, etc.) offer limited performance. There are many technical reasons for this. Far ahead in usage are Xilinx's Micro Blaze (for the Spartan and Virtex family of FPGAs) /12/ and Altera's Nios (for Cyclone and Stratix FPGAs) /13/ sold as IP cores. These processors can achieve the maximum clock speed in the range of 100MHz and can occupy quite a large portion of FPGA; the more complex the processor is the slower the speed is. OSs can be very simple and provide only some basic functionality thus making the portability of application harder. Advanced OSs require a more powerful processor, more FPGA resources, but also decrease the maximal clock speed.
- Standalone processor with FPGA logic as its periphery /14/. Embedded systems are a very good example of it. Their maximal performance is attained if FPGA is connected directly to the processor's bus to optimize data transfer rates. A lower overhead for accessing external HW provides more partitioning possibilities. Despite their greater complexity and an additional HW overhead, an extensive computation power can be attained. The various OSs are well supported for many processors on the market with compilers, cross-compilers and debuggers. Many of them can be obtained free of charge. The initial cost includes building such an embedded platform and porting some OS to make the platform alive and stable.
- The PC environment and some additional custom HW /15/. PC does not represent any overhead as a result of its popularity and availability. Executing SW is stable and a variety of development tools exist. If communication method is not of primary interest (PCI bus), it offers a great set of architectural resources when combined with a resource-wealthy add in PCI board. Also, when moving to another set of architectural resources, it allows for a great amount of code reusability (SW or HW IP). Some HW scalability is also supported in the PC environment through PCI extension slots.
- New extensions to HW/SW co-design are offered by programmable SoC platforms. They comprise programmable arrays, hard wired microprocessors and rich set of fast communication peripheries. Their rep-

resentatives are Xilinx Virtex II Pro /12/ and Altera Excalibur /13/. Virtex II Pro consists of up to four PowerPCs. They are integrated within a regular FPGA structure by sacrificing some silicon that would otherwise be used for CLBs and interconnections. Excalibur offers an ARM9 processor and programmable array integrated within the same IC, with a smaller level of integration than the former. In this way, HW/SW cohesion can be applied very efficiently and the whole design can be finally fitted in one chip.

As a result of the overall complexity of the whole system design, regardless of the environment chosen, stable and efficient SW tools are required to efficiently manage application mapping onto available architectural resources.

3 Related work

There is currently a lot of activities related to HW/SW co-design methodology underway. Many of the research groups focus on some particular stages in the design process or even optimize some of these stages to best suit their finite extent of supported architectures. Such closed areas of increased interest can be the system level specification and modeling, partitioning and scheduling, compilation and synthesis, co-verification and co-simulation, automatic code generation for HW and SW interfacing, and automatic code generation for the task manager. The common denominator among them is splitting the input description into subtasks and describing data dependency between them. For that purpose most of them use some form of directed acyclic hyper-graph (DAG) /3/, /6/. Nodes in the graph represent subtasks (more or less complex operations) and edges represent data dependency between them. Many automatic scheduling and partitioning tools uses DAG (or some extension of it) for applying some optimization methods to obtain satisfactory mapping of applications onto architecture. The task of optimization methods is to find an optimal partitioning and scheduling scenario for subtasks extracted from the input specification. Common partitioning and scheduling problems belong to the class of NP-hard and intractable problems. Research studies have been done on algorithms involving heuristic search /7/. Heuristic optimization methods are guided by applied cost functions to evaluate implementation space realizations.

Numerous researches have already been done in the field of HW/SW co-design. Here we report only the work that we find particularly interesting for our study.

Wiangtong, Cheung, and Luk /6/ presented a semi-automatic co-design environment for a system consisting of a single general purpose processor and multiple reconfigurable HW units. Their study involves building HW/SW architecture suited for dataflow dominated applications. The proposed design flow enables input application description in high level language (HLL). Mapping the input description into DAG is done manually. Authors implemented automatic generation of the underlying code and taking care of necessary application sub-tasks communication by wrapping tasks in standard frames. Independent tasks are executed on several processing elements. They are controlled by an automatically generated task manager program running on the SW processor. Because of the task's standard frame overhead, this method is appropriate for coarse grain partitioning. Authors presented a study of heuristic methods suited for partitioning and scheduling /7/. They applied them onto DAG and thus made a next step towards a fully automatic design flow.

AAA methodology /3/ extends DAG and adds ability to specify loops through factorization nodes. This leads to an algorithm model called factorized data dependence graph (FDDG). Graph factorization consists of replacing a repeated pattern by only one instance of it. Because of extension, it is suitable both for data and control flow dominated applications. FDDG may be specified directly or it may be generated from HLL (Esterel, Signal). Methodology main efforts are towards graph transformations. Optimization consists of finding defactorization transformations within implementation space. This gives best results in terms of cost function (heuristics guided by their cost function). AAA uses a single factorized graph model from the algorithm specification down to the architecture implementation through optimizations expressed in terms of defactorization transformations applied to the algorithmic graph. Automatic generation of a HW implementation from an algorithm specification based on FDDG is supported by employing a set of rules for data and control path. The algorithm employs synchronization rules and a delocalized control approach (as opposed to the above mentioned methodology). Support for real-time extension is studied, too.

A very important area of HW/SW co-design is task communication in terms of resource sharing, which often does not get enough attention compared to its influence on the overall system performance. Communication channel is a resource, similarly as other processing elements, and must be scheduled. When several tasks use the same communication resource, the channel activity also causes task delays which must be taken into account when task scheduling. /9/ gives an overview of this topic, proposes rules and explores genetic algorithm heuristics to schedule tasks. While achieving shorter execution time, implied rules impose only a small overhead to the whole scheduling and partitioning process.

Work has also been done in the direction of finding a language that would meet the needs for describing HW and SW so as to enable compilation and synthesis, and support various level application modeling. Several mature languages exist that were originally suited for SW (C/C++) or for HW (VHDL/ Verilog) design. They all exhibit some weak points when bridging the heterogeneity gap. Some special points of interest are: support for HW description, concurrency support, system level description and modeling,

gradual model refinement, and verification. SystemC /10/ solves this problem by introducing specific class libraries which are ANSI C++ compliant. SystemC benefits from all C++ object oriented attributes and leverages it by introducing concurrency, notion of time and support for HW data types. Extensions are realized through running an executable system description under the SystemC simulation kernel. SystemC tends to become a standard as a language-based modeling tool for system-level design; OSCI has already submitted it to the IEEE for standard approval. SystemC itself should not be considered as a methodology. It is a modeling language from which HW/SW co-design can benefit. Another very important feature is system verification support. Support is enabled through Cadenece SystemC verification extension built on top of SystemC library /11/.

4 Seamless design flow

If we outline some properties, which in our opinion the designer-friendly and applicable HW/SW co-design CAD tool should have, we quickly find some weak points of methodologies in many of the currently active research studies in the field of HW/SW co-design. The CAD tool, which we are steaming to, should take the advantage of mature languages and just fill the gap caused by heterogeneity. Input description languages that are already widely accepted and have a rich set of underlying supporting tools should not be disregarded and, for the same reason, new description languages should not be forced by any means. A work around could be implementing some additional features to the already existent languages (by means of libraries or language extensions of a reasonable level) or building some supporting environment to extend the language description capability. Tools for building SW executives (compilers) are already well optimized, and designers are trained to use them efficiently. Tools for building HW net-lists (synthesis tools) are also very powerful. In this paper we are introducing a seamless environment where these sets of already existent tools can be used in a uniform way to support design flow from the system level description to distributed executives and net-lists. Effort should be made in the direction of automatically crossing the HW/SW barrier and at the same time reusing powerful aspects of tools on both sides.

The gap between HW and SW is currently handled by the system designer, who is doing a tedious work of the explore-propose-validate-refine process. The model accuracy is gradually increased when more details are added. This consequently prolongs the time needed for the system model development and simulation. To reduce the time required for design space exploration evaluation of design choices should be supported earlier in the design process, which leads us to system level exploration.

Figure 1 outlines the traditional design flow. This approach is also known as Y-chart approach /16/. It introduces the main idea that seamless HW/SW co-design environment should provide for a sufficient support. The input specification consists of an architecture and application description as well as application constraints. HW/SW co-design approach main object is finding the best mapping of application onto available HW resources, while satisfying constraints. As the Y-chart suggests, the process of finding the optimal mapping consists of iterating cycles. The process of evaluating different possible solutions that are candidates to realize the application within given constraints is named design space exploration. The design space consists of a variety of spatial and temporal mappings and, as mentioned before, this problem can easy become unsolvable. Dashed arrows suggest the order of design space exploration. First, the design space built from a given architectural and application description is explored. If no solution within the design space satisfies constraints, the next step is to revise the application description in terms of algorithm speedups. The whole design cycle from the previous step is repeated. If widening the design space still does not produce satisfactory solutions, this is an indication that, within given architectural resources, application mapping cannot be made by realizing constraints. Another important aspect of the Y-chart is reusability since it enables mapping of multiple target applications onto candidate architectures in order to evaluate performance.

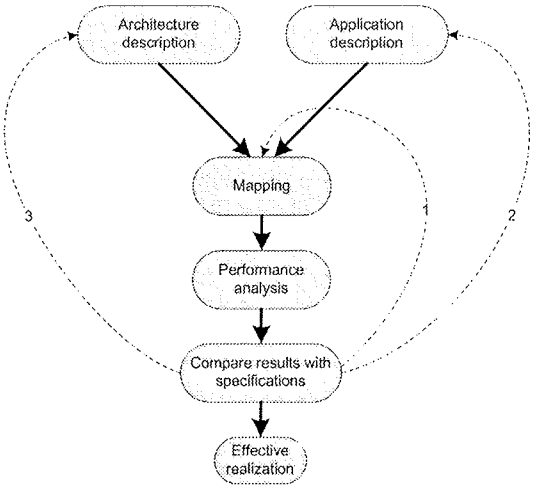

Figure 1: Y-chart approach

Our approach to HW/SW co-design partially follows the traditional Y-chart approach guidelines. It mostly extends it as it is in detail explained in Figure 2. The application is in the foreground. Optimal partitioning and scheduling are obtained by employing gradual model refinement.

The application description is split into the system level description and full-detail level description. At the system level description we benefit from SystemC system level modeling and model refinement. The system level application description satisfies two purposes. First, information about tasks and data dependency between them is captured to construct DAG. Second, the system level description is used as a simulation skeleton to guide heuristic

methods so as to find the optimal spatial and temporal distribution. The task description can be very loose at this stage. The full-detail level is not needed at this stage and can be postponed.

Architecture is described by a set of available system resources, providing necessary external tools for synthesis, compilation, verification and simulation, providing IP blocks of more or less complex operators in terms of library, specifying standard frames to enable automatic generation of task communication and automatic generation of control logic for task scheduling, and specifying communication channels.

Similar to the application description, the architecture description is also split into two parts. The term architecture description means all kinds of specifications that smooth the higher level description compilation or synthesis onto target architecture (C/C++, VHDL, or an even higher level task representation abstraction). The coarse grain architecture description is provided with external tools that enable smooth transition from the HLL HW and SW code to the netlist (synthesis) and executable code (compilation) and provide its testing, simulating, verifying, debugging and profiling. Clearly defined architecture limitations that sensibly limit the design space size are also a part of the coarse grain description; e.g. a number of processing elements suitable for SW execution, amount of available memory, number of system buses... Library provides synthesizable and compilable description of standard elements, supports automatic generation of the underlying code and provides support for IP reuse. Library consists of blocks of HW and SW descriptions of various complexity levels. These can be all kinds of wrappers, supporting smoother integration of the user defined code (with HW or SW tasks), communication channels (implementing SW drivers and HW protocols), and various complexity level operators (from simple adders and multipliers to more complex cores such as DCT).

Although the split architecture description may look somehow artificially made, it is a necessary design approach, because programmable gate arrays enable realization of virtually any function, endlessly extending the design space. The coarse grain description is used for quick infallible partitioning and scheduling decisions, rejecting unfeasible schemes. Providing library of synthesizable cores wraps the endless design space to a final extension and enables IP reuse.

Constraints are used to build cost functions needed by heuristic methods to identify the best solution within the design space and to evaluate the result from heuristics. Constraints can be given in any combination of resource utilization, power consumption, and application execution time. Constraints must be later given appropriate weights to obtain the cost function to guide heuristic search methods.

Given the necessary input specification, the system level application description is studied and data dependency between tasks is obtained to build DAG. The main feature of DAG is determining the dataflow dependency to overcome the sequential nature of the application description and to discover parallelism possibility. Tightly connected to building DAG is rearranging parts of the graph by applying different algorithms, i.e. by increasing the parallelism rate and granularity modification /3/.

After application is split into subtasks and potential parallelism is discovered, DAG partitioning and mapping take place. Application is partitioned on the basis of the input specification about HW only, SW only and HW or SW tasks, and the design space, to be explored later, is defined. While partitioning and mapping, architectural resources information is needed to obtain a set of operators capable of executing application operations to be mapped. Up to this point the design space consists of a variety of combinations, covering every possible mapping of every subtask to appropriate available resource. In the case of implementation of HW resources with programmable circuits, the design space is infinite, thus practical limitation is set by a

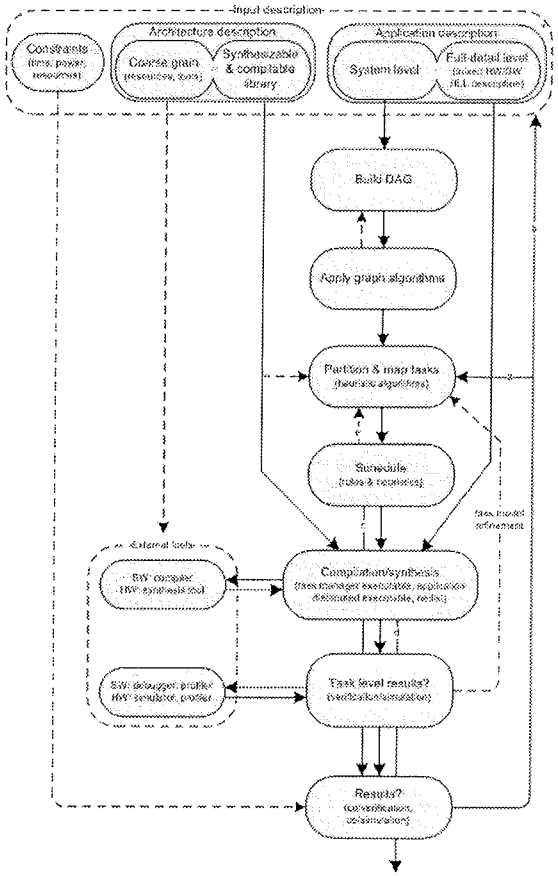

Figure 2: HW/SW co-design design flow

finite number of library components. Finding the optimal solution within the design space takes time that is exponentially dependant on the design space size when solved with feasible computers. Even in the case of a modest

application, the problem quickly becomes unmanageable. Here, the system level approach enables us to explore only defined subsection(s) of the entire system, thus isolating the detailed level description of a partition and schedule enabled task from the rest of the system, described only for a necessary interaction. In the next step, scheduler extends the design space even more. Solving this kind of optimization problems belongs to the class of NP problems. Keeping the design flow time under control, heuristic methods are necessary. These methods will select a point from the design space and estimate its result adequation guided by the cost function. The way how the design space is explored depends on the chosen heuristic method /7/.

The partitioning step is tightly integrated with scheduling step heuristic methods and rules. The scheduler task is to find optimal temporal distribution which would produce the shortest application runtime. Temporal mapping is applied to subtasks that share common resources. The execution order depends on data dependency extracted from DAG and when determining the execution order, rules are applied which take into consideration resource conflicts and task delays caused by them /9/. Two resource allocation policies /4/ can be applied; dynamic and static. This paper addresses only the static one. To find optimal scheduling, each task must be described by its communication and processing time. This time can be obtained either as the input given approximately or as a more realistic feedback from subsequent stages. In Figure 2 it is depicted by dotted arrow labeled task model refinement.

After tasks are spatially and temporally mapped, the mapping efficiency can be estimated using SystemC system level model executive. It is indicated by a solid arrow labeled c. The input specification for SystemC executive is built from the system level application description input, modified by graph transformation algorithms and spatial and temporal mappings. Estimations are getting closer to realistic values when task descriptions are becoming gradually refined, which is the primary feature of SystemC. Partitioning and scheduling heuristic algorithms iteratively explore the design space until an optimal solution is found (depicted by a dotted arrow labeled a). If iterative heuristic algorithms fail to find a solution within the design space, the input description must be reviewed (depicted by a dotted arrow labeled b).

Gradual application system level model refinement introduces optimal spatial and temporal mapping for a given input specification. If results conform to constraints, the subtask descriptions should be refined to a full-detail level according to the winning partitioning scheme. Currently, we assume mixed SW and HW language description (C/C++, VHDL). At this point, architectural information is used to wrap detailed described subtasks into standard frames thus enabling automatic task connectivity and automatic control generation. Compilation and synthesis are done with the usage of external tools connected into a seamless design flow through command line extension. When constraints are satisfied, this is also the subsection of the design flow where the entire HW and SW code is generated for every programmable part of the architecture. After a synthesizable and compilable code is obtained for every task, it can be verified and simulated with the use of external tools. Task level verification and timing simulation can be applied using external tools, which will serve as an exact guide to the partitioning and scheduling algorithm.

5 JPEG design Example

As previously described, the design flow gradually evolved by taking into account the related work in this area, leveraged by our experiences obtained with an ad-hoc approach of partitioning and system level integration. Experiences with real-life applications were the motivation key while evaluating the related methodology successfulness, and later they were golden guidelines when developing our own design flow within a seamless environment.

Following the architectural classification in section 2, our targeted exploration architecture fits into the second group of co-design exploration suitable architectures (processor, accompanied with array of programmable logic). The platform is based on the Intel Strong ARM microprocessor, supporting a variety of peripheries which eases communication and extends its flexibility /14/. HW programmability is achieved by introducing FPGA connected directly onto the microprocessor's bus. The platform supports the Linux operating system. Integration of SW executive and necessary control logic with the rest of programmable HW resources is supported through kernel drivers. While improving the design flow, we also made a move towards the PC based HW/SW co-design platform /15/, presented as the third possible architecture in section 2.

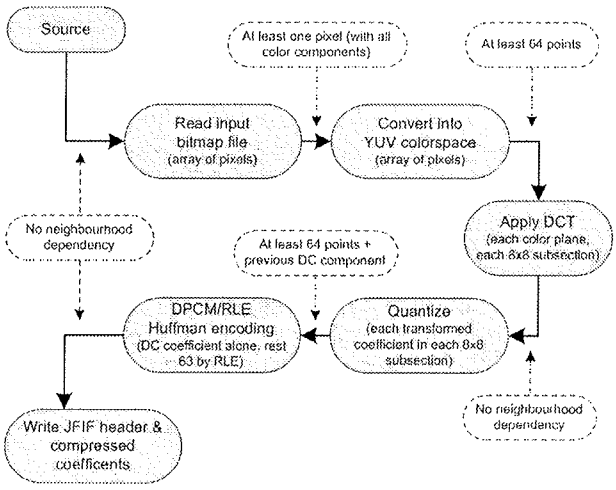

Figure 3: JPEG encoding steps

In order to carefully study the whole design flow, we decided to manually realize all design steps by implementing the JPEG coding / decoding image processing application

/17/. The JPEG image processing overall complexity is well suited for a wide range of processors and their performance improvement can be substantial, provided that an optimal HW-SW co-design solution is found. Figure 3 shows JPEG compression steps, suitable as a starting point for the system level application description. This figure also exhibits the high level input application specification tightly connected to our basic idea of the high level task description. A closer examination of encoding steps already reveals not easily observable possibilities of design decisions, explicitly at the system level. Although the compression flow exhibits pure sequential data processing, the exploration space can be still revealed. Shaded nodes in Figure 3 straightforwardly resemble the JPEG compression flow. Only broken line circuited explanations commenting data dependency are here important. Dependency comments explain the minimally required amount of data provided by the previous task and needed to start the next one. If every task requirements were an entire image array, then the application task flow would be seen as strictly sequential. Here, we can discover/apply a mixed sequential, parallel, and in some stages even pipelined behavior. An optimal system level partitioning and scheduling decision would consider the required/available amount of memory between tasks, number of necessary task repetitions linked to the task execution time, and possible resource conflicts. Figure 3 expresses a close resemblance to DAG; the application is logically coarsely partitioned into subtasks, represented with nodes, and tasks data dependency is represented with arrows. After the tasks resource usage is evaluated, guidelines for finer task re-partitioning are obtained, leading into a successively refined partitioning scheme.

Following the Figure 2 design flow, a coarse grain architecture description is provided by means of a gcc compiler and gdb debugger, limitation of only one SW processor, and a certain amount of the available memory. A detailed library description is provided by a Wishbone compliant 1D DCT core, Wishbone communication structure, and device driver (SW/processor to HW/FPGA communication). Since we chose a point from the design space manually, the only constraint that makes sense is HW and SW resource usage limitation.

As every portion of the design flow was processed manually and the turnaround time was expected to be rather long, our focus was not on design space exploration, but rather on realization of the entire design flow from description to realization. It was noted that by choosing just one design point from the design space, only a suboptimal solution could be obtained. The design space is explored thoroughly as the entire flow is automated thus shortening the time required for the design decision.

Rather than generating an executable application description for several partitioning and scheduling schemes with the use of SystemC, we analyzed application execution by hand C coding. By studying the JPEG coding algorithm, it was easily established that DCT is computationally the most intensive part of image processing. We decided to implement DCT in HW (VHDL) and the rest of application sequentially in SW (C). Considering our modest initial constraints, we were successful. However, despite straightforward partitioning scheme, it took us some time to hand write the necessary code. Any modification at the system level required from us a fair amount of tedious handwriting. The main drawback of the ad-hoc approach is that a lot of handwriting has to be done. Namely, not taking the entire system integrity (e.g. communication resource conflicts) into account makes the partitioning scheme inefficient. Solution to this problem is automatization of evaluating successively chosen design points.

6 Conclusion

We presented a HW/SW co-design methodology design flow based on the study of current research activities in this area and our experiences with an ad-hoc approach to partitioning and system level integration. With the presented ad-hoc approach drawbacks we highlighted features that we found particularly important. We proposed a seamless environment supporting system level development and automatization of repetitive tasks, and softened the solution to the issue of heterogeneity gap. The main idea is to reuse the already existent tools. Our future research effort will be towards blurring the gap caused by languages capable of describing heterogeneous capabilities.

Our future work will address the following two main issues. First, the persistent need of increasing the system complexity will widen the interest in IP-cores reusability. Our effort will be laid in finding an efficient way of IP libraries re-usage leveraged by user code development. IP libraries can consist of any of fine grain and coarse grain operators, encapsulating wrappers enabling automatic application subtasks connectivity, and communication channels. The second area of our future work will be towards optimizing specific parts of the design flow.

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Prispelo (Arrived): 11.02.2004 *Sprejeto (Accepted): 25.02.2004*

NEPORUŠNO TESTIRANJE PLANARNIH PARAMAGNETIKOV IN FEROMAGNETIKOV

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Kjučne besede: neporušno testiranje, vrtinčni toki, vrtilno magnetno polje, magnetna sonda, MKE, FLUX-2D;

Izvleček: Delo obravnava problematiko neporušnega testiranja električno prevodnih plošč z metodo vrtinčnih tokov. Metoda je osnovana na merjenju sprememb magnetnega polja induciranih vrtinčnih tokov v testirani plošči. Fizikalno, metoda neporušnega testiranja temelji na uporabi vrtilnega magnetnega polja. Posledično, se zaradi tega polja inducirajo vrtinčni toki v plošči in njihovo magnetno polje nad površino plošče vpliva na induciranje napetosti v iskalnih tuljavicah. Sprememba magnetnega polja vrtinčnih tokov nastane, ko poškodba plošče, bodisi razpoka bodisi korozijska razjeda, spremeni pot vrtinčnim tokom. Spremembo polja zaznamo s pomočjo iskalnih tuljav na površini plošče. Stanje preizkušane plošče tako ovrednotimo na način brezkontaktnega merjenja. Magnetne razmere pri testiranju z vrtinčnimi toki smo analizirali s pomočjo metode končnih elementov (MKE), ki jo podpira programski paket FLUX-2D /1/. S pomočjo modela magnetne sonde smo preiskovali vpliv lege in dimenzij utora v testirani plošči na inducirane napetosti 3-osnega iskalnega navitja. Ovrednotili smo merilne rezultate v smislu sposobnosti zaznavanja zarez in določanja njihovih smeri dveh tipov iskalnih navitij: 3-osnega iskalnega navitja in izvedbe s petimi z-osnimi iskalnimi tuljavicami. Teoretične izsledke smo testirali na aluminijasti in litoželezni plošči z vrezanimi zarezami.

Nondestructive Testing of Planar Paramagnetics and Ferromagnetics

Key words: non-destructive testing, eddy currents, rotational magnetic field, magnetic probe, FEM, FLUX-2D

Abstract: The paper reports the principle of eddy current non-destructive testing of conducting plates. The flow paths of eddy currents induced in the testing plate are perturbed by cracks and defects, and the result is reflected in the magnetic field above the plate surface. The change of the magnetic flux density can be measured by search coil which is in vicinity with a specimen. The advantage of this method is that the cracks and defects can be evaluated without contact in a short time.

Magnetic field distribution in electrically conductive plates was analysed with two-dimensional finite element method (FLUX-2D). The influence of the position and the size of a slot on output signals of the three-axis search coil were investigated. The relationship between the ability to consistently detect slots on one hand, and the electromagnetic properties of the specimen, the exciting frequency and the lift-off between the magnetic probe and the sample under test on the other hand have been estimated. The numerical results reveal the fundamental behaviour of magnetic probe. The prototype of the magnetic probe which generates rotational magnetic field in the testing plate was built-up. The mechanism of slot detection was elucidated. The results of this analysis show that output signals of the three-axis search coil include a lot of effective information of the direction and the position of a slot. Furthermore, experimental work has been carried out: the effects of the machined slots on aluminium and steel plate have been measured by the probe. In order to obtain better detection results of a slot, a set of five z-axis search coils was also used in the magnetic probe. Experimental results have proved that measurement system is useful in slot detection and recognition of slot direction.

1 Uvod

Potreba po učinkovitem avtomatiziranem neporušnem testiranju ima za seboj močno ekonomsko ozadje. Avtomatizirana inšpekcijska oprema odpravlja dolgotrajne postopke vizualnih pregledov (nalogo odločanja seveda prepušča človeku) in nekajkrat prekaša njihovo učinkovitost odkrivanja poškodb. Posebej pomembno pa je, da lahko z instrumentalnimi metodami detektiramo in ovrednotimo skrite poškodbe. Sem sodijo: skrite razpoke, skrite korozijske razjede ali nezveznosti v kompozitnih materialih /2/. Poleg višjega odstotka odkritih poškodb omogočajo instrumentalne metode tudi enostaven način njihovega dokumentiranja. Z analizo zbranih podatkov testiranja serije enakih izdelkov oz. naprav lahko določimo njihove najpogostejše poškodbe. Podatke o tipičnih poškodbah določenega izdelka lahko uporabimo pri iskanju boljših konstrukcijskih rešitev in proizvodnih procesov s katerimi poskušamo izboljšati poškodbam najbolj izpostavljene dele.

Izbira senzorja, ki določa metodo neporušnega testiranja, je ključnega pomena glede na vrsto okolja v katerega bo postavljen, saj lahko okolje dramatično vpliva na njegovo delovanje. Za preizkušanje sestavov iz prevodnih materialov se v zadnjem času vedno bolj uveljavlja metoda vrtinčnih tokov (ang. eddy current testing). Metoda je osnovana na merjenju sprememb magnetnega polja induciranih vrtinčnih tokov v testiranem objektu. Prednosti te metode so, da so senzorji vrtinčnih tokov neobčutljivi na umazanijo, prah, vlago, olje ali druge dielektrične materiale v razpokah, ki jih želimo oceniti /3/. Tako so ti senzorji primerni za delovanje tudi v okoljih z manj čistimi razmerami. Omogočajo tudi testiranje z veliko hitrostjo, zanesljivo delujejo v širokem temperaturnem razponu ter njihova izdelava je relativno poceni. Prednost je tudi njihova enostavna vključitev v računalniški merilni sistem. Širšo uporabnost metode testiranja na principu vrtinčnih tokov med drugim omejuje zahteva po enakomerni nalegi senzorja na površino testiranca. Tako težje preizkušamo objekte z zakrivljeno,

hrapavo ali kako drugače slabo dostopno površino. Nezanesljiva in tudi ekonomsko neupravičena je preiskava poškodovanosti predmeta zaradi splošne utrujenosti materiala.

2 Magnetna sonda

Pri neporušnem testiranju z vrtinčnimi toki skušamo v testiranem objektu doseči čim večjo gostoto induciranih tokov. V ta namen sta vzbujalna para navitij nameščena na feritnih jedrih, ki vzbujalno magnetno polje ojačita in ga usmerita v ploščo (slika 1). Med seboj pravokotno postavljena vzbujalna para navitij napajamo z za 90° fazno premaknjenima izmeničnima tokoma. V območju plošče pod sredino magnetne sonde se ustvari vrtilno magnetno polje. Le-to generira vrtinčne toke, ki se z njim sinhrono vrtijo. Poškodba plošče spremeni pot vrtinčnim tokom, kar se v zunanjosti plošče odraža kot sprememba magnetnega polja vrtinčnih tokov. To spremembo lahko zaznamo preko spremembe induciranih napetosti iskalnega navitja nad površino plošče. Na spodnji levi strani slike 1 je narisano 3-osno iskalno navitje: iskalne tuljavice so orientirane v smereh koordinatnih osi, tako da posamezna tuljavica zaznava le komponento magnetnega polja v smeri istoležne osi. Druga različica uporabljenega iskalnega navitja je prikazana na spodnji desni strani slike 1. To je set 5-ih z-osnih iskalnih navitij, ki detektirajo spremembe magnetnega pretoka pravokotno na površino plošče. Z analizo induciranih napetosti iskalnih navitji moremo določiti prisotnost in usmeritev razpoke v plošči.

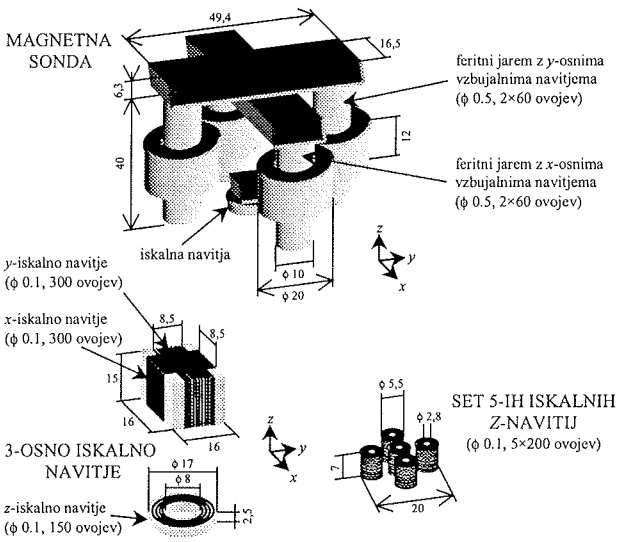
Uporaba vrtilnega magnetnega polja je ključnega pomena za učinkovitejše odkrivanje poškodb /4/.

Vrtinčne toke v preizkušani plošči lahko vzbudimo tudi z izmeničnim poljem. Vendar pa je detekcija napak v tem primeru slabša. Največja sprememba magnetnega polja in s tem tudi induciranih napetosti iskalnega navitja namreč nastane takrat, ko je smer razpoke pravokotna na smer vrtinčnih tokov. Razpoka v takšnem položaju ovira vrtinčne toke na območju cele svoje dolžine. Obratno pa velja za razpoke, ki so vzporedne s tokovnicami. Tako orientirane razpoke v mnogo manjši meri vplivajo na magnetno polje na območju iskalnih navitji. V primerjavi z izmeničnim poljem požene vrtilno magnetno polje vrtinčne toke v vseh smereh proti razpoki. Tako zagotovo pride do stanja, ko se prisotnost razpoke najmočneje odrazi.

Učinkovitost zaznavanja napak je odvisna tudi od frekvence vzbujalnega magnetnega polja. Večji odziv induciranih napetosti iskalnih navitji na poškodbo, ki leži na isti strani plošče kot magnetna sonda, dosežemo z višjo frekvenco vzbujanja. Pri tem se v plošči inducira večja gostota vrtinčnih tokov in posledično naraste tudi gostota magnetnega polja induciranih tokov na območju iskalnih navitji. Pri odkrivanju razpok na nasprotni strani plošče pa moramo biti pozorni na učinek izrivanja toka. Stopnja kožnega učinka je pogojena z vdorno globino /5/. Globina prodiranja δ je poleg snovnih konstant testiranca, to je specifične električne prevodnosti γ in permeabilnosti μ, odvisna še od električne krožne frekvence vzbujalnih tokov ω:

$$\delta = \sqrt{2/\omega\mu\gamma}\,. \qquad (1)$$

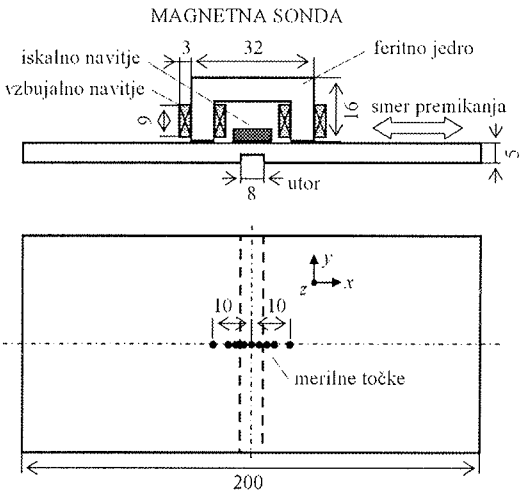
Zaradi opisanega učinka moramo uporabiti dovolj nizko frekvenco, da se tudi na nasprotni strani plošče inducira zadostna gostota vrtinčnih tokov. Zaradi manjše gostote induciranih tokov je razpoke na drugi strani plošče mnogo težje detektirati.



Slika 1: Konfiguracija magnetne sonde in iskalnih navitij

3 Dvodimenzionalna numerična analiza

S pomočjo dvodimenzionalne metode končnih elementov /6/ smo analizirali vpliv lege in velikosti utora (simulacija razpoke) na inducirano napetost v x, y in z tuljavici 3-osnega iskalnega navitija. Na sliki 2 je prikazana postavitev



Slika 2: Postavitev magnetne sonde, dimenzije testirane plošče in lege merilnih točk.

magnetne sonde, dimenzije testirane plošče in položaji merilnih točk (sondo smo premikali prečno na razpoko, to je od -10 mm do 10 mm glede na njeno središče).

Numerično analizo smo opravili pri sledečih razmerah: gostota vzbujalnega toka $2{,}2\times10^6$ A/m^2, relativna permeabilnost feritnega jedra 1000, preizkušali pa smo 5 mm debelo aluminijasto ploščo z relativno permeabilnostjo $\mu_{rAl}=1$ in specifično električno prevodnostjo $\gamma_{Al}=35{,}4\times10^6$ S/m ter enako debelo litoželezno ploščo relativne permeabilnosti $\mu_{rFe}=1000$ in specifične električne prevodnosti $\gamma_{Fe}=8\times10^6$ S/m. Rezultati analize, ki so predstavljeni na slikah 3, 4 in 5, veljajo za primer ko je utor širok 8 mm in globok 2 mm. S takim utorom smo simulirali stanje vrtilnega polja v plošči, ko inducirani vrtinčni toki tečejo prečno na utor. V takem primeru dobimo največji odziv induciranih napetosti v iskalnih tuljavah na prisotnost utora. Frekvenco napajanja smo prilagodili tako, da je globina prodiranja magnetnega polja (1) še presegala debelino plošče. Pri analizi aluminijaste plošče to pomeni napajanje frekvence 250 Hz, pri litoželezni plošči pa 1 Hz. Na sliki 3 so prikazani poteki induciranih napetosti v *x*- in *z*-iskalnem navitju pri različnih globinah utora na nasprotni (spodnji) strani aluminijaste plošče. Pri gibanju magnetne sonde čez utor doseže napetost U_{ix} največjo spremembo takrat, ko sonda leži nad sredino utora. Takrat je zaradi prisotnosti razpoke vpliv zmanjšanega polja vrtinčnih tokov na *x*-iskalno navitje največji. Pri inducirani napetosti *z*-osnega iskalnega navitja pa se središčni položaj sonde glede na utor odrazi ravno nasprotno. Inducirana napetost U_{iz} je v tem primeru enaka nič, kot v primeru plošče brez utora. V tej, simetrični legi *z*-tuljavice na razpoko se namreč izniči magnetni vpliv vrtinčnih tokov (magnetni pretok polja vrtinčnih tokov skozi *z*-navitje je enak nič). Inducirana napetost U_{iz} pa je odvisna le od magnetnega polja vrtinčnih tokov. Vzbujalno magnetno polje nanjo neposredno ne vpliva. Temu je tako, ker je *z*-osno navitje postavljeno na sredini med poloma jarma in je njena normala pravokotna na gostotnice vzbujalnega magnetnega polja.

Na sliki 4 so predstavljene napetosti iskalnih navitij pri analizi litoželezne plošče z utorom na spodnji strani.

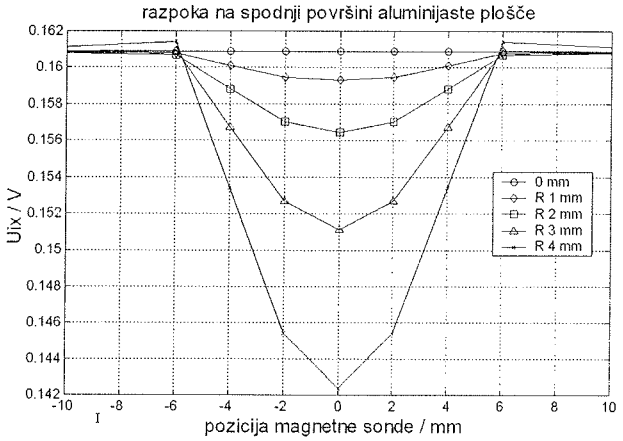
Zanimiva je primerjava potekov napetosti U_{ix} v primeru litoželezne in aluminijaste plošče (sliki 3.a in 4.a). Pri prehodu magnetne sonde čez utor v litoželezni plošči napetost U_{ix} naraste.

Porast napetosti je posledica stresanega vzbujalnega magnetnega polja čez utor. Pri plošči brez utora se magnetno polje v celoti zaključuje po plošči in ne pride do pojava stresanja polja. Zaradi tega je gostota magnetnega polja nad površino plošče na območju iskalnih navitij manjša kot v primeru plošče z utorom, posledično pa je manjša tudi inducirana napetost. Pri aluminijasti plošči pa je stresanje polja enako prisotno v primeru brez ali z utorom. Aluminij je namreč za magnetno polje enako sprejemljiv medij kot zrak. Ob prisotnosti utora se gostota magnetnega polja nad površino aluminijaste plošče zmanjša zaradi oslabljenega polja vrtinčnih tokov in inducirana napetost U_{ix} upade.

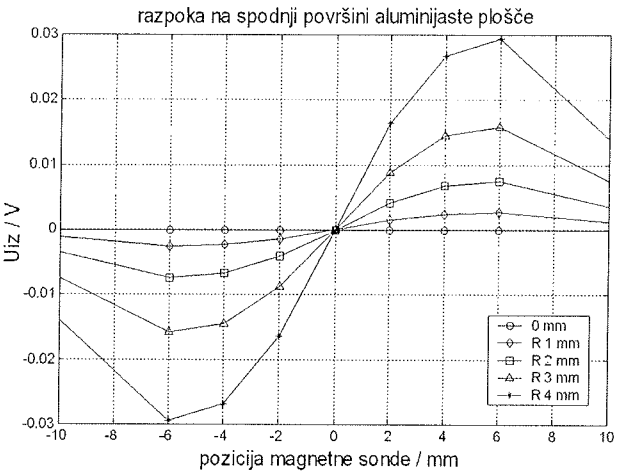
Odvisnost inducirane napetosti *z*-iskalnega navitja od lege utora se pri litoželezni plošči kaže na podoben način kot pri preizkušanju aluminijaste plošče. Napetost U_{iz} zavzame najmanjšo vrednost v položaju sonde nad sredino utora (slika 4.b).

3 Rezultati meritev

Merilni sistem je sestavljen iz treh glavnih sklopov: napajalne enote, magnetnega senzorja in sistema za zajem in obdelavo merilnih signalov. Omenjeni sklopi so podrobneje predstavljeni na sliki 5.



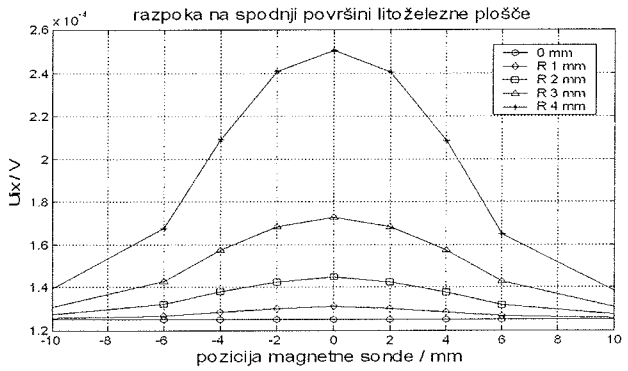
a)



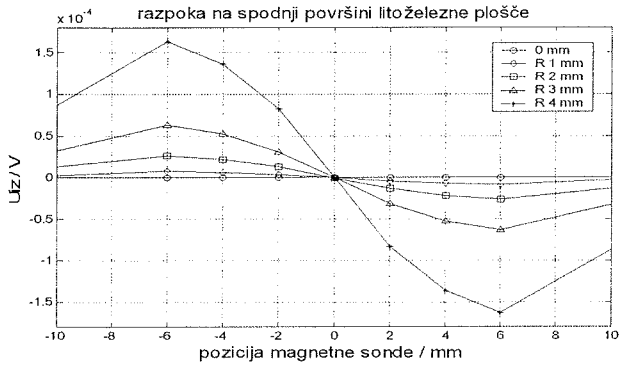
b)

Slika 3: Inducirana napetost v x- in z- iskalnem navitju glede na lego sonde in utora (razpoke) v aluminijasti plošči.

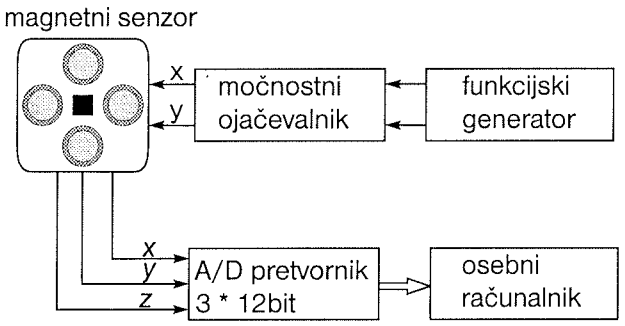
Sposobnost odkrivanja poškodb plošče s 3-osnim iskalnim navitjem in s setom 5-ih *z*-osnih iskalnih navitij smo preizkusili na različnih umetno "poškodovanih" vzorcih plošč in pri različnih merilnih pogojih. V 2 mm debelo aluminijasto ploščo velikosti 200×280 mm, relativne permeabilnosti $\mu_{rAl}=1$ in specifične električne prevodnosti $\gamma_{Al}=35\times10^6$ S/m, smo vrezali tri utore dolžine 100 mm in širine 4 mm. Utori globine 0.7 mm, 0.8 mm in 0.9 mm so enakomerno razporejeni na površini plošče. V litoželezno ploščo rela-



Slika 4a:Poteki inducirane napetosti v x- iskalnem navitju v odvisnosti od relativnega položaja magnetne sonde in utora (razpoke) v primeru litoželezne plošče.



Slika 4b:Poteki inducirane napetosti v z- iskalnem navitju v odvisnosti od relativnega položaja magnetne sonde in utora (razpoke) v primeru litoželezne plošče.



Slika 5: Merilni sistem.

tivne permeabilnosti $\mu_{rFe} \approx 1000$ in specifične električne prevodnosti $\gamma_{Fe} = 35 \times 10^6$ S/m ter dimenzij 200×420×3.15 mm pa smo vdelali pet zarez dolžine 110 mm ter širine in globine: 3.3×2 mm, 3.3×1.3 mm, 2.8×0.75 mm, 2.8×0.5 mm, 1.8×0.2 mm. Občutljivost 3-osnega navitja smo tudi preverili s prehodom čez 0.1 mm široko režo med dvema 2.35 mm debelima ploščama iz Al-Fe litine.

Za doseganje dobrih merilnih rezultatov je najbolj odločujoča frekvenca napajanja vzbujalnih tuljav. Najboljše rezultate pri odkrivanju utorov na isti strani aluminijaste plošče, kot je bila postavljena magnetna sonda, smo dosegli z napajanjem frekvence 3 kHz. Utore na spodnji strani plošče pa so se najjasneje "pokazale" pri frekvenci 1 kHz. Pri litoželezni plošči pa smo dobili dobre rezultate pri frekvenci 250 Hz, seveda pri testiranju plošče z zarezami na zgornji površini.

4.1. Rezultati testiranja s 3-osnim iskalnim navitjem

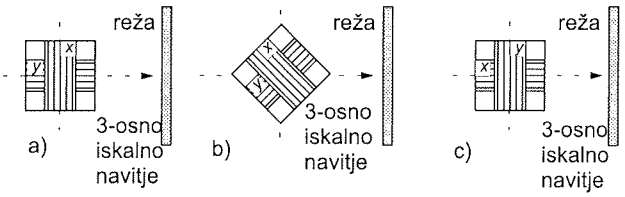
Prednost izvedbe 3-osnega iskalnega navitja je v tem, da lahko enostavno določimo smer reže (razpoke) iz razmerja signalov *x*- in *y*-iskalnega navitja. Na sliki 6 so prikazani trije možni prehodi *x*- in *y*-navitja čez režo:

a) *y*-iskalno navitje pravokotno prečka režo, *x*-navitje se giblje vzporedno proti njej,

b) obe navitji preideta režo pod kotom 45°,

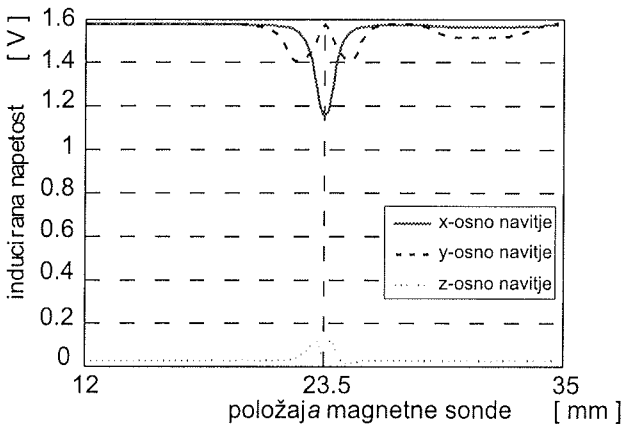
c) položaj navitij je ravno obraten kot v primeru a).

Glede na prej omenjene prehode iskalnih navitij čez režo dobimo tri značilne poteke induciranih napetosti (slika 7).

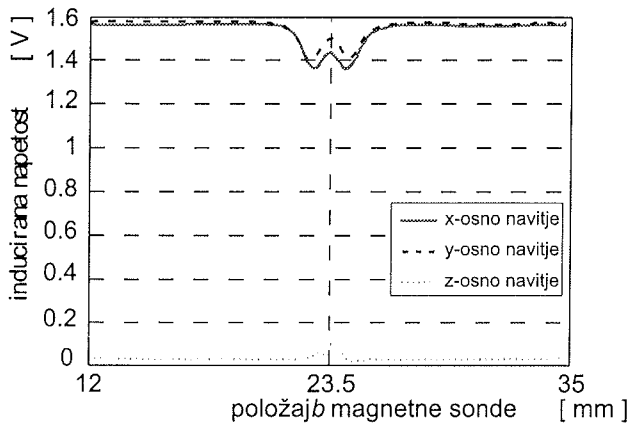


Slika 6: Prehodi x- in y-iskalnega navitja čez režo med dvema ploščama iz Al-Fe litine.

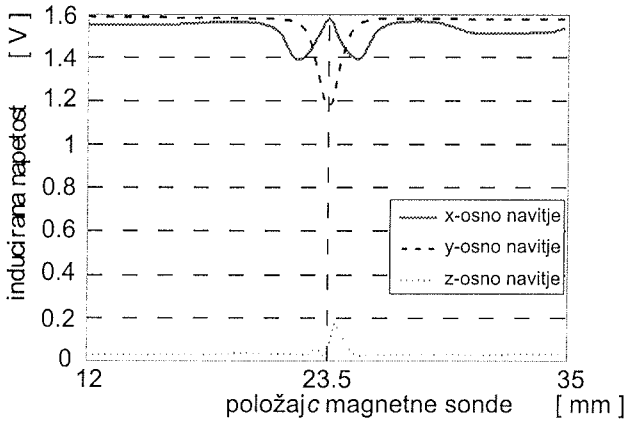
Inducirana napetost iskalnega navitja, ki se giblje pravokotno na smer reže, doseže najnižjo vrednost v legi navitja nad sredino reže. To velja za napetost *x*-navitja na sliki 7.a in napetost *y*-navitja na sliki 7.c. V tem položaju je merodajna komponenta gostote magnetnega polja vrtinčnih tokov



Slika 7a:Inducirane napetosti 3-osnega iskalnega navitja v položaju a (slika 6) glede na prehod čez režo med ploščama iz Al-Fe litine.



Slika 7b:Inducirane napetosti 3-osnega iskalnega navitja v položaju b *(slika 6) glede na prehod čez režo med ploščama iz Al-Fe litine.*



Slika 7c:Inducirane napetosti 3-osnega iskalnega navitja v položaju c *(slika 6) glede na prehod čez režo med ploščama iz Al-Fe litine.*

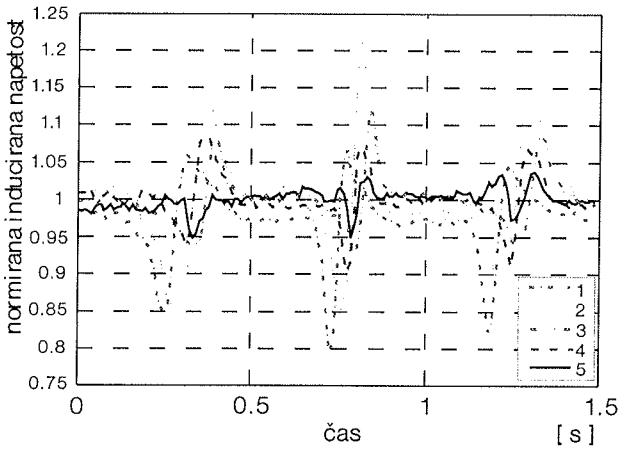
najmanjša zaradi netekočih vrtinčnih tokov na območju reže. V primeru diagonalnega prehoda iskalnegih navitji čez režo pa sta poteka induciranih napetosti *x*- in *y*-navitja enaka, slika 7.b. Velika razlika napetostnih nivojev signalov *x*- in *y*-navitja na eni in *z*-iskalnega navitja na drugi strani je posledica narave teh navitij. Večji del magnetnega pretoka, ki preide skozi *x*- in *y*-navitje, je stresani magnetni pretok med vzbujalnimi navitji. Od tod tako velika inducirana napetost na območju plošče brez reže. Simetrična lega *z*-tuljavice med jarmoma sonde pa vpliv vzbujalnega polja izniči, saj je normala na ravnino *z*-tuljavice pravokotna na gostotnice vzbujalnega magnetnega polja.

4.2. Rezultati testiranja s setom 5-ih *z*-osnih iskalnih navitij

Izvedba iskalnega navitja s petimi *z*-osnimi tuljavicami (slika 1) zelo dobro izpolnjuje prvenstveno funkcijo, to je detekcijo poškodb testirane plošče. Pri najustreznejši frekvenci napajanja je sprememba amplitude induciranih napetosti iskalnih navitij ob prehodu sonde čez utor tako izrazita, da lahko nedvoumno razpoznamo prisotnost utorov na zgornji in spodnji površini aluminijaste plošče. Iskalno navitje prav tako zanesljivo "odkrije" prve štiri najgloblje zareze na zgornji površini litoželezne plošče. Najmanjšo zarezo širine 1,8 mm in globine 0,2 mm pa zazna v 40% poizkusov.

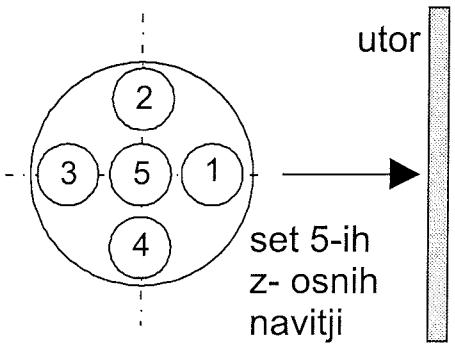
Pri odkrivanju smeri utorov (zarez) kot drugotni funkciji magnetnega senzorja s petimi *z*-osnimi iskalnimi navitji smo zabeležili slabše rezultate. Pravilno informacijo o smeri zarez smo dobili le v približno 20% primerov testiranja aluminijaste plošče. Pri preizkušanju litoželezne plošče pa je ta odstotek še manjši.

Krajevna razmeščenost iskalnih navitij nam omogoča, da lahko iz časovnega poteka signalov določimo smer utora ali zareze. V ta namen pri vsakem signalu določimo trenutek nastopa spremembe napetosti, ki označuje prehod iskalnega navitja čez utor ali zarezo. Trenutek prehoda smo določili s pomočjo ekstremov motnje. Tak način določanja trenutka prehoda iskalnega navitja čez razpoko je seveda uspešen le v primeru dobro izražene spremembe inducirane napetosti. Signale oštevilčenih iskalnih navitij nato razporedimo glede na čas nastanka motnje in s tem dobimo informacijo, v kakšnem vrstnem redu so navitja prešla zarezo. Primer razvrstitve signalov je prikazana na legendi slike 8. Signali so bili "posneti" pri testiranju aluminijaste plošče z utori na zgornji površini pri napajalnem toku 0.14 A, frekvence 3 kHz. Signale smo normirali z njihovimi povprečnimi vrednostmi z namenom, da lahko lažje preverimo pravilnost razporeditve. Na podlagi razporeditve signalov ugotovimo orientiranost razpoke (slika 9).

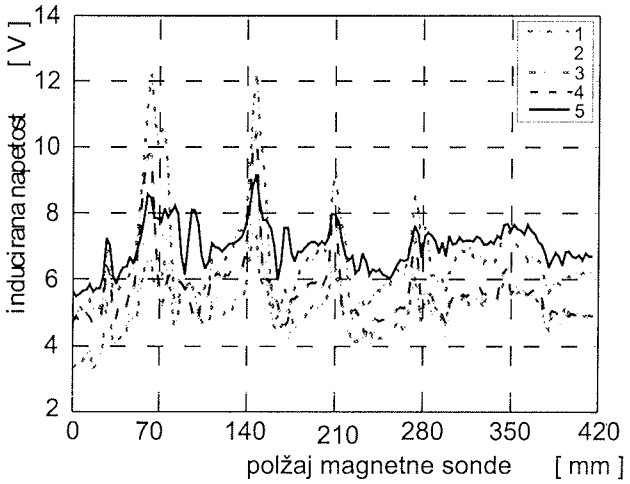


Slika 8: Razporeditev signalov glede na vrstni red prehoda iskalnih navitij čez utor v aluminjasti plošči.

Na sliki 10 so prikazani še poteki induciranih napetosti pri prehodu magnetne sonde čez zareze na zgornji površini litoželezne plošče. Inducirane napetosti smo posneli pri vzbujanju s tokovi 0.54 A, frekvence 250 Hz, ter jih zgladili z računanjem povprečnih vrednosti efektivne napetosti s korakom dveh period. Zaradi prevelikega vpliva stresanih magnetnih polj v okolici zarez nismo mogli določiti orientiranost le-teh glede na iskalna navitja. Medtem, ko so pris-



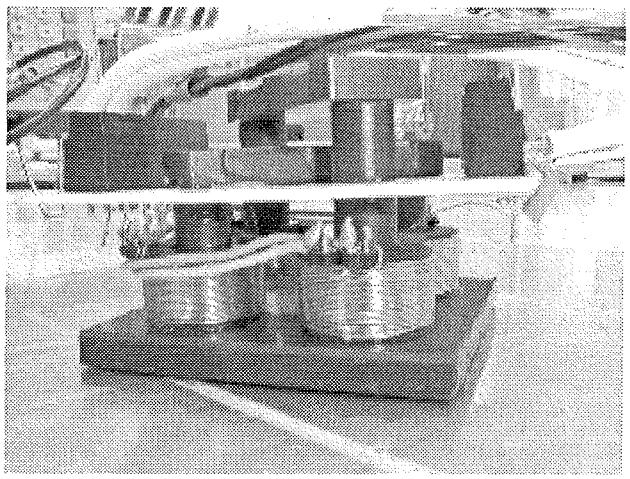
Slika 9: Konfiguracija iskalnih navitij pri prehodu sonde čez razpoko.



Slika 10: Inducirane napetosti seta 5-ih z-iskalnih navitij pri testiranju litoželezne plošče z zarezami na zgornji površini.

otnost in velikost zarez zelo izražena na obliki induciranih napetosti (slika 10).

Na sliki 11 si lahko ogledamo izdelano magnetno sondo.



Slika 11: Izdelana magnetna sonda.

5 Zaključek

S pomočjo metode končnih elementov (modeliranje s pomočjo programskega paketa FLUX-2D) smo analizirali magnetna dogajanja v magnetni sondi. Pri tem smo osrednjo pozornost namenili odzivu induciranih napetosti iskalnih navitij glede na lego in dimenzije utora testirane plošče. Rezultate teoretične analize smo zaokrožili z merilnimi rezultati izdelane magnetne sonde. Analizirali smo geometrijo vzbujalnega dela magnetnega senzorja. Vrtilno magnetno polje se je pokazalo za zelo učinkovito pri iskanju napak preiskušanca, saj lahko le z enoosnim premikom senzorja zaznamo prisotnost vseh možnih leg napak. Definirali smo odločujoči parameter za zagotavljanje kvalitetnih meritev, to je vrednost frekvence vzbujalnih tokov. Primerjava rezultatov meritev s 3-osnim iskalnim navitjem in setom 5-ih z-osnih iskalnih navitji je pokazala prednosti in slabosti posameznega merilnega sistema. Delo predstavlja tudi osnovo za nadaljnji razvoj magnetne sonde oz. merilnega sistema. Odprava pomanjkljivosti, ki so se pokazale pri praktičnem preizkušanju, pa zahteva celovitejši pristop k reševanju problematike metode testiranja z vrtinčnimi toki. Predvsem z namenom, da postane ta metoda zanesljivejša in učinkovitejša ter uporabniku prijaznejše "orodje" za vrednotenje stanja preizkušanega objekta.

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Prispelo (Arrived): 10.11.2003 *Sprejeto (Accepted): 25.02.2004*

TIME-OPTIMAL MAGNETIZATION OF INDUCTORS WITH PERMANENT MAGNET CORES

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Key words: magnetization processes, pulse magnetizing devices, permanent magnets, ferrites

Abstract: Time-optimal accurate magnetization process for small magnetic cores in mass-production is presented. The procedure consists of magnetization to the saturation level, followed by optimal partial demagnetization, which sets the stable operating point of a magnet within required inductance tolerance (< 3 %). The basic topology of a pulse magnetizer/demagnetizer is described and some improvements in algorithm to calculate optimal demagnetization voltage are suggested. Thus, proper magnetization of a core can be achieved in less than 4 s per piece. Additionally, the production waste is drastically reduced.

Časovno-optimalno magnetenje dušilk z jedrom iz trajnega magneta

Ključne besede: magnetilni postopki, impulzne magnetilne naprave, trajni magneti, feriti

Izvleček: V članku predstavljamo časovno-optimalni postopek natančnega magnetenja v velikoserijski proizvodnji majhnih magnetnih jeder. Postopek sestoji iz magnetenja do nasičenja, čemur sledi optimalno delno razmagnetenje, s čimer postavimo magnet v stabilno delovno točko. Pri tem dosežemo induktivnost dušilke, ki je znotraj predpisanih toleranc (< 3 %). Opisana je še osnovna topologija impulzne magnetilne/razmagnetilne naprave, prav tako pa je predlagan izboljšani algoritem za izračun optimalne razmagnetilne napetosti. S postopkom dosežemo želeno namagnetenost v manj kot 4 sekundah po kosu, pri čemer pa velja omeniti tudi znatno zmanjšanje izmeta.

1. Introduction

In this paper we will focus on accurate magnetization ("calibration") of the permanent magnet that is attached to a coil with soft-ferrite core in so-called "linearity corrector" (Fig. 1). The correctors are used for horizontal linearization of a picture in CRTs and TV sets, where the coil's desired inductance is selected by the dc current. The deviation in physical dimensions of ferrite correctors from the same manufacturing batch is up to 3 %, which results in an inductance variation of up to 23 %. To provide their equal performance in an application circuitry, it is more convenient to magnetize each single magnet to appropriate level in order to obtain magnet's desired effective height /1/. Namely, mechanical grinding would be inadequate for mass-production, because it is cost-and-time consuming.

Permanent magnet's desired operating point can be achieved by magnetization to the saturation level, followed by one or more consecutive partial demagnetizations, where gradually higher magnetic field strength is applied. Thus, stable magnetization is provided, i.e., during normal operation in an application circuitry, the magnet's operating point cannot be affected /2/. However, if eventually too high magnetic field strength is used for demagnetization, we cannot reach stable operating point by any partial magnetization. On the contrary, the magnet has to be magnetized to the saturation level again and thereafter demagnetized to the desired level by applying proper magnetic field strength.

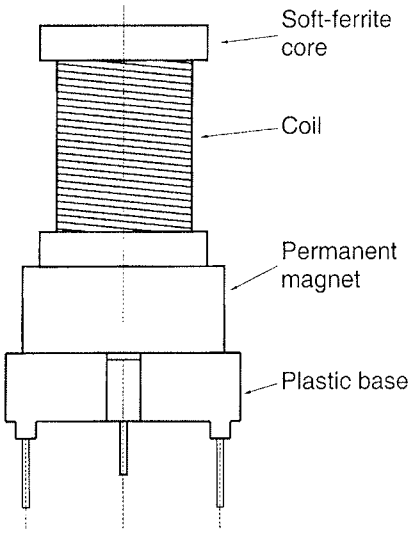

Fig. 1. Linearity corrector consists of a ferrite permanent magnet, attached to a coil.

Speed of described magnetization and demagnetization procedures is very important, since they have to be performed in the mass-production of linearity correctors. Therefore, the most suitable principle to magnetize and demagnetize such a permanent magnet, considering also the power consumption, is the pulse method /3/, /4/, where appropriate capacitor voltage is discharged on magnetizing/demagnetizing coil, into which the permanent magnet (corrector) is placed.

Fig. 2 shows the coil's inductance as a function of the dc control current through the coil. Calibrated correctors (with properly magnetized permanent magnets) should have the same characteristics, as close as possible to the "reference corrector" (left curve). The inductance limits are tightest in the reference point (with reference control current I_{c_ref}), where 5 % or even 3 % accuracy is required. On the other hand the relative limits are wider at no current (e.g. 10 %) or at higher current (e.g. 14 %). A characteristic for corrector with saturated permanent magnet is also shown (right curve) in order to illustrate, how the curve has to be moved to the "left" by partial demagnetization(s) after prior magnetization to the saturation level.

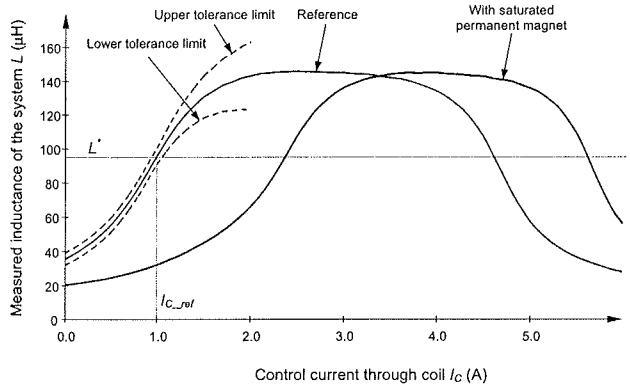

Fig. 2. Tolerance range for calibrated corrector and characteristic of the saturated corrector.

2. Magnetization Method

Permanent magnets can be magnetized to the desired level in many different ways. Under operating conditions it is important, that the magnetization is stable, i.e. that external magnetic fields do not affect the working point of the permanent magnet. This can be achieved by magnetization to the saturation level, followed by partial demagnetization. An operating point of permanent magnet is defined in an intersection between the magnetizing curve, that is specific to the material, and straight load line p_o, which represents the geometry of entire magnetic system (Fig. 3) /2/. When the permanent magnet is magnetized to the saturation level, the operating point is point 0 (H_o, B_o). An external demagnetizing force H_1 reduces flux density B to the point 1_D. After disengagement of this external field, flux density follows the curve 1^* (lower part of the recoil loop) and reaches the point 1 on the line p_o. Now only demagnetizing force H_2, which is stronger than previously applied H_1, can move the operating point by the curve 1^{**} (upper part of the recoil loop) and demagnetization curve to the point 2_D; after its disengagement the new operating point will be 2. Note that any partial magnetization cannot move the operating point upward the load line, i.e., from point 2 to point 1; full magnetization to the saturation level is required instead, followed by partial demagnetization, as described.

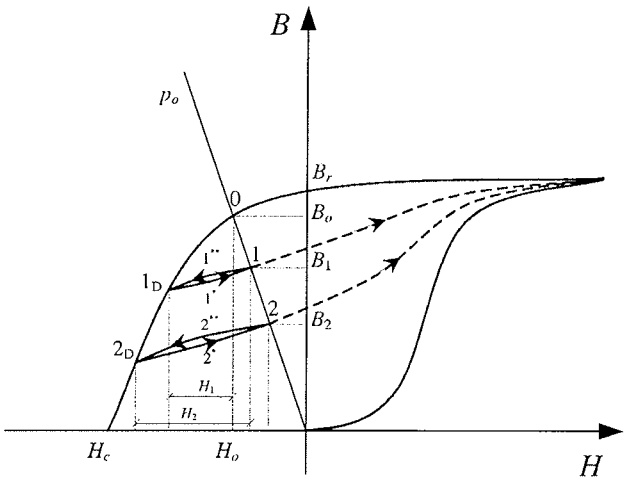

Fig. 3. (De-) magnetization curve and load line determine the operating point of a permanent magnet.

From the energetic point of view the most suitable principle to magnetize and demagnetize a permanent magnet is the pulse method. Magnetization can be achieved by the circuitry from Fig. 4, which releases energy, stored in "magnetizing" capacitor C_M, in an aperiodic current transient:

$$i_L(t) = \frac{U_{CM0}}{\omega L} e^{-\delta t} \sin(\omega t) \quad \text{for} \quad t \le \frac{T}{4} \tag{1}$$

$$i_L(t) = \frac{U_{CM0}}{\omega L} e^{-\delta \frac{T}{4}} e^{-\delta (t-\frac{T}{4})} \quad \text{for} \quad t > \frac{T}{4} \tag{2}$$

with

$$\omega_o^2 = \frac{1}{LC_M}, \qquad \delta = \frac{R}{2L}, \tag{3, 4}$$

$$\omega = \sqrt{\omega_o^2 - \delta^2}, \qquad T = \frac{2\pi}{\omega} \tag{5, 6}$$

When the "magnetizing" capacitor voltage is at its reference value U_{CM0}, charging is stopped and the charger is disconnected. Thyristor T_M is triggered, allowing the current i_L to flow through the magnetizing inductor L, in which the permanent magnet is placed, and the diode D. The aperiodic transient is shown in Fig. 5. Load current reaches its maximal value at $t = T/4$:

$$I_{L\max} = i_L(t = \frac{T}{4}) = \frac{U_{CM0}}{\omega L} e^{-\delta \frac{T}{4}} \tag{7}$$

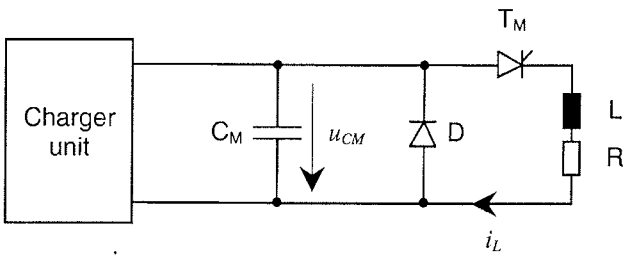

Fig. 4. Principal magnetization circuitry.

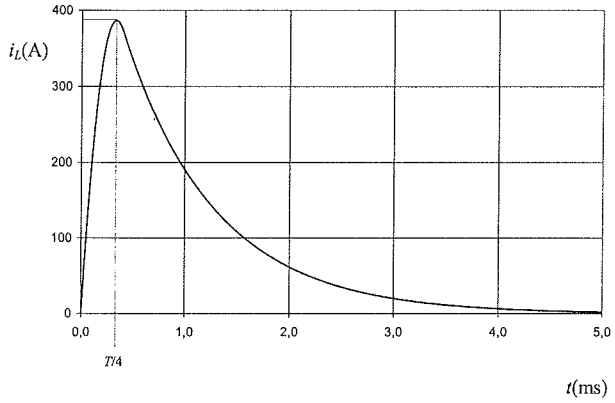

Fig. 5. Current pulse for magnetization

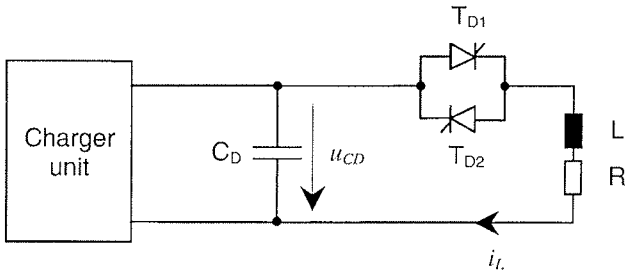

Fig. 6. Principal demagnetization circuitry.

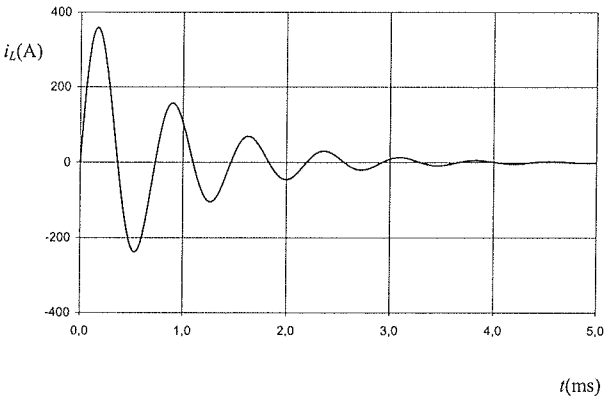

Fig. 7. Current pulse for demagnetization.

For demagnetization, dumped periodic transient can be used and applied by circuitry from Fig. 6. After charging the "demagnetizing" capacitor C_D to the desired value U_{CD0}, the charger is disconnected and thyristors T_{D1} and T_{D2} are triggered simultaneously, resulting in a current transient, shown in Fig. 7:

$$i_L(t) = \frac{U_{CD0}}{\omega L} e^{-\delta t} \sin(\omega t) \qquad (8)$$

The same charger unit can be utilized for both magnetization and demagnetization. Due to the process requirement, that the magnetization must always reach the saturation level, while the demagnetization should be executed partially and more precisely, it is reasonable to use two separate capacitors. Namely, the energy, stored in a capacitor, is controlled through its voltage. Therefore the capacitor with lower capacitance can store the same amount of energy at higher voltage, thus enabling wider voltage range with better precision. Consequently, frequencies and time constants (3, 5, 6) are different for demagnetization, where capacitance C_D has to be considered before applying their values in (8). Magnetizing inductor is nevertheless the same for both actions.

3. Time-optimal magnetization procedure

From Fig. 8 it is evident, that magnetic properties of magnets, made of the same material and with the same required dimensions, can differ significantly. Demagnetization curves for several linearity correctors of the same type were measured through pulse demagnetization. Magnets were magnetized to the saturation level and then gradually demagnetized by increasing the applied capacitor voltage. As it can be seen, the reference inductance L^* can be achieved by applying very different demagnetization voltages. Obviously the capacitor voltage, that would properly demagnetize the particular permanent magnet, has to be determined for each single piece separately.

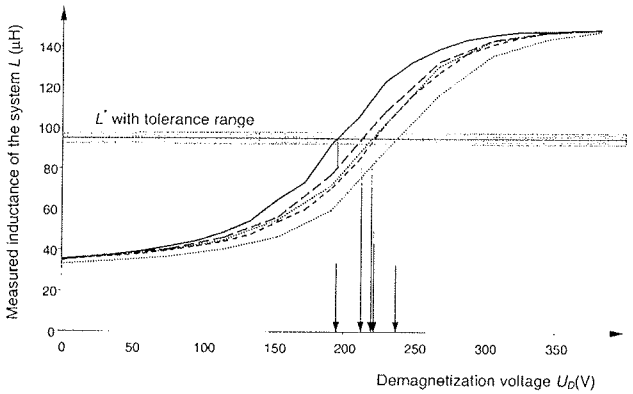

Fig. 8. Demagnetization characteristics for several permanent magnets of the same type.

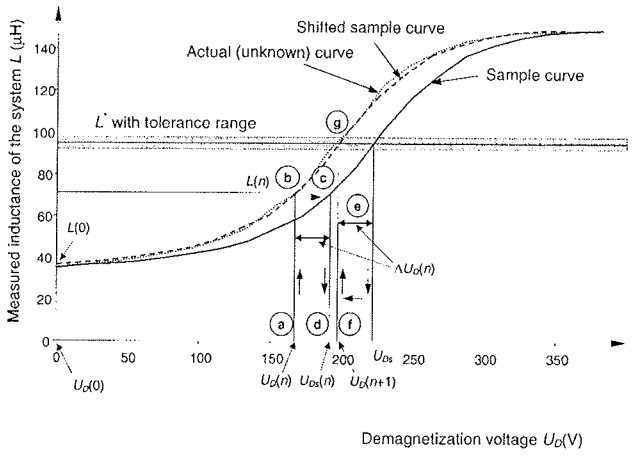

Fig. 9. Determination of demagnetization voltage.

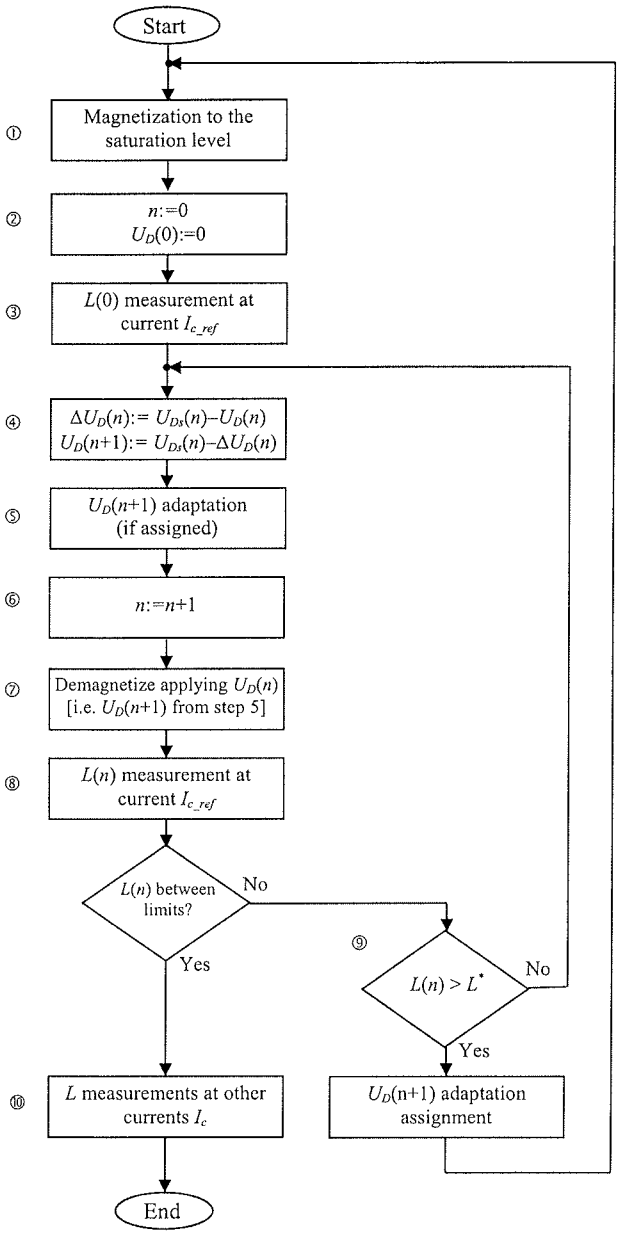

Fig. 10. Basic steps of magnetization procedure.

It is possible to achieve the reference inductance L^* through several consecutive demagnetizations, starting from saturated magnet, by increasing the capacitor voltage in small steps. But this would result in numerous demagnetization steps, which would require too much time. Ideally, there should be only one demagnetization step, since the speed is paramount.

To provide an optimal number of demagnetization steps, it is reasonable to measure the demagnetization curve for a sample (or an average curve for several samples), which is selected randomly among the magnets from the same batch. The form of this sample curve is then used to determine suitable demagnetization voltages for all individual magnets from the batch. The recursive principle is explained in Fig. 9 and Fig. 10, as follows: After the magnet is beforehand magnetized to the saturation and then partially demagnetized by demagnetization voltage $U_D(n)$ (sign a in Fig. 9, step 7 in Fig. 10), its inductance $L(n)$ is measured (sign b, step 8) and its approximate relation to the sample curve can be established accordingly. Unknown demagnetization curve can be treated like a shifted sample curve (dashed), with the shift being estimated from the measured inductance of a magnet. Namely, the sample demagnetization curve reaches the same measured inductance $L(n)$ (sign c) at demagnetization voltage $U_{Ds}(n)$ (sign d), which is for $\Delta U_D(n)$ higher than the voltage $U_D(n)$. The same voltage difference $\Delta U_D(n)$ can be assumed at the reference inductance (sign e), i.e., the voltage, that has to be applied to this magnet, is for $\Delta U_D(n)$ lower than the voltage U_{Ds}, which provided demagnetization of the sample in order to reach the reference inductance L^* at reference control current I_{C_ref}. The new demagnetization voltage, which can provide proper demagnetization of this magnet, is now $U_D(n+1)$ (sign f in Fig. 9, step 4 in Fig. 10). Although the actual curve does not match the "shifted" sample curve entirely, the inductance after the demagnetization with voltage $U_D(n+1)$ would be set within required limits (sign g).

The most important is the demagnetization voltage $U_D(n) = U_D(1)$, which has to be applied for first demagnetization step. In the best case, this demagnetization should result with an inductance within tolerances of its reference value. Therefore, the above-described principle could be used directly after the magnetization to the saturation level (step 1 in Fig. 10); in this case the demagnetization voltage $U_D(n) = U_D(0)$ that is used in further calculation, is zero (step 2), i.e., only inductance $L(0)$ after magnetization is measured (step 3). This approach gives excellent performance on magnets whose characteristics are close enough to the measured sample curve, because only one demagnetization is needed. In practice this condition cannot be assured, so undesired excessive demagnetizations can appear, i.e. the inductance L can exceed its reference value L^*. Consequently, new magnetization is needed, but with some magnetizing devices, which require longer time to charge magnetizing capacitor, this has to be avoided. The solution towards is to apply 75 % of voltage U_{Ds} for the first demagnetization, (step 5 in Fig. 10) thus avoiding the excessive demagnetizations for the expected range of magnets.

4. Conclusion

The magnetizing procedure, described in this paper, was applied in mass production of linearity correctors with very good results. The obtained total time for the magnetization to the reference point was bellow 4 s. Beside the improved accuracy of the magnet's operating point, the production waste was significantly reduced.

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Prispelo (Arrived): 14.11.2003 *Sprejeto (Accepted): 25.02.2004*

A PRECISION HYBRID AMPLIFIER FOR VOLTAGE CALIBRATION SYSTEMS

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Key words: voltage amplifier, hybrid power amplifier, feedforward-feedback, high efficiency, harmonic distortion

Abstract: The paper describes a voltage amplifier that is capable of accurate amplifying voltages up to 300 V rms within the frequency range from 40 Hz to 70 Hz with or without the presence of higher harmonic components up to 1.4 kHz. Its sophisticated topology consists of a supreme linear amplifier and an inner hybrid power amplifier with an output transformer. The hybrid power amplifier, which acts as a self-oscillating system, is based on a parallel connection of a superior three-stage class AB linear power amplifier and a switch-mode inverter. The latter provides a full load current while the former filters the waveform ripple. In this way a power efficient system is obtained whose efficiency at a nominal output power of 60 VA exceeds 90%. The experimental results demonstrate good performance of the proposed hybrid topology.

Precizijski hibridni ojačevalnik za napetostne kalibracijske sisteme

Kjučne besede: napetostni ojačevalnik, hibridni močnostni ojačevalnik, visok izkoristek, nelinearno popačenje

Izvleček: V članku je predstavljen napetostni ojačevalnik za precizijsko ojačevanje napetosti do 300 V efektivne vrednosti na frekvenčnem območju od 40 Hz do 70 Hz z možnostjo superponiranja višjeharmonskih komponent do 1.4 kHz. Celotna topologija je zgrajena okoli hibridnega močnostnega ojačevalnika z izhodnim, večodcepnim transformatorjem. Slednji narekuje uporabo notranje regulacijske zanke za odpravljanje parazitne enosmerne komponente napetosti. Hibridni močnostni ojačevalnik, ki deluje kot lastno-oscilirajoči sistem, sestavljata paralelno vezana linearni močnostni ojačevalnik in stikalni inverter. Takšen moderen koncept zagotavlja, da izkoristek pri nazivni izhodni moči 60 VA preseže 90%, kajti celoten bremenski tok zagotavlja inverter. Linearni ojačevalnik skrbi le za odpravljanje visokofrekvenčne valovitosti. Za linearizacijo odziva celotnega vezja je dodana zunanja regulacijska zanka s »feedforward-feedback« principom povratne zanke. Posledica tega je majhno nelinearno popačenje izhodne napetosti. Poleg tega eksperimentalni rezultati dokazujejo stabilno kratkotrajno delovanje ojačevalnika, ter odlično obnašanje tudi v primeru, ko ga obremenimo z nelinearnim, pretežno kapacitivnim bremenom.

1. Introduction

Over the past two decades an extensive growth in the number of nonlinear loads, such as rectifiers in electronic equipment, and a rapid development of the static power converters have been noticed. Because of the nonsinusoidal waveform of the current, which they draw from the grid, and the grid impedance, which is not zero, the voltage waveform at the end user differs from the sinusoidal one. Besides other undesirable phenomena, performing voltage measurements in presence of harmonics is also quite a task. However, they are not only the voltage meters but also wattmeters and energy meters that are exposed to the distorted environments. Especially the last ones are the most widespread. To assure the ability of accurate measurement in distorted conditions, treated meters must be calibrated at the end of manufacturing process and periodically, after they are put in use. This demands special equipment, which is capable of performing the harmonics analysis.

The focus of this paper is a precision voltage amplifier designed for a portable three-phase power calibrator. The calibrator is used to calibrate three-phase energy meters in the phantom load test arrangement with the fundamental power and also with harmonics power components added in accordance with the International Standard /1/. Besides three voltage amplifiers, three current amplifiers are needed. The voltage amplifier for one phase should provide maximum power of 60 VA within the voltage range from 30 V to 300 V rms. Moreover, the output waveform should also be accurate in amplitude (±0.2%) and phase (±0.1°). Within the frequency range from 40 Hz to 70 Hz its distortion (THD) should not exceed 0.5%. To allow for a harmonics analysis of the unit under test, the amplifier has to amplify a frequency spectrum up to 1.4 kHz. The magnitude of the first four higher harmonics should measure up to 50% and the rest of the harmonics up to 10% of the voltage magnitude at the fundamental frequency.

Till now, such stringent demands have been efficiently solved using only the linear power amplifiers /2/. Their main disadvantage is low efficiency, which leads to excessive power losses for which reason an efficient cooling system is required. This may result in an unacceptable contribution to the volume and mass of the portable calibrator.

To meet the above requirements, an advanced topology combining a switch-mode and linear technique was developed. Such concept was first applied in low voltage audio power amplifiers /3, 4/.

2. Description of the proposed topology

The overall diagram of the precision voltage amplifier is shown in Fig. 1. The key element of the topology is the hybrid power amplifier (HPA) having its output connected to the primary winding of the transformer. By means of a local voltage feedback loop, HPA controls the voltage of the transformer primary to be the exact template of the signal applied on the noninverting input of HPA. The secondary of the transformer has three taps. In this way the operation of the voltage amplifier is split into three ranges. Output voltage u_o, which is the voltage on the secondary of the transformer, is controlled by a supreme voltage control loop. In order to obtain stable operation, the feedforward-feedback principle is followed.

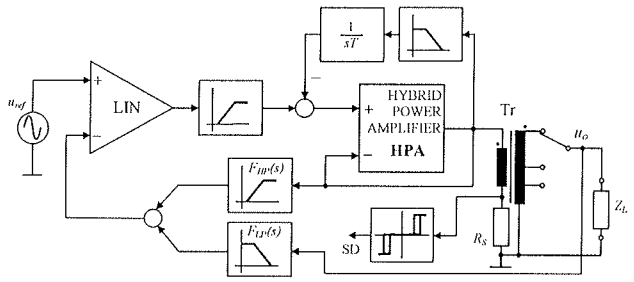

Fig. 1: Overall diagram of the precision voltage amplifier

2.1 Hybrid power amplifier

HPA is composed of a three-stage class AB linear power amplifier (LPA) /5/ and a switch mode inverter. They are connected in parallel as shown in Fig. 2. In this configuration LPA plays the leading role because it directly controls the voltage at the output of HPA. The inverter can be treated as a slave since its control signals are derived from the output current of LPA.

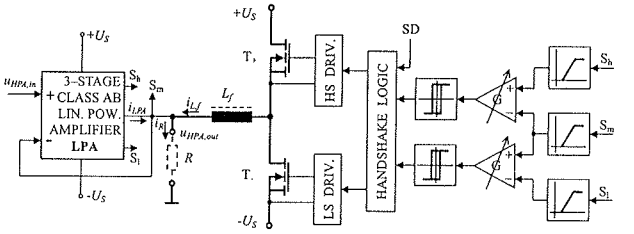

Fig. 2: Block diagram of the hybrid power amplifier

If we assume that T_+ is turned on (conducting) and T_- is turned off, the current through inductor L_f increases. Depending on the output voltage of HPA $u_{HPA,out}$ and load resistance R, part of it flows into the load and the rest sinks into LPA. When a certain value of the latter ($-I_{tr}$) is reached, we turn T_+ off and T_- on. The current through L_f decreases. After a while it becomes smaller than the load current and LPA starts to deliver the deficit. At the value $+I_{tr}$, we again turn T_+ on and T_- off. The self-oscillating system is thus obtained. Its frequency f_{so} is defined by

$$f_{so} = \frac{U_S^2 - \left(u_{HPA,out} + \frac{L_f}{R}\cdot\frac{du_{HPA,out}}{dt}\right)^2}{4\cdot I_{tr}\cdot L_f\cdot U_S}. \qquad (1)$$

The inverter can supply most of the load current as long as the slew rate of the load current is smaller than the slew rate of the inductor current. The inverter power bandwidth PB_{inv}, this is the highest frequency of $u_{HPA,out}$ at which the upper condition still holds, is

$$PB_{inv} = \frac{R}{2\pi L_f}\cdot\sqrt{\frac{1}{\left(U_{HPA,out}/U_S\right)^2}-1}, \qquad (2)$$

where $U_{HPA,out}$ is the amplitude of the output voltage and U_S is the supply voltage.

The LPA current is sensed as a voltage drop across the emitter resistors in the LPA output stage. The signals (S_h, S_m, S_l) are then led through high-pass filters (Fig. 2) in order to block the low frequency content that belongs to the amplified signal. It is important that the crossover frequencies of the aforementioned filters are matched. If they are not, the load current i_R and the inverter current $i_{L,f}$ are out of phase. In this case LPA not only filters the switching frequency current ripple but also delivers part of the fundamental and higher harmonics components of the load current. The differential amplifiers with an adjustable gain adapt the signals to the threshold levels of the Schmitt-triggers. These signals are further processed inside the handshake logic in a digital way. An interlock delay between the switching maneuvers of transistors is generated here. Optional blocking of the inverter is also possible by an external signal SD.

2.2 Suppressing the parasitic dc component

The voltage error, being the result of asymmetry and nonlinearities inside LPA, can lead to a considerable dc voltage component at the HPA output. If such dc component were applied to the output transformer, its magnetic core would become saturated and operation of the circuit would be unreliable or even impossible.

In order to cope with the above problem, two methods were investigated. The first addressed the use of an additional dc voltage sensor in the form of a differential transformer with an extracting circuit as proposed in /6/. Because of its complexness and high cost, the solution was not accepted. An autonulling control circuit was applied instead.

It consists of a low-pass first order filter and an integrator (Fig. 1). The latter integrates the output of the filter, where the low frequency content is present including the dc component. The result is then subtracted from the signal of the supreme control loop. The voltage drop, resulting from the dc current through the transformer primary winding, is relatively small because the resistance of the winding is small, too. Better performance of the autonulling circuit can be achieved by applying a higher voltage drop for the same value of the dc current. Hence a resistor with a small resistance (R_S = 0.1 Ω) is added in series with the transformer primary winding. Its impact on the overall efficiency can be neglected. A high-pass filter, positioned right after the superior amplifier, assures an autonomous operation of the autonulling circuit.

2.3 Supreme feedforward-feedback control loop

The use of a superior linear amplifier and a supreme control loop is of a paramount importance in providing a linear response of the system. The output voltage u_o of the amplifier is measured with a precision noninductive film resistor divider. The high frequency response of the measured voltage is attenuated as a result of its passing through the transformer. If we want to obtain a stable operation of the supreme loop, accurate information about the high frequency response in the feedback should be made available. This can be done by using the feedforward path from the output of HPA and thus bypassing the transformer. The feedforward-feedback network should have a transfer function $F_F(s)$ that can be written as

$$F_F(s) = F_{LP}(s) + F_{HP}(s) = 1. \tag{3}$$

In other words, the constant-voltage condition must be fulfilled. This can only be achieved by using the first order low-pass $F_{LP}(s)$ and high-pass $F_{HP}(s)$ filters with matched crossover frequencies. Equation (3) can be written as

$$F_F(s) = \frac{1}{1 + s/\omega_{LP}} + \frac{s/\omega_{HP}}{1 + s/\omega_{HP}} \tag{4}$$

and finally with regard to $\omega_{LP} = \omega_{HP} = \omega$,

$$F_F(s) = \frac{1}{1 + s/\omega} + \frac{s/\omega}{1 + s/\omega} = \frac{1 + s/\omega}{1 + s/\omega} = 1. \tag{5}$$

The crossover frequency has to be high enough to avoid any remarkable impact on the linearity of the supreme control loop for the reason of the nonideality of the transformer.

3. HPA efficiency enhancement

Practically all power losses of the hybrid voltage amplifier have their origin inside the hybrid power amplifier or more precisely inside the output stages of LPA and inverter. If a power efficient system with low *THD* is to be obtained, an adequate ratio between the quiescent current of LPA and the threshold current I_{tr} has to be chosen. An additional guidance for the design is the condition that the minimum switching frequency of HPA must be beyond the perceptibility of the human ear, which is about 20 kHz. Considering the maximum loading of HPA, the minimum switching frequency and the threshold current I_{tr} = 100 mA, the inductance L_f = 1 mH is obtained. This results in the inverter power bandwidth (2) much higher than the frequencies of the amplified voltage and enables the inverter to provide most of the load current. To have evidence of this, we need some parameters that are given below.

The class AB linear power amplifier is designed to withstand the highest amplitude of its output voltage of 45 V at the supply voltage of ±50 V. The quiescent current through the output power transistors is set to 25 mA. Under these conditions the saturation and the clipping are eliminated. Though the quiescent current of a relatively small value generates small quiescent power losses, it is large enough to minimize the crossover and switching distortion. The power losses of HPA at a low output current are higher compared to the LPA losses alone. Because of this the hysteresis element is used to form the control signal SD. The inverter is enabled only when the current through the primary of the transformer exceeds 120 mA. When it falls under 100 mA, the inverter is disabled again.

The whole range of the voltage amplifier operation is split into three subranges with the nominal voltages of 75 V, 150 V and 300 V. However, the output power of 60 VA is to be provided in each subrange. When connected with the aforementioned solution, this solution leads to a higher efficiency of LPA due to the longer operation with the output voltage swing closer to $\pm U_S$ provided the desired output voltage is amplified within an appropriate voltage range.

Since the hybrid topology is an efficient exchange for the pure linear topology, it is reasonable to compare their efficiencies. Evaluation will be done in particular working points where extreme values are expected. The first point is at maximum output power P_R = 60 W and voltage amplitude $U_{HPA,out}$ = 45 V. Under these conditions HPA supplies the load R = 16.88 Ω. To answer the question what would be the efficiency if at this working point the inverter were disabled, we have to determine power losses on the power transistors in the output stage of LPA. Power losses P_T on the upper transistor are generated as a consequence of the voltage difference between the supply voltage $+U_S$ and the output voltage of HPA

$$u_{HPA,out} = U_{HPA,out} \cdot \sin\Theta \tag{6}$$

and the current through the load

$$i_R = \frac{u_{HPA,out}}{R} = \frac{U_{HPA,out}}{R} \cdot \sin\Theta. \tag{7}$$

As the ratio between the amplitude of the load current I_R and the quiescent current is very high (2.67 A : 25 mA), the quiescent current can be neglected. Calculation of P_T

can be done in the same way as for the class B amplifier where each transistor conducts only half of the period

$$P_T = \frac{1}{2\pi}\int_0^{\pi}\left\{\frac{u_{HPA,out}}{R}\cdot\sin\Theta\cdot\left(U_S - U_{HPA,out}\cdot\sin\Theta\right)\right\}\cdot d\Theta. \quad (8)$$

The efficiency is defined by

$$\eta = \frac{P_R}{P_R + 2P_T} \quad (9)$$

and for the assumed conditions amounts to 70%. In other words, for 60 W of the output power 25 W are dissipated inside the linear amplifier.

An accurate calculation of the efficiency for the hybrid topology is difficult to perform because power losses of the inverter are hard to be determined exactly. Although the conductive losses and the choke losses are known, the calculation of the switching losses is almost impossible because of the variable switching frequency (1) inside the period of the output voltage. Our evaluation will therefore be based on the assumption that the efficiency of the inverter h_{inv} is 95%. This value can be obtained if we use high-speed switching transistors with low $R_{DS,ON} \leq 0.18\ \Omega$ and the choke with a low loss ferrite core. Furthermore, in this topology of the inverter only one transistor is in series with the load at a time. This is not the case with the bridge topology where two transistors are in series. LPA now only filters the high frequency ripple and its output current is of a triangular shape with the peak value of I_{tr}. The shape of the current through the transistor in the output stage of LPA is of a triangular shape, too, but it has two slopes because of the quiescent current. Its average value $I_{T,av}$ is 31.25 mA. In this case power losses on the upper transistor are defined by

$$P_T = \frac{1}{2\pi}\int_0^{2\pi}\left\{I_{T,av}\cdot\left(U_S - U_{HPA,out}\cdot\sin\Theta\right)\right\}d\Theta \quad (10)$$

and the overall efficiency by

$$\eta = \frac{P_R}{P_R/\eta_{inv} + 2P_T}. \quad (11)$$

Thus the calculated dissipated power of LPA and the overall efficiency are 3.1 W and 90.5%, respectively.

The second working point worth the while of being considered is in the situation when the voltage at the voltage amplifier output is the lowest possible (30 V rms). For R = 16.88 Ω, HPA has to deliver 9.6 W at an 18 V peak. The overall efficiency is more than 72% while that of LPA alone is some 28%.

Compared to the linear amplifier, the essential advantage of the hybrid voltage amplifier are low power losses in case of reactive load. For the 60 VA reactive power LPA would dissipate more than 65 W, while HPA dissipates ten times less.

When the amplifier is in the idle state, the reference signal and the output voltage are zero. The power dissipated by LPA is 3.1 W when the inverter is enabled. With the inverter disabled, only 2.5 W are dissipated. When the amplifier is unloaded, losses are the same regardless of the output voltage. Moreover, disabling the inverter at low output currents abolishes the switching noise.

4. Experimental results

The performance of the precision hybrid voltage amplifier was tested under various conditions. A special attention was particularly paid to the determination of *THD*, voltage error and phase error. Fig. 3 shows the voltage error and the phase error versus frequency of the amplifier within the 300 V range. The magnitude of the output voltage inside the frequency ranges was set according to the foreseen target values. The amplifier was loaded with a 6600 Ω resistor. Our measurements were made with a dynamic signal analyzer (DSA) HP 35665A. The performance of the amplifier within the ranges of 75 V and 150 V is better than at the 300 V range.

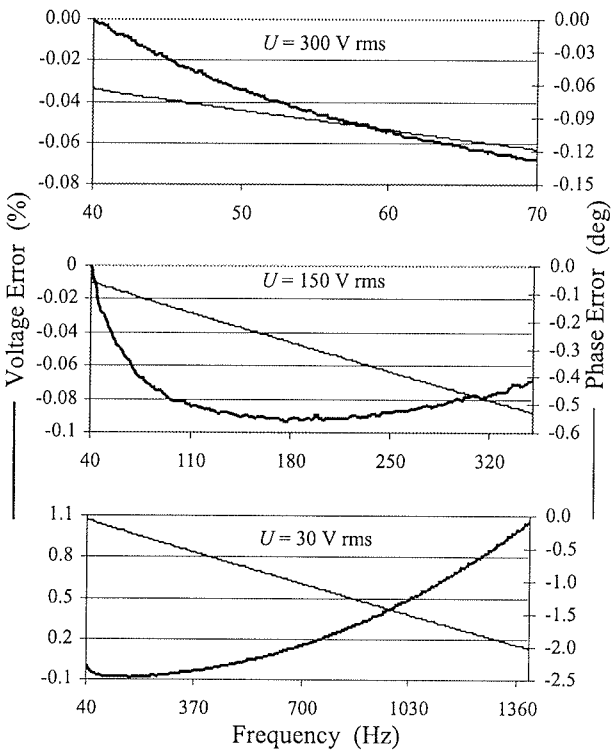

Fig.3: Voltage and phase error versus frequency

Short-term stability of the amplifier was measured after a warm-up period using an automatic measuring system consisting of PC with a LabWIEV™ software and a digital multimeter (DMM) HP 34401A. Rms voltage readings were recorded at 30 s intervals over a five-hour period. The results are presented in Fig. 4. The amplifier was loaded within a particular voltage range with resistive loads as noted in Table 1. According to the DMM specifications, the meas-

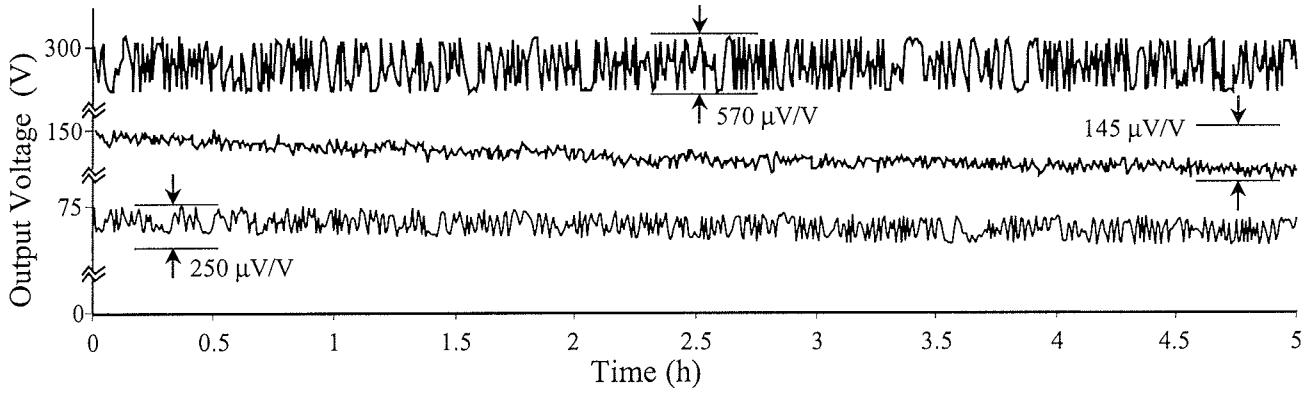

Fig. 4: Short-term stability

uring uncertainties for 300 V, 150 V and 75 V were 0.09%, 0.14% and 0.07%, respectively.

THD of the amplifier was measured using a digital low distortion sine wave generator and DSA. Values for certain set points within the different voltage ranges are shown in Table 1. All the measurements were made at 50 Hz and a spectrum containing 30 higher harmonics was observed.

Table 1: THD of the precision voltage amplifier

f = 50 Hz N = 30	**75 V range** R_L = 560 Ω			**150 V range** R_L = 2100 Ω			**300 V range** R_L = 6600 Ω			
U (V)	25	50	75	75	100	150	150	200	250	300
THD (%)	0.05	0.025	0.015	0.028	0.023	0.015	0.025	0.017	0.015	0.013

In order to test the performance of the amplifier under nonlinear load conditions, an electronic energy meter was applied to its output. *THD* of the voltage and current shown in Fig. 5 is 0.11% and 16%, respectively. The current is heavily distorted because of the rectifier and dc-dc converter, which are used as a power supply for the electronic circuits inside the energy meter. Although the load is of a capacitive nature, the stability of the amplifier is not impaired.

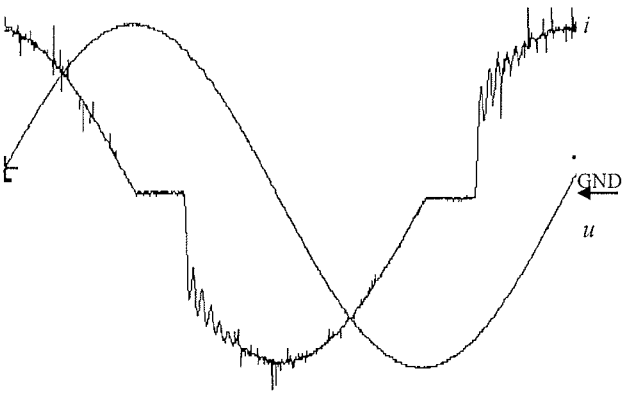

Fig. 5: Output voltage and load current (k_u = 100 V/div, k_i = 20 mA/div, k_t = 2 ms/div)

5. Conclusion

A precision hybrid voltage amplifier is presented. By means of a novel topology combining linear and switching techniques, upgraded by a supreme feedforward-feedback control loop, a power efficient system with low output voltage distortion is obtained. Owing to the use of the output transformer, the output voltage is free of the dc component. This is extremely advantageous when calibrating meters, which contain input voltage transformers.

As expected, the amplifier meets the amplitude inaccuracy and *THD* specifications. It is only the phase error that slightly exceeds the limit value when approaching the frequency of 70 Hz. This can be compensated by a voltage reference generator. Since the long-term inaccuracy depends only on the absolute stability of very few components in the supreme feedback circuit, it is expected that it will not exceed the limit value.

The proposed topology is not necessarily limited to the discussed application. It can be also exploited in applications with even more rigorous demands. A further improvement of the amplitude and phase accuracy within a wider frequency range could be achieved by using a digital control loop /7/.

For more powerful applications a topology survey of the switch mode inverter is presented in /8/. However, with only minor changes of the design parameters the output power of the topology, presented in this paper, can be increased significantly.

Refereces

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Prispelo (Arrived): 05.11.2003 *Sprejeto (Accepted): 25.02.2004*

A COMMUTATOR WITH INTEGRATED CAPACITORS

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Key words: commutation, universal motor, capacitor, finite element method, arc model.

Abstract: The paper presents a method of an improvement of commutation of a high-speed universal commutator motor with ceramic capacitors integrated in a commutator. A model of the motor was established to enable an analysis of an armature coil commutation. The capacitors were included in the model as well. A prototype motor with integrated capacitors was made. The multilayer ceramic capacitors in the form of surface mounted chips were used. Good (sparkless) commutation is essential for long operational lifetime of the commutator motor. The calculation of internal brush resistances and non-linear coil inductances was made with the finite element method . Brush contact resistances were also calculated. All resistances and inductances were calculated with respect to the rotor position. An actual overlap between the brush and the commutator segment was taken into consideration. A suitable arc model was used to estimate the arc, which varies with the width of the charred layer on the brush. The calculated results are compared with the ones measured on a special test motor. It was found out from calculation and from the measurement which closely agree, that the rightly chosen capacitors greatly improve the commutation of the motor and therefore extend the lifetime of the motor significantly.

Komutator z integriranimi kondenzatorji

Kjučne besede: komutacija, univerzalni motor, kondenzator, metoda končnih elementov, model obloka.

Izvleček: V prispevku predstavljamo izboljšavo komutacije hitrotekočega univerzalnega motorja z kondenzatorji, integriranimi v komutator. Izdelali smo računalniški model komutacije, ki omogoča analizo komutacijskih tokov v posameznih rotorskih tuljavah. Kondenzatorji so bili prav tako vključeni v model. Izdelali smo tudi prototipe motorjev z integriranimi kondenzatorji. Uporabljeni so bili večplastni keramični kondenzatorji izdelani v SMD tehnologiji. Dobra komutacija brez oblokov je bistvena za dolgo življenjsko dobo komutatorskih motorjev. Za določitev porazdeljenih upornosti ščetk in induktivnosti tuljav v računalniškem modelu smo uporabili metodo končnih elementov. Upornosti so bile odvisne od relativnega položaja komutator - ščetka, prav tako tudi induktivnosti, ki so bile odvisne še od toka, ki je tekel skoznje. Upoštevali smo realno prekrivanje ščetka - komutatorska lamela, to je 1,8. Zaradi takega prekrivanja smo morali upoštevati, da dve tuljavi komutirata istočasno. Izračunali smo tudi kontaktne upornosti. Za upoštevanje nastanka obloka smo uporabili model po Holmu /9/, ki določa pogoje za nastanek obloka v odvisnosti od kontaktnih materialov. Ugotovili smo, da pojav obloka pod ščetko povzroči spremembe na ščetki, kjer nastane ožgana plast, ki ima slabšo prevodnost od ščetke same. Nastanek te plasti močno vpliva na potek komutacijskih tokov. Izračunane komutacijske tokove smo primerjali s tokovi, izmerjenimi na prirejenem motorju, ki je imel konce dveh rotorskih tuljav izvedene na drsne obroče. Izračunani rezultati so se dovolj dobro približali merjenim rezultatom. Komutacija se tako pri izračuni kot pri meritvi zelo izboljša, če v komutacijski krog vključimo kondenzatorje. Podali smo kriterije za pravilno izbiro kondenzatorjev, ki najbolj učinkovito izboljšajo potek komutacije. Zaradi izboljšane komutacije s kondenzatorji se podaljša tudi življenjska doba motorja.

1. Introduction

The universal motor is one of the most common motors used in domestic appliances. It is a commutator motor that has its field winding connected in series with the armature winding. The revolving speed of this motor is increasing because of the tendency to decrease both the motor size and weight. It is not uncommon for this motor to have 50000 rpm or more. But good commutation (current direction change) is difficult to achieve at such high speeds.

The commutation in the commutating armature coil has to be fast enough to enable minimizing the current difference at the moment, when the commutator bar is leaving the brush. Excessive current differences give rise to the development of sparks and arcs, which shortens the motor operational lifetime through an increased brush wear. Moreover, the arc may occur before the commutator bar leaves the brush, if a voltage between the brush and the bar is large enough. The aim of this paper is to present a method of improvement of commutation with capacitors integrated in the commutator of the motor. The capacitors absorb the inductive energy which would otherwise disperse in the arcs and therefore greatly improve the commutation.

Until recently, the commutation phenomena has been mainly investigated on DC machines, preferably equipped with interpole windings /1,2/, which significantly improve the commutation. The commutation in AC universal motors is much worse compared to the one in the DC motors. One of the causes for this state is the absence of interpoles and the other is the presence of transformer EMF because of the AC line voltage. Authors in /3/ researched the universal motor commutation, where during one commutation period constant current is presumed. For the calculation of the circuit parameters (inductances and flux linkages) they used the finite element method. In /4/ the universal motor model is improved by using the real current and by modelling brush resistances with the finite element method, though the arc model is somehow simplified.

The model of the commutator motor with the integrated capacitors is presented, with which the commutation current and other commutation related phenomena in small universal motor can be analysed. The inductances, the flux linkages and the brush resistances for the model are calculated with the finite element method. The commutation equation is solved iteratively until the calculated currents converge. The arc model is improved by using the arc U/I characteristics /6/. The change in the contact resistance and the appearance of the charred layer on the brush due to the arc under the brush are explained. With this model, the optimal value of capacitance of integrated capacitors was calculated to diminish the arc. These capacitors were mounted on a special prototype motor with slip rings. The improvement of commutation both in the computer model and in the prototype motor was found to be satisfactory and the lifetime of the motor was extended.

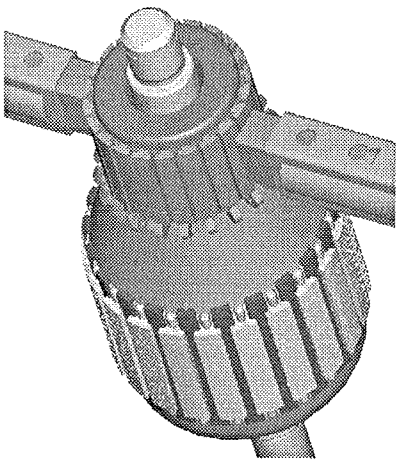

Figure 1: A universal motor rotor and brushes.

2. A universal motor circuit topology and model equations

The circuit topology of the two-pole universal motor is shown in Fig. 2. Because the brush-to-bar width ratio is 1.8, there are two possibilities: in the first one the brush covers two commutator bars and in the second one the brush covers three bars. In our model, both topologies are used, with a proper transition from one topology to the other, depending on the brush - bar position.

The circuit in Fig. 2 is symmetrical, so it can be simplified. Four commutating coils in Fig. 2 are considered as two paralleled windings. The parallel rotor winding branches in series with the field winding are replaced with one equivalent winding. Consequently, when the brush covers three commutator bars, there are three windings in the system - two commutation windings and one main winding. But, if the brush covers only two bars, there are two windings, the commutation one and the main one in the system.

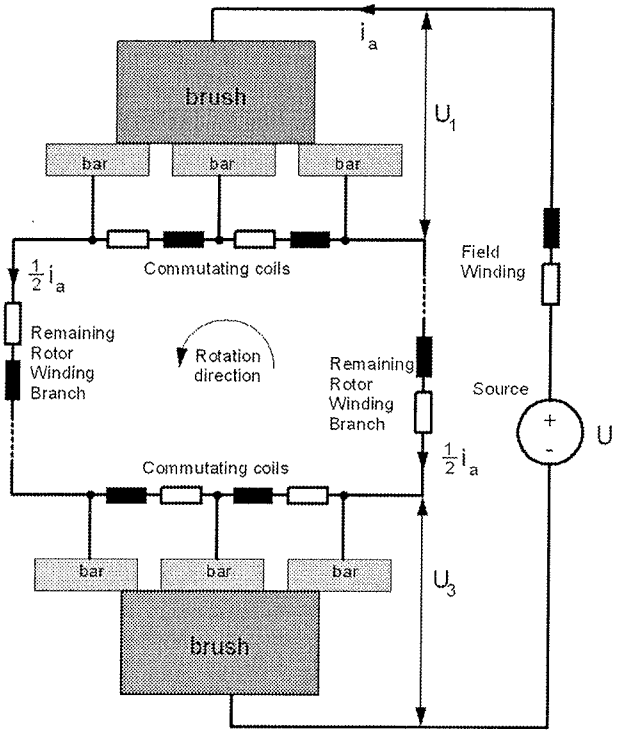

Figure 2: The universal motor circuit topology - the brush covers three bars.

The capacitors are connected parallel to the commutating windings. In series with the capacitor there is the damping resistance R_c. Fig. 3 shows two parallel commutating windings (L_{33}, R_3 and L_{44}, R_4), the capacitor C and the damping resistance R_c. The contact resistances R_{c1}, R_{c2} and R_{c3} can also be observed.

The main Equation (1) for Fig. 2 is:

$$U = (R_1 + R_2) \cdot i_a + \frac{d\psi_a}{dt} + U_1 + U_3 \qquad (1),$$

where:

U is the applied voltage,
R_1 is the field winding resistance,
R_2 is the resistance of the non-commutating parallel armature winding branches,
i_a is the main current,
ψ_a is the total flux linkage of the main winding,
U_1, U_2 and U_3 are the commutator bar voltages.

From Fig. 3 the following voltage Eqs. (2,3), are derived:

$$U_1 - U_2 = R_3 \cdot i_{c3} + \frac{d\psi_3}{dt} \qquad (2),$$

$$U_2 - U_3 = R_4 \cdot i_{c4} + \frac{d\psi_4}{dt} \qquad (3),$$

where:

ψ_3, ψ_4 are the total flux linkage commutating windings,
R_3, R_4 are the commutating winding resistances,
i_{c3}, i_{c4} are the commutating currents.

For the capacitor branch from Fig. 3 Eqs. (4,5) can be written:

$$U_1 - U_2 = R_c \cdot i_{cc1} + \frac{1}{C} \cdot \int i_{cc1} dt \quad (4),$$

$$U_2 - U_3 = R_c \cdot i_{cc2} + \frac{1}{C} \cdot \int i_{cc2} dt \quad (5),$$

where:

C is the capacitance of the integrated capacitor,
R_c is the damping resistance,
i_{cc1}, i_{cc2} are the capacitor currents.

The connection between the commutator bar voltages and the currents is defined by Eq. (6):

$$\begin{bmatrix} U_1 \\ U_2 \\ U_3 \end{bmatrix} = \begin{bmatrix} r_{11} + r_{c1} & r_{12} & r_{13} \\ r_{12} & r_{22} + r_{c2} & r_{23} \\ r_{13} & r_{23} & r_{33} + r_{c3} \end{bmatrix} \cdot \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \quad (6),$$

where:

r_{11}, r_{12}, r_{13}, r_{22}, r_{23}, r_{33} are elements of the brush resistance matrix,
r_{c1}, r_{c2}, r_{c2} are the brush contact resistances,
i_1, i_2, i_3 are commutator bar currents.

The value of the above resistances depends on the instantaneous brush position with respect to the commutator bars. The brush resistance matrix elements are determined by the brush dimensions and the brush material properties (e.g. material specific resistances).

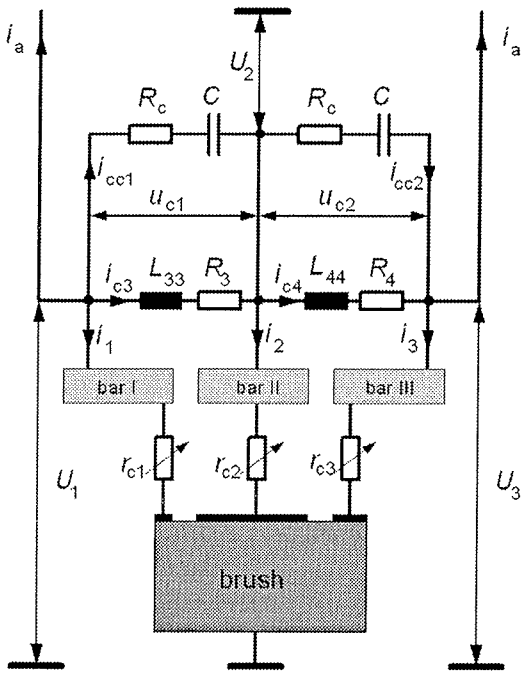

Figure 3: The brush with the parallel commutating windings and the integrated capacitors.

According to Fig. 3, the commutator bar currents are defined as:

$$i_1 = -i_a - i_{c3} - i_{cc1} \quad (7),$$

$$i_2 = i_{c3} - i_{c4} + i_{cc1} - i_{cc2} \quad (8),$$

$$i_3 = -i_a + i_{c4} + i_{cc2} \quad (9).$$

Energy in the capacitors is represented by the capacitor voltage. The capacitor voltages are defined in (10) and (11):

$$U_1 - U_2 = u_{c1} \quad (10),$$

$$U_2 - U_3 = u_{c2} \quad (11).$$

When the matrix (6) with the currents (7), (8), (9) is inserted in Eqs. (10) and (11) the following two equations for the capacitor voltage are obtained - (12) and (13):

$$\begin{aligned} u_{c1} &= -i_a \cdot R_{21} - i_{c3} \cdot (R_{22} - R_3) - \\ & i_{c4} \cdot R_{23} - i_{cc1} \cdot (R_{22} - R_3) - i_{cc2} \cdot R_{23} \end{aligned} \quad (12),$$

$$\begin{aligned} u_{c2} &= -i_a \cdot R_{31} - i_{c3} \cdot R_{32} - i_{c4} \cdot (R_{33} - R_4) \\ & - i_{cc1} \cdot R_{32} - i_{cc2} \cdot (R_{33} - R_4) \end{aligned} \quad (13),$$

The resistances in the above equations are (14):

$$\begin{aligned} R_{21} &= r_{11} + r_{c1} + r_{13} - r_{12} - r_{23} \\ R_{22} &= R_3 + r_{11} + r_{c1} - 2r_{12} + r_{22} + r_{c2} \\ R_{23} &= r_{12} - r_{13} - r_{22} - r_{c2} + r_{23} \\ R_{31} &= r_{12} - r_{13} + r_{23} - r_{33} - r_{c3} \\ R_{32} &= r_{12} - r_{13} - r_{22} - r_{c2} + r_{23} \\ R_{33} &= R_4 + r_{22} + r_{c2} - 2r_{23} + r_{33} + r_{c3} \end{aligned} \quad (14).$$

From the equations (12) and (13), the equations of the capacitor currents are derived - (15) and (16):

$$i_{cc1} = -u_{c1} \cdot g_{11} + u_{c2} \cdot g_{12} + i_a \cdot k_1 - i_{c3} \quad (15),$$

$$i_{cc2} = u_{c1} \cdot g_{21} - u_{c2} \cdot g_{22} + i_a \cdot k_2 - i_{c4} \quad (16).$$

Where the conductances $g_{11}...g_{22}$ and the coefficients k_1 and k_2 are:

$$\begin{aligned} g_{11} &= \frac{R_{33} - R_4}{(R_{22} - R_3) \cdot (R_{33} - R_4) - R_{23} \cdot R_{32}} \\ g_{12} &= \frac{R_{23}}{(R_{22} - R_3) \cdot (R_{33} - R_4) - R_{23} \cdot R_{32}} \\ g_{21} &= \frac{R_{32}}{(R_{22} - R_3) \cdot (R_{33} - R_4) - R_{23} \cdot R_{32}} \\ g_{22} &= \frac{R_{22} - R_3}{(R_{22} - R_3) \cdot (R_{33} - R_4) - R_{23} \cdot R_{32}} \\ k_1 &= \frac{R_{31} \cdot R_{23} - R_{21} \cdot (R_{33} - R_4)}{(R_{22} - R_3) \cdot (R_{33} - R_4) - R_{23} \cdot R_{32}} \\ k_2 &= \frac{R_{21} \cdot R_{32} - R_{31} \cdot (R_{22} - R_3)}{(R_{22} - R_3) \cdot (R_{33} - R_4) - R_{23} \cdot R_{32}} \end{aligned} \quad (17).$$

The time derivative of the capacitor voltages are obtained by inserting Eqs. (15) and (16) into Eqs. (4) and (5), and are represented by Eqs. (18) and (19):

$$\frac{du_{c1}}{dt} = R_c \cdot \left(-\frac{du_{c1}}{dt} \cdot g_{11} + \frac{du_{c2}}{dt} \cdot g_{12} + \frac{di_a}{dt} \cdot k_1 - \frac{di_{c3}}{dt} \right) + \\ + \frac{1}{C} \cdot \left(-u_{c1} \cdot g_{11} + u_{c2} \cdot g_{12} + i_a \cdot k_1 - i_{c3} \right) \quad (18),$$

$$\frac{du_{c2}}{dt} = R_c \cdot \left(\frac{du_{c1}}{dt} \cdot g_{21} - \frac{du_{c2}}{dt} \cdot g_{22} + \frac{di_a}{dt} \cdot k_2 - \frac{di_{c4}}{dt} \right) + \\ + \frac{1}{C} \cdot \left(u_{c1} \cdot g_{21} - u_{c2} \cdot g_{22} + i_a \cdot k_2 - i_{c4} \right) \quad (19).$$

The time derivative of the flux linkages is divided into the transformer and speed EMF (10):

$$\frac{d[\psi]}{dt} = \frac{d[\psi]}{di} \frac{di}{dt} + \frac{d[\psi]}{d\varphi} \frac{d\varphi}{dt} \quad (20).$$

The values of incremental inductances /5/, which are the derivatives of flux linkages with respect to the current, and the values of the flux linkages at different angles and currents were obtained with the commercially available finite element method (FEM) program. Since we presume the speed of the motor to be constant, the following equation can be written (21):

$$\frac{d[\psi]}{dt} = [L] \frac{di}{dt} + \frac{d[\psi]}{d\varphi} \omega \quad (21).$$

By substituting the time derivative of the flux linkages in (1), (2) and (3) with (21) and by adding the time derivative of the capacitor voltages (18), (19), we get (22):

$$\begin{bmatrix} U \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} R_{11} + R_2 & 0 & 0 & -1 & -1 \\ 0 & R_3 & 0 & -1 & 0 \\ 0 & 0 & R_4 & 0 & -1 \\ \frac{k_1}{C} & -\frac{1}{C} & 0 & -\frac{g_{11}}{C} & \frac{g_{12}}{C} \\ \frac{k_2}{C} & 0 & -\frac{1}{C} & \frac{g_{21}}{C} & -\frac{g_{22}}{C} \end{bmatrix} \cdot \begin{bmatrix} i_a \\ i_{c3} \\ i_{c4} \\ u_{c1} \\ u_{c2} \end{bmatrix} + \\ + \begin{bmatrix} L_{aa} & L_{a3} & L_{a4} & 0 & 0 \\ L_{a3} & L_{33} & L_{34} & 0 & 0 \\ L_{a4} & L_{34} & L_{44} & 0 & 0 \\ R_c \cdot k_1 & -R_c & 0 & -R_c \cdot g_{11} - 1 & R_c \cdot g_{12} \\ R_c \cdot k_2 & 0 & -R_c & R_c \cdot g_{21} & -R_c \cdot g_{22} - 1 \end{bmatrix} \cdot \\ \begin{bmatrix} \frac{di_a}{dt} \\ \frac{di_{c3}}{dt} \\ \frac{di_{c4}}{dt} \\ \frac{du_{c1}}{dt} \\ \frac{du_{c2}}{dt} \end{bmatrix} + \begin{bmatrix} \frac{d\psi_a}{dt} \\ \frac{d\psi_3}{dt} \\ \frac{d\psi_4}{dt} \\ 0 \\ 0 \end{bmatrix} \cdot \omega \quad (22).$$

Rearranging (22), we obtain the following equation:

$$\begin{bmatrix} \frac{di_a}{dt} \\ \frac{di_{c3}}{dt} \\ \frac{di_{c4}}{dt} \\ \frac{du_{c1}}{dt} \\ \frac{du_{c2}}{dt} \end{bmatrix} = \begin{bmatrix} L_{aa} & L_{a3} & L_{a4} & 0 & 0 \\ L_{a3} & L_{33} & L_{34} & 0 & 0 \\ L_{a4} & L_{34} & L_{44} & 0 & 0 \\ R_c \cdot k_1 & -R_c & 0 & -R_c \cdot g_{11} - 1 & R_c \cdot g_{12} \\ R_c \cdot k_2 & 0 & -R_c & R_c \cdot g_{21} & -R_c \cdot g_{22} - 1 \end{bmatrix}^{-1} \\ \cdot \left(\begin{bmatrix} R_{11} + R_2 & 0 & 0 & -1 & -1 \\ 0 & R_3 & 0 & -1 & 0 \\ 0 & 0 & R_4 & 0 & -1 \\ \frac{k_1}{C} & -\frac{1}{C} & 0 & -\frac{g_{11}}{C} & \frac{g_{12}}{C} \\ \frac{k_2}{C} & 0 & -\frac{1}{C} & \frac{g_{21}}{C} & -\frac{g_{22}}{C} \end{bmatrix} \cdot \begin{bmatrix} i_a \\ i_{c3} \\ i_{c4} \\ u_{c1} \\ u_{c2} \end{bmatrix} + \begin{bmatrix} U - \frac{d\psi_a}{dt} \cdot \omega \\ -\frac{d\psi_3}{dt} \cdot \omega \\ -\frac{d\psi_4}{dt} \cdot \omega \\ 0 \\ 0 \end{bmatrix} \right) \quad (23).$$

Eq. (23) represents the model of the system in the standard form of the state space formulation. At each time step the values of the inductances, the resistances and the flux linkages derivatives with respect to the angle are updated according to the angle (brush position) and main current i_a. Since the flux linkages, but not their derivatives, were obtained with FEM, the table of the flux linkages derivatives with respect to the angle were calculated from the table of the flux linkages before the solution to the system (23) was initiated. The system is solved by time stepping numerical integration.

3. FEM computed inductances and flux linkages and their dependence on the commutation

A large number of the finite element magnetostatic iterations had to be calculated to obtain the complete incremental inductance matrix and the flux linkage vector, since they depend on the current and the angle. They must be calculated at each angle and current step throughout all the currents values involved.

The inductance computation method used by the commercially available FEM program /7/ is based on Gyimesi and Ostergaard /8/. The method uses incremental energy, which is calculated around the working point, when the currents are incremented.

In Eq. (23) there are three currents; main current i_a, and two commutating currents, i_{c3} and i_{c4}. The inductance matrix and the flux linkage vector are dependent on all the three currents. The FEM magnetostatic solution should be calculated at each combination of these currents, which leads to an unmanageable number of calculations. Jet, since main current i_a has the greatest influence on iron saturation, it is presumed that commutation currents do not considerably change the inductance values. A number

of test calculations was made, using the following two commutation current forms:

1. *the linear commutation,* using the linear commutation current from $-i_a$ to i_a and the length of the commutation equals to the whole brush width;
2. *the 50% overcompensated linear commutation*, using also the linear commutation current from $-i_a$ to i_a but shortening the length of the commutation by 50%.

The results of these calculations with respect to the angle and at an unchanged value of the main current can be seen in Fig. 4. The maximum difference between the inductances is 5%, which is considered acceptable for further use. The difference is due to the slightly lower saturation at 50% overcompensated linear commutation.
A database table is created at each angle and current step. It consists of an inductance matrix and flux linkage entries. As the integration of Eq. (23) is progressing, the values in the table are interpolated from the nearest values of angles and currents in the table.

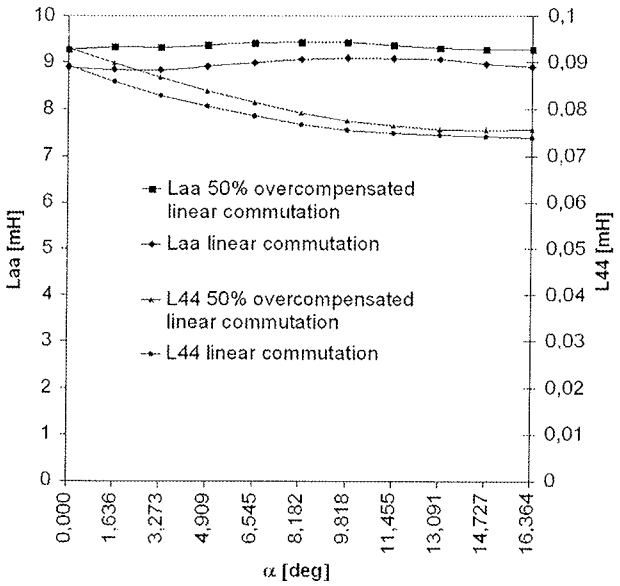

Figure 4: The inductance comparison at i_a=5A and at two different commutation forms - at 50% overcompensated linear commutation and at linear commutation.

4. The distributed brush resistance matrix, the brush-commutator contact resistances and the arc model

4.1. The distributed brush resistances

The internal brush resistances were calculated by the commercially available FEM package. These resistances are dependent on the brush to the commutator position. They were calculated according to /4/, where the cross-section of the brush is covered with an FE mesh. The result of the FEM computation is the voltage distribution throughout the cross-section of the brush, and the electric current density is calculated from this voltage distribution. On the side of the brush, where it touches the commutator bars, voltages are applied (Dirichlet boundary condition), depending on the brush to commutator position. On the opposite side, the end surface voltage is defined as zero. The brush FE mesh is shown in Fig. 5.

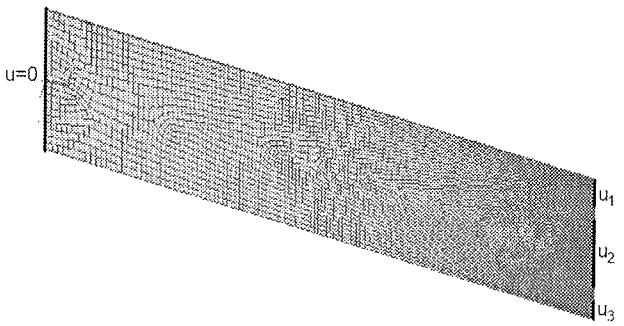

Figure 5: The brush FE model with the mesh and the boundary conditions.

The entries of the brush resistance matrix were calculated from the system energy /4/. Results dependent on the brush position are given in Fig. 6.

The initial commutator position is the position where the commutator groove is at the centre of the brush (α=0). At that position the brush covers two commutator bars and the brush matrix entries r_{33}, r_{13} and r_{23} are there infinite. The infinite values are replaced with high resistance values. From α=3.304° to 13.059° the brush covers three bars entirely, so each matrix entry is finite. Where the angle is larger than 13.059°, the brush again covers only two bars and the infinite resistance matrix entries are again replaced with high but finite values.

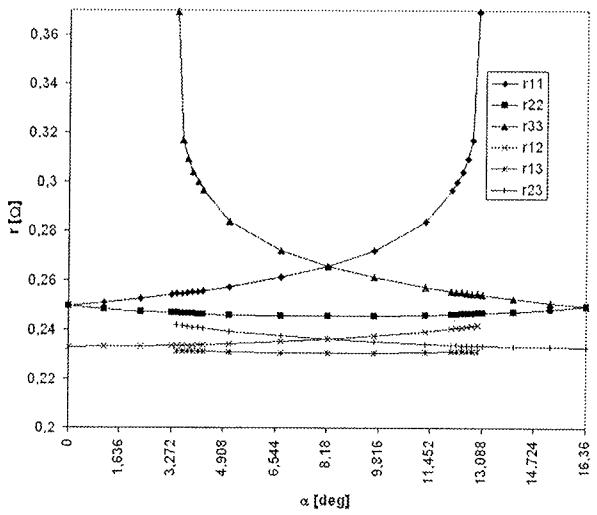

Figure 6: The FEM calculated brush resistance matrix entries

4.2. The brush-commutator contact resistances

The full brush contact resistance R_{full} is calculated from the average contact voltage drop and from the current at which the collector film is formed. The brush contact resistance due to the commutator position is calculated using the following equation:

$$r_c = R_{full} \cdot \left(A_{full} / A(\alpha)\right)^{0.75} \qquad (24).$$

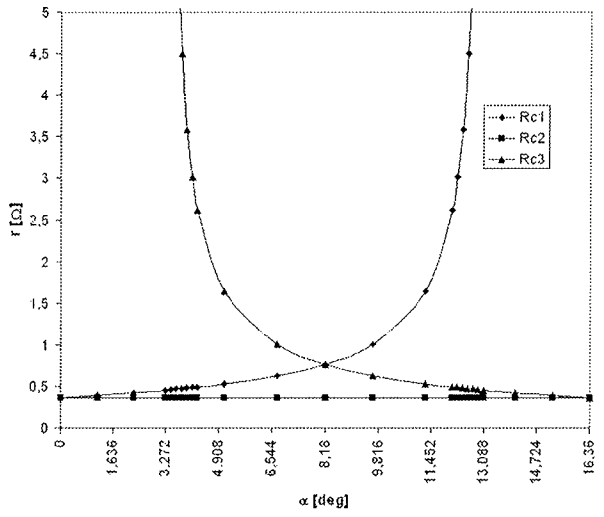

Figure 7: The brush – commutator bars contact resistances.

Here A_{full} represents the full commutator bar-brush contact area and $A(\alpha)$ commutator bar-brush contact area on instantaneous commutator position. The contact resistance equations are written for all the three commutator bars with regard the commutator position. At the initial and final commutator positions, two bars only are covered by the brush and one contact resistance has an infinite value replaced by a large finite value. The calculated resistances are shown in Fig. 7.

4.3. The arc model

When the commutator bar is leaving the brush, the conducting area $A=A_1$ draws near to zero and the contact resistance becomes infinite. The current density increases and causes vaporization of the surface material and formation of the electric arc. The conditions for the arc formation were thoroughly examined by Holm et al/9/ who measured U-I characteristics of the arc. The voltage at which the arc is formed (U_m) depends on the cathode material of the separating contacts, whereas the current at which the arc extinguishes (I_m) at the latest depends on the anode material. According to /9/, different authors have measured different values of I_m and U_m. In Table 1 these values for carbon and copper can be seen.

In our case, the source voltage is the AC voltage. So in one brush-commutator bar contact the cathode in one half of the AC cycle is copper and in the other half is carbon. At the other brush-commutator bar contact this is just the opposite. Average value for U_m and I_m, measured by Holm, are then used. They are 16.5V and 0.22A, respectively. These values were confirmed by our measurements on a motor equipped with an additional brush, closely following one of the main brushes. The voltage was measured over both brushes.

In the system described by Eq. (23), the arc characteristic is implemented by changing the value of R_{c1}, that is the contact resistance of the first commutator bar and the brush. When the contact voltage on the trailing edge of the brush reaches U_m, the arc is assumed to ignite and an apparent contact resistance is calculated by maintaining the arc voltage drop. This model is valid as long as the commutator bar is under the brush and the distance between them is constant. This distance is the thickness of the commutator film and other deposits. When the commutator bar leaves the brush, the contact voltage is no longer constant. It increases with the distance from the commutator bar. In this case, the arc U/I characteristic from /9/ is applied. The arc extinguishes when the arc current falls below a certain value derived from the U/I characteristics of the arc and of the load. The minimal arc current is larger than I_m. In our case this is 0.22A.

Under normal operating conditions of the universal motor, arcs under the brush appear very often. They affect the brush visibly; a blackened charred layer or a belt develops on the brush. A photography of such layer is shown in Fig. 8.

The contact resistance of the charred layer is about fifty times larger than the normal brush-bar contact resistance. This contact resistance is of no importance if the arc has already been ignited. It is important for the formation of the arc. If the charred layer is already formed, the contact resistance reaches the value at which, as a result of other conditions, the arc occurs. This happens at a lower angle compared to the clean brush. This means that the charred layer itself grows in the direction opposite to rotation. The growing of the charred layer stops when the system reaches equilibrium.

Table 1: I_m and U_m for carbon and copper, measured by different authors

	I_m [A]			U_m [V]			
Material	Ives	Fink	Holm	Ives	Gaulrapp	Fink	Holm
C	0.02		0.01	15.5			20
Cu		1.15	0.43		12.5	8.5	13

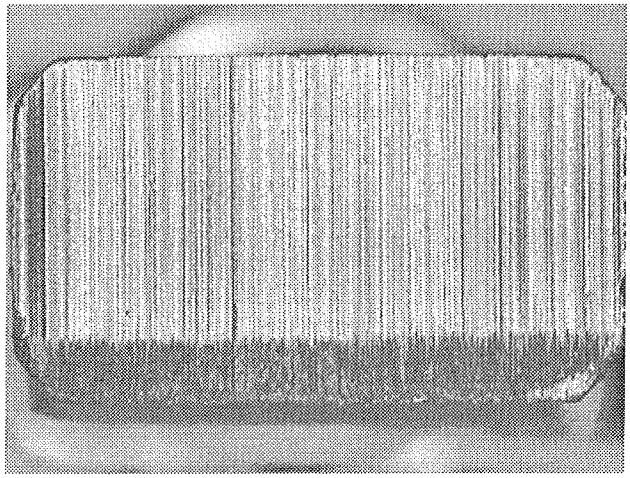

Figure 8: Photography of a brush with a charred layer.

In the model, instead of one contact resistance R_{c1} we have two contact resistances, i. e. the resistance of the clean brush and the resistance of the charred layer with a variable width as it is depicted on Fig. 9.

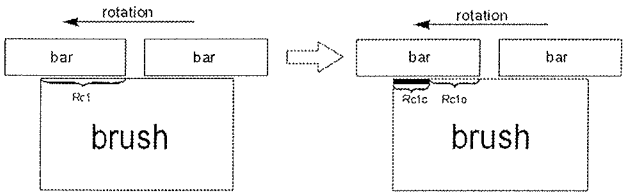

Figure 9: Change in the contact resistance Rc1 due to the charred layer on the brush.

Fig. 10 shows the contact resistance R_{c1} which includes the increased resistance of the charred layer.

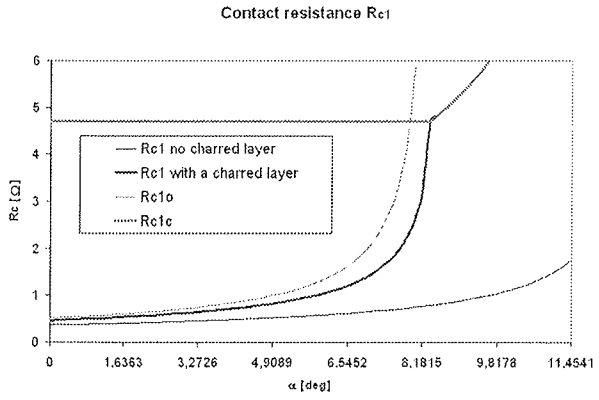

Figure 10: The comparison of R_{c1} with and without the charred layer.

5. Solving the system of equations

The Runge-Kutta method of the fourth order was used for solving the system of equations (23). To solve the system, we need initial values for the system variables i_a, i_{c3}, i_{c4}, u_{c1} and u_{c2}. The initial values for these variables were set to zero. The system (23) was now solved. If conditions for the arc formation developed, the arc model is applied. The starting position of the commutator ($\alpha = 0°$) is at the position where the commutator groove is aligned with the center of the brush. The ending position ($\alpha = \alpha_p = 360°/22 = 16.36°$ if there are 22 commutator bars) is defined by the position, at which the next commutator groove is aligned with the center of the brush. The values of the system variables at the ending position of the commutator are used for the initial conditions for the next iteration in a way as it is shown in Eq. (25):

$$\begin{aligned} i_{a,i+1}(\alpha = 0°) &= i_{a,i}(\alpha = \alpha_p) \\ i_{c3,i+1}(\alpha = 0°) &= i_{c4,i}(\alpha = \alpha_p) \\ i_{c4,i+1}(\alpha = 0°) &= i_{a,i}(\alpha = \alpha_p) \\ u_{c1,i+1}(\alpha = 0°) &= u_{c2,i}(\alpha = \alpha_p) \\ u_{c2,i+1}(\alpha = 0°) &= R_4 \cdot i_{a,i}(\alpha = \alpha_p) + \frac{d\psi_{4,i}(\alpha = \alpha_p)}{dt} \end{aligned} \quad (25),$$

where i is the index of the current iteration.

In the case of the DC source voltage, the system iterates until the values of the system variables at the end of the iteration are the same as the values of the system variables from the previous iteration within the tolerance limits. If an arc develops in any of the iterations, the width of the charred layer is calculated and then used for the next iteration. The system usually reaches the converged value in less than 100 iterations.

In the case of the AC source voltage, the solution to the system is much more time consuming. At 30000 rpm, the motor makes 10 revolutions in one 50Hz AC cycle. This means 220 iterations in one AC cycle for the commutator with 22 segments. At each commutation iteration the width of the charred layer is remembered and at the end of one AC cycle the average width of the charred layer is calculated and used for the next AC cycle. The iteration stops when the RMS current and the charred layer width stop changing. This is usually after several tens of AC cycles.

6. The simulation and the verification results using the commutator without the integrated capacitors

At the first the simulation was done for the case without the capacitors. Since the capacitors are already integrated in the numerical model, the capacitors are presumed to have no effect on commutation, if a large value of resistance R_c is chosen.

The simulated and the measured data were based on the technical data for a vacuum cleaner motor, equipped with 22 commutator bars and 22 slots. It is a standard two-pole universal motor having an effective brush advance angle

of 24.5°. The value of the main current was 3.6A and the motor speed was 22000 rpm. This is below the nominal working point of the motor, because our test motor did not allow higher speed and current. The nominal voltage of the analysed unit is 230V, but the voltage of 180V was used in our tests.

The measurements were made on a special test motor, which has two rotor coils connected to the slip rings through a hollow shaft. The brushes on the slip rings are special low resistance brushes, made of graphite with large portion of copper. On these brushes it is possible to measure the commutation current. On the Fig. 11, a photography of the test motor with slip rings is shown.

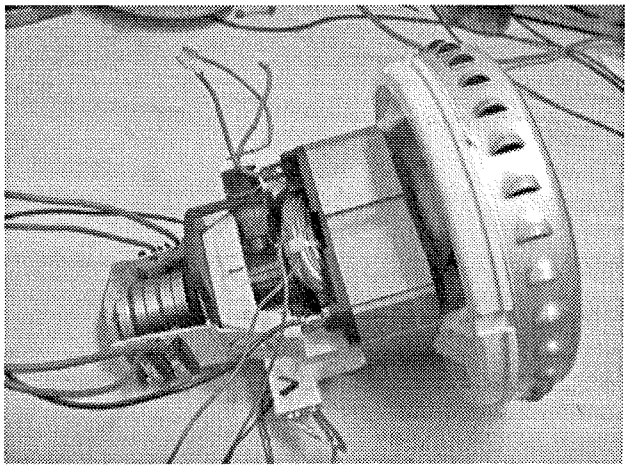

Figure 11: The test motor with the slip rings.

The five important positions of the commutator were defined, as it is shown in Fig. 12.

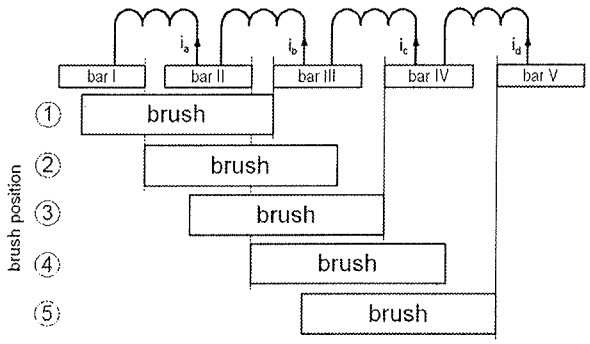

Figure 12: The five important commutator positions.

Fig. 13 shows the simulated commutating current. The charred layer width was calculated to be 1°. This is the width of 0.2mm on the brush. This means there was the arc under the brush with the constant voltage. The current fell below I_m when the commutator bar left the brush, so there was no arc in the air gap between the trailing edge of the brush and the leaving bar. In Fig. 13, two identical sequential calculations are shown thus presenting one complete commutation (current I_b).

In some commutator positions, two sequential coils commutate and affect each other. For example, when the bar III enters the brush, the direction of the current I_a changes. It begins to decrease despite having no direct contact with the bar III. This happens because of the mutual inductance of the coils a and b. The opposite happens when the bar I enters the charred layer; the arc develops and rapidly changes I_a and also I_b - the commutation of I_b is slowed down. It is seen, that the commutation of one coil current worsens the commutation of the other. But if the arc develops, the other coil dissipates the energy of the arc because of the mutual inductance between these coils. As the arc develops in the charred layer, the arc current decreases quickly. When it drops bellow the limit value, the arc extinguishes. In our case this happened just before the bar II left the brush.

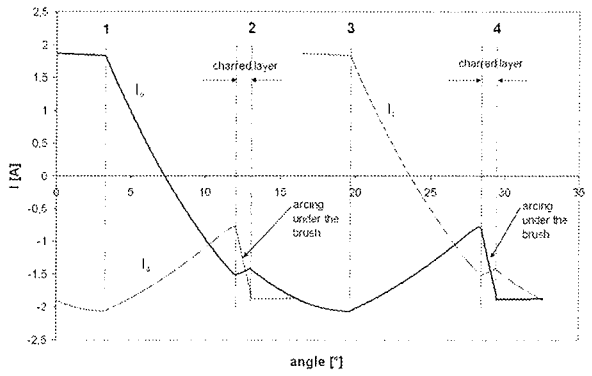

Figure 13: The simulated commutation currents without the capacitors.

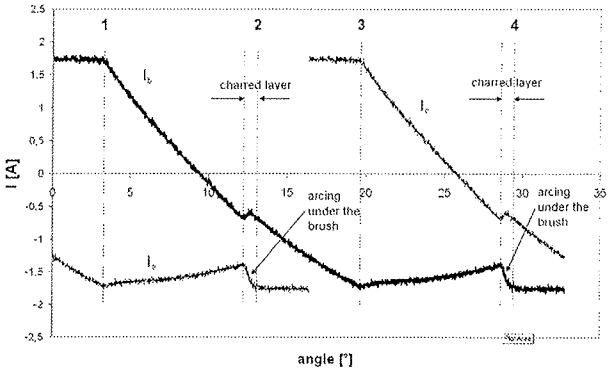

Figure 14: The measured commutation currents without the capacitors.

Let us now examine the comparable measurements. The measurements results are shown in Fig. 14. The measured commutating current has the same form as the calculated one. At the beginning of the commutation of the current I_b - the point 1 - the simulated current commutated faster than the measured current. The effect of arcing of the previous current can clearly be seen on the simulated and on the measured current. The largest difference between these two currents happens from the points 3 and

4, where the next current I_c starts to commutate. The current I_b at simulation starts to increase rapidly, at measurement this increase of the current is not so steep. The current difference, which dissipates the energy through arcing is therefore larger at simulation. The length of the charred layer is 0.8° in both cases.

It is clearly shown, that arcing under the brush did occur, when a commutator without integrated capacitors was used.

7. The simulation and the verification results using the commutator with the integrated capacitors

The integration of the capacitors in the commutator is seen in Fig. 15. The multilayer ceramic capacitors, manufactured as surface mounted chips, were used. The dimensions of capacitors were 2.0x1.25x1.2mm. The cross-section of such capacitor is seen in Fig. 16. The ceramic dielectric used was the stable 2R1. This material is made of ceramic materials, which are ferroelectric, principally barium titanate. The capacitors of the ferroelectric types have a nonlinear temperature characteristics, the capacitance and tand are effected by temperature, voltage and frequency. The material 2R1 was used because it has the best compromise between capacitance per volume unit and temperature and voltage stability. There is not much space in the commutator, so the size of the capacitor is critical. The above mentioned dimensions are maximal, which can be used in the given commutator. The maximal capacitance of capacitor with dimensions 2.0x1.25x1.2mm, using the 2R1 dielectric, is 1μF and its withstand voltage is 100V.

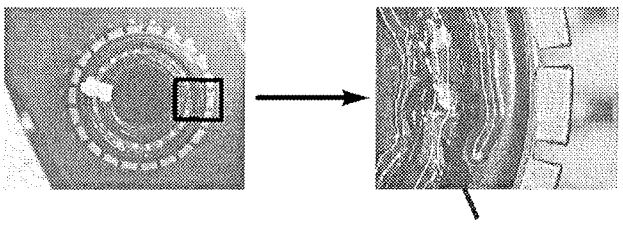

Figure 15: The integration of the capacitors in the commutator.

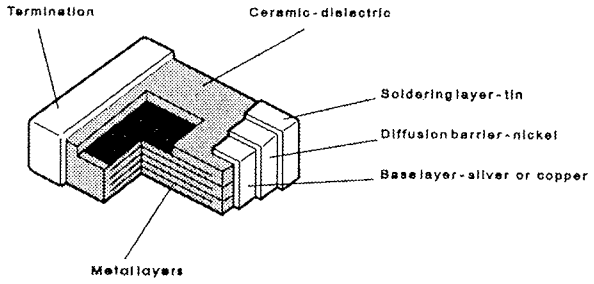

Figure 16: The cross-section of the used ceramic capacitors.

The capacitors were integrated into the commutator because of large centrifugal forces which are present at the rotational speed up to 50,000 rpm. As it is seen in Fig. 15, the capacitors were firmly soldered into the circular groove at the top of the commutator. The groove was then filled with a clear plastic glue, which further fixed the capacitors into the groove and also prevented any debris from the brush to make any additional unwanted contacts.

The capacitors in the commutator work in a very harsh environment. As it was stated above, it is exposed to large centrifugal forces. The temperatures on the commutator surface reach the values of 110°C - 120°C. On the inside of the commutator the temperatures are lower by 10°C - 20°C. So the ceramic material must not loose its dielectric capability because of temperatures around 100°C.

The voltage of the capacitor must not exceed the nominal voltage of the capacitor, and it also must not reach too high value to cause additional arcing. The theoretical maximal capacitor voltage can be estimated using the magnetic and electrical energy equations. In Eq. (16) it is presumed, that all the magnetic energy, stored in the commutating winding at the angle, where the commutator bar leaves the brush, changes into the electrical energy of the capacitor.

$$\frac{L_{33}\cdot(\Delta i)^2}{2}=\frac{C\cdot(U_{C\max})^2}{2} \qquad (26),$$

where:

Δi = 1A	the current difference,
$U_{C\max}$ = 16,5V	maximal allowed capacitor voltage to avoid arcing,
L_{33} = 240 μH	inductance of the commutating winding.

The value of the required capacitance can be calculated using the Eq. (27), which is derived form (26):

$$C=L_{33}\cdot\left(\frac{\Delta i}{U_{C\max}}\right)^2=918\,\mathrm{nF} \qquad (27).$$

With this capacitance the capacitor voltage will not exceed the arcing limit U_m=16,5V at the given working point. It must be emphasized, that the inductance L_{33} is dependent both on the main current and on the angle of rotation - this mean the position of the rotor. The current difference Δi depends on the behavior of the whole system. So this calculation is valid only for the estimation of the required capacitance for the working point.

The capacitors which were used in the simulation and in the measurement had the capacitance C= 1μF, which leaves us slight safety margin. The capacitors nominal voltage is 100V.

The simulation results are seen in Fig. 17. To avoid confusion only one commutating current is shown. The current has first oscillation at the position 2, which is the conse-

quence of the previous commutation. From the position 3 to 4 the current starts to increase, because at the position 3 the next winding starts to commutate. The same effect can be seen in Fig. 13, where the commutation without capacitors is shown. When the commutator bar reaches the end of the brush at the position 4, the current starts to flow into the capacitor. This is the beginning of LC oscillations, which are damped because of the winding resistance R_3 and because of the damping resistance R_c. At the angle 45°, the oscillations have not yet ceased.

In Fig. 18 the simulated capacitor voltage is shown. Only the second part of the simulation is shown - the rotor positions 3, 4 and 5. At the position 4 the commutator bar is leaving the brush and at that angle the energy starts to flow from inductance into capacitor. Therefore the capacitor voltage increases. The maximal capacitor voltage reaches the value of 17V, which is slightly above the estimated value. But this voltage is can cause arcs, if it is present at position 4, where the commutator bar is still close to the brush. When the bar - brush distance increases, the voltage, necessary for arcing, increases as well. At the angle 32°, where the capacitor voltage is maximal, the distance of the brush from the bar is 3°, which is 0,65mm. According to /10/ at that distance the required arcing voltage is around 35V. The capacitor voltage has not reached this value at which arcing could occur. So the rightly chosen capacitors prevent arcing.

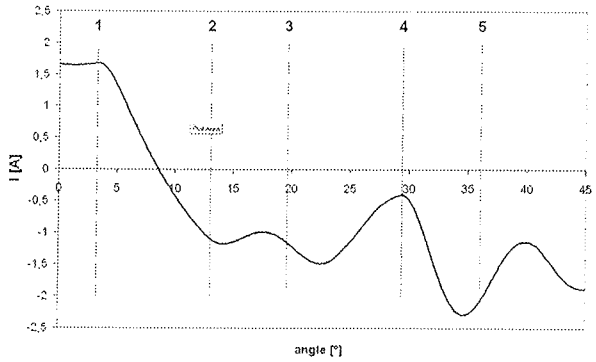

Figure 17: The simulated commutation currents with the integrated capacitors C=1μF.

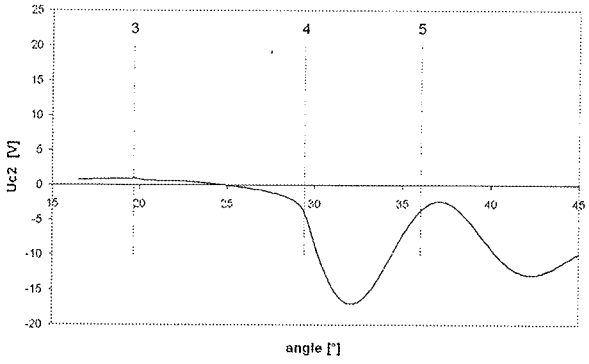

Figure 18: The simulated capacitor voltage.

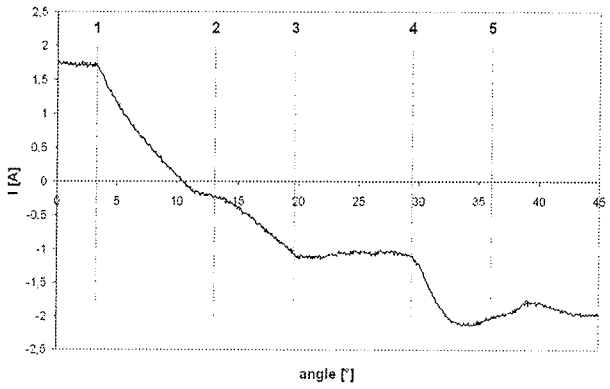

Figure 19: The measured commutation currents with the integrated capacitors C=1μF.

The measurements were made on another test motor with the same construction as in Fig. 11, but with capacitors integrated in the commutator. The measured results are in Fig. 19. The current difference at the position 4, where the commutator bar is leaving the brush, is smaller than in the simulation, so the oscillation afterwards have smaller amplitude. The oscillation at the position 2 are smaller as well. This is because the commutation of the previous coil has smaller oscillations and the effect on the observed commutation also diminishes. Measurements show that there is no arcing.

Quality of the commutation has direct effect on the lifetime of the universal motor. Arcing causes migration of material on the brush-commutator contact, specially the brush material. The brush material losses are divided to loses due to the mechanical causes- friction and vibration - and to the losses due to electrical one - arcing. It was proven in this work, that to prevent arcing the integrated capacitors have to be used. Because of that, the tested actual lifetime of the motors with integrated capacitors increases by 25% to 30%.

5. Conclusions

The method for the analysis of the commutation current and arcing of the high-speed universal motor with the integrated capacitors built in the commutator is presented in this paper. The analysis is done by the mathematical model. The model consists of the circuit elements obtained with the finite element method. These elements are inductances, flux linkages and internal brush resistances. The actual brush - commutator segment overlapping of 1.8 is used. The contact resistances are thoroughly examined and the arc model is implemented. The effect of the charred layer on the brush is considered as the increased contact resistance. The charred layer is caused by the arc under the brush. As the charred layer contact resistance is very high, it actually helps commutation. Because of this layer the commutation ends before the commutator bar leaves the brush and no arc develops in the air gap at the trailing edge of the brush. But still, there is the arc under the brush,

and the brush wears down more rapidly than it would in absence of the arc.

The method for the estimation of the required integrated capacitance is presented too. The criterion for the capacitance choice was the capacitor voltage which must not exceed the value, at which arc is formed.

The commutation currents with and without the capacitors are compared. It is shown, that without the capacitors arcing under the brush occurs. When capacitors are added to the commutation circuit, no more arcs occur, and the lifetime of the motor is extended by 25-30%.

The calculated commutation currents are also compared with the measured ones. The measurements were made on special test motors with the slip rings. The results of the calculation are found satisfactory.

With the appropriate machinery the integration of capacitors into the commutator is possible in the serial production. The cost of such an enhanced commutator in not too high and it is estimated that for high performance universal motors that kind of commutator is going to be used.

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Prispelo (Arrived): 31.10.2003 *Sprejeto (Accepted): 25.02.2004*

UDK621.3:(53+54+621+66), ISSN0352-9045 Informacije MIDEM 34(2004)1, Ljubljana

MERILNI SISTEM SPEKTRALNEGA ANALIZATORJA S FIKSNO NAMEŠČENIMI FOTOPOMNOŽEVALKAMI

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Kjučne besede: atomska spektroskopija, monokromator, analogno-digitalni pretvornik, optične komunikacije, mikrokrmilnik, programirna logična vezja, USB vodilo

Izvleček: Predstavljena je sodobna zasnova merilnega sistema analizatorja ultravijoličnega svetlobnega spektra. Merilni sistem je predstavljen za spektralni analizator z 64 fiksno nameščenimi fotopomnoževalkami. Pri tem smo: - razvili, za krmiljenje visoke napetosti na fotopomnoževalkah, vezje z digitalnimi potenciometri in tokovno-napetostnimi pretvorniki, - uporabili smo optične vodnike med posameznimi stopnjami ter USB povezavo z osebnim računalnikom, - uporabili programirna logična vezja in mikrokrmilnike v posameznih delih merilnega sistema. Posebno skrb smo namenili nadzoru delovanja sistema in avtokalibraciji. Tako zasnovan merilni sistem je primeren za avtomatizirano meritev svetlobnega spektra z možnostjo dodatne obdelave izmerjenih vrednosti s programskimi orodji na osebnem računalniku. Dodana je možnost nadzora spektralnega analizatorja preko spleta.

The Spectral Analyzer Measurement System with Fix Placed Photomultiplier Tubes

Key words: spectrometer, atomic spectroscopy, monochromator, analog-to-digital converter, optical communication, microcontroller, programmable logic devices, USB bus, plug&play

Abstract: Design and implementation of 64-channel spectral analyzer measurement system for ultraviolet spectrum of light is presented. The basic idea was to build a versatile measurement system for spectral analyze in atomic spectroscopy employment using of up-to-date digital and communication solutions. A basic structure and schematic drawing of an atomic spectral analyzer with 64-photomultipliers is presented in Figure 1 and 2. Figure 3 shows a monochromator. The first step in the spectral measurement system an attenuator system with high-voltage power supply system and attenuator module is presented. The next step is analog-to-digital measurement module with an analog-to-digital input module and system controller module. Analogue current-to-voltage converter, voltage-to-frequency converter and frequency-to-digital converter are in the structure of input analog-to-digital module. Figures 7, 8 and 9 present individual converters. All of 64-channels are connected to two digital measurement modules with 32-channels per module. The digital modules are connected to the system controller. The system controller is presented with a block diagram on Figure 10 and contains a microcontroller ATmega103. Its serial and parallel ports are used for communication with digital module, LCD bus, LCD display and USB bus for communication with a personal computer. At the same time, the ATmega103 is connected to a temperature and vacuum sensor with analogue inputs, to FLASH memory programmer with SPI bus and with a serial bus UART to an attenuator module. The high-voltage module and analog-to-digital module are isolated with fibre-optic communication from system controller and attenuator module. Four fibre-optic lines are used from analog-to-digital module to digital module.

Measurement acquisition is carried out in two steps. The first step is the initialization of all system modules. In the attenuator system, the high-voltage for power supply of photomultiplier tubes are set to the initialization state. All digital counters in digital modules are set to the reset state. High-voltage on photomultiplier tubes and reset of digital counter on the digital module is set. Measurement value in the second step is acquired. For increasing reliability of measurement system an auto calibration function in both steps of measurement acquisition is used. In Figure 13, the schematic drawing of multilevel model for communication between user and measurement system is showed. The user can use the system methods and objects. They are represented in Tables 1 and 2. In the results, transfer function and error function of analog-to-digital module, analog-to-digital and digital module together, transfer function of vacuum and temperature sensor and transducer, transfer function of high-voltage regulator, current limiting characteristic of high voltage regulator and transfer function of attenuator module are presented.

1 Uvod

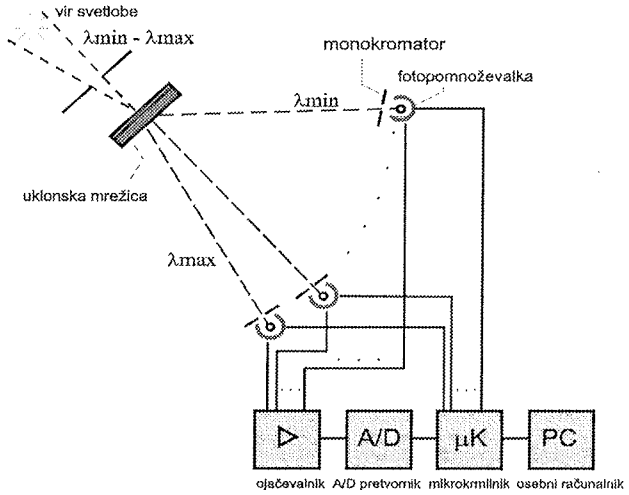
Spektrometri so selektivni instrumenti grajeni za analiziranje posameznega področja elektromagnetnih valov. Spektroskopija se uporablja na primer za analize materialov, ki jih ne smemo uničiti (dragocene slike), materialov, ki niso dostopni (zdravila v zaprtih stekleničkah), pri analizi preveč oddaljenih objektov (raziskovanje zvezd) in podobno. Pri tem se spektroskopija ne omeji samo na vidno svetlobo ampak zajame elektromagnetna valovanja širše, kot so rentgenski žarki, ultravijolična in infrardeča svetloba.

Eno od področji spektralne analize je atomska spektroskopija, ki raziskuje zgradbo snovi. Po načinu delovanja ločimo atomsko: - emisijo, - absorbcijo in - fluorescenco. Pri atomski emisiji analiziramo vir svetlobe (plamen). Pri atomski absorbciji se del svetlobe iz širokopasovnega vira absorbira v plamenu in opazujemo neabsorbirane komponente svetlobe. Pri atomski fluorescenci pa se pod vplivom dodatnega vira pojavijo v plamenu posamezne stimulirane komponente svetobe.

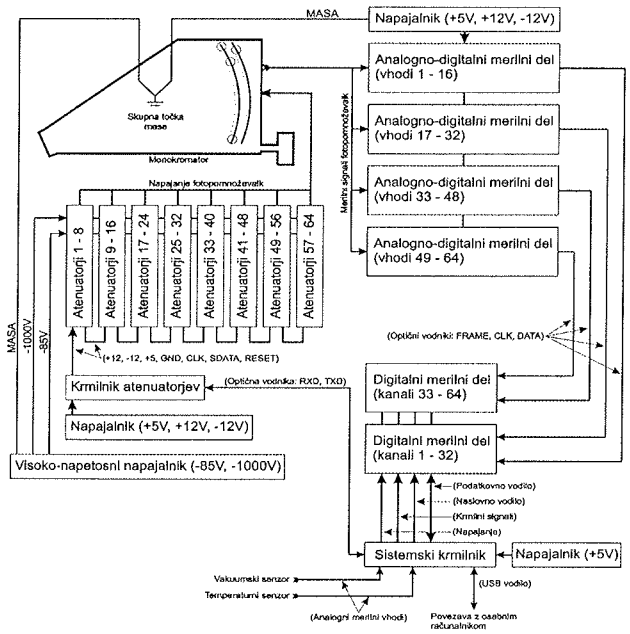
Predstavili bomo merilni sistem spektrometra za analizo ultravijolične svetlobe, ki je uporaben za vse tri načine delovanja /1,2,3/.

2 Zgradba atomskega spektrometra

Atomski spektrometer ima: vir svetlobe na vhodu, monokromator z uklonsko mrežico ali prizmo /2,6/ za razdelitev spektra na komponente, fotopomnoževalne vakuumske elektronke in merilni sistem. Merilni sistem /1,13,16/ vsebuje: vhodne ojačevalnike, analogno-digitalne pretvornike, mikrokrmilnike in komunikacijska vezja za povezavo z osebnim računalnikom.



Slika 1. *Splošna zgradba atomskega spektralnega analizatorja.*
Figure 1. *Basic structure of an atomic spectral analyzer.*

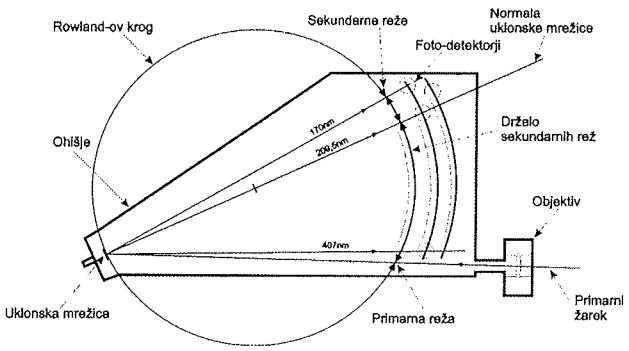


Slika 2. *Blokovna shema atomskega spektralnega analizatorja s 64 fotopomnoževalkami.*
Figure 2. *Shematic drawing of atomic spectral analyzer with 64-photomultipliers.*

2.1 Monokromator

Konkavno zrcalni monokromator proizvajalca spektrometrov Thermo Electron Corporation (ARL model 31000 z 2160 (režami/mm)) vsebuje: primarno režo, konkavno uklonsko mrežico, po principu Rowland-ovega kroga nameščene sekundarne reže in fiksno nameščene fotodetektorje (fotopomnoževalne cevi). Pri tem je razmestitev Paschenova /3/, ki odpravi rabo gibajočih delov. Prednost uklonske mrežice pred prizmo je v njeni enakomerni porazdelitvi svetlobe na posamezne spektralne komponente, slabost pa prekrivanje pasov.

Monokromator lahko deluje v vakuumskem ali zračnem načinu. V vakuumskem načinu delovanja ni absorbcije svetlobe, zato je ta način primeren za ultravijolično svetlobo valovnih dolžin od 170nm do 400nm. V zračnem načinu pa opazujemo svetlobo iz vidnega spektra v območju od 250nm do 610nm. Pri spremembi načina delovanja moramo zamenjati uklonsko mrežico. Sekundarne reže so nameščene kot maske pred fotodetektorji in zagotavljajo osvetlitev detektorjev z ozkim pasom svetlobe - spektralno črto.



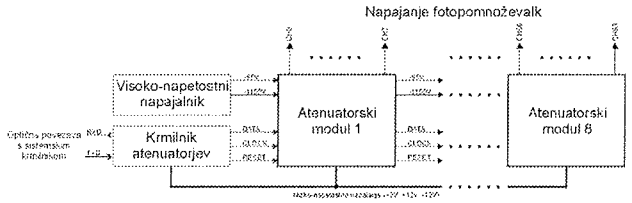
Slika 3. *Monokromator.*
Figure 3. *Monochromator.*

2.2 Fotodetektor

Za detektorje svetlobe so uporabljene fotopomnoževalne vakuumske elektronke - IP27 podjetja Hamamatsu /4/. Fotopomnoževalka IP27 vsebuje devet dinod in pri najvišji napajalni napetosti 1250V zagotovi tokovno ojačenje 10^7. Pri tem naj anodni tok ne preseže 100µA. Za napajanje dinod je uporabljena veriga devetih uporov velikosti 300kΩ.

2.3 Atenuatorski sistem

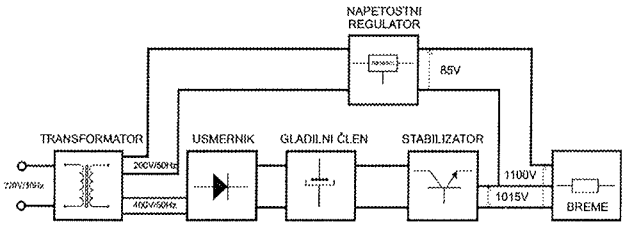
Atenuatorski sistem omogoča izbiranje želene vrednosti napajalne napetosti ločeno za vsako fotopomnoževalko, s čimer nastavljamo ojačenje. Pri višji napajalni napetosti je ojačenje fotopomnoževalke večje in pri enaki intenzivnosti vpadle svetlobe dobimo večji izhodni anodni tok. Ojačenja posameznih fotopomnoževalk je potrebno nastavljati z ozirom na zahteve spektralne analize.



Slika 4. Atenuatorski sistem.
Figure 4. The attenuator system.

Atenuatorski sistem napaja 64 fotopomnoževalk in je sestavljen iz: visokonapetostnega napajalnika, krmilnika atenuatorjev in osmih atenuatorskih modulov z osmimi izhodi.

2.3.1 Visokonapetostni napajalnik



Slika 5. Napajalnik.
Figure 5. Power supply system.

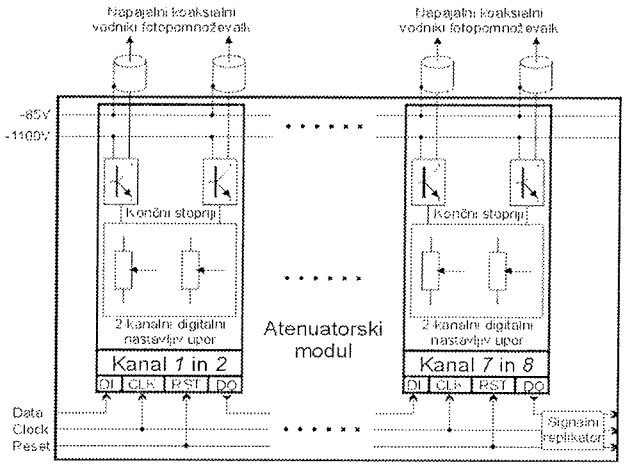
Omrežna napetost je priključena na transformator, ki ima na sekundarni strani navitji z napetostjo 200V in 400V /7/. Iz napetosti 200V je z napetostnim regulatorjem HIP5600 /5/ dobljena napetost -85V za napajanje anod fotopomnoževalk. Posamezna anoda je vezana preko upora velikosti 10kΩ na Millerjev integrator. Le-tega odlikuje velika linearnost. Iz 400 V izmenične napetosti dobimo iz dvovalnega množilnika enosmerno napetost velikosti 1074V, ki jo visokonapetostni stabilizator zmanjša na 1015V. Stabilizirana napetost 1015 V je potrebna za napajanje dinod fotopomnoževalk. Napetostni stabilizator napetosti s tokovno zaščito je narejen z diskretnimi elementi in zagotovi ustrezno napetost za breme z upornostjo do 19,1kΩ.

2.3.2 Atenuatorski modul

Blokovna shema atenuatorskega sistema je podana na sliki 6. Izbira velikosti napajalne napetosti je izvedena s krmilnikom atenuatorjev /8/. Za vsako od 64 fotopomnoževalk je izvedena ločena krmilna stopnja z digitalno spremenljivimi upori DS1267 /9/. V enem digitalno spremenljivem uporu sta dva osem-bitna uporovna delilnika, s katerimi nastavljamo referenčno napetost za napajanji dveh fotopomnoževalk.

Za krmilnik atenuatorjev je uporabljen Atmelov RISC mikrokrmilnik AT90S8515 v CMOS tehnologiji. V mikrokrmilniku vgrajen asinhron zaporedni vmesnik je uporabljen za komunikacijo s sistemskim krmilnikom. Povezava s sistemskim krmilnikom je izvedena po dveh optičnih vodnikih.

Glavni program v mikrokrmilniku ob sprejetem pravilnem ukazu izvede nastavitev želenih vrednosti napajalnih napetosti fotopomnoževalk. Ob sprejetju nerazumljivega ukaza ali ob nepravilnih parametrih ukaza krmilnik atenuatorjev o napaki obvesti sistemski krmilnik, ki glede na tip napake ustrezno reagira.



Slika 6. Blokovna shema atenuatorskega modula.
Figure 6. Block diagram of the attenuator modul.

Iz krmilnika atenuatorjev se željena digitalna vrednost zaporedno vpiše v register digitalnega uporovnega delilnika. Z nastavljeno upornostjo izbiramo napetost na vhodu napetostno-tokovnega pretvornika. Napetostno-tokovni pretvornik je izveden z operacijskim ojačevalnikom in visokonapetostnim tranzistorjem BUX85. Na visokonapetostnem uporovnem delilniku dobimo napajalne napetosti za posamezne dinode fotopomnoževalke /1,7/.

2.4 Analogno-digitalni merilni modul

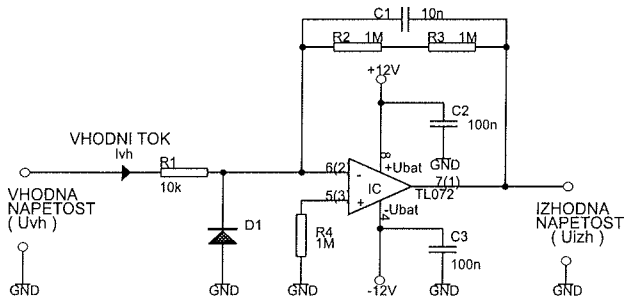
Merilni sistem spektralnega analizatorja je zgrajen iz:

a) štirih vhodnih modulov z: 16 analognimi vhodi, analogno-digitalnimi pretvorniki izvedenimi z napetostno-frekvenčnimi pretvorniki, vezjem za združevanje in izbiranje kanalov (multiplekser);
b) dveh digitalnih merilnih modulov z 32 kanali in
c) modula sistemskega krmilnika.

Analogni vhod vsebuje tokovno-napetostni pretvornik /23/ s prenosno funkcijo opisano z enačbo: $U = - k_{in} \cdot I_{vh}$, kjer je $k_{in} = R_2 + R_3 = 2 \cdot 10^6$ /Ω/. Pričakovano območje vhodnih tokov je od 0 do -2,5 μA, celotno vhodno območje pretvornika pa od 0 do -5μA in izhodno U_{izh} od 0 V do +10 V.

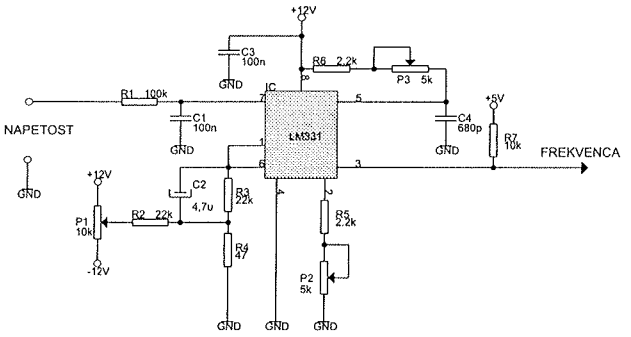
Izbran operacijski ojačevalnik TL072 ima visoko vhodno upornost (JFET tranzistorji), nizek šum, majhna mirovna vhodna tokova in vhodni ničelni tok.

Napetostno-frekvenčni pretvornik je izveden z integriranim vezjem LM331 /20/. Prenosna funkcija napetostno-frekvenčnega (U/f) pretvornika je podana v izrazu: $f = k_{uf}u = 20(kHz/V)U_{izh}$. Za območje vhodnih napetosti od 0 do



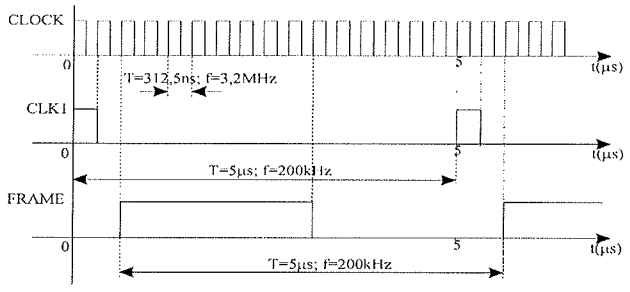
Slika 7. Tokovno-napetostni pretvornik.
Figure 7. The current-to-voltage converter.

10V je območje izhodnih frekvenec je od 0 do 200kHz. V primeru, ko bo vhodni tok v tokovno-napetostni pretvornik večji od -2,5μA, bo U_{iz}>5V in bo izhodna frekvenca večja od 100 kHz.



Slika 8. Napetostno-frekvenčni pretvornik.
Figure 8. The voltage-to-frequency converter.

Da bi zmanjšali število povezav med posameznimi kanali in sistemskim krmilnikom, je na vhodnem modulu dodano vezje za združevanje in izbiranje kanalov. To vezje zajema hkrati vrednosti iz izhodov 16 U/f pretvornikov v taktu CLK1 v vzporedno-zaporedni register. Med dvema impulzoma za zajem pa drugi del vezja sinhrono z uro CLOCK zaporedno odda na treh linijah: signal ure za sinhronizacijo CLK1, 16-bitne podatke posameznega kanala in okno FRAME oziroma okvir, v katerem so poslani podatki posameznega kanala (slika 9).

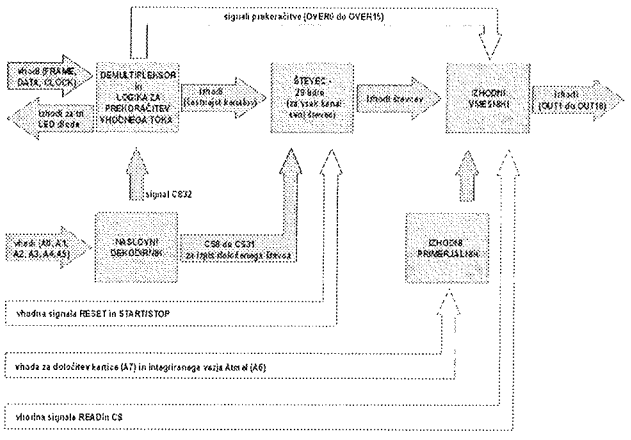


Slika 9. Signali FRAME in CLOCK.
Figure 9. The signals FRAME and CLOCK.

Tako je za povezavo med vhodnim modulom in sistemskim krmilnikom dovolj povezava s tremi optičnimi vodniki za vsakih 16 kanalov. Uporabljeni so Thoshibini digitalni optični povezovalni moduli TORX173 /18/ in TOTX173 /19/. Celotni 16-kanalni združevalnik in izbiralnik je izveden v programirljivem logičnem vezju Lattice ipsLSI1016 /17/.

2.5 Digitalni merilni modul

Dva digitalna merilna modula, z 32 merilnimi kanali na modul, sprejemata merilne signale iz štirih analognih merilnih modulov. Digitalni merilni modul ima dve programirljivi polji logičnih vrat AT40K20LV/21/ z 2 x 16 = 32 merilnimi kanali. V statični RAM vezja AT40K20LV se ob vklopu vpiše konfiguracijska nastavitev iz EEPROM pomnilnika AT17LV512 /22/. V AT40K20LV vezjih se najprej izvrši razdruževanje sprejetih signalov na posamezne kanale, nato pa se preveri za vsak kanal prekoračitev zgornje meje toka iz fotopomnoževalke -2,5μA. Ker se signal v analogno-digitalnem modulu vzorči s frekvenco 200kHz, bo ob nastopu največje vrednosti vhodnega toka -2,5μA na izhodu prisoten impulz v vsakem drugem okviru 16-bitne besede. V primeru večjega toka od -2,5μA se bo impulz pojavil v vsakem podatkovnem okvirju. V tem primeru se izmerjena vrednost izloči. V naslednji meritvi se zmanjša napajalno napetost fotopomno-ževalke in s tem njeno tokovno ojačenje. Po izbranem časovnem intervalu 10s predstavlja vsebina števca vsoto merjenih vhodnih impulzov, ki je premosorazmerna z vhodnim tokom. Pri -2,5μA toka dobimo: (1 impulz/10μs)x10s = 10^6 impulzov. Impulze prešteje 20-bitni števec (2^{20}=1048576). Vrednost 20-bitnega števca za posamezni kanal se poveča s pozitivno fronto prenešenega impulza.

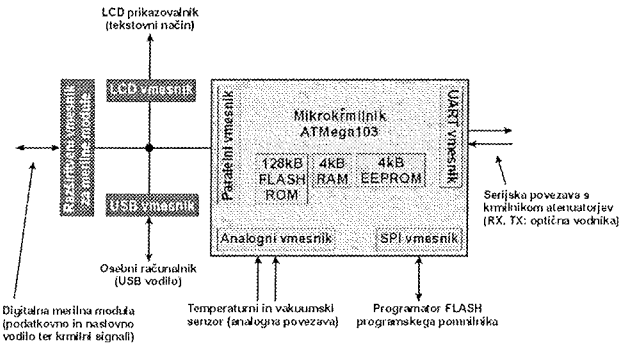


Slika 10. Digitalni merilni modul.
Figure 10. The digital measurement modul.

Naslovne linije A0 do A5 so uporabljene za dekodiranje kanalov, A6 za naslavljanje posameznega integriranega vezja FPGA, A7 pa za naslavljanje digitalnega merilnega modula. CS0 do CS31 so interne naslovne linije po dve na kanal, ker je vodilo 16-bitno in sta potrebni po dve 16-bitni besedi za 20-bitni rezultat. Z CS32 je naslovljen vektor prekoračitve.

2.6 Sistemski krmilnik

Sistemski krmilnik s svojim programom povezuje implementirane module spektralnega analizatorja v funkcionalno celoto.



Slika 11. Blokovna shema sistemskega krmilnika.
Figure 11. Block diagram of the system controller.

Povezave sistemskega krmilnika z drugimi moduli so izvedene z optičnimi vodniki. To so:

- povezava s krmilnikom delilnikov, s katerim nastavljamo napajalno napetost za fotopomnoževalke,
- povezave z digitalnima merilnima moduloma, s katerih dobi izmerjene vrednosti tokov,
- povezava s senzorjem za merjenje temperature in vakuuma v monokromatorju,
- zaporedni vmesnik SPI uporabljen za programiranje programskega FLASH pomnilnika in že omenjena
- povezava z USB vodilom z osebnim računalnikom.

Sistemski krmilnik je 8-bitni mikrokrmilnik ATMega103 /14/ z RISC arhitekturo. Vsebuje programski in podatkovni pomnilnik ter večino vhodno-izhodnih vmesnikov, ki so potrebni za izvedbo sistemskega krmilnika. Za povezavo med sistemskim krmilnikom in USB vodilom je uporabljeno integrirano vezje PDIUSB12 /15/. Na sistemski krmilnik je priključen LCD prikazovalnik s tekstovnim zapisom. Le-ta je zelo uporaben pri razvijanju naprave, saj omogoča sprotno izpisovanje kontrolnih vrednosti sistemskega krmilnika. Ob nastopu napak pri prenosih lahko spremljamo vrednosti in kontroliramo stanje povezav.

Sistemski krmilnik dostopa do števcev digitalnega merilnega modula preko 16-bitnega podatkovnega vodila. Za naslavljanje števcev je uporabljeno osem naslovnih linij in krmilna signala za izbiro integriranega vezja CS in signal za branje oziroma vpisovanje R/W. Za krmiljenje meritev sta dodana signala RESET in START/STOP. S signalom RESET se izbrišejo vsebine vseh merilnih števcev in naprava se pripravi za novo meritev. Meritev se začne s krmilnim signalom START v logičnem stanju enice oziroma se po izbranem intervalu konča s signalom STOP v stanju logične ničle. Vsebine števcev se zadržijo do nastopa RESET signala.

Za boljši nadzor nad delovanjem merilnega sistema so dodani indikatorji na vseh optičnih povezavah. Ob izpadu katere od optičnih povezav ugasne ustrezna svetleča LED dioda.

V času razvoja je možno vpisati vsebine v integrirana vezja iz osebnega računalnika. S tem je odpravljeno zamudno izvajanje programiranja raznih tipov ROM pomnilnikov. Ob tem je enostavno preizkušanje logičnih sklopov celotnega logičnega vezja na izvedenih modulih.

2.6.1 Temperaturni senzor

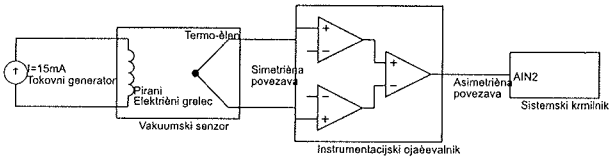
Temperaturni senzor je nameščen na železno ohišje monokromatorja. Specificirani podatki za mono-kromator so podani pri temperaturi 25°C. Dovoljena je sprememba temperature ohišja za ±0,5°C. Uporabljen integriran polprevodniški analogni temperaturni senzor DS699 podjetja Dallas. Pri napajalni napetosti med 2,7V in 5,5V je izhodna napetost senzorja U=6,25(mV/°C) T(°C) + 424mV. Območje senzorja je od -40°C do +125°C in je za naše potrebe preširoko. Prilagoditev nivojev med senzorjem in analogno-digitalnem A/D pretvorniku vgrajenem v vezju sistemskega krmilnika ATMega 103 /14/ je izvedeno z napetostnim ojačevalnikom z ojačenjem A_u=6. Na vhodu analogno- digitalnega pretvornika dobimo pri T= 10°C napetost 2,919V in pri T=65°C napetost 5V. Pri 10-bitnem A/D pretvorniku z območjem med 0 in 5V je korak 4,89mV. S tem izmerimo temperaturo na 0,13°C, kar je za našo napravo zadostovalo.

Temperaturni senzor oziroma izhod ojačevalnika je povezan na prvi analogni vhod sistemskega krmilnika.

2.6.2 Vakuumski senzor

Optične poti, ki so podane za predstavljen monokromator, veljajo samo v primeru vakuuma v komori monokromatorja. Vakuum zagotovi vakuumska črpalka, ki neprestano črpa zrak iz komore monokromatorja. V komori monokromatorja je nameščen vakuumski senzor, katerega izhodni signal se ojači in poveže na drugi analogni vhod sistemskega krmilnika.

Princip delovanja vakuumskega senzorja je Piranijev /12/. Če postavimo v prostor s plinom električno ogrevan kos žice, je njegova temperatura odvisna od pritiska plina, saj je njegova toplotna prevodnost odvisna od spremembe pritiska plina. Temperaturo žice meri termočlen.



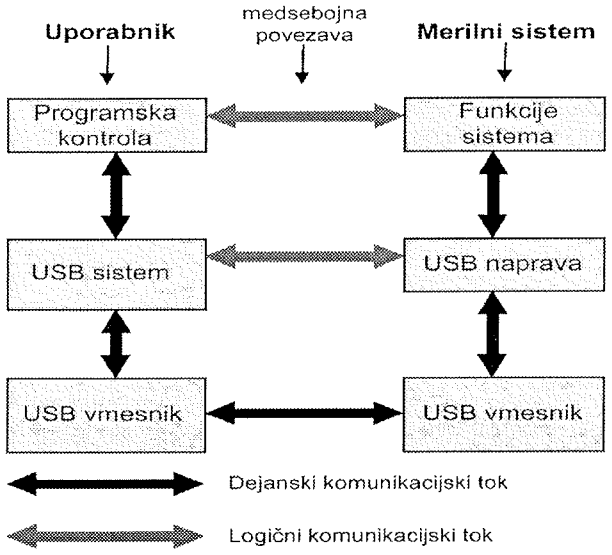
Slika 12. Priključitev vakuumskega senzorja na analogni vhod sistemskega krmilnika.
Figure 12. Simplified connection diagram of vacuum sensor to analog input of system controller.

Območje napetosti iz senzorja je dano v mejah: za normalni zračni tlak P_1=101325 Pa je U_1=0,599 V in za vakuumsko stanje P_2 =101,325 Pa je U_2=4,99 V.

2.7 Programska oprema

Popolno avtomatizacijo merilnega postopka analize svetlobe omogoča programska oprema, ki je nameščena na osebnem računalniku. Osebni računalnik mora imeti vgrajeno USB vodilo za komunikacijo s spektralnim analizatorjem. Programska oprema je izdelana za operacijske sisteme Windows 98, Windows 2000, Windows NT4 in Windows XP v obliki programske komponente tipa ActiveX /10/.

Pri razvoju aplikaciji je možno uporabiti različne programske jezike, kot so Visual C^{++}, Visula Basic, Delphi, C^{++} Bilder in podobni. Uporabnik lahko izvede vizualizacijo glede na svoje potrebe, možno pa je programsko komponento spektralnega analizatorja uporabljati v že izvedenih aplikacijah, kot na primer v urejevalnikih tabel Microsoft Excel, s pomočjo njihovega skriptnega jezika. Prav tako je možno programsko komponento spektralnega analizatorja uporabiti v Internetu z vizualizacijo na poljubnem računalniku, vezanem na splet.



Slika 13. Prikaz večnivojskega modela komunikacije med uporabnikom in merilnim sistemom.
Figure 13. Shematic drawing of multilevel model for communication between user and measurement system.

Ob dinamični priključitvi spektralnega analizatorja na osebni računalnik omenjeni operacijski sistemi avtomatično prepoznajo priključeno napravo pri vključitvi na vodilo (po standardu Plug&Play /11/).

Programska komponenta spekt64.dll je tipa ActivX in predstavlja dinamično programsko knjižnico, v katero je preslikana funkcionalnost spektralnega analizatorja kot celote. Merilne metode in lastnosti izvedene programske komponente delimo na: sistemske metode in lastnosti, ki omogočajoo izvajanje sistemskih ukazov in z njimi povezanih parametrov namenjenih konfiguraciji sistema, ter uporabniške metode in lastnosti, ki so vezane na merilni postopek spektralne analize svetlobe.

Glede na enote delimo sistemske metode in lastnosti: asinhronega zaporednega vmesnika, analogno-digitalnega pretvornika, LCD tekstovnega prikazovalnika, časovnika in digitalnih merilnih modulov.

Asinhroni zaporedni vmesnik	
objekt. **Baudrate** vrednost	objekt. **ReadSerialData**
objekt. **SerialInterfaceOn**	objekt. **WriteSerialData** vrednost
objekt. **SerialInterfaceOff**	objekt. **BytesReceived**
Analogno-digitalni pretvornik	
objekt. **ADCSampleFrequency**	objekt. **ADCStartConversion**
objekt. **ADCOn**	objekt. **ADCValue**
objekt. **ADCOff**	
Tekstovni LCD prikazovalnik	
objekt. **LCDOn**	objekt. **LCDShowCursor** vrednost
objekt. **LCDOff**	
Tekstovni LCD prikazovalnik	
objekt. **LCDOn**	objekt. **LCDShowCursor** vrednost
objekt. **LCDOff**	
Tekstovni LCD prikazovalnik	
objekt. **LCDClear** vrednost	objekt. **LCDWrite** vrednost
objekt. **LCDLocate** vrednost	
asovnik	
objekt. **TimerOn**	objekt. **TimerOff**
objekt. **TimerInterval** vrednost1, vrednost2, vrednost3	
objekt. **TimerStart**	
Digitalni merilni moduli	
objekt. **ResetChannels**	objekt. **Test**
objekt. **ReadChannels**	objekt. **TestAttenuators** vrednost
objekt. **ReadOver** vrednost	

Tabela 1. Sistemske metode in lastnosti.
Table 1. System methods and objects.

Uporabniške metode in lastnosti, ki so podane v tabeli 2, se nanašajo na merilni postopek spektralne analize svetlobe. Pri izvajanju meritve se uporabljajo uporabniške in sistemske metode in lastnosti , ob tem pa se preverja pravilnost delovanja merilnega sistema.

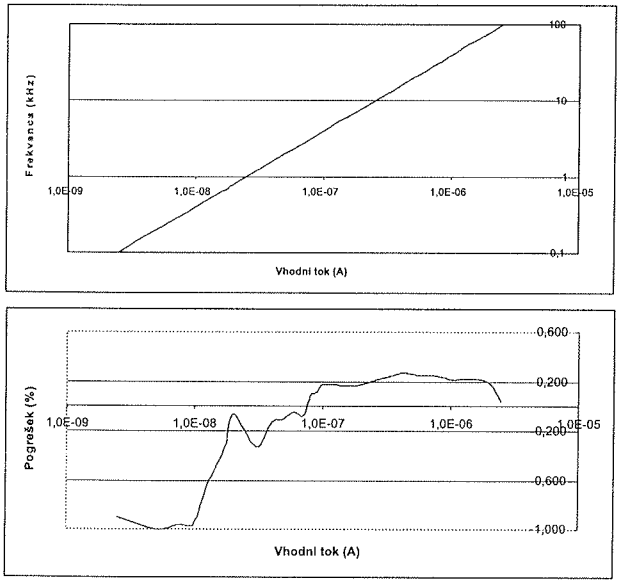
Uporabiake metode in lastnosti	
objekt. **Attenuator** vrednost1, vrednost2	
objekt. **SaveAttenuators** vrednost	objekt. **UpdateAttenuators**
objekt. **LoadAttenuators** vrednost	objekt. **SetAttenuators**
objekt. **MeasureInterval**	objekt. **ResetData**
objekt. **Measure**	objekt. **GetData**
objekt. **GetControl**	objekt. **GetTemperature**
objekt. **GetVacuum**	

Tabela 2. Uporabniške metode in lastnosti.
Table 2. User methods and objects.

3 Rezultati

Delovanje merilnega sistema spektralnega analizatorja smo preizkusili po posameznih sklopih. Analogno-digitalni merilni modul vsebuje tokovno-napetostni in napetostno-

frekvenčni pretvornik. Na vhod dobi tok iz fotopomnoževalk in daje na izhodu impulze s frekvenco od nič do 100 kHz. Za umerjanje modula sta referenčni vrednosti toka na vhodu analogno-digitalnega merilnega modula: - i_{vh}=0, pri tej vrednosti vhodnega toka je frekvenca izhodnega signala pravokotne oblike $4 \leq f_{iz} \leq 5$Hz in - i_{vh}=-2,5μA, pri tej vrednosti toka je frekvenca izhodnega signala f_{iz}=100 kHz. Prenosna funkcija idealnega analogno-digitalnega modula je podana z enačbo premice: $f_{iz}(i_{vh}) = f_{iz}(0) + k_{ifi} \cdot i_{vh} = 40$ (kHz / μA) · i_{vh} . Na sliki 14 je podana prevajalna funkcija in funkcija pogreška analogno-digitalnega merilnega modula.



Slika 14. Prevajalna funkcija in relativni pogrešek analogno-digitalnega merilnega modula.

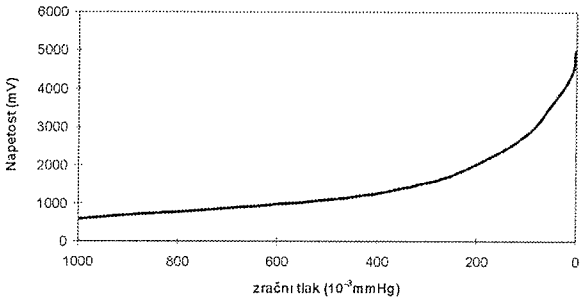
Figure 14. Transfer function and relative error of the analog-to-digital modul.

Največji pogrešek je -1% pri majhnih tokovih do 50 nA ter ±0,2% med 50 nA in 2,5μA. Zaradi večjih pogreškov za tokove pod 50nA se z nastavitvami napajalnih napetosti fotopomnoževalk z atenuatorji zagotovili začetni tok 100nA.

Prevajalna funkcija vakuumskega tipala z instrumentacijskim ojačevalnikom je nelinearna. Za potrebe spektralne analize je pomembno, da je v monokromatorju prisoten vakuum, sama nelinearnost karakteristike ni bistvena.

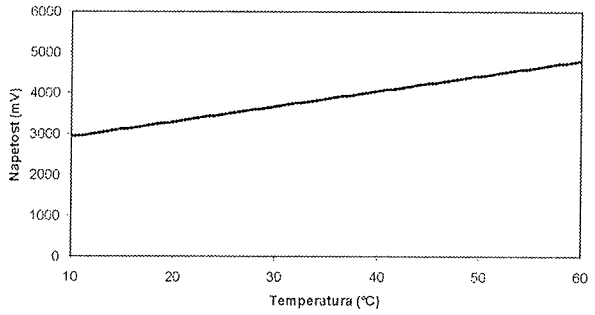
Temperaturna karakteristika tipala in ojačevalnika je v podanem območju linearna in omogoča spremljanje temperature do $\Delta T = \pm 0{,}5^{\circ}C$ točno. Območje zanimivih temperatur je od +10°C do +60°C.

Visokonapetostni stabilizator napetosti za napajanje dinod fotopomnoževalk daje $U_{izhodna}$=1015V napetosti z obremenitvijo do 50mA. Pri tem potrebuje na vhodu napetost U_{vhodna} v območju od 1030V do 1130V. Prevajalna funkcija visokonapetostnega stabilizatorja napetosti je bila izmerjena z ločilnim avto-transformatorjem, zato je območje vhodne napetosti do 1200V.



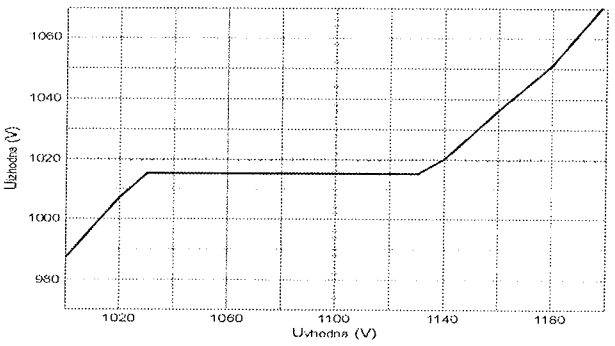
Slika 15. Prevajalna funkcija vakuumskega tipala in instrumentacijskega ojačevalnika.

Figure 15. Transfer function of vakuum sensor and instrumentation amplifier.



Slika 16. Prevajalna funkcija temperaturnega tipala in ojačevalnika.

Figure 16. Transfer function of the temperature sensor and amplifier.

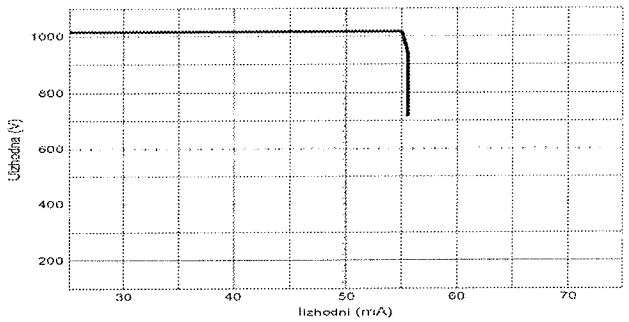


Slika 17. Prevajalna funkcija visokonapetostnega stabilizatorja napetosti.

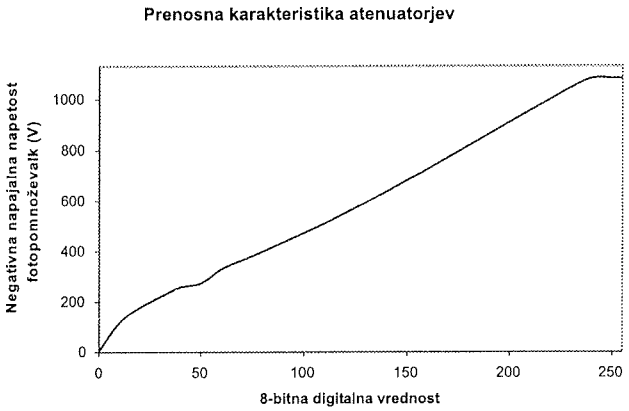
Figure 17. Transfer function of high voltage regulator.

Iz obremenilne karakteristike visoko-napetostnega napajalnika, vidimo da je največji tok do 55mA.

Atenuatorski moduli nastavljajo napetosti posameznih fotopomnoževalk. Prevajalno funkcijo smo izmerili od začetne vrednosti 0 do končne vrednosti 255. V območju, ki je potrebno za nastavljanje napetosti fotopomnoževalk od 300V do 1100V je prevajalna karakteristika linearna.



Slika 18. *Obremenilna karakteristika visokonapetostnega stabilizatorja napetosti.*
Figure 18. *Current limiting characteristic of high voltage regulator.*



Slika 19. *Prevajalna funkcija atenuatorskih modulov.*
Figure 19. *Transfer function of the attenuator moduls.*

4 Sklep

Vodilna podjetja, ki izdelujejo atomske spektrometre, so Advance Research Laboratories (ARL), Perklin Elmer in Hewlett Packard. Ker je število spektrometrov v uporabi relativno majhno glede na druge merilne sisteme, je posodabljanje merilnih sistemov počasno. V prispevku smo predstavili možnosti realizacije 64-kanalnega merilnega sistema namenjenega za spektralno analizo ultravijoličnega svetlobnega spektra. Ugotovili smo, da je z novimi rešitvami možno izgraditi učinkovite merilne sisteme, pri tem pa je dodana: - komunikacija s svetlobnimi vlakni med posameznimi moduli merilnega sistema, ki zagotovi galvansko ločitev med stopnjami, - hitra komunikacija med merilnim sistemom in osebnim računalnikom preko USB vodila, - upravljanje z merilnim sistemom preko spleta.

Programska oprema v merilnem sistemu omogoča hitro prilagajanje spektralne analize za različne tipe analize. Pri tem je nastavljanje ojačenja fotopomnoževalk neposredno z mikrokrmilnikom samo ena od prednosti predlagane posodobitve analizatorja spektra.

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Prispelo (Arrived): 08.09.2003 *Sprejeto (Accepted): 25.02.2004*

POVZETKI MAGISTRSKIH DEL IN DOKTORSKIH DISERTACIJ V LETU 2003
M. S. and Ph. D. ABSTRACTS, YEAR 2003

MAGISTRSKA DELA

Naslov naloge: **Miniaturni optični merilnik tlaka za biomedicinske aplikacije**

Avtor: **Edvard CIBULA, univ. dipl. inž. el.**

Mentor: **doc. dr. Denis Đonlagič; komentor izr. prof. dr. Boris Tovornik**

Univerza v Mariboru, Fakulteta za elektrotehniko, računalništvo in informatiko

V okviru magistrske naloge je predstavljena realizacija prototipa miniaturnega optičnega merilnika tlaka za uporabo v biomedicini, katerega senzorski del je izveden v obliki Fabry-Perot interferometra z membrano, postavljeno v notranjost vdolbine na koncu standardnega optičnega vlakna premera *1251 μm*. Vdolbina na koncu optičnega vlakna je izdelana s postopkom površinske mikroobdelave na osnovi jedkanja SiO2+GeO2 kompozitne strukture optičnega vlakna. Podani so teoretični opis, tehnika procesiranja optičnih signalov, tehnologija izdelave ter eksperimentalni rezultati, ki kažejo uporabnost merilnika v področju tlakov 0-40 kPa.

Naslov naloge: **Polprevodniške strukture z resonančnim tuneliranjem**

Avtor: **Uroš Merc, univ.dipl.inž.el.**

Mentor: **Prof. dr. Franc Smole**

Univerza v Ljubljani, Fakulteta za elektrotehniko

V tem delu predstavljamo fizikalno sliko in princip delovanja polprevodniških heterostruktur: dioda z resonančnim tuneliranjem in superrešetka. Medtem ko je dioda z resonančnim tuneliranjem zgrajena iz treh nanometrskih plasti dveh različnih polprevodnikov, se superrešetka sestavljena s periodičnim nizanjem večjega števila zaporedno izmenjujočih se dveh različnih polprevodniških materialov z različnima energijskima režama. V strukturi z večjim številom period, podobno kot v kristalni zgradbi, nastajajo energijski pasovi - m minipasovi, ki pod vplivom zunanjega električnega polja razpadejo v diskretna lokalizirana stanja. Razpad drastično vpliva na transport elektronov prek strukture in posledično na električne karakteristike strukture, med katerimi je najpomembnejša negativna diferencialna upornost v tokovno napetostni karakteristiki. Slednja je tudi najzanimivejša značilnost diod z resonančnim tuneliranjem. To omogoča izvedbo številnih novih zanimivih aplikacij, od katerih so mnoge prav predstavniki optoelektronike.

Ker znašajo debeline plasti v superrešetkah le nekaj nanometrov, se je pri njih analizi potrebno zateči h kvantnomehanskim fenomenom, kot je resonančno tuneliranje, ki ga prvič srečamo pri strukturah z dvema barierama. V delu izvajamo analizo z reševanjem enoelektronske 1D Schroedingerjeve valovne enačbe, ki jo razvijemo v enačbo razpreševalnih matrik. Ta nam služi za določanje valovne funkcije v strukturi in transmisijskega spektra strukture, ki nam nazorno kažeta tako formacijo energijskih minipasov kot tudi vpliv električnega polja na njih. Naš namen je bil s pomočjo numerične analize, ki predpostavlja končno število plasti, spoznati delovanje diod z resonančnim tuneliranjem in superrešetkastih struktur ter pri tem spoznati svetlo prihodnost njihove uporabe, ki se nam obeta.

V tem delu bomo za uvodom predstavili osnove kvantnomehanskega tuneliranja, pri čemer bomo z uporabo enačbe efektivne mase predstavili enostavnejše enodimenzionalne probleme, kot so potencialna stopnica, bariera in jama. S tem bomo postavili temelje, na podlagi katerih bomo lahko razložili fenomen resonančnega tuneliranja. Po tem, ko bomo spoznali diode z resonančnim tuneliranjem in nekaj njihovi izpeljank ter posebnosti ,se bomo v četrtem poglavju posvetili kaskadnim RT strukturam z dvema barierama in še posebej superrešetkam. Pri slednjih bo analiza temeljila na Blochovih oscilacijah in Wannier-Stark lestvenih stanjih. Na koncu bomo spoznali še nekaj področij uporabe superrešetk z najpomembnejšimi predstavniki.

Naslov naloge: **Zasnova in izvedba grafičnega procesorja v FPGA tehnologiji**

Avtor: **Aleš Stojan**

Mentor: **dr. Andrej Žemva**

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Prikazovalniki s svetlečimi diodami (LED) so se že močno razširili. Srečamo jih skoraj na vsakem koraku, od najmanjših in najenostavnejših kot so digitalne ure, do velikih barvnih LED zaslonov. Krmiljenje je zahtevna naloga in glede na velikost LED zaslona in tip svetlobnih kartic zahteva bolj ali močan procesor (CPU).

Za krmiljenje večjih LED prikazovalnikov sam procesor (CPU) ne zadostuje, uporabiti moramo še neko dodatno vezje, ki ga imenujemo grafični procesor. Ta razbremeni procesor in hkrati zagotovi tudi stabilno osveževanje.

Magistrska naloga opisuje načrtovanje grafičnega procesorja z uporabo FPGA programabilnih vezij. Najprej so predstavljeni LED prikazovalniki in programsko okolje, tako da dobimo občutek, kakšna je funkcija grafičnega procesorja, nato sledi postopek načrtovanja grafičnega procesorja.

V prvem poglavju so zasloni razdeljeni po skupinah za vsako je opisano, kateri zasloni sodijo vanjo, kakšne lastnosti mora imeti krmilnik, kje so njegove pomanjkljivosti in omejitve. Prikazovalniki s svetlečimi diodami so sestavljeni iz dela, ki prikazuje informacije (LED zaslon) in iz dela, ki sprejema informacije iz zunanjega sveta in generira signale za prikaz želenih podatkov na zaslonu (krmilnik). Krmilnik razdelimo na procesorski del (CPU) in grafični procesor.

Princip delovanja je pokazana s pomočjo blokovnih shem, dodani so tudi izračuni za minimalne frekvence urinih signalov, s katerimi moramo brati podatke iz pomnilnika ali pošiljati informacije na zaslon.

Celoten sistem prikazovalnikov, filozofija dela in programska oprema so opisani v drugem poglavju. Ideja pri razvoju in postavitvi sistema je bila zgraditi tako kombinacijo LED zaslonov, osebnega računalnika in programske opreme na njem, da lahko zelo enostavno upravljamo s prikazovalniki in nam ni treba ničesar vedeti o njihovem delovanju. Na PC-ju že imamo nameščeno programsko opremo s funkcijami, ki komunicirajo z zasloni. Uporabnik programira svojo aplikacijo na najvišjem nivoju in le kliče funkcije iz knjižnice.

Tak princip funkcioniranja sistema je mogoč, ker se v krmilniku grafični procesor prilagaja različnim vrstam svetlobnih kartic. Procesor ima ne glede na vrsto zaslona vedno isti način dela.

V uvodnem delu tretjega poglavja so naštete in razložene lastnosti, ki jih mora imeti grafični procesor. V nadaljevanju je najprej opisan princip delovanja. CPU zlaga podatke v video pomnilnik, grafični profesor pa jih jemlje ven in prikazuje na zaslonu.

Na osnovi izračunov frekvenc za posamezne signale in zahtevanih časovnih potekov je podana blokovna shema rešitve.

Avtomat smo sestavili iz dveh modulov. Za oba je shematično prikazano, iz katerih gradnikov sta zgrajena, da dobimo na izhodi signale želenih oblik. Opisane so tudi funkcije posameznih gradnikov in način delovanja.

Navedena rešitev je specifična za postavljene zahteve. V naslednjem poglavju je predstavljeno, kako lahko avtomat naredimo bolj univerzalen in kakšne lastnosti mu lahko še dodamo. Opisano je, kakšne spremembe moramo narediti za krmiljenje statičnih zaslonov, kako se lotimo načrtovanja avtomata, ki je sposoben prikazovati sliko tudi v barvnih odtenkih in na kakšen način lahko v grafični procesor dodamo avtomat za animacije oziroma razne efekte.

V zadnjem delu je predstavljen fizični izgled krmilnika in njegova aplikacija v prikazovalnikih različnih oblik, ki so vsi del sistema za obveščanje potnikov. Prikazovalniki se razlikujejo tako po številu pik kot po velikosti uporabljenih svetlobnih kartic.

Naslov naloge: **Elektronski napetostni vir z digitalno korekcijo izhodne vrednosti**

Avtor: **Matjaž Mavrer**

Mentor: **prof. dr. Janez Nastran**

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V pričujočem delu je utemeljen koncept enofaznega elektronskega napetostnega vira z digitalno korekcijo izhodne vrednosti. Namenjen je napajanju napetostnih tokokrogov števcev električne energije v času njihovega umerjanja in kontrole. Vir omogoča generiranje sinusne napetosti efektivne vrednosti od 30V do 320V s frekvenco od 45 Hz do 65 Hz. Tej napetosti je možno kontrolirano dodajati tudi višjeharmonske komponente (do 30-te). Izhodna moč vira (60 VA) zadošča hkratnemu napajanju do največ petih števcev električne energije. Topologija vira je preprosta, tako da omogoča serijsko proizvodnjo. Ker je vir sestavljen iz elementov široke potrošnje, katere je na tržišču mogoče dobiti po zmerni ceni, bo s takim izdelkom mogoče uspešno nastopiti na tržišču.

Osrednji del vira je močnostni ojačevalnik, zgrajen v obliki polmostičnega razsmernika z izhodnim ločilnim transformatorjem. Predlagana topologija ojačevalnika onemogoča generiranje nezaželene enosmerne komponente. Proženje tranzistorjev je izvedeno na principu pulzno-širinske modulacije želene vrednosti. Poseben poudarek je na dimenzioniranju izhodnega filtra, čigar naloga je preprečevanje prehajanja nezaželenih višjkeharmonskih komponent na breme. Istočasno pa mora imeti filter v delovnem področju čim manjšo frekvenčno odvisnost ojačenja in faznega kota med želeno in dejansko napetostjo odprtega regulacijskega kroga. Zaželeno je tudi ,da se na izhodnem filtru troši čim manj energije, zaradi katere bi se znižal energijski izkoristek naprave. S klasičnim LC filtrom zastavljenih ciljev nisem mogel doseči. Zato sem s pomočjo simulacijskih orodij zasnoval modificiran LC filter, katerega frekvenčna odvisnost ustreza zahtevam pri opisanem, primeru uporabe. V delu je podana celotna regulacijska shema vira, ki je izvedena v dveh nivojih. Notranja napetostna regulacijska zanka kompenzira padec napetosti na parazitnih impedancah filtrske dušilke in izhodnega transformatorja. Istočasno tudi odpravlja posledice nelinearnosti uporabljenih elementov in nihanja enosmerne napetosti na sponkah razsmernika. Tako uspešno znižuje pogrešek izhodne napetosti vira na manj kot dva procenta želene vrednosti.

Ker se breme vira tekom delovanja občutno ne spreminja in ker je notranja regulacijska zanka stabilna, je predlagan nov koncept nadrejene regulacije. To je digitalna korekcijska zanka. Ta ob diskretnih intervalih vzorči razliko med želeno in dejansko napetostjo ter glede na izmerjeni pogre-

šek ustrezno korigira želeno napetost. S tem se pogrešek izhodne napetosti zniža na vrednost znotraj ozkih predpisanih mej.

Generiranje vrednosti želene napetosti je realizirano s pomočjo osebnega računalnika in s posebej za ta primer razvitega vezja. Uporabnik na osebnem računalniku s pomočjo ustrezne programske opreme generira tabelo vrednosti referenčne napetosti. Ta tabela se nato prenese v generator referenčnega signala, ki se nahaja znotraj vira. Prenos podatkov in njihovo kasnejše zaporedno branje krmili nadzorna enota, ki je narejena s pomočjo sodobnega programirljivega vezja.

Delovanje izdelanega modela sem preveril z meritvami, ki potrjujejo ustreznost predlagane topologije vira.

Naslov naloge: **Razvojni modul za MC68HC11 z integriranim perifernim vmesnikom PSD834**

Avtor: **Andrej Nussdorfer univ.dipl.inž.el.**

Mentor: **prof. dr. Tadej Tuma**

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Cilj te magistrske naloge je bila izdelava mikrokrmilniškega razvojnega sistema, osnovanega na mikrokrmilniku Motorola MC68HC11. Ta obsega tako strojno opremo (mikrokrmilniško razvojno enoto HC11PSD IDT).

Zelo dobra stran mikrokrmilniške razvojne enote je univerzalnost, zato omogoča uporabniku v kombinaciji z razvojnim okoljem izdelavo raznovrstnih mikrokrmilniških aplikacij. Poleg samega razvoja aplikacij ta enota nudi tudi možnost preizkušanja programske opreme v živo, saj se jo lahko brez kakršnekoli spremembe uporabi kot prototipni sistem.

Mikrokrmilniška enota je sestavljena iz sledečega:

- Mikrokrmilnik Motorola MC68HC11A1FN.
- Programabilna sistemska enota PSD834F2, ki vsebuje
- 8kBajtov BIOS programskega pomnilnika
- 8kBajtov Uporabniškega programskega FLASH pomnilnika
- 8kBajtov Uporabniškega podatkovnega RAM pomnilnika
- Dva 8-bitna vhodno/izhodna vmesnika
- Priključek RS-232 s pretvornikom nivojev
- Napetostni regulator
- Reset vezje
- LED prikazovalnik napajalne napetosti
- RESET tipka
- MODE tipka
- Napajalni priključek
- Razširitveni priključek
- Vhodno/izhodni priključek

Razvojna enota je, kot že rečeno, zgrajena na osnovi mikrokrmilnika MC68HC11A1. Prednost tega mikrokrmilnika je velika količina vgrajenih enot, kar poenostavi vezje same enote. Z uporabo programabilnega sistemskega vezja PSD834F2, pa je že tako enostavno vezje še bolj okleščeno. Kljub vsem v mikrokrmilniku vgrajenim enotam pa je razvojni sistem načrtovan tudi s pogledom na odprtost in razširljivost. To seveda le še poveča končno uporabnost tega sistema.

Še tako izpopolnjena mikrokrmilniška enota je brez ustrezne programske opreme le neuporaben kup plastike. Prav programska oprema enoto oživi. Za življenje same mikrokrmilniške enote skrbi BIOS (Basic Input Output System). Ta je majhen strojni program, ki omogoča osebnemu računalniku nadzor nad mikrokrmilniško enoto. Podajanje podatkov poteka prek RS-232 zaporednega vmesnika in omogoča tako nalaganje uporabniškega programa kot tudi iskanje in odpravljanje napak v programu samem

Mikrokrmilniški sistem ima sledeče značilnosti:

- Mikrokrmilnik Motorola MC68HC11A1FN v razširjenem načinu delovanja:
  - 8-bitni CPE z razširjenim M6800/M6801 naborom ukazov
  - 256 Bajtov vgrajenega RAM pomnilnika
  - 512 Bajtov vgrajenega EPROM pomnilnika
  - 12 vhodno/izhodnih linij z dodatnimi funkcijami
  - 8-kanalni 8-bitni analogno/digitalni pretvornik
  - 16-bitni časovnik (Timer) s posebnimi funkcijami
  - sinhroni zaporedni vmesnik (SPI)
  - asinhroni zaporedni vmesnik (SCI)
  - prekinitve
- Programabilna sistemska enota PSD834F2, ki vsebuje
  - 8kBajtov BIOS programskega pomnilnika
  - 8kBajtov Uporabniškega programskega FLASH pomnilnika
  - 8kBajtov Uporabniškega podatkovnega RAM pomnilnika
  - Dva 8-bitna vhodno/izhodna vmesnika
- BIOS, ki omogoča:
  - Nalaganje uporabniških programov
  - Poganjanje in koračno izvajanje uporabniških programov
  - Bralno/pisalni dostop do celotnega pomnilniškega prostora
  - Prenos podatkov preko zaporednega RS232-vmesnika.

Kljub vsemu, kar BIOS nudi, je le vmesnik med nadzornim osebnim računalnikom in mikrokrmilniško razvojno enoto. Za razvijanje mikrokrmilniške programske opreme je potreben še krmilni program na osebnem računalniku. To je programski paket HC11PSD IDT (Integrated Development Tools). Ta ima vgrajene vse funkcije za razvoj uporabniške programske opreme, vse to pa je zvito v uporabniku prijazno grafično okolje in deluje v vseh Windows operacijskih sistemih (95/98, Me, 2000, XP).

Razvojno okolje nudi možnost pisanja, prevajanje in nalaganja uporabniških programov na mikrokrmilniško razvojno enoto. Tako naložen program je nato na voljo uporabniku za preizkušanje in iskanje napak, pri čemer so mu na voljo različna orodja - koračno izvajanje, programa, opazovalnica (Watches), ustavitvene ročke (Breakpoints), dostop do celotnega pomnilniškega prostora mikrokrmilnika in njegovih vgrajenih registrov. Vse to z namenom čim bolj olajšati odpravljanje napak v uporabniški programski opremi.

Razvojno okolje se odlikuje s sledečimi značilnostmi:

- urejevalnik teksta
- prevajalnik (assembler)
- povratni prevajalnik (disassembler)
- nalaganje programov na razvojni mikrokrmilniško enoto
- poganjanje programov
- korakanje skozi programe
- ustavitvene točke (Breakpoints) opazovalnice (Watches)
- zbirka simbolov
- dostop do vsebine vseh registrov
- dostop do celotnega pomnilniškega prostora
- poznavanje osnovnih številskih sistemov (dvojiški, osmiški, desetiški, šestnajstiški)
- vgrajen zaporedni terminal
- vgrajena pomoč

Predstavljena mikrokrmilniška razvojna enota skupaj z integriranim razvojnim okoljem predstavljata zmogljivo orodje za razvoj mikrokrmilniških aplikacij. Z lastnostmi, ki jih nudi, se močno približuje k profesionalnim razvojnim orodjem, od katerih pa ga loči ocena, ki je v primerjavi s profesionalnimi orodji zelo nizka.

To razvojno orodje je končno namenjeno predvsem za pedagoško delo, saj je obvladanje uporabniku prijaznega grafičnega vmesnika lahka naloga še tako neizkušenega začetnika, nizka cena mikrokrmilniške enote pa naredi ta sistem dosegljiv širokemu krogu študentov in drugih navdušencev.

DOKTORSKE DISERTACIJE

Naslov naloge: **Problem neponovljivosti simulacij električnih vezij**

Avtor: **mag. Matej ŠALAMON, univ. dipl.inž. el.**

Mentor: **izr. prof. dr. Tomaž DOGŠA**

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Simulatorji električnih vezij so danes nepogrešljivo orodje pri načrtovanju integriranih vezij ter pri različnih znanstvenoraziskovalnih dejavnostih. Kljub relativni zrelosti tovrstnih simulatorjev se dogaja, da dajejo napačne rezultate.

Če simulacijo vezja ponovimo z istim simulatorjem na drugem računalniku, pričakujemo, da se rezultati ne bodo bistveno razlikovali. To lastnost imenujemo ponovljivost. Ponovljivost pa lahko postane v različnih okoliščinah problematična. Ponovno simulacijo lahko namreč izvedemo z istim simulatorjem na istem računalniku, z drugim simulatorjem na istem ali drugem računalniku, z istim simulatorjem, inštaliranim na drugem računalniku. V doktorski disertaciji smo se osredotočili na testiranje ponovljivosti rezultatov, ki jih dajejo simulatorji, inštalirani na različnih platformah. Omejili smo se le na simulatorje tipa SPICE in na rezultate analize prehodnega pojava.

Kadar ponovljivost ni zagotovljena, je smiselno oceniti neponovljivost rezultatov simulacij. Ker se odstopanja med referenčnimi rezultati in rezultati ponovne simulacije lahko kažejo na različne načine, smo predlagali tri različne mere. Mera za neponovljivost 1. stopnje je namenjena oceni odstopanj trenutnih vrednosti primerjanih časovnih potekov, mera za neponovljivost II. stopnje oceni njihove ob likovne nepodobnosti, mera za neponovljivost III. stopnje pa oceni odstopanja globalnega obnašanja testnega vezja.

Pri testiranju simulatorjev s pomočjo vezij iz zbirke *CircuitSim90* problema neponovljivosti ni bilo mogoče zaznati. Zato smo simulatorje testirali še s kaotičnimi vezji. Ugotovili smo, da so kaotična vezja pri odkrivanju neponovljivosti zaradi hiperobčutljivosti na začetne pogoje učinkovitejša. Zato smo za testno vezje izbrali predstavnika kaotičnih vezij - Chujev oscilator.

Ugotovili smo, da nekateri simulatorji ne zagotavljajo ponovljivih rezultatov na različnih platformah in da je neponovljivost rezultatov simulacij najpogostejša, če so simulatorji inštalirani na platformah s procesorji različnih proizvajalcev. Neponovljivost posledično povzroči zelo velika odstopanja trenutnih vrednosti primerjanih časovnih potekov in njihovo oblikovno nepodobnost, medtem ko na odstopanja v globalnem obnašanju testnega vezja ne vpliva bistveno.

Proučevali smo tudi vzroke za obravnavani problem neponovljivosti in možnost njegove odprave. Ugotovili smo, da gre lahko za eno ali več napak v programu simulatorja ali prevajalniku, ki dopuščajo različno interpretacijo istih procesorskih ukazov na različnih procesorjih.

Naslov naloge: **Določanje položaja kožnih formacij pri taktilni komunikaciji v navideznih vmesnikih**

Avtor: **mag. Iztok Kramberger, univ. dipl. inž. el.**

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Ljudje brez težav uporabljamo kretnje za komunikacijo z drugimi ljudmi in tako so kretnje kot metoda interakcije uporabnika in stroja bolj naravne in neposredne v primerjavi z obstoječimi napravami, kot so miška, tipkovnica in podobno. Metoda je tudi bolj funkcionalna, saj je uporaba kretenj roke, ki predstavlja pomembno človeško kretnjo, ključnega pomena za izgradnjo prijaznih uporabniških okolij v domeni navidezne ali razširjene resničnosti. Pomembno vlogo za čim bolj intuitiven način interakcije med uporabnikom in strojem ima procesiranje v realnem času. Cilj pričujoče disertacije je razvoj na računalniškem vidu zasnovanega vmesnika in uporabniškega okolja, ki omogočata poglobljeno interakcijo med uporabnikom in strojem znotraj aplikacij navidezne in razširjene resničnosti ter uporabo leteh v sodobnih telekomunikacijskih tehnologijah. Glavni problem sodobnih mobilnih telekomunikacijskih tehnologij predstavlja omejena velikost prikazovalnega polja in načina vnosa podatkov oziroma navigacije same naprave. Za dosego navedenega cilja smo definirali postopke barvnega filtriranja, analize gibanja, prepoznavanja kretenj uporabnika in predlagali model uporabniškega okolja v aplikacijah navidezne ali razširjene resničnosti.

V nalogi smo uporabili metodo barvnega sledenja, kjer smo razvili nov pristop barvnega in prostorskega filtriranja za označevanje kožnih značnic in tvorbe kožnih formacij na nivoju bitnih mask.

Prikazali smo novo strukturo strojnega pospeševanja v obliki digitalnega nelinearnega parametričnega filtra, ki omogoča iskanje kožno obarvanih regij v dvodimenzionalnem slikovnem zaporedju v realnem času. Parametrična zasnova predstavljenega pristopa omogoča samodejno sprotno prilagajanje na spremembe osvetlitve v sceni, kjer obstaja tudi možnost samodejne adaptacije na različne tipe kože. V nadaljevanju smo definirali postopek razpoznavanja dvodimenzionalnega gibanja v slikovnem zaporedju bitnih mask in kasnejšo klasifikacijo temu podrejenih tridimenzionalnih vzorcev gibanja.

Razvili smo metodo izločanja in klasifikacije dvodimenzionalnega gibanja v slikovnem zaporedju bitnih mask, ki uporablja logični operator. Podali smo oceno predlagane metode z obravnavo težav zaradi prekrivanja subjektov ali objektov kožne barve v sceni. Da bi dosegli človeku čim bolj intuitiven način interakcije v predlaganem uporabniškern okolju znotraj aplikacij navidezne ali razširjene resničnosti, smo uporabili stereoskopski računalniški vid, ki vmesniku omogoča določanje položaja v vseh treh prostorskih razsežnostih. Predstavili smo pristop klasifikacije podrejenih tridimenzionalnih vzorcev gibanja, ki predstavljajo potencialne pare aktivnih področij s pripadajočimi epipolarnimi področji na levi in desni dinamični bitni maski. Klasifikacija potencialnih parov temelji na geometrijskih lastnostih aktivnih področij, pogojih stereoskopske neenakosti vzporedne konfiguracije kamer in algoritmu iskanja korespondence, ki uporablja kriterija korespondence za aktivna in pripadajoča epipolarna področja. Predstavljeni so problemi paralakse gibanja ob uporabi časovno-zaporednega video sistema. Pristop določanja prostorskih koordinat navigacijske točke vključuje modeliranje prstne konice uporabnikove roke, ki je uporabljena kot krmilni subjekt. Obravnavali smo vpliv gibanja slikovnih senzorjev, ki vključuje novo metodo kontrole gibanja slikovnih senzorjev z uporabo senzorja pospeška. Predlagali smo pristop ocenjevanja pripadajočih parametrov kontrole gibanja z izračunom zapletenosti scene. Za analizo uporabnikovih kretenj oziroma določanje izraznega stanja in sledenja krmilnega subjekta v domeni taktilne komunikacije smo predlagali pristop časovne analize prostorskega položaja navigacijske točke. Prikazali smo pristop razpoznavanja kretenj navigacije in potrjevanja želene aktivnosti stroja, ki temelji na časovno ustaljenem gibanju in kratkotrajnih anomalijah v časovno odvisni prostorski funkciji gibanja.

Problem sodobnih mobilnih telekomunikacijskih tehnologij smo naslovili z novo predlaganim uporabniškim okoljem, ki vključuje stereoskopska računalniška podatkovna očala, stereoskopsko namestitev kamer in senzor pospeškov. Znotraj uporabniškega okolja smo predlagali uporabniško področje, ki ga uporabnik vidi v danem trenutku, pri tem je le-to prostorsko usklajeno z navigacijskim področjem vmesnika in ga je možno premikati znotraj uporabniškega okolja s sledenjem orientacije uporabnikove glave.

V zaključnem poglavju smo predlagali zasnovo potrebne strojne opreme, ki omogoča izvajanje podanih algoritmov v realnem času in vključuje nov pristop strojno pospešenega barvnega filtriranja.

Naslov nalogr: **Načrtovanje preizkusljivih struktur vzorčenih analognih integriranih SC vezij**

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V disertaciji je predstavljen posplošen pristop k reševanju problematike načrtovanja struktur in postopkov za oscilacijsko preizkušanje osnovnih topologij filtrov, realiziranih s časovno vzorčenimi analognimi SC strukturami.

Izreden razmah elektronskih naprav široke potrošnje čedalje bolj določa poglavitne smernice razvoja polprevodniške tehnologije. V tem kontekstu ponovno narašča pomen analognih oziroma mešanih analogno-digitalnih integriranih vezij in sistemov, saj so tovrstne elektronske naprave v veliki meri odvisne od analognih tehnik obdelave električnih signalov. Proizvajalci sledjo zahtevam tržišča z razvoja

čedalje kompleksnejših namenskih integriranih sistemov, kar prinaša nove izzive na področje načrtovanja vezij, povzroča pa tudi številne težave pri zagotavljanju ustrezne kakovosti proizvodov. Problem postaja vse bolj pereč, saj uveljavljeni pristopi k načrtovanju struktur in postopkov za preizkušanje analognih podsklopov že danes predstavljajo eno izmed ozkih grl pri nadaljnjem razvoju integriranih sistemov. Posledično se povečuje število raziskav, katerih cilj je razvoj novih tehnik in postopkov strukturiranega načrtovanja preizkusljivih analognih integriranih vezij. Zaradi obsežnosti področja, ki je predvsem posledica raznolikosti analognih integriranih vezij, poteka razvoj v različnih smereh. Predstoječe delo se tako osredotoča na načrtovanje učinkovitih postopkov preizkušanja za ožji razred časovno vzorčenih analognih SC filtrskih struktur, ki pogosto nastopajo kot podsklopi v mešanih CMOS integriranih vezjih.

Reševanje problema preizkušanja je tesno povezano s postopkom načrtovanja vezja. Z upoštevanjem pravil in postopkov načrtovanja, ki jih skupno označujemo kot tehnike načrtovanja preizkusljivosti, lahko bistveno olajšamo izvedbo in povečamo učinkovitost preizkusnega postopka. Na področju načrtovanja preizkusljivosti v mešanih analogno.digitalnih integriranih vezjih so bile v preteklih letih predstavljene številne rešitve, le redke pa so se uveljavile tudi v praksi. Posamezne tehnike se po svoji zasnovi precej razlikujejo, vendar jih lahko v grobem razdelimo na načrtovanje struktur za izvedbo vgrajenega samodejnega preizkusa vezja. Prav slednja skupina tehnik naj bi v prihodnosti igrala zelo pomembno vlogo pri zagotavljanju kakovosti kompleksnih integriranih vezij in sistemov, saj odpravlja nekatere omejitve, ki so vezane na uporabo klasičnih proizvodnih preizkuševalnih naprav, ter povečuje zanesljivost delovanja proizvoda skozi celotno življenjsko dobo.

Postopek preizkušanja vezij z oscilacijsko metodo lahko uvrstimo v skupino tehnik za izvedbo vgrajenega samodejnega preskusa. Metoda temelji na predpostavki, da je preizkušano vezje možno pretvoriti v oscilator. V tem primeru lahko napake v vezju odkrijemo s preprostim preverjanjem frekvence oscilacij, pri čemer pa mora biti zagotovljena ustrezna občutljivost izhodnega signala na spremembe parametrov tistih komponent, ki sicer določajo značilno karakteristiko preizkušanega vezja. Osnovni problem oscilacijskega preizkušanja vezij tako predstavlja zasnova ustreznih preizkusnih struktur in taksnih shem rekonfiguracije, ki omogočajo čim bolj učinkovito izvedbo preizkusa. V preteklih letih je bilo objavljenih več prispevkov, ki obravnavajo uporabe oscilacijske metode pri preizkušanju hibridnih in integriranih analognih R-C filtrov in dokazujejo praktično uporabnost postopka v okviru proizvodnega preizkušanja vezij.

Analogne R-C filtre v sodobnih mešanih integriranih vezjih vse bolj izpodrivajo druge tehnologije, ki so precej bolje združljive z digitalno logiko visoke gostote. Osrednji del disertacije se tako nanaša na uporabo oscilacijske metode pri preizkušanju filtrskih struktur, izvedenih v tehnologiji analognih časovnih vzorčenih SC vezij. Predlagane rešitve so namenjene načrtovanju preizkusnih struktur za osnovne podsklope, ki realizirajo prenosne funkcije drugega reda. V delu je predstavljen posplošen teoretičen pristop, ki temelji na analizi splošne prenosne funkcije drugega reda v časovno diskretnem prostoru. Na podlagi izpeljave eksaktnih relacij med parametri, ki opisujejo filtrsko vezje v časovno zveznem prostoru in koeficienti časovno diskretne prenosne funkcije, so določeni splošni pogoji za vzpostavitev vzdrževanih oscilacij v preizkušanem vezju. V nadaljevanju sta obravnavana dva različna pristopa k transformaciji SC stopnje drugega reda v oscilatorsko strukturo. Za preprostejšo tehniko, ki temelji na notranji rekonfiguraciji SC stopnje s pomočjo obstoječih ali dodatno vgrajenih stikal je na podlagi računalniških simulacij na specifičnem primeru in posplošene analize delovanja preizkusnega sistema ugotovljeno, da ni primerna za uporabo v integriranih vezjih. V nadaljevanju dela se tako osredotočamo na rešitev, ki temelji na uporabi zunanje nelinearne povratne zanke in omogoča boljši nadzor nad pogoji obratovanja vezja med preizkusnim postopkom . Realizacija nelinearne povratne zanke v integriranih vezjih je relativno preprosta, vendar metoda predvideva, da preizkušano vezje med priklopnima vozliščema realizira pasovnoprepustno prenosno funkcijo z zadostno selektivnostjo. Ob predpostavki izpolnjevanja tega pogoja sta na podlagi opisne prenosne funkcije SC stopnje drugega reda izpeljana izraza za frekvenco in amplitudi oscilacij transformiranega vezja. Splošne teoretične izpeljave so prenesene na univerzalno Fleischer-Lakerjevo SC stopnjo drugega reda (FLB), ki predstavlja osnovo najbolj razširjenim SC filtrskim topologijam. Za FLB konfiguracije, ki realizirajo različne tipe prenosnih funkcij, so predlagani ustrezni postopki pretvorbe, ki omogočajo izvedbo oscilacijskega preizkusa vezja z nelinearno povratno zanko. Ker je frekvenca oscilacij določena s frekvenco pola preizkušenega vezja, so za specifične topologije SC filtrov, ki realizirajo kompleksne ničle v števcu prenosne funkcije, predlagani dodatni postopki rekonfiguracije, ki ničle pretvorijo v pole sistema.

Izpeljave teoretičnih osnov za načrtovanje oscilacijskega preizkusa izhajajo iz idealnih modelov komponent vezja. Ker v praksi karakteristike komponent niso idealne, prihaja z vgradnjo prez6kusne infrastrukture do dodatnih odstopanj parametrov sistema med normalnim obratovanjem, kot tudi do vnosa napak v rezultate preizkusa. V integriranih vezjih običajno ni možna naknadna kompenzacija odstopanj ali pa umerjanje sistema, zaradi česar je potrebno ustrezno ovrednotiti vplive različnih neidealnosti. Na podlagi analize univerzalne SC stopnje z neidealnimi modeli komponent lahko ugotovimo, da predstavlja poglavitno težavo vnos šuma preko preizkusne infrastrukture, kar pa je možno reševati z ustreznim načrtovanjem. Drugo slabost uporabe nelinearne povratne zanke predstavlja zmanjšanje zanesljivost merilnega postopka, ki izvira iz neidealnosti karakteristike nelinearnega elementa. Z analizo modela te neidealnosti lahko dokaj dobro ocenimo vneseno merilno napako ter jo ustrezno upoštevamo pri vrednotenju merilnih rezultatov.

V zadnjem delu disertacije je podana ocena ustreznosti predlaganih rešitev oscilacijskega preizkušanja SC vezij. Na podlagi računalniških simulacij realističnih modelov vezja v vgrajenimi okvarami sem ocenil doseženo pokritje napak. Ločeno sem ovrednotil učinkovitost oscilacijske preizkusne metode pri odkrivanju katastrofalnih in parametričnih napak v osnovnih komponentah vezja, na izbranem primeru pa sem izvedel podrobnejšo analizo in primerjavo z nekaterimi drugimi znanimi rešitvami. Končni rezultati nakazujejo, da predstavlja oscilacijska metoda učinkovito alternativo pri preizkušanju mešanih analogno digitalnih integriranih vezij.

Naslov naloge: **Analiza in optimizacija integriranih magnetnih mikrosistemov**

Avtor: **Albin Pevec**

Mentor: **prof. dr. Janez Trontelj**

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Doktorska disertacija predstavlja postopke pri analizi in optimizaciji integriranih magnetnih mikrosistemov. Sedanji trend integracije čim večjega števila elementov nekega sistema na eno silicijevo rezino je prisoten tudi pri magnetnih mikrosistemih. Magnetni mikrosistemi so takšni sistemi, ki zaznavajo ali velikost, smer, predznak, prostorsko porazdelitev ali prisotnost enosmernega ali izmeničnega magnetnega polja. Vedno pogosteje se senzor in pripadajoči elektronski sklopi za obdelavo senzorskih signalov integrirajo na eni silicijevi rezini. S tem se poenostavi in poceni izdelava sistema za merjenje magnetnega polja.

Pri integraciji senzorja na rezino je potrebno ugotoviti, da ima ta integrirani senzor ponavadi slabše lastnosti kot diskretni senzorji, ki so izdelani z namensko tehnologijo. Ker se za integracijo senzorjev uporablja standardna mikroelektronska tehnologija, se tehnologija izdelave ne prilagodi posebnim zahtevam senzorja. Tako je potrebno lastnosti senzorja sprejeti takšne, kakršne so, pozornost za izboljševanje lastnosti pa preusmeriti v optimizacijo elektronskega procesiranja senzorskih signalov. Hallov magnetni senzor je najprimernejši za integracijo na standardnih mikroelektronskih procesih CMOS. Obravnavani senzor je Hallov senzor, ki je posebej prilagojen uporabi v senzorskem polju. Ima minimalne dimenzije, zato ga lahko uporabimo kot točkasti senzor, ali pa ga uporabimo v večjem številu za izboljšanje razmerja signal/šum. Tradicionalni senzorji imajo ponavadi večje dimenzije, zaradi katerih pa so nekatere lastnosti, kot npr. ničelna napetost, boljše.

Z analizo se ugotovijo vse lastnosti integriranega Hallovega senzorja, se ovrednotijo in zberejo v modelu senzorja. Ta model se uporabi pri električni simulaciji postopkov obdelave senzorskih signalov, ki izboljšajo lastnosti senzorja. S temi postopki lahko nekatere lastnosti senzorskih elementov izboljšamo ali odpravimo.

Pri uporabi Hallovega senzorja v magnetnih mikrosistemih, kjer je prisotno enosmerno magnetno polje, je najbolj nezaželena lastnost njegova ničelna napetost, ki nastane zaradi nepopolnosti izdelave. Za odpravo te nezaželene lastnosti poznamo več načinov, zaradi specifičnosti predstavljenega senzorja minimalnih dimenzij pa se uporabijo postopki posebej prilagojeni velikim ničelnim napetostim. Predstavljena je metoda večfaznega vrtenja priključkov senzorja in metoda uporabe senzorskih parov. Pri vrtenju priključkov je postopek takšen, da se vrtenje toka in napetostnih priključkov senzorja izvaja v vse štiri smeri krakov senzorja, pri čemer se nato z ustreznim procesiranjem signalov posameznih faz lahko izloči ničelna napetost. Pri uporabi para senzorjev se predpostavi, da sta zelo podobno izdelana in imata torej tudi enake nepravilnosti. Če sedaj priključke teh dveh senzorjev ustrezno zavrtimo za 90°, izhodne signale obeh senzorjev pa seštejemo, lahko dosežemo drastično zmanjševanje ničelne napetosti. Ustrezno kombiniranje teh dveh metod nam omogoča doseči najboljše rezultate.

Naslednja nezaželena lastnost magnetnega mikrosistema je šum. Šum v magnetnih mikrosistemih je sestavljen iz kombinacije termičnega šuma in šuma 1/f. Pri uporabi magnetnega mikrosistema za zaznavanje enosmernega ali nizko-frekvenčnega magnetnega signala je najbolj nezaželena komponenta šum 1/f, ki ima največjo gostoto pri nizkih frekvencah. Za odpravo te lastnosti se uporabi metoda vrtenja, ki je alternacija priključkov senzorja s komutacijsko frekvenco, po ojačitvi signalov pa se rekonstruira originalni signal. Pri vrtenju se komponenta šuma 1/f preslika na okolico komutacijske frekvence, ki je mnogo višja od signalnega frekvenčnega pasu in se zato lahko enostavno izloči z nizko-prepustnim filtrom.

Zaradi minimalnih dimenzij se le-ta lahko uporabi v večjem število na eni silicijevi rezini. S tem se odpirajo nove možnosti uporabe integriranega Hallovega senzorja. Ustrezno razporejeno polje senzorjev lahko zaznava prostorsko porazdeljena magnetna polja in s tem lahko posredno preko magnetnega polja zaznava položaj vira magnetnega polja proti integriranemu vezju. Zaradi uporabe magnetnega polja kot posrednika informacije se pri tem izognemo mehanskemu stiku med merjencem in integriranim vezjem, kar je pomembno v aplikacijah, kjer je stik med njima nemogoč ali pa povzroča obrabo (npr. potenciometer).

Naslednja nezaželena lastnost integriranega Hallovega senzorja je njegova časovna spremenljivost. Lastnosti senzorja se lahko spremenijo pod vplivom zunanjih ali notranjih dejavnikov, kot so temperatura, mehanske sile, procesne spremembe itn. Za odpravo te nezaželene lastnosti se uporabi metoda avtomatske nastavitve, ki med delovanjem nenehno prilagaja občutljivost magnetnega mikrosistema na pravilno vrednost. Ta metoda deluje z dovajanjem referenčnega magnetnega signala, ki ima višjo frekvenco od koristnega frekvenčnega pasu merjenega signala.. Za dovajanje referenčnega signala se uporabi integrirana tuljava in referenčni tok. Odziv na referenčni signal se izmeri in

primerja s pričakovanim odzivom, morebitna razlika pa se uporabi za krmiljenje nastavitvenega toka Hallovega senzorja. S prilagajanjem tega toka se prilagodi občutljivost na pravilno vrednost. Ker je frekvenca referenčnega signala nad frekvenčnim pasom merjenega signala se lahko enostavno izloči in tako ne moti osnovne funkcije merjenja signalov.

Predstavljeni integrirani Hallov senzor in večina metod za izboljševanje lastnosti le-tega se uporablja v integriranem vezju za merjenje gostote magnetnega polja. Na primeru tega magnetnega mikrosistema je prikazano delovanje optimizacijskih metod, kot del celote, prav tako pa so razvidne težave, ki nastanejo pri integraciji senzorjev na silicijevo rezino, ki jo deli z ostalimi elektronskimi sklopi. Pri tem je potrebno zelo skrbno razporediti senzorje in posamezne podsklope, da ne pride do medsebojnih motenj. V nasprotnem primeru lahko nezaželeni signal, ki nastane zaradi medsebojnih presluhov preglasi koristni signal.

Izdelava in evaluacija vzorcev je zelo pomemben del analize integriranih senzorjev. Pri merjenju lastnosti senzorjev je največjo težavo predstavljala izdelava dovolj natančnega magnetnega polja. Le-ta ni odvisen samo od električnih parametrov, ampak tudi od položaja in oddaljenosti senzorja od vira magnetnega polja. Pri tej karakterizaciji so nam v veliko pomoč integrirane tuljave, kjer so dimenzijski parametri zelo natančni, saj so odvisni od natančnosti izdelave integriranega vezja.

Natančna evaluacija nam omogoči analizo in s tem modeliranje lastnosti integriranih senzorjev. S pomočjo modela se te lastnosti lahko izboljšajo, kar nas privede do vedno boljših optimizacijskih metod, s tem pa je krog razvoja sklenjen.

Naslov naloge: **Raziskave integriranih bralnikov v sistemih za brezkontaktno identifikacijo in komunikacijo**

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V disertaciji raziskujemo možnosti za izvedbo v celoti integriranega bralnika v sistemu za brezkontaktno komunikacijo in identifikacijo, izsledke raziskav pa preverimo v praksi z zasnovo integriranega bralnika v frekvenčnem območju okoli 13,56MHz.

Ob sedanjem stanju tehnike je uporaba bralnika pametnih kartic manjše moči v enem integriranem vezju običajna v frekvenčnem območju okoli 125kHz. Integrirani bralnik je majhen in cenen. S stališča sistemskega načrtovalca je uporaba namenskega integriranega vezja najpreprostejša rešitev, saj so bili problemi, ki jih opazimo pri komunikaciji s pametno kartico, ovrednoteni in rešeni že v fazi načrtovanja vezja. Naloga načrtovalca sistema je, da upošteva pogoje, v katerih določeni integrirani bralnik pravilno deluje, in z veliko verjetnostjo lahko pričakuje, da bo dokaj hitro in preprosto prišel do delujočega sistema.

V frekvenčnem območju okoli 13,56MHz se na tržišču pojavljajo prvi integrirani bralniki. Izzivi, s katerimi se srečujemo pri komunikaciji z brezkontaktno pametno kartico, so najpomembnejši del disertacije. V delu analiziramo razmere, v katerih poteka prenos podatkov in ponujamo rešitve nekaterih problemov, ki se pri tem pojavijo. Večji del disertacije se nanaša na komunikacijo v omenjenem frekvenčnem območju, izsledki pa so splošnejši in uporabni v vseh območjih, ki so dovoljeni za uporabo v namene komunikacije s pametnimi karticami.

Po uvodnem poglavju najprej kratko predstavimo način delovanja sistema brezkontaktne komunikacije in identifikacije. Predstavimo možnost izvedb bralnika in kartice. V nadaljevanju zberemo tiste podatke o sistemih, ki jih različni proizvajalci uporabljajo v tem frekvenčnem območju. ISO standarda, ki urejata to področje, predpisujeta uporabo podnosilnega signala za prenos podatkov s pametne kartice proti bralniku na frekvencah 424kHz za kartice z večjim dosegom in manjšo hitrostjo prenosa podatkov ter 848kHz za kartice z manjšim dosegom in večjo hitrostjo prenosa podatkov. Poleg teh nekateri proizvajalci uporabljajo tudi frekvenco podnosilnega signala 212kHz, nekateri pa direktno modulacijo brez podnosilnega signala. Za prenos podatkov z bralnika proti pametni kartici standarda predpisujeta uporabo OOK (ang. *on-off keying*) modulacije ali 10% ASK (ang. *amplitude shift keying*) modulacije. Nekateri proizvajalci uporabljajo ASK modulacijo z nekoliko višjim indeksom modulacije - do približno 30%. Kodiranje je v različnih sistemih lahko zelo različno. Za zelo univerzalen bralnik, ki lahko deluje v kar največ sistemih, prepustimo dekodiranje zunanjemu mikrokontrolniku. Žal so nekateri postopki kodiranja, ki so sicer del ISO standardov, patentno zaščiteni, kar je dodatna ovira za vgradnjo v vezje.

Ugotovimo, da bi splošni bralnik za frekvenčno območje okoli frekvence 13,56MHz potreboval sprejemnik, ki sprejema modulacijo na vseh treh frekvencah podnosilnega signala, po možnosti pa tudi modulacijo brez podnosilnega signala. Imel naj bi možnost ASK modulacije bralnikovega polja v območju med 10% in 30% in tudi možnost 100% ASK modulacije. Splošni bralnik naj bi imel dekodiranje podatkovnih paketov prepuščeno zunanjemu mikrokontrolniku.

V poglavju o matematičnem modelu antenskih krogov prikažemo odvisnost impedance pametne kartice od elementov kartice. Analizo razširimo na preslikavo impedance kartice na bralnikovo stran in opazujemo fazo in absolutno vrednost spremembe impedance bralnikove antene v odvisnosti do sprememb lastnosti kartice. Spreminjanje teh lastnosti uporabljamo za prenos podatkov s pametne kartice proti bralniku. Na kartici lahko spreminjamo omski del ali pa reaktivni del impedance. Tako dobljeno modulacijo tudi imenujemo omska ali realna in reaktivna (kapacitivna ali induktivna) ali imaginarna. Pogosto se zgodi, da kartica odd-

aja modulacijo, ki je deloma omska in deloma reaktivna. Omska modulacija kartice se v primeru, ko sta bralnikova antena in antena pametne kartice uglašeni na vzbujevalno frekvenco, preslika v amplitudno modulacijo na sponkah bralnikove antene. Reaktivna modulacija kartice se takrat preslika v fazno modulacijo. V poglavju o matematične modelu antenskih krogov ugotovimo, da se pri drugačni uglasitvi anten omska modulacija pametne kartice na priključkih bralnikove antene lahko pojavi kot mešana ali kot samo fazna modulacija. Podobno se spremeni tudi reaktivna modulacija na pametni kartici. V delu prikažemo odvisnost preslikave modulacije v primeru drugačne uglasitve ene ali obeh anten in pri različnih oddaljenostih med njima. Opazimo, da v splošnem lahko pričakujemo eno ali drugo, najpogosteje pa obe vrsti modulacije. V nadaljevanju je prikazan vpliv vezij za preslikavo impedance. Opazimo, da prilagoditveno vezje spreminja vrsto modulacije tudi, kadar je uglašeno in vzbujevalno frekvenco.

Eno od rešitev problema sprejema fazne modulacije najdemo v razdelku o možnosti uporabe večkratne modulacije polja s strani pametne kartice v različnih fazah. Če bi pametna kartica oddala podatke dvakrat - enkrat kot omsko modulacijo, drugič pa kot reaktivno modulacijo - bi se tudi na sponkah bralnikove antene vsaj ena od oddaj preslikala v amplitudno modulacijo. Sistem je primeren za prenos majhne količine podatkov.

V poglavju o napajanju pametne kartice si ogledamo možnosti za napajanje kartic. Pridobivanje energije iz elektromagnetnega polja bralnikove antene si podrobneje ogledamo. Iz hitrosti upadanja komponent polja antene lahko ugotovimo največji doseg napajanja v danih pogojih.

Sledi obsežno poglavje o sprejemnikih v sistemih brezkontaktne komunikacije in identifikacije. Najprej ugotovimo, kakšne so zahteve glede vrste modulacije, ki jo sprejemnik sprejema, kakšno dinamično območje pričakujemo in kako nanj vpliva prisotnost močnega nosilnega signala na vhodu v sprejemnik. Prikažemo tudi merilno metodo, primerno za merjenje občutljivosti sprejemnika, ki je namenjen sprejemu signalov s pametne kartice.

V poglavju o zasnovah sprejemnika si ogledamo način delovanja sprejemnika z mešanjem v visoko medfrekvenco, sprejemnika z mešanjem v zelo nizko medfrekvenco brez in z uporabo metode za slabljenje zrcalne frekvence. Prikazana sta tudi sprejemnika z mešanjem v medfrekvenco nič in sprejemnik s sledilnikom ovojnice. V nadaljevanju več pozornosti namenimo zasnovi vhoda v sprejemnik. .Nosilni signali v vhodu v sprejemnik je mnogo večji, kot so modulacijske bočne komponente. Da vhodna stopnja v sprejemnik ni prekrmiljena (vhodni sledilnik ali vhodni mešalnik), moramo celotni vhodni signal zmanjšati, s tem pa se velikost modulacijskega signala pri veliki razdalji med antenama približuje šumnemu nivoju sistema. Posledično dobimo manjšo občutljivost sprejemnika. Da bi zmanjšali le velik nosilni signal, modulacijskih signalov v bočnih pasovih pa ne, lahko uporabimo dve metodi. Prva metoda je vezava smernega sklopnika ali smernega mostička med anteno, oddajnikom in sprejemnikom. Smerni sklopnik za velikost smernosti izboljša razmerje med velikostjo bočnih pasov in z velikostjo nosilnega signala na vhodu v sprejemnik. Ob tem pa žal tudi koristni vhodni signal zmanjša velikost sklopa sklopnika. Druga možnost je uporaba zapornega sita za nosilni signal na vhodu v sprejemnik. Učinkovito sito je le sito visoke kvalitete, kajti sredina bočnih pasov je le od 1,6% do 6,3% oddaljena od nosilne frekvence. Obe metodi sta učinkoviti, vendar zaradi velikosti komponent in cene nista primerni za uporabo v integriranem bralniku.

Sistem za samodejno nastavitev ojačenja sprejemnika, ki je prilagojen paketnemu prenosu podatkov, omogoča delovanje sistema v področju močnejših motečih elektromagnetnih polj. Samodejna nastavitev ojačenja ne slabša razmerja med koristnim signalom in motnjo na sprejemni poti, kot se to lahko zgodi, če uporabljamo omejevalnik signala na sprejemni poti. Za predlagani sistem je značilno, da ima tri stanja: hitri napad, mirovanje in hitri razpad. Ko na vhod v sprejemni pride velik signal, sistem hitro zmanjša ojačenje. Dokler je signal približno enako visok, sistem ohrani ojačenje nespremenjeno kljub kratkim prekinitvam zaradi OOK kodiranja. Ko pa signal pade pod nivo ohranjanja mirovanja za čas, ki je daljši, kot je najdaljša možna prekinitev v kodiranju, pa sistem privzame, da je prenosa enega paketa konec in hitro poveča ojačenje. V tem stanju pričakuje nov paket, ki ima lahko bistveno drugačno amplitudo kot prejšnji. Za ta sistem smo tudi predlagali patentno zaščito.

V naslednjem poglavju si ogledamo preslikavo amplitudne modulacije v fazno na prenosnem vodu med vezjem bralnika in njegovo anteno. Pojav lahko izkoristimo za sprejem amplitudne in fazne modulacije. Signal opazujemo na enem in drugem koncu prenosnega voda z dolžino ene osmine valovne dolžine. Na tej razdalji se vrsta modulacije ravno zamenja in vedno dobimo vsaj na enem koncu tega voda amplitudno moduliran antenski signal. Povsem enak pojav opazimo tudi na filtru, ki vrti fazo za 45°. Uporaba filtra je boljša, ker filter lahko naredi impedančno prilagoditev in doda del slabljenja višjih harmonskih komponent, pa tudi manjši je. metodo in način uporabe smo patentno zaščitili.

Večino opisanih in vse predlagane rešitve smo tudi praktično preskusili. Načrtali smo troje integriranih vezij. Vezja smo uspešno preskusili in v tem delu podajamo nekaj zanimivejših merilnih rezultatov. Eno vezje je testno integrirano vezje, namenjeno v raziskovalne namene, ostali dve, ki temeljita na spoznanjih iz prvega, pa sta samostojna bralnika za dvoje različnih področij uporabe.

Prvo od njiju je splošni bralnik z integriranim oddajnikom s 100% ASK modulacijo ali z nastavljivim indeksom modulacije v območju med 7% in 30%. Ima sprejemnik z dvojnim vhodom za uporabo v sistemu, pri katerem sprejemamo amplitudno in fazno modulirane signale s pametne kartice s pomočjo linije ali faznega sukalnika. Izhod iz vezja je lahko digitalizirani podnosilni signal ali ojačeni in očiščeni analogni signal. Vezje omogoča tudi BPSK dekodiranje po-

datkovnih paketov v skladu z ISO14443, Type B [3]. Seveda ima vezje vse pomožne sklope, kot so izvor referenčne napetosti, tokovne vire, oscilator s kremenčevim kristalom in ukazni del, ki skrbi za skladno delovanje vseh sklopov. Drugo vezje pa je namenski bralnik, namenjen delovanju z eno vrsto pametne kartice. Kartica ima obliko valjčka in je vedno enako oddaljena od bralnika. Deluje v napetostnem območju med 1,8V in 3,2V in s precej ohlapnimi tolerancami uglasitve antenskih krogov. Ima nizkoomsko izhodno stopnjo oddajnika in dve vrsti sprejemnika. Za sprejem amplitudne modulacije smo uporabili sprejemnik z zunanjim elementom za sledilnik ovojnice, za sprejem fazne modulacije pa sprejemnik z mešalnikom na vhodu. Vezje pretvori sprejeti podnosilni signal v posamezne bite po Millerjevem postopku in doda taktni signal, ki predstavlja veljavnost bitov.

Oba bralnika delujeta v skladu s pričakovanji in dokazujeta veljavo in uporabnost izsledkov tega dela.

PREDSTAVITEV PODJETJA

RLS

RLS merilna tehnika d.o.o. je bila ustanovljena decembra 1989 v Ljubljani. RLS pomeni "rotacijski in linearni senzorji pomika in zasuka".

Že od vsega začetka smo osredotočeni na zagotavljanje rešitev za široko področje merilne tehnike ter nadzora pomika in zasuka. Med našimi izdelki so med drugim fotodiodni moduli, izdelani v tehnologiji COB, in interpolatorska vezja ASIC za proizvajalce dajalnikov, ter magnetni rotacijki dajalniki, PC vmesniki in merilni sistemi po naročilu.

Z dajalniki pomika in zasuka ter komponentami zanje oskrbujemo industrijske uporabnike po vsem svetu. Z zagotavljanjem celovitih rešitev za merilne sisteme po naročilu pa smo osredotočeni na slovenski trg in okolico.

Zaradi prilagodljivosti in odličnega inženiringa lahko proizvajamo zahtevne komponenete po posebnih specifikacijah strank. Na področju raziskav mikrosistemov zelo dobro sodelujemo s Fakulteto za elektrotehniko Univerze v Ljubljani. Ponosni smo na svetovne inovacije, kakršen je naš magnetni rotacijski dajalnik na enem čipu.

PRODAJNI PROGRAM

Dajalniki pomika in zasuka

Rotacijski in Linearni

Magnetni in Optični

Komponente za dajalnike pomika in zasuka

Fotodiodni moduli, Magnetni rotacijski dajalniki, Analogni interpolatorji

Merilna tehnika in merilni sistemi po naročilu

Kazalniki pozicije, PC vmesniki, MerOpt (brezkontaktna dimenzijska kontrola), GausSPC (statistični nadzor procesov), Merilni sistemi po meri

Renishaw izdelki

Smo distributerji podjetja Renishaw

GLAVNA PARTNERSTVA

Smo majhno in prilagodljivo podjetje. Dostop do kupcev in virov širimo s partnerstvi z drugimi uspešnimi podjetji.

Renishaw

Smo distributerji za podjetje Renishaw, Renishaw pa preko svoje mreže distribuira tudi naše izdelke. Od leta 2001 ima Renishaw tudi 50% lastniški delež v RLS.

Renishaw (Velika Britanija, globalno), TWK (Nemčija), SKB IS (Rusija, Skupnost neodvisnih držav), ELAP (Italija)

To so naši glavni distributerji za dajalnike pomika in zasuka.

Fakulteta za elektrotehniko Univerze v Ljubljani

S Fakulteto zelo dobro sodelujemo na področju raziskav mikrosistemov.

Nova družina izdelkov slovenskega visokotehnološkega podjetja - plod izvrstnega sodelovanja med podjetji in akademskim okoljem

Nova družina miniaturnih brezkontaktnih dajalnikov zasuka

Inovativno podjetje RLS merilna tehnika d.o.o. iz Ljubljane, član tehnološkega parka Ljubljana, je predstavilo novo družino inovativnih izdelkov z visoko dodano vrednostjo, s katerimi bo v sodelovanju s svojimi partnerji oskrbovala industrijske uporabnike po vsem svetu.

Izdelki so plod dolgoletnega sodelovanja z Laboratorijem za mikroelektroniko Fakultete za elektrotehniko Univerze v Ljubljani, podjetjem IDS integrirani in diskretni sistemi d.o.o. iz Ljubljane in britanskim podjetjem Renishaw plc, solastnikom podjetja RLS. Projekt je s sofinanciranjem podprlo tudi Ministrstvo za gospodarstvo Republike Slovenije v okviru programa »Sofinanciranje predkonkurenčno razvojno-raziskovalnih aktivnosti projektov tehnološkega razvoja v letu 2002«.

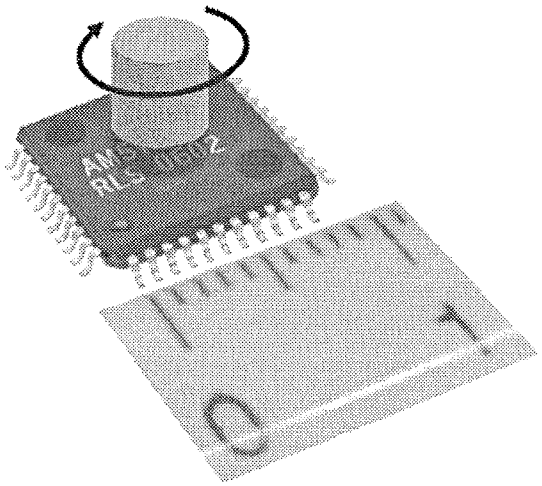
Zaradi naraščajočih potreb po zanesljivem, natančnem ter stroškovno ugodnem merjenju zasukov v zahtevnih pogojih delovanja, je podjetje RLS razvilo vrsto brezkontaktnih miniaturnih magnetnih dajalnikov zasuka z ločljivostjo do 4096 pozicij (12 bitov).

Pri novo razviti brezkontaktni zasnovi modelov RM, sta nosilec magneta in integrirano senzorsko vezje, ki je vgrajeno v čitalni glavi, med seboj ločena, kar omogoča zanesljivo in dolgotrajno obratovanje. Natančnost merjenja zasuka dosega 0,3 kotne stopinje v širokem temperaturnem območju, tudi v zahtevnih okoljih (do IP68) in pri visokih vrtljajih.

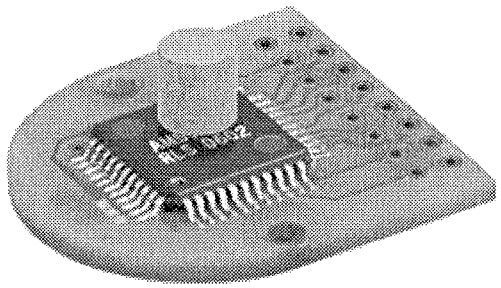
Ideja za nov izdelek je nastala že leta 1996, ko je prof. dr. Janez Trontelj iz Fakultete za elektrotehniko Janezu Novaku, ustanovitelju in direktorju podjetja RLS, predstavil osnovni princip delovanja integriranega Hall senzorja zasuka, ki je jedro vseh izdelkov v novi paleti. Podjetje RLS je potem skupaj s podjetjem IDS razvilo visoko integrirano vezje ASIC, ki v enem samem vezju združuje množico Hall

senzorjev in vso elektroniko za obdelavo signalov. Projekt je sofinanciralo tudi Ministrstvo za gospodarstvo v okviru programa sofinanciranja predkonkurenčno razvojno-raziskovalnih aktivnosti projektov tehnološkega razvoja v letu 2002.

Novi magnetni dajalniki zasuka so enostavni za vgradnjo. Na voljo so v kovinskem ohišju, v modularni izvedbi ali kot komponenta.



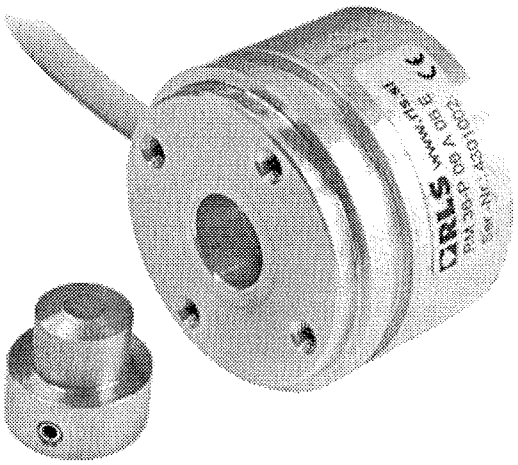
Slika 1 Integrirano vezje AM512 in magnet
Visoka integracija vezja z vgrajenimi Hallovimi senzorji omogoča kompaktne rešitve merjenja zasuka diametralno polariziranega magneta.



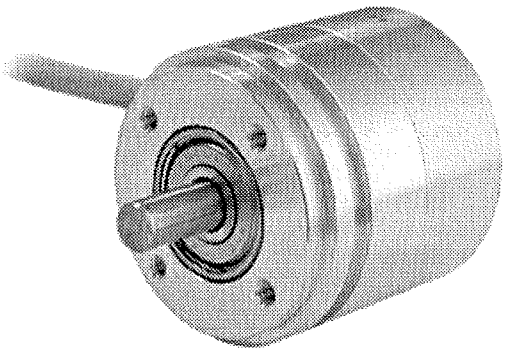
Slika 2 Primer modularne izvedbe
Integrirano vezje AM512 na tiskani ploščici, primerni za vgradnjo.

Absolutni dajalniki nudijo do 12-bitno ločljivost (4096 pozicij) s paralelnim ali serijskim podatkovnim izhodom, na voljo pa so tudi inkrementalni (1024 pulzov na obrat), analogni, linearni napetostni ter linearni tokovni izhod. Izvedbo z linearnim napetostnim ali tokovnim izhodom lahko uporabljamo pri aplikacijah, kjer nadomešča tradicionalne uporovne potenciometre (npr. pri komandnih ploščah).

Zaradi tako prilagodljive zasnove so novi dajalniki uporabni za širok spekter aplikacij. Uporaba vključuje od področja avtomatizacije, na primer vgradnjo v motorje za namen pozicioniranja, vgradnjo v pomorske instrumente, nadzor



Slika 3 Dajalnik zasuka RM v brezkontaktni izvedbi
Brezkontaktna breztorna zasnova, ki ne vsebuje ležajev, nudi visoko zanesljivost. Pri montaži ni potrebna sklopka med osjo dajalnika in merjencem.



Slika 4 Dajalnik zasuka RE »klasične« zasnove
Magnetni dajalniki v primerjavi z optičnimi ne vsebujejo stekla kot nosilca informacije, kar omogoča visoko odpornost na udarce, vibracije in umazanijo.

položaja ventilov, črpanje goriva, merjenje nivoja, videonadzorne kamere, samopostrežne avtomate, do delovnih vozil in medicinske opreme.

Glavni distributerji nove palete izdelkov bodo poleg RLS še britansko podjetje Renishaw, nemško podjetje TWK, rusko podjetje SK BIS, italijansko podjetje ELAP, ter ameriški podjetji Encoder Devices in Gurley Precision Instruments. Izdelki bodo na različnih trgih na voljo pod blagovnimi znamkami RLS, Renishaw ali TWK.

Nadaljnje informacije v zvezi z novimi magnetnimi dajalniki zasuka so na voljo na spletnih straneh www.rls.si in www.renishaw.com.

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POROČILA
REPORTS

Simpozij o pripravi elektronske keramike *Processing of Electroceramics*, 31. 8. – 3. 9. 2003, Bled, Slovenija

Od enaintridesetega avgusta do tretjega septembra 2003 je na Bledu potekal simpozij o pripravi elektronske keramike *Processing of Electroceramics* pod pokroviteljstvom tematske mreže Evropske skupnosti POLECER – Polar Electroceramics. Simpozij je organiziral Odsek za elektronsko keramiko Instituta Jožef Stefan s predsednico organizacijskega odbora Marijo Kosec ter sopredsednicami Danjelo Kuščer Hrovatin, Barbaro Malič in Wando W. Wolny (Ferroperm, Danska).

Na simpoziju je sodelovalo 92 udeležencev iz 26 držav-poleg večine evropskih držav tudi iz Japonske in ZDA. K udeležbi na simpoziju smo pritegnili tudi raziskovalce in razvijalce s področij fizike materialov, elektronike in načrtovanja elektronskih elementov, z namenom, da se podrobneje seznanijo s pripravo elektronske keramike.

Simpozij se je po nagovorih predsednika Znanstvenega sveta Instituta Jožef Stefan, prof. Roberta Blinca, predsednice simpozija prof. Marije Kosec ter koordinatorke mreže POLECER gospe Wande Wolny začel s sklopom učnih predavanj o merjenju velikosti delcev od nano- do milimetrske velikosti ter o karakterizaciji keramičnih suspenzij (P. Bowen, Švica), o oblikovanju in žganju elektronske keramike (J.-M. Haussonne) ter o pripravi elektronske keramike iz raztopin (B. Malič, Slovenija). Dve nadaljnji predavanji sta bili namenjeni pomembnima metodama karakterizacije keramičnih materialov – praškovni difrakciji (A. Meden, Slovenija) in mikrostrukturni analizi ter pregledu mikroskopskih metod (G. Dražić, Slovenija).

V sklopu preglednih predavanj je osemnajst raziskovalcev predstavilo tako stanje raziskav kot tudi svoje dosežke na izbranih področjih. P. Bowen, Švica, je predaval o koloidnem procesiranju in problemih, povezanih z delci nanometrske velikosti. V vrsti predavanj s področja sinteze iz raztopin je S.-I. Hirano predstavil raziskave hibridnih nanodelcev oksid/polimer, J.A. Varela sintezo keramičnih materialov iz polimernih prekurzorjev, M. Yoshimura sintezo keramičnih materialov iz raztopin brez dodatne toplotne obdelave, K. Kato in M. L. Calzada pa sta predavali o pripravi keramičnih tankih plasti iz raztopin.

V sklopu predavanj, namenjenih 'klasični' pripravi elektronske keramike je J.-M. Haussonne opisal problematiko mešanja in mletja keramičnih prahov, M. Senna je predstavil mehanokemijsko sintezo elektronske keramike, C. Pithan je predaval o konsolidaciji keramike s pomočjo pritiska, M. Kosec pa o problematiki priprave elektronske keramike na osnovi svinčevih spojin. Oblikovanje keramičnih materialov so predstavili A. Safari s predavanjem o oblikovanju keramičnih struktur z računalniško podporo (SFF- Solid Freeform Fabrication), T. Button je govoril o oblikovanju piezokeramičnih elementov brez izrazitega krčenja med toplotno obdelavo, D. Sporn je opisal pripravo piezokeramičnih vlaken, C. Galassi pripravo porozne keramike, D. A. Payne pa pripravo usmerjene keramike. M. Alexe je opisal procesiranje feroelektrikov na nanometrski ravni, L. Golonka pa uporabo LTCC (Low Temperature Cofired Ceramic) tehnologije v mikroelektroniki. Simpozij je zaključil P. Gonnard s predavanjem o okoljski problematiki elektronske keramike. Predavanja so objavljena v zborniku Processing of Electroceramics: Conference Notes.

V poster sekciji je bilo 64 prispevkov s področij sinteze elektronske keramike v trdnem stanju in sinteze iz raztopin, mehanokemijske sinteze, tankih plasti (debelin do nekaj 100 nm), debelih plasti (do približno 100 mm) in večplastnih struktur, nano-tehnologij in elektronskih elementov.

Barbara Malič, Odsek za elektronsko keramiko,
Institut Jožef Stefan
(povzeto po prispevku v internem glasilu
Instituta Jožef Stefan 'Novice', sept. 2003)

Semicon Europa - Monakovo, 20.-22. april 2004

Semicon Europa je sklop več dogodkov, ki se odvijajo v tednu dni (19.-24. aprila) pod pokroviteljstvom SEMI (Semiconductor Equipment and Materials International) organizacije. Najbolj odmevna je seveda razstava, ki je bila letos v dneh od 20.-22. aprila. Tri glavne veje mikroelektronske industrije, ki jih SEMI spremlja že od leta 1970 so materiali, postopki proizvodnje (wafer fabrication) in testiranje skupaj z montažo (assembly) vezij in elementov. Ena od najpomembnejših vlog SEMI organizacije pa je razvoj tehničnih standardov za mikroelektronsko industrijo opreme. Z rastočo ceno razvoja nove opreme in materialov za naslednjo generacijo polprevodniških procesov predstavlja postavljanje globalnih standardov ključno vlogo pri povečevanju izkoristka proizvodnje in dviga kvalitete produktov.

Vsakoletna razstava Semicon Europa je bila tudi tokrat na sejemskem prostoru (The New Munich Trade Centre) v Munchnu na Bavarskem. Poleg razstave Semicon West, ki se ponavadi odvija na zahodni obali ZDA in razstave Semicon East, ki pokriva azijski del in se odvija na daljnjem

vzhodu, je Semicon Europa največja razstava proizvajalcev opreme, materialov in tehnologij, povezanih z mikroelektronsko industrijo. Po obsegu je glede na kapacitete sejemskega prostora zasedla le majhen del razstavnih prostorov, vendar ni bila zato nič manj pestra kot ostala leta. Poleg informacij o novitetah, ki so danes dostopne na spletnih straneh, je obisk sejma koristen iz več zornih kotov. Sejem sam po sebi ni namenjen izključno prodajnim menedžerjem in potencialnim kupcem, temveč v veliki meri razvojnim in raziskovalnim ekspertom ter procesnim inženirjem, ki iščejo specifične rešitve in zmožnosti opreme, ki se ponuja na trgu. Nenazadnje je pomemben za vzdrževanje medsebojnih osebnih stikov in novih poznanstev, ki so pogosto odločilnega pomena, navkljub vsej informacijski tehnologiji, ko pride do strateških odločitev o nakupih opreme ali reševanju povsem tehničnih detajlov.

Manj znano je, da se že pred, med in po razstavi Semicon odvijajo pomembni in pestri poslovni forumi, tehnični simpoziji in sestanki komisij za SEMI standarde.

Posebna srečanja in seminarji so bila letos namenjena tudi aktualnim vprašanjem kot so npr. možnosti poslovanja s Kitajsko, ki danes predstavlja ogromen potencial za nova vlaganja, avtomatizacija in logistiki proizvodnje ter vidikom intelektualne lastnine. Potekalo je tudi 25 srečanj ekspertov iz vodilnih podjetij in posameznih komisij za usklajevanje SEMI standardov, ki določajo prihodnje smernice razvoja.

Mednarodni MEMS forum se je letos osredotočil na proizvodne tehnologije in procesno opremo, tehnologije zapiranja MEMS v ohišja ter na izboljšane in nove materiale. MEMS tehnologije predstavljajo danes hitro razvijajočo vejo mikroelektronske industrije za potrebe avtomobilskega trga kot tudi čedalje večjega trga telekomunikacij in potrošne elektronike. Poudarek letos je bil predvsem na komercializaciji MEMS izdelkov.

SEMI tehnološki simpozij je bil sestavljen iz niza tehničnih prispevkov, ki so predstavili najpomembnejše tehnične novosti tako na strani proizvajalcev opreme kot tudi uporabnikov iz industrije. Po nekaj letih recesije mikroelektronske industrije in posredno industrije opreme se je trend končno obrnil navzgor. Poudarek je bil na temah kot so tehnologije 3D metalnih Cu povezav in dielektrikov z nizko relativno dielektrično konstanto (low-K) za 65 in 45 nm tehnologije z vidika samih procesov in materialov. Realizacija novih materialov in plasti za napredne CMOS strukture kot so SiGe/SOI/Si z raztegnjena kristalno strukturo je bil tudi eden od segmentov omenjenega foruma, kot tudi fotopostopki, optika in maske za osvetljevanje pri 193nm oziroma 65nm valovnih dolžinah.

Standardizacija 300mm silicijevih rezin je še vedno dopolnjujoč proces, kjer so bila trenutno v ospredju vprašanja povezana z napakami na robu rezine in vpliv ter spremljanje defektov zadnje strani rezine, vprašanja kaj in kako s ponovno uporabo procesiranih rezin (reclaimed wafers) in kontaminacijo pri ponovnem procesiranju.

Del simpozija je bil namenjen prispevkom o kontroli kontaminacije rezin v začetnih fazah procesiranja po čiščenju in oksidaciji ter vpliv na končni izplen. Poseben forum je bil namenjen tudi skrbi in vplivu na okolje, zdravje in varnost, čemur morajo biti zavezani vsi proizvajalci opreme in materialov.

Poleg naštetih forumov so potekali tudi izobraževalni tečaji o novih SEMI in IEC standardih ter o osnovnih ULSI procesnih tehnologijah.

Na letošnjem sejmu je sodelovalo preko 800 razstavljalcev opreme, materialov, konzultantov, kot tudi vseh, kakorkoli posredno povezanih z industrijo mikroelektronike. Poleg močnih podjetij se je predstavilo tudi veliko število manjših, združenih podjetij na skupnih stojnicah ali pa so se predstavili zastopniki, ki so predstavljali nabor ponudb več podjetij. Zanimiv pristop je bila tudi skupna predstavitev celih regij s svojo industrijo mikroelektronske opreme in tehnoloških zmogljivosti, kot npr. Koroška, Škotska in zvezna država New York.

Spekter razstavljalcev je bil izredno širok, kar je razvidno iz kataloga, zatorej omenjam le nekaj pomembnejših. Največ je bilo ponudbe avtomatiziranih modulov pri manipulaciji in proizvodnji 300mm silicijevih rezin od začetnega čiščenja do posameznih faz procesiranja predvsem z eno samo rezino.

Veliko je bilo tudi ponudnikov za t.i. "background facilities" kot na primer popolne rešitve za pridobivanje DI vode s popolno kontrolo procesa in tudi rešitve glede odpadnih voda. Podobno je bilo tudi precej proizvajalcev sistemov za ultrafiltracijo in precizno kontrolo pretokov procesnih plinov. Veliko nove opreme je bilo predstavljeno za montažo in zapiranje integriranih vezij in mikrosistemov ter razne dodatne optične analitske kontrole.

Predstavljeni so bili različni proizvajalci merilne in analitske opreme za spremljanje posameznih faz procesa, kot tudi pogojev v čistih prostorih. Za kontrolo kompleksnih tehnoloških procesov in sledljivosti postaja tak pristop vedno bolj nujen.

Predstavljena je bila tudi oprema za globinsko suho (DRIE) in mokro mikroobdelavo silicija. Ponujene so bile celovite rešitve za globinsko mokro jedkanje silicijevih rezin s posebnimi držali in pretočnimi termostatiranimi jedkali ter mikroprocesorsko kontrolo procesa.

Kot vsako leto je bilo tudi precej ponudnikov obnovljene rabljene opreme. Medtem ko so včasih prednjačila v ponudbi ameriška podjetja, je sedaj zelo veliko že tudi evropskih podjetij, saj je trg rabljene opreme precej bolje založen in so povpraševanja po obnovljeni rabljeni opremi večja. Tak pristop močno znižuje začetno investicijo v določenih primerih zagona novih postrojenj.

Marsikaj pove o razstavi izjava enega od udeležencev: " Informacijski boom je sejem precej spremenil, saj so sedaj vse informacije o produktih dostopne dan in noč na spletu.

Konec koncev sejma zaradi predstavitve novosti niti ne bi rabili, saj so stroški transporta in postavitve demo opreme na sejmu izredno visoki. Sam imam vpeljane produkte in prodajno mrežo že leta in na sejmu nimam kaj novega ponuditi. A kljub vsemu si ne morem privoščiti, da ne bi bil prisoten."

Naslednje leto bo prireditev na istem mestu od 12-14 aprila, opozarjam pa tudi na možnost brezplačne registracije za obisk razstave na spletni strani *www.semi.org/semiconeuropa* (vsaj mesec dni prej).

SEMI koledar prireditev si lahko ogledate na spletni strani *www.semi.org.*

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NOVICE
NEWS

Konec leta 2003 je Društvo za vakuumsko tehniko Slovenije izdalo knjigo **Vakuumska znanost in tehnika**, ki jo je pripravljalo nekaj let. Širokega znanja, ki ga je potrebno imeti za obvladovanje postopkov za doseganje in meritev nizkih tlakov ter vakuumskih tehnologij ne daje nobena od sedanjih študijskih usmeritev v Sloveniji. To vrzel že vrsto let zapolnjuje DVTS z organiziranjem tečajem, katerih dopolnilo je tudi primeren učbenik.

Prvi slovenski učbenik **Osnove vakuumske tehnike** iz leta 1981 je pošel v nekaj letih, zato je bil leta 1984 izdan delno razširjen in dopolnjen ponatis. Od takrat se je na področju vakuumske znanosti in tehnike spremenilo marsikaj. Vakuumska tehnika je ostala pomembna veja na mnogih področjih življenja, osvojila in spremenila je mnogo tehnologij, česar neposredno najbrž niti ne opazimo. Predvsem pa je pridobila na pomenu na področju temeljnih in aplikativnih raziskav, ki so bile nekoč izključno domena fizike, danes pa se metode uporabljajo v mikroelektroniki, biologiji, farmaciji, genetiki, metalurgiji itd. Največji napredek v zadnjem desetletju je bil dosežen na področju, kjer preučujemo, gradimo, urejamo in opazujemo lastnosti snovi na atomskem nivoju, kar imenujem nanotehnologija. Mnogo spoznanj v navedenih vedah je bilo dobljenih z metodami, ki delujejo v ultravisokem vakuumu.

Z izdajo knjige na 150 straneh, tiskani na kvalitetnem papirju formata A4, s 150 slikami in 10 tabelami v dovršeni grafični obliki, se Slovenci uvrščamo v skupino razvitih držav, ki imajo svoj učbenik vakuumske znanosti in tehnike. Knjiga je razdeljena na 14 poglavij, ki so delo 9 avtorjev.

Cena knjige je 6000 SIT. Knjigo lahko naročite na elektronski naslov: alenka.vesel@ijs.si ali pa jo kupite na Odseku za tehnologijo površin in optoelektroniko - F4, Instituta "Jožef Stefan", pri dr. Alenki Vesel (tel. 01- 4264592), v 1. nadstropju stavbe na Teslovi 30, Ljubljana, v kateri ima prostore tudi Tehnološki park Ljubljana.

Urednik knjige
Dr. Vincenc Nemanič

AMD builds 300mm fab in Germany

AMD has broken ground on a 300mm manufacturing facility in Germany. AMD Fab 36 will be part of AMD Dresden Fab 36 LLC &Co. KG and will be located in Dresden next to AMD's Fab 30, a 200mm production site. The 300mm facility is expected to be in volume production in 2006, employing 1000 people, mostly skilled engineers and technicians.

External financing is expected to include up to $700mn in loans from a consortium of banks with an 80% residual guarantee from the German and Saxony governments. Grants and allowances of $500mn are expected from the local and federal governments (pending European Commission approval). Equity funding of $320mn is due from Saxony and a group of European investors led by M + W Zander. AMD and other potential partners will provide the balance.

"AMD's investment in Dresden is one of the largest in East Germany since unification in 1990," says minister president of the Free State of Saxony, Professor Georg Milbradt.

"By building in Dresden, we are able to leverage the outstanding capabilities of our existing AMD Fab 30 and gain access to the most substantial government-backed financial incentives package available to us," comments Bob Rivet, chief financial officer at AMD. "We expect AMD Fab 36 will cost approximately $2.4bn over the next four years. We have arranged external financing and government support of approximately $1.5bn during that period."

IMEC pushes high-k/metal gate performance

IMEC says that it has successfully demonstrated the use of high k dielectrics and metal gates to values below Inm. The European research centre believes that this level of electrical performance removes one of the industry's Ved brick walls' to advancing semiconductor technology. The research team used metal gates to overcome the problems imposed by the interaction between high k materials with the commonly used polysilicon electrode.

Using TiN or Tal\I gates and Hf02 as dielectric, aggressive scaling down to a 0.5 nm equivalent-oxide thickness (EOT) was demonstrated in both nMOS (8.2A EOT) andpMOS (7.5A EOT) transistors.

The metal-gated devices outperformed their polysilicon-based counterparts in terms of electrical performance pa-

rameters, including high conductance, low leakage and reduced threshold-voltage instabilities.

The Hf02 was deposited by atomic layer chemical vapour deposition (ALCVD).

Part of this research was done in collaboration with IMEC's high k industrial affiliation programme partners International Sematech, Renesas, Matsushita and Samsung.

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Tel.+33 476 57 4617; Fax.+33 476 47 3814
Email : cmp@imag.fr; http://cmp.imag.fr

CMP INTRODUCING 0.35 M CMOS-OPTO PROCESS

Grenoble, December 2003 - CMP today announced the introduction of the CMOS-Opto 0.35um process from austriamicrosystems AG.

The optical process C35B4O1 provides enhanced optical sensitivity for embedded photodiodes. It enables the design of high density photo sensors, APS, and CMOS cameras.

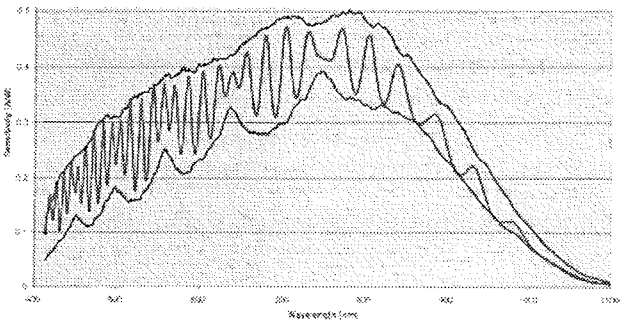
The process is fully compatible with the already supported 0.35 µm CMOS, thus enabling IP reuse with the existing CMOS standard-cell libraries. The Peripheral cell libraries are available for 3.3 V and 5 V with high driving capabilities and excellent ESD performance.

Process features:

- 0.35um CMOS polycide-gate process
- 4 layers metal, 2 layers poly, and MIM
- Peripheral Cells with high driving capabilities
- High performance digital and mixed signal capabilities
- N/PMOS saturation current: 520/240

Opto features:

Q Dark current < 45 pA/cm^2© 27° C
Q Cut-off frequency > 20 MHz
Q Responsitivity @ 550 nm: 290 mA/W
G Responsitivity © 850 nm: 330 mA/W
G Minimum pixel size 6 (jm x 6 pm)



The design kit is supported under Cadence CAD tools.

CMP offers 5 MPW runs for this process in 2004: 26 January, 19 April, 05 July, 27 September, 06 December.

Xerox reports three-basic materials needed for printable circuits

News:R&D

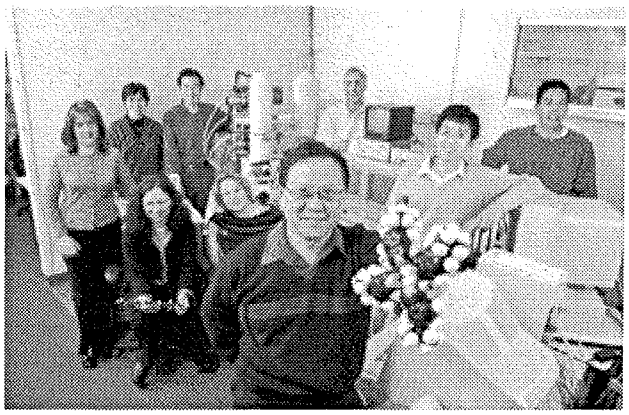
Xerox says that it has developed a high-performance semiconductive ink that can be used to print transistor channels at low temperatures and in open air - a requirement for low-cost manufacturing. The company hopes that flexible roll-up television screens and computer displays will be one step closer to reality as a result. Low-cost RFIDs are also in prospect.

Most semiconductor materials, including those that are polymer-based, require processing at high temperatures and under inert atmospheres. Beng Ong's team at the Xerox Research Centre of Canada (XRCC) has also developed materials for printing conductor and dielectric components.

Ong discussed the research findings in a presentation at the Materials Research Society spring conference.

Thus, all three elements necessary to make a plastic circuit - a semiconductor, a conductor and dielectric - may now be printed using inkjet techniques. The technology promises a low-cost alternative to silicon technology that could print flexible plastic transistors as easily as printing a newspaper.

"Having developed these three critical liquid-processable materials may make it possible to create low-cost, flexible plastic transistor circuits using common liquid-deposition



techniques such as spin coating, screen or stencil printing, offset or inkjet printing," says Ong. He believes that products based on these or similar materials will be available commercially in the near future.

Xerox's advances build on the unique polythiophene semiconductor previously designed by Ong's team at XRCC, as well as on a method developed by the Palo Alto Research Center (PARC) for creating a plastic semiconductor transistor array using inkjet printing. PARC is a wholly owned subsidiary of Xerox.

Being able to print in open air is significant because the electrical properties of most liquid-processable organic semiconductors degrade when exposed to atmospheric oxygen. This makes it difficult to build functional transistors in air. However, the Xerox polythiophene semiconductor not only possesses better air stability, it also exhibits excellent self-assembly behaviour. Its unique molecular characteristics allow it to be readily processed into structurally ordered semiconductor nanoparticles. These nanoparticles, when dispersed in a liquid, form an environmentally-stable nanoparticle ink. The ink provides consistent properties and enables inkjet printing of high-performance organic transistor channel layers under ambient conditions.

Xerox is working with Motorola and Dow Chemical to develop plastic integrated circuits for various electronic applications under a National Institute of Standards and Technology (NIST) Advanced Technology Program grant. In addition to XRCC's materials and PARC's inkjet printing of active-matrix addressed arrays for display backplane switching circuits, Motorola is fabricating plastic circuits for various applications using commercial printing technologies.

Last week, US company TDA Research announced development of a new conductive plastic - oligotron polymer possessing a conducting polyethylenedioxythiophene (PEDOT) centre and two non-conducting ends (Bulletin 526, April 14, 2004).

Caption: Beng Ong's research team at the Xerox Research Centre of Canada.

Infineon puts audio into snowboard jacket

SPORTSWEAR producer O'Neill Europe has joined with Infineon Technologies on a joint product development project for 'wearable electronics'. Infineon developed a chip module suitable for integration into a snowboard jacket based on O'Neill's specifications. This technology enables Bluetooth mobile phone and MP3 player use. The product, called "THE HUB", will be part of O'Neill's 2004/05 winter collection.

Woven into THE HUB are electrically conductive fabric tracks that connect the chip

module to a fabric keyboard and built-in speakers in the helmet. If the snowboarder wants to make a phone call, the stereo system acts as the headset. A microphone is integrated in the collar of the jacket. Since presenting its technology, Infineon has discussed projects with more than 200 companies from the textile industry. In co-operation with Vorwerk Teppichwerke carpet plant in Germany, Infineon is currently working on an initial prototype for a "smart carpet".

Informacije MIDEM
Strokovna revija za mikroelektroniko, elektronske sestavine dele in materiale

NAVODILA AVTORJEM

Informacije MIDEM je znanstveno-strokovno-društvena publikacija Strokovnega društva za mikroelektroniko, elektronske sestavne dele in materiale - MIDEM. Revija objavlja prispevke s področja mikroelektronike, elektronskih sestavnih delov in materialov. Ob oddaji člankov morajo avtorji predlagati uredništvu razvrstitev dela v skladu s tipologijo za vodenje bibliografij v okviru sistema COBISS.
Znanstveni in strokovni prispevki bodo recenzirani.

Znanstveno-strokovni prispevki morajo biti pripravljeni na naslednji način:

1. Naslov dela, imena in priimki avtorjev brez titul, imena institucij in firm
2. Ključne besede in povzetek (največ 250 besed).
3. Naslov dela v angleščini.
4. Ključne besede v angleščini (Key words) in podaljšani povzetek (Extended Abstract) v angleščini, če je članek napisan v slovenščini
5. Uvod, glavni del, zaključek, zahvale, dodatki in literatura v skladu z IMRAD shemo (Introduction, Methods, Results And Discsussion).
6. Polna imena in priimki avtorjev s titulami, naslovi institucij in firm, v katerih so zaposleni ter tel./Fax/Email podatki.
7. Prispevki naj bodo oblikovani enostransko na A4 straneh v enem stolpcu z dvojnim razmikom, velikost črk namanj 12pt. Priporočena dolžina članka je 12-15 strani brez slik.

Ostali prispevki, kot so poljudni cčlanki, aplikacijski članki, novice iz stroke, vesti iz delovnih organizacij, inštitutov in fakultet, obvestila o akcijah društva MIDEM in njegovih članov ter drugi prispevki so dobrodošli.

Ostala splošna navodila

1. V članku je potrebno uporabljati SI sistem enot oz. v oklepaju navesti alternativne enote.
2. Risbe je potrebno izdelati ali iztiskati na belem papirju. Širina risb naj bo do 7.5 oz.15 cm. Vsaka risba, tabela ali fotografija naj ima številko in podnapis, ki označuje njeno vsebino. Risb, tabel in fotografij ni potrebno lepiti med tekst, ampak jih je potrebno ločeno priložiti članku. V tekstu je treba označiti mesto, kjer jih je potrebno vstaviti.
3. Delo je lahko napisano in bo objavljeno v slovenščini ali v angleščini.
4. Uredniški odbor ne bo sprejel strokovnih prispevkov, ki ne bodo poslani v dveh izvodih skupaj z elektronsko verzijo prispevka na disketi ali zgoščenki v formatih ASCII ali Word for Windows. Grafične datoteke naj bodo priložene ločeno in so lahko v formatu TIFF, EPS, JPEG, VMF ali GIF.
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Journal of Microelectronics, Electronic Components and Materials

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