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SPUTTERED DEPOSITED TUNGSTEN SILICIDE FILMS FOR MICROELECTRONICS APPLICATIONS

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Key words: Tungsten Silicide films; DC plasma magnetron sputtering; pressure; substrate temperature

Abstract: This paper addresses the effect of substrate temperature and deposition pressure on the electrical properties of Direct Current (DC) plasma magnetron sputter-deposited Tungsten Silicide (WSi) films on silicon substrates. Results from experiments show that, substrate temperature and deposition pressure has exerted significant influence on the electrical properties of the WSi films. The electrical properties of the WSi films are inferior at high deposition pressure and high substrate temperature.

Nanašanje silicidnih filmov WSi za uporabo v mikroelektroniki

Kjučne besede: filmi vofframovega silicida, magnetronsko naprševanje v DC plazmi , pritisk, temperatura substrata

Izvleček: Prispevek obravnava vpliv temperature podlage in pritiska pri magnetronskem naprševanju v DC v plazmi na električne lastnosti napršenega volframovega silicida na silicijevih substratih. Rezultati eksperimentov so pokazali, da imata temperatura podlage in pritisk pri naprševanju velik vpliv na električne lastnosti WSi filmov. Le-te so slabše pri visokih pritiskih in temperaturah.

1. Introduction

Polycrystalline silicon (Poly-Si) has been intensively used in the manufacture of integrated circuits in MOS technology, where it is employed as a gate or interconnection material. The achievement of maximal signal transmission in emerging chip and system architectures requires the minimization of high resistance in Poly-Si. High resistance is a major limitation in circuit performance for Ultra Large Scale Integrated Circuits (ULSI) /1/. In order to tackle this problem, alternative materials other than Poly-Si are needed. Several types of silicides of refractory metals have been investigated as a replacement for Poly-Si such as Tantalum Silicide (TaSi), Tungsten Silicide (WSi) and Molybdenum Silicide (MoSi) / 1-4/. Under optimum deposition conditions, WSi has the lowest resistivity of approximately 50 μΩ cm, comparing to others, for example, 70 μΩ cm for TaSi and 80 μΩ cm for MoSi /5/. Furthermore, WSi has high melting point of 2160°C, excellent step coverage of 85% over a vertical step, high thermal stability, low stress and chemical resistance /6/. These properties make WSi an appropriate alternative to Poly-Si as gate or interconnection material. Furthermore, WSi can be applied as barrier liner in copper interconnection, to prevent the diffusion of copper (Cu) into silicon substrate. Cu interconnection is an emerging interconnection scheme employed in microelectronic industries as Cu exhibit better electrical properties than existing aluminum metallization scheme /7/.

In the present study, experiments were carried out to investigate the electrical properties of the Direct Current (DC) plasma magnetron sputter-deposited WSi films on Si substrates as a function of the deposition pressure and the substrate temperature.

2. Experimental

Figure 1 shows the schematic diagram of the magnetron sputtering deposition system. All WSi films were deposited in a DC plasma magnetron (balanced planar magnet-

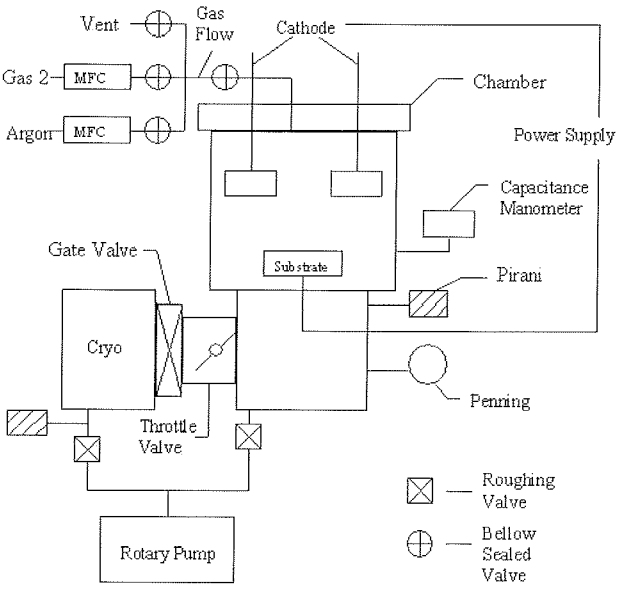

Fig. 1. The schematic diagram of the employed magnetron sputtering deposition system.

ron) sputtering deposition chamber with the base pressure maintained below 10^{-5} Torr. The circular 50.8 mm diameter WSi target was of 99.5% purity. High purity argon (Ar) gas with 99.995% purity was used as working gas in all the sputtering deposition processes. The flow rate of the Ar gas fed into the chamber was controlled by using SEVENSTAR (D07-7A/ZM) mass flow controllers. The magnetron cathode was placed at a distance of about 8 cm from the substrate holder and the substrate. The substrate was grounded during the deposition process in order to improve the efficiency of sputtering. Pressure in the sputtering chamber was measured using Pirani and Penning gauges. The geometry of Si substrates was approximately 6 mm x 12 mm. The electrical measurements of the WSi films were performed with Karl Suss four-point probe at room temperature. The deposition conditions of the WSi films presented in this study are summarized in Table 1.

Table 1. Deposition details of experiments

Target	WSi
Substrate	p-type Si
Target-substrate distance	8 cm
Ar Flow Rate	18 -20 (sccm)
Deposition duration	30 minutes
Deposition Power	50 Watt
Deposition pressure	12 mTorr to 25 mTorr
Substrate temperature	27 °C to 200 °C

3. Results and discussion

Figure 2 shows the measured I-V curves of the WSi films deposited with different pressures ranging from 12 mTorr to 25 mTorr. From the I-V curves, the voltage to current ratio (V/I) is higher when the deposition pressure is increased.

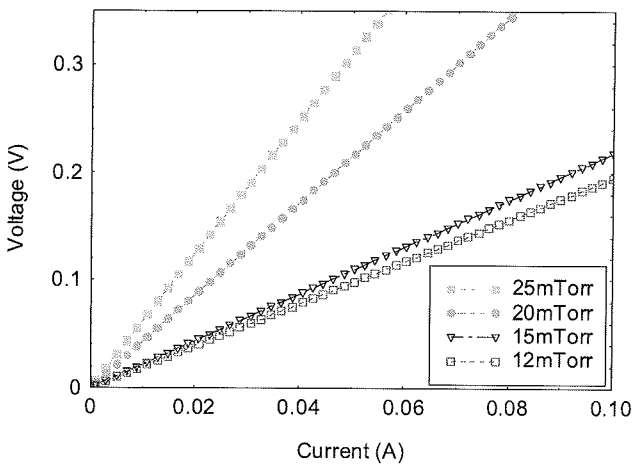

Fig. 2. WSi films at difference deposition pressures.

Referring to figure 2, the resistance, R, of the WSi films can be expressed as /8/:

$$R = V / I, \quad (1)$$

where V and I represent the voltage and current, respectively. Increase in the deposition pressure causes the film resistance to increase. The sheet resistance, R_S, can be correlated to film resistance, R. The R_S can be estimated using following equation /9/:

$$R_S = C.F. (V/I), \quad (2)$$

where C.F. is the correction factor, depending on sample geometry, which accounts for the sample size, shape and I-V probe tip spacing /10/. In this investigation, all samples geometry was kept constant. The measured film resistance of the WSi films is proportional to the sheet resistance, R_S, of the WSi films.

The film resistivity, ń, can be correlated to sheet resistance, R_S. The film resistivity can be expressed as /11/:

$$\rho = R_S t, \quad (3)$$

where t represents the thickness of the deposited WSi films. Change in the deposition pressure has no significant effect on the thickness of the deposited WSi films /12/. Therefore, the film resistivity of the WSi films can be suggested as proportional to the sheet resistance. Therefore, it can be suggested that the electrical resistivity of the deposited WSi films increases when the deposition pressure is increased.

The reason for the electrical properties of the WSi films become inferior at high deposition pressure can be explained in the following. Hara et al. /13/ have pointed out that the composition of WSi (Si/W ratio) increases when the deposition pressure is increased, because the atomic mass of the W is larger than Si. The electrical conductivity of W is higher than Si. Godbole et al. /14/ reported that film resistivity increases when the composition of WSi (Si/W ratio) increases. Si is a lighter element, so it tends to scatter more than W in the sputtering process /14/. Therefore, with the increase in the deposition pressure, resistance and resistivity of the WSi films grown on Si substrates also increase.

Figure 3 shows the electrical properties of the WSi films deposited with difference substrate temperatures ranging from 27 °C to 200 °C. The result from experiments show that the I-V curve is higher when the substrate temperature is increased; indicating a higher WSi films resistivity is obtained when a higher substrate temperature is used. This is true as the film thickness does not depend on the substrate temperature.

This result is corroborated by the research work carried out by Liang et al. /15/ on WSi films. According to Liang et al., the Si/W ratio increase when annealing temperature for the WSi films is increased up to 400 °C. Additionally, Horiuchi et al. /16/ also discussed about the film resistivity increases with the increases of the annealing tempera-

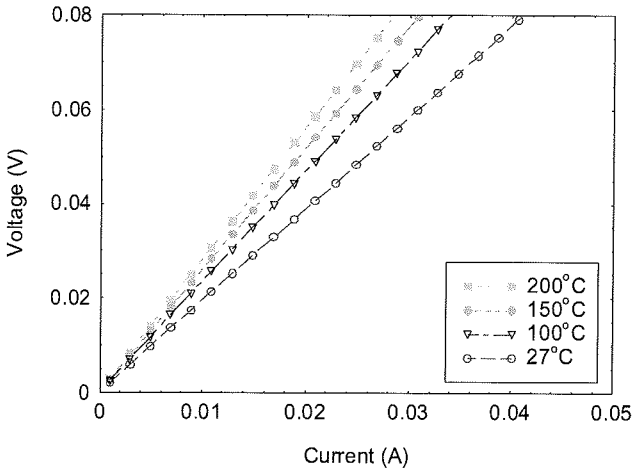

Fig. 3. WSi films at difference substrate temperatures.

ture up to around 575 °C for Titanium Silicide (TiSi) thin films. Karmed et al. reported that higher value of film resistivity is related to the change in the crystalline phase of the deposited WSi films with increasing temperature. Therefore, with the increase in the substrate temperature, resistance and resistivity of the WSi films had grown on Si substrates also increase.

4. Conclusions

In this work, the effects of the deposition pressure and substrate temperature on the electrical properties of the DC plasma magnetron sputter deposited WSi films were demonstrated. The experiment results show that the deposition pressure and substrate temperature significantly influence the electrical properties of the WSi films. The lower deposition pressure and lower substrate temperature favor the growth of WSi films with low resistivity.

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DISTRIBUTION OF DROPLETS ON RUTHENIUM THIN FILMS PREPARED BY PULSE ND:YAG LASER

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Key words: Droplet, Pulsed laser deposition, Ruthenium

Abstract: Ruthenium (Ru) has been suggested as a potential material used for various applications in microelectronic industry. Pulsed laser deposition (PLD) enables the growth of Ru thin films at low temperatures. In this report, a thin layer of Ru has been grown on silicon (Si) substrates by pulsed laser deposition technique. When using the PLD technique, the grown layers very often exhibit some micrometer sized droplets. Although the droplets on the surface of the deposited Ru film can be dramatically reduced, there is still much effort being aimed at completely eliminating their presence, which could clearly restrict its applications. In this study, we report on the droplet formation on the deposited Ru thin films. The deposition processes were carried out at room temperature in vacuum environment with a pulsed laser Nd:YAG laser of 355 nm laser wavelength, employing various laser fluences ranging from 2 J/cm^2 to 8 J/cm^2. Therefore in this paper, we studied the droplets formation under the influence of pulsed laser deposition parameters on the ruthenium. The effect of the laser fluence on the droplets formation on the deposited Ru films was observed by field effect scanning electron microscopy (FESEM).

Porazdelitev kapljic na tankem filmu rutenija pripravljenega s pulznim laserjem Nd:YAG

Kjučne besede: kapljica, nanašanje s pulznim laserjem, rutenij

Izvleček: Rutenijum je bil predlagan kot možen material za različne uporabe v mikroelektronski industriji. Pulzno lasersko nanašanje (PLD) omogoča rast tankih filmov iz rutenija pri nizkih temperaturah. V prispevku popisujemo rast tanke plasti rutenija na silicijevem substratu s pomočjo tehnike PLD. Pri uporabi te tehnike se na rastočih plasteh razvijejo mikrometrske kapljice. Čeprav njihovo število lahko zmanjšamo, je bilo veliko truda vloženega, da bi njihov nastanek popolnoma onemogočili. V tem prispevku poročamo o tvorbi kapljic na rutenijevih tankih filmih. Nanašanje je potekalo pri sobni temperaturi v vakuumu s pomočjo pulznega laserja Nd:YAG pri valovni dolžini 355nm in pri različnih energijah, med 2 J/cm^2 in 8 J/cm^2. V prispevku torej obravnavamo nastanek kapljic pri različnih pogojih nanašanja rutenija. Vpliv parametrov nanašanja smo opazovali s pomočjo elektronske mikroskopije (FESEM).

1. Introduction

Pulsed laser deposition (PLD) has been a popular thin film deposition technique to grow a large variety of thin film materials covering inorganic, organic and high melting metal from solid targets /1,2/. This method is known to have the following advantages: (a) stoichiometric agreement with the target material /3/, (b) crystallinity enhancement due to the highly energetic species /4/ and (c) clean deposition due to particle ejection only by laser irradiation /5/. In view of these advantages, the development of new materials using PLD has advanced rapidly in comparison to other thin film deposition techniques. However, the formation of droplets using PLD which is detrimental to the quality of the thin film, is a major concern that needs to be properly addressed and studied /6/. These undesirable droplets deposition is main drawback for electronic device quality semiconductor films and optical films where droplets can introduce the formation of defects and scattering centers that lower the charge carrier mobility, shorten the carrier lifetime, and downgrade the damage threshold of optical films. To date, several methods /7/ have been attempted to eliminate the undesirable droplets,. However, it has been extremely challenging to eliminate the droplets without comprising the advantages of PLD. The droplets do not grow from the precipitation on film as a grain of irregular growth, but are ejected from the surface of the target.

In this paper, we investigate and study the formation of droplets on ruthenium (Ru) thin films grown by PLD, and its dependence on the laser fluence. For these experiments, Ru was used as the material for deposition due to its increasing popularity and widely acceptance in various applications in the microelectronic industry /8-12/. In order to obtain the relevant droplet distribution information, field effect scanning electron microscopy (FESEM) was employed to study the droplet formation on the surface of the Ru target and the deposited Ru thin films.

2. Experimental

The schematic diagram of the film preparation chamber is shown in Fig.1. Ruthenium thin films were deposited on silicon (Si) substrates at room temperature by pulsed laser deposition using a circular 2-inch diameter Ru target of 99.95 % purity. The substrates were set parallel to the target at a distance of 50 mm from the target. The pulsed laser beam with energy ranging from 17 mJ to 64 mJ was

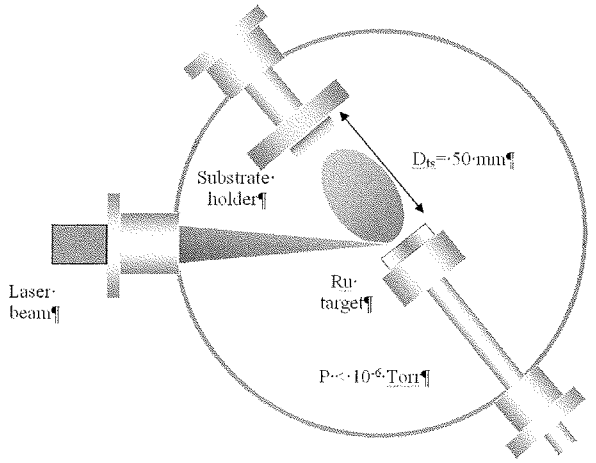

Fig. 1 Schematic diagram of the pulsed laser film deposition chamber

focused with a spherical lens onto a target with an area of 0.8 mm^2. The laser fluence was ranged from 2 J/cm^2 to 8 J/cm^2 with a repetition rate of 10 Hz. The laser beam struck on the target at an angle of 45° to the normal. The base pressure was lower than 2 × 10^{-6} Torr, achieved with a rotary pump coupled with a diffusion pump. The pulsed laser deposition processes were carried out in high vacuum environment with a pulsed Nd:YAG 355-nm laser source. The film deposition was run for a total number of irradiated laser pulses of 36,000.

The thickness of the pulsed laser deposited Ru films was characterized by Mahr surface profilometer after the deposition processes by measuring the step height between masked and unmasked regions on the substrate. The droplet formation on the surface of the Ru target and the deposited Ru thin films were observed by means of field emission scanning electron microscopy (FESEM) (LEO Electron Microscopy, LEO 1560). Detailed deposition conditions of the Ru films presented in this work are summarized in Table 1.

Table 1 Parameters for the pulsed laser deposited Ru

Laser	Nd:YAG laser (wavelength 355 nm)
Laser fluence	2 to 8 J/cm^2
Laser repetition rate	10 Hz
Targets	Ruthenium (purity: 99.95 %)
Substrates	(100) Si
Deposition time	60 min
Target-substrate distance	50 mm
Base pressure	< 2 × 10^{-6} Torr

3. Result and Discussion

Fig.2a shows the surface morphology of the Ru target before irradiation. After a few minutes of ablation which amounts to more than a few hundred laser pulses, high surface roughness of Ru target with ripple-mark was observed as shown in Fig. 2b. During PLD deposition, laser beam was directed onto the target, as the target was ablated until a certain depth in which the laser energy was rose above the threshold value where the surface evaporation happened and the molten pool was formed. The melting period was very short, and the melting zone was in minutes; as a result, the molten pool was compressed from inside of the target, and hence the formation of ripples. The ripples seem to organize and follow a certain growth direction with a small tilting angle from the surface.

The seemingly organized and same growth direction of the ripples might well attribute to the incident laser beam that was angled at 45° to the normal of the target during the deposition. As laser irradiation continues, droplets will form subsequently from the top of the ripples in the molten pool as shown in Fig 2c. The number of droplets continues to

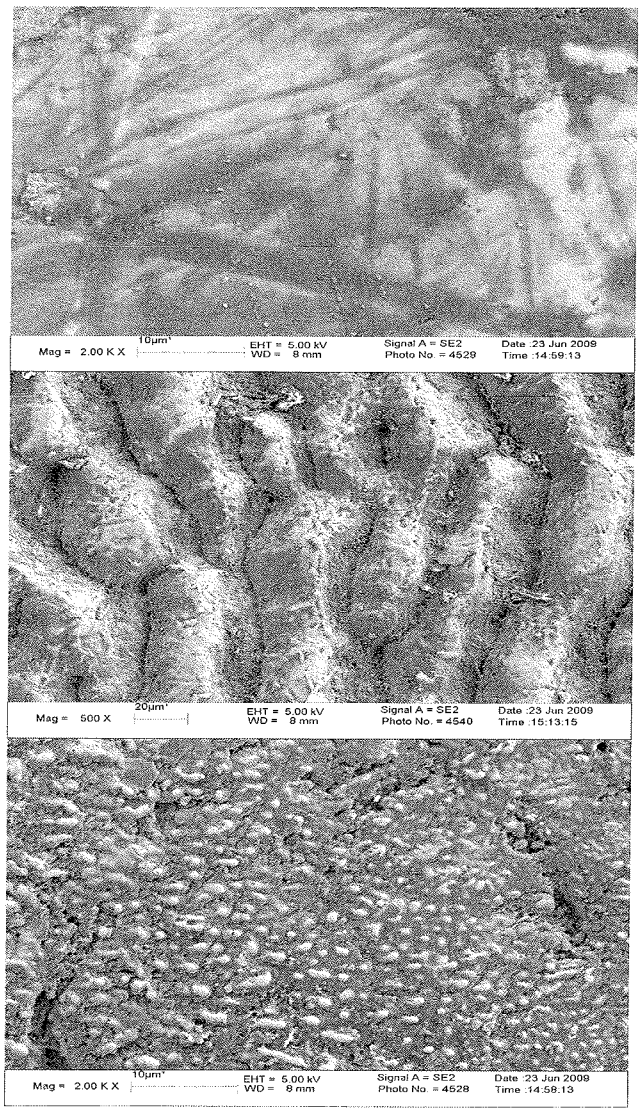

Fig. 2 The morphology of target surface before (upper), after few tens pulses (middle), and after 36,000 pulses (lower) of laser ablation.

increases as a result of continuous laser irradiation which lead to rougher surface morphology of the target and deepened laser /13/.

The thickness of Ru films deposited with laser fluence of 2 J/cm^2, 4 J/cm^2, 6 J/cm^2 and 8 J/cm^2 for duration of an hour were about 60 nm, 85 nm, 140 nm, and 180 nm as shown in Fig. 3 a, b, c, d, respectively. On the deposited Ru film surface, droplets are found as shown in Fig. 3. The presence of droplets which are rather spherical in shape on the surface of the PLD deposited Ru surface (Fig. 3) suggests that they are resulted from target splashing during laser target interaction and indicated that these droplets were (at least partially) molten before hitting the substrate. These observation of ripples on ablated target surface were also reported to contribute to the droplet formation /14/, which were formed as a result of Kevin-Helmholtz /15/ instability occurring in the interface between the molten layer and the plume. From Fig. 3, we can observe that the number of droplets and its size increase with increasing laser fluence. In order to quantitatively study the droplet formation, droplets with different sizes and diameters on FESEM images of 350 μm × 225 μm at the centre of the film were counted.

In our research, it is still not clearly understood for the mechanisms of the droplets formation. It is perhaps due to two mechanisms. First, it is due to the mechanically dislodged from the target due to laser-induced thermal and mechanical shock. Second, it is due to the rapid expansion of trapped gas bubbles beneath the surface during laser irradiation, causing forcible ejection of surface matter.

In our experiment, different droplet sizes ranging from 1 μm to 10 μm were observed as shown in Fig. 3. The number of droplets increased, and larger droplets were found with increasing laser fluence. The number of droplets and its diameter for different laser fluences are summarized in Fig. 4. From Fig. 4, it is worth noting that the droplets size falls mainly in the range between 2 to 6 μm. For Ru ablation with laser fluence of 4 to 8 J/cm^2, the size distribution of droplets follow a normal distribution curve with a peak number of droplets of 13, 38, and 65 respectively. Those droplets size which falls at the two ends of the normal distribution, increased the laser fluence seems to have less significant effect on increment of droplets count. In general, there exists threshold laser fluence, below which the droplets are negligible in size and number. Above the threshold laser fluence, the droplets number density increases rapidly with increasing laser fluence as shown in Fig 4b, c, and d. Through this experiment, we come to a simple approach to reduce the number of droplets by reducing the laser fluence to below the threshold level that causes the splashing of the molten layer. Under the Ru thin film deposition conditions in our study, we observed that the threshold laser fluence to be about 4 J/cm^2. Fig. 4 also shows that the total number of droplet increases rapidly from 22 to 73 and 147 with increasing

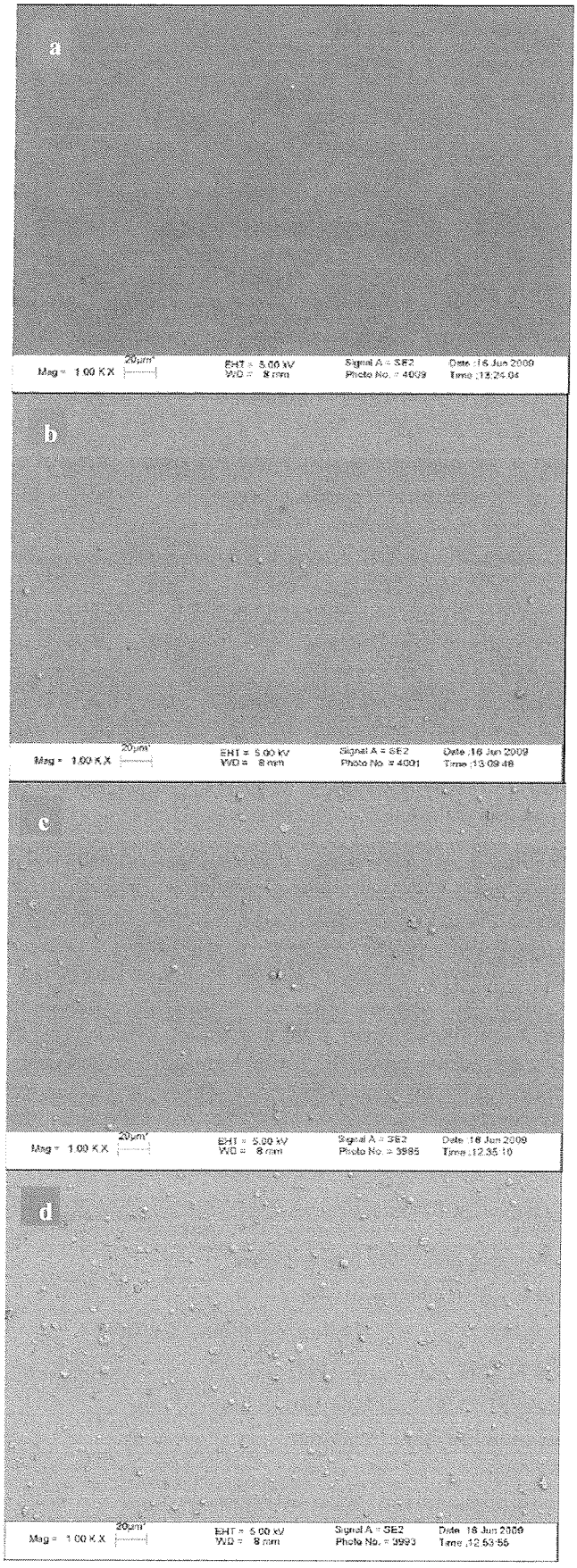

Fig. 3 The morphology of the deposited Ru film surface at laser fluence (a) 2 J/cm^2, (b) 4 J/cm^2, (c) 6 J/cm^2, and (d) 8 J/cm^2.

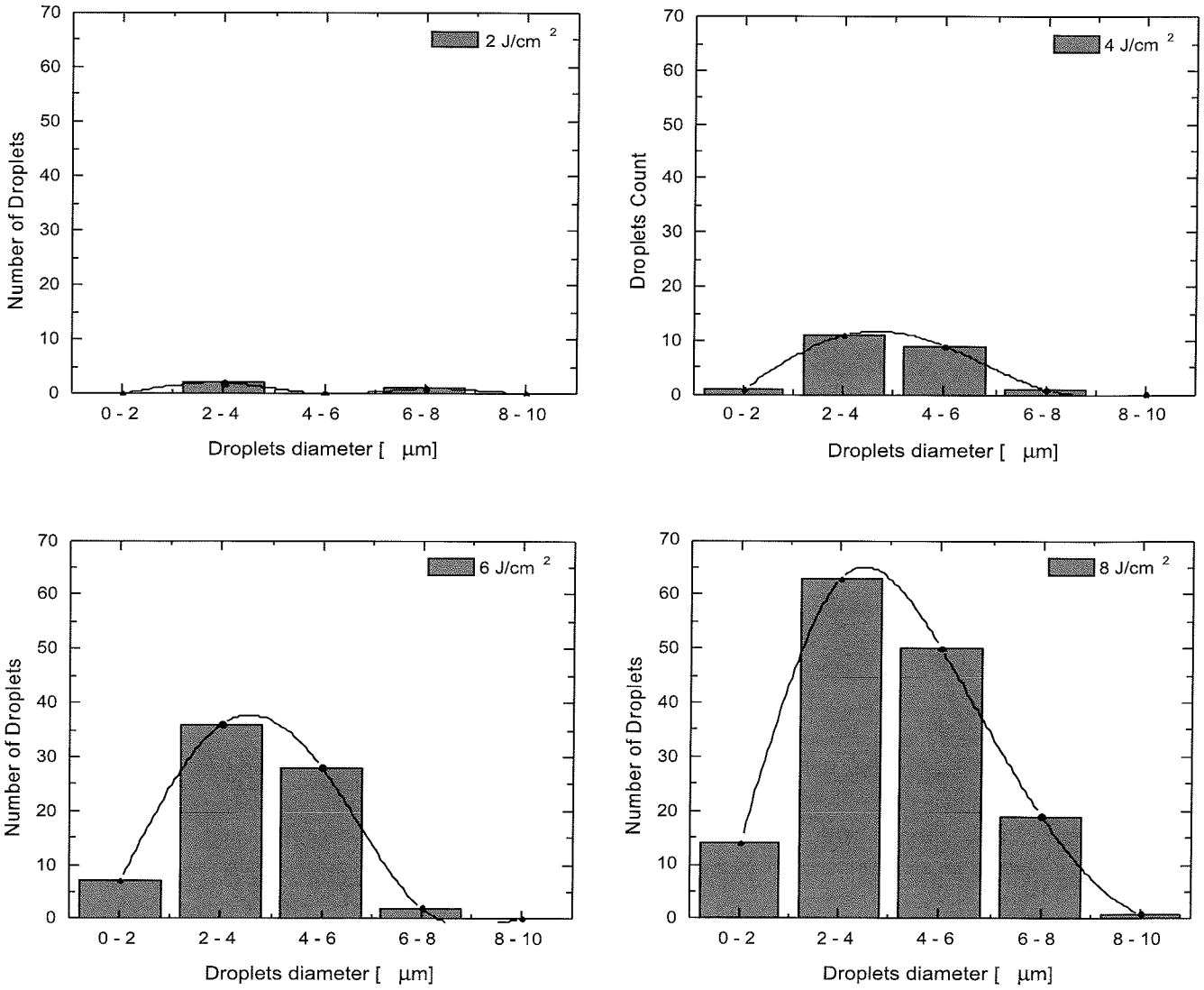

Fig. 4 Number of droplets for various droplet sizes at laser fluence (a) 2 J/cm^2, (b) 4 J/cm^2, (c) 6 J/cm^2, and (d) 8 J/cm^2.

fluence from 4 J/cm^2 to 6 J/cm^2 and 8 J/cm^2 respectively. This trend is in line with the observation made by van de Riet et al. /14/ and Dupendant et al. /16/ by comparing with different kinds of metals deposited using laser ablation.

The relationship of the number of droplets and laser fluence is shown in Fig. 5. It shows a general trend that the number of droplets increases with laser fluence. For droplets size of 2 to 4 μm and 4 to 6 μm, the increment of droplets is 61 and 50, respectively, when the laser fluence is increased from 2 to 8 J/cm^2. With compare to the droplets size of 0 to 2 μm and 6 to 8 μm, the droplets increasing is lesser with increment of 14 and 18, as the laser fluence increases from 2 to 8 J/cm^2. In addition, for droplets size of 8 to 10 μm, increasing the laser fluence from 2 to 8 J/cm^2, the droplets only increase by 1, therefore laser fluence seems to have less significant on the increment of the droplets in this region. This droplet distribution on deposition substrate can be described with a power-law for-

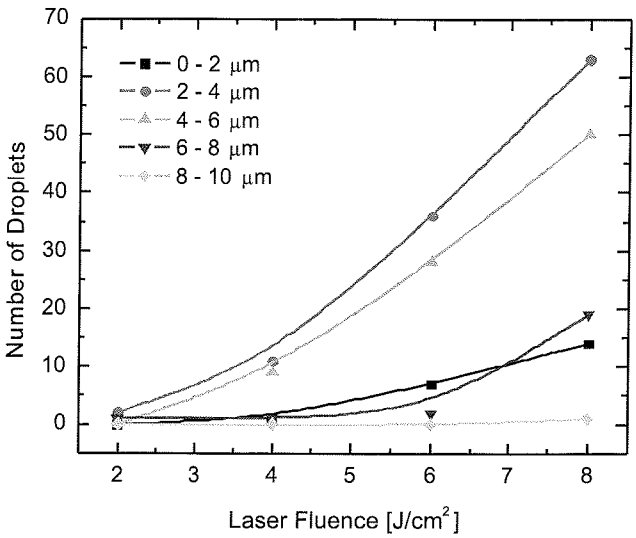

Fig. 5 Number of droplets as a function of laser fluence ranging from 2 J/cm^2 to 8 J/cm^2.

mula of the type $N(d) = a \times d^{n}$, where $N(d)$ is the density of droplets with diameter d (in μm) per square centimeter and laser pulse, a is a constant and n is the exponent of the power law /17/.

4. Conclusions

Droplets were formed from the top of the ripples that formed by the melt from laser beam on ruthenium target surface during the deposition. The initial morphology of the target was affected by the droplets formation on the target itself, which later are co-deposited to the surface of the growing substrate to form a thin Ru film with some micrometer size droplets on it. In this paper, droplets size between up to 10 μm was observed. The number of the droplets increases with increasing laser fluence. Droplets with size of 2 to 6 ěm were mainly seen on the deposited Ru films for all laser fluences. Therefore, it is observed that for Ru, as in our experiment, the threshold laser fluence is 4 J/cm^2 for 355 nm wavelength pulsed Nd:YAG laser. Below this threshold value, droplets formed on the deposited Ru films are less significant. Therefore, with the proper choice of laser fluence, droplets formation can be minimized.

Acknowledgements

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KONTAKTNI MATERIALI ZA NIZKONAPETOSTNA STIKALA V ELETROENERGETIKI

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Kjučne besede: kontaktni pojavi, nizkonapetostna stikala za energetiko, kontaktni materiali za elektroenergetiko, zlitine AgMe, kompoziti Ag/Me, kompoziti Ag/MeO, kompoziti Ag/C, uporaba kontaktnih materialov

Izvleček: Učinke kontaktnih pojavov, ki delujejo na električne kontakte v stikalih za nizkonapetostne energetske tokokroge, upoštevamo pri presoji ustreznosti kontaktnega materiala za predvidene specifične pogoje uporabe. Izbiramo pretežno materiale na osnovi bakra in srebra, od teh pa se največ uporabljajo zlitine AgCu in AgNi 0,15, kompoziti Ag s kovinskimi granulati (Ag/Me), z granulati kovinskih oksidov (Ag/MeO) iz z grafitnimi vlakni. Značilni predstavniki Ag/Me materialov so Ag/Ni in Ag/W, od Ag/MeO materialov pa Ag/CdO, pridobljen s postopkom notranje oksidacije in Ag/CdO, Ag/SnO_2 ter Ag/ZnO, pridobljen s postopkom metalurgije prahov. Za odklopnike je zanimiv kompozit Ag/C z pravokotno in vzporedno usmeritvijo grafitnih vlaken. Za te materiale so opisane njihove osnovne električne lastnosti s poudarkom na uporabi v stikalni tehniki, prikazana je njihova metalografska struktura in kratek opis postopkov izdelave. V sklepu je podana ugotovitev, da do sedaj še ni uspelo izdelati univerzalnega kontaktnega materiala za vse pogoje, pri katerih morajo stikalni aparati v energetskih tokokrogih nizke napetosti dolgo in zanesljivo delovati.

Contact materials for low-voltage power switching devices

Key words: electric contact phenomena, low-voltage switching devices, contact materials for low-voltage power conditions, AgMe alloys, composites Ag/Me, composites Ag/MeO, composites Ag/C, application of contact materials

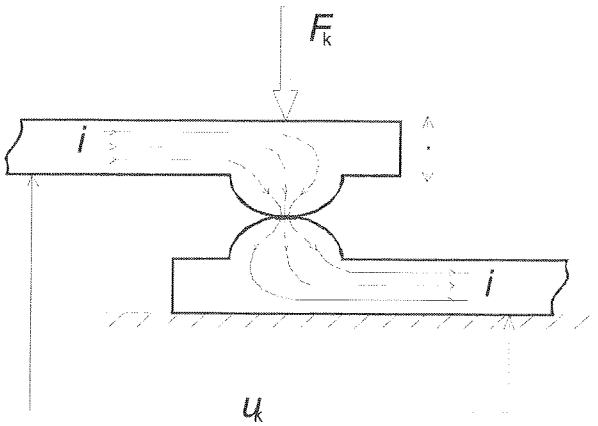
Abstract: Electrical contact phenomena affecting contacts of low-voltage switching devices in power circuits shall be taken into consideration for selection of the suitable contact material regarding the presumed specific conditions of switching operation. The candidates for contact materials are found among copper-base and silver-base materials. Most frequently used are AgCu and AgNi 0,15 alloys, as well as composite materials of Ag with metal granulates (Ag/Me), with metal-oxide granulates (Ag/MeO) and with graphite filaments (Ag/C). Typical materials of Ag/Me composites are Ag/Ni and Ag/W, while among Ag/MeO materials widely used Ag/CdO produced by internal oxidation, as well as Ag/CdO, Ag/SnO_2 and Ag/ZnO produced by powder metallurgy. In circuit breakers frequently used are Ag/C materials having graphite filaments oriented in parallel or perpendicularly to the contact surface. Basic electrical characteristics concerning the application for electrical contacts are described and the metallographic structure is shown as well for the above listed materials. Brief descriptions of manufacturing methods are also given. In the conclusion it is stated that up to now not any contact material has been manufactured yet having universal contact characteristics which provide durable and reliable switching operations of contacts at majority of operating conditions in low-voltage power circuits.

1. Uvod

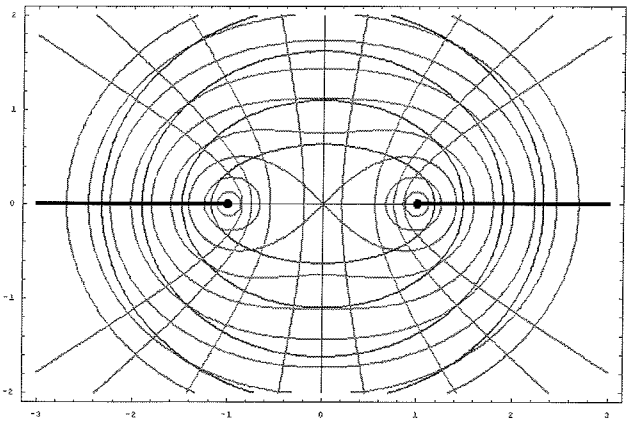
Če v električnem tokokrogu želimo vključevati in prekinjati električni tok skozi porabnik, lahko to opravimo to enostavno tako, da fizično stikamo in razmikamo med seboj dva električna vodnika. Vendar so se elektrotehniki več desetletij ukvarjali z vprašanjem, kako zagotoviti dolgotrajen zanesljiv stik, zakaj tudi na priključku transformatorja stik lahko odpove, zakaj v stikalu pri kakem od vklopov mehanizma tok ni stekel, zakaj pri izklopu stikala včasih toka ne moremo prekiniti in teče skozenj do uničenja stikala ali komponente tokokroga, ter podobnim, ki so še danes ne tako redka vprašanja vsakdanje prakse v stikalni tehniki. Zato je treba opisati nekatere značilne pojave pri vklopu, prevajanju in izklopu toka z mehansko upravljanimi kontakti.

Dva električna vodnika, ki ju staknemo med seboj, da med njima teče električni tok, tvorita kontaktni par. Na stičnih delih, ki so najpogosteje na izpostavljenih delih obeh električnih vodnikov, nastane kontaktno mesto, kjer je električni kontakt med deloma kontaktnega para. V stiku ju drži zunanja sila F_k [N], ki nanju izvaja kontaktni stisk (Sl. 1).

Ta povzroča na kontaktnem mestu deformacijo stičnih površin, tako da je kontaktni par v fizičnem stiku na majhnem delu naležne površine, ki jo določa deformirano področje. Vendar je eksperimentalno ugotovljeno, da v realnih pogojih le majhen del stične površine s ploščino *a* tudi prevaja električni tok /1/. Pri prehodu skozi električno prevodno ploskev *a* se tokovnice električnega toka zelo zgostijo (Sl. 2), kar se na kontaktnem mestu odraža kot upor zožitve R_k [Ω]. Ker kontaktna sila F_k neposredno vpliva na velikost ploskve *a*, je tudi upor zožitve v neposredni zvezi z R_k. Empirično je ugotovljena splošna relacija (1), ki



Slika 1: Shematični prikaz kontaktnega para v sklenjenem stanju



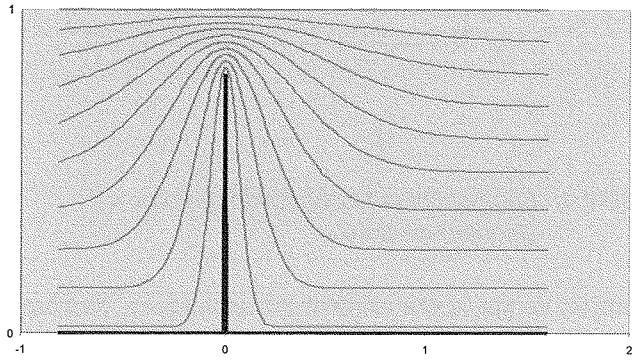
Slika 2: Simulacija razmer na električno prevodnem delu kontaktnega mesta - tokovnice električnega toka (hiperbole), ekvipotenciali (elipse) in izoterme (Cassinijeve jajčnice)

velja dovolj dobro za kontaktni par iz različnih materialov v različnih okoljih in raznih geometrij:

$$R_k = \alpha F_k^{-\beta} \qquad (1)$$

kjer so v vrednosti konstante α in eksponenta β upoštevani zgoraj našteti vplivi. Za vrednost eksponenta se najpogosteje navaja vrednosti $0{,}3 < \beta < 1$ /2/. Okoli zožitve se znatno poveča tudi gradient električnega potenciala, zato pretežni del električne napetosti U_k med deloma kontaktnega para pripade razliki potenciala ob stičnem mestu. Zaradi električne upornosti materiala kontaktnega para se sprošča toplota, ki se odvaja po kontaktnih delih in preko okoliškega medija v okolico. Izoterme na stičnem mestu kažejo, da najbolj vroče področje leži na robu električno prevodne ploskve /3/, kar pri vplivu okoliškega medija in tujih plasti na stičnih površinah omejuje dolgoročno stabilnost stika.

Zožitev toka skozi stično mesto povzroča tudi magnetne učinke. Če se snop tokovnic toka I pri prehodu iz preseka s



Slika 3: Zoženje tokovnic električnega toka na čelnem stiku dveh valjastih vodnikov pri prehodu skozi majhno električno prevodno ploskev na osi cilindra, simetrijska os polja tokovnic poteka po zgornjem robu slike

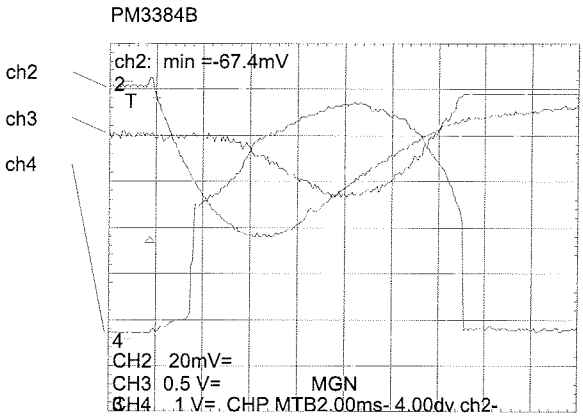
ploščino A zoži na presek s ploščino a (Sl. 3), nastane na zožitvi med vodnikoma odbojna sila F_b, določena z (2) /4/:

$$F_b = C\, I^2 \ln\left(\frac{A}{a}\right) \qquad (2)$$

kjer je empirično ugotovljeno, da za primere običajne prakse velja približna ocena iz (2a):

$$F_b\,[\mathrm{N}] = 0{,}5\, I^2\,[\mathrm{kA}]^2 \qquad (2a)$$

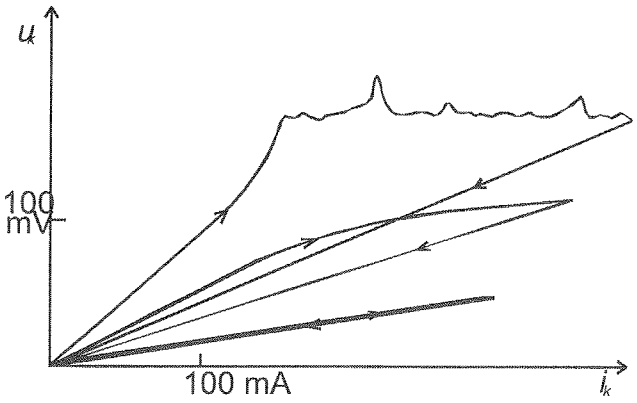
Če odbojna sila F_b pri toku I preseže silo kontaktnega stiska F_k, se kontaktni par razpre in prekine tok I (samo pri dovolj majhnem toku in/ali napetosti!), nakar sila F_k ponovno sklene kontakt. Če pa so pogoji v tokokrogu $I > 1$ A, $U_k > 125$ V /5/, kar v je elektroenergetskih tokokrogih zelo pogosto (npr. $U_e = 230$ V, $I_n = 6$ A), potem v trenutku razmaknitve stičnih površin nastane električni oblok z napetostjo $U_a \geq 12$ V pri toku $i(t)$, ki ga določajo pogoji v tokokrogu (Sl. 4). Integral produkta $U_a\, i$ po t v času trajanja obloka t_a določa količino sproščene toplote, ki na stičnem mestu ustvari bazen staljenega kontaktnega materiala, v katerem se kontaktni par po kratkotrajnem odskoku spet stakne in takoj po ohladitvi nastane kontaktni zvar. Velikost kontaktnega zvara je odvisno od sproščene energije v času odskoka kontaktov in s tem tudi sila, ki jo je treba za prekintev zvara. Na preklopnih kontaktih stikal so tudi v običajnih razmerah mikrozvari na kontaktnem paru dokaj pogost pojav (Sl. 5).



Slika 4: Odskok gibljivega kontaktnega dela v kontaktnem paru (sled »ch3«: ≈ 0,5 mm/del) zaradi tokovnega sunka i(sled »ch2«: 500 A/del) in napetost na kontaktnem paru u_k (sled »ch4«: 10 V/del). Opazen je takojšnji skok u_k na vrednost minimalne obločne napetosti v trenutku razmaknitve kontaktnih površin.

Zaradi dobrega električnega stika morajo biti kontaktne površine primerno čiste. Vsaka tehnično čista kovinska površina, ki je v okoliški atmosferi, je vedno pokrita vsaj s tanko tujo plastjo adsorbiranih, kondenziranih ali kemijsko vezanih komponent plinov in par, ki povzroča dodatni prehodni upor kontaktnega para /6/. Če je vpliv tuje plasti nezaznaven, ima prehodni upor kontakta značilnosti ohmskega upora. Prehodni upor kontakta pa se lahko z velikostjo prevajanega toka spreminja bodisi zaradi širjenja ele-

Slika 5: Mikrozvar na kontaktnem mestu po vklopu toka, stanje po razmaknitvi kontaktnih površin, SEM - dolžina markerja 100 μm



Slika 6: Nelinearnost u_k (i) kontaktnega para glede na razmere na kontaktnem mestu

ktrično prevodne ploskve *a*, zaradi tanjšanja vmesne slabo prevodne plasti, zaradi taljenja stičnega mesta ali zaradi električnega preboja tuje plasti. Ti pojavi se odražajo na grafih Sl. 6 in jih pripisujemo učinku »cvrtja« (fritting) kontaktnega mesta /7/. Intenzivnost cvrtja je odvisna od vrste kontaktnega materiala, okoliškega medija in od tuje plasti na kontaktni površini. Glede na namen uporabe kontaktnega para (napetost, tok, okoliški medij, kontaktna sila, ...) se izbere tudi ustrezni kontaktni materiali, za katerega so ti vplivi zanemarljivi /8/.

Zaradi potrebne kontaktne sile in zaradi dinamičnih mehanskih obremenitev pri vklopu (deformacija pri naletu kontaktnih površin) mora biti material kontaktnih oblog (t. j. kontaktni material) na stičnem mestu mehansko dovolj odporen, da ne pride do nedopustne spremembe oblike ali celo hladnega zvara kontaktov. Zaradi elastične deformacije kontaktov pri vklopu nastane nekaj odskokov gibljivega kontaktnega dela v paru, kar lahko povzroči do kontaktni zvar /9/ zaradi istih pojavov, kot pri elektromagnetni odbojni sili na kontaktnem paru zaradi zožitve toka.

Pri izklopu toka pri pogojih $I > 1$ A, $U_k > 125$ V nastane na stičnem mestu med razmikajočimi se površinami kontaktnega para električni oblok. Sproščena toplota, ki se absorbira v kontaktne površine, na njih tali in uparja kontaktni material. Ta delno izpari v okolico, večidel pa se izbrizga po kontaktnih delih, tako se ga z vsakim izklopom nekaj izgubi s kontaktnih oblog /10/. Ko so te na kontaktnem mestu večidel izžgane, nastane kontaktni zvar ali prevelika prehodna upornost kontakta ali pa fizični stik kontaktnega para sploh ni več mogoč. Ti pojavi določajo električno trajnost kontaktov v stikalih za energetiko.

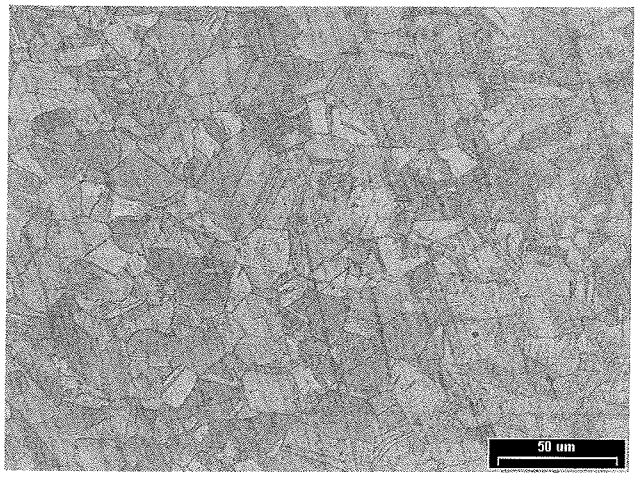
2. Splošne zahteve za kontaktne materiale v energetiki

Za zanesljivo opravljanje stikalne naloge moramo kontaktnemu paru zagotoviti silo kontaktnega stiska, ki ustreza izbranemu kontaktnemu materialu, tega pa izberemo med materiali z dobro električno prevodnostjo, ki omejuje prekomerno segrevanje kontaktnih delov, ter z ustrezno mehansko trdnostjo, ki zagotavlja omejene deformacije kontaktov. Tvorba izolacijskih ali slabo prevodnih tujih plasti na kontaktnih površinah v okoliškem mediju ne sme omejevati dobrega kontakta, zato mora biti material kontaktnih oblog kemijsko dovolj odporen na vplive okolice, da je tuja plast dovolj tanka in/ali mehansko in termično dovolj razgradljiva. Zaradi velikega termičnega učinka obloka na kontaktno površino naj bo material kontaktnih oblog dovolj odporen na obločno izžiganje, ali pa oblok čim hitreje speljemo s kontaktnega mesta, zato naj material omogoča dobro gibljivost obloka po kontaktni površini /11/. Kjer je možnost kontaktnega zvara velika ali pa predstavlja ta nevarno napako delovanja stikalnega aparata, izberemo kontaktni material z visokim tališčem ali pa z mehansko krhkim zvarom.

Veliko teh zahtev si medsebojno bolj ali manj nasprotuje, zato so za posamezne aplikacije potrebni kompromisi. Širšim zahtevam za kontakte v energetiki nizke napetosti v splošnem dokaj dobro ustreza srebro (Ag) in materiali z osnovo srebra /12/, delno tudi baker (Cu) in materiali z osnovo bakra. Kot pomožne materiale z omejeno uporabnostjo in za dodatke k Ag in Cu pogosto najdemo tudi Sn, Cd, Ni, Fe, Mo, W in C (grafit).

3. Baker, srebro in srebrove zlitine

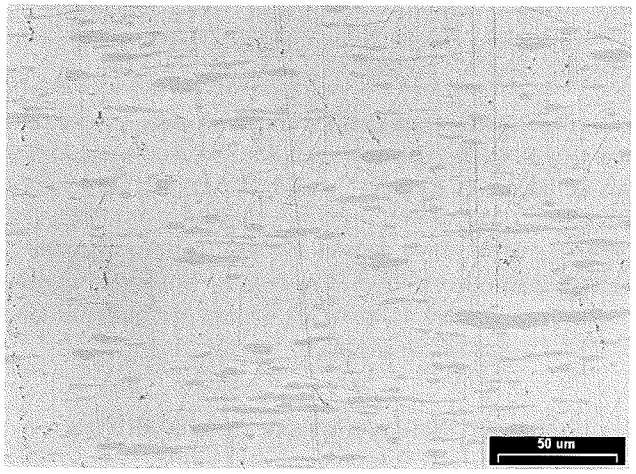
Obe kovini imata zaradi svoje kristalne strukture veliko električno prevodnost in omogočata dobro preoblikovanje v hladnem (Sl. 7). Baker (Cu) je podvržen oksidaciji in v vročem tvori debele plasti CuO /13/, zaradi česar ga upo-



Slika 7: Značilna metalografska struktura nelegiranega Cu, Ag in večine drugih nelegiranih kovin za električne vodnike v energetiki, vidne so meje med posameznimi kristali

rabljamo največ kot nosilni material za kontaktne obloge in električno prevodne dele. Kot kontaktni material nastopa v nesimetričnem kontaktnem paru, kadar je drugi partner kemijsko obstojnejši srebrni material z zelo nehomogeno sestavo kontaktne površine, na kateri je gibljivost obloka zelo omejena. Kontaktna površina Cu omogoča obloku dobro gibljivost, tako da je s tem kompenzirana ta slabost prvega partnerja v kontaktnem paru.

Srebro (Ag) ima bakru podobne električne lastnosti, odporno je na oksidacijo, eventualni oksidi so termično razgradljivi pri ≈ 200° C /13/. V atmosferi s spojinami žvepla pa tvori površinski Ag_2S, ki je glede na debeline plasti modre do črne barve. Plast Ag_2S se mehansko delno razgradi že z mehanskim stikanjem kontaktnega para in ima polprevodne lastnosti /13/, zato nima katastrofalnega vpliva na kontaktne lastnosti. Srebro je mehko in zato neodporno na mehanske deformacije pri preklopih, zato se uporablja za kontakte z majhnimi kontaktnimi silami, t. j. za preklapljanje majhnih tokov reda 1 A.



Slika 8: Metalografska struktura kompozita Ag/Ni - prerez v smeri ekstrudiranja. Razpotegnjene temnejše lise so zrna Ni v svetlejšem Ag.

Zaradi večje mehanske odpornosti je srebro legirano s 3 ... 5 ut. % Cu (materiali AgCu 3 ... AgCu 5), pri čemer se mu nekoliko zmanjša električna prevodnost. Tudi legiranje z Ni do meje topnosti 0,2% /14/ ima podoben učinek, kot s Cu, zato uporabljamo za kontaktni material tudi zlitino AgNi 0,15 z 0,15 ut. % Ni.

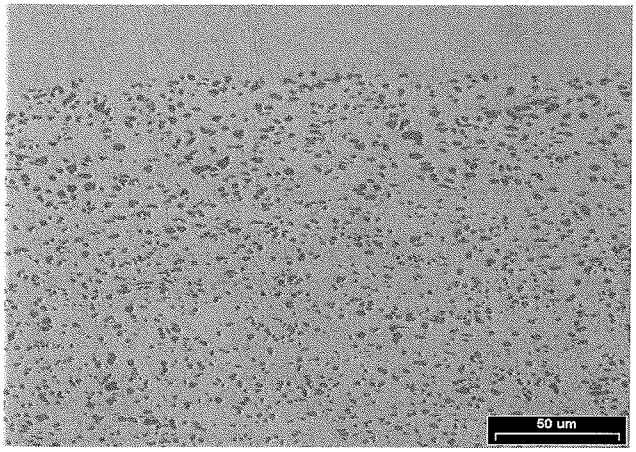
4. Zmesi srebra s kovinskimi granulati

Med kontaktnimi materiali na osnovi srebra najdemo tudi zmesi, kjer so srebru dodana drobno razpršena zrna v Ag slabo topne kovine z višjim talliščem od Ag, v velikosti reda 1 μm /8/. Kot primes se dodaja granulat niklja (Ni) ali železa (Fe). Značilni predstavnik teh materialov z vsebnostjo od 10 ut.% do 30 ut.% Ni je kontaktni material Ag/Ni 10 ... Ag/Ni 30, kjer so ohranjene pretežno vse dobre električne in mehanske lastnosti Ag, tudi zmožnost dobrega preoblikovanja v hladnem. Zato je kot polproizvod vlečen v žico ali profil pravokotnega preseka, kjer se mu metalografska struktura uredi v smeri deformacije (Sl. 8). Material je primeren za kontaktne obloge, ki so izpostavljene intenzivnemu izžiganju z oblokom pri izklopu in kjer naj stikalni aparat v svoji delovni dobi opravi veliko število preklopov. Talina Ag s primešanim trdnim granulaton Ni ima večjo viskoznost od čistega Ag, ker trdni granulat zgosti talino, zato se ga manj materiala izbrizga v okolico. Stopnja erozije Ag/Ni je zato manjša in električna trajnost kontaktov večja. Ker ima nehomogeni material v notranji zgradbi dodatne mejne površine, je manj odporen na nateg, zato je tudi kontaktni zvar manj trden: material Ag/Ni je zato primeren za pogoje, kjer obstaja nevarnost kontaktnega zvara. Iz zdravstvenih razlogov se namesto Ni uporablja tudi granulat Fe.

Material se da dobro preoblikovati v hladnem, zato lahko izdelamo kontaktne obloge neposredno iz žice, ki jo po koščkih nanašamo na kontaktne dele, uporovno ali ultrazvočno privarimo na podlago in pregnetemo v obliko kovice. Lahko pa je izdelan v obliki predfabriciranih kontaktnih kovic, ki jih vstavimo v kontaktni del. Kovice so lahko sestavljene iz dveh ali treh delov (bimetalne, trimetalne) kot kombinacija Cu in Ag/Ni, ki so spojeni z udarnim varjenjem v hladnem.

Zmesni kontaktni material je tudi kompozit volframa (W) in srebra - Ag/W, kjer je osnova kontaktne obloge iz poroznega sintranega W, ki je prepojen z Ag. Vendar je vloga W v Ag bistveno drugačna od vloge Ni ali Fe. V sestavi materiala Ag/W je dominantna komponenta W (50 ut. % do 80 ut. %) /8/, ki je zaradi visokega tališča zelo odporen na izžiganje z izklopnim oblokom, Ag pa zagotavlja dobro električno prevodnost. Zato se kontaktni materiali Ag /W50 ... 80 uporabljajo za dele kontaktnih oblog na mestih, ki so izpostavljeni intenzivnemu obločnemu izžiganju.

Material se zaradi sintrane osnove iz W ne da preoblikovati, pač pa je treba uporabiti predfabricirano končno obliko kontaktne obloge.

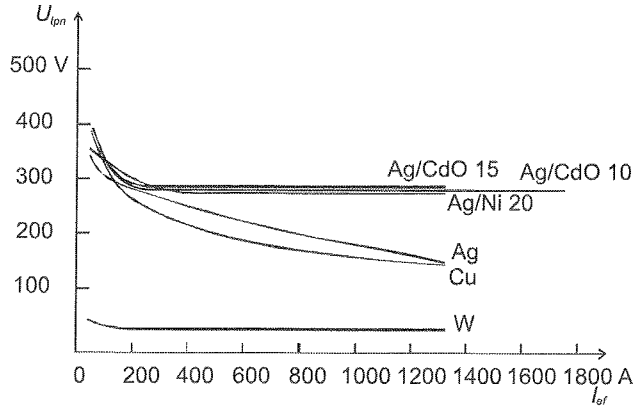


Slika 9: Značilna metalografska struktura Ag/MeO: Ag/CdO 10 - temnejše pegice so zrna CdO v svetlejšem Ag, ob zgornjem robu slike je plast Ag brez oksidnih zrn uporabljena kot varilna plast za spajanje kontaktne obloge na nosilec.

5. Zmesi srebra z granulati kovinskih oksidov (MeO)

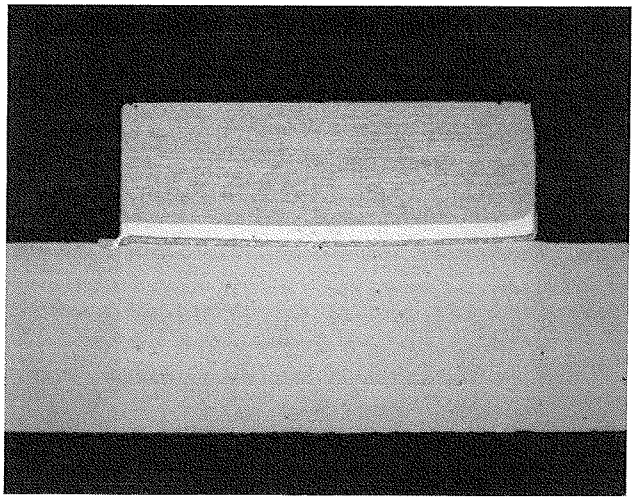
Kovinski oksid je primešan srebru v obliki drobno razpršenega granulata z zrni reda velikosti 1 μm /15/, metalografsko strukturo kaže Sl. 9. Predvsem so to oksidi kadmija CdO, cinka ZnO in kositra SnO_2 z vsebnostjo do 15 ut.% oksida v Ag. Primes oksida nebistveno poslabša dobre električne lastnosti Ag, bolj pa mehanske. Material z vsebnostjo več kot nekaj ut. % oksida se zaradi povečane krhkosti ne da več zadovoljivo preoblikovati v hladnem. Zaradi izrazito nehomogene mikrostrukture je odporen na varjenje, ker nastane krhek kontaktni zvar, ki ga mehanizem za upravljanje kontaktov stikalnega aparata zlahka raztrga. Kovinski oksid pri stiku z izklopnim oblokom zmanjša obločno napetost, vendar nekoliko podaljša čas gorenja obloka, lahko tudi razpada (CdO pri približno 1300° C disociira na kadmij in kisik /16/). Struktura materiala se v področju delovanja obloka lahko tudi precej spremeni zaradi koagulacije drobno razpršenih oksidnih zrn v večje kose. Vendar je stopnja izžiganja zaradi obloka pri teh materialih zadovoljivo majhna, da se uporabljajo za pogosto preklapljanje tokov reda velikosti nekaj 100 A in za vklop tokov nekaj 1000 A, kjer obstaja velika možnost kontaktnega zvara. Ag/CdO 10 ... 15, Ag/ZnO 6 ... 10 in Ag/SnO_2 8 ... 12. Zaradi navedenih lastnosti imajo kontaktni materiali z MeO večjo stikalno zmogljivost, kot kontakti iz Ag/Ni.

Ti materiali se odlikujejo tudi po veliki in od toka skoraj neodvisni *takojšnji napetosti povratnega vžiga*. Po ugasnitvi izklopnega obloka se med razprtim kontaktnim parom takoj (to pomeni v časovnem merilu 1 μs) vzpostavi napetost 200 ...300 V tudi pri izklopih tokov reda do nekaj 100 A /17/ (Sl.10), V tokokrogih z obratovalno napetostjo do 230 V kontakti s tem kontaktnim materialom zanesljivo, brez povratnega vžiga obloka, pri veliki pogostostjo preklapljanja izklapljajo toke reda nekaj 100 A.



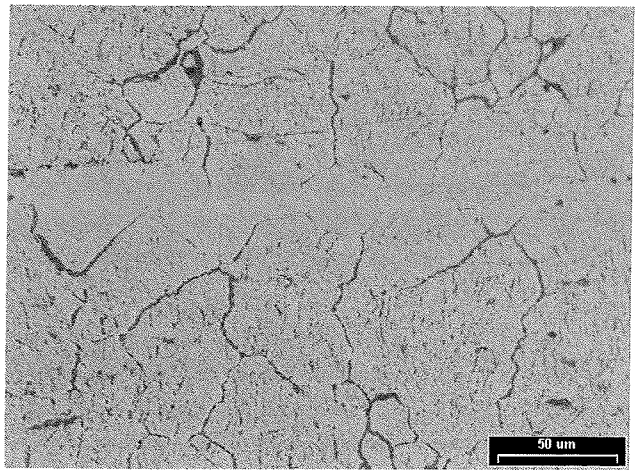
Slika 10: Takojšnja napetost povratnega vžiga U_{tpn} kot funkcija toka izklopa za nekatere največ uporabljene kontaktne materiale. Prednost kompozitov Ag/Me in Ag/MeO pred Ag in Cu je izrazita pri večjih tokovih.

Zaradi omenjenih mehanskih lastnosti se te materiale z več kot kak ut. % kovinskega oksida oblikuje z ekstruzijo, zato pri izdelavi kontaktnih delov lahko uporabljamo le predfabricirane kontaktne obloge v obliki kovic za vstavljanje ali profiliran trak ustrezne oblike, iz katerega režemo ploščice in jih elektrouporovno ali ultrazvočno navarimo na kontaktni del. Odpornost proti kontaktnemu zvaru pomeni tudi slabo varljivost na nosilno podlago, zato je kontaktna obloga na strani spajanja na podlago obložena s tanko plastjo za varjenje, npr. Ag ali trde spajke za spajkanje, kot kaže prečni presek kontaktne obloge na Sl. 11.



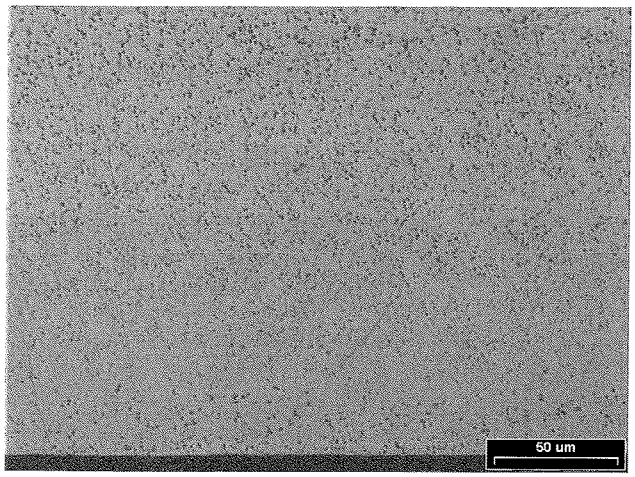
Slika 11: Zgradba ploščice za kontaktno oblogo (pravokotnik na zgornji polovici slike) iz Ag/MeO, odpornega na kontaktni zvar, ki je privarjena na nosilec. Med Ag/MeO materialom (večje sivo polje) in Cu nosilcem je vidna plast Ag (svetel pas) in plast trde spajke Agphor 15 (tenak siv pas)

Vnos kovinskega oksida (MeO) v Ag je mogoč s procesom notranje oksidacije zlitine AgMe, kjer zlitino pri visoki tem-



Slika 12:Delna notranja oksidacija Me-komponente v AgMe zlitini po mejah kristalnih zrn

peraturi izpostavimo kisikovi atmosferi. Zaradi difuzije kisika s površine kovinskega kosa v notranjost se Me globinsko oksidira in izloča v obliki oksidnih zrnc. Proces je najhitrejši po kristalnih mejah (Sl. 12), z dovršeno tehnologijo pa je MeO razporejen enakomerno po vsem volumnu (Sl. 13).

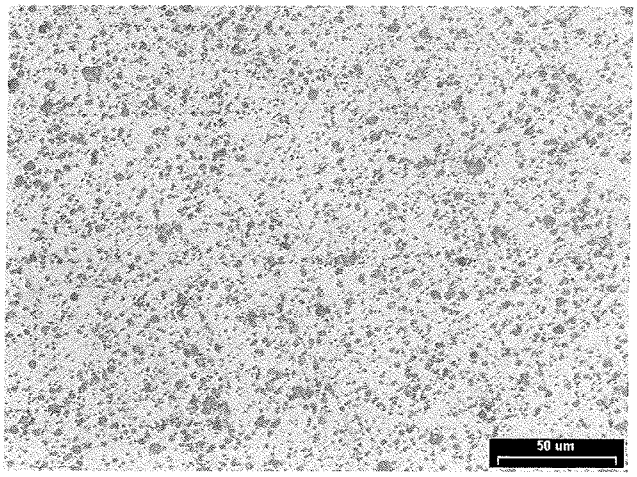


Slika 13:Notranja oksidacija Cd v zlitini AgCd, zrna CdO so razporejena enakomerno po kristalni strukturi materiala. Kontaktna površina je ob spodnjem robu slike

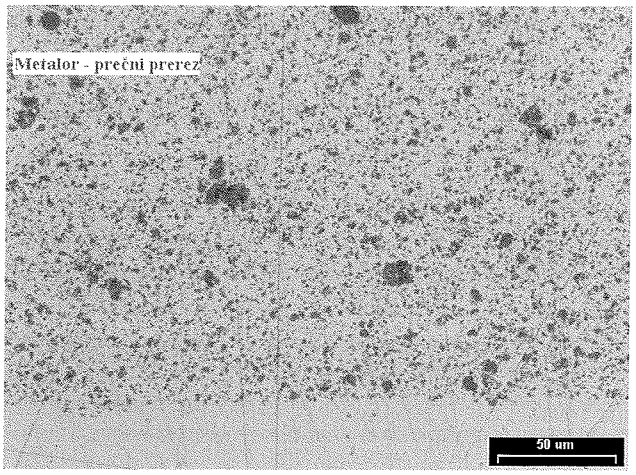
Tehnologija notranje oksidacije se uporablja pri Ag/CdO in Ag/SnO_2, Ag/ZnO in nekatere različice materiala Ag/CdO pa se izdelujejo z metalurgijo prahov iz zmesi granulata Ag in MeO s sintranjem in ekstruzijo v profilirane trakove (Sl. 14) in kovice. Zaradi direktive ROHS se Cd opušča, zato bo opuščen tudi Ag/CdO.

6. Zmesi srebra z grafitnim granulatom

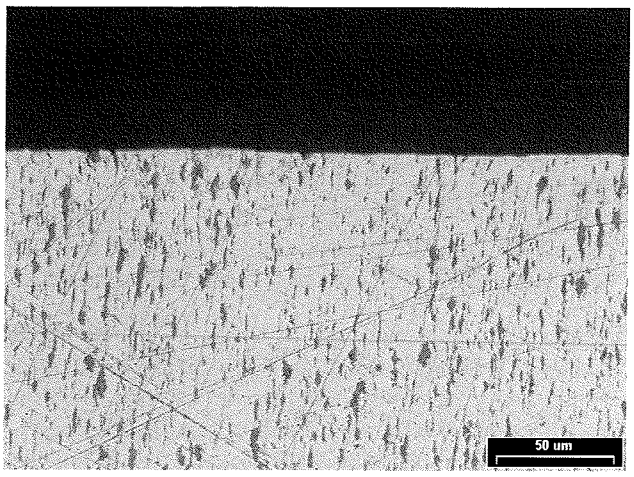
Kontaktni materiali z grafitnim prahom od 3 ut. % do 5 ut. % v Ag (Ag/C 3 ... 5) imajo veliko odpornost na kontaktni



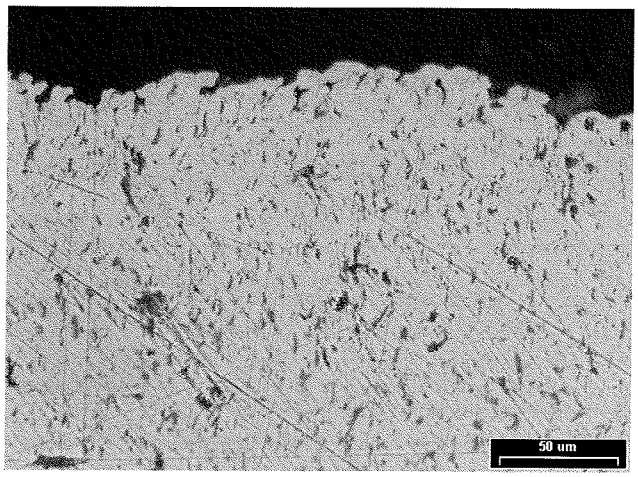
Slika 14a: Material Ag/MeO, izdelan z metalurgijo prahov – metalografska struktura Ag/SnO_2 12



Slika 14b: Material Ag/MeO, izdelan z metalurgijo prahov – metalografska struktura Ag/ZnO 12, ob spodnjem robu plast Ag kot varilna plast za spajanje na nosilec.

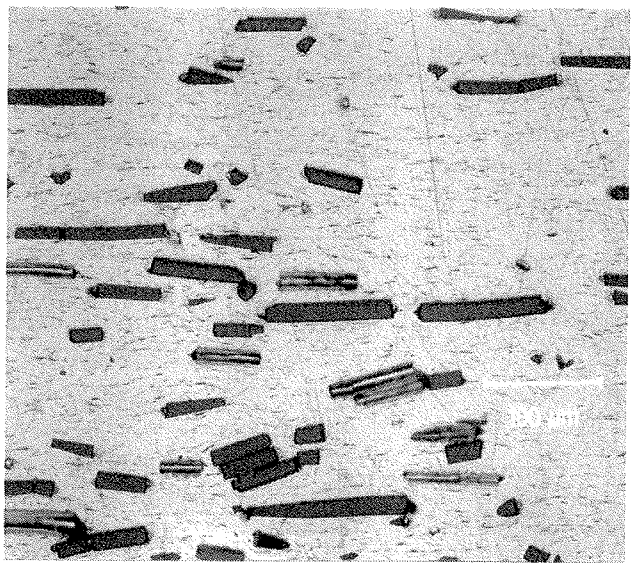


Slika 15:Struktura Ag/C s pravokotno na kontaktno površino usmerjenimi grafitnimi vlakni (temne lise), prikazan je predel pod kontaktno površino

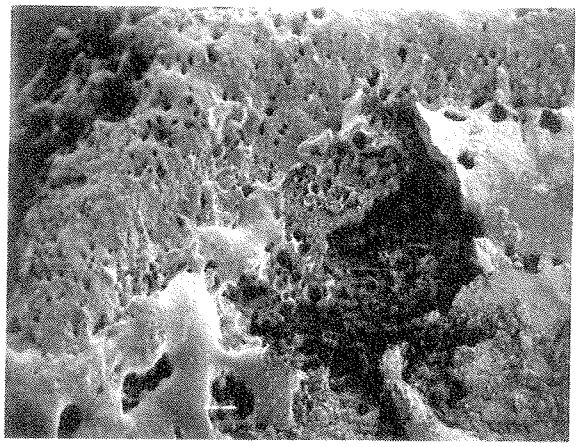


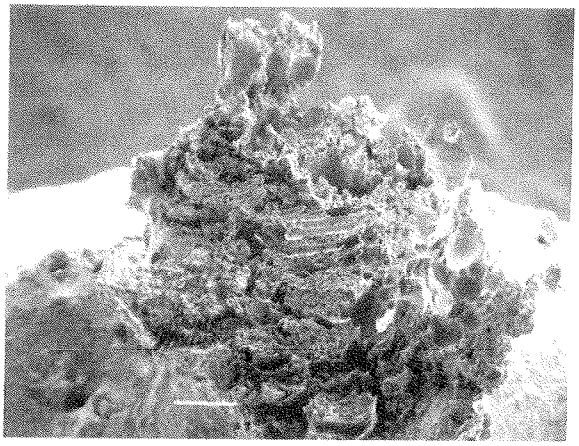
Slika 16: Tvorba gobaste plasti na staljeni kontaktni p površini Ag/C zaradi termičnega učinka podnožja izklopnega obloka.

zvar. To jim omogoča posebna struktura porazdelitve C: grafitna vlakna so postavljena pravokotno na stično ploskev (Sl. 15). V površinski plasti na stičnem mestu pri nastanku obloka nastane talina Ag, v kateri grafit zgori v CO in CO_2, katerih mehurji oblikujejo gobasto površinsko strukturo (Sl. 16). Zvar s tako strukturo je zelo krhek, zato je Ag/C odporen na kontaktni zvar /18/. Zaradi velike stopnje obločne erozije material ni primeren za kontakte z veliko pogostostjo preklapljanja. Na električno zelo nehomogeni površinski strukturi Ag/C je tudi gibljivost obloka majhna, ker se njegovo podnožje zasidra na grafitna vlakna. Da izboljšamo to slabost kontaktne obloge Ag/C, ima za nasprotnega partnerja v paru kontakt iz Cu. V tej vlogi stična površina Cu ni zelo izpostavljena oksidaciji v vročem, ker stično mesto na Cu obdajata CO in CO_2 kot zaščitni plin, izkoriščena pa je velika gibljivost obloka na Cu, ki kompenzira slabo gibljivost na Ag/C.



Slika 17: Struktura Ag/C DF z grafitnimi vlakni in grafitnimi paličicami, usmerjenost grafitnih delcev je vzporedna s kontaktno površino.





Slika 18: Kontaktni zvar na Ag/C DF po pretrganju – na iztrganem delu so vidni odtisi grafitnih paličic, SEM – dolžina markerja 100 μm

Kontaktne obloge Ag/C so v obliki ploščic, ki jih dobijo iz ekstrudirane palice z C-vlakni v smeri vlečenja palice. Palico narežejo v prizme, ki jim na površine izžgejo grafit, prizme pa razrežejo na pol. Ploskev razreza postane stična ploskev s pravokotno postavljenimi grafitnimi vlakni. Ta postopek je dokaj zamuden v primerjavi s tehnologijo izdelave miniprofila z ekstruzijo, vendar pa so zato v strukturi miniprofila grafitna vlakna postavljena vzporedno s kontaktno površino, kar je glede stopnje erozije in možnosti kontaktnega zvara slabša izbira. Za izboljšanje odpornosti na kontaktni zvar so grafitnim vlaknom dodane drobne, do 100 μm dolge palčke grafita /8/ (Sl. 17), ki naredijo strukturo Ag/C dovolj mehansko nehomogeno, da se kontaktni zvar pretrga na palčkah (Sl. 18).

7. Sklep

Vsaka vrsta kontaktnega materiala ima v podanih pogojih nekaj za izbrane pogoje uporabe ustreznih in nekaj neugodnih lastnosti. Univerzalni kontaktni material, ki bi ustrezal vsem pogojem preklapljanja toka, ne obstaja. Izbira kontaktnega materiala za vnaprej določene pogoje upo-

rabe je stvar kompromisa med ugodnostjo njegovih ustreznih lastnosti in sprejemljivostjo neugodnih. Primer kompromisa je nesimetrični kontaktni par Ag/C - Cu za odklopnike, v katerem z enim samim materialom ne odpravimo motečih pomanjkljivosti, ampak slabosti enega materiala kompenziramo z prednostmi drugega v nesimetriji kontakta.

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SINGLE ELECTRON FAULT MODELING IN QCA DEVICES

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Key words: Quantum Cellular Automata, Single Electron Fault

Abstract: Quantum Cellular Automata (QCA) represents an emerging technology at the nanotechnology level. There are various faults which may occur in QCA cells. One of these faults is the Single Electron Fault (SEF) that can happen during manufacturing or operation of QCA circuits. The behavior of single electron fault in QCA devices is not similar to either previously investigated faults or conventional CMOS logic. A detailed simulation based logic level modeling of Single Electron Fault for QCA basic logic devices is represented in this paper.

Modeliranje napake SEF pri delovanju component QCA

Kjučne besede: QCA, napaka SEF

Izvleček: QCA (Quantum Cellular Automata) predstavlja prihajajočo tehnologijo na nanotehnološkem nivoju. Obstaja veliko različnih napak, ki se lahko pojavijo v QCA celicah. Ena izmed teh je napaka enega elektrona (Single Electron Fault-SEF), ki se lahko pripeti med izdelavo ali delovanjem QCA vezij. Obnašanje SEF v QCA vezjih ni enako nobeni preje obravnavani napaki v konvencionalni CMOS logiki. V prispevku obravnavamo natančno logično simulacijo pojava SEF v QCA vezjih.

1. Introduction

The microelectronics industry has improved the integration, the power consumption, and the speed of integrated circuits during past several decades by means of reducing the feature size of transistors. But it seems that even by decreasing the transistor sizes, some problems such as power consumption can't be ignored. Utilizing the QCA technology for implementing logic circuits is one of the approaches which in addition to decreasing the size of logic circuits and increasing the clock frequency of these circuits, reduces the power consumption of these circuits. QCA, which was first introduced by Lent et al. /1/, represents an emerging technology at the nanotechnology level. QCA cells have quantum dots, in which the position of electrons will determine the binary levels of 0 and 1.

Various types of cell misplacement faults may occur during fabrication and manufacturing of QCA devices and circuits. Some of them which have been characterized are *cell displacement*, *cell misalignment*, *cell omission* and *cell rotation* /2-7/.

- A *cell displacement* is a defect in which the defective cell is misplaced from its original direction.
- A *cell misalignment* is a defect in which the direction of the defective cell is not properly aligned.
- A *cell omission* is a defect in which a particular cell is missing compared to the original.
- A *cell rotation* is a defect in which the defective cell is rotated in its location.

There are some other faults, such as missing or extra dots or/and electrons which may occur in QCA devices and circuits /2, 3/. Single event effects (SEE) are an example of such phenomena which can affect QCA devices and circuits. These types of effects can cause electrons to tunnel outside or inside QCA cells, and therefore some remaining QCA cells may contain zero, one, two, three, four or more electrons. This is the main defect caused by SEEs which may occur for QCA devices and circuits. Considering the QCA structure with two electrons in each cell, we can conclude that defected cells may lead to circuit malfunctioning /8/.

The main goal of this paper is to model and characterize the single electron fault in QCA devices. We will investigate the effects of faulty cell in binary wire, inverter chain, inverter gate, and majority gate.

The remainder of this paper is as follows. In Section II, a brief review of QCA is presented. In Section III, the effects of single electron fault on QCA devices are investigated. Finally, Section IV will conclude this paper.

2. QCA Review

In Quantum Cellular Automata (QCA), a cell contains four quantum dots, as schematically shown in Fig. 1. The quantum dots are shown as the open circles which represent the confining electronic potential. Each cell is occupied by two electrons which are schematically shown as the solid dots.

In a cell, the electrons are allowed to jump between the individual quantum dots by the mechanism of quantum mechanical tunneling but they are not allowed to tunnel between cells. The barriers between cells are assumed sufficient to completely suppress intercellular tunneling.

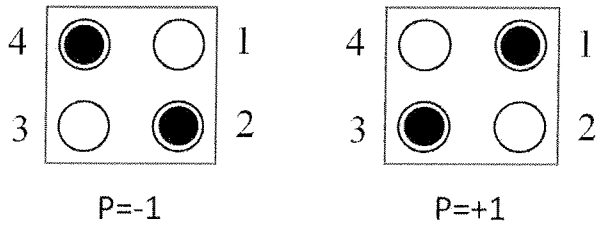

Fig. 1. QCA cell and its ground states

If they are left alone, they will meet the configuration corresponding to the physical ground state of the cell. It is in an obvious manner that the two electrons will tend to occupy different dots because of the Coulombic force associated with bringing them together in close proximity on the same dot.

By these concepts, it's concluded that the ground state of the system will be an equal superposition of the two basic configurations with electrons at opposite corners, as shown in Fig. 1. The positions of the electrons are also shown in this figure.

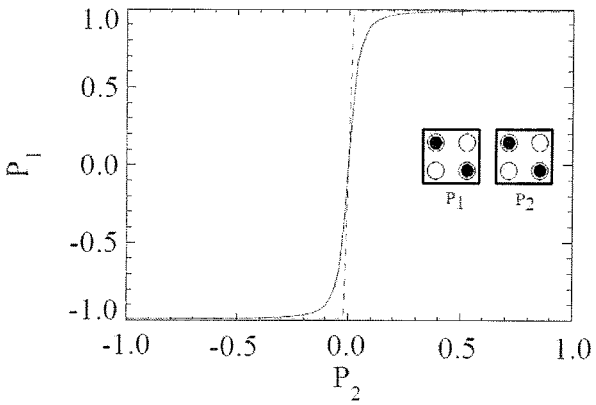

Fig. 2. Coupling of QCA cells

Coupling between the two cells is provided by the Coulomb interaction between electrons in different cells. Fig. 2 shows how one cell is affected by the state of its neighbor /10/. This figure shows the two cells where the polarization of cell 1 (P1) is determined by the polarization of its neighbor (P2). P2 is assumed to be fixed at a given value, corresponding to a specific arrangement of charges in cell 2 and this charge distribution exerts its influence on cell 1, thus determining its polarization. The result which can be drawn here is the strongly non-linear nature of the cell-cell coupling. Cell 1 is almost completely polarized even though cell 2 might only be partially and not completely polarized /9, 10/.

The physical interactions between cells may be used to realize elementary Boolean logic functions. The basic logic gates in QCA are the Majority logic function and the Inverter which are illustrated in Fig. 4(a) and Fig. 3, respectively. The Majority logic function can be realized by only 5 QCA cells /11/.

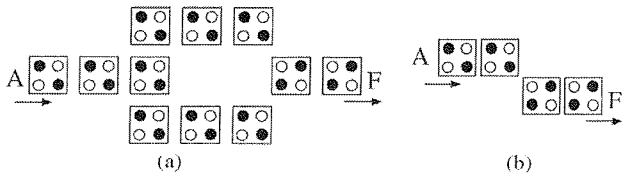

Fig. 3. (a) Redundant inverter gate, (b) Inverter gate

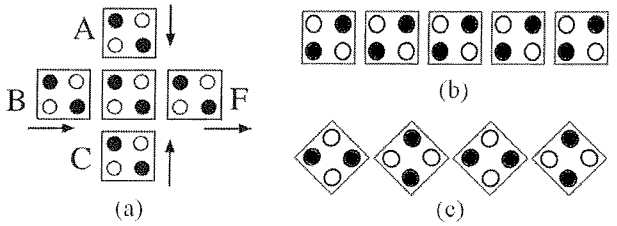

Fig. 4. (a) Majority logic gate, (b) Binary wire, (c) Inverter chain

The logic AND function can be implemented by a Majority logic function by setting one of its inputs permanently to 0 and the logic OR function can be implemented by a Majority logic function by setting one of its inputs permanently to 1.

QCA clocking provides a mechanism for synchronizing information flow through the circuit. It should be considered that the clock also controls the direction of information flow in a QCA circuit. The QCA clock also provides the power required for circuit operation. More precisely, the QCA clock is used to control the tunneling barrier height in cells. When the clock is low, the electrons are trapped in their associated positions and can't tunnel to other dots, therefore latching the cell (Hold phase). This is caused by the intracellular barriers which are held at their maximum height. When the clock signal is high, the cell goes to the null polarization state (Relax phase). This is caused by the intracellular barriers which are held at their minimum height. Between these two cases, the cells are either releasing or switching.

Fig. 5 shows the barrier height in four phases of clock. Each cell in a particular clocking zone is connected to one of the four available phases of the QCA clock shown in Fig. 6. Each cell in the zone is latched and unlatched in synchronization with the changing clock signal and therefore the information is propagated through cells /12-15/.

3. Single Electron Fault Modeling

In this Section, fault modeling will be accomplished for QCA wires, inverter, and majority gates. All cells are assumed to have a length and width of 18 nm and quantum dots are 5 nm in diameter. The center to center distance of two neighbor cells is 20 nm. Thus, the cell size can be defined as 20 nm. As an assumption, a 20 nm cell size was used in /16/ and a 25 nm cell size was used in /5/. Thus, the 20

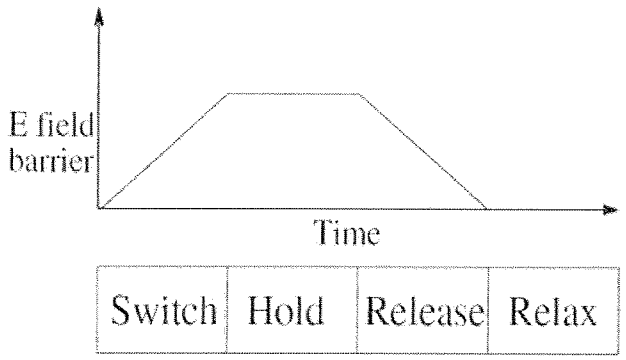

Fig. 5. Barrier height in four phases of clock

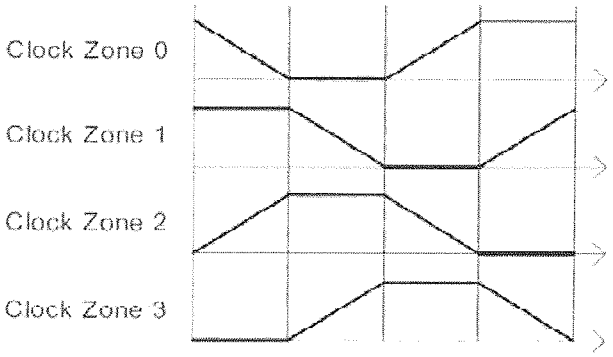

Fig. 6. QCA clock zones

nm assumption is valid for QCA cells. The center to center distance of two neighbor quantum dot in a QCA cell is 9 nm (For example, dot1 and dot2 in Fig. 1). According to previous definitions, other geometric distances are calculated. As an example, considering two neighbor cells, the distance between dot4 in the left cell and dot1 in the right cell is 29 nm and so on. Also it is assumed that each cell is assigned to an individual clock zone and there are no neighbor cells with the same clock zone. Positions of electrons and polarization of cells are obtained from the fact of the least Kink energy. It means that all possible configurations are considered and the Kink energy is calculated for each configuration. Configuration with the least Kink energy is the most stable configuration. The Kink energy can be computed by the following equation.

$$E_{i,j} = \frac{q_i q_j}{4\pi\varepsilon_0\varepsilon_r\left|r_i - r_j\right|} \quad (1)$$

All following simulations i.e. calculating the Kink energy (electron-volt) are accomplished by MATLAB software /17/.

3.1. Fault Modeling for QCA Wires

There are two types of wires in QCA technology, binary wire and inverter chain (Fig. 4(b, c)). We have investigated the single electron fault for these two types of wire and modeled the fault for them. Binary wire will be discussed in this subsection and inverter chain will be discussed in the next.

Two major questions should be answered for a binary wire which contains a faulty cell:

- Considering the faulty cell, where should its single electron go if the previous cell has the polarization of zero or one?
- Considering the faulty cell, which polarization shall be dictated to its next cell?

For the first case, simulation results show that if a cell is faulty and its previous cell has the polarization of zero, the single electron will go to position number 1 and if its previous cell has the polarization of one, the single electron will go to position number 2. The Kink energy is computed for each position and the position with the least Kink energy is considered to be the target position. The kink energy of each position is illustrated in Table 1.

Table 1 Kink energy for positions of electron in a faulty cell in binary wire according to its previous cell polarization

Prev. Cell Pol.	Position 1	Position 2	Position 3	Position 4
Zero	**0.0089309**	0.0092492	0.015224	0.013423
One	0.0092492	**0.0089309**	0.013423	0.015224

For the second case, simulation results show that if a cell is faulty and its electron is in positions of 1, 2, 3 or 4, the next cell will obtain the polarization of one, zero, zero and one correspondingly. The Kink energy is computed for each polarization and the polarization with the least Kink energy is considered to be the target polarization. The kink energy of each polarization is illustrated in Table II. It can be concluded from Table I that positions of 3 and 4 cannot be occupied by single electron in a faulty cell. But in order to have a complete simulation result, they are considered as occupied positions in Table 2.

Table 2 Kink energy for polarization of next cell in binary wire according to the position of electron in faulty cell

Faulty Cell Position	Next Cell Polarization Zero	Next Cell Polarization One
Position 1	0.015224	**0.013423**
Position 2	**0.013423**	0.015224
Position 3	**0.0089309**	0.0092492
Position 4	0.0092492	**0.0089309**

Fig. 7 illustrates the faulty cell effect on a binary wire. As illustrated in Fig. 7(a), if the left side cell has the logic value of zero, the faulty cell will have its electron in position 1 and the right side cell will obtain the logic value of one and as illustrated in the Fig. 7(b), if the left side cell has the logic value of one, the faulty cell will have its electron in position 2 and the right side cell will obtain the logic value of zero. According to simulation results, if a single electron fault occurs in a binary wire, the logic value of that wire will be inverted.

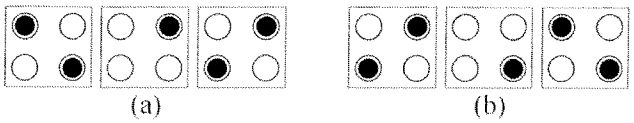

Fig. 7. Faulty cell effect on binary wire

3.2. Fault Modeling for QCA Inverter Gate

In this section we will discuss the inverter gate or inverter chain and also redundant inverter gate of Fig. 3(a) which has two inverters in parallel.

Two previous questions for an inverter chain containing a faulty cell should be addressed.

For the first case, simulation results show that if a cell is faulty and its previous cell has the polarization of zero, the single electron will go to position number 2 and if its previous cell has the polarization of one, again the single electron will go to position number 2. The Kink energy is computed for each position and the position with the least Kink energy is figured out to be the target position. The kink energy of each position is illustrated in Table 3.

Table 3 Kink energy for positions of electron in a faulty cell in inverter chain according to its previous cell polarization

Prev. Cell Pol.	Position 1	Position 2	Position 3	Position 4
Zero	0.0080519	**0.0066624**	0.0080519	0.011112
One	0.0075388	**0.0063317**	0.0075388	0.0097721

For the second case, simulation results show that if a cell is faulty and its electron is in positions of 1, 2, 3 or 4, the next cell will obtain the polarization of one. It means that the output is stuck at one. The Kink energy is computed for each polarization and the polarization with the least Kink energy is figured out to be the target polarization. The kink energy of each polarization is illustrated in Table 4.

Table 4 Kink energy for polarization of next cell in inverter chain according to the position of electron in faulty cell

Faulty Cell Position	Next Cell Polarization Zero	Next Cell Polarization One
Position 1	0.0080519	**0.0075388**
Position 2	0.011112	**0.0097721**
Position 3	0.0080519	**0.0075388**
Position 4	0.0066624	**0.0063317**

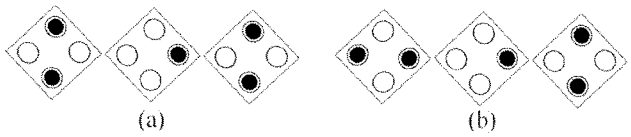

Fig. 8. Faulty cell effect on inverter chain

Fig. 8 illustrates the faulty cell effect on inverter chain. As illustrated in Fig. 8 (a), if the left side cell has the logic value of one, the faulty cell will have its electron in position 2 and the right side cell will obtain the logic value of one and as illustrated in Fig. 8 (b), if the left side cell has the logic value of zero, the faulty cell will have its electron in position 2 and the right side cell will obtain the logic value of one. According to simulation results, if a single electron fault occurs in an inverter chain, the logic value of that wire will be stuck at one.

Considering the redundant inverter gate, the fault may occur on 3 cells which are two right most cells on up and down input wires and a cell which is at the diagonal neighborhood of these two cells. Occurrence of the fault on other cells of redundant inverter gate may be treated as binary wire fault. Also two previously mentioned questions for the redundant inverter gate should be answered.

Table 5 Kink energy for positions of electron in a faulty cell in redundant inverter gate according to its previous cells polarization

Prev. Cell Pol.	Position 1	Position 2	Position 3	Position 4
Zero	0.014384	**0.014201**	0.017824	0.018651
One	**0.014201**	0.014384	0.018651	0.017824

First, the single diagonal neighbor cell will be investigated. For the first case, simulation results show that if this cell is faulty and its previous up and down cells have the polarization of zero, the single electron will go to position number 2 and if its previous cells have the polarization of one, the single electron will go to position number 1. The Kink energy is computed for each position and the position with the least Kink energy is figured out to be the target position. The kink energy of each position is illustrated in Table 5. Second case of fault modeling for this cell is similar to binary wire.

Fig. 9 illustrates the output faulty cell effect on redundant inverter gate. Simulation results show that the redundant inverter gate will act as a wire in presence of single electron fault in the output cell, i.e. the single diagonal neighbor cell.

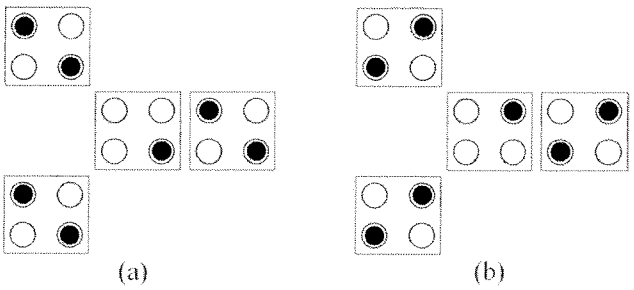

Fig. 9. Output faulty cell effect on redundant inverter gate

There are also two cases for two right most cells on up and down wires. The first case is like binary wire but for the sec-

ond case, simulation results show that if the cell in the up position is faulty, the next cell, i.e. the diagonal neighbor cell, will be stuck at zero and if the cell in the down position is faulty, the next cell, i.e. the diagonal neighbor cell, will be stuck at one. The Kink energy is computed for each polarization and the polarization with the least Kink energy is figured out to be the target polarization. The kink energy of each polarization is illustrated in Table 6. Fig. 10 illustrates the up input faulty cell effect on redundant inverter gate.

Table 6 Kink energy for polarization of next cell in redundant inverter gate according to the faulty cell in up or down input position

Input Polarization and Faulty Input	**Next Cell Polarization Zero**	**Next Cell Polarization One**
Zero and Up	**0.02313**	0.023643
One and Up	**0.027216**	0.027547
Zero and Down	0.027547	**0.027216**
One and Down	0.023643	**0.02313**

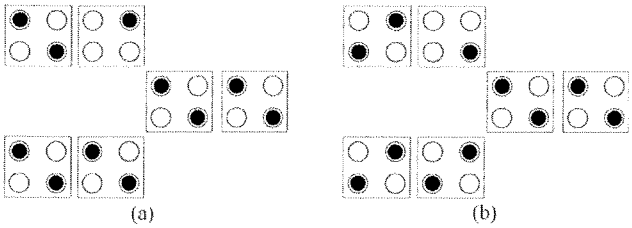

Fig. 10. Up input faulty cell effect on redundant inverter gate

3.3. Fault Modeling for QCA Majority Gate

To model the single electron fault in majority gate, we have exhaustively simulated this gate and the fault effect of each of its four cells, i.e. input A, input B, input C, and central cell was investigated for every input vector. If the fault occurs on output cell, it can be treated as a wire between central cell and output cell.

As an example of simulation, the computed Kink energy and the position of electron in faulty central cell of majority gate are listed in Table 7. Again the least Kink energy will introduce the target position. All faulty states in presence of the faulty central cell are illustrated in Fig. 11.

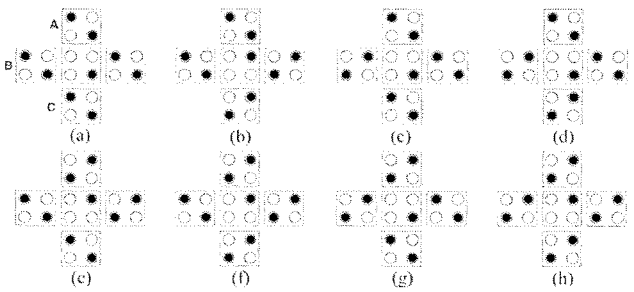

Fig. 11. Faulty states of majority gate in presence of the faulty central cell

Table 7 Kink energy for positions of electron in faulty central cell of majority gate

Input ABC	Position 1	Position 2	Position 3	Position 4
000	0.033086	**0.031922**	0.039379	0.036096
001	**0.033404**	0.033722	0.037578	0.035777
010	0.033404	**0.031603**	0.037578	0.037896
011	0.033722	**0.033404**	0.035777	0.037578
100	**0.031285**	0.031603	0.039697	0.037896
101	**0.031603**	0.033404	0.037896	0.037578
110	0.031603	**0.031285**	0.037896	0.039697
111	**0.031922**	0.033086	0.036096	0.039379

Output Simulation results are shown in Table 8. Like other gates, here we computed the Kink energy for finding the output of the majority gate.

Table 8 Desired output of the majority gate and computed output in presence of single electron fault

Input ABC	Output for Faulty A	Output for Faulty B	Output for Faulty C	Output for Faulty Cent.	Desired Output
000	0	0	0	0	0
001	1	1	0	1	0
010	1	0	1	0	0
011	1	0	0	0	1
100	0	1	1	1	0
101	0	1	0	1	1
110	0	0	1	0	1
111	1	1	1	1	1

Looking more precisely at the simulation results, we can conclude that if a fault occurs on an input, the output will change its functionality to majority of other inputs and inverse of faulty input. Occurrence of the fault on central input is equivalent to occurrence of the fault on B input.

4. Conclusion

A detailed modeling and characterization of single electron fault for QCA basic logic devices has been represented in this paper. As stated before, the behavior of single electron fault in QCA devices is not similar to either previously investigated faults or conventional CMOS logic. For example, stuck at zero or stuck at one fault model in redundant inverter gate is based on the input on which the fault occurs.

Our results show that if a single electron fault occurs in a binary wire, the logic value of that wire will be inverted. If the mentioned fault occurs in an inverter chain or a Not gate, the output will be stuck at one. If this fault occurs on the output of redundant inverter gate, the function of this gate will be inverted and it acts as a wire. Occurrence of the single electron fault on the right most cells of up and down wires of redundant inverter gate will lead to the output getting stuck at zero and one respectively. Single electron fault on the central cell of majority gate will change the

majority output to majority of vertical inputs and inversed horizontal input. Occurrence of this fault on each input of majority gate will change the output to be the majority of other inputs and the inverse of this faulty input.

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A FLASH INTERPOLATOR ASIC WITH BUILD-IN AMPLITUDE MEASUREMENT CIRCUIT

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Key words: Interpolation, amplitude measurement, orthogonal signals, flash interpolator, automatic gain control, encoder.

Abstract: A flash interpolation circuit converts a pair of periodic and orthogonal sine-signals into a stream of periodic - phase shifted sinusoidal signals, the amplitudes of which can be combined to produce useful information about the peak amplitude of the input sine-signals, independently of the signal's frequency. An interpolation factor of 4 is shown to be sufficient for measuring amplitudes with an accuracy of 5.8 %.

The interpolator architecture, combined with an amplitude measuring system, has been designed, integrated as a part of the interpolator ASIC, evaluated and analyzed. The ASIC is designed and processed in 0.35 ěm CMOS technology.

Bliskovni interpolator z vgrajenim merilnikom amplitude

Kjučne besede: interpolator, merjenje amplitude, pravokotni signali, bliskovni interpolator, avtomatična kontrola ojačanja, kodirnik.

Izvleček: V članku je opisano bliskovno interpolacijsko vezje za pretvorbo analognih sinusnih in ortogonlnih signalov v množico prav tako sinusnih - fazno zamaklnjenih signalov, ki predstavljajo osnovno informacijo za nov algoritem merjenja amplitude. Merjenje je neodvino od frekvence signalov, interpolacijsko število 4 pa zadošča za preciznost merjenja 5.8%. Algoritem je podan in preizkušen v interpolacijskem vezju, ki je bilo procesirano v 0,35um tehnologiji CMOS.

1. Introduction

A typical application in the motion control field is in magnetic or optical linear and rotary encoders, the major part of which comprises integrated electronics. In general, the electronics comprise an opto-sensing area or hall sensors structure, analog front-end and signal conditioning, and a fast interpolator and digital signal processing unit. The front-end performs sensors supply, sensors excitation and signal magnification functions. The operation speed of the encoders, based on magnetic sensors, is usually much slower than one based on light modulation. This holds true mainly for magnetic rotary encoders, the speed of the magnetic linear encoders being faster, but usually never exceeding the speed of optical encoders /1/, /4/, /16/, /21/, /24/, /31/ and /35/.

An analog signal generated from a sensors array is amplified and digitized to provide incremental orthogonal digital signals named track A and track B. Before digitizing the analog signals they can be further interpolated to achieve better measurement resolution /2-3/, /6-7/, /11/, /13/, /18/, /22/, /25/, /28/, /29/ and /35/.The same is true for an absolute type encoder which can perform absolute position detection /9/, /14/, /20/, /32/.

In the case where more than 7-bit resolution is required, analog signals conditioning need to be implemented. This includes equalization of the sine and cosine signal amplitudes, their offset equalization and phase difference adjustment to 90 degrees. The most common practice is adjusting analogue front-end parameters via a serial interface or reprogramming them with access to internal EEPROM /12/. Automatic offset measurement and cancellation are relatively simple /17/, the phase measurement and correction and the amplitude regulation and measurement being more complicated /5-6/, /11/, /25/, /28/, /38/ and /42/. A magnitude and phase estimation algorithm has been published /5/ for a signal with time-varying frequency. The method is slow and requires modest computations.

Squaring algorithm using analog multipliers is a well known method for obtaining/extracting DC information from sine-cosine signals /36/. The main disadvantages are the limited linear input voltage range and its temperature behavior. Also the flash interpolator circuits that comprise the signal generating circuit, of which the out-of-phase signals are generated by gain stages having different magnifications, are much slower /37/. The appropriate comparators circuit /37/ compares signals at different common mode levels, which may additionally cause different delays and offsets. The Cordic-based Loeffler discrete cosine transform (DCT) architecture is presented in /41/. It requires high level of digital complexity and is very suitable for low-power and high-quality codecs.

Anything that can affect the accuracy of the final application is related to the overall decoder system's components /9/, /19-20/, /40/, /43/, /44/ and to the applied algorithms /27/, /28/. Therefore, the question of calibration is system related.

The aim of this work is to present a less precise, but cost-effective and robust amplitude measurement algorithm, based on a flash interpolating circuit, suitable for VLSI integration on "system on chip SoC". Amplitude measurement is a basic pre-processing step for automatic signal-amplitude correction and for the AGC function. The major advantage of the proposed method is that there is no need for an extra system clock. Due to the lower silicon area consumption, low power consumption and signal frequency independent measurement method, the present solution is suitable for use in all integrated automatic signal conditioning systems.

This paper is organized as follows. The typical application - encoder - that uses AMM, and the design considerations are described in Section 2. A detailed description of the proposed flash interpolation method using sine wave input signals with an interpolator-inherent principle of amplitude measurement are described in the third and in fourth Section. The results of measurements are presented in Section 5.

2. Encoders - Basic Principles

An optical encoder translates an angular or linear position into an electrical signal. It is typically composed of a light source (LED), a main scale with a built-in optical grating with measuring period MP, and an optical scanner that is composed of an opto-sensor array and a reading scale with a built-in optical grating with a reading period, RP. The scanning head is usually composed of reverse polarized photodiodes that produce the quadrature signals, together with an additional photodiode (DF) that generates the index signal that is used for absolute position encoding.

In short, as the scanner moves along the main scale the amount of light from the light source is modulated. The electrical signal that is produced by the opto-sensor in the optical array is also modulated.

As we have seen, the encoder produces two ninety-degree shifted (quadrature) signals A+, A- and B+, B- (Figure 1b). The signals in Figure 1b are periodic; this periodicity corresponds to the movement of the scanner head with constant velocity along the main scale One period of the signal corresponds to a movement of the scanner head equal to the grating period (MP, RP). In general, the signals are not periodic in time, but are periodic in relation to the displacement along the main scale. The signals A+, A-, and B+, B- in Figure 1b are also not pure sine-cosine, but, in reality, are distorted and contain harmonic components. The incoming signals are also imbalanced in phase, offset and amplitude. The encoder system therefore requires signal conditioning prior to interpolation.

The two pairs of signals from optical array are usually transformed into voltages with a fully-differential voltage amplifier to remove the large DC component and suppress even harmonics to produce the signals to be further interpolated. The voltage amplifier should have a low output impedance to drive the resistive interpolation network. The two quadrature signals enable the position of the scanner head to be detected at all times, just by measuring the values of these two signals. To achieve high interpolation accuracy, the amplitude of the incoming sine signals should be regulated to the acceptable maximum level.

The signals can be digitized directly by an analog comparator. The two resulting digital signals (signal F4 and F8 in Figure 1b) will still be in quadrature and all information be in the low-high and high-low transitions of the signals. There are four such transitions per grating period (MP, RP). Therefore the intrinsic resolution of the encoder is one fourth of the grating period. Alternatively, interpolation can be used to increase the resolution.

An incremental type encoder outputs a pair of digital square waves Ao and Bo (Figure 1b) that are 90 degrees apart and convey, for instance, the change in the shaft's position, and direction of rotation. An absolute type encoder, on the other hand, detects an absolute position. Optical or magnetic encoders are widely used transducers that have applications in robotics, manufacturing, motors, and the hi-tech industry /1/, /14/, /23/, /24/ and /26/. All these may have incremental or absolute encoders.

3. Flash Interpolator - Theory and Fundamentals

The basic architecture of the proposed flash interpolation converter consists of four matched resistive chains, connected in a symmetric bridge (Figure 1a). The resistivity of each chain is R_v The differential channel signals CH-A and CH-B, ordinary and inverted (A+, A-, B+, B-), are connected to opposite sites of the bridge, the voltages of which are of equal amplitude, but phase shifted by 0 and 180 degrees (CH-A) and by 90 and -90 degrees (CH-B) as shown in Figure 1b. An interpolation factor of *IP=4* is chosen as an example. Thus interpolator circuit in Figure 1a consists of four resistive chains, each having *IP* resistors (r1 to r4 with total resistivity of $R_v = \sum_1^4 r_i$). It also consists of twice as many voltage comparators, C1 to C8, connected to the taps of the bridge. Each comparator always compares tap voltages on the same common mode (CM) level, as shown from simulations in Figure 2 (s1, s2, to s16). Each comparator compares two voltages, shifted in phase by exactly 180 degrees. Although all comparators operate at the same CM level, they differ in performance, which causes INL and DNL errors of the output code (variations of the separation time). Interpolator linearity is also limited by the resistors' matching requirements. Resistance values in the chain are calculated according to the shape of the incoming orthogonal and differential signals connected to the bridge corners (A+, A-, B+, and B-). Angle resolution *K* is defined by interpolation resolution set by *IP* within a single chain interval of 90 angle degrees. *K* is a constant:

$$K = \frac{90}{IP}, \text{ where } IP \text{ is defined in (6).} \quad (1)$$

From the present example of orthogonal sine signals, calculation of the resistivity of the chain resistors in a resistor bridge is:

- signal-angle calculation on individual resistor tap:

$$\alpha_I = I \cdot K; \quad I = 1, 2, \ldots, IP, \quad (2)$$

where maximal angle is α_{max} = 90 deg, and resistors are:

$$R_I(\alpha_I) = R_V \cdot \frac{\cos(\alpha_I)}{\sin(\alpha_I)+\cos(\alpha_I)}; \quad 45\text{deg} \le \alpha_I \le 90\text{deg} \quad (3)$$

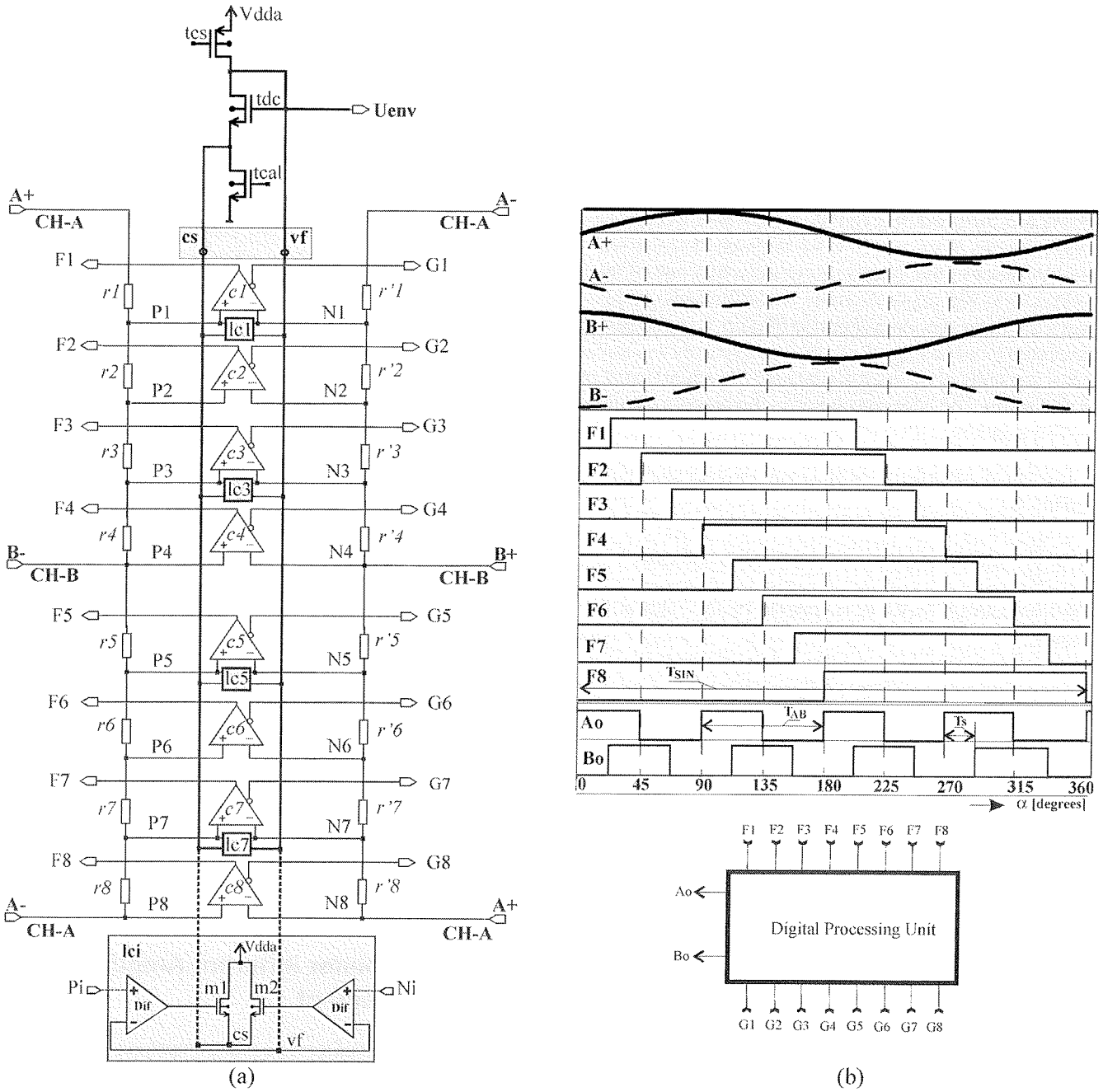

Fig.1. The linear optical encoder system – principle of operation. The interpolation factor of four is taken as an example, the realization of which is shown in (a). Signals A+, A- and B+, B- are the interpolator's input signals. The interpolator's output signals Fi and Gi are differential-digital signals, generated by the flash A/D converter/ interpolator. An XOR in the Digital Processing Unit (b) operates on them to produce a quadrature output signal Ao and Bo. Signals generated at the chain taps P1, P2, P3, P5, P6, P7 and N1, N2, N3, N5, N6, N7 are phase shifted. The all-followers common circuit (at the top (a) consists of the single load device tcal, *the level-shift circuit, constructed from diode device* tdc *and the biasing device* tcs. *Topology at the bottom (a) shows a distributed amplitude measurement structure within* ***lc1***, ***lc3***, ***lc5*** *and* ***lc7***. Vdda *is positive supply voltage,* vf *is feedback connection and* cs *a common source terminal for all distributed follower pairs, each consisting of two differential amplifiers* Dif *and a follower device* m1 *and* m2.

T_{SIN} is the sine-wave period and corresponds to the grating period RP; T_{AB} is the processor tracks output period and T_S the separation time between the two neighboring edges of tracks Ao and Bo (b).

$$R_I(\alpha_I) = R_V \cdot \frac{\sin(\alpha_I)}{\sin(\alpha_I)+\cos(\alpha_I)};\ 0\,\mathrm{deg} < \alpha_I < 45\,\mathrm{deg} \qquad (4)$$

$R_I(\alpha_I)$ is the sum of the resistivity of the resistors from *i=1* to *i=I*. Resistivity of a single resistor in a chain $R(r_i)$ is calculated by subtracting all resistors $(R(r_1)$ to $R(r_i\text{-}1))$ from the previously calculated sum.

Resistors are symmetrically positioned from the center of each resistive chain; thus the resistor values are mirrored within a range from 45 degrees to 90 degrees, and all four chains are matched. It is therefore sufficient to calculate resistors in the range from 0 to 45 degrees. It is also sufficient to process the incoming signals within half of their periods (0 to 180 angle degrees), since the same comparators act in the second half-period (Figure 1). As shown in the present example for *IP=4*, the resistivity of *r1* is equal to the resistivity of *r4,* the resistivity of *r2* is equal to that of *r3* and so on. The angle resolution in the present example is 22.5 degrees.

In the case of saw-shape incoming quadrature signals, the relation is:

$$R_I = \frac{R_V}{IP} \text{ and all resistors are of the same resistivity.} \qquad (5)$$

The interpolation factor *IP* is defined by the ratio of two periods:

$$IP = \frac{T_{SIN}}{T_{A,B}} \qquad (6)$$

T_{SIN} is the period of the incoming sine signals, $T_{A,B}$ is the period of the outgoing digital-orthogonal signals **Ao** and **Bo**, as shown in Figure 1b, where the track signals **Ao** and **Bo** are generated from the comparators' output signals **Fi** and **Gi** (Figure 1a).

Lagging or leading of the track signals depends on the current positions of the sine wave signals or, in other words, on the direction of movement of the measuring-head. Processor input signals contribute equal delay to the generated tracks, so it is important to achieve constant separation time between digital output edges over the whole input sine wave period. This is very important at high moving speed.

3.1 Identifying the Non-ideality Sources

Although all comparators operate at the same CM level, they differ in performance, which causes INL and DNL errors of the output code (variations of the separation time). It is important to note that the comparator's input signals from the resistor taps have different slopes. The offset of the comparators would influences the switching point by the ratio between peak sine signal amplitude and the comparator offset voltage. This influence can be expressed as an angle difference of $d\alpha=\sin^{-1}(Voff)$ (we assume that the peak sine amplitude is 1V). The most critical non-ideality is the comparator offset difference (mismatch). Interpolator linearity is also limited by the resistors' matching requirements. The resistor mismatch directly affects the comparator switching. Furthermore, the influence of different non-idealities on the system performance becomes important when a higher order interpolator is an issue (resistors mismatch directly influences tracks separation time). It is therefore important to follow the matching parameters' information supported by an IC manufacturer and design resistors wide accordingly. Mismatch of the resistors' contacts and taps' resistance are in some cases more important. Therefore, the realization of the current contacts differs from that used only as a voltage tap. Moreover, all the resistors' related layout rules, like dummy material, should also be considered.

The influence of the comparator's delay on the interpolator performance depends on the scanner moving speed. The delay degrades the separation time (and the real head position) only minimally at lower speed, while the effect increases with increasing moving speed. The comparator's delay limits the upper measuring speed. Just take an example from section 4: the realized interpolation factor of 100 gives 400 transitions per sine signal period (IP=100). Using a grating period of 20 µm, a sine signal frequency of 100 kHz is achieved by the scanner moving speed of 2m/second. The rate of the track signals Ao and Bo are 100 times faster and is 10 MHz. The nominal separation time between the two neighboring edges of Ao and Bo is therefore 25 ns. At such a high speed, the comparator's delay should not exceed 6 ns (to maintain a minimal separation time of 50% from the nominal one). It is also important to note that the comparator's delay could be much larger; the difference between neighboring comparators delay should not exceed 6 ns. The position error will be accumulated in this case.

Temperature dependence and reliability of the product are the most serious issues in high accuracy motion control.

4. Interpolator Inherent Amplitude Mesurement

The proposed circuit for measuring amplitude is combined into an interpolator architecture shown in Figure 1a. This results in a compact, area efficient topology that contributes to better dynamics and finally to better speed performance. The interpolator is therefore a basic structure, upgraded by an envelope detector, the output of which tracks the maxima of relevant signals generated along the resistor bridge. The AMM upgrade consists of distributed voltage followers Ic1, Ic3, Ic5 and Ic7, combined to odd comparators *c1*, *c3*, *c5* and *c7* (Figure 1a). As described later, only odd comparators handle phase shifted signals having maxima at:

$$P_i, N_i \equiv i \cdot K, \quad i=1, 3, 5, \ldots 2(IP-1) \tag{7}$$

Each follower consists of a differential stage (Dif) followed by a source follower device m1 or m2, the sources of which are connected to a single - active load device *tcal* at the common node *cs* (at the top in Figure 1a). The active load structure is common to all followers in the AMM circuit. The drain voltage of the *tcal* device follows voltages on the inputs of the follower devices m1 and m2 from all comparators/followers. Follower feedback voltage, vf, is shifted up by the diode voltage of the *tdc* device, which forces the source voltages of m1 and m2 to be below the gate voltages of m1 and m2 for a diode voltage of the *tdc* device. This action is required for differential amplifiers *Dif* to compare input signals to the common feedback signal *cs*, where all input signals have the correct common-mode level. The common source potential, therefore, follows that input voltage on the follower devices m1 and m2, which have the maximum amplitude. Consequently, a higher source potential on node *cs* forces the devices m1 and m2 with lower input amplitudes to the off state. The current source *tcs* provides proper biasing for the diode device *tdc*. Output signal Uenv tracks the input signal on resistor taps that is currently of the highest amplitude. The potential on node *vf* is therefore the envelope (maxima) of all compared signals and carries useful information about the peak amplitude of incoming signals from channels CH-A and CH-B.

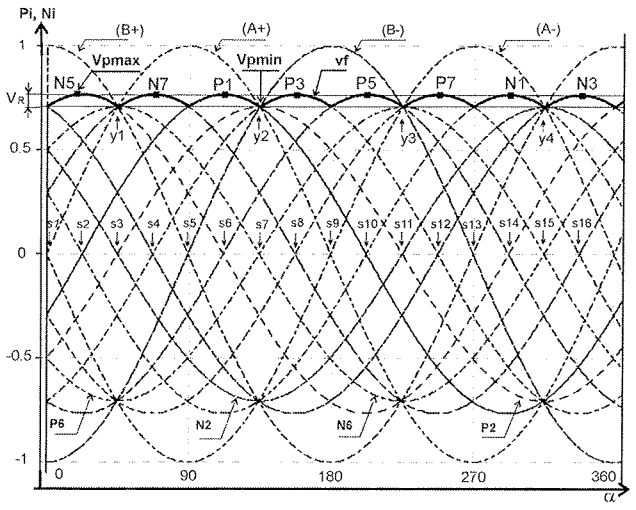

Fig. 2. Simulated waveforms of the phase shifted signals Pi and Ni on the symmetrical resistive bridge of an interpolator from Figure 1a. The shadow area V_R is an envelope range (envelope ripple), showing also local minima and maxima. Signals P2, N2, P6, and N6, as well as input signals from CH-A (A+, A-) and from CH-B (B+, B-), do not contribute to minimization of the envelope ripple. All signals have the same period and offset as input signals, but differ in amplitude and phase shift.

The tracking accuracy depends on differential amplifier gain and offset voltage. All signals within one segment of the bridge cross at the same points (y1, y2, y3 and y4) which are multiples of 45 degrees. The ripple extremes exist at multiples of α=45/2 degree:

$$\alpha = K = \frac{360}{4 \cdot IP} = 22.5 \deg. \tag{8}$$

from which it follows that *IP=4* is sufficient to realize amplitude measuring (AMM) and automatic-gain control (AGC) functions. The extremes of the Uenv envelope are:

- global minima that are at even multiples of α, where α is 22.5 angle degrees, and are defined as:

$$Vp\min = Vp \cdot \left\{ \left[\sin(\alpha) + \frac{\cos(\alpha) - \sin(\alpha)}{\cos(\alpha) + \sin(\alpha)} \cdot \cos(\alpha) \right] \cdot \sin(90 - \alpha) \right\} = Vp \cdot 0.707106 \tag{9}$$

Vp is the peak amplitude of the input sine signal.

- maxima that are at odd multiples of α and are defined as:

$$Vp\max = Vp \cdot \left[\sin(\alpha) + \frac{\cos(\alpha) - \sin(\alpha)}{\cos(\alpha) + \sin(\alpha)} \cdot \cos(\alpha) \right] = Vp \cdot 0.76536 \tag{10}$$

As the interpolation factor *IP* increases, the signal amplitudes on the resistor bridge taps closer to input signals increase, while the ripple extremes remain at multiple of the 22,5 degrees (Figure 2). An interpolation factor IP of 4 is therefore optimum for the proposed algorithm. Because the minima are global, a ripple of 5,825% of the peak input amplitude *Vp* is a minimum and is defined as:

$$ripple[\%] = Vrip[\%] = \frac{Vp\max - Vp\min}{Vp} \cdot 100 \tag{11}$$

The *ripple* function $V_{rip}(a)$ can also be described using a general *modulo* function, valid over the whole signal period:

$$Vrip(\alpha) = Vp \cdot \left[\begin{array}{l} \sin\left(\alpha\left(\bmod\frac{\pi}{4}\right)\right) \cdot \left(1 - \sin\frac{\pi}{4}\right) + \\ + \cos\left(\alpha\left(\bmod\frac{\pi}{4}\right)\right) \cdot \sin\frac{\pi}{4} \end{array} \right], \tag{12}$$

and the extreme functions are:

$$Vrip\_\max(n) = Vrip\left((2n+1) \cdot \frac{\pi}{8}\right) \cdot \text{ and is: } 0.76536 \,.\, V_p, \tag{13}$$

where maxima are positioned at all odd multiples of $\pi/8$;

$$Vrip\_\min(n) = Vrip\left(2n \cdot \frac{\pi}{8}\right) \text{ - and is: } 0.707106 \,.\, V_p, \tag{14}$$

minima are positioned at all even multiples of $\pi/8$, where *n* ranges from ....,-2, -1, 0, 1, 2...., and where $\pi/8$ radians is equal to 22.5 angle degrees. Any other search for maxima in terms of "searching for minima above global minima" is much more complex and requires much higher

speed Ic$_i$ circuits, the tracks of which have to be controlled by extra - fast comparators.

4.1 Identifying the Non-ideality Sources

Resistor *r1* mismatch of 1% and 2% (Figure 1a) is taken as an example for analysis shown in Figure 3. The larger *r1* resistivity then required slightly reduces the maximum at the corresponding angle position, as is shown in detail on top of the picture (curves *r1_1%_mis* and *r1_2%_mis*). It is evident that the comparator offset cannot affect the sine signals on resistors' taps. On the other hand, the offset voltage of the differential stages Dif drastically affects the envelope extremes. As the Dif is in a source follower configuration, its offset contributes directly with a unity gain to the envelope change as is shown, as an example, for 10mV offset (curve *Dif_10mV_offset*) and for -10mV offset (curve *Dif_-10mV_offset*). It is also clear that each Dif stage contributes only at an appropriate angle position area (we put offset voltage to Dif stage in the Ic1 block only - Figure 1a).

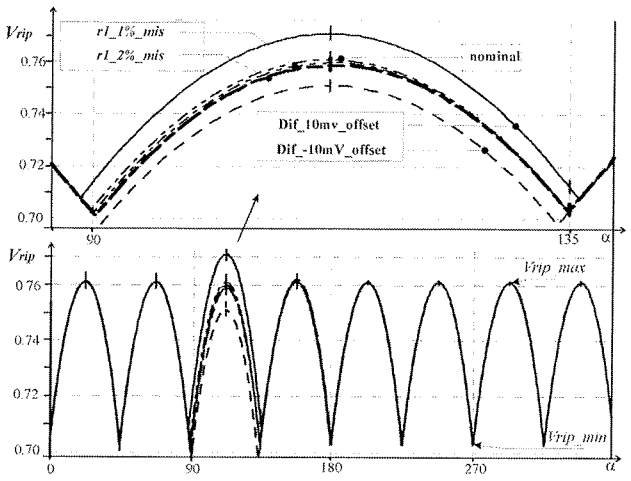

Fig. 3. Simulated envelope voltage, Vrip, *on Uenv output node (curve P1 is shown in detail).*

5. Results and Discussion

The proposed technique was realized in an encoder ASIC to verify the accuracy of the AMM technique. The realization is an integrated incremental ASIC (Figure 4) which operates at an input sine wave signal frequency from DC to 100kHz in a temperature range from -40°C to 125°C and at a supply voltage of 4.5V±0.5V. The processed ASIC is fully operational up to 200 kHz under typical conditions. The opto-sensor array is a separate integrated circuit comprising the reverse biased Si photodiodes and the signal is in the form of an electrical current. The light intensity of the LED device is controlled by part of the generated error signal in the AGC block. The measured performances of the AMM itself are shown in Table I. Measured ripple is filtered out at higher frequencies (pad-probe: 300Ω/8pF-1MΩ/90pF) and therefore cannot be reported without filtering action (Table I). The measurement at the fastest operation is shown in Figure 5.

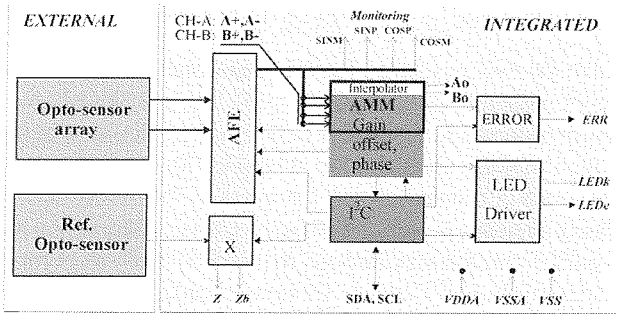

*Fig. 4. Interpolator ASIC combines a signal conditioning feature, where externally generated input sine signals are applied to the analog-front-end, AFE, and where the AMM module (**am**plitude **m**easurement as part of the interpolator) automatically controls the amplitudes of the incoming orthogonal sine signals to the interpolator circuit.*

Table I: Measured AMM output signals.

Sine/Cosine Frequency [kHz]	Sin/Cosine peak [mV]	Measured Uenv additionally loaded by the probe – 1M/90PF	
		V_{min} [mV]	V_{max} [mV]
0.1	500	352	383
1	100	74	80
1	500	352	383
20	1000	709	755
100	1000	740	740

It is clear that, in practice, the signal conditioning is not running when the scanner is moving fast, simply because the measurement, and therefore the interpolation, should not be disturbed by the automatic AMM and AGC. The amplitude measurement and regulation are running within a certain frequency window and that range has to be monitored simultaneously. Result 5,8% represents an optimum and the minimum for the flash interpolator we proposed. Measurement accuracy of 5,8% for the AGC function is sufficient for most industrial applications.

6. Conclusion

The aim of this work was to find a cost-effective and area-effective method of generating peak amplitude information from sine wave signals. The major part of the amplitude measurement and envelope extraction is already inherent in the presented flash interpolator and only minor additional electronics has been added. The target of this work was to improve the quality of the quadrature signals to enable higher interpolation factors and higher encoder resolution.

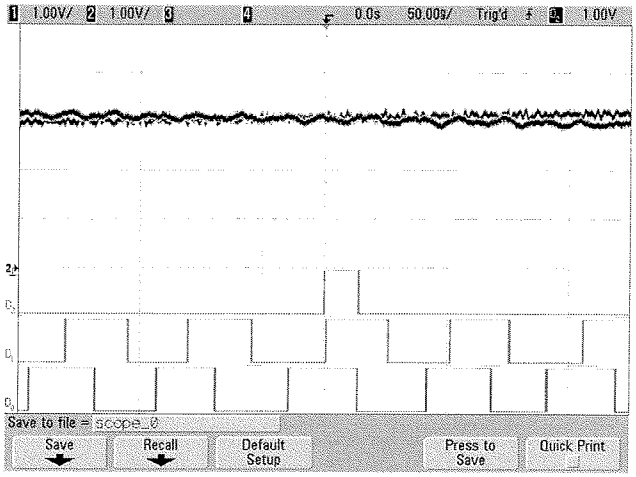

Fig. 5. Measurement of the interpolator at IP=100 and at input sine signals frequency of 100 kHz. Index is shown in D2, track Ao in D1 and the track Bo in D0.

The amplitude information, when evaluated, shows the following: if the AC part of the information is larger than the expected 5.8 % ripple (seen at lower head moving speed only), it results from the sine-signal-pair to cosine-signal-pair amplitude mismatch. To implement precise amplitude correction, matching of the quadrature sine signals prior to AGC is necessary. Moreover, appropriate comparator circuits that weight the measured signal amplitudes to predefined values need to be designed, having the hysteresis ratiometric to generated signal amplitude to overcome undesired ripple at lower signal frequencies. It is also important to regulate sensors supply and light intensity parameters prior to AGC (based on AMM measurement) to maintain the design requirements for the dynamic range.

The proposed solution for AMM is much more robust than that using a square circuit to generate DC voltage out of sine and cosine signals. The amplitude measurement described in this paper is an inherently linear process that generates envelope by using the same signal processing path as the interpolator itself. Interpolator monotonicity is guaranteed by the proposed architecture.

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REALIZATION OF 4th ORDER RECURSIVE DIGITAL FILTER WITH PLC CONTROLLER

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Key words: digital signal processing, recursive digital filters, IIR filter, eliptic filter, PLC controller realization

Abstract: This paper describes the design and realization of the third and fourth order recursive digital filter (IIR digital filter) using PLC controller. The purpose of the filter is elimination of unwanted signals which occur during processing of analog signals in the industrial process automation with PLC controllers. The Siemens S7-315-2DP PLC controller is used in practical realization. In this application, we chose the eliptical filter with a cut-off frequency of 3 Hz and a sampling frequency of 50 Hz. With format long of the filter coefficients values we obtain the expected stop band attenuation of 40 dB as it is designed with MATLAB software. The values of impulse response are applied to compare PLC controller realization of digital filter and simulated structure with MATLAB.

The results for the third and fourth order digital filter with format long filter coefficients and with shortened mode format of filter coefficients entry are summarised in tables.

A magnitude frequency response of the 4th order digital filter for a cascaded form is displayed as figures, general and detailed for passband. Comparison of errors in impulse response for direct and cascade structure is demonstrated in this article. Finally, in comparison to the third order digital filter where the attenuation of 40 dB is obtained at 7 Hz, with the fourth order filter structure, the attenuation of 40 dB reaches at 4 Hz.

Izvedba rekurzivnega digitalnega filtra 4. stopnje s PLC krmilnikom

Kjučne besede: digitalna obdelava signalov, rekurzivni digitalni filtri, eliptični filtri, izvedba s PLC krmilnikom

Izvleček: V prispevku je opisan postopek načrtovanja in izvedbe rekurzivnih digitalnih filtrov tretje in četrte stopnje s programirljivim logičnim krmilnikom (PLC). Uporaben je za izločanje neželenih signalov nizkih frekvenc pri obdelavi analognih vrednosti v sistemu industrijskega krmiljenja s PLC krmilnikom SIEMENS S7-315-DP. Za praktično izvedbo smo izbrali eliptični filter z mejno frekvenco 3 Hz in frekvenco vzorčenja 50 Hz. Vrednosti koeficientov smo zapisali v formatu tipa long. Tako smo dosegli dušenje v zapornem pasu 40 dB, kot smo to pričakovali glede na simulacijske rezultate dobljene v okolju MATLAB. S PLC krmilnikom realizirani digitalni filter in simulacijsko strukturo v okolju MATLAB smo primerjali s pomočjo impulznega odziva.

Tabelarično smo podali rezultate za filtra tretje in četrte stopnje s koeficienti zapisanimi v daljšem in krajšem formatu. Grafično smo podali celoten, podrobneje pa le prepustni pas amplitudnega frekvenčnega spektra digitalnega filtra 4 stopnje. Podali smo primerjavo odstopanj impulznih odzivov digitalnega filtra v direktni in kaskadni izvedbi. V primerjavi z digitalnim filtrom tretje stopnje, kjer dušenje 40 dB dosežemo pri frekvenci 7Hz, smo s filtrom četrte stopnje dosegli dušenje 40 dB že pri frekvenci 4Hz.

1. Introduction

Processing of analog signals is usual in almost every automation process which is done with PLC controller. The analog input values which we obtain at the input (or as a result of intermediate calculations), are modified in most cases due to the various interferences. Therefore, it is often neccessary to dump interference with additional equipments, such as software (SW) or hardware (HW) in order to assure undisturbed continuity of the process which we control. For the fact that used sensors and converters do not distinguish among useful and disturbing signals, the controller system receives useful signals corrupted with unwanted signal as interference. Interferences are especially dangerous, if the frequency matches with mechanical resonant frequency of the system. In such cases, the controller becomes completely useless.

The interferences can be removed in several ways; by means of the analog filter in the output of controller, or by SW implemented filter inside PLC controller.

Analog filter represents a simple way to separate interferent signals. The most used is RC filter. Sometimes it could be enough to use only capacitor because resistance is already included in resistance of contacts, conductors and internal resistance of signal source. The problems appear when loop resistance is changed because at the same time cutt-off frequency will be changed as well. Differences appear at the use of current and voltage inputs of PLC controller. With current inputs, where low resistance is present, it is even harder to remove interferences. With current inputs, we also need a coil for smoothing , even though coil is not so common used as a capacitor. That is why analog filtering in that manner is very rare. Analog filter also becomes completely useless, if we want to separate

interferences in the signal which is present as a result of intermediate calculations of one or more different variables.

In this article, the way of filtering with digital filter is described. Digital filter is implemented inside the PLC controller, which is used for controlling of the main industrial process. The simple solutions use algorythms for smoothing, which work as non-recursive filter and is used by emphirical directions. In our example, we designed and made recursive form of the third and fourth order digital filter with exact determinated parameters connected to a cut-off frequency, a gain in passband and attenuation in stop band. The coefficients of the filters are calculated with MATLAB.

2. Basic structures of digital filters

The origin for design of filter structure is a system function H(z) and diference equation. For every linear, time invariant discrete system, exist more than one equivalent structure. Structures are canonic or noncanonic. A digital filter structure is said to be canonic if the number of delays in the block diagram representation is exactly equal to the order of the filter /1/. Noncanonic structure we use with processors with floating point arithmetic, because they have only one adder. Within PLC automation applications the second order filter is the most popular structure used.

For realization of higher order digital filters, we can use direct canonic or direct transposed structure. In our case both are equal. The only difference makes the number of adders and multipliers needed for realization. For the structure of the higher order, we generally use cascaded /2/ or paralel realization of structures of the 1st and 2nd order, regardless the filter is IIR or FIR type.

3. PLC controller

Programmable logic controller is dedicated microcontroller which is used in industrial automation field and remote controlling of various process. In the beggining, PLC signals were only digital. Also, modern PLC controller handles analog signals. It means that we can carry out digital filter as a part of program. Such filter is equivalent to hard wired filter as equipment.

3.1 Cycle time

Cycle time is very important criteria for evaluation of PLC speed. These data give us information about time needed for execution of all functions of PLC controller. Execution of PLC program is cyclic which means that changing of variables during one cycle will not be considered and executed in PLC program.

3.2 Cyclic interupt

If we need very fast processing of some signals or functions, e.g. allarms, PID regulators etc., it is possible to use a different models of program executing with interrupt functions so called „watchdog interrupt". A „watchdog interrupt" is an interrupt which is generated at the same periodic intervals. It allows to execute a particular program or function, periodically, independently of the processing time of the cyclic program. Access to this function is different for different maker of PLC devices. It is possible to make cyclic interrupt in different ways with S7-300/400, because it is made with organisation block OB35. There are two possible modes; to generate pulse with OB35 and use this pulse as a clock for digital filter or to call function of digital filter from OB35. In this example, digital filter is implemented in OB35.

Time interval for cyclic interupt of OB35 must be longer than time neccessary for executing function which is called from OB35. If this condition is not satisfyed, the operating system calls OB80 (timing interupt). If OB80 has not been programmed, the CPU goes to STOP. /3/.

4. Higher order recursive digital filters

The higher order recursive filters are usually performed as a cascaded structure of more structures of first and second order, with exception in a direct form. Although it is possible to obtain rather good results with second order filter compared to empirical filters, with the former it is possible to obtain either greater attenuation or narrower transition band of amplitude frequency characteristic (greater slope). We must bear in mind that such designed filter must not make any interference with main program in PLC, or to make a significant delay in the main program.

4.1 The third order recursive digital filter

In our case, we are going to show a design of the 3rd order recursive digital filter which meets the requirements. For this filter, the requirements are: sampling frequency Fs=50 Hz; cutt-off frequency Fm=3 Hz; max attenuation in passband Ap=1 dB; Attenuation (minimal) in stopband As=40 dB. In order to achieve this, it is neccessary to use 2 cascade structures. For this, we made a special function block (FB) that analised behaviour of the filter.

Comparison between results of simulation, (obtained with MATLAB) and practical realization with PLC controller, we estimated when comparing impulse responses. Phase frequency characteristic was not important, so we didn't analyse it in this work. To record the impulse response, we modified function block of the 2nd order recursive filter with the „clk" input being active. This input is active, if we trigger FB with internal clock, generated internaly in program. If FB is called from OB35, this input is not active, i.e. must be deactivated. It means that we obtain at each trigger just one output value (value of inpulse response). As input value at the first cycle was 1000.0, and zero for all other cycles.

Filter coefficients we calculated with MATLAB program or directly with FDA toolbox, which is also a part of Matlab. The elliptic filter coefficients in a long form are shown in table 1.

Table 1: The coefficients of 3rd order elliptic filter

b3= 0,0136 426 503 0127	a3= 1,00
b2=- 0,0018 096 880 4567	a2= -2,5336 859 770 7381
b1= 0,0018 096 880 4567	a1= 2,2493 565 017 9860
b0= 0,0136 426 503 0127	a0= -0,6920 046 002 1359

For transforming of higher order filter in cascade form, we use MATLAB (FDA toolbox or instruction *ZP2SOS*), which gives us the second order stucture, SOS matrix in the following form:

$$SOS = \begin{bmatrix} b_{21} & b_{11} & b_{01} & 1 & a_{11} & a_{01} \\ b_{22} & b_{12} & b_{02} & 1 & a_{12} & a_{02} \\ . & . & . & . & . & . \\ b_{2L} & b_{1L} & b_{0m} & 1 & a_{1m} & a_{0m} \end{bmatrix} \quad (1)$$

In the first row, there are coefficients of the first structure (nominator and denominator), in the second row a second structure, etc. In the matrix, "m" refers to the number of second order structures.

If SOS matrix is known, we can write down a general form of the transfer function in the form as follows:

$$H(z) = g \cdot \prod_{k=1}^{L} \frac{b_{2k} + b_{1k} \cdot z^{-1} + b_{0k} \cdot z^{-2}}{1 + a_{1k} \cdot z^{-1} + a_{0k} \cdot z^{-2}}, \quad (2)$$

where "g" refers to gain.

For the 3rd order digital filter, SOS matrix can be expresed as:

$$SOS = \begin{bmatrix} 1{,}00 & 1{,}00 & 0{,}00 & 1{,}00 & -0{,}818337350 & 0{,}00 \\ 1{,}00 & -1{,}132649302 & 1{,}00 & 1{,}00 & -1{,}715348626 & 0{,}845622651 \end{bmatrix} \quad (3)$$

and gain is g = 0,013642650301

For transfer function of digital filter with two cascade structures

$$H(z) = g \cdot \frac{b_{2a} + b_{1a} \cdot z^{-1} + b_{0a} \cdot z^{-2}}{1 + a_{1a} \cdot z^{-1} + a_{0a} \cdot z^{-2}} \cdot \frac{b_{2b} + b_{1b} \cdot z^{-1} + b_{0b} \cdot z^{-2}}{1 + a_{1b} \cdot z^{-1} + a_{0b} \cdot z^{-2}}, \quad (4)$$

SOS matrix gives us values of coefficients of each structure, a and b; their coefficients are shown in table 2.

It is shown that for 3rd order digital filter, coefficient b0a=0 and a0a=0. Therefore, we will assume gain in the first structure, because of less coefficients and less multipliers.

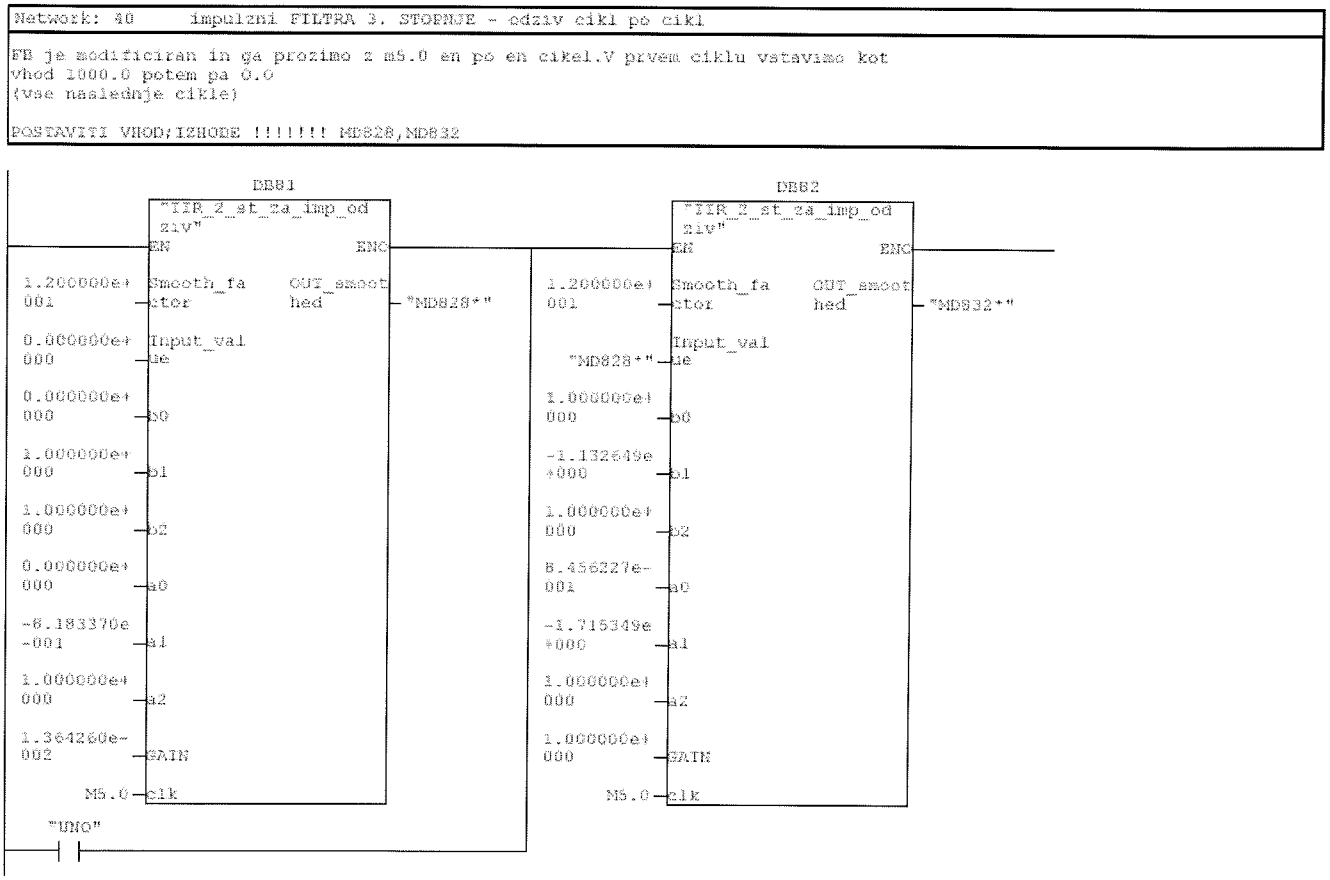


Fig. 2: A part of the organisation block for entry of the coefficients and input variables of 3rd order IIR filter in the first and second cascaded structure

A general realization form for the 3rd order IIR filters is shown in figure 1. Since it is a general form for two cascade structure, it can be also used for 4th order IIR filter.

Table 2: The coefficients of both cascaded structures for 3rd order eliptic filter

b2a	=	1,00
b1a	=	1,00
b0a	=	0,00
a1a	=	-0,818337350
a0a	=	0,00

b2b	=	1,00
b1b	=	-1,132649302
b0b	=	1,00
a1b	=	-1,715348626
a0b	=	0,8456226513

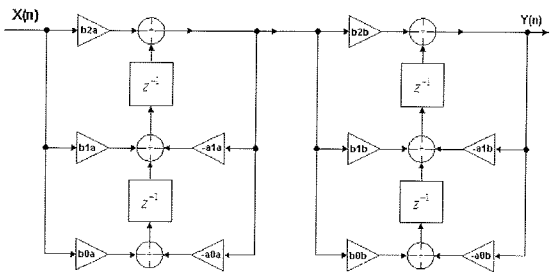


Fig. 1: General cascade realization for two structures recursive digital filter

The figure 2 shows a mask for input of coefficients in each cascade structure of digital filter. In the proceeding example, the output from the first structure is 32 bits marker double word (MD828), and is the input into the second structure. The output from the filter is MD832.

Comparison the impulse response of the 3rd order digital filter, carried out with PLC in the cascade structure and with simulation results, (got from MATLAB), shows us that is in case of long format coefficients, deviation could be neglected, as we already concluded in case of 2nd order

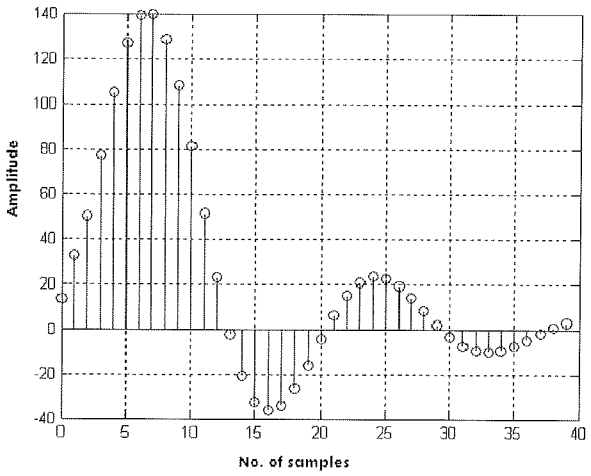


Fig. 3: Impulse response of 3th order IIR digital filter

Table 3: The comparision of first 20 values of impulse response of of 3rd order digital filter

sample no.	Results of simulation (MATLAB)	Practical realisation with PLC	Deviation %
0	13,642650301273000	13,6426	0,000368706
1	32,756503712783000	32,7564	0,000316617
2	50,497821912436000	50,4977	0,000241421
3	77,347995718632000	77,3478	0,000253036
4	105,0555793178170	105,055	0,000551439
5	127,13935612429400	127,139	0,000280105
6	139,34892221216300	139,349	-5,58223E-05
7	139,83616962670000	139,783	0,0380228
8	128,70340523262500	128,703	0,000314858
9	108,10092058526500	108,101	-7,34635E-05
10	81,12485120469300	81,1248	6,31184E-05
11	51,45073780478000	51,4507	7,34776E-05
12	22,68763570368100	22,6877	-0,000283398
13	-2,10893694285100	-2,10885	0,004122591
14	-20,77181759385600	-20,7717	0,000566122
15	-32,18556365668600	-32,1855	0,00019778
16	-36,28428240826100	-36,2843	-4,84831E-05
17	-33,91036398052200	-33,9104	-0,00010622
18	-26,57448525769500	-26,5746	-0,000431776
19	-16,16379328939600	-16,164	-0,00127885
20	-4,64461306675500	-4,64483	-0,004670642

filter. The First 20 samples of impulse response are illustrated in table 3.

A complete impulse response of digital filter made with PLC is shown in figure 3. According to impulse response we calculated appropriate magnitude frequency characteristic with MATLAB (gain response) as it is shown in figure 4.

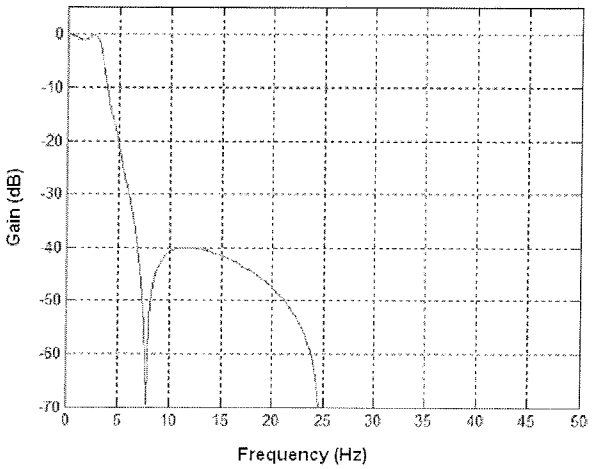


Fig. 4: The magnitude frequency response of 3th order IIR digital filter with cut off frequency 3 Hz

The amplitude frequency characteristic correspond with requirements. Attenuation of 40 dB is obtained at 7 Hz, almost at double sampling frequency.

4.2 The fourth order recursive digital filter in direct form

Similar to the 3rd order filter, when using a mentioned filter block, we can extend it to the 4th order filter. We are going

to analyse a behaviour of the eliptic recursive digital filter with following characteristics:

- Fs= 50 Hz
- Fm=3 Hz
- Ap=1 dB
- As=40 dB
- Elliptic (Cauer) filter
- Lowpass filter

We will analyse a deviation of the values of impulse response and frequency amplitude characteristic with shortened coefficients.

Block diagram of the filter is shown in the figure 5:

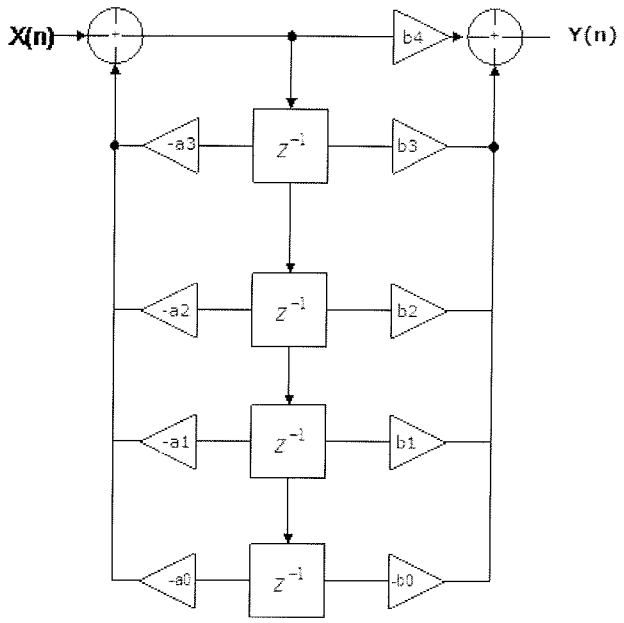


Fig. 5: Block diagram of the 4th order recursive filter realized in the direct form

We can get the coefficient of the filter with partially modificated MATLAB script, the same we used for the 2nd order filter, or with FDA toolbox , which is also a part of the same program package.

Table 4: The coefficients of 4rd order elliptic filter

b4= 0,0128 150 304	a4= 1,00
b3=-0,0308 830 053	a3=-3,5033 975 914
b2= 0,0416 358 137	a2= 4,7510 732 531
b1=-0,0308 830 053	a1=-2,9436 272 013
b0= 0,0128 150 304	a0= 0,7021 224 885

If we cut off a certain number of decimal places of coefficients, we will get a deviation of the impulse response values and a deviation of the shape of magnitude frequency response. For analyse, we cut number of decimal places to 3. The table 3 shows the results of comparison of impulse response obtained with MATLAB simulation and response of real PLC for the 4rd order digital filter with coefficients in a shortened mode. A deviation is noticed in the input of the coefficients with 3 decimal places.

Table 5: Comparison of the first 20 values of impulse response for 4th order digital filter

sample no.	MATLAB	From PLC	Deviation %
0	12,81503050	12,0	6,359
1	14,01314165	12,0	14,366
2	29,84427179	26,15	12,378
3	44,81855444	39,737	11,338
4	60,29166857	53,957	10,506
5	76,30091953	68,731	9,921
6	91,83710540	83,006	9,616
7	105,23871650	95,126	9,609
8	114,63757670	103,264	9,921
9	118,38576890	115,5098	10,608
10	115,40354470	101,792	11,794
11	105,40486000	90,919	13,743
12	88,97838699	73,833	17,021
13	67,5241582	51,965	23,042
14	43,06632776	27,369	36,449
15	17,9783246	2,454	86,350
16	-5,333836469	**-20,332**	**-281,189**
17	-24,74190315	-38,816	-56,883
18	-38,655628	-51,363	-32,873
19	-46,19925186	-57,072	-23,534

It is evident from the table 5 that a deviation of impulse response values are large in case of cutting off the coefficients. A graph in the figure 6 shows an impulse response for double precision and shortened mode coefficients.

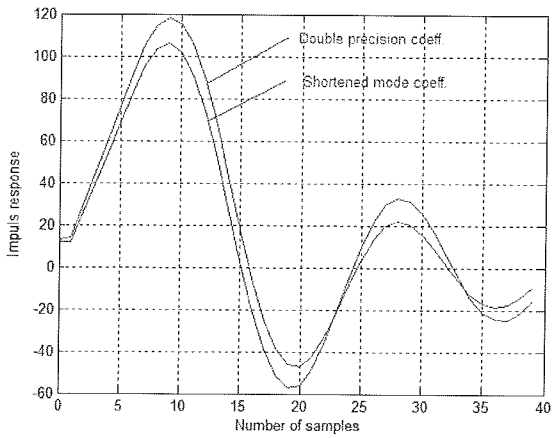


Fig. 6: Impulse response of the 4th order digital filter for the exact and shortened coefficients

Although a deviation of impulse response values is large, a frequency characteristic is not deformated to a great extent. In the figure 7, a frequency characteristic of digital filter for shortened and long (original) coefficients are shown. From this figure it is transparent that characteristic is more degraded in passband, above all in a bigger ripple in passband than it is designed. Figure 8 shows a detail of passband ripple. In the stopband there is a filter with shortened coefficients is even better than originally designed

filter (at this design stage, we determine maximal allowed ripple in passband and minimal allowed attenuation in stop-band).

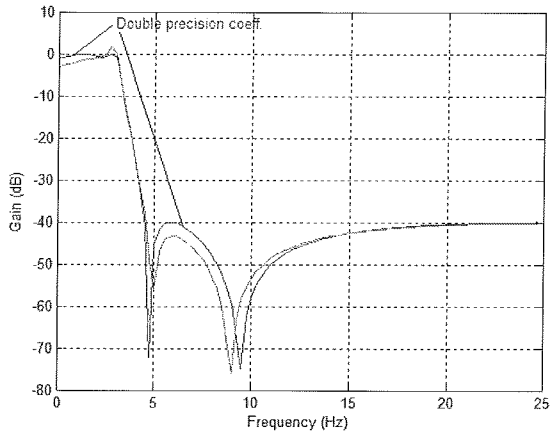


Fig. 7: The magnitude frequency response of 4th order recursive filter for shortened and long format coefficient

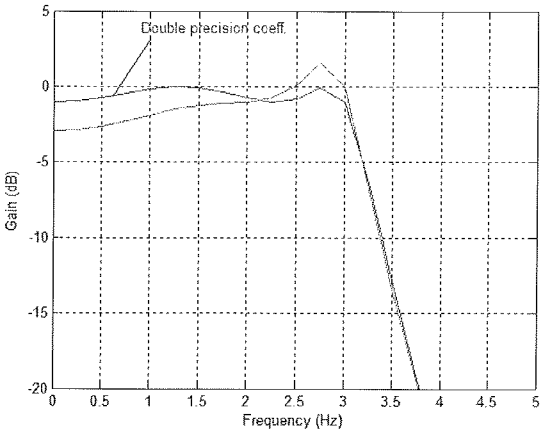


Fig. 8: The magnitude frequency response of the 4th order recursive digital filter for shortened and long format coefficient -detail of passband - ripple

4.3 The fourth order recursive digital filter in cascade form

Having in mind that a direct form of realization is the most sensitive influence of quantization of the coefficients (in our case cutting off the decimal places), we will continue analysis of the behaviour of the digital filter in a cascade form. All requirements will remain unchanged. With FDA tools, we will calculate coefficients of two cascade structures (SOS matrix). Equations (1) and (2) are given in detail.

Following coefficients are:

The first structure :

b21=b2a=	+1,00		1,00
b11=b1a=	-0,7544 77 551	a11=a1a=	-1,7130 35 557
b01=b0a=	+1,00	a01=a0a=	+0,7587 40 607

The second structure :

b22=b2b=	+1,00		1,00
b12=b1b=	-1,6555 42 739	a12=a1b=	-1,7903 62 034
b02=b0b=	+1,00	a02=a0b=	+0,9253 78 821

and gain g= 0,0128 150 304. Regarding equation 4, we got following (gain and coefficients are shown shortened, for the sake of clarity):

$$H(z) = g \cdot \frac{b_{2a} + b_{1a} \cdot z^{-1} + b_{0a} \cdot z^{-2}}{1 + a_{1a} \cdot z^{-1} + a_{0a} \cdot z^{-2}} \cdot \frac{b_{2b} + b_{1b} \cdot z^{-1} + b_{0b} \cdot z^{-2}}{1 + a_{1b} \cdot z^{-1} + a_{0b} \cdot z^{-2}}$$

$$H(z) = 0.0128 \cdot \frac{1 - 0.7544 z^{-1} + z^{-2}}{1 - 1.713 z^{-1} + 0.7587 z^{-2}} \cdot \frac{1 - 1.6555 z^{-1} + z^{-2}}{1 - 1.7903 z^{-1} + 0.9253 z^{-2}} =$$

$$g \cdot \frac{N1}{D1} \cdot \frac{N2}{D2} = H1 \cdot H2 \quad ;$$

where N1, N2; D1 and D2 are nominator and denominator of both functions and **g** is gain. In function H1 is already included gain **g**. If we use instruction **zp2sos** instead FDA toolbox for calculation of coefficients, than the gain **g** is already included in coefficients of the transfer function, i.e. **g=1**, so it can be omitted. (Regularity of calculation cascade structure, is possible to check with MATLAB instruction **conv** with following script:

```
N1= /1 -0.7544 1/
N2= /1 -1.655 1/
g=0.0128150
N= conv (N1,N2);
Ng=g*N
```

In this equation, "Ng" is a nominator of the filter in a direct realisation.(Similar goes also for a denominator)

With MATLAB, we can represent magnitude response for each structure separately. In the figure 9, there are shown magnitude responses of the first, second and direct realisation of the filter. From the picture is visible that the characteristic of direct realisation is a result of multiplication of the characteristic of the first and second structure (in log. scale , it will be the summ, i.e. H=H1 + H2)

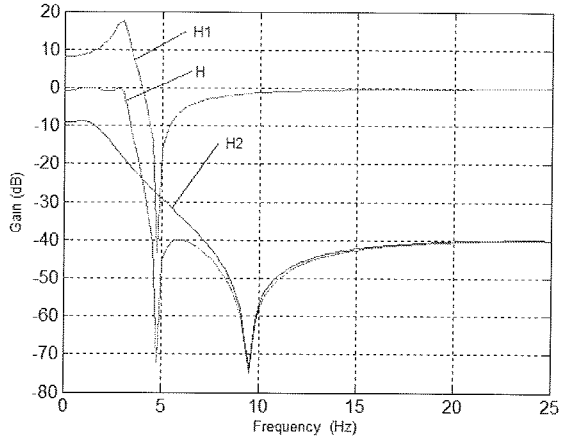


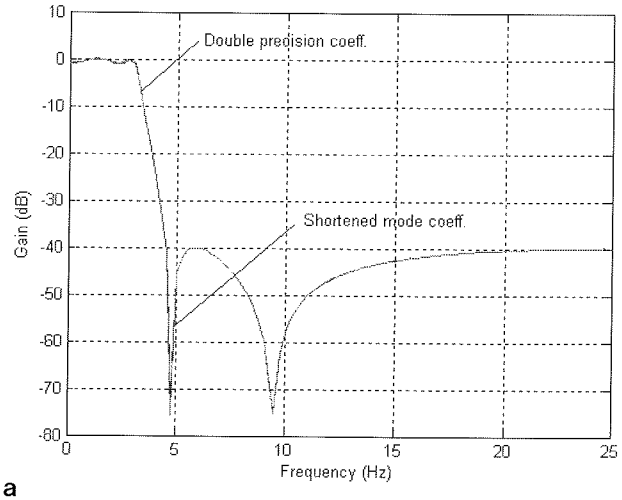
Fig. 9: Decomposition of frequency characteristic of the 4th order digital filter into two second order functions

We continued the analysis with quantized coefficients especially those in shortened mode. For analysis, we cut coefficients to 3 decimal places. Table 6 shows results of comparison of impulse response of MATLAB simulation and a real digital filter 4th order, realised with PLC controller, with coefficients in a shortened mode. Deviation (error) is shown for coefficients cut down to 3 decimal places.

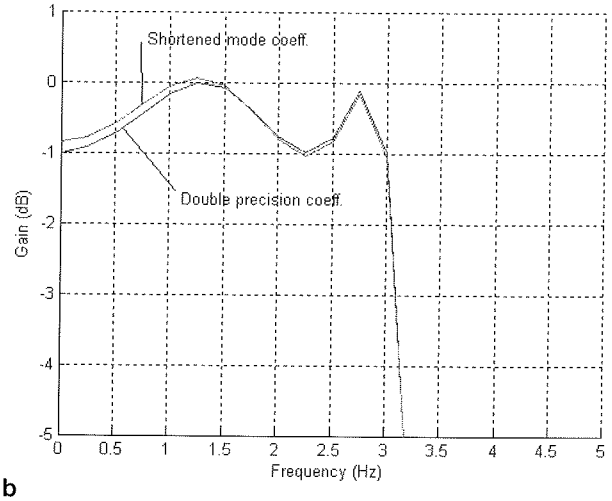
Table 6: Comparison of the first 20 values of the impulse response, for the 4th order digital filter, realised in cascade realisation, with coefficients in long and shortened mode

sample no.	MATLAB	From PLC	Deviation %
0	12,81503050	12,8150304	7,6859E-07
1	14,01314165	14,01964326	-0,04639651
2	29,84427179	29,87032369	-0,0872928
3	44,81855444	44,87469011	-0,12525094
4	60,29166857	60,40018669	-0,17998858
5	76,30091953	76,48888885	-0,24635262
6	91,83710540	92,13215093	-0,32127049
7	105,23871650	105,6664377	-0,40642949
8	114,63757670	115,2196907	-0,50778637
9	118,38576890	119,138391	-0,63573696
10	115,40354470	116,3353537	-0,80743537
11	105,40486000	106,5151964	-1,05340152
12	88,97838699	90,25555199	-1,43536543
13	67,5241582	68,94430001	-2,10316107
14	43,06632776	44,59330464	-3,54563986
15	17,9783246	19,56483705	-8,8245845
16	-5,333836469	-3,743727912	**29,8117231**
17	-24,74190315	-23,20897484	6,19567662
18	-38,655628	-37,24072413	3,66027909
19	-46,19925186	-44,95804954	2,68662861

From results shown in table 6, it is evident, that deviation is significantly smaller than in a direct realization structure. Magnitude frequency characteristic are practically equal for coefficients given in long and short mode, as shown in the figure 10a. A small deviation is still present in passband, in the figure 1b is a detail of characteristic in passband.



a



b

Fig. 10: a) Frequency characteristic of the 4th order digital filter in cascade realization with coefficients in a shortened mode b) detail of characteristic in passband

Comparison of deviation of impulse response for entering coefficients in long and shortened mode, for direct realisation, and shortened mode for direct realisation as it is shown in table 7. In this comparison, values calculated with MATLAB, are referent.

From the results we have shown so far, we can conclude that entering of shortened coefficients for the 4th order digital filter in a direct realisation, is very important for behaviour of such filter. We can not neglect a deviation of impulse response from teoreticaly calculated and actual magnitude response. For a direct realisation of the higher order filter, realised in a direct form, is it necessary to enter coefficients in exact (long) form. A graphic representation of deviation for the 4th order IIR filter in cascade realisation, for the extact and shortened mode of the coefficients and for a direct realisation is shown in the figure 11. Figure shows absolute values of deviation.

Table 7: Comparison of the first 20 values of impulse response for the 4th order digital filter for direct and cascade realisation with coefficients in a long and shortened form.

MATLAB X 1000	PLC impulse response		
	Direct form shortened coefficients	Cascaded realisation	
		Long coefficients	Shortened coefficients
12,81503050	6,35995754	3,88992E-06	7,6859E-07
14,01314165	14,36609791	-5,95899E-05	-0,04639651
29,84427179	12,37849533	-9,45304E-05	-0,0872928
44,81855444	11,33805967	-0,000101644	-0,12525094
60,29166857	10,50670635	-0,000217991	-0,17998858
76,30091953	9,921138016	-0,000236518	-0,24635262
91,83710540	9,616053733	-0,000320783	-0,32127049
105,23871650	9,609311903	-0,000364398	-0,40642949
114,63757670	9,921333834	-0,000456498	-0,50778637
118,38576890	10,60834337	**0,014924823**	-0,63573696
115,40354470	11,7947371	-0,000654489	-0,80743537
105,40486000	13,7430665	-0,001081544	-1,05340152
88,97838699	17,02142228	-0,000913721	-1,43536543
67,52415820	23,0423579	-0,001246658	-2,10316107
43,06632776	36,4491903	-0,002025343	-3,54563986
17,97832460	86,35022977	-0,004312944	-8,8245845
-5,333836469	**-281,1890394**	0,013432533	**29,8117231**
-24,74190315	-56,883647	0,002518605	6,19567662
-38,65562800	-32,87327787	0,0013659	3,66027909

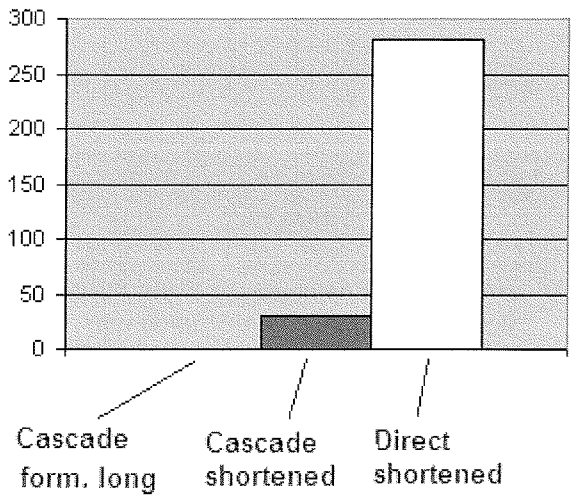


Fig. 11: Error of impulse response of 4th order IIR filter for different realization and lenght of coefficient (in %)

5. Conclusion

This article challenges a possibility of realization of the recursive digital filter of the third and fourth order with plc controller. Although sensors and transducters, (we usually have at automation fields with plc controllers), do not distinguish useful signals from unwanted signals (noise and interference) the system does. Therefore, there is a need for additional equipment, SW or HW, which helps to eliminate the disturbances, so the controlled process would continued faultlessly. As the application of automation of industrial processes gets more demanding, appears the demand for digital elimination of unwanted input signals.

Regarding this in our applications, the influence of nonlinear phase is not critical for filtering of disturbanced signals, we chose recursive filter applying the coefficients of elliptic filter. We chose elliptic filter, because a useful slope of frequency characteristic in passband has lowest order. Also a ripple of amplitude characteristic was not critical if we consider limit values of the system.

A description goes furher for a function of the PLC controller and importance of cycle time and interupt, especially with controller Siemens S7 .

The coefficients of filter with MATLAB are calculated directly specifically with the aid of FDA toolbox.

For digital filter of the 3rd and 4th order, we analysed a detailed influence of cutting the coefficients length to the characteristic of the filter. For realization of the filter, we used structures of 2nd order, which we applied in cascade realization of filter.

For recalculation of the 3rd order filter in cascade structure, we used MATLAB, which enabled determination of the second order structures as a matrix structure (SOS matrix). With shown SOS matrix, cascade realization of the 3rd and 4th order filter is simple defined. The figure 2 shows a part of the organization block of PLC controller with the mask for input of coefficients and input variables in each structure.

Comparison of impulse responses of the 3rd order digital filter made by PLC in cascade form with simulation results from MATLAB, also specifies a negligible deviation in case of exact values of coefficients (format long). Larger deviations appear just at calculation with shortened coefficients. Deviations are result of recursive mode of calculation. A direct form realization of the 4th order filter with shortened coefficients, reveal large deviations, even though deviation of the amplitude characteristic is not significant. In stopband, such filter is considered a better option, because it has less ripple than a designed one. With cascade realization of the 4th order filter, we indicate that deviation using coefficients values in long format, can be truncated, they match MATLAB results. For the filter in cascade form realization with shortened coefficients, we proved that deviation of values of impulse response is not neglectful, but is still lower than in a direct realisation. Deviation of amplitude characteristic appears in passband and is really small (<0.5 dB). Comparation of impulse response for different realizations are illustrated in table 7 and figure 11.

The obtained amplitude characteristic matches with requirements. Attenuation of 40 dB is obtained at double cut-off frequency, which is essentially better to the 2nd order filter.

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RATIOMETRIC MEASUREMENT FOR LONG TERM PRECISION, REASONING AND CASE STUDY

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Key words: Circuit-aging effects, current reference, measurement precision, offset voltage, pasteurized soft-boiled eggs, ratiometric measurement, RTD, temperature measurement, temperature sensor, thermistor, thermocouple

Abstract: A survey of modern temperature sensor types is presented. A canonical circuit for temperature measurement is analyzed with emphasis on age-induced measurement error. The circuit requires periodic calibration, which is accepted for instruments, but not for most machines that are used in different industrial processes.

A ratiometric method for temperature measurement and its implementation are introduced. The number of circuit components is minimized as much as possible. What remains, are only the effects of age-induced resistance drift. A stable precision resistor gives confidence in measurement accuracy over a period of 15 years, without periodic calibrations, which is the life time of many apparatuses.

Razmerna meritev za doseganje trajne preciznosti, argumenti in implementacija

Ključne besede: staranje elektronskih vezij, tokovna referenca, precizna meritev, napetosni premik, pasterizirana mehko kuhana jajca, razmerna meritev, temperaturna meritev, temperaturno zaznavalo, termistor, termočlen

Izvleček: Podan je pregled polprevodniških in kovinskih temperaturnih zaznaval. Analizirana je časovna stabilnost meritve temperature z napetostno ali tokovno referenco in z meritvijo toka ali napetosti na temperaturno odvisni upornosti. Vkolikor je potrebna točnost tekom več let in so pogoji delovanja zahtevni, je spremembo napetostnega premika operacijskih ojačevalnikov v takšnem vezju potrebno kompenzirati s kalibracijo. To je uveljavljena praksa pri merilnih inštrumentih, ne pa pri napravah za robustne industrijske procese, npr. za industrijsko pripravljanja hrane.

V nadaljevanju prispevka predstavimo ratiometrično oziroma razmerno izvedbo merjenja temperature. Vplivi spreminjanja parametrov merilnega vezja so v največji možni meri izločeni. Motilni veličini meritve v predstavljeni implementaciji sta samo še vpliv staranja referenčnega upora in staranja temperaturno odvisnega upora. Po znanih podatkih o staranju uporov meritev ostane stabilna brez vmesnih kalibracij vsaj petnajst let, kar je življenjska doba strojev za industrijske procese.

1 Introduction

The contribution of this paper is in the development of a component that encapsulates the ratiometric measurement principle to achieve long-term precision. It has been developed as part of the design of a new type of an industrial kitchen appliance that produces pasteurized soft-boiled eggs. The constraints are: a) temperature error of the thermal process is to be within +-0.25 °C; and b) apparatus life lime is at least 15 years, without periodic calibrations.

The apparatus is a novelty on the market of industrial kitchen appliances. Until now, pasteurized soft-boiled eggs were not industrially produced. Domestic cooking of soft-boiled eggs does not kill salmonella, if present. Killing the bacteria, at higher temperatures, results in hard-boiled eggs.

The pasteurization and cooking of soft-boiled eggs have contradictory requirements. For the former, salmonellae, if present in the center of eggs' mass need to be unfailingly killed. For the latter, the yolk is to remain soft, i.e., coagulation is not to take place. A soft yolk requires a relatively small amount of delivered thermal energy, and the opposite is true for the destruction of salmonella in the center of the yolk. Since the two requirements are in contradiction, there have been until now no soft-boiled eggs offered in places where infection by bacteria, especially salmonella, would present a catastrophic event that could even lead to death of an elderly customer and potential law suits. A short calculation shows that pasteurized soft-boiled eggs have selling potential in breakfast restaurants of hotels, in hospitals, in homes for elderly people, as a replacement or supplement to salami and cheese.

The patented thermal process /1.2/ requires implementing a specific thermal function with temperature error less than +-0.25 °C. When regulating within +-0.25 °C, measurement imprecision is to be at most within +-0.1 °C. It is commonly understood that the market of professional kitchen appliances does not tolerate much servicing during the lifetime of a product, which is no less than 15 years. Calibration of the temperature measurement circuit every few years of operation is out of question

The problem of precise and stable temperature measurement divides into two details. One is choice of a temperature sensor; the other is design of an electronic component that converts temperature into some electrical quantity. Temperature can be measured by contact or by infrared emission, which is not addressed in this paper.

2 Contact temperature sensors

For a contact temperature sensor, one chooses amongst thermocouples, Resistance Temperature Detectors (RTDs), thermistors, and semiconductor transducers /3/. These types of sensors are built into temperature measurement devices that are built for different purposes.

When one assembles e.g. a production line he chooses among pre-built measurement devices. It is irrelevant to the designer of a new production line, which type of sensor is used in the device. The important factors are technical specification, quality, and cost.

When designing a new apparatus with common constraints on temperature measurement, it is about ease of integration and cost of the temperature measurement device.

When designing a mass-produced high-tech product where long-term measurement precision and accuracy are critical, careful selection of sensor and circuit is needed. Issues besides precision and accuracy are: responsiveness, indifference to environment disturbances, simple calibration in production, and measurement accuracy within years of product life time, if only feasible without recalibrations. Such are the constraints of the apparatus in the case study.

2.1. Thermocouple

Two wires of different metals or alloys, being connected at one side to a voltmeter, and being soldered or welded at the other side, are laid out in a temperature field with gradient, produce voltage that is proportional to the temperature difference between both wire ends, i.e., between the voltmeter and the joint. Voltage readout is a function of temperature difference between locations of the voltmeter and the joint.

Different combinations of materials produce different voltages. They are used for different temperature ranges, with different accuracies.

The American Society for Testing and Materials defines a number of commercially available thermocouple classifications in terms of performance. Types E, J, K, N, and T are base metal thermocouples, and can be used to measure temperatures from about -270 to 1372 °C. Types S, R, and B are noble-metal thermocouples, and can be used to measure temperatures from about -50 to 1820 °C /4/.

Characteristic data of most used thermocouples (types E, J, K, R, S and T) can be found in /3/. One reads that thermocouple type S (platinum with 10% rhodium vs. platinum) is used for the highest temperature range (0 °C to 1750 °C), and thermocouple type J (iron vs. constantan) has the highest accuracy (+0.1 °C). Typical values of temperature-induced voltages are in a range of some ten microvolts per degree Celsius.

A thermocouple measures temperature difference between two locations in space, one being at the joint of the two different wires, and the other being at the connector of the measuring device. In order to measure the actual temperature at the joint of the wires, one must know, and add the temperature at the location of the measuring device. This temperature is to be measured by some other means, as an absolute value and not as a temperature difference - which is the case with thermocouples.

A logical question arises at this point: if one is able to measure temperature by other means, with the same or better precision and accuracy, why add the temperature difference instead of directly measuring the temperature at the point of interest? The single most important answer is that other means of measurement can only be used over a smaller temperature range. Thermocouples, on the other hand, can be used over a wide range of temperatures. They are quite rugged. As such, they are often fastened under a screw. They can be manufactured on a spot, by either soldering or welding. If the measurement system performs the entire task of reference temperature measurement and conversion of voltage to temperature in software, using a thermocouple becomes easy: to measure temperature, one connects only a pair of wires. Thermocouple measurement is convenient when it is required to monitor many temperatures at once.

If one builds a thermocouple-based temperature transducer from scratch, he will face two challenges: a) it is challenging to linearly amplify signals in order of only some 10 microvolts because of low signal to noise ratio; and b) a solution is needed to measure the temperature at a reference location. Typical accuracy of a thermocouple is +-0.5 °C /5/.

2.2. Resistance Temperature Detector (RTD)

RTD is a synonym for a metal resistor used for temperature measurement. Metal resistance increases with temperature. Already about 1870 platinum was considered as a metal for sensing temperature. Platinum RTD (PRTD) is considered as one of most stable, linear, and accurate temperature sensors. Platinum, being a noble metal, does not react with elements of the environment, even at elevated temperatures - consequentially, it is a stable base for design of a precise and accurate temperature measurement system.

Before development of microelectronic technology, RTDs were wound up to a skeleton that was mounted within a cylinder. A seal was added at the end. Theses sensors suffered a delay /6/. Modern RTDs are produced as the deposit of a platinum film on a ceramic substrate. Each individual sensor is calibrated, i.e., laser-trimmed and sealed in casing.

All noble metals can be considered for RTDs, since they do not change internal structure at elevated temperatures. They do not react with the environment. For practical reasons, metals with higher resistance are preferred to minimize effects of parasitic resistances of wires and intercon-

nect. Gold and silver have low resistance, tungsten is fragile, and platinum presents an optimal choice. Commercial annotations for PRTDs are PT100 and PT1000. The former has resistance of one hundred Ohms at zero degrees Celsius, the latter one thousand Ohms at zero degrees Celsius. The function of resistance versus temperature is nearly linear. For higher accuracy, polynomial coefficients are available.

A basic RTD circuit requires a constant current source for biasing and an analog instrumentation circuit (such as an instrumentation amplifier) to instrument the voltage drop across the RTD /4/.

2.3. Thermistor

Thermistors are made using semiconductor materials and can have either a Positive or Negative Temperature Coefficient (PTC or NTC, respectively). The vast majority of thermistors have a NTC.

Thermistors are more sensitive to temperature changes than metal-based sensors. In metals, resistance is proportional to temperature. In semiconductors, conductance (the amount of free electrons) is an exponential function of temperature. Small temperature changes result in high changes of resistance and the relation is nonlinear. Accuracy and long-term stability are substantially lower than for RTDs. As elevated temperatures gradually effect the distribution of dopants in a semiconductor, thermistors are not to be used above 150 °C /7/.

2.4. Monolithic linear temperature sensor

Monolithic linear temperature sensor is an integrated circuit with a built-in sensor and circuitry for signal conditioning. Output is a linear function of temperature in the form of current or voltage source, usually with 1 uA/K or 10 mV/K. The temperature range is between -55 °C and 150 °C /4/. Some of these circuits transmit temperature data in a form of serial protocol; some have only a logic output that toggles at a preset temperature.

Monolithic linear temperature sensors present an ideal design option when the simplicity of system design is crucial. Issues of a low signal-to-noise ratio and nonlinearity are solved by filtering, amplification, and linearization within the monolith. Outputs have excellent signal-to-noise ratio and values in a range that is easy to process.

Temperature measurement is based on the exponential relation of free electrons in a semiconductor to temperature. The circuit makes a logarithm of the function. The result is a linear function of temperature. Calibration constants are added. As for thermistors, these circuits are not to be used above 150 °C.

A monolithic linear temperature sensor is designed primarily for ease of usage. It is not to be used in applications of high accuracy with required long-term stability.

3 Circuits for contact temperature measurement

When measuring temperature with thermocouples, low voltages (tenths of microvolts) are to be linearly amplified by an instrumentation amplifier. When building such an amplifier, issues are low signal-to-noise ratio (low voltage on input), gain linearity, long-term stability, and robustness to environment variables (variation in power supply voltage, changes in ambient temperature). The need for accuracy requires calibration. Since thermocouples measure temperature differences, a reference temperature needs to be measured by other means. Monolithic linear temperature sensor is usually used for the purpose /3/.

Measuring temperature with a monolithic linear temperature sensor is most straightforward since the signal conditioning (amplification, filtering, linearization, and calibration) is performed within the monolithic circuit. The output can be directly connected to an A/D converter, comparator, or some serial interface.

Regarding measuring temperature with an RTD or a thermistor, they are both temperature-dependent resistors. As such, they require current or voltage excitation to produce a temperature-dependent variable (voltage or current) by Ohms' law. When processing voltage as a measure of temperature, the sensor needs to be powered by a current reference source.

Filtered and amplified voltage is a base for temperature readout. Some calculation, i.e., linearization and consideration of calibration factors is needed before the readout. Filtered and amplified voltage signal, proportional to temperature, is fed to an A/D converter (usually being an integral part of the microcontroller) and calculation is performed in the microcontroller software.

A canonical circuit for mapping temperature to voltage, by usage of an RTD or a thermistor, is in Figure 1, which is the core of the proposed circuit in /8/.

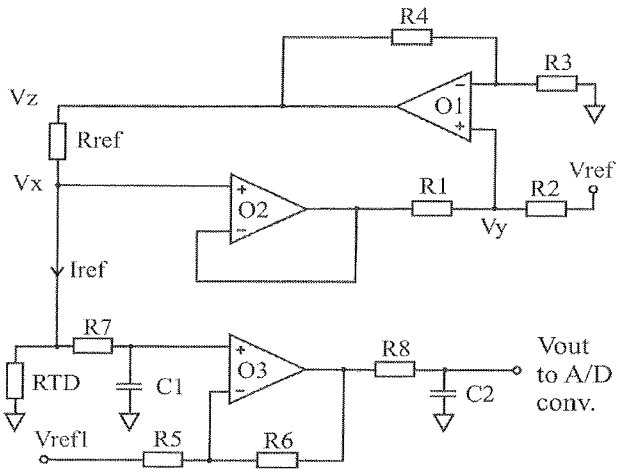

Fig. 1: RTD is powered by a current reference, voltage drop on the RTD is being filtered and amplified, by /8/.

The current reference is built from the operational amplifiers O1, O2, and from the resistors R1 to R4, and Rref. The two filters are made from the R7, C1, and from R8 and C2. The operational amplifier O3, and the resistors R5 and R6 form a gain stage.

Resistors R1, R2, R3, and R4 are of a same value. Consequentially, functionality of the current source is governed by the equations:

$$V_Z = 2V_Y = V_{ref} + V_X$$
$$V_Z - V_X = V_{ref}$$
$$I_{ref} = \frac{V_{ref}}{ref}$$

I_{ref} flows through the RTD to the ground. The corresponding voltage drop V_X on the RTD, being a function of temperature, is amplified by (1):

$$V_{out} = \frac{R_5+R_6}{R_5}\left(V_X - V_{O3\_offset} - V_{ref1}\right) \quad (1)$$

The circuit in Figure 1 consists of three operational amplifiers, eight resistors, two capacitors and two reference voltages. Sensitivity analysis shows that the output voltage V_{out} is most sensitive to changes of V_{O3_offset} at the operational amplifier O3. V_{O3_offset} is multiplied by (R5+R6) / R5, which needs to be about 50 for proper circuit operation. A new circuit is calibrated, but years of usage do influence the electrical parameters of the circuit. Age induced drift of the O3 offset voltage, in 10 years of usage, can cause, based on manufacturers' data on time induced offset voltage drift, an error of one degree Celsius at a measurement range of one hundred degrees Celsius. Importance of time-induced one percent error depends on applications' nature.

When a relatively expensive, accurate, and time-wise stable PRTD is chosen as a sensor, then measurement quality is not to be deteriorated over years of operation by the signal conditioning circuit.

4 Ratiometric measurement

The circuit in Figure 1 is built from 13 circuit components. Each of them is prone to slight changes over years of operation. One cannot expect to build an artifact that would be completely insensitive to influence the environment. Even pyramids, which were built with all available technology of that time to last, changed over centuries.

As one looks into inner working of Nature, he notices that things are interrelated and objects are in certain relations to each other. Different organisms, from bacteria to most powerful predators, compete for their daily source of energy, for water and for space. An absolute amount of stamina is not as important as to be stronger than the competition. Outcome of fight and daily success depends on power imbalance. The power ratio counts the most in practical survival.

In sociology, humans copied these mechanisms quite fast and successfully. For example, Justitia, the Roman goddess of justice, is most often depicted with a set of weighing scales typically suspended from her left hand, upon which she measures the strengths of a case's support and opposition. In the educational process, a teacher makes a ranking of students based on a comparison of their work, not by an absolute scale.

Results of Nature observation were utilized also in some technical domains. For example, in control theory some 15 years ago principles of fuzzy regulation emerged. There, variables are exchanged for probability functions. In manufacturing, some 20 years ago emerged a bionic paradigm. There, manufacturing systems are to have capability of self-organization as different forms of life do. In integrated circuit design, required functionality depends more on ratios of dimensions and dopants than on their absolute values.

Ratiometric measurement is about inducing the measurement result from the comparison of different values. For example, an object of blue color is about blue. When it is compared to another object of blue color, one immediately notices which one is darker and which one is brighter.

4.1. Why measuring by a ratiometric method?

The answer is of a conceptual nature. A hypothesis is that the comparison system is simple enough and robust that it can effectively compare objects (variables) through its lifetime. When it is so, comparison only depends on the properties of the two objects, which are the reference and the measured object.

It is important for implementation that: a) the comparison system is designed to be most robust regarding environment disturbances and aging; and b) that the reference object changes minimally through its lifetime.

An important detail of the answer to the question, why measuring by a ratiometric method, is that such a measuring system does only comparison. This is conceptually a much simpler category than an absolute measurement.

4.2. Implementation

Usually, there are more possible implementations of a particular concept. Criterion on implementation efficiency is that equations of the implementation are to show minimal dependence on environment disturbances and on aging effects.

When precision and accuracy are important in temperature measurement, one chooses the PRTD as a temperature sensor. Logical consequence is to choose a precision resistor for a reference object. A precision resistor is to be least sensitive to temperature, moisture, and aging.

Circuit theory is explored to find means for comparing the two resistors. A working solution compares resistors by

the time that is needed to discharge a capacitor via each of them.

The time needed to discharge a capacitor from voltage V_{co} to V_c, is defined by

$$t = -RCln\frac{V_C}{V_{CO}} \quad (2)$$

The time t is measured in a digital system by counting clock ticks:

$$t = \frac{N}{f_{clk}} \quad (3)$$

For precision, clock frequency f_{clk} is to be high. Then N also becomes high, but the uncertainty of non-measured time within a clock period decreases. This adds to measurement precision.

If one compares capacitor discharge times, discharging the capacitor separately via R_{ref} and via $R(T)$, from the two equations above follows equation (4):

$$\frac{-R_{ref}Cln\frac{V_C}{V_{CO}}}{-R(T)Cln\frac{V_C}{V_{CO}}} = \frac{N_{Rref}f_{clk}}{N_{R(T)}f_{clk}} \quad (4)$$

Then,

$$R(T) = \frac{N_{R(T)}}{N_{Rref}}R_{ref} \quad (5)$$

f_{clk}, V_{co} and V_c in (4) do cancel out. $R(T)$ is calculated by (5) only from the value of a precision reference resistor and from the two discharge times. The implication is that the capacitor, the voltage comparator to V_c and the voltage reference V_{co} can drift over time (years of operation) without affecting the measurement accuracy. In Figure 1, there are 10 circuit elements (O1, O2, O3, R1, R2, R3, R4, Rref, R5, and R6) and two voltage references (Vref, Vref1) that influence the measurement result. In equation (5), it is only the inaccuracy of measuring the two times and temperature induced drift of R_{ref} that affect the measurement..

5 Case study, implementation of ratiometric temperature measurement in the golden egg apparatus

When implementing (5) by the circuit in Figure 2, a new source of measurement uncertainty is introduced. It is resistance of the monolithic analog switches S2 and S3. As a result, equation (5) changes into (6):

$$R(T) + R_{S3} = \frac{N_{R(T)}}{N_{Rref}}(R_{ref} + R_{S2}) \quad (6)$$

To nullify measurement uncertainty that is indicated by the analog switches one has freedom to introduce a second reference resistor. Equation (5) changes to (7); circuit in Figure 2 is modified to circuit in Figure 3.

$$R(T) = \frac{N_{R(T)}-N_{Rref1}}{N_{Rref2}-N_{Rref1}}(R_{ref2} - R_{ref1}) + R_{ref1} \quad (7)$$

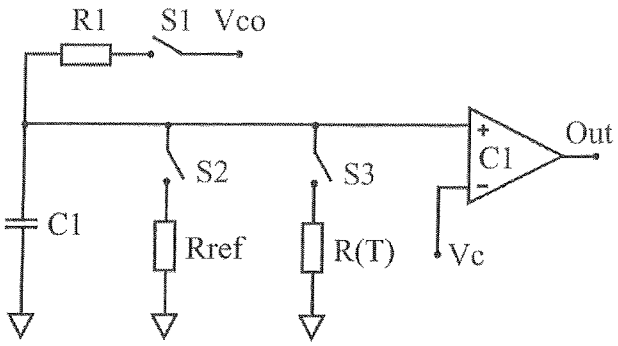

Fig. 2: The circuit to measure R(T) by the equation (5)

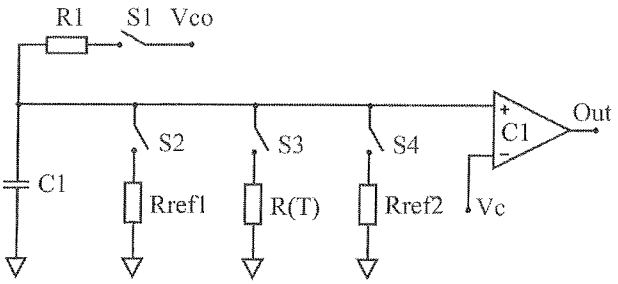

Fig. 3: The circuit that measures R(T) by the equation (7)

Taking into account resistances of switches S2 to S4, equation (7) changes to (8):

$$R(T) + R_{S3} = \frac{N_{R(T)}-N_{Rref1}}{N_{Rref2}-N_{Rref1}}(R_{ref2} + R_{S4} - \\ - R_{ref1} - R_{S2}) + R_{ref1} + R_{S2} \quad (8)$$

Since the switches S2 to S4 are part of the same analog switch monolith, one presumes that their resistances are about same. Then, equation (8) changes to (9):

$$R(T) = \frac{N_{R(T)}-N_{Rref1}}{N_{Rref2}-N_{Rref1}}(R_{ref2} - R_{ref1}) + R_{ref1} \quad (9)$$

Figure 4 shows a circuit for the implementation of (9). The encircled elements are Rref1, Rref2, C1, R1, a monolithic analog switch and two capacitors between the ground and a power supply rail.

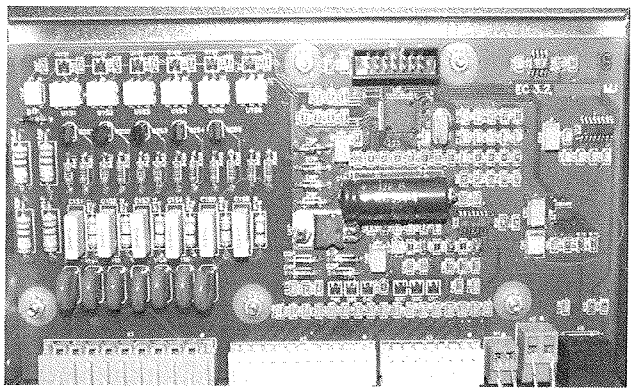

Fig. 4: Hardware of the Egg cooker control system, the temperature measuring circuit is encircled

6 Discussion

While a thermocouple is the most versatile temperature sensor and thermistor is the most sensitive, an PRTD is the most stable.

The most important factors, influencing engineering optimization in the development of the temperature sensing component in the Egg cooker in Figure 5 are: measurement accuracy, long-term stability, reliability, and ease of integration with the rest of the system.

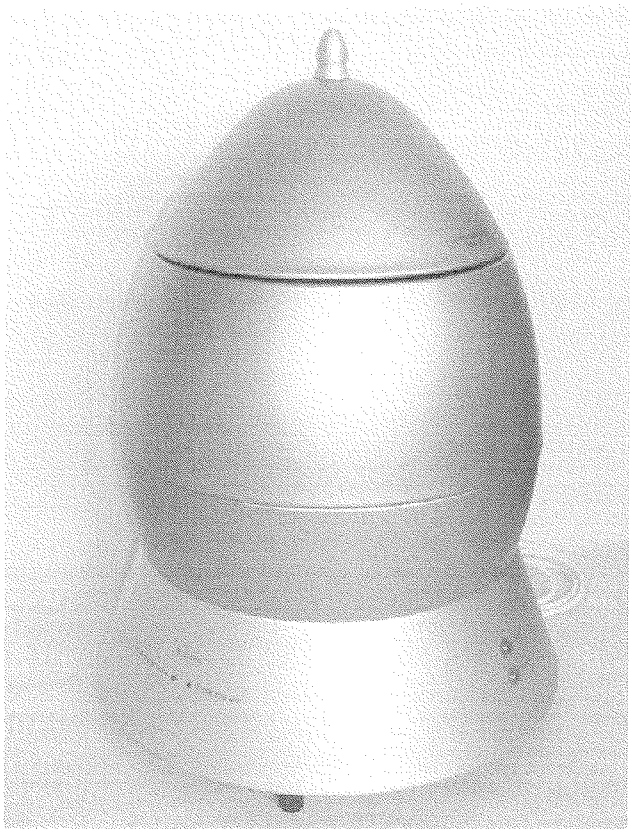

Fig. 5: Egg cooker, an industrial kitchen appliance with the precise and long-term accurate temperature regulation

Design complexity of temperature measurement is to be kept low, to minimize potential failures during the lifetime of the apparatus. In the market of professional kitchen appliances, the expected lifetime is 15 years. Servicing is reduced to elementary maintenance that is to be performed by kitchen personnel. Regular cleaning, water, and filters changing are the usual procedures. Regular calibration of temperature measuring circuit, as for measurement instruments, is not accepted for machines of industrial kitchens.

The requirement for precision of the thermal process of simultaneous pasteurization and cooking soft-boiled eggs is enormously rigorous compared to other types of cooking. The reason is the contradiction that is built into the coexistence of pasteurization and cooking of soft-boiled eggs. Pasteurization needs a high temperature and cooking soft-boiled eggs needs a low temperature. The physics of temperature distribution in eggs was studied and the thermal process was designed and patented. For the required temperature regulation within +-0.25 °C the temperature measurement accuracy of the initially calibrated system needs to stay within +-0.1 °C for the lifetime of the product.

The presented component for ratiometric temperature measurement can be used in other applications where long-term accuracy is required. The remaining issues, i.e., potential differences in resistances of analog switches, and resistance of interconnects, are nullified to greatest extent by the initial calibrations at the most important temperatures of the particular thermal process.

7 Conclusion

Characteristics of a thermocouple, an RTD, a thermistor, and a monolithic linear temperature sensor are annotated. A thermocouple is most versatile, but additional temperature measurement is needed for the reference temperature. The typical thermocouple accuracy is about +-1 °C. A thermistor is the most sensitive, which is important for fast response to a temperature change. A monolithic linear temperature sensor is simplest to integrate into an embedded control system. Both, monolith and thermistor can only be used up to 150 °C. RTDs are the most accurate and stable for the whole time of operation.

A canonic measurement circuit is built from a current reference, a filter, and a voltage amplifier. These functional blocks are made from operational amplifiers, resistors, and capacitors which all change parameters to some extent over years of operation. Time induced change of offset voltage at the operational amplifier of the gain stage affect measurement accuracy the most.

To make measurement consistently accurate over years of operation one is forced to modify the circuit. Not by fixing it, but changing it on the conceptual level. Absolute temperature measurement is changed for ratiometric measurement. The reasoning is elaborated. One of the possible ratiometric implementations is synthesized. Aging induced measurement changes are minimized on a system level to the greatest extent.

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VPLIV NELINEARNOSTI KOMPONENT NA OSCILACIJSKO PREIZKUSNO STRUKTURO SC FILTROV

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Kjučne besede: oscilacijski preizkus, SC filtri, merilna točnost

Izvleček: Večina objavljenih prispevkov s področja oscilacijskega preizkusa je bila usmerjena v razvoj preizkusnih struktur in študij načinov preoblikovanja preizkušanega vezja v oscilator, malo pozornosti pa je bilo doslej posvečeno merilni točnosti samega preizkusa. V tem delu obravnavamo vpliv nelinearnosti komponent splošne Fleischer-Lakerjeva SC stopnje drugega reda na napako merilne metode in nakažemo možnosti za njeno zmanjšanje.

The Impact of Component Nonlinearities on Osillation Based Test Structure of SC Filters

Key words: oscillation based test, SC filters, measurement accuracy

Abstract: Oscillation based test has been applied to different kind of circuits including filters, A/D and D/A converters, PLLs, etc. The method is based on the assumption that the tested circuit can be reconfigured into an oscillator. The frequency of oscillation is measured and compared to a reference value obtained on a known-good circuit operating in the same conditions. Faults that manifest in the discrepancy from the reference oscillation frequency can thus be detected. So far, most of the papers on oscillation- based test have focused on the design of testability structures and circuit-reconfiguration schemes of individual classes of analog and mixed-signal circuits. Little attention has been paid to the measurement accuracy of the developed solutions. In this paper we address the issue of measurement inaccuracy of oscillation based test of a generic Fleischer-Laker biquad SC filter stage. Theoretical framework for the analysis of the impact of the non-ideal characteristics of circuit components on the resulting oscillation frequency is presented.

1. Uvod

V zadnjih letih je bilo objavljenih več prispevkov, ki obravnavajo uporabo oscilacijske metode pri preizkušanju aktivnih analognih filtrov /1/. Predstavljene so bile nekatere rešitve za izbrane razrede aktivnih R-C filtrov, ki temeljijo na pretvorbi preizkušanega vezja v oscilatorsko strukturo s pomočjo vgrajenih stikal in dodatnih pasivnih elementov /2/, ali pa z uporabo zunanjega vezja, /3/. Poleg tega naletimo tudi na nekatere rešitve, ki obravnavajo specifična aktivna R-C vezja, /4/, /5/, in dokazujejo praktično uporabnost postopka v proizvodnem preizkušanju integriranih analognih filtrov. Huertas et al. so v /6/ in /7/ predstavili oscilacijsko preizkusno strukturo SC filtrske stopnje. Na podlagi analize pokritosti napak so tudi pokazali, da je možno izboljšati kakovost preizkusa z dodatnim preverjanjem amplitude izhodnega signala. Splošne teoretske osnove načrtovanja preizkusljivih struktur časovno vzorčenih analognih SC filtrov za oscilacijsko preizkušanje so opisane v /8/ in /9/. Opisan je enostaven način transformacije SC filtrske stopnje drugega reda v oscilatorsko strukturo s pristopom, ki temelji na notranji rekonfiguraciji s pomočjo obstoječih ali dodatno vgrajenih stikal. Nakazana je tudi rešitev z uporabo zunanje nelinearne povratne zanke, ki omogoča boljši nadzor nad pogoji obratovanja vezja med preizkusnim postopkom in je uporabna tudi v integriranih vezjih.

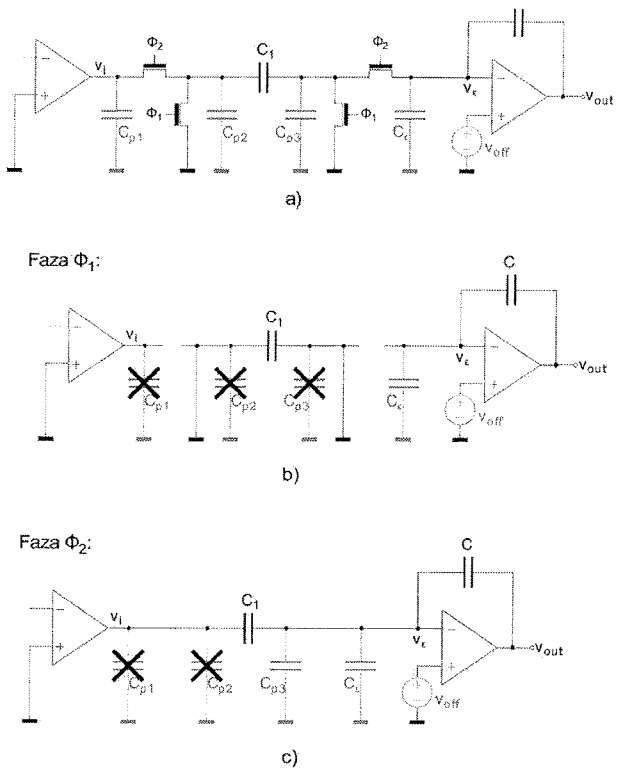
Rešitve predstavljene v /8/ in /9/ slonijo na predpostavki, da sestojijo SC vezja iz idealnih komponent. V praksi imamo opravka z operacijskimi ojačevalniki s končnim enosmernim ojačenjem in pasovno širino, kar lahko povzroči odstopanje dejanske karakteristike vezja od načrtovane. V integriranih vezjih predstavljajo precejšen problem tudi enosmerni odmiki v vhodnih stopnjah ojačevalnikov ter parazitne kapacitivnosti, ki nastopajo v različnih vozliščih vezja in so lahko, za razliko od diskretnih realizacij filtrskih vezij, po velikosti primerljive z namensko realiziranimi kondenzatorji v vezju. V tem prispevku obravnavamo vpliv nelinearnosti komponent na delovanje SC filtrskega vezja in na frekvenco oscilacij preizkusne strukture.

2. Analiza vpliva neidealnosti komponent na delovanje Fleischer-Laker bikvadratne SC stopnje

Za splošno Fleischer-Laker bikvadratno (FLB) SC stopnjo drugega reda je značilna neobčutljivost na parazitne kapacitivnosti, ki izhaja iz strukturne zasnove vezja /10/. To pa velja samo v primeru realizacije vezja z idealnimi operacijskimi ojačevalniki, saj lahko v tem primeru predpostavljamo, da so preklapljani kondenzatorji vedno umeščeni med idealni napetostni vir (izhod ojačevalnika) in pravo ali navidezno maso (invertirajoči vhod ojačevalnika).

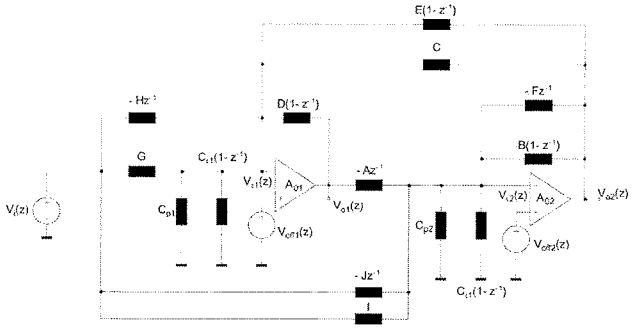
V predlaganih rekonfiguracijskih shemah za FLB stopnje za izvedbo oscilacijskega preizkusa, je potrebno v večini primerov v prvotno SC vezje vgraditi dodatna stikala, s katerimi dosežemo preoblikovanje vezja med preizkusom v oscilator. Z vsakim dodatnim CMOS stikalom vnesemo v vezje parazitne kapacitivnosti in dodatne vire šuma (presluh urinega signala), zaradi česar nas zanima njihov vpliv na delovanje filtrske stopnje v realnih razmerah. Slika 1a

prikazuje shemo invertirajočega SC integratorja, v kateri so predstavljene parazitne kapacitivnosti v različnih vozliščih vezja (C_{p1}, C_{p2}, C_{p3}, C_{p4}) medtem ko vpliv enosmernega odmika operacijskega ojačevalnika in signal šuma modeliramo s skupnim napetostnim virom v_{off}.



Slika 1: Vplivi parazitnih kapacitivnosti in signala šuma na SC vezje

V praktičnih realizacijah so operacijski ojačevalniki zaradi vzorčene narave SC vezij "predimenzionirani", zato lahko smatramo izhod ojačevalnika za dober približek idealnega napetostnega vira. Hkrati morajo biti tudi ostale komponente dimenzionirane tako, da so časovne konstante polnjenja kondenzatorjev veliko krajše od periode vzorčenja. Ob teh predpostavkah lahko brez večje napake zanemarimo vpliv parazitnih kapacitivnosti v določenih vozliščih, kot je prikazano na slikah 1-b in 1-c. Ugotovimo lahko, da bo odstopanje karakteristike SC vezja v pretežni meri odvisno od tistih parazitnih kapacitivnosti in virov šuma, ki se navezujejo na invertirajoče vozlišče ojačevalnika. Slika 2 tako prikazuje model FLB stopnje drugega reda z upoštevanimi neidealnostmi.



Slika 2: z-model FLB stopnje drugega reda z neidealnimi komponentami

Zaradi poenostavitve privzemimo, da smo z vgradnjo dodatnih stikal vplivali samo na invertirajoči vhod drugega operacijskega ojačevalnika. V tem primeru so se parazitne kapacitivnosti in šum stikala v tem vozlišču povečali za ΔC_p in ΔC_ε oziroma ΔV_{off}. Vpliv sprememb na prenosno funkcijo splošne FLB SC stopnje lahko opišemo z izrazom:

$$V_{o2} = -V_i \frac{DI-(DI+DJ-AG)z^{-1}+(DJ-AH)z^{-2}}{D(F+B)+\frac{1}{A_{02}}C_2-(2DB+DF-AC-AE+\frac{1}{A_{02}}C_1)z^{-1}+(DB-AE+\frac{1}{A_{02}}C_0)z^{-2}} + \Delta V_{off}H_o(z) \quad (1)$$

kjer so

$$H_0(z) = \frac{C_2 - C_1 z^{-1} + C_0 z^{-2}}{D(F+B)+\frac{1}{A_{02}}C_2-(2DB+DF-AC-AE+\frac{1}{A_{02}}C_1)z^{-1}+(DB-AE+\frac{1}{A_{02}}C_0)z^{-2}} \quad (2)$$

in

$$C_2 = D(B+F+I-\Delta C_p-\Delta C_\varepsilon) \quad (3)$$

$$C_1 = D(A+2B+F+I+J-\Delta C_p-2\Delta C_\varepsilon) \quad (4)$$

$$C_0 = D(A+B+J-\Delta C_\varepsilon) \quad (5)$$

Iz enačbe (1) je razvidno, da bo vpliv parazitnih kapacitivnosti zmanjšan za faktor enosmernega ojačanja operacijskih ojačevalnikov. To pri praktičnih vrednostih A_0 v območju od 1000 do 5000 in parazitnih kapacitivnostih, ki so za velikostni razred manjše od vrednosti komponent, pomeni, da lahko vplive ΔC_p in ΔC_e zanemarimo brez večje napake. Pri velikem A_0 lahko izraz (2) dodatno poenostavimo v:

$$H_0(z) \approx \frac{C_2 - C_1 z^{-1} + C_0 z^{-2}}{D(F+B)-(2DB+DF-AC-AE)z^{-1}+(DB-AE)z^{-2}} \quad (6)$$

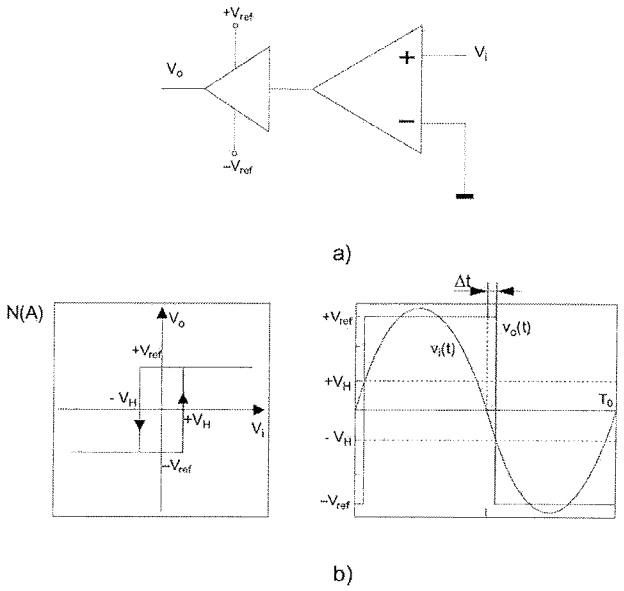
Očitno je, da v nasprotju s parazitnimi kapacitivnostmi, sama struktura FLB ne zmanjšuje vpliva šuma stikal oziroma enosmernih odmikov na vhodih operacijskih ojačevalnikov. V primerih, ko načrtujemo preizkusne postopke za SC filtre z visokim ojačanjem ali širokim dinamičnim območjem, je zato potrebno posebno pozornost posvetiti vnosu dodatnih motenj, ki bi v vezje med normalnim obratovanjem lahko vstopale preko vgrajene preizkusne infrastrukture.

3. Vpliv nelinearne povratne zanke na frekvenco oscilacij

Oscilacijski preizkus SC stopnje drugega reda z zunanjo povratno zanko temelji na uporabi nelinearnega elementa z neinvertirajočo oziroma invertirajočo karakteristiko. V integriranih vezjih je takšen element mogoče realizirati na dokaj preprost način z uporabo napetostnega primerjalnika. Za njegovo osnovo lahko uporabimo strukturo Millerjevega transkonduktančnega operacijskega ojačevalnika, iz katere odstranimo kompenzacijsko *RC* vezje, in na izhod

dodamo močnostno stopnjo z referenčno napajalno napetostjo (slika 3a). Če ojačevalnik v odprtozančni konfiguraciji povežemo z SC vezjem, dobimo na izhodu primerjalnika pravokotni signal, ki je v fazi s sinusnim signalom na izhodu SC stopnje.

V praksi se je pri realizaciji zunanje povratne zanke s primerjalnikom nemogoče izogniti zakasnitvam v poti signala. Po drugi strani je minimalna histereza v karakteristiki primerjalnika (slika 3b) celo zaželjena, saj preprečuje naključno preklapljanje izhoda zaradi šuma na vhodu primerjalnika. Ker je delovna točka oscilatorske strukture določena z izpolnitvijo Barkhausen-ovega pogoja, bo histereza z vnosom zakasnitve Δt oziroma faznega zamika ϕ_H vplivala na frekvenco oscilacij preizkušanega SC vezja.



Slika 3. Realizacija nelinearne povratne zanke

Če izrazimo signal na vhodu primerjalnika z

$$v_i = A\sin(\omega_0 t) = A\sin\Phi \tag{7}$$

je zakasnitev zaradi histereze primerjalnika enaka

$$\Delta t = \frac{\Phi_H T_0}{2\pi} \tag{8}$$

kjer je

$$\Phi_H = \arcsin(\frac{V_H}{A}) \tag{9}$$

Pogoj mejne stabilnosti sistema bo sedaj izpolnjen pri

$$\angle H(z) + \angle N(A) = 0 \tag{10}$$

Če uporabimo izraz za fazo prenosne funkcije *H(z)*

$$\Phi_H = \arctan(\frac{\mathrm{Im}[H(z)]}{\mathrm{Re}[H(z)]}) \tag{11}$$

in izraz za amplitudo signala A

$$A = \frac{4V_{ref}}{\pi}|H(z)| \tag{12}$$

kjer je

$$|H(z)| = \sqrt{(\mathrm{Re}\{H(z)\})^2 + (\mathrm{Im}\{H(z)\})^2} \tag{13}$$

lahko ob upoštevanju povezav med krožnimi funkcijami

$$\arctan(x) = \arcsin(\frac{x}{\sqrt{1+x^2}}) \tag{14}$$

izpeljemo izraz, ki omogoča določitev frekvence ω_{osc}

$$\mathrm{Im}\{H(e^{j\omega_{osc}T})\} = \frac{\pi V_H}{4V_{ref}} \tag{15}$$

Iz zadnje enačbe sledi, da se vpliv histereze primerjalnika na frekvenco oscilacij zmanjšuje z amplitudo izhodnega signala SC stopnje. Z izbiro takšne V_{ref}, ki v čim večji meri izkorišča celotno dinamično območje filtrskega vezja, lahko torej vplivamo tudi na zmanjšanje napake merilne metode. Na podlagi simulacij realnih primerov SC vezij in vrednostih V_H reda nekaj milivoltov se je izkazalo, da napaka meritve dosega do nekaj desetink odstotka, kar je seveda potrebno ustrezno upoštevati pri vrednotenju rezultatov preizkusa.

4. Zaključek

Večina objavljenih rešitev na področju oscilacijskega preizkusa se osredotoča na snovanje preizkusne strukture, ki spremeni vezja preizkušanca v oscilator. Malo pozornosti je bilo doslej posvečene merilni točnosti oscilacijskega preizkušanja. D. Vazquez et al. /11/ navajajo oceno merilne točnosti v splošnem primeru, ko so meritve oscilacijske frekvence izvedene z digitalnim števcem. V članku /12/ pa je opisana inherentna merilna netočnost oscilacijskega preizkusa analogno digitalnega pretvornika. V tem delu prispevamo teoretske osnove za vrednotenje rezultatov oscilacijskega preizkusa SC filtrov ob upoštevanju vpliva nelinearnosti uporabljenih komponent. Nakazan je način, kako lahko vplivamo na zmanjšanje napake merilne metode.

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MAGNETIC FIELD SENSITIVE ANTENNA DESIGN FOR HF BAND RFID SYSTEM

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Key words: RFID, Near field and far field, ISM band, Magnetic field sensitive antenna.

Abstract: Antenna designs are influenced by a range of matters, such as the region of label operation (near or far), the coupling field (electric field or magnetic field), the regulatory constraints and the environment in which they operate. Typically antennas used in the high frequency (HF) band RFID operate at 13.56 MHz whose frequency has an electromagnetic wavelength of around 22 m giving a near-field far-field boundary of around 3.5 m. A common practice of using a magnetic field-sensitive HF antenna suitable for operation in the HF ISM band (13.56 MHz).The label is designed to have a sufficient number of turns to provide the resonating inductance for the microcircuit input capacitance, as well as a flux collecting area in the interior, which is as large as practicable and consistent with the size requirement for the label. This paper presents a design method to optimize the RFID magnetic field sensitive antenna design with an EM simulation program Sonnet Lite manufactured by Sonnet Software Inc. The Sonnet Lite simulator program is very well known program for antenna design. A well designed RFID antenna can effectively reduce the system cost and improve the radio wave broadcast. Apart from that, communication range between tag and reader can be improved. In this project we have designed an antenna, where design has been done and verified its performance by simulation.

Načrtovanje antene občutljive na magnetno polje za RFID sisteme, ki delujejo na HF pasu

Kjučne besede: RFID, ISM frekvenčni pas, na magnetno polje občutljiva antena

Izvleček: Na načrtovanje anten za RFID sisteme vpliva veliko stvari, kot so zahtevana čitalna daljava (bližnje ali oddaljeno), sklopitveno polje (električno ali magnetno področje), zakonske omejitve in okolje, v katerem deluje. Antene, ki se uporabljajo v HF frekvenčnem pasu delujejo pri 13.56 MHz, oz. valovna dolžina je okoli 22m, kar omeji področje čitanja na okoli 3.5 m. Kartica je narejena tako, da ima zadostno število navojev, da omogoči resonanco z obstoječo vhodno kapacitivnostjo, kakor tudi, da omogoči zadosten pretok skozi navoj.

V prispevku predstavimo načrtovalsko metodo in programsko opremo, s katero optimiziramo geometrijo RFID antene. Dobro načrtana RFID antena lahko močno zniža stroške celega sistema in izboljša oddajno-sprejemni signal, oz. komunikacijo med kartico in oddajnikom.

1. Introduction

The history of Radio Frequency Identification (RFID) is old as far back as the 1920s with the birth of radar systems / 1/. The development of the technology, a combination of radar and radio broadcast technology, is messy and convoluted but there is consensus that it developed from the work carried out during WW-II to identify enemy aircraft, known as 'Identification: Friend or Foe' (IFF) systems.

The RFID systems use radio frequency waves to identify, locate, and track people, assets and animals when RFID tag is attached to them /2/. RFID systems composed of mainly two components a reader (or interrogator) and tag as shown if Figure 1.

Antennas used in the HF region operate at 13.56 MHz. Thus, given reading distance requirements of <3 m and using the regulated radiation power at the HF ISM band, reader antennas are almost always near-field creation structures that aim to create large energy density fields with the minimum amount of radiation. However, at UHF frequencies the scenario is different. At UHF frequencies, the near-field far-field boundary is around 50 mm. Thus the region of operation in the UHF spectrum is almost always in the far field, and therefore reader antenna designs are far-field creation structures that aim to operate at the highest possible efficiency.

The base station or reader continuously transmits an RF signal through its antenna while always watching for modulated backscattering signal. Once the tag has received sufficient energy to operate correctly, it begins clocking out its stored data that make to tuned and de-tuned the antenna circuit. As a result it causes amplitude fluctuation of antenna voltage across the antenna circuit. The reader detects the amplitude variation of the tag and uses a peak-detector to extract the modulation data. The most popular medium frequency band RFID system used 13.56 MHz frequency as carrier. Now the largest component of an RFID tag is obviously the antenna. However, the practical tag

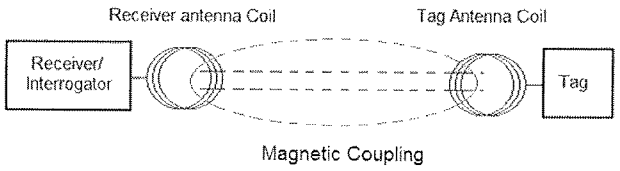

Fig. 1: Basic Block Diagram of RFID systems (near field)

has dimensions of only a few centimeters. These dimensions are very small compared to the wavelength and the radiation resistance is only few milliohms /3/.

Thus a 13.56 MHz RFID system cannot possibly radiate very well. It is essentially not an antenna. Some people refer to RFID reader as "couplers" /2//4/. This terminology is certainly quite appropriate in this case. We have indeed to consider the RFID system antenna plus tag, as a loosely coupled transformer, with reader antenna coil acting as a primary and the tag coil acting as the secondary of this transformer respectively.

2. Materials and Method

Designs are carried out in this project by used EM analysis software called Sonnet Lite version 11.55. Design method and calculations ware made by following the standard loop antenna design theory.

2.1 Designing of 13.56 MHz Antenna

The first step is to create an RFID inductor. Figure 2 (a) shows a typical RFID inductor.

a

b

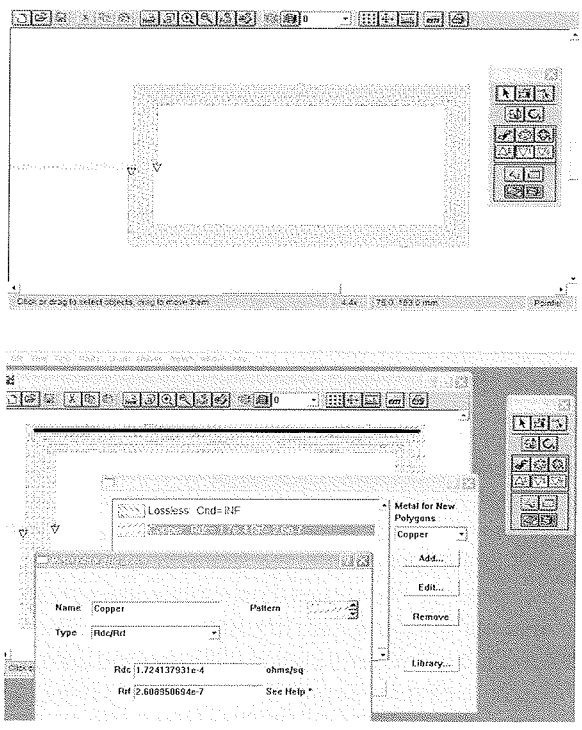

Fig. 2: (a) Designed RFID Planar Inductor (b) Metal Properties

It is a planar inductor with 6 turns, each 0.5 mm wide and separated by 0.5 mm. The coil has the dimensions are 78 mm × 41mm. Metal losses are taken into consideration during the design process. Since this analysis uses the Sonnet ABS interpolation, accurate data at 300 frequencies is calculated from electromagnetic analysis at only four frequencies.

By using the Sonnet Option Analysis, a lumped equivalent PI-model sub-circuit is generated. The output, shown here, is in PSPICE codes.

```
* Analysis frequencies: 12.1, 13.3 MHz
.subckt SON9_2 1 GND
C_C1 1 GND 1.185049pf
L_L1 1 2 4495.387nh

* Analysis frequencies: 13.3, 14.65 MHz
.subckt SON9_3 1 GND
C_C1 1 GND 1.198058pf
L_L1 1 2 4493.561nh
R_RL1 2 GND 1.859145
.ends SON9_3
R_RL1 2 GND 1.770104
.ends SON9_2
```

It shows that models are generated between two frequency bands. The first SPICE netlist is generated from data at 12.1 and 13.3MHz. The second SPICE netlist is generated from data at 13.3 and 14.65MHz. These PSPICE models are used to design the RFID antenna circuit.

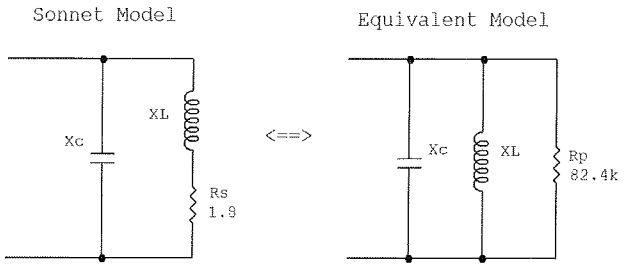

Fig. 4: (a) Sonnet Mode (b) Equivalent Model

Figure 4(a) is the direct Sonnet SPICE model and Figure 4(b) is its equivalent model. The generated lumped equivalent component for PI-model at 13.56 MHz frequency, the value of the capacitance is 1.2 pF and the inductance is 4523 nH. The series resistance of Rs =1.8 Ω is equivalent to parallel resistance /5/ Rp = 82.4 kΩ as shown Figure 4.

In this design we assumed that a typical 13.56 MHz RFID integrated circuit has capacitance 23.5 pF and internal resistance 25 kΩ. The simulated equivalent circuit is shown in Figure 5.

The RFID IC that has been used in this design has a total internal capacitance 23.5 pF. The distributed capacitance of the inductor is calculated by the Sonnet SPICE model is 1.2 pF. To make resonate an antenna coil of inductance 4523 nH with a frequency 13.56 MHz, total capacitance must be 30.6 pF /6/. So for the best matching between the tag (or reader) coil and the RF IC, an external capacitor 5.9 pF is calculated to tune the inductor at the frequency 13.56 MHz. The total impedance of the resonant circuit at resonance is the parallel combination of the internal resistance of the IC and the equivalent parallel resistance of the coil is 19.2 KΩ. This is the impedance that the RFID

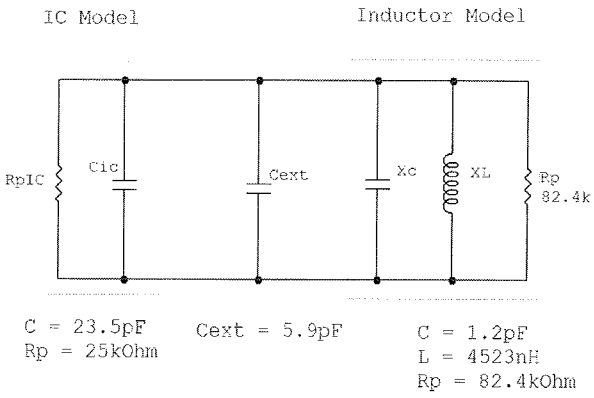

Fig. 5: Equivalent Model for IC and External Capacitor to Tune the Circuit

tag/reader IC will "see" at resonance. The nodal circuit analysis is accomplished for the complete RFID design by using Sonnet software.

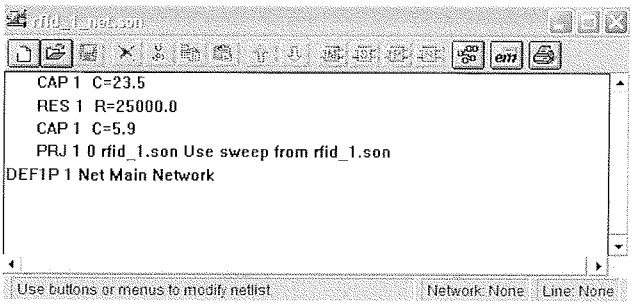

Fig. 6: Nodal Analysis for Complete RFID Circuit

In the Figure 6 the first two lines are showing the internal capacitance and resistance of the RFID chip respectively. The external capacitance is included in the third line. The fourth line begins with "PRJ". This includes the Sonnet project file for this inductor.

3. Simulated Result

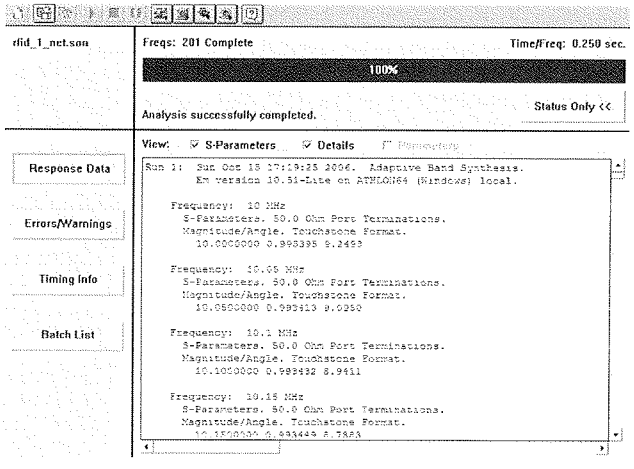

Fig. 7: Frequency Analysis Starts at 10 MHz

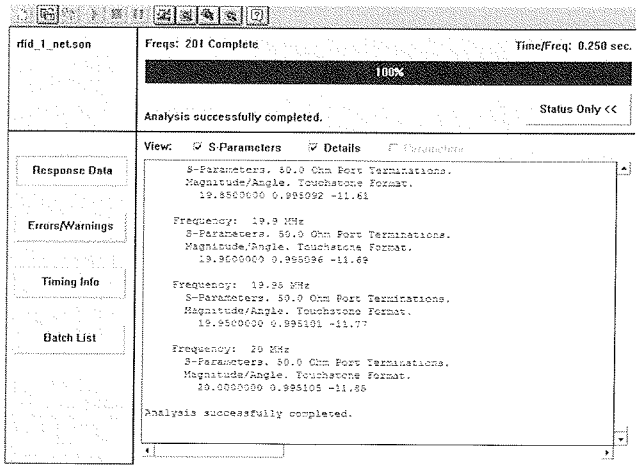

Fig. 8: Frequency Analysis Ends at 20 MHz

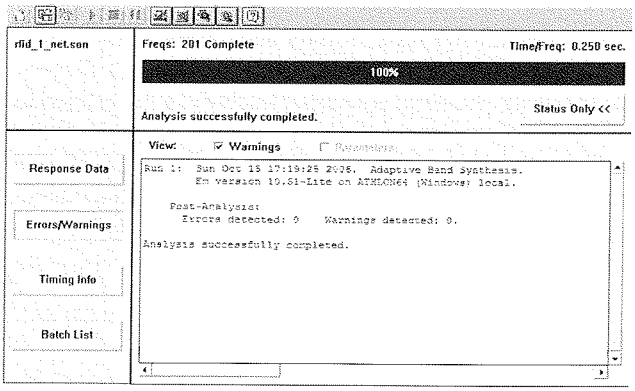

Fig. 9: Analysis Using 'Adaptive Band Synthesis' at a Rate of 0.25 Second

4. Result and Discussion

Figure 10 shows the graphical representation of the simulated result for the nodal analysis of RFID tag/reader. From this graph, it is clearly seen that the magnitude Z_{in} is maximum at the resonance frequency 13.56 MHz and same as the calculated value i.e. 19.2 kΩ. It is also seen from the graph that the imaginary part of the impedance at resonance frequency is close to zero.

For matching the antenna circuit with the RFID chip an external capacitor, *Cext*=5.9 pF is calculated and its position is shown in the Figure 5.

5. Conclusions

To verify the PSPICE results, lumped components value between two netlists near the frequency band of interest are compared and found the same result. In other words, the PSPICE model generated by Sonnet is working well for this circuit. Ones the data in the Sonnet project file is ready, it just reads the data and proceeds with the nodal analysis. If the layout has been changed the old data is no

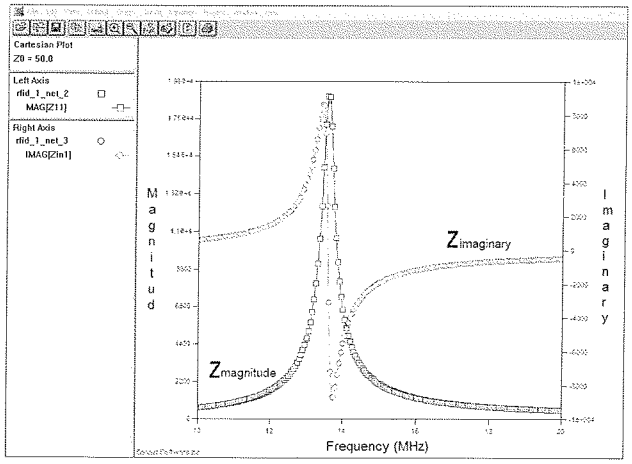

Fig. 10: Frequency Analysis Plotted in both Real and Imaginary

longer valid, in this case Sonnet calculates a new electromagnetic data automatically.To find the optimized parameter values of the RFID antenna matched to the conjugate of the RFID chip impedance, a design automation tool is very useful. The one of RFID antenna is successively optimized with this design optimization process. This method can be applied to any other applications with different simulation tools.

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DEKODIRANJE SIGNALOV V INTEGRIRANIH VEZJIH ZA RFID

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Kjučne besede: RFID, izpraševalnik, kartica, dekoder

Izvleček: predstavljen je pregled dekoderjev, uporabljenih v integriranih vezjih pri radijski frekvenčni identifikaciji (RFID) na HF (13.56 MHz) kakor tudi na UHF (860 MHz - 960 MHz) frekvenčnem področju. Pri istem standardu se za prenos podatkov med kartico (tag, transponder, target) in izpraševalnikom (reader, interrogator, initiator) ter v obratni smeri uporabljajo različni načini kodiranja. V prispevku je opis nekaterih dekoderjev, ki se uporabljajo v integriranih vezjih za kartice in izpraševalnike. Predstavljeni so načini kodiranja za različne standarde in nekateri osnovni principi dekodiranja signalov.

Signal Decoding in RFID ASICs

Key words: RFID, interrogator, reader, initiator, transponder, tag, target, decoder

Abstract: Review of decoders used for RFID is presented in this article. Described are methods how to decode signals which takes into consideration different ISO protocols on RF (13.56 MHz) and UHF (860 MHz - 960 MHz) frequency ranges. Data coding from transponder (tag, target) to interrogator (reader, initiator) and from interrogator to transponder is usually different and described decoders are implemented on ASICs for transponders and interrogators. Different ISO protocols enables many coding methods and basic principles from this article can be used for decoding of these signals.

1. Uvod

Radiofrekvenčna identifikacija (RFID) sestoji iz izpraševalnika in kartice, pri čemer sta izpraševalnik in kartica kompleksna integrirana sistema na čipu (SoC). Tovrstni integrirani sistemi so običajno mešana analogno-digitalna vezja ASIC, ki vsebujejo vrsto analognih sklopov, kot na primer /1/, /2/, /3/, /4/ in /5/ ter kompleksen digitalni kontrolni sistem na čipu, kamor štejemo tudi kodiranje in dekodiranje signalov. Kodiranje signalov pri RFID tehnologijah je v večini primerov določeno z mednarodnimi standardi. Na ta način je zagotovljena kompatibilnost med RFID karticami in RFID izpraševalniki, ki jih proizvajajo različni svetovni proizvajalci. Ob upoštevanju zgoraj omenjenih standardov v podjetju IDS d.o.o. načrtujemo RFID integrirana vezja za kartice in izpraševalnike /6/, /7/, /8/. S tem pristopom zagotavljamo, da so naši produkti kompatibilni z različnimi svetovnimi proizvajalci, ki standarde v celoti upoštevajo. V ogromni paleti ponudnikov integriranih vezij imajo nekatera vezja vgrajene kakšne specifične lastnosti, ki v posameznih aplikacijah olajšajo komunikacijo med karticami in izpraševalniki. Kadar je to ekonomsko upravičeno, tudi mi vgrajujemo takšne funkcije v naša integrirana vezja in s tem omogočimo proizvajalcem naprav, da z našimi integriranimi vezji sprogramirajo željene specifične lastnosti kartice ali izpraševalnika.

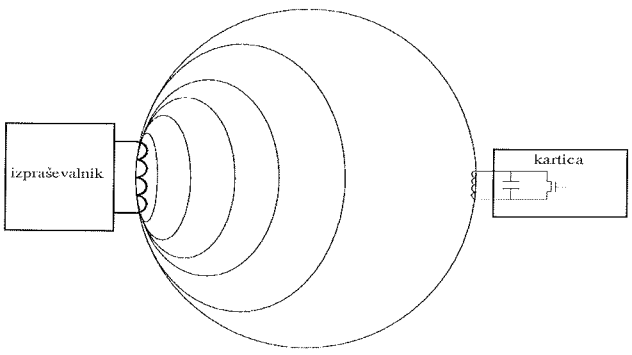
Signali, ki se uporabljajo pri kodiranju signalov v RFID komunikacijah, so večinoma iz naslednjih delov:

- pilotski ton
- preambula ali SOF (start of frame)
- podatki
- konec podatkov ali EOF (end of frame)

Pilotski ton se uporablja za sinhronizacijo vhodnega signala z referenčnim signalom. Le-ta omogoča delovanje dekoderja ob mirujočem vhodnem signalu in tudi takrat, ko so prisotne motnje. Po sinhronizaciji običajno sledi preambula za nastavitev začetka sprejemanja podatkov. V dekoderju se podatki dekodirajo in se v serijski obliki s pripadajočim urinim signalom pošiljajo v vezje, ki jih zloži v osembitne besede ter posreduje v ustrezne registre, kjer so na voljo kontrolerju. Le-ta upravlja s podatki in jih posreduje na ustrezna mesta. Na koncu podatkov je običajno dodana zaključna sekvenca. Takrat se niz podatkov zaključi in dekoder sporoči kontrolerju, da je dekodiranje sprejetih signalov končano. V primeru uspešnega sprejema je pri nekaterih standardih izvedeno še izračunavanje CRC (cyclic redundancy check) vrednosti in/ali paritete.

2. Osnove prenosa podatkov pri RFID

Ko se pojavi kartica v elektromagnetnem polju, ki ga povzroča antena izpraševalnika, se v njenem antenskem navitju inducira napetost. To napetost kartica usmeri in uporabi



Slika 1: Osnovni princip RFID.

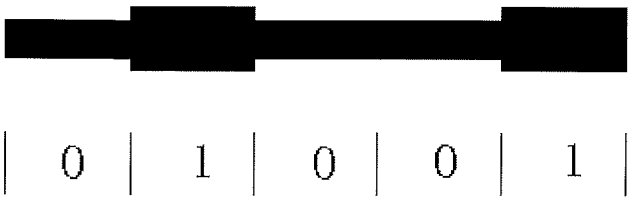
za lastno napajanje, prav tako pa iz nosilne frekvence ekstrahira svoj lasten urin signal, ki je nato osnova za frekvenco podnosilca. S tem podnosilcem so nato kodirani podatki in s tem kodiranim signalom moduliramo induktivni sklop med kartico in izpraševalnikom, le-ta pa detektira modulacijo na svojem nihajnem krogu.

Nosilna frekvenca v večini opisanih standardov je 13.56 MHz, frekvenca podnosilca pa je nekajkrat nižja in sinhrona z nosilno frekvenco in je odvisna od hitrosti prenosa podatkov v različnih standardih. Na UHF področju (860 MHz do 960 MHz) pa so pogoji nekoliko drugačni. Komunikacija poteka podobno po veljavnem standardu. Razlika je v tem, da urin signal na kartici ni ekstrahiran, pač pa ima vsaka kartica lasten oscilator, ki deluje v določenih tolerancah. Izpraševalnik pošlje kartici nastavitvene podatke, ki omogočajo uspešno komunikacijo, čeprav ni sinhronosti med nosilno frekvenco in podnosilcem. Znatne tolerance za frekvenco podnosilca in s tem povezane dolžine modulacijskih signalov so razlog za mnogo zahtevnejše načrtovanje dekoderjev za UHF kartice in izpraševalnike.

3. Dekoderji za različne standarde

3.1. NRZ decoder

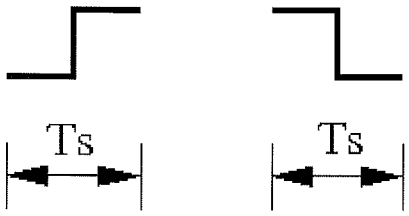
Kot najenostavnejša modulacija pri prenosu podatkov iz izpraševalnika do kartice se uporablja NRZ (non return to zero) kodiranje. V standardu 14443 tip B /9/ imamo enko takrat, kadar nosilec ni moduliran, ničlo pa, kadar imamo 10% modulacijo. V tem primeru startna sekvenca nastavi fazo takta za sprejem podatkov in demoduliran signal nam ob pravem taktu predstavlja logične ničle in enke.



Slika 2: NRZ moduliran signal.

3.2. Manchester decoder (FELICA, NFC)

Zelo razširjen način za prenos logičnih simbolov je uporaba Manchester kode. Logična simbola sta definirana tako, da sprememba logičnega stanja v sredini časovnega okna iz ničle v enko oziroma iz enke v ničlo pomeni logični simbol.



Slika 3: Osnovna simbola v Manchester kodi.

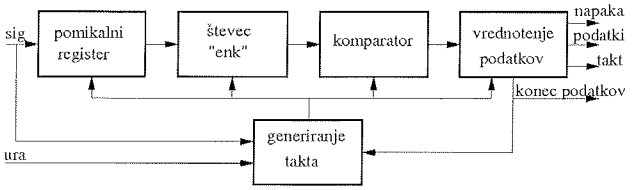
Standarda FELICA /10/ in NFC (near field communication) /11/ uporabljata tovrstno kodiranje na HF področju. Dekodiranje teh signalov poteka tako, da začetni pilotski ton sinhronizira fazo takta pri dekoderju in s tem nastavi okno za določitev vrednosti logičnega simbola.

3.3. Dekoder za modificirane Manchester simbole

Izpraševalniki uporabljajo to vrsto simbolov, ko sprejemajo signal iz kartice po standardu ISO 15693 /12/, ISO 14443A /9/ ali EPC /13/ (electronic product code).

Slika 4: Modificiran Manchester simbol za logično ničlo in logično enko.

Tem standardom je skupno, da je logična ničla sestavljena iz določenega števila impulzov in prav toliko časa trajajočo pavzo, ki se na RF signalu manifestira kot nemoduliran signal. Pri logični enki pavzi sledijo impulzi, ki modulirajo RF signal. Število impulzov in njihova dolžina je za prej omenjene standarde različna in znaša od 2 do 32 impulzov. Najbolj razširjena je komunikacija, kjer sta logična signala definirana z osmimi impulzi. Večje število impulzov pri določitvi logične enke oziroma ničle se uporablja v okoljih, kjer so večje radiofrekvenčne motnje in kjer je lahko hitrost prenosa manjša. Vedno večje hitrosti pri prenosu podatkov silijo snovalce mednarodnih standardov, da predpisujejo za logične simbole krajši čas trajanja in pri tovrstnih simbolih to dosežejo z manjšim številom impulzov. S tem pa se poveča vpliv motenj. Posamezni prej omenjeni standardi imajo različno definirane startne in zaključne sekvence, ki jih dekoderji uporabijo za pravilno zajemanje podatkov.

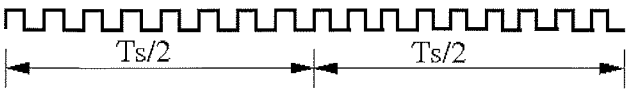


Slika 5: Blokovna shema dekoderja.

Vhodni signal se v pomikalnem registru pomika in na njegovem izhodu dobimo trenutno število impulzov. Števec jih šteje in posreduje komparatorju. Le-ta ima nastavljeno histerezo, ki omogoča pravilno dekodiranje tudi takrat, ko se na vhodu pojavijo motnje v obliki manjkajočih impulzov ali pa je med pavzo dodan kakšen impulz. Pri standardih, kjer logične simbole definira večje število impulzov, je lahko nastavljena večja histereza in s tem je narejena večja robustnost na motnje.

3.4. Dvofrekvenčni dekoder

Tudi tu gre za modificirane Manchester simbole, kjer je na sliki 6 prikazana logična ničla, logična enka pa je obrnjena /12/, /14/. V prvem delu simbola je osem impulzov frekvence fc/32, v drugem delu pa devet impulzov frekvence fc/28.

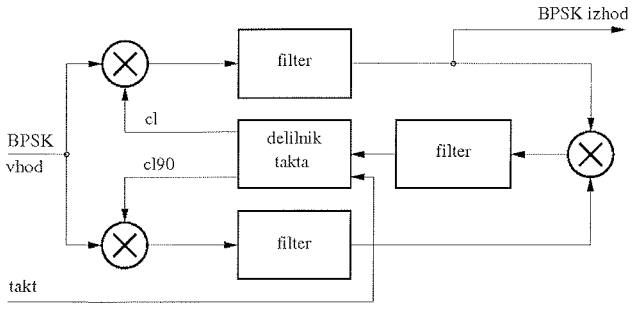


Slika 6: Dvofrekvenčni modificiran Manchester simbol.

Za dekodiranje takšnih signalov je potreben enostaven digitalni filter, ki odstrani impulze z višjo frekvenco. Na izhodu filtra dobimo identične signale, kot so že prikazani na sliki 4 in jih z enakim dekoderjem (slika 5) tudi dekodiramo. Pri teh signalih sta frekvenci impulzov za 14% različni, vendar kljub temu ni težav s filtriranjem impulzov z višjo frekvenco, ker sta frekvenci ure pri izpraševalniku in kartici enaki.

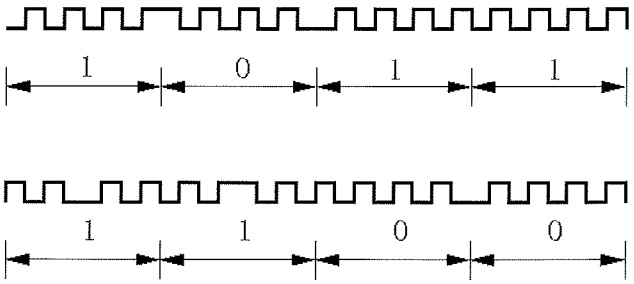
3.5. BPSK (binary phase-shift keying) dekoder

Osnovna BPSK modulacija je proces, kjer sta logična simbola medsebojno fazno zamaknjena za 180 stopinj, oziroma enostavneje povedano, da sta medsebojno invertirana. Tovrstna modulacija se uporablja na HF in tudi na UHF področju. Za dekodiranje teh signalov se uporablja modificirana Costasova zanka /15/, ki ima namesto napetostno krmiljenega oscilatorja uporabljen delilnik signala nosilne frekvence z možnostjo spremembe premika faze signala *cl* in *cl90* pri manjših faznih odstopanjih med vhodnim BPSK signalom in taktom *cl*. Ko pa so ta odstopanja večja, se delilniku spremeni v ustrezno smer tudi faktor deljenja. Modificirana Costasova zanka je predstavljena na sliki 7. Za pravilen start je pred podatki dodano določeno število impulzov, ki so potrebni za sinhronizacijo takta *cl* in *cl90*. Ti impulzi imajo isto fazo kot simbol "1", zato pomeni prvi fazni prehod logično ničlo.



Slika 7: Modificirana Costasova zanka.

Na HF področju se uporabljajo BPSK modulirani signali pri komunikaciji iz kartice do izpraševalnika (standard ISO 14443B) /9/. Osnovna hitrost prenosa podatkov pri osemimpulzni dolžini simbola je 106 kbit/s. Za povečanje hitrosti prenosa podatkov so standard dopolnili in omogočili hitrosti prenosa 212 kbit/s, 424 kbit/s ter 848 kbit/s. Ker pa je ostala frekvenca podnosilca enaka, so zmanjšali število impulzov za en simbol in sicer na štiri, dva in enega. S tem pa se je zmanjšala tudi odpornost na motnje. Dolžina BPSK simbola na sliki 8 je sestavljena iz štirih impulzov. Logična enka ima enako fazo kot podnosilec, logična ničla pa je za 180 stopinj fazno premaknjena. Prav tako pa je na UHF področju uporabljen dekoder v izpraševalniku za dekodiranje modificiranih Millerjevih signalov, definiranih v standardu ISO 18000-6 /16/. Tudi v tem standardu so simboli definirani z osmimi, štirimi ali pa dvema impulzoma.



Slika 8: BPSK signal (1011) in Millerjevo kodiranje (1100) s štirimi impulzi.

Po Millerjevem pravilu se za logično enko zgodi fazna sprememba na sredini simbola, za logično ničlo pa na koncu simbola. Dodatno je upoštevano še eno pravilo, ki ne dovoljuje fazne spremembe pri prehodu iz logične enke v logično ničlo. Dovoljene fazne spremembe se lahko nahajajo po eni, eni in pol ali dveh dolžinah simbola. Po dekodiranju z BPSK dekoderjem dobimo serijski niz podatkov s pripadajočim taktom. Ti podatki so še vedno zakodirani z osnovno Millerjevo kodo, prikazano na sliki 9.

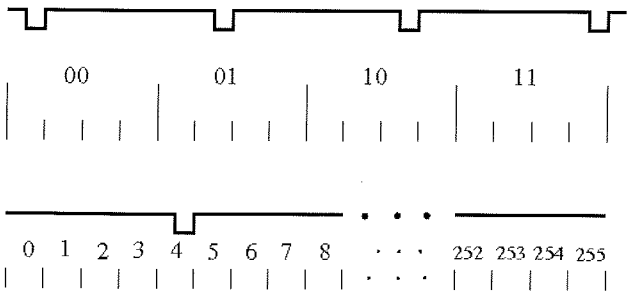
Slika 9: Kodirani podatki z osnovno Millerjevo kodo.

V zgornjem primeru služijo začetne ničle kot pilotski ton, biti 10111 pa kot preambula, ki določi začetek podatkov. Na začetne ničle se sinhronizira delilnik takta, ki ima glede na začetne podatke dvojno frekvenco. Generira se tudi takt, ki je zamaknjen za 90 stopinj in če se zgodi sprememba signala, kadar je le-ta v enki, dobimo logično enko, v vseh drugih primerih pa imamo logično ničlo.

3.6. 1/4 in 1/256 dekoder

To kodiranje se uporablja pri prenosu podatkov iz izpraševalnika na kartico. Princip kodiranja je takšen, da je pri načinu 1/256 osem bitov zakodiranih s pozicijo moduliranega signala v enem od 256 taktov /12/. Modulacija je izvedena tako, da je samo polovica periode modulirana, ostali čas pa je podnosilec prisoten. Pri signalih 1/4 pa je osem bitov sestavljenih iz štirih delov, kjer pozicija modulacije podnosilca predstavlja dva bita. Tudi v tem primeru je modulirana samo polovica periode, ki določa dva logična simbola. Na sliki 10 je prikazano kodiranje osmih bitov v

obeh načinih. Ker je širina modulacijskega impulza v obeh načinih enaka, je hitrost prenosa podatkov različna in znaša 26.48 kbit/s za kodiranje 1/4 in 1.65kbit/s za kodiranje 1/256. Preklop iz enega načina kodiranja v drugega določa izpraševalnik s startno sekvenco, ki je sestavljena iz dveh zaporednih impulzov, razdalja med njima pa določa način kodiranja.

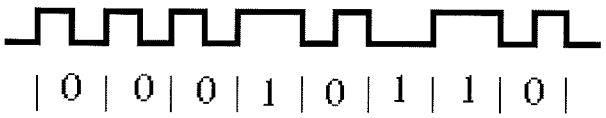


Slika 10:Primer kodiranja podatkov 1 / 4 in 1/256.

Dekodiranje teh signalov je sorazmerno enostavno in temelji na točnem taktu, ki ga kartica pridobi od izpraševalnika. Po prvi meritvi časa med dvema impulzoma se vezje odloči za enega od dveh načinov dekodiranja. V načinu 1/4 si nastavi časovno okno, ki je dolgo 16 period podnosilčevega takta. V tem času zajete podatke pomakne v pomikalni register, vsakih 16 taktov pa v izhodni register. Pri načinu 1/256 pa števec šteje takte v časovnem oknu, ki je dolgo 256 taktov. Ko pride do impulza, shrani vrednost preštetih taktov v osembitni register in ta vrednost je enaka kodiranemu podatku.

3.7. FM0 dekoder

Poleg večimpulzne Millerjeve kode se na UHF področju pri prenosu podatkov iz kartice do izpraševalnika uporablja tudi FM0 koda /16/.

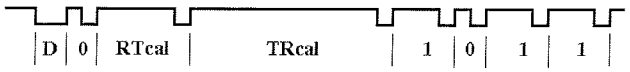


Slika 11:FM0 kodiranje osmih bitov.

Pri Millerjevi kodi nastopata dve dolžini impulzov. Značilnost te kode je, da je pri logični ničli sprememba v sredini simbola, logična enka pa ima ves čas trajanja simbola enako vrednost. Pri prehodu iz enega simbola v drugega pa se vedno spremeni tudi stanje. Tudi osnovni dekoder takšnih signalov je sorazmerno enostaven. Na začetku prenosa podatkov je 12 ničel, na katere se sinhronizira takt izpraševalnika. Na osnovi tega ugotavljamo fronto signala znotraj simbola. Če se le-ta pojavi, imamo logično ničlo, sicer pa gre za logično enko.

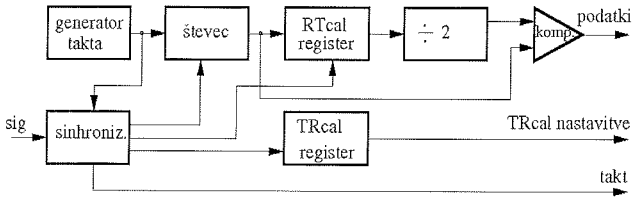
3.8. PIE (pulse interval encoding) dekoder

Nekoliko specifično je dekodiranje signalov na karticah na UHF področju. Ekstrahiranje takta iz nosilne UHF frekvence na kartici bi zahtevalo mnogo več energije kot pa na HF področju. Zato je uporabljena drugačna tehnična rešitev. Na kartici je oscilator s frekvenco 1.92 MHz. Ima tolerance, ki jih dekorer pri dekodiranju podatkov upošteva. Signali, ki prihajajo od izpraševalnika do kartice, so prikazani na sliki 12. Sestavljeni so iz preambule in podatkov /16/.



Slika 12:PIE kodiranje pri UHF kartici.

Prvi modulirani signal, ki ga kartica sprejme, je delimiter D, ki ima predpisano dolžino in sproži dekodiranje signalov. Delimitru sledi simbol za logično ničlo, imenovan tudi tari, ki predstavlja osnovno dolžino, s katero so določene dolžine tudi vseh ostalih simbolov. Tariju sledi simbol RTcal, njegovo trajanje pa je enako vsoti logične enke in ničle. Simbol TRcal ima informacijo za nastavitev frekvence podnosilca za oddajo iz kartice k izpraševalniku. Po uspešno sprejeti preambuli pa sledijo podatki.



Slika 13:Blokovna shema dekoderja za PIE signale.

Signal, ki pride v dekoder, ob začetku vsakega simbola postavi števec v začetno stanje. S časovno bazo, ki jo določa generator takta, izmerimo čas trajanja RTcal in TRcal simbolov ter ju shranimo v ustrezna registra. Vrednost registra, kjer je shranjen čas trajanja RTcal simbola, prepolovimo in uporabimo kot referenčno vrednost za dekodiranje logičnih ničel in enk. Ko prihajajo podatki, je izhod števca povezan direktno na digitalni komparator. Če stanje števca preseže polovično vrednost RTcal registra, dobimo na izhodu logično enko, v nasprotnem primeru pa logično ničlo. Ker je merjenje dolžine RTcal simbola opravljeno z istim taktom kot kasneje merjenje dolžin simbolov za enko in ničlo, frekvenčne tolerance takta ne vplivajo na rezultat.

4. Zaključek

V tem članku so opisane nekatere kode in načini dekodiranja, ki smo jih uporabili pri načrtovanju integriranih vezij za kartice in izpraševalnike v podjetju IDS d.o.o. Nekoliko podrobneje so prikazani zahtevnejši načini kodiranja, ki so tudi bolj odporni na motnje ter seveda načini, kako takšne signale dekodirati.

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SELF-HEATING COMPENSATION IN TEMPERATURE SENSOR RFID TRANSPONDERS

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Key words: RFID, data logger, voltage limiter, Smart Active Label.

Abstract: In this article we present the analysis and compensation of self-heating in a passive temperature sensor RFID transponder. The problem of heating due to the operation of the integrated voltage limiter can be observed in most RFID transponders. In temperature sensor RFID transponders this causes errors in the measured temperature, as the integrated sensor measures the IC temperature which is higher due to the operation of the voltage limiter. We propose a new algorithm of self-heating compensation with the use of an analogue to digital converter in the RF analogue front-end that measures the current level in the voltage limiter. The interrogator uses this value in the compensation equation that is presented in this paper.

Kompenzacija lastnega segrevanja pri merjenju temperature z RFID značko

Kjučne besede: RFID, podatkovni sledilnik, napetostni omejevalnik.

Izvleček: V članku je predstavljen vpliv lastnega segrevanja na točnost merjenja temperature z RFID značkami. Predstavljen je model segrevanja integriranega vezja RFID značke zaradi vpliva energije, ki se porablja v napetostnem omejevalniku v radijsko frekvenčni enoti. Prikazan je nov način kompenzacije lastnega segrevanja, kjer se kompenzacija izvede v RFID izpraševalniku. Predstavljeno vezje RFID značke ima v analogni radijsko frekvenčni enoti integriran analogno digitalni pretvornik za pretvorbo toka napetostnega omejevalnika. Izhodna vrednost tega analogno digitalnega pretvornika se, skupaj z digitalno vrednostjo temperature, pošlje RFID izpraševalniku. Kompenzacije se izvede v izpraševalniku na osnovi izmerjene temperature, vrednosti toka v napetostnem omejevalniku in časa prisotnosti RF polja.

1 Introduction

RFID (Radio Frequency Identification) is no longer considered to be a pure automatic identification technology. Due to the fact that the transponder is an electronic circuit (IC), it is possible to extend the functionality to other areas /1/, /2/, /3/, /4/.

This article deals with RFID transponders with integrated temperature sensors. The application areas of such systems are spread across all kinds of industries. Just to mention few, the first is the cold-chain industry, where a RFID tag with an temperature sensor can be used as a low-budget data logger. In medicine such tags can be used as permanent human body thermometers and in the automotive industry as a tire temperature indicator.

The advantage of using RFID technology in those applications is the wireless data transfer /5/, /6/, /7/ and even more important, the fact that, in passive RFID systems, the transponder does not need its own energy source. The problem we face in passive RFID transponders is the self-heating that is caused by the operation of the voltage limiter. The amount of self heating is dependant on the distance between the interrogator and transponder antennas and is such not predictable.

Chapter 2 describes the basic principle of passive RFID transponder power supply and the problem of self-heating. The new algorithm for self-heating compensation is presented in chapter 3. The IC heating model used in our analysis is presented in chapter 4. Measurement results and comparison with the model is in chapter 5. The conclusion is in chapter 6.

2 Passive rfid transponder supply

Passive RFID transponders are powered from the electromagnetic field that is generated by the interrogator /8/, /9/. The electromagnetic field induces an AC voltage over the antenna (Figure 1) and can be calculated with the following equation /9/:

$$u'_2 = \frac{j\omega k \cdot \sqrt{L_1 \cdot L_2} \cdot i_1}{1 + (j\omega L_2 + R_2)\left(\frac{1}{R_L} + j\omega C_2\right)}, \quad (1)$$

u'_2 – induced voltage on the IC pads,

k – coupling factor,

L_1 – interrogator antenna inductance,

L_2 – transponder antenna inductance,

R_2 – transponder antenna parasitic resistance,

R_L – transponder load (IC current drain),

C_2 – transponder parallel capacitance (C_p+C_L).

The real form of equation (1) is /9/:

$$u'_2 = \frac{j\omega k \cdot \sqrt{L_1 \cdot L_2} \cdot i_1}{\left(\frac{\omega L_2}{R_L} + \omega R_2 C_2\right)^2 \cdot \left(1 - \omega^2 L_2 C_2 + \frac{R_2}{R_L}\right)^2}, \quad (2)$$

The AC voltage is rectified by the transponder IC with a diode or transistor rectifier. The transponder antenna usually has a certain Q factor in order to boost the induced voltage and extend the reading and writing range:

$$Q = \frac{1}{R_2 \cdot \sqrt{\frac{C_2}{L_2}} + \frac{1}{R_L}\sqrt{\frac{L_2}{C_2}}} = \frac{1}{\frac{R_2}{\omega L_2} + \frac{\omega L_2}{R_L}}, \quad (3)$$

At longer distances the transponder benefits from the Q factor. At close proximity to the interrogator antenna this can cause that the induced voltage exceeds the maximum voltage defined by the technology /10/, /11/, /12/, /13/ . In modern CMOS technologies this is usually 2.5V, 3.6V or 5.5V.

For a reliable operation in a weak filed, further away from the interrogator antenna, and in a strong field, close to the interrogator antenna, the IC must have a possibility to lower its quality factor. Transponder IC manufacturers most commonly use a regulated voltage limiter that is composed of a transistor. At long distances from the interrogator antenna the induced voltage will be within the limits of the technology so the limiter transistor will be turned off completely and will drain no current. When the transponder moves closer to the interrogator, the induced voltage will rise to the point where it reaches the technology limit. At this point the limiter transistor will start to drain current from the rectifier, thus lowering the overall Q of the transponder. The current through the limiter transistor is therefore dependent on the distance between the interrogator and transponder.

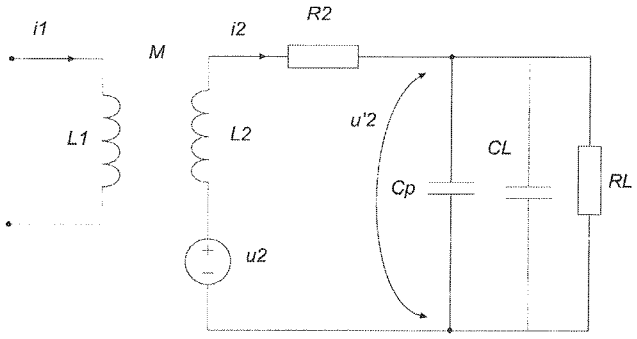

Fig. 1: Equivalent circuit of magnetically coupled interrogator and transponder. The left part shows the interrogator and the right part shows the transponder.

The excessive electromagnetic energy is converted to heat in the transponder voltage limiter causing a self heating effect /14/. This causes problems in transponders with an integrated temperature sensor, as the IC temperature will be higher than the environment temperature when the voltage limiter is active. This effect is not predictable as the amount of heat, that is generated by the voltage limiter, is dependent on the distance between the interrogator and transponder.

A solution to the above problem is presented in /14/. The author proposes to use a variable tuning capacitor integrated in the IC. The capacitance is regulated according to the value of the induced voltage, thus changing the resonance value of the antenna. After power-on the value of the capacitance is such, that the resonance frequency is equal to the carrier frequency. When the transponder moves closer to the interrogator and the value of the induced voltage rises, the value of the capacitance changes and de-tunes the resonant frequency. This consequently lowers the induced voltage, or rather, keeps it on a constant level, below the technology limit.

The above concept works on low and high frequency transponders (135kHz and 13.56MHz), but only to a certain level, as the value of the integrated capacitor can not be dynamically changed to any desirable level. Even more, this works only to a certain distance between interrogator and transponder, where the coupling coefficient *k* becomes too large. In this case the induced voltage can exceed the technology limit, even with a low Q value. In RFID systems in the UHF frequency range (900MHz) this approach is not feasible due to the fact that the IC capacitance has to be as low as possible to ensure the correct resonant frequency with a typical dipole antenna.

It is clear that a more robust and general approach needs to be used.

3 Self-heating compensation

Self heating presents a problem everywhere where temperature dependent parameters are crucial to observation or functionality of component. The easiest solution is to isolate and separate heat sources and thermal sensitive components. In our case, where we have everything integrated on a single silicon die. We can move the heat source

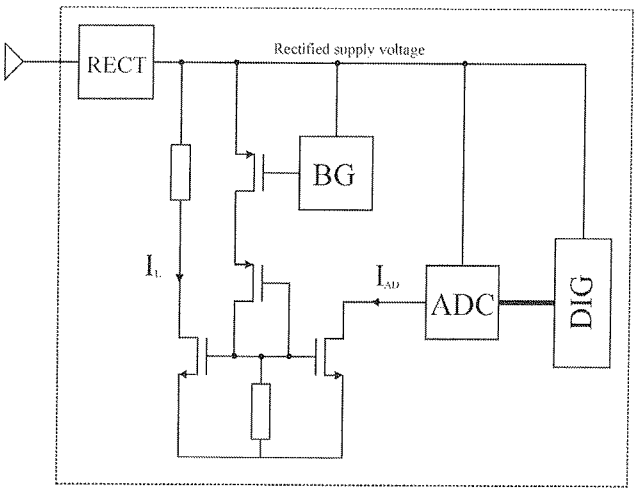

Fig. 2: Analogue front end with current limiter AD converter. RECT - RF rectifier, BG - band gap reference, ADC - current balancing analogue to digital converter, DIG - RF digital circuit.

far away from the temperature sensor, but this is not always possible. Sometimes components can be made invariable to temperature changes (0 TC resistors, bandgap reference voltages /15/, /16/). When temperature dependent resistors are used (Pt1000), the manufacturer usually provides data about self heating or some way of compensation to get real results.

We found ourselves in front of a unique problem, when we want to measure the temperature of surrounding air and not temperature of surrounding air plus temperature difference caused by heat source on silicon. We can ignore the self heating of temperature sensor caused by the excitation current, because the sensor is excited for brief moments (2ms) and the current passing trough the sensor is very small (a few μA). The heating of temperature sensor is caused by the current flowing into the voltage limiter. The heat source and the temperature sensor are placed far apart on the silicon die (Figure 3).

We have introduced a new method of compensation that takes part in two stages. We have to measure the duration of power dissipation and the power dissipated on heat source (voltage limiter). Time of power dissipation is measured in the RFID reader, since it has control over the RF field. When the RFID tag is powered it can measure the sink current and convert it to a digital value (Figure 2). A part of the limiter current I_L is fed to the current balancing AD converter (current I_{AD}). The output code is then back scattered to the RFID reader, together with the temperature value, where the actual compensation is done.

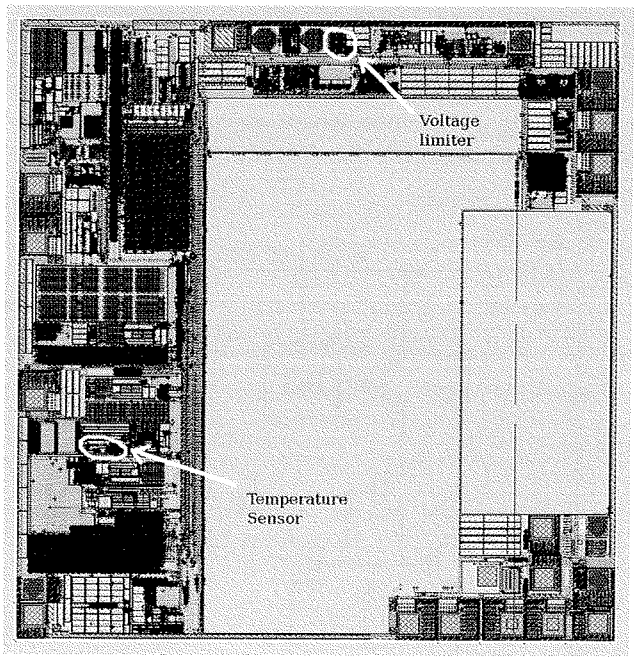

Fig. 3: Temperature sensor RFID transponder IC layout view. The digital circuits are not shown.

Since our heat source is a voltage limiter its voltage is constant. Therefore we can calculate how much power is dissipated with the information on the voltage limiter current level. Now that the RFID reader has all information about time and power (current), it can calculate temperature error and subtract it from the measured value. In this method of compensation we assume a time invariant power dissipation in the voltage limiter. This demands a constant distance between the reader antenna and the transponder antenna during temperature conversion. The temperature rise as the effect of self heating is calculated with the following equation:

$$\Delta T = T_s \cdot \left(1 - e^{-\frac{t}{R_T C_T}}\right), \quad (4)$$

T_S – stable state temperature,

τ – time constant.

We can write the above equation as:

$$\Delta T = P \cdot R_T \cdot \left(1 - e^{-\frac{t}{R_T C_T}}\right), \quad (5)$$

P – power in voltage limiter,

R_T – characteristic thermal resistance,

C_T – characteristic thermal capacitance.

The R_T and C_T values can be determined either with measurements or analytically.

It is also possible to implement this compensation algorithm for the case where we can not assume a constant distance between the interrogator and transponder, but a more sophisticated software is required on the interrogator side.

4 IC heating model

Heat transfer occurs when a heat gradient is present in an object or between objects. Every object or medium with mass has a tendency to establish a thermal equilibrium with the adjacent object.

Heat transfer occurs in three different ways:

- conduction – heat transfer trough solids,
- convection – heat transfer trough liquids or. gases,
- radiation – heat transfer to distant object trough electromagnetic waves.

In describing thermodynamic events we relay on two basic laws, firs and second law of thermodynamics. The first law states that energy can be transformed (changed from one form to another), but cannot be created or destroyed. Therefore, increase in the internal energy (U) of a system is equal to the amount of energy added by heating (Q) the system minus the amount lost as a result of the work(W) done by the system on its surroundings.

$$dU = dQ - dW, \quad (6)$$

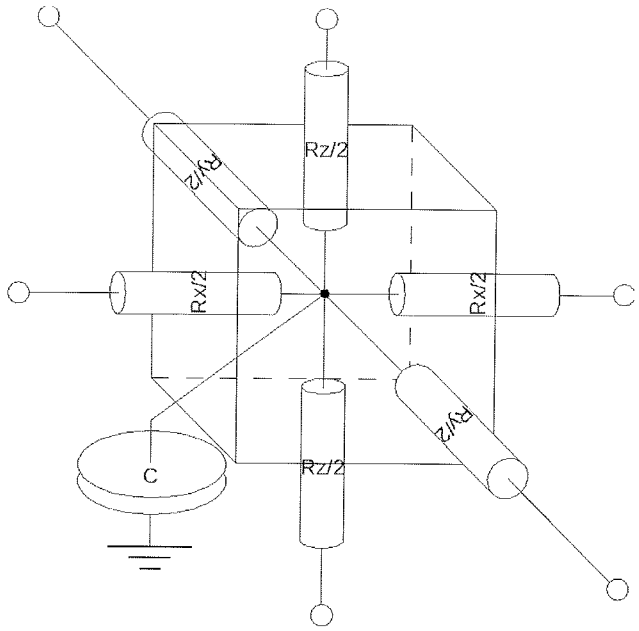

Fig. 4: Single cell finite state multi nodal model

The second law of thermodynamics states that the entropy of an isolated macroscopic system never decreases; that the entropy (S) of an isolated system which is not in equilibrium will tend to increase over time, approaching a maximum value at equilibrium.

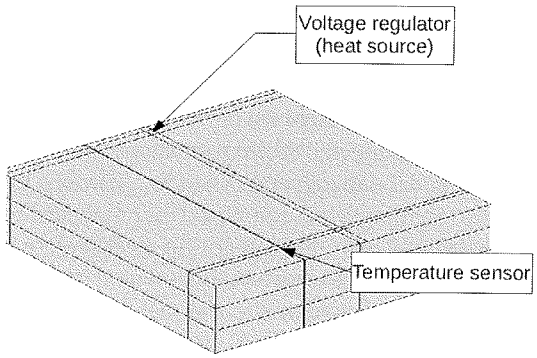

Fig. 5: Transponder IC silicon model

There are many methods of modeling thermal processes /17/, /18/, CFD (Computational Fluid Dynamics), ND (Nodal method), Zonal modeling. In our case we are modeling the transponder IC encapsulated in 20 pin DIL housing and the transponder IC glued directly to a PCB. Our goal is to predict heat gradient over IC on which a temperature sensor and a heat source are located. The heat source is a voltage limiter that modulates load on the rectified RF signal. Heat transfer trough solids is done with conduction so the temperature of air surrounding the housing is not in interest of observation. We can therefore simplify our model and ignore heat radiation. Natural heat convection is only present at contact surfaces of IC. The simplest method to use in this case is nodal method extended to multinodal method. Each node in model presents small piece of silicon with homogenous temperature its thermal capacity C_T and thermal resistance R_T in all three directions (Figure 4). This is also known as finite state model.

$$C_T = c \cdot m \left[\frac{J}{K}\right], \tag{7}$$

Where C_T is thermal capacitance /J K^{-1}/, c is specific thermal capacity /J kg^{-1} K^{-1}/ and m is mass /kg/.

$$R_T = \frac{l}{k \cdot S}\left[\frac{K}{W}\right], \tag{8}$$

Where R_T is thermal resistance in the direction of heat transfer /K W^{-1}/, l is length in the direction of heat transfer, k is thermal conductivity /W m^{-1} K^{-1}/, S is the area perpendicular to the direction of heat transfer /m^2/.

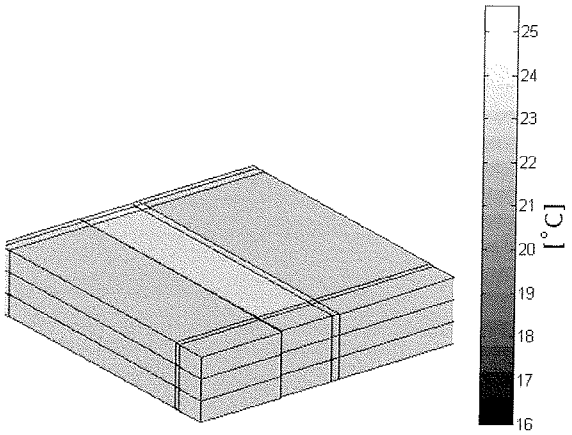

Fig. 6: Cell temperature gradient

The nodes that are positioned on outer edges of silicon have contact with the surrounding air. Since the heat escapes from the silicon die to air with convection, the heat transfer coefficient (h) of air must be taken into account. Typical values of the air heat transfer coefficient are from 10 to 100 W m^{-2} K^{-1}. The heat transfer coefficient is greatly dependent of the direction of moving air. Planes poisoned vertically have greater heat transfer coefficient than planes positioned horizontally.

$$R_{conv} = \frac{1}{h \cdot S}, \tag{9}$$

where R_{conv} is thermal resistance of air /K W^{-1}/, h is heat transfer coefficient /W m^{-2} K^{-1}/ and S is area of contact with air /m^2/.

At the bottom side of the IC, where silicon is attached to the ceramic housing, thermal resistance and capacitance of the housing needs to be added to equations. Ceramic material in general has a high thermal resistance and a large thermal capacitance. We also made a model where the IC is attached directly on the PCB and covered with a plastic mass. The model of silicon die is the same as in previous case, except there is no natural heat convection directly on the surface of silicon. All heat transfer is done trough conduction. Since plastic material have a high thermal resistance (much higher than air - h ~ 0.3W m^{-1} K^{-1}), we can neglect the thermal resistance of surrounding air.

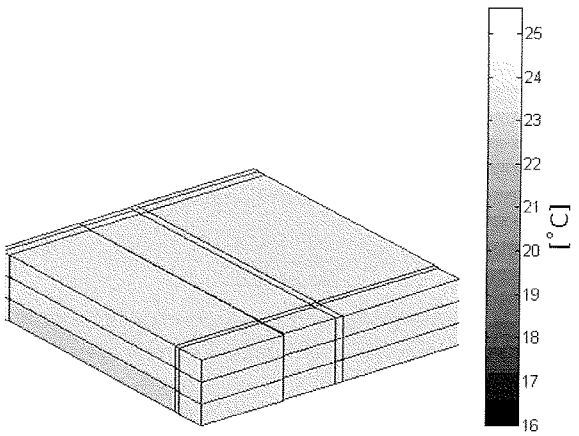

Fig. 7: Settled cell temperature

We expect to see that an IC in ceramic housing won't heat as fast and not as hot as an IC mounted directly on PCB, since the mass of housing and contact area with surrounding air is greater than that on IC mounted on PCB.

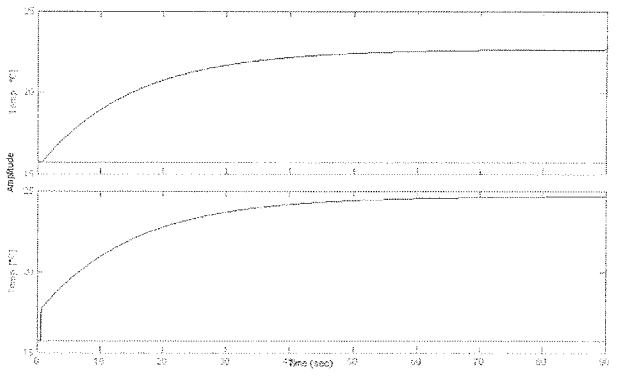

Fig. 8: Step response plot

Top - sensor cell response,

Bottom - heat source response (voltage limiter cell).

In the model all cells have all properties calculated, but not every property is always used. The properties are used when they are needed in relation to a position of cell. That way process for automatic calculation of cell properties is simpler. In Figure 9 properties of cell # 35 are shown. The ambient temperature for simulation was set to 15,73 °C and power dissipation from heat source was 33 mW. The heat source was turned on after 0,6 seconds. Figure 6 shows the current state of a cell's temperature after 30 seconds. The same data is shown in Figure 7 after 90 seconds. In Figure 8 the temperature of the heat source cell and temperature sensor cell are shown in relation to time.

5 Results

The model of an IC glued to the PCB predicts a rise of temperature for about 6°C in the area where the temperature sensor is located and with a simulated voltage limiter

```
cell(35):
        start: [0.0014 2.9100e -004 2.5000e-004]
    dimension: [0.0012 5.2000e -005 2.5000e-004]
       center: [0.0020 3.1700e -004 3.7500e-004]
       volume: 1.5613e -011
          cap: 5.1657e -004
          res: [710.6509 1.3322 30.7929]
      resconv: [7.6923e+004 3.3306e+003
8.0061e+004 1.6012e+005]
```

Fig. 9: The model values of cell #35.

current drain of 10mA (Figure 10). This temperature rise is caused by the heat source located on silicon. Ambient temperature was set to 15,73 °C and the heat source to dissipate 33mW (3,3V and 10mA) of heat.

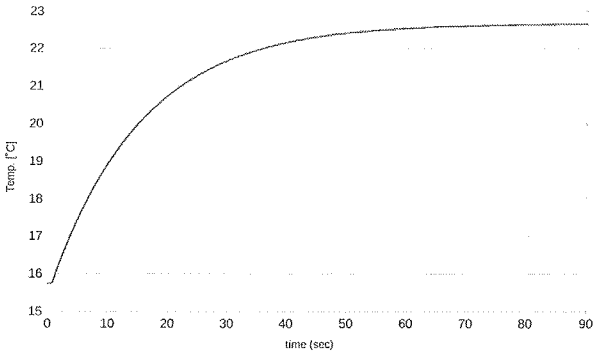

Fig. 10: IC model step response with 33mW heat dissipation.

From the computed results we can calculate the time constant τ, the characteristic thermal resistance and the characteristic thermal capacitance. The characteristic thermal resistance represents the combined thermal resistance of an observed cell with respect to the temperature difference to environment and the dissipated heat from the heat source (10). The characteristic thermal capacitance represents the combined thermal capacitance effect of an observed and all adjacent cells.

$$R_T = \frac{T_{observedcell} - T_{ambient}}{P_{heatsource}}, \quad (10)$$

$$\tau = R_T \cdot C_T, \quad (11)$$

For the model of IC glued to the PCB we can compute the characteristic values:

R = 209,393 K/W,

C = 0,047 J/K,

τ = 9,85 s.

We can easily measure the value of 5τ (time it takes for the temperature to rise from ambient temperature to 99.3 % of final-stable temperature) and then calculate value of τ and the characteristic thermal capacitance. The measurement can be done by forcing a known current value to the antenna pads of the transponder. The current flows to the voltage limiter thus consuming power and causing heat-

ing. As the transponder IC has an integrated temperature sensor the temperature measurements can be done by the chip itself. We used a sampling time of 200ms (Figure 11).

Measurements (*Figure 11*) gave the next results:

R = 139,946 K/W,

C = 0,066 J/K,

τ = 9,2 s.

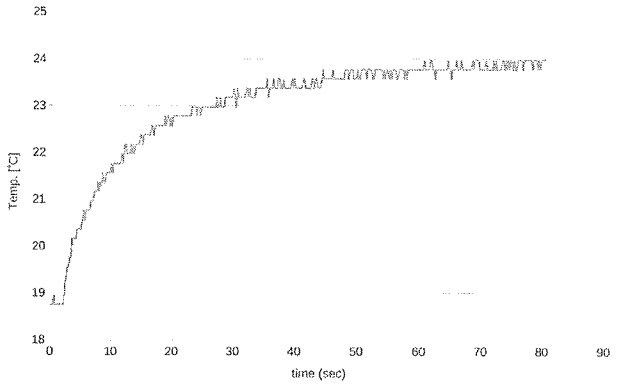

Fig. 11: Measured step response with a constant voltage limiter current drain of 10mA (37.3mW).

Since the model was simplified in many ways some differences between model and measurements were expected. The time constant τ has a difference of 0,65 seconds. Since the whole process of heating takes around 90 seconds, this error is minimal. A somewhat larger difference appeared in the calculation of characteristic resistance and capacitance. The modeled thermal resistance is larger than the measured and thus the temperature in an observed cell is slightly higher. A more detailed model of natural thermal convection would give a more accurate thermal resistance. The same is valid for thermal capacitance. In the model we neglected the PCB and it's mass that was not in direct contact with the IC.

The characteristic of the voltage limiter current analogue to digital converter is on Figure 12.

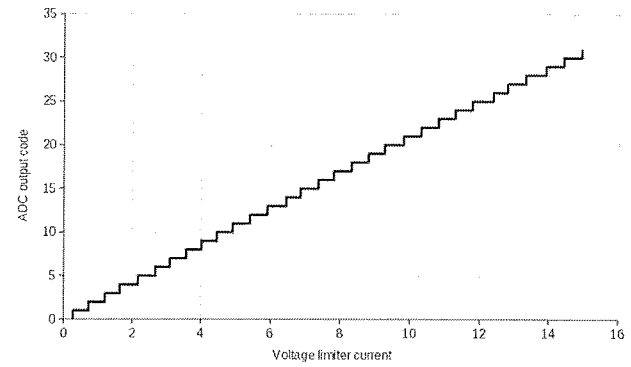

Fig. 12: Voltage limiter current ADC measurement

As an example we can now use the equation (5) to calculate the effect of self heating after 1 second:

$$\Delta T = P \cdot R_T \cdot \left(1 - e^{-\frac{t}{R_T C_T}}\right) =$$

$$= 0{,}0373 \cdot 139{,}946 \cdot \left(1 - e^{-\frac{1}{139{,}946 \cdot 0{,}066}}\right) = 0{,}536K \qquad (12)$$

We can see that the transponder will heat up for 0,536 °C in 1 second in a RF filed that causes a current of 10mA in the voltage limiter.

6 Conclusion

The algorithm for self heating compensation presented in this paper is suitable for RFID transponders with an integrated temperature sensor and also for RFID transponders with other sensors that have high temperature dependence. The characteristic temperature resistance and temperature capacitance that is required by the algorithm needs to be determined for a particular silicon die, IC package or IC mounting technology. We have presented a model for the transponder in a ceramic package and for the transponder glued directly to a PCB. We have shown that the required parameters can be determined either analytically or with measurements and that both have very similar results.

The compensation equation has an exponential dependence, therefore it is not directly suitable for the implementation in a low cost microcontroller. For such applications we propose to use a look-up table for the calculation of the amount of self heating. The equation can be simplified if the RF field is active for a predetermined amount of time before the temperature measurement is done. In this case the exponential factor becomes a constant value and the only variable remains the power (current flowing to the voltage limiter). In our case, where we have a 5-bit voltage limiter current AD converter, we require a look up table with only 31 values.

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AUTOMATIC SCREWING OF CAPS TO SPIKE CONNECTORS ON APD PERITONEAL DIALYSIS LINES

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Key words: hemodialysis, peritoneal dialysis, APD, CAPD, manual caps screwing, automatic caps screwing,

Abstract: Around 3 million people worldwide with end stage renal disease regularly need to use one of the established dialysis methods. The most common is haemodialysis but less invasive is peritoneal dialysis where peritoneum takes the role of artificial kidney /1/.

Using APD - Automatic peritoneal Dialysis, PD dialiser executes the whole cycle of successive charging and dialysis fluid discharging during the night. Connection of lines, solutions and patient to PD dialyser is done by use of connectors which are protected with caps that must be unscrewed sterilly before use. In the production of disposable PDL lines the caps are screwed to connectors manually or automatically. Automatic screwing guarantees controlled and repetitive screwing conditions, as well as higher throughput. In the article we describe such a machine that we built. It is fully automatic and needs to be occasionally refilled with material and reset to define new material lot. Process, as well as production, parameters are put-in through user friendly touch screen.

Avtomat za vijačenje kapic na konektorje linij za avtomatsko peritonealno dializo

Kjučne besede: hemodializa, peritonealna dializa, APD, CAPD, ročno vijačenje kapic, avtomatsko vijačenje kapic,

Izvleček: Dandanes se je nekaj manj kot tri milijone bolnikov s stalno ledvično odpovedjo prisiljeno redno zatekati k eni od uveljavljenih metod dialize. Gre bodisi za hemodializo, oz.krvno dializo, kjer bolnika trikrat tedensko priključimo na umetno ledvico, ali pa za peritonealno dializo, kjer vlogo (umetnih) ledvic prevzame bolnikova potrebušnica, peritonej /1/.

Pri kontinuirani peritonealni dializi (CAPD - Continuous Ambulatory Peritoneal Dialysis) bolnik štirikrat dnevno ročno prazni in nato polni močno prekrvavljeno trebušno votlino z ustreznimi raztopinami. Pri avtomatski peritonealni dializi (APD - Automatic peritoneal Dialysis) pa to funkcijo prevzame PD dializator.

Priključitev linije in vrečk z raztopinami na dializator bolnik opravi s pomočjo ustreznih konektorjev. Le-ti so zaščiteni s čepki, ki jih mora bolnik predhodno pazljivo sterilno odviti.

V proizvodnji dializnih linij za enkratno upoprabo se vijačenje čepkov na konektorje izvaja ročno ali avtomatsko. Ročno vijačenje ima določene slabosti, kot so:

- nekontroliran navor privijanja, ki posledično lahko povzroči težave bolniku pri odvijanju, če so čepki preveč priviti ali pa netesnost linije, če so čepki premalo priviti
- dolgotrajno ročno privijanje zaradi ponavljajočih se gibov lahko povzroči bolečine v prstih in rokah delavcev.

Avtomatsko privijanje na drugi strani zagotavlja kontrolirane pogoje privijanja in višjo produktivnost. Delovanje avtomata je v veliki meri samodejno, saj ga je potrebno le občasno posluževati z materialom, kakor tudi vnašati proizvodne parametre za posamezne lote materiala. V prispevku opišemo konstrukcijo in delovanje avtomata za privijanje čepkov. Po začetnem testiranju je naprava začela delovati v proizvodnji ter dosegla vse planirane parametre : kapaciteto nad 8.000 privijanj/izmeno ter navor privijanja v željenem oknu od 3Ndm do 8Ndm.

1. Introduction

Around 3 million people worldwide with end stage renal disease need to regularly use one of the established dialysis methods. The most common is haemodialysis, which needs to be done three to four times a week where the patient is dialysed by use of artificial kidney. Less invasive is peritoneal dialysis where peritoneum takes the role of artificial kidney /1/.

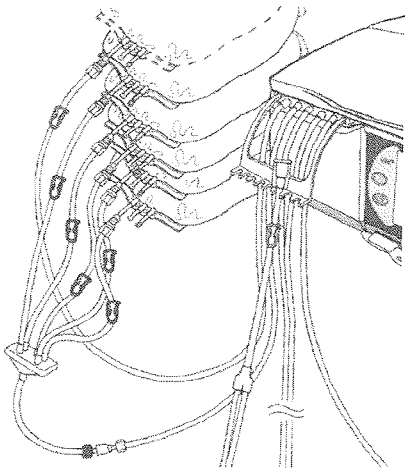
Using CAPD - Continuous Ambulatory Peritoneal Dialysis, the patient needs to manually discharge and charge the peritoneal cavity four times a day with suitable solutions. On the other hand with APD - Automatic peritoneal Dialysis, PD dialiser takes over the whole cycle of successive charging and discharging during the night.

Connection of lines, solutions and patient to PD dialyser is done by use of suitable connectors, figure 1 and figure 2. These connectors are protected with caps which must be unscrewed sterilely before use. Cap colour defines to which type of dialysis solution the line connector must be connected to.

In the production of disposable PDL lines the caps are screwed to connectors manually. Manual screwing has several disadvantages like:

- uncontrollable screwing torque which may lead to problems during cap unscrewing by patient due to too tight force, or on the other hand, leakage of the whole line due to too light force
- continuous repetitive manual screwing may cause operator finger and handaches.

a



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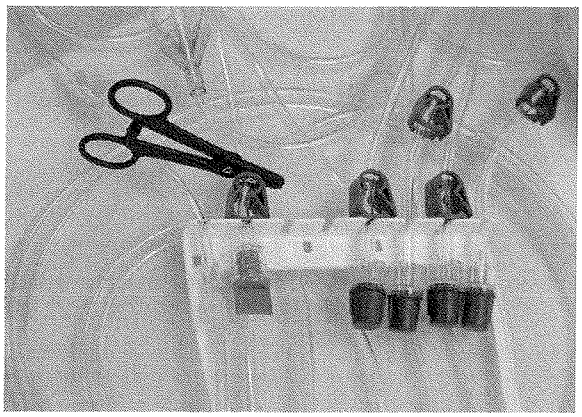


Fig. 1: a) connection of APD line to solution bags; b)Part of an APD line with five connectors

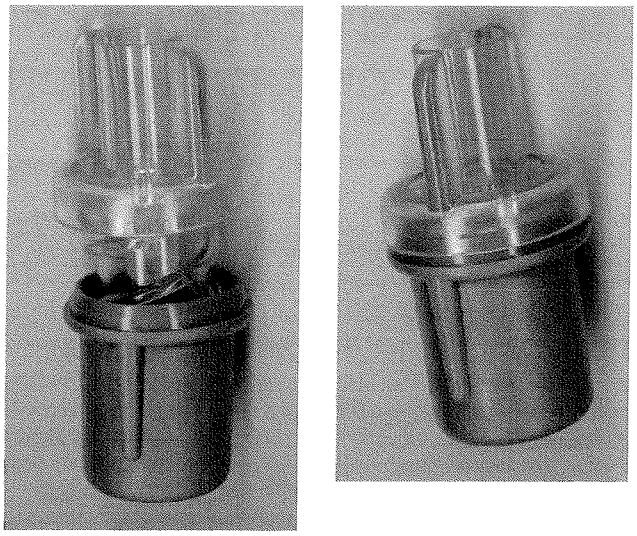
Automatic screwing guarantees controlled and repetitive screwing conditions, as well as higher throughput. The machine is fully automatic and needs to be occasionally refilled with material and reset to define new material lot. Process, as well as production, parameters are input through user friendly touch screen.

2. Machine design

2.1 General

The idea was to construct a machine that could replace a human operator for screwing caps onto connectors of PDL lines. Torque should be controlled within the broad range of 1 Ndm to 10Ndm with central value of 5±1 Ndm. Machine capacity should be more than 8.000pcs/shift.

Basically the machine consists of the ***cap feeding system*** which feeds the caps to the ***cap transport mechanism.*** When caps arrive close to the holder the ***cap feeding arm*** takes the caps and puts them into the ***screwing holder.*** On the opposite side of the machine connectors are fed from ***connector feeding system*** which feeds connectors to the ***connector transport mechanism***. When connectors arrive close to the holder the ***connector feeding arm*** takes the connectors and puts them into the ***screwing holder. Three screwing heads with motors*** are downloaded to screw the connectors onto the caps by using appropriate software driven algorithm. Once screwed, the holder opens and connectors with cap fall into the material box.



a b

Fig. 2: a) cap (bottom) and spike (up) separated; b) cap screwed on spike

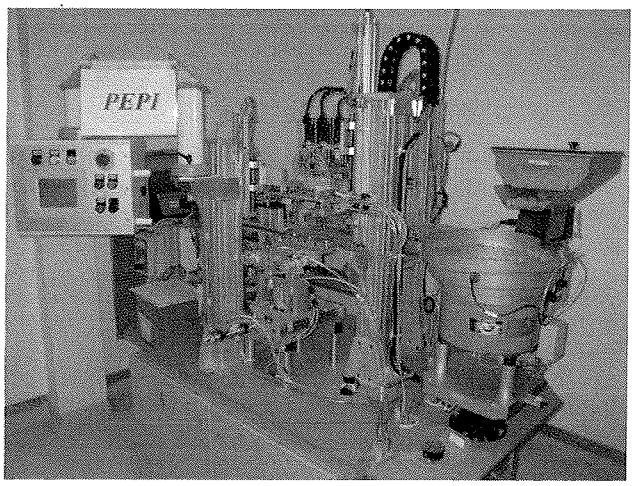


Fig. 3: Machine

2.2 Machine hardware and software

Heart of the machine are screwing heads with servo motors and microprocessor closed loop control of torque and rotation speed. These two parameters are inserted by operator through the control panel.

The process consists of two steps:

1. screwing up to predefined torque of 3Ndm, rotation speed is variable and should be inputted via control panel

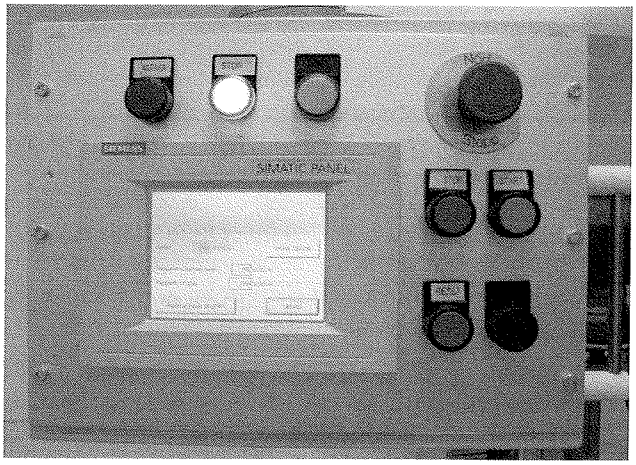


Fig. 4: Machine control panel

2. screwing with lower rotation speed of 10RPM, final torque is variable and should be inputted via control panel

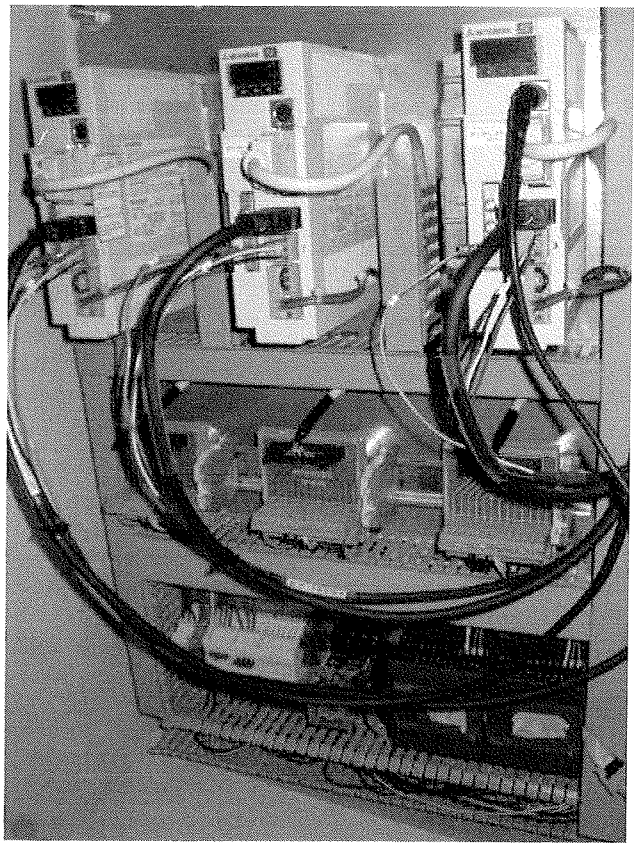


Fig. 5: Servo controllers and DA units

2.2.1 The program flowchart and explanation of the speed/torque control

The flow chart of the screwing procedure is presented in figure 7. The process is intentionally divided into two phases, so that optimum between speed and accuracy can be reached without remarkable overshooting in torque.

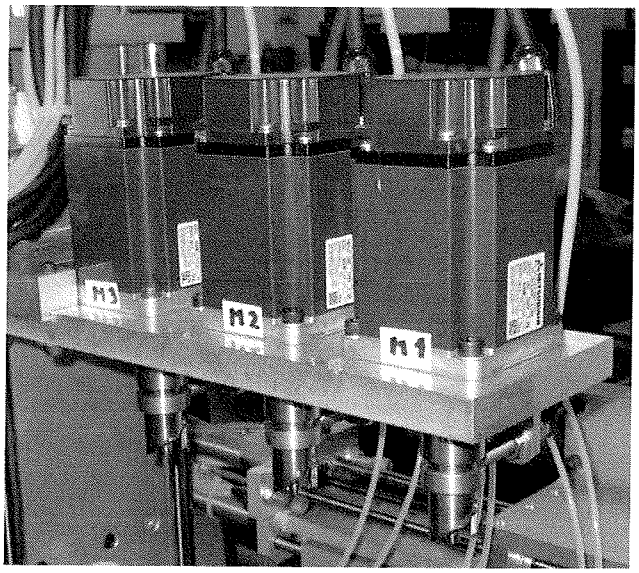


Fig. 6: Servo motors with screwing heads

Control signals for adjusting the speed and torque from PLC to servo controllers are provided by analogue signals with 0 to +10V reference. The resolution of the system is 12 bit. Theoretically we can adjust the torque with accuracy better than 0,005 Ndm, which is more than enough in this particular application.

When the routine starts the servo regulator works in a "speed control mode", in order to perform quick and reliable positioning of the screwing heads in home position. Just before the screwing procedure starts, the servo regulator switches into the "torque control mode" where it is able to provide the specified torque.

In this particular mode the servo regulator follows torque and speed reference from superior PLC. However the speed reference can be followed and carried out, only if the torque reference value has not been exceeded. When load reaches predefined torque value the speed of servomotor begins to fall and eventually it reaches zero.

The signal of motor zero speed is also the crucial signal in the control program and represents the condition for jumping to next programming sequence.

The time graph of the screwing sequence in torque control mode can be seen on figure 8. The *"ON" signal* line represents the control signal from superior PLC to servo regulator, it has two states (HIGH state energizes the servomotor and LOW state deenergizes it). There is a clear point of speed drop when the torque reaches its maximum. This graph was recorded during the second phase of screwing procedure.

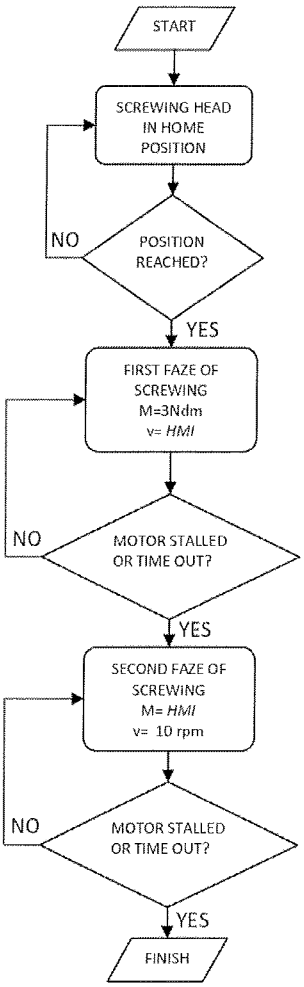


Fig. 7: Flow chart (simplified)

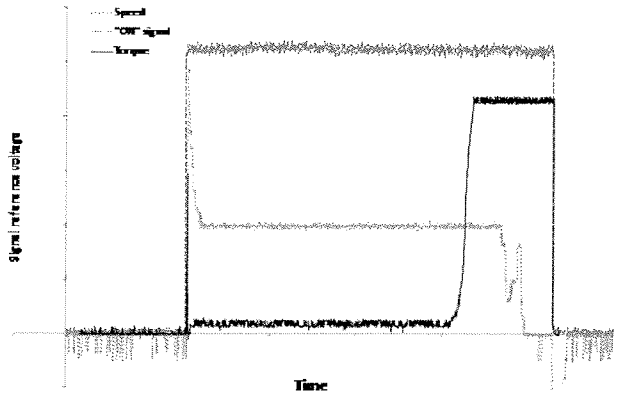


Fig. 8: Screwing sequence time diagram (phase 2)

2.3 Check of system linearity and accuracy

Before the servo system was installed into the machine, some basic tests were made in order to check the linearity and accuracy of the motor torque output as a function of torque reference. This was also a base for system calibration.

On figure 9 schematic drawings represent the system calibration procedure. The procedure is considered as a static measurement. The torque of servomotor was "weighted" with known masses on a light rope, which was connected to the light pulley of known perimeter. The pulley was directly connected to the servo motor axis. The servo controller is capable of providing feedback information of the servo motor's momentary torque output.

The data was acquired when the outer torque with respect to mass gravity force and the servo motor torque were in equilibrium. The condition of a constant angular velocity must be met in order to use the equation's below:

$$\sum \vec{M}_i = 0, \omega = 0$$

$$\vec{M}_{F_g} + \vec{M}_{SM} = 0$$

$$\vec{M}_{SM} = -\vec{r} \times \vec{F}_g$$

$$M_{SM} = F_g \cdot \frac{d}{2}$$

Based on upper equation we were able to calculate the theoretical torque, which was compared to servo controller feedback.

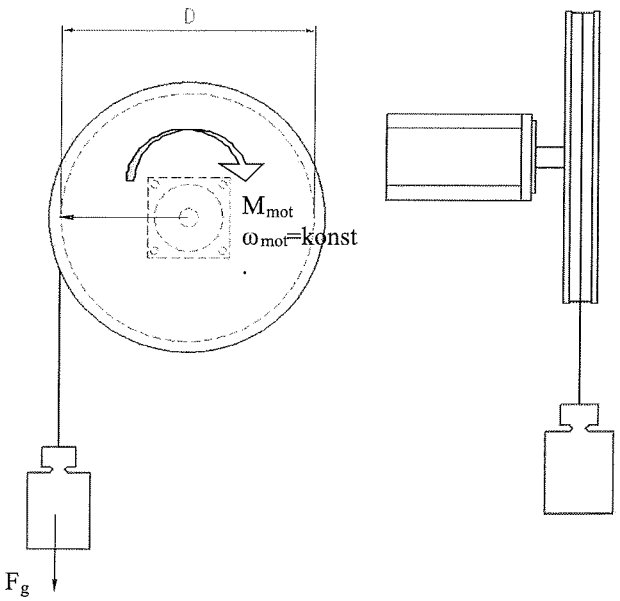
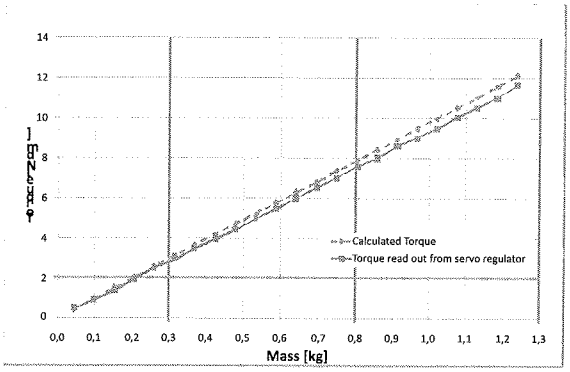


Fig. 9: Scheme of a torque measurement procedure a) front view; b) side view

The graphical representation of the results can be seen on figure 10a. In general there is a constant 5% difference between calculated value and the feedback from servo controller. This difference can be successfully compensated in the software of the control PLC.

In order to assure precise control of the torque on the connector screwing machine, the linearity measurement of the DA converter from the PLC was carried out. The graphical representation is on figure 10b. The R^2 factor of the data has a value very near 1, which gives us a great confidence in DA converter linearity.

a



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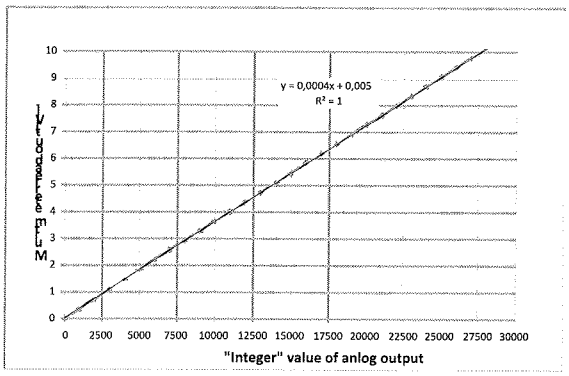

Fig. 10: Graphs of torque measurement and voltage output – a) Theoretical and servo controller feedback torque; b) Linearity of the DA converter

3. Results

3.1 Machine operation

Machine has been in operation for several months and besides some minor mechanical and software changes it has been performing according to expectations.

3.2 Machine throughput

Planned throughput of 8.000pcs/shift has been reached very soon. Today, the machine throughput is in the range of 9.500pcs/shift.

3.3 Determination of torque window

Torque window within which the cap should be screwed on the connector was determined in the following way :

a)if minimum torque is applied the line should still not leak through the connector cap

By use of graph shown on figure 11 the minimum torque required before the line starts to leak was determined to be 2Ndm. As can be seen on figure 12, line leakage through the connector screwed with less than 2Ndm becomes substantial.

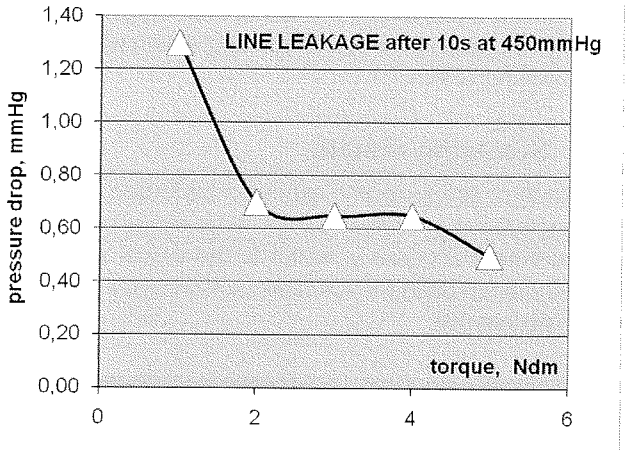

Fig. 11: Line leakage versus torque

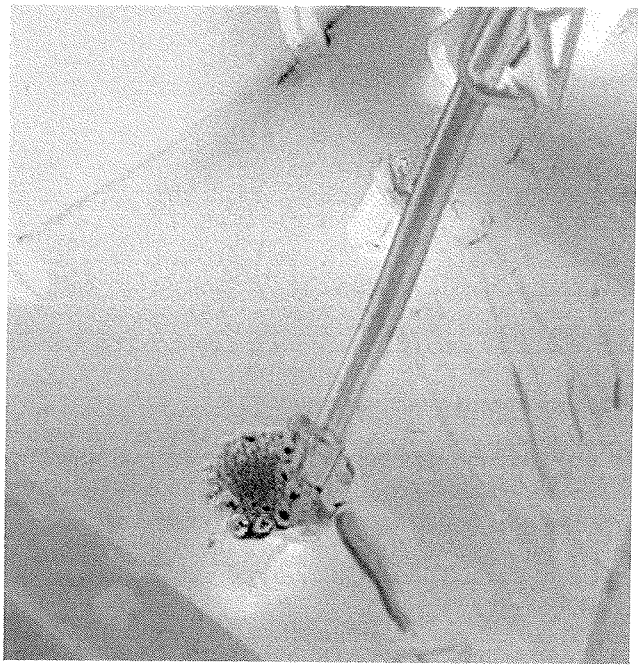

Fig. 12: Cap to screw leakage

b)if maximum torque is applied it becomes impossible to unscrew the cap manually without the appropriate tool. Several people were asked to unscrew the caps and subjectively classify the force they had to use. The results are shown in the Table 1. Obviously, torque above 8Ndm is already too high and it becomes impossible to unscrew the cap.

Table 1, force needed to unscrew the cap, subjective rating

torque, Ndm	unscrewing, subjective rating
3	easy
4	easy
5	not so easy
6	difficult
7	almost impossible
8	impossible
20	impossible

From above experiments the acceptable torque window was defined to be between 3Ndm and 8Ndm with central value around 5Ndm.

3.4 Screwing results

Validation of screwing was executed by torque measurement needed to unscrew the cap. To do so we prepared a measurement accessory similar to the actual machine's screwing head used for automatic screwing but with added dynamometer.

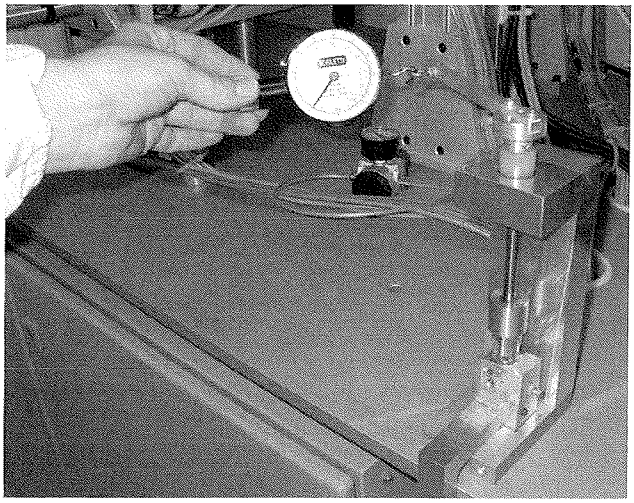

Fig. 13: Torque measurement

To execute the measurement the subassembly must be positioned in the holder, the measurement head lowered and the dynamometer arm forced to open the cap.

The force is read and the torque needed to unscrew the cap calculated.

The data acquired for the torque needed to unscrew the caps and spikes is represented on figure 14. The calculated mean value of the torque is 5,2 Ndm with standard deviation of 0,9 Ndm (based on population of 336 samples). Shape of the histogram is very close to theoretical normal distribution N (5.2;0.9).

4. Conclusion

The machine for automatic screwing of caps to spike connectors was constructed and built. Due to its high throughput it successfully replaced several manual operators with which we also avoided problems of long term operator finger and handaches, as well as we obtained good control of screwing process. Long term results of torque measurements show almost 30 % better accuracy of automatic system over the manual assembly. Operator friendly user interface allows easy machine set up and control of main process parameters.

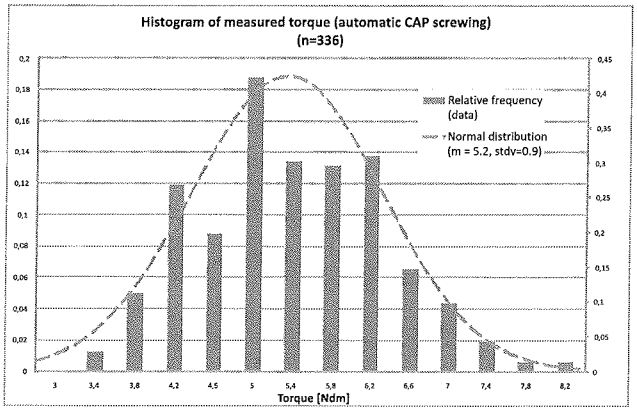

Fig. 14: Histogram of torque measurements

Although main goals of machine operation and process control were met, there is still room for further development and research, especially in shortening cycle time and lowering standard deviation of the unscrewing torque.

5. References

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Our Company

Originated in 1996 as an IC design center, IDS has a vast creative pool of highly motivated engineers, offers substantial IP, and holds many patents.

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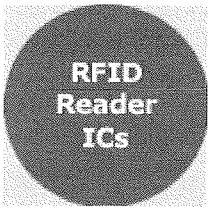
Our comprehensive portfolio comprises passive, semi-passive and active RFID systems, as well as services and IPs. For example, our smart label chip makes it practical for the first time to track, monitor, time-stamp and record information about any goods in any supply chain or cold chain transport. And our reader chip reduces the specialized RFID knowledge required to design a UHF reader. We look forward to serving you with our unique RFID expertise as we lead the development and integration of RFID-based solutions for companies around the world.

Product Overview



R13MP »

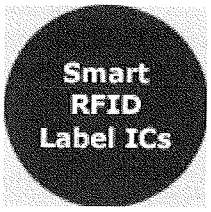
13.56 MHz RFID reader chip reads/writes multiple protocols.

R14AB »

ISO 14443 Reader Chip Optimized for Battery-Powered RFID Readers.

R900 Series »

Highly integrated EPC Gen 2 reader ICs.

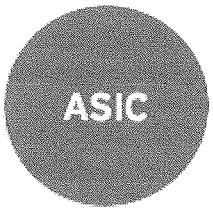


SL13A »

Smart label chip with sensor identifies, monitors and logs.

SL900A »

EPC Class 3 chip with sensor.



ASIC - IP »

R13MP *13.56 MHz RFID reader chip reads/writes multiple protocols*

The R13MP is a multi-protocol RFID reader chip covering a wide range of applications including complete RFID data logging systems complementing SL13A-based smart data loggers. The R13MP supports all commonly used standards. Proprietary protocols are supported through the direct mode.

Adding a simple low-cost 8-bit microcontroller completes a universal reader system suitable for numerous applications, both in proximity and vicinity RFID systems, and approved in more than 70 countries worldwide.

A complete development kit including a R13MP reader board and a SL13A smart data logger board is available. The kit comes with demo application and GUI software with source codes.

R14AB *ISO 14443 Reader Chip Optimized for Battery-Powered RFID Readers*

The R14AB is an extremely low-power ISO 14443A/B RFID reader IC. It also supports NFCIP-1 106-kbps active communication and Mifare® Ultralight 4-bit ACK/NACK reply. Other standards and custom protocols are possible via the transparent mode.

A complete development kit including a R14AB reader board is available. The kit comes with demo application and GUI software with source codes.

R901G and R902DRM *Highly integrated EPC Gen 2 reader Ics*

The R901G and R902DRM are EPC Gen2 RFID reader chips enabling battery-powered, small form-factor handheld and embedded UHF reader systems. The chips fully

Glede na navedene podatke in kvaliteto vabljenih in rednih prispevkov smo organizatorji, upamo pa tudi da udeleženci

support ISO 18000-6C, and ISO 18000-6A/B as well as proprietary protocols are supported through the direct mode.

Adding a simple low-cost 8-bit microcontroller completes a portable UHF reader system. In embedded systems, the R901G / R902DRM can share a common CPU with the rest of the system. Hence reducing BOM and enabling cost-efficient solutions with minimum form factor. The R902DRM also includes dense reader mode function, which prevents reading conflicts in a multi-reader environment.

Complete development kits including R901G reader boards are available. The kits come with demo application and GUI software with source codes.

SL13A *Smart label chip with sensor identifies, monitors and logs*

IDS significantly broadens the scope of affordable RFID automatic data logging applications with its unique SL13A smart label chip. Priced up to 10 times lower than existing RFID temperature-sensing modules, this sophisticated chip for the first time makes it practical and affordable to automatically track, monitor, time-stamp and record information about any goods in any supply chain or cold chain transport.

The SL13A works in semi-passive (battery-assisted) as well as in fully passive modes. The chip is ideal for applications using thin and flexible batteries (1.5V or 3V) for autonomous logging from the integrated temperature sensor or an external sensor with time-stamp from on-chip real-time clock. The SPI port allows connection of other external circuits.

konference, z letošnjo konferenco zelo zadovoljni. To nam je v motivacijo in izziv pri pripravi aktualnih znanstvenih in razvojnih tem ter organizacije konference MIDEM 2010.

A complete development kit including an R13MP reader board and a SL13A smart data logger board is available. The kit comes with demo application and GUI software with source codes.

SL900A *EPC Class 3 Chip with Sensor*

The SL900A is an EPC Class 3 tag chip enabling affordable RFID automatic data logging applications with sensor functions. This sophisticated chip makes it practical and affordable to automatically track, monitor, time-stamp and record information about any goods in any supply chain or cold chain transport. Furthermore, the SL900A enables vast new applications in areas such as medical, healthcare and environmental supervision.

A complete development kit including an R902DRM reader board and a SL900A smart data logger board will be available. The kit comes with demo application and GUI software with source codes.

ASIC IP

IDS has a vast pool of IP (intellectual properties) at its disposal. To a great extent, our IP is protected through patents providing USP (unique selling proposition) for our partners and customers.
Our IP is mainly RFID-related with focus on integrated circuits for HF and UHF readers and smart labels and used in our application specific integrated circuits (ASIC) including both application specific standard products (ASSP) as well as customer specific integrated circuits (CSIC).

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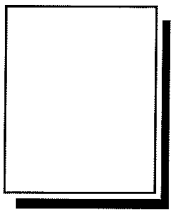

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