UDK 621.3:(53+54+621+66)(05)(497.1)=00 ISSN 0352-9045

INFORMACIJE MIDEM 3 ◦ 1999

Strokovno društvo za mikroelektroniko elektronske sestavne dele in materiale

Strokovna revija za mikroelektroniko, elektronske sestavne dele in materiale
Journal of Microelectronics, Electronic Components and Materials

INFORMACIJE MIDEM, LETNIK 29, ŠT. 3(91), LJUBLJANA, september 1999

UDK 621.3:(53+54+621+66)(05)(497.1)=00 ISSN 0352-9045

INFORMACIJE MIDEM 3 ◦ 1999

INFORMACIJE MIDEM LETNIK 29, ŠT. 3(91), LJUBLJANA, SEPTEMBER 1999
INFORMACIJE MIDEM VOLUME 29, NO. 3(91), LJUBLJANA, SEPTEMBER 1999

Revija izhaja trimesečno (marec, junij, september, december). Izdaja strokovno društvo za mikroelektroniko, elektronske sestavne dele in materiale - MIDEM.
Published quarterly (march, june, september, december) by Society for Microelectronics, Electronic Components and Materials - MIDEM.

Naslov uredništva
Headquarters
Uredništvo Informacije MIDEM
Elektrotehniška zveza Slovenije
Dunajska 10, 1000 Ljubljana, Slovenija
tel.: +386 (0)61 1512 221
fax: +386 (0)61 1512 217
Iztok.Sorli@guest.arnes.si
http://paris.fe.uni-lj.si/midem/journal.htm

Letna naročnina znaša 12.000,00 SIT, cena posamezne številke je 3000,00 SIT. Člani in sponzorji MIDEM prejemajo Informacije MIDEM brezplačno.
Annual subscription rate is DEM 200, separate issue is DEM 50. MIDEM members and Society sponsors receive Informacije MIDEM for free.

Znanstveni svet za tehnične vede I je podal pozitivno mnenje o reviji kot znanstveno strokovni reviji za mikroelektroniko, elektronske sestavne dele in materiale. Izdajo revije sofinanci rajo Ministrstvo za znanost in tehnologijo in sponzorji društva.
Scientific Council for Technical Sciences of Slovene Ministry of Science and Technology has recognized Informacije MIDEM as scientific Journal for microelectronics, electronic components and materials.
Publishing of the Journal is financed by Slovene Ministry of Science and Technology and by Society sponsors.

Znanstveno strokovne prispevke objavljene v Informacijah MIDEM zajemamo v podatkovne baze COBISS in INSPEC.

Prispevke iz revije zajema ISI ® v naslednje svoje produkte: Sci Search® , Research Alert® in Materials Science Citation Index™

Scientific and professional papers published in Informacije MIDEM are assessed into COBISS and INSPEC databases.

The Journal is indexed by ISI® for Sci Search®, Research Alert® and Material Science Citation Index™

Po mnenju Ministrstva za informiranje št.23/300-92 šteje glasilo Informacije MIDEM med proizvode informativnega značaja, za katere se plačuje davek od prometa proizvodov po stopnji 5 %.

Grafična priprava in tisk
Printed by
BIRO M, Ljubljana

Naklada
Circulation
1000 izvodov
1000 issues

Poštnina plačana pri pošti 1102 Ljubljana
Slovenia Taxe Percue

UDK621.3:(53+54+621+66), ISSN0352-9045 Informacije MIDEM 29(1999)3, Ljubljana

DRUŠTVO MIDEM IN KONFERENCA MIDEM NA INTERNETU

Dragi člani društva in bralci revije !

Predstavitev društva MIDEM in predstavitev konferenc MIDEM lahko poiščete na INTERNETU in sicer :

1. Predstavitev društva MIDEM in revije " Informacije MIDEM " na naslovu
http://paris.fe.uni-lj.si/midem/society.htm
http://paris.fe.uni-lj.si/midem/journal.htm

2. Predstavitev konference MIDEM na naslovu
http://paris.fe.uni-lj.si/midem/conf99.htm

3. Elektronsko pošto lahko pošiljate na naslov :
Iztok.Sorli@guest.arnes.si
Pri vpisu naslovov pazite na velike in majhne črke !!

Vse člane vljudno prosimo, da poravnajo članarino za leto 1999.

MIDEM SOCIETY AND MIDEM CONFERENCE ON INTERNET

Dear readers and Society members !

Presentation of MIDEM Society and the information on the MIDEM Conference can be found on INTERNET as follows :

1. Presentation of MIDEM Society and Journal "Informacije MIDEM", address
http://paris.fe.uni-lj.si/midem/society.htm
http://paris.fe.uni-lj.si/midem/journal.htm

2. Presentation of the MIDEM'99 Conference, address
http://paris.fe.uni-lj.si/midem/conf99.htm

3. Email can be sent to :
Iztok.Sorli@guest.arnes.si
Please, use exact lower and upper case letters as indicated.

We kindly ask all our members to pay the membership fee for 1999.

PREPARATION OF THIN COATINGS OF TITANIUM COMPOUNDS WITH ION IMPLANTATION

M. Mozetič[1], A. Zalar[1], J. Jagielski[2,6], G. A. Evangelakis[3],
M. Drobnič[4] and V. Chab[5],
[1]Institute of Surface Engineering and Optoelectronics, Ljubljana, Slovenia
[2]Institute of Electronic Materials Technology, Warszawa, Poland
[3]University of Ioannina, Ioannina, Greece
[4]IBM Slovenija, Ljubljana, Slovenia
[5]Institute of Physics, Czeh Academy of Sciences, Praha, Czech Republic
[6]A. Soltan Institute of Nuclear Studie,Swierk/Otwock, Poland

Keywords: microelectronics, ion implantation, surface technologies, surface engineering, surface coatings, thin coatings, semiconductor compounds, computer simulations, SRIM IBM software, Stopping and Range of Ions in Matter, Ti compoounds, titanium compounds, Ti oxides, titanium oxides, Ti nitrides, titanium nitrides, ion beams, irradiation damages, thin films, AES, Auger Electron Spectroscopy, AES depth profiling

Abstract: The growth of thin coatings of titanium oxide and nitride during ion implantation of respective ions into titanium substrate was studied theoretically and experimentally. The IBM SRIM software was used to determine the concentration profiles of implanted ions, the sputtering rate, probability of back – scattering and ion energy loss mechanisms. Theoretical results were compared with experiments. Samples of pure titanium plates were carefully polished and exposed to a flux of oxygen and nitrogen ions with the kinetic energy of 100 keV per molecule (50 keV per atom). The ion doses were $5x10^{16}$, $1x10^{17}$, $2.5x10^{17}$, $5x10^{17}$, $7.5x10^{17}$, $1x10^{18}$ atoms/cm^2. Depth profiles of the samples were determined by the AES method. Both the theory and experiment showed that the ion range at the low dose was about 90 nm for the case of nitrogen, and 80 nm for the case of oxygen, with depth distribution typical for ion implantation. Experimental results showed that a layer of titanium compound with a constant composition was formed at the ion dose above 7.5 x 10^{17} atoms/cm^2.

Priprava tankih prevlek titanovih spojin z ionsko implantacijo

Ključne besede: mikroelektronika, implantacija ionov, tehnologije površin, inženiring površin, prevleke površinske, prevleke tanke, snovi polprevodniške, simulacije računalniške, SRIM oprema programska IBM, Ti snovi titanove, Ti oksidi titanovi, Ti nitridi titanovi, curki ionski, poškodbe vsled obsevanja, plasti tanke, AES Auger spektroskopija elektronska, AES prifiliranje globinsko

Povzetek: Prikazujemo rezultate teoretične in eksperimentalne preiskave rasti tankih plasti titanovega oksida in nitrida med ionsko implantacijo z ustreznimi ioni. Z uporabo programske opreme IBM SRIM smo določili koncentracijske profile implantiranih ionov, razprševanje titanovih atomov, verjetnost za odboj vpadnega iona od površine in mehanizme izgube kinetične energije ionov. Teoretične rezultate smo primerjali z eksperimentalnimi. Vzorce ploščic iz čistega titana smo gladko polirali in izpostavili toku kisikovih in dušikovih ionov s kinetično energijo 100 keV na molekulo (50 keV na atom). Doza ionov je bila $5x10^{16}$, $1x10^{17}$, $2.5x10^{17}$, $5x10^{17}$, $7.5x10^{17}$ in $1x10^{18}$ atomov/cm^2. Globinske profile vzorcev smo določili z metodo AES. Tako teoretični kot eksperimentalni rezultati so pokazali, da je doseg ionov približno 90 nm za dušik in 80 nm za kisik. Globinska porazdelitev elementov je bila značilna za tehniko ionske implantacije. Eksperimentalni rezultati so pokazali, da se formira tanka plast titanove spojine s konstantno sestavo pri dozi, ki je večja od 7.5 x 10^{17} atomov/cm^2.

1. INTRODUCTION

The performance of technical products is considerably influenced by surfaces. A coating with proper characteristics can significantly increase the resistance against physical and chemical attack by the medium in environmental, tribological, electrical or electrochemical contact with the surface. In the past few decades, numerous techniques for changing of surface and/or deposition of protective coatings have been developed. Many of them are based on different chemical vapour deposition (CVD) processes and physical vapour deposition (PVD) processes /1/. Operating pressure, the temperature of both the substrate and the surrounding gas, vapour phase composition and particle energy are the main parameters, which distinguish between the two deposition processes. The CVD processes are based on the interaction of gaseous chemical compounds in the immediate vicinity of the substrate surface and the subsequent deposition of the reaction products. In the PVD processes, on the other hand, the material vapour source primarily emits atomic particles, which hit the substrate surface and remain bonded. The kinetic energy of incidence particles in PVD processes is of the order of 0.1 eV for the case of evaporation, 1-10 eV for sputtering and 100 – 1000 eV for ion plating. An even higher kinetic energy of incidence particles is in the process of ion implantation, where the energy may be of the order of keV or even MeV /2,3/. In the present paper, we describe experimental and theoretical study on ion implantation of oxygen and nitrogen ions into titanium substrates.

2. COMPUTER SIMULATION

Theoretical study of the formation of thin ceramic films on titanium substrates was performed by the use of the IBM SRIM software package /4,5/. A typical output of

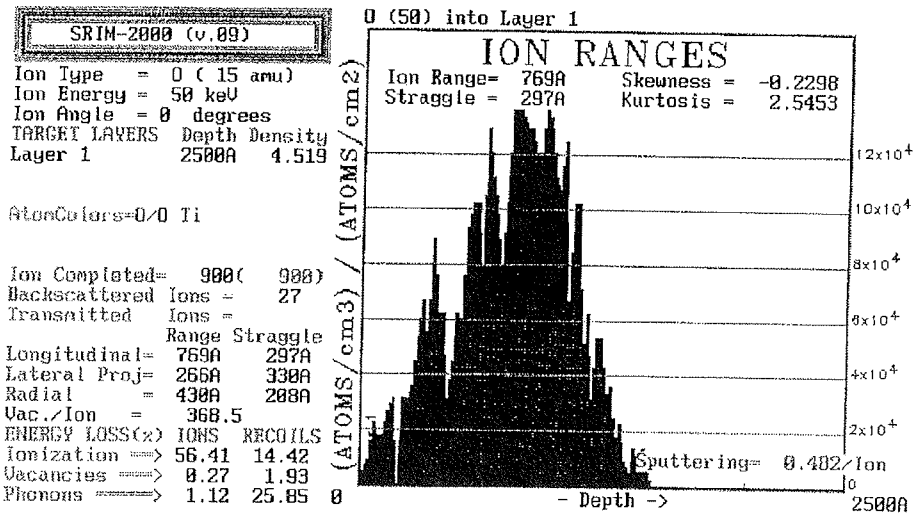


Fig. 1. A typical output of SRIM simulation of 50 keV O^+ implantation into titanium substrate.

the computer simulation is plotted in Figure 1. In this case, we simulated implantation of 50 keV O^+ ions into perfectly flat titanium substrate. The calculated distribution of oxygen atoms show that the ion range is 76.9 nm. Damage in the surface layer of the sample is caused both by the original ions and the recoils. The major part of the kinetic energy of incident ions is lost by ionization of titanium atoms in the bulk. The ions hardly cause any formation of vacancies or phonons. The recoils, on the other hand, lose most of their kinetic energy by formation of phonons. The great difference of the channels of the energy lost between the ions and the recoils is due to a great difference of their kinetic energy. As long as the kinetic energy is high, the far most probable way of lose of the energy is ionization. As the energy decreases, the ionization becomes less probable on the expense of phonons and vacancies. Since the kinetic energy of recoils is much lower than the original kinetic energy of ions, there is a great difference in the way of losing their energy. At the kinetic energy of oxygen ions of 50 keV and the normal incidence angle the calculated rate of sputtering is 0.482 titanium atoms per ion. The probability of back - scattering at that kinetic energy and angle of incidence is low. The computer simulation calculated only 3 out of 100 ions are back – scattered.

Similar results were obtained also at simulation of 50 keV nitrogen ions into titanium substrate. The calculated data for oxygen and nitrogen implantation are summarized in table 1.

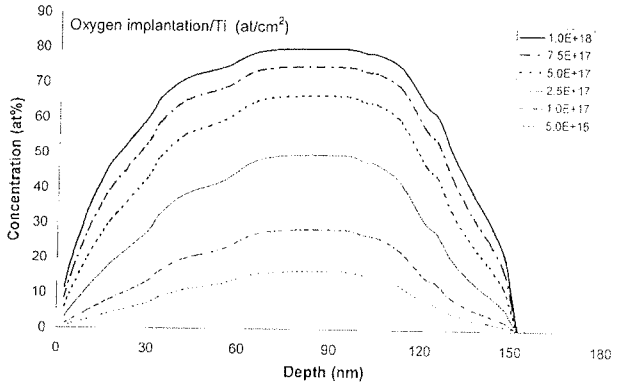


Fig. 2. Calculated oxygen concentration profiles in titanium samples treated with 50 keV oxygen ions at different doses, obtained with a SRIM simulation.

Table 1. Comparison of different mechanisms of energy loss for oxygen and nitrogen

Type of ion	O^+ 50 keV	N^+ 50 keV
Ion range	76.9 nm	84.7 nm
Sputtering rate	0.482 atoms/ion	0.341 atoms/ion
Ions energy loss (ionization)	56.41 %	60.22 %
Ions energy loss (vacancies)	0.27 %	0.27 %
Ions energy loss (phonons)	1.12 %	1.75 %
Recoils energy loss (ionization)	14.42 %	12.94 %
Recoils energy loss (vacancies)	1.93 %	1.75 %
Recoils energy loss (phonons)	25.85 %	23.68 %

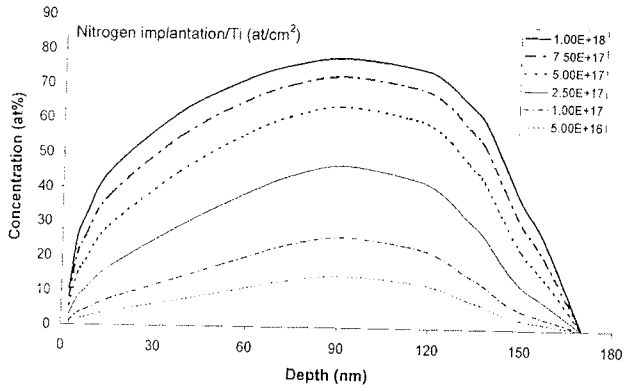


Fig. 3. Calculated nitrogen concentration profiles in titanium samples treated with 50 keV nitrogen ions at different doses, obtained with a SRIM simulation.

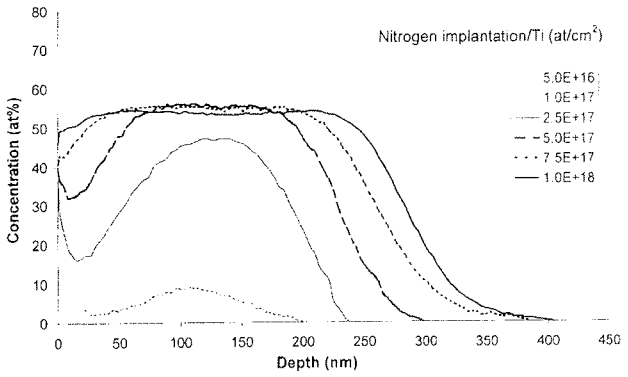


Fig. 5. AES nitrogen depth profiles in titanium samples treated with 50 keV nitrogen ions at different doses.

In order to calculate depth profiles of thin ceramic films on titanium substrate the doses of O^+ and N^+ ions was varied between 5 x 10^{16} and 1 x 10^{18} ions/cm^2. The calculated distribution of O and N atoms in the target is shown in Figure 2 and 3, respectively.

3. EXPERIMENTAL

Samples of pure titanium plates were carefully polished and exposed to a flux of oxygen and nitrogen ions with the kinetic energy of 100 keV per molecule (50 keV per atom). The ion doses were 5x10^{16}, 1x10^{17}, 2.5x10^{17}, 5x10^{17}, 7.5x10^{17} and 1x10^{18} atoms/cm^2. The composition of the surface layer on the samples was determined by the AES depth profiling. The samples were analyzed with a scanning Auger microprobe (Physical Electronics Ind. SAM 545 A). A static primary electron beam with 3keV energy, 0.5 μA beam current and about 40 μm diameter was used. The electron incidence angle with respect to the normal to the average surface plain was 30°. The samples were ion sputtered with two symmetrically inclined beams of 3 keV Ar^+ ions, rastered on a surface area larger than 5 x 5 mm at an incidence angle of 47°. A sputter rate of about 2,5 nm/min was determined on a reference multilayer Cr/Ni thin film structure.

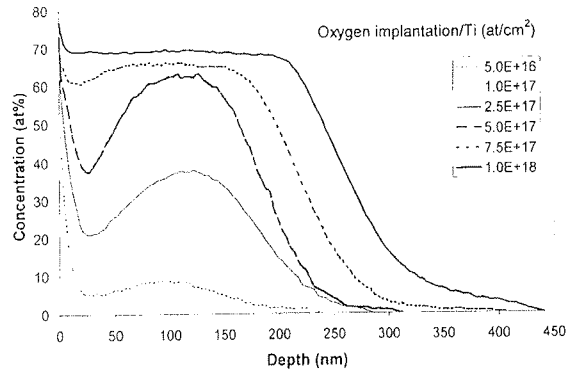


Fig. 4. AES oxygen depth profiles in titanium samples treated with 50 keV oxygen ions at different doses

The depth profiles of the samples for the case of oxygen and nitrogen implantation are shown in Figure 4 and 5, respectively.

4. DISCUSSION AND CONCLUSION

Formation of a thin ceramic layer on titanium substrate was studied theoretically and experimentally. For theoretical study we performed computer simulation using the IBM SRIM software package. The simulation allowed for estimation of the energy loss during implantation of oxygen and nitrogen ions with the kinetic energy of 50 keV. At the normal incidence angle the most probable loss of kinetic energy of ions was via ionization of bulk titanium atoms. The ionization efficiency was somewhat higher for nitrogen ions. In both cases, the recoils lost most of their energy via interaction with crystal lattice. For this mechanism the energy loss was about 10% higher for recoils displaced during oxygen implantation. The ion range in the target was 76.9 nm for oxygen and 84.7 nm for nitrogen. The sputtering rate was 0.482 atoms/ion for the case of oxygen implantation and 0.341 atoms/ion for the case of nitrogen implantation. The difference in both the ion

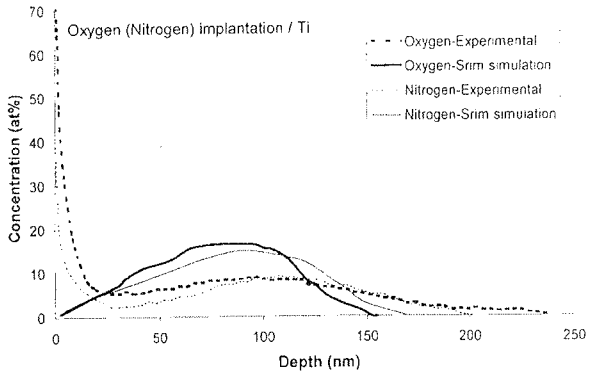


Fig. 6. Theoretical and experimental distribution of oxygen and nitrogen atoms in titanium substrate after implantation with respective ions at the dose of 5 x 10^{16} atoms/cm^2.

range and sputtering rate is due to a different mass of the ions.

Results of computer simulation are reasonably sound with the experimental observations at low doses (Figure 6). The discrepancy between the computer simulation and experimental results increases with increasing ion dose. At high doses (in our case above 5 x 10^{17} ions/cm^2) the computer simulation give much different results than the experiment. This is due to at least two reasons: i) the software package does not take into account the chemical interaction of implanted ions with solid material, and ii) the package does not take into account the change of the surface line position due to extensive sputtering of the surface atoms.

Acknowledgement

This work has been funded by the Ministry of Science end Technology of the Republic of Slovenia. M. Mozetič gratefully acknowledges a grant from NATO Science Fellowship Programme.

5. REFERENCES

/1/ H. Freller, Vapour – phase coating processes for hard coatings, Vacuum 45 (1994), 997-1000.

/2/ J. Jagielski, G. Gawlik, A. Zalar and M. Mozetič, "Ion implantation; a modern tool for surface engineering", Inf. Midem 29, 2, (1999), 61-67.

/3/ A. Vesel, M. Mozetič, J. Kovač, Izračun koeficienta razprševanja, Vakuumist 18 (1998),14-18.

/4/ J.F. Zeigler, SRIM-The Stopimg and Range of Ions in Matter, IBM-Research, YorkTown, (1998).

/5/ J.F. Ziegler, J.P. Biersack, U. Littmark, The Stopping and Range of Ions in Solids, Pergamon Press, New York, (1985).

M. Mozetič, A. Zalar,
Institute of Surface Engineering and Optoelectronics,
Teslova 30, 1000 Ljubljana, Slovenia,
miran.mozetic@ guest.arnes.si,
anton.zalar@ guest.arnes.si

J. Jagielski,
Institute of Electronic Materials Technology,
Wolczynska 133, 01-919 Warszawa, Poland,
jagiel_j@sp.itme.edu.pl
A. Soltan Institute of Nuclear Studies,
05-400 Swierk/Otwock, Poland

G.A. Evangelakis,
University of Ioannina
P.O.Box 1186, 45110 Ioannina, Greece,
gevagel@ cc.uoi.gr

M. Drobnič,
IBM Slovenija,
Trg republike 3, 1000 Ljubljana, Slovenia,
matija_drobnic@si.ibm.com

V. Chab,
Institute of Physics,
Czech Academy of Sciences,
Cukrovarnicka 10, 16253 Praha, Czech Republic,
CHAB@FZU.CZ

Prispelo (Arrived): 05.09.99 *Sprejeto (Accepted): 15.09.99*

POROUS THIN FILM HUMIDITY SENSOR BASED ON DOPED AND UNDOPED TITANIA

Jaroslav Slunečko, Janez Holc, Marija Kosec, Drago Kolar
Institute "Jožef Stefan", Ljubljana, Slovenija

Key words: humidity sensors, TiO_2, titanium dioxide, thin films, potassium doped TiO_2 titanium dioxide, undoped TiO_2 titanium dioxide, porous materials, electrical properties

Abstract: Potassium doped and undoped TiO_2 thin films were prepared by the sol-gel technique. The influence of potassium addition and of the film firing temperature on the sample morphology, and on the electrical properties of TiO_2 thin films were studied. The effect of introducing pores in undoped and potassium doped TiO_2 thin films on their humidity sensing characteristics was also studied. Introduction of the porosity in thin films had a positive effect on the humidity sensing characteristics of the samples. Sol-gel processed, porous, and 10 at. % potassium doped TiO_2 thin films heated to 450°C exhibited an outstanding humidity sensitivity over the entire RH range.

Senzor vlage na osnovi poroznega dopiranega in nedopiranega TiO_2

Ključne besede: senzorji vlage,TiO_2 dioksid titanov, plasti tanke, TiO_2 dioksid titanov dopiran s kalijem, TiO_2 dioksid titanov nedopiran, materiali porozni, lastnosti električne

Povzetek: S sol gel tehniko so bile pripravljene s kalijem dopirane in nedopirane TiO_2 tanke plasti. Študirali smo vpliv kalija in temperature žganja tanke plasti na morfologijo in električne lastnosti plasti. Preiskovali smo tudi vpliv poroznosti tankega filma na senzorske lastnosti. Poroznost filma ima pozitivni efekt na lastnosti senzorja vlage. Senzor vlage pripravljen iz poroznega TiO_2 filma dopiranega s 10 at.% kalija ima po žganju pri 450°C zelo dober odziv v celotnem področju vlažnosti.

Introduction

Today, most commercially available humidity sensors are based on polymeric films, in spite of the fact that ceramic humidity sensors exhibit better chemical resistance and mechanical strength than polymeric sensors /1/. This situation is a consequence of the high costs that are incurred during the production of ceramic humidity sensors based on porous sintered oxides /2, 3/, because of the use of conventional ceramic technology. For that reason less costly manufacturing technology for miniature ceramic sensing elements is needed. Recently, films prepared by sol-gel methods were studied /4, 5/ as humidity sensing devices. This chemical technique offers a very promising feature, namely, the possibility of powder-free processing of ceramics in their final shape (films or fibres), which can be used as active elements in sensing devices /6/.

That is probably one of the reasons that several authors studied the suitability of sol-gel processed TiO_2-based thin films for humidity sensors /4, 5, 7, 8/. Titania was used as a sensing material because very interesting results have been reported for sintered porous compacts and thick films of titania and doped titania-based humidity sensors /9, 10, 11/. In the literature it was considered that a large pore volume and control of the pore size distribution are necessary for high humidity sensitivity of ceramic materials /3, 12/. For this reason it is interesting that an outstanding humidity sensitivity over the entire RH (relative humidity) range has been reported in dense, pore-free thin films/8/. Such a high response of sol-gel processed K-doped TiO_2 films has also rarely been observed for porous sintered ceramics. It is known that addition of alkali ions is effective in increasing the RH sensitivity of several ceramic oxides by affecting the sinterability of the material in pellet form /10/, decreasing the intrinsic resistance of the material /13/, or increasing the number of adsorption sites /14/. However, measurements performed by the authors /4, 8/ indicated a humidity sensing mechanism that is different from that generally accepted for porous ceramics This mechanism involves the direct participation of alkali ions in conduction during the exposure of the sensing material to a humid environment /4/.

In this study the influence of the introduction of pores in undoped and potassium doped TiO_2 thin film on their sensing characteristics is studied. Potassium ethoxide was used for introduction of potassium ions to the sols. The influence of potassium compound and pore former on the morphology and on the electrical properties of TiO_2 thin films were studied.

Experimental

TiO_2 thin films were prepared by the sol-gel technique. Precursor solutions for production of porous TiO_2 coatings were prepared by a slightly modified method reported by Kato et al. /15, 16/. Titanium tetraisopropoxide (TTIP) (Alfa Products), diethanolamine (Alfa Products), and ethanol (Carlo Erba) were mixed and stirred in a nitrogen glove box to prepare a homogenous solution. For preparation of doped TiO_2 films 10 at % of K was added to the solution. Sols were doped with potassium ethoxide (Alfa Products). Afterwards water diluted with ethanol was mixed into the solution. The water/alkoxide molar ratio was 1.

Polyethylene glycol (PEG) (Aldrich), molecular weight 1800-2200, was used as a pore former /15/ in several samples. In order to evaluate the influence of the concentration of the pore former on the porosity, the amount of PEG was varied between 2 and 4 wt. %. In the text we will use following notation: KE/Px.x - samples prepared with potassium dopant added, NK/Px.x -

samples prepared without potassium dopant added. In the notation Px.x represents the wt. % of PEG added.

Silicon wafers and alumina plates were used as support substrates. For electrical measurements, prototype sensors were prepared by depositing TiO_2-based films on alumina substrates with comb-type Au electrodes. The films were deposited from the solutions by the spin coating technique, using a rotation speed of 3000 RPM. Gel coatings were dried at 100°C and fired at 650°C for 1 hour /15/. Samples were also fired at 450°C for 2 hours in order to evaluate the influence of firing temperature on the sensing characteristics of TiO_2 thin films. The thickness of the TiO_2 coating was increased by repeating the cycle from spinning to firing.

The morphology and topography of the coatings was examined by scanning electron microscopy (SEM, JEOL JXA-840A) and scanning probe microscope (SPM, Digital Instruments Nanoscope III). Generaly, SPMs are best suited for imaging relatively flat samples. Its depth of field is limited by the travel limits of the scanning tube and by tip size and geometry. For that reason real values for pores depth can be greater than observed values. Topography of the sample is represented by different contrast. Contrast bar on the left side of the SPM images links the contrast with the surface height of the sample.

The humidity sensitive electrical properties of the thin films were evaluated using an impedance analyser (HP 4192A LF). An environment varying relative humidity (RH), ranging from 15 to 95 % at 25°C was obtained using an environmental chamber (Weiss SB1 160).

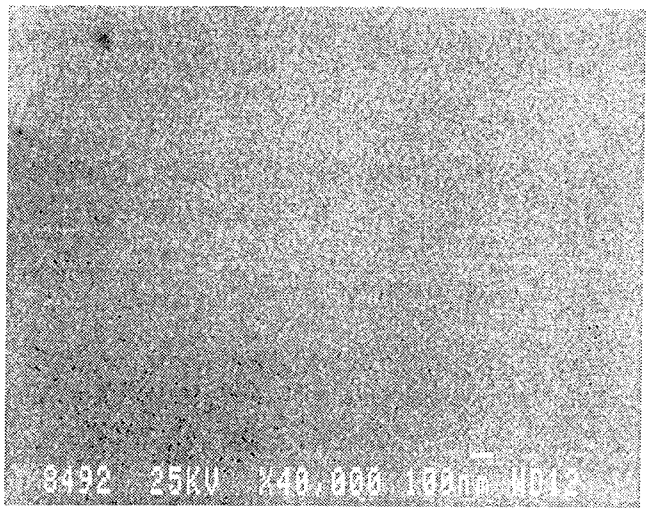
Results and discussion

The TiO_2 coating prepared from the solution without addition of polyethylene glycol (NK/P0.0) had almost no visible texture after firing at 450°C and 650°C (Fig. 1A). Firing of TiO_2 coating that was prepared from undoped sols with 2.4 wt. % of PEG added, at 650°C yielded thin films (NK/P2.4) with a porous microstructure (Fig. 1 B and C). Pores were from 100 nm to approximately 270 nm wide and at least 110 nm deep (Fig 1 C). There was almost no difference between microstructures of the samples NK/P2.4 fired at 450°C and 650°C.

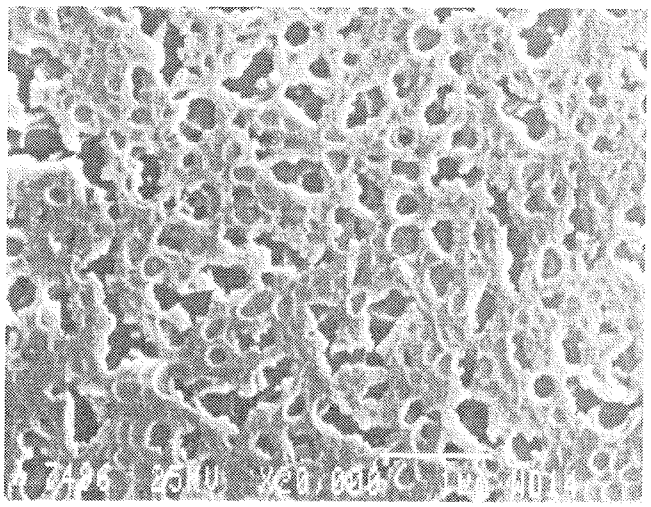
The influence of the addition of potassium compounds to the TTIP sol on the microstructure of the TiO_2 thin film is presented in Fig. 2 and 3.

Fig 2 show the morphology of K doped TiO_2 thin films fired at 650°C for 1 hour. There was slight difference between the morphology of KE/P0.0 (Fig. 2A and 2C) and the morphology of the KE/P4.0 sample (Fig. 2B and 2D). The sample without PEG added (KE/P0.0) had a granular microstructure with grains approximately 80 nm in diameter. Pores in Fig 2 C were from 10-50 nm wide and from 5 to ~15 nm deep. The sample KE/P4.0 with PEG added (Fig. 2D) had a microstructure with grains approximately 100 nm in diameter and pores ~50 nm wide and ~30 nm deep.

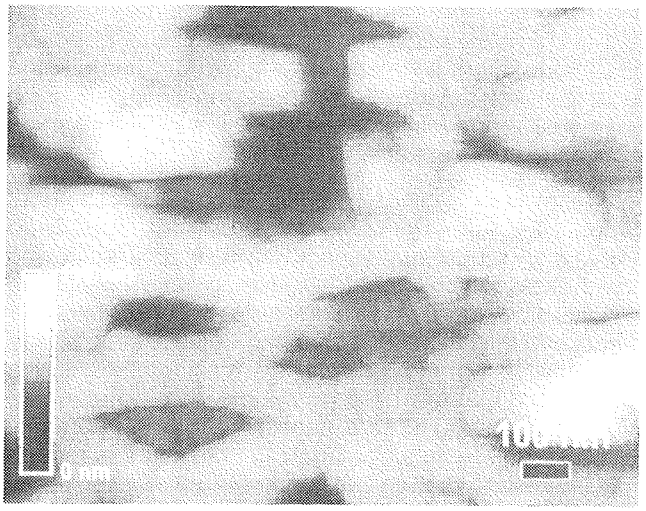
KE/P0.0 samples had also some areas with different contrast (Fig 2A). Areas with different contrast could also be observed in samples where the PEG concen-



A



B



C

Fig 1. Morphology of undoped TiO_2 thin films fired at 650°C for 1 h.
A. NK/P0.0 (SEM image),
B. NK/P2.4 (SEM image),
C. NK/P2.4 (SPM image)

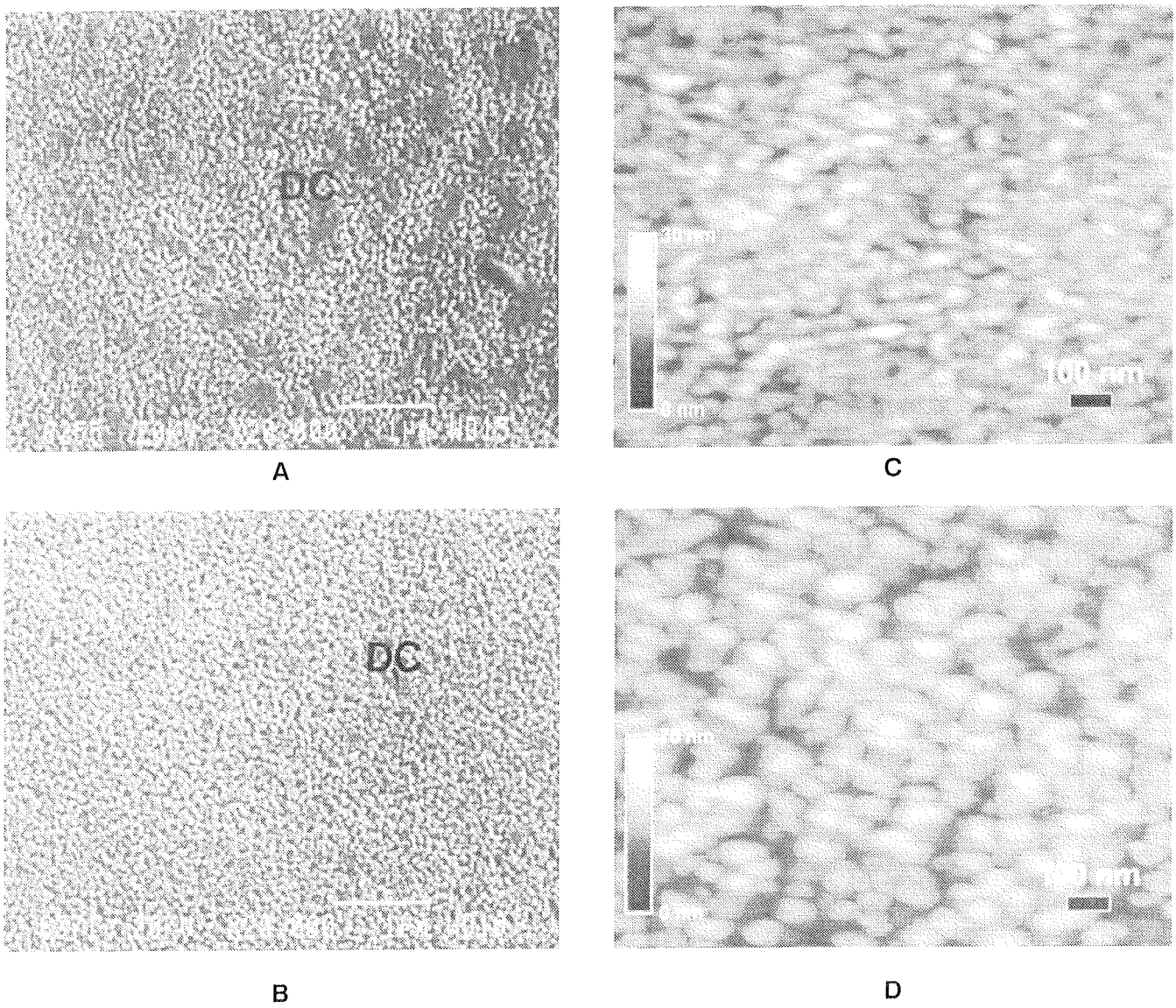


Fig 2. Morphology of potassium doped TiO_2 thin films fired at 650°C for 1 h. Samples were prepared from KOC_2H_5 doped sols.
A. KE/P0.0 (SEM image), B. KE/P4.0 (SEM image),C. KE/P0.0 (SPM image), D. KE/P4.0 (SPM image)

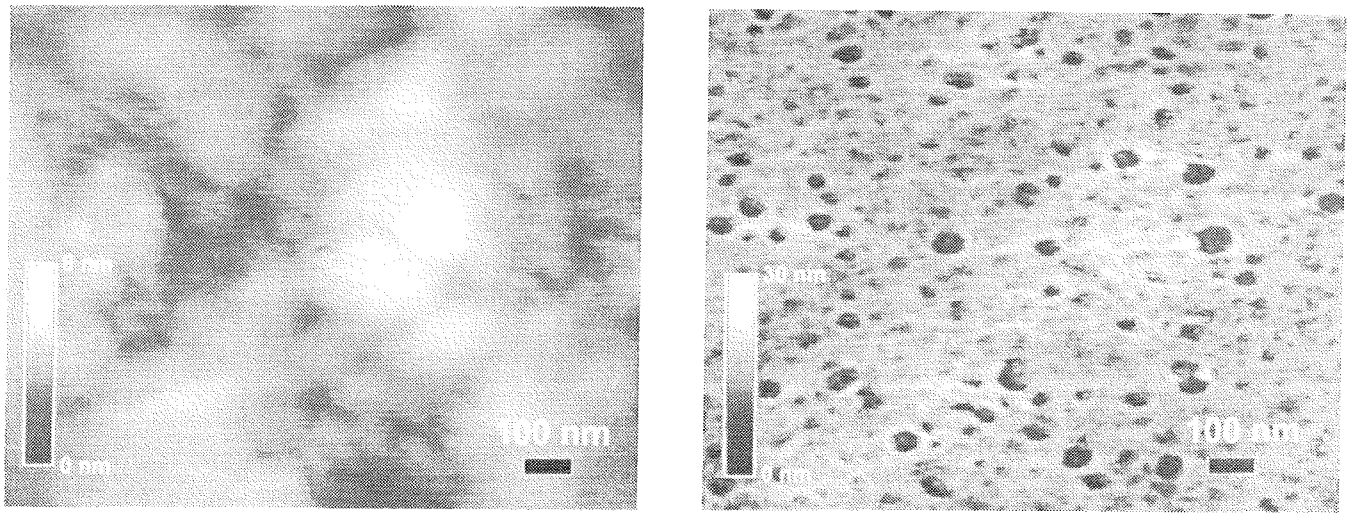
tration was increased to 4.0 wt. % (sample KE/P4.0 at Fig 2B), but their visibility was worse. EDX analysis revealed that concentration of K ions is higher in areas of different contrast (DC) than in the rest of the coating.

It is interesting that in spite of the fact that the PEG concentration in KE/P4.0 samples (Fig. 2B) was higher than in potassium undoped (NK/P2.4) samples (Fig 1B and 1C), no pores with higher diameter developed. The microstructure was still similar to the microstructure of the KE/P0.0 sample in Fig 2A.

It can be seen from these results that introduction of potassium compounds into the TTIP sols had a profound effect on the sample morphology. First, the formation of the pores in the samples with added potassium precursors was hindered with respect to the samples without K added. Second, the potassium doped samples fired at 650°C always exhibited the granular morphology whereas the undoped samples fired at same temperature (Fig.1A) had almost no granular texture.

Samples KE/P0.0 and KE/P4.0 fired at 450°C for 2 hours are presented in Fig 3A and B, respectively. TiO_2 thin films without added pore former (KE/P0.0) had no visible texture (Fig 3A). Topography of the sample varied in the range of 8 nm. TiO_2 coatings prepared from the precursor solution with PEG added (sample KE/P4.0) developed a different microstructure. As can be seen from the SPM micrograph in Fig 3B, there were pores in the coating. The pores were up to ~80 nanometres wide and ~20 nm deep. Segregation of potassium was not observed in these samples.

Dependence of the capacitance versus relative humidity for undoped TiO_2 thin films measured at 200 Hz and 25°C is presented in Fig 4. Samples NK/P2.4 and NK/P0.0, fired at 650°C for 1 hour, exhibit a change of capacitance only at high RH. There is almost no differ-



A B

Fig 3. Morphology of KE/P0.0 and KE/P4.0 samples fired at 450°C for 2h. A. KE/P0.0 (SPM image), B. KE/P4.0 (SPM image)

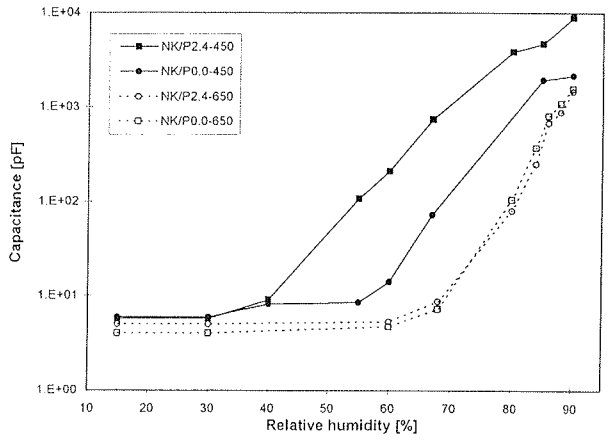


Fig 4. Dependence of capacitance vs. relative humidity for undoped thin films at 25°C. Sensors were fired at 650°C for 1h and at 450°C for 2h. The frequency of the applied field was 200 Hz.

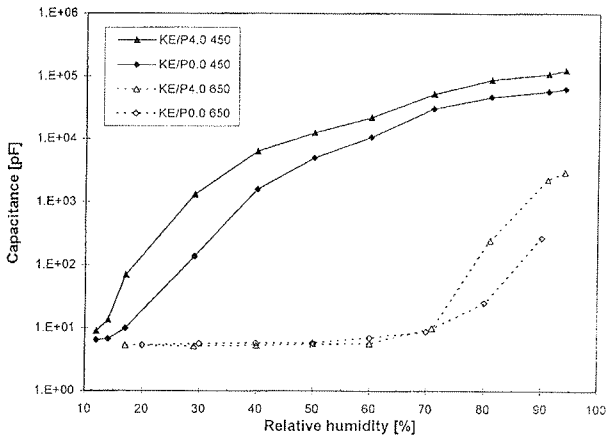


Fig 5. Dependence of capacitance vs. relative humidity for K doped thin films at 25°C. Sensors were fired at 650°C for 1h and at 450°C for 2h. The frequency of the applied field was 200 Hz.

ence between the samples. Thin films fired at 450°C exhibit higher sensitivity. The sensitivity of the samples with addition of pore former (sample NK/P2.4) is approximately for one order of magnitude higher than the sensitivity of NK/P0.0 sample. Dependence of the capacitance versus relative humidity for potassium doped TiO_2 thin films are presented in Fig 5 Samples KE/P0.0 and KE/P4.0, fired at 650°C for 1 hour, exhibit a change of capacitance only at high RH. The sensitivity of the samples to change of RH increased with addition of pore former (sample KE/P4.0) only for a relative humidity over 70 %.

The capacitance change for samples KE/P0.0 and KE/P4.0 fired at 450°C was 4 orders of magnitude between 15 and 90 % RH. Sample prepared from precursors with an increased concentration of PEG (KE/P4.0) had higher sensitivity in the range from 15 to 45 % RH than the KE/P0.0 sample. From 45 % RH, sensitivity of the KE/P4.0 sample decreased, and in the range from 50 to 95 % RH followed the sensitivity of the KE/P0.0 sample at higher capacitance level.

Frequency dependence of capacitance versus relative humidity for KE/P4.0 sample that was fired at 450°C, is presented in Fig 6 It can be seen that in the region from 15% RH to 60 % RH a sensitivity of KE/P4.0 sample decreases with increasing frequency of applied field.

On the one hand, the dramatic increase of sensitivity with decreased firing temperature could be explained by a coarsening of the microstructure at 650°C. At that temperature grains of TiO_2 are already well formed. Grains are also connected with necks (Fig 2C and 2D), in contrast to the sample films fired at 450°C which show

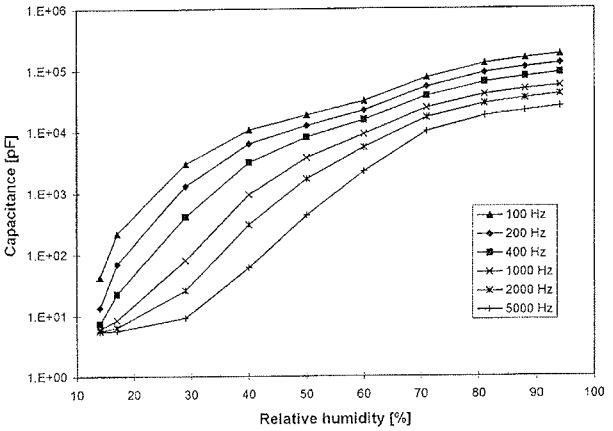


Fig 6. Dependence of capacitance vs. relative humidity for K doped thin films at 25°C measured at frequencies between 100Hz and 5000 Hz. Sensors were fired at 650°C for 1h and at 450°C for 2h

no grain morphology (Fig 3). It has been shown that formation of grain boundaries and ordering of the crystalline structure is able to block ionic conduction within the material /4, 5/. The authors /4/ showed that the free movement of alkali ions is necessary for exceptional conductivity of K doped TiO_2 thin films. The decrease of sensitivity could probably be also connected with the potassium segregation that can be observed in the samples fired at 650°C (Fig 2A and 2). Such segregation is not yet well understood, and further investigations are needed to explain it.

On the other hand, samples fired at 450°C show an exceptional change of capacitance in the entire RH range. This change could also be related to the increased number of water adsorption sites, due to the formation of a higher number of surface defect sites /2, 14/.

The presence of small pores in the KE/P4.0 sample fired at 450°C is probably responsible for the higher sensitivity of the thin film at lower relative humidity (below 45% RH) compared to the KE/P0.0 sample which was fired at the same temperature, and that has no visible porosity. Formation of grains and further coarsening of the sample microstructure (KE/P4.0) at 650°C probably resulted in the disappearance of the porosity that can be observed in Fig 3B. In any case, the porosity of the KE/P4.0 sample sintered at 650°C was still higher than the porosity of the KE/0.0 sample sintered at same temperature, and that probably resulted in higher sample sensitivity at a relative humidity over 70%RH.

Conclusions

Porous potassium doped and undoped TiO_2 thin films were prepared from alkoxide solutions by the spinning technique. The results showed that the formation of pores in the samples prepared from TTIP sols with potassium precursors added was hindered with respect to the samples prepared from TTIP sols without added potassium precursors.

Introduction of porosity in thin films had a positive effect on the humidity sensing characteristics of the potassium doped samples. Sol-gel processed, porous, and 10 at % potassium doped TiO_2 thin films heated to 450°C show an outstanding humidity sensitivity over the entire RH range. The change of capacitance was 4 orders of magnitude in the range from 15 to 95% RH.

Acknowledgments

The authors express their thanks to Dr. Enrico Traversa for providing substrates with sputtered Au electrodes. Financial support from the Ministry of Science and Technology of Slovenia is gratefully acknowledged.

References

/1/ B.M. Kulwicky, "Humidity Sensors", J. Amer. Ceram. Soc. 74 /4/, 697-708 (1991).
/2/ E. Traversa, "Ceramic sensors for humidity detection: the state-of -the-art and future developments", Sensors and Actuators B 23, 135-156 (1995).
/3/ N. Yamazoe, "Humidity sensors: Principles and Applications", Sensors and Actuators 10, 379-398 (1986).
/4/ E. Traversa, "Ceramic thin films by sol-gel processing as novel materials for integrated humidity sensors", Sensors and Actuators B 31 /1-2/, 59-70 (1996).
/5/ G. Gusmano, G. Montespirelli, P. Nunziante, E. Traversa, A. Montenero, M. Braghini, G. Mattogno, A. Berazotti, "Humidity-Sensitive Properties of Titania Films Prepared Using the Sol-Gel Process", J. Ceram. Soc. Jap. 101 /10/, 1095-1100 (1993).
/6/ J.C. Brinker, G.W. Scherer, Sol-Gel Science, Academic press, San Diego (1990) pp. 839-880
/7/ S. Ito, S. Tomotsune, N. Koura, "Preparation of vanadium doped rutile humidity sensor by dipping-pyrolysis process", Denki Kagaku 60 /6/, 474-9 (1992).
/8/ G. Montespirelli, A. Pumo, E. Traversa, G. Gusmano, A. Berazotti, A. Montenero, G. Gnappi, "Sol-gel processed TiO_2-based thin films as innovative humidity sensors", Sensors and actuators B 24-25, 705-709 (1995).
/9/ Y.C. Yeh, T.Y. Tseng, D.A. Chang, "Electrical Properties of TiO_2-$K_2Ti_6O_{13}$ Porous Ceramic Humidity Sensors", J. Am. Ceram. Soc. 73 /7/, 1992-98 (1990).
/10/ K. Katayama, K. Hasegava, Y. Takahashi, T. Akiba, H. Yanagida, "Humidity Sensitivity of Nb_2O_5-doped TiO_2 Ceramics", Sensors and Actuators A 24, 55-60 (1990).
/11/ K. Katayama, K. Hasegava, Y. Takahashi, T. Akiba, H. Yanagida, "Effect of Alkaline Oxide Addition on the Humidity Sensitivity of Nb_2O_5-doped TiO_2", Sensors and Actuators B 2, 143-149 (1990).
/12/ T. Seiyama, N. Yamazoe, H. Arai, "Ceramic Humidity Sensors" Sensors and Actuators 4, 85-96 (1983).
/13/ Y. Sadaoka, Y. Sakai, S. Mitsui, "Humidity sensor using zirconium phosphates and silicates. Improvements of humidity sensitivity", Sensors and Actuators, 13, 147-157 (1988).
/14/ F. Uchicawa, K. Shimammoto, "Time Variability of Surface Ionic Conduction on Humidity-Sensitive SiO_2 Films", Am. Cera. Soc. Bull. 64, 1137-1141 (1985).
/15/ K. Kato, A. Tsuzuki, Y. Torii, H. Taoda, "Morphology of thin anatase coatings prepared from alkoxide solution containing organic polymer, affecting the photocatalytic decomposition of aqueous acetic acid", J. Mat. Sci. 30, 837-841 (1995).
/16/ K. Kato, A. Tsuge, K. Niihara, "Microstructure and Crystallographic Orientation of Anatase Coatings Produced from Chemically Modified Titanium Tetraisopropoxide", J. Amer. Ceram. Soc. 79 /6/, 1483-88 (1996).

Dr. Jaroslav Slunečko,
Dr. Janez Holc,
Dr. Marija Kosec,
Dr. Drago Kolar
Institute "Jožef Stefan", Jamova 39,
1000 Ljubljana, Slovenija

Prispelo (Arrived): 06.09.99 *Sprejeto (Accepted): 15.09.99*

SMART INTEGRATED MAGNETIC SENSOR CELL

Janez Trontelj
Faculty of Electrical Engineering, Ljubljana

Keywords: magnetic sensors, smart sensors, integrated sensors, sensor cells, integrated HALL elements, electrical noise, noise optimization, autocalibration, sensitivity calibration

Abstract: The paper presents a design approach to an optimized integrated magnetic sensor cell. The cell is optimized for signal to noise ratio and for silicon area. A smart autocalibration is included to provide an output signal insensitive to process parameters variations, temperature variations, aging and stress caused by plastic packaging.

Celica pametnega integriranega magnetnega senzorja

Ključne besede: senzorji magnetni, senzorji pametni, senzorji integrirani, celice senzorske, celice magnetne, HALL elementi integrirani, šum električni, optimizacija šuma, kalibracija lastna, kalibracija občutljivosti

Izvleček: V članku je opisano načrtovanje optimizirane celice integriranega magnetnega senzorja. Celica je optimizirana glede razmerja signal šum in glede silicijeve površine. Pametna lastna kalibracija je vključena tako, da je izhodni signal neodvisen na variacije procesnih parametrov, variacije temperature, na staranje in na vplive pritiska zaradi zapiranja v plastično ohišje.

1 Introduction

Integrated Hall sensors offer very good offset voltage compensation. This is achieved by high frequency spinning of Hall element bias current.

The disadvantage of the Hall element is its relatively low sensitivity and consequently relatively poor signal to noise ratio. An improvement of signal to noise ratio was proposed /1/ by using N equal sensors. The signal to noise ratio is then improved by $\sqrt{N}$. For such optimization, a small silicon area of the sensor and the input amplifier is required.

The sensitivity of Hall sensor is linear function of its bias current. It is also temperature dependent and stress dependent. The stress introduced by packaging is changing both with temperature and time. To achieve the best results it is necessary to introduce a self calibration method.

2 Hall element spinning bias current and front end amplifier block

The aim of the proposed cell is to provide a maximum possible bias current for the given supply voltage. The other requirement is to design a block having a ratiometric sensitivity to the supply voltage. Additionally a design objective is to minimize the required silicon area, without loosing the performance of the block. This requirement is necessary to create a possibility to multiply the cell N times.

The schematic diagram of the described cell is shown in fig. 1.

The bias current of the spinned Hall element is determined simply by the ratio V_{dd}/R_h where V_{dd} is the supply voltage and R_h is the Hall element resistance, assuming that the R_{ON} resistance of the switches is very low compared to R_h.

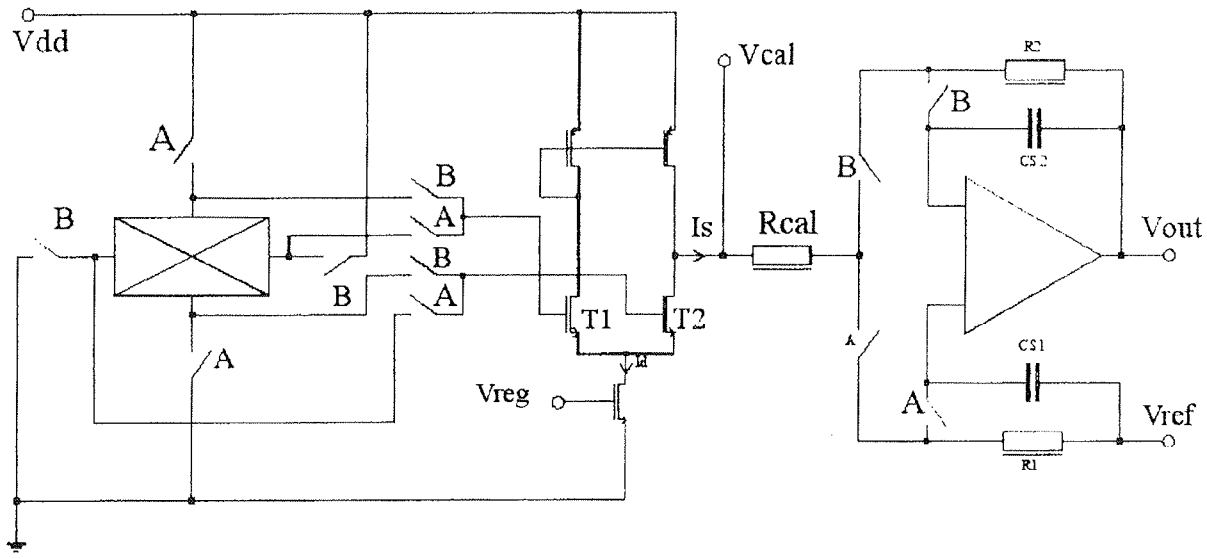


Fig.1: Hall element spinning bias current generation, front end amplifier and connecting amplifier.

The advantage of this approach is that all possible bias current for the given Vdd is flowing through Hall element. This advantage is quite substantial compared to constant bias current. When constant current bias is used it is usually only one third of total available current. This is caused by constant bias current electronic circuit which has to operate under all process corners and temperature variations.

The signal to noise ratio improvement of the proposed schematic is therefore up to three times.

The disadvantage of this approach is the fact that the bias current varies with the temperature coefficient of the well resistance. This temperature coefficient is very high and can not be easily compensated by autocalibration.

This temperature dependence is compensated by the arrangement shown in fig. 1. The resistors R1 and R2 are equal and realized as well resistors, i.e. having the same temperature dependence as R_h.

The Hall element voltage is given as:

$$V_h = B \cdot S_{h0} \cdot \frac{I_b}{I_0} = B \cdot S_{h0} \cdot \frac{k_0}{R_h} \qquad (1)$$

where B is magnetic field perpendicular to the surface of the chip, S_{h0} is Hall element sensitivity at constant bias current $I_o = 1/k_0$, and I_b is actual Hall element bias current.

The output current of the differential stage is given as:

$$I_S = g_m \cdot V_h = \sqrt{I_d \cdot k' \cdot \frac{w}{L}} \cdot V_h \qquad (2)$$

where g_m is transconductance of the differential transistors T1 and T2, I_d is bias current of the differential stage and w/L are the channel dimensions of transistors T1 and T2.

The output voltage V_{out} is:

$$V_{out} = I_S \cdot R1 + I_S \cdot R2 \qquad (3)$$

The resistors R1 and R2 are made equal and have the same temperature coefficient as Hall element resistance R_h so the output voltage is:

$$V_{out} = 2B \cdot S_{h0} \cdot k_0 \cdot \sqrt{I_d \cdot k' \cdot \frac{\omega}{L}} \cdot \frac{R}{R_h} =$$

$$= K(I_d, k') \cdot V_h = K(I_d, k') \cdot S_{h0}(T,P,t) \cdot B \qquad (4)$$

where K is a constant dependent on I_d and k' and S_{h0} is sensitivity of Hall element dependent on temperature (T), pressure (P) and time (t).

As seen from the equation 4 the most critical temperature and process dependence of the output voltage is replaced by constant ratio R/R_h which can be made very stable. The dependencies of the sensitivity due to mobility temperature coefficient and due to pressure variations are canceled by varying I_d in the selfcalibrating feed-back loop.

3 The offset voltage considerations

There are two most critical offset sources:

1. The offset of Hall element: V_{offh}
2. The offset of the front end differential stage: V_{offdif}.

The signal and the offset of Hall element seen at the input of the front end differential stage is:

$$V_A = V_{sig} + V_{offh}$$
$$V_B = -V_{sig} + V_{offh} \qquad (5)$$

where V_A and V_B denote the situation in spinning phases A and B.

This translates to the signal on resistors R1 and R2:

$$V_{R1} = K(V_{sig} + V_{offh} + V_{offdif})$$
$$V_{R2} = K(-V_{sig} + V_{offh} + V_{offdif}) \qquad (6)$$

In phase A the signal V_{R1} is sampled on capacitor C_{S1} and the operational amplifier is in voltage source configuration, i.e. the gain is +1.

In the spinning phase B the current S flows through resistor R2 and is sampled on capacitor C_{S2}. In this configuration the gain is -1 so the output is simply:

$$V_{out} = 2 \cdot I_S \cdot R \qquad (7)$$

where R = R1 = R2 and both offsets are subtracted. The efficiency of the subtraction is given by common mode rejection factor of the operational amplifier.

4 Autocalibration

The autocalibration is performed by generation of on board reference magnetic field /2/, /3/. This is done by integrated coils as shown in fig. 2.

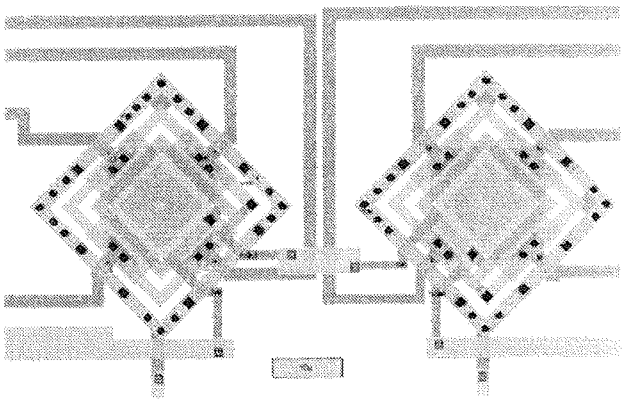


Fig. 2: Hall element pair with integrated coil for reference field generation.

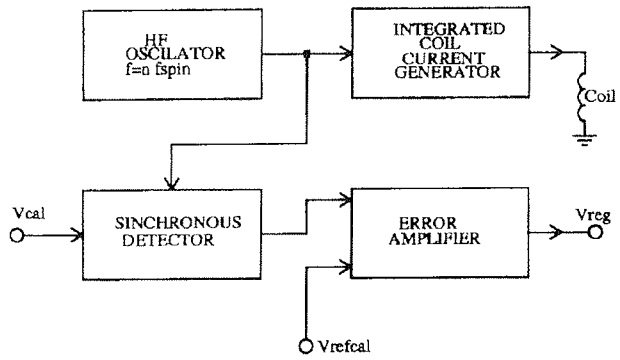


Fig. 3: Block diagram of magnetic sensitivity correction.

The block diagram of the autocalibration loop is shown in fig. 3.

The calibration current frequency is n times higher than the spinning frequency so it can not be seen on V_{out}.

The resistor R_{cal} is inserted to see high frequency signal V_{cal}. The phase of the reference field generation is inverted according to the spinning phase so no phase jump is seen on V_{cal}.

The signal V_{cal} is an AC signal which is effectively rectified by synchronous detector. An error amplifier compares this rectified signal and regulates the gain of the input differential stage by varying its bias current I_d.

5 Conclusions

An effective magnetic cell has been developed. It offers up to three times lower noise than the conventional approach.

The offset voltage is canceled by spinning and by introduction of a new differential sample and hold stage. The autocalibration is achieved by on board generation of the high frequency reference magnetic field.

References

/1/ J. Trontelj, "Optimization of Integrated Magnetic Sensor by Mixed Signal Processing", Proc. of 16th IEEE International and Measurement Technology Conference, IMTC´99, Venice, Italy, pp299-302, 1999

/2/ J. Trontelj, R. Opara, A. Pleteršek, "Integrirano vezje magnetnega senzorja", Patentna listina št. 9300622, 1995

/3/ J. Trontelj, "Integrirano vezje z magnetnimi senzorji, obdanimi s testnimi tuljavicami", Patentna prijava št. 99 0 0094, 1999

Dr. Janez Trontelj
Fakulteta za elektrotehniko in računalništvo
Tržaška 25
1000 Ljubljana

Prispelo (Arrived): 10.8.99 *Sprejeto (Accepted): 15.9.99*

DESIGN CONSIDERATIONS OF LOW POWER MIXED SIGNAL FRONT-END FOR VOICE APPLICATIONS

Drago Strle
Faculty of Electrical Engineering, Ljubljana, Slovenia

Keywords: semiconductors, microelectronics, IC, integrated circuits, telecommunications, CMOS, Complementary Metal Oxide Semiconductors, circuit design, low power design, LV, Low Voltages, mixed analog digital integrated circuits, A/D converters, analog/digital converters

Abstract: Design considerations for low-voltage, low-power mixed signal front-end is presented in the article. Combined with digital decimation and interpolation filters it can be used as an embedded voice CODEC cell. Architecture and circuit design considerations to achieve low-power and low-voltage of important analog and mixed signal modules are described. Simulation and measured results demonstrate that circuit can operate from a single 1.2V supply voltage with quiescent power consumption of less than 4mW. The front-end layout area including periphery occupies about 4mm^2 and is fabricated in 0.35μm double poly, triple metal CMOS technology.

Načrtovanje analogno-digitalnega vmesnika z nizko porabo moči

Ključne besede: polprevodniki, mikroelektronika, IC vezja integrirana, telekomunikacije, CMOS polprevodniki kovinskooksidni komplementarni, snovanje vezij, snovanje za moči male, LV napetosti nizke, IC vezja integrirana mešana analogno digitalna, A-D pretvorniki analogno-digitalni

Povzetek: članek opisuje načrtovalske postopke pri načrtovanju mešanega analogno digitalnega integriranega vezja, ki deluje pri nizki napajalni napetosti in ima majhno porabo moči. Skupaj z digitalnim decimacijskim in interpolacijskim filtrom je uporaben kot "makro" celica CODEC. Predstavljena je arhitektura in načrtovalski postopki nekaterih pomembnih sklopov, ki sestavljajo vezje. Simulacijski rezultati dokazujejo, da predstavljeni moduli lahko delujejo pri napajalni napetosti 1.2V in pri porabi manšji od 4mW. Celotno vezje vključno s periferijo zaseda približno 4mm^2 silicija v tehnologiji CMOS z dolžino kanala 0.35μm, dvemi nivoji polisilicija in tremi nivoji metalov.

1 Introduction

Reducing power consumption in a mixed-signal integrated circuits is usually accomplished by reducing supply voltage as much as possible because in digital circuits power consumption is quadratically related to the supply voltage. Voltage reduction is limited by the analog portion of the circuit because of operating points and because of S/N ratio reduction. Decreasing noise level requires more area and more power consumption unless some clever system and circuit design tricks are used. Supply voltage is optimized in such a way that power is minimized while required characteristics are achieved. Using short channel CMOS process means, that matching accuracy of resistors, capacitors and MOS transistors are improved considerably while noise characteristics remains almost the same.

In this article circuit design considerations for low-power, low-voltage analog front-end that can be used in various voice integrated circuits are presented. The circuit is fabricated in 0.35μm CMOS technology and used together with digital decimation and interpolation filters as an embedded CODEC cell. For portable devices the most important characteristics is low power consumption to support extended life of the battery, so it is important that power optimization is carried out on all levels of the hierarchical design procedure. This includes selection of appropriate technology, architecture of the system and analog and/or mixed signal modules, minimization of power supply voltage and optimized circuit and layout design technique.

Section II describes typical mixed-signal front-end system for voice applications. In section III some basic design considerations for reduction of power consumption in a mixed-signal integrated circuits are presented. For voice frequency signal processing the supply voltage of a digital module can be lower than for analog modules because of small speed demands, so minimum supply voltage is determined by the analog modules requirements if common supply voltage is used. Most of the section III is reserved for describing selection of appropriate architecture and circuit design technique of critical analog modules such as modulator, band-gap reference and low noise microphone amplifier, having in mind low supply voltage and power consumption, while power buffer circuit design issues will be published in a separate article because of complexity of the problem. Some simulation results are presented in this section. Section IV summarizes experimental results of complete analog front-end.

2 System description

Figure 1 shows block diagram of an analog front-end of the embedded CODEC cell /4/. Microphone signal is amplified by programmable gain, low noise microphone amplifier, which adapts weak signal level of the electret microphone appropriately for modulator's 13 bits S/(N+D) ratio and linearity. Supply voltage for electret microphone is extracted from the band-gap reference circuit and buffered. Band-gap circuit also supply Σ - Δ A/D and D/A converters with appropriate differential reference voltages of Vref = $\pm$0.3V. Spectrum of the signal from microphone amplifier is limited by anti-aliasing filter which attenuates out of band spectral components; it is than sampled by input S-C stage of the Σ - Δ modulator, which converts analog signal into the bit-stream and is filtered by hard wired digital sinc^3 decimation filter followed by digital filter for band

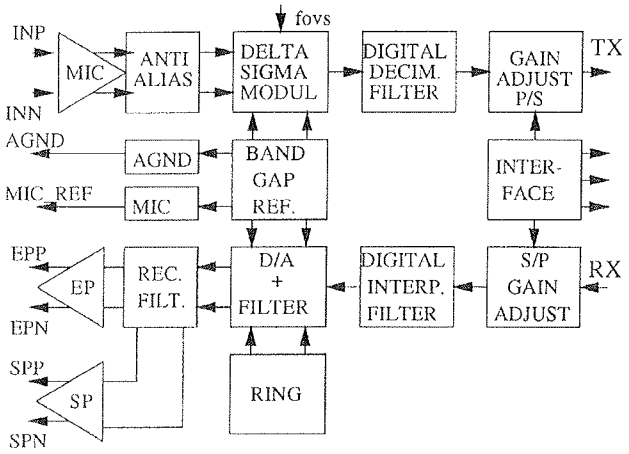


Fig. 1: Block diagram of mixed signal part of the embedded CODEC cell

limiting voice signal to 300-3400Hz band. Digital multiplier provides fine gain adjustment of the transmit gain. Digital voice signal is converted to 8 bit code (A- law or μ - law) and serially sent to the TX output, which can than be processed by appropriate DSP algorithm defined by the application.

On the receive side serial signal is coming from the DSP (dependent on the application) to the RX input where it is converted to 8 bits parallel code and than to 13 bits linear code (A- law or μ - law) running at 8kHz. Fine gain adjustment is followed by digital interpolation filter and digital Σ - Δ modulator, which increase the oversampling rate to approximately 1MHz and reduce number of bits to 1 by appropriate noise shaping; 1 bit D/A and 2´nd order Chebishev S-C filter followed by a 1´st order continuous time reconstruction filter produce voice band signal with correct spectrum, so that S/N ratio requirements of the receive section are full-filed. The signal is than buffered by 2 on chip power buffers; one can drive 300Ω headphones and has a programmable gain, while the other has a fixed gain and is capable of driving 50Ω loudspeaker.

3 Reduction of power consumption in mixed-signal IC

The most efficient way to reduce power consumption in a mixed-signal integrated circuit having big DSP and just small analog or mixed signal front-end is reduction of supply voltage. In a digital part of the circuit power consumption is quadratically related to the consumption approximately following the equation:

$$P = V^2 \Sigma_i C_i \beta_i f_i,$$

where β_i is a factor between 0 and 1 dependent on activity of the digital node i, C_i is the load capacitance of node i, f_i is the frequency of switching at corresponding digital node and V is constant supply voltage. From this equation it is clear that several possibilities exist to reduce power consumption. By using short channel technology and appropriate layout, node capacitances C_i can be reduced, by appropriate algorithm factor β_i and maybe f_i can be reduced. So it is very important to select appropriate architecture. Reduction of supply voltage is the most efficient way to reduce power consumption because its effects are related quadratically.

Using short channel technology forces to use low V_{sup} because of reduced break down voltages. The area of a digital module is directly related to the minimum channel length. Comparing the area needed to draw D type flip-flop cell in a 0.6μm and in a 0.35μm CMOS technology shows that the area is approximately 3 times smaller for later technology. Because the price of processing is not higher for the same factor it is clear that for digital circuits the realization is in favor to the short channel technology. It is not so for the isolated analog portion of the circuit but because the area of analog part is relatively small compared to the on chip digital DSP in a typical "voice" application, total area reduction still follows the rule and using short channel technology and low supply voltage is feasible.

The reduction of supply voltage has its limitations both in digital and analog modules of a mixed signal circuits as it will be presented in next subsections 3.1 and 3.2. Low supply voltage limit is defined by the analog portion of the chip because it needs bigger supply voltage compared to digital circuits. The baseband speed requirements for voice digital signal processing is not very demanding. Low supply voltage limit can be determined from required signal dynamics, speed, driving requirements, technology parameters etc.

3.1 Supply voltage influence on digital modules

Several mechanisms are responsible for power consumption in a digital IC /11/. The biggest contribution is the dynamic current needed for charging and discharging capacitive loads (gates, interconnect and parasitics) than current between supplies when both P and N channel transistors are switched on (careful design can reduce this current below 10% of the total consumption) and sub-threshold leakage which is dependent of the technology. Because power consumption of a digital circuit is quadratically related to the supply voltage minimum possible supply voltage must be used.

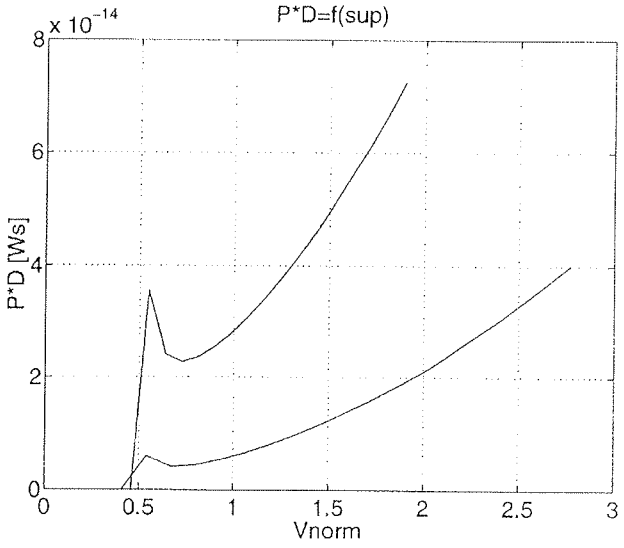


*Fig. 2: P*D product as a function of normalized supply voltage*

To determine appropriate supply voltage for digital part of a mixed-signal circuit for selected technology we performed a simulation of a simple inverter loaded with 3 inverters of the same size (C_{norm} = 3). On figure 2 PD (power*delay) product is plotted as a function of normalized power supply voltage ($V_{norm}=V_{sup}/(V_{THn}+V_{THp})$, with V_{THp} and V_{THn} threshold voltages of P and N channel MOS transistors, V_{sup} is supply voltage and V_{norm} is normalized supply voltage) as a function of supply voltage of loaded inverter for 0.6μm (upper curve) and 0.35μm (lower curve) CMOS technology. The dimensions are scaled in such a way that propagation delays are approximately the same at V_{sup} = 3V. From this figure we can conclude that the smallest supply voltage must be bigger than $0.8(V_{THn} + V_{THp})$ and that this is valid as long as the propagation delay is smaller than t_{pdmax}, which is a design parameter defined by the algorithm which has to be executed on this logic. For real technology with threshold voltages around $V_{THn} = |V_{THp}| = 0.6V$ the supply voltage must be bigger or equal to $V_{sup} \geq 1V$. For analog part of a mixed-signal circuit this supply voltage is not big enough for proper operation as will be explained in next subsection.

3.2 Supply voltage influence on analog and mixed signal modules

Real limitation to a minimum supply voltage is proper operation of analog or mixed signal modules under low voltage constraints. The following modules from the block diagram determine minimum supply voltage: band-gap reference, modulator, power amplifier and low noise amplifier. To avoid on chip supply voltage multipliers (they require additional power and silicon area and possibly external capacitors) careful evaluation of possible architectures and optimum circuit design is needed. The designer must take care of the following design issues when trying to design analog or mixed-signal circuit at low supply voltage:

- architecture of the module,
- dynamic range, noise and power consumption,
- switch ON impedance,
- selection and design of appropriate OTA or OPAMP to optimize power consumption, noise, driving capability etc.

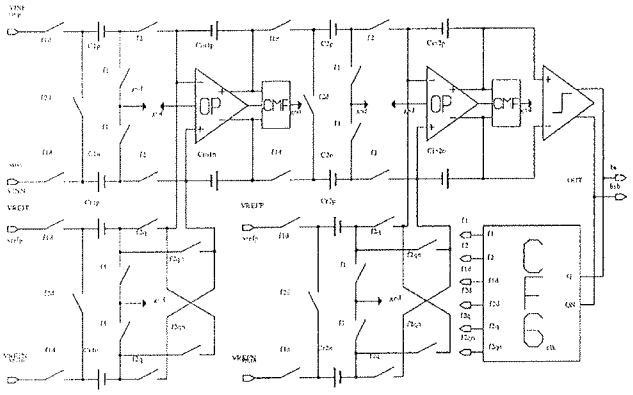


Fig. 3: Simplified circuit diagram of the modulator

Selection of appropriate architecture of the mixed-signal module (for example modulator) is a separate issue, which is beyond the scope of this article. Second order S-C modulator was selected because of reliability and inherent stability of the loop /7/ (figure 3). Its operation is described in literature. At low supply voltage max. signal is limited by proper operation of the circuit and by required dynamic range.

3.2.1 Dynamic range and power consumption of the modulator

Dynamic range is defined as a ratio between signal and noise power: DR = 10 log(S/N). Signal power is proportional to the supply voltage and efficiency factor β (β = 0.....1), which tells us how close to the supply voltage the signal can be (dependent of the circuit): $S=(\beta V_{sub}/\sqrt{2})^2$. Noise power is composed of several sources:

- $kT/C_{in}D_{ovs}$ and $kT/C_{ref}D_{ovs}$ are aliased thermal noise sources of the input and reference feedback S-C stage, which are the dominant noise sources; k is Boltzman´s constant, T is absolute temperature, C is input capacitor, $D_{ovs} = f_{ovs}/2f_0$ is the oversampling ratio and C_{in} and C_{ref} are input and reference S-C stages. The contributions of other S-C stages are smaller because they are multiplied by appropriate noise shaping transfer function weight.
- Noise of the first OPAMP of the modulator
- Noise of the microphone amplifier
- Noise of the band-gap reference circuit

We can assume equal thermal noise contribution from each source, so $N_{S-C}=N_r/5$; where N_r is required noise power obtained from the dynamic range specification of the system (DR from equation 1). If higher dynamic range is required at fixed V_{sup} and β the capacitance C of the S-C stage must be increased to reduce kT/C noise. If we assume simple model of class A OTA where supply current required for proper operation is proportional to $I_{sup} = k_I g_m (V_{gs}-V_{TH})$ (g_m is a transconductance and k_I is a constant, V_{gs} and V_{TH} are gate-source and threshold voltage of the differential stage transistors) and simple dominant pole model of the OTA where $g_m=k_f C f_{ovs}$ (k_f is constant, C is load capacitor of the OTA and f_{ovs} is oversampling frequency) than for higher load capacitance higher g_m is required, which can be achieved only by increased supply current Isup at fixed oversampling ratio and fixed V_{sup}. Power consumption of the S-C stage of the modulator is proportional to (equation 1):

$$P = \gamma\left(\frac{kT2f_0 10^{\frac{DR}{10}+1}}{\beta^2 V_{sup}}\right)(V_{GS} - V_{TH}) \qquad (1)$$

where: k is Boltzman´s constant, T is absolute temperature, f_0 is Nyquist frequency, DR is required dynamic range of the system and γ is a constant dependent on the type of OTA or OPAMP. We have several options to reduce power consumption:

- Higher V_{sup} gives smaller power consumption of the mixed-signal S-C modulator. It is thus recommended to have as big supply voltage as possible to increase

the dynamic range. This is so because by increasing supply voltage we can reduce capacitances of the S-C stages to achieve the same dynamic range and thus reduce the current. The limit of that optimization is the accuracy of the capacitor ratio, which is on the lower side limited by the technology. Because this analog front-end must coexists with big digital circuit where power consumption and supply voltage are related quadratically the optimum is dependent on the application and technology. Usually the V_{sup} is also defined by other components of the system, so careful evaluation of all design constraints and limits are necessary.

- β is important factor because it is squared, so it must be as close to 1 as possible, which means that the signal swing must be as close to the supply voltage as possible ($\beta = 1$ means that $V_{sig} = V_{sup}$). This can be achieved by careful selection of the architecture and circuit design of the modules.
- Power consumption is linearly dependent of γ. By selecting different kind of OTA (for example class AB) we can reduce γ and thus power consumption.

For good power optimization, careful considerations of each S-C stage aliased thermal noise contribution is necessary. For properly designed signal and noise transfer functions of the modulator only the contributions of the first stages enter the loop directly while the others are multiplied by appropriate noise transfer function weights, which means that the capacitances of the following stages of the modulator can be much smaller than in the first stage and limited only by the ratio accuracy requirements defined by the stability of the modulator´s loop and gain accuracy requirements.

3.2.2 Switch ON impedance

To increase signal swing in the S-C circuit, analysis of the switch ON resistance is necessary. Usually the switch is built of P and N MOS transistors of equal dimensions in parallel to reduce clock-feed-through effect /8/. Figure 4 shows setup for measuring ON resistance of the switch. Gate and body are connected to corresponding supply voltages, while input voltage is changing from gnd to V_{sup}. Figure 5 shows a conductance of the NMOS transistor (circles), PMOS transistor (stars) and combined conductances (solid line) as a function of normalized input voltage (V_{in} / V_{sup}) for two

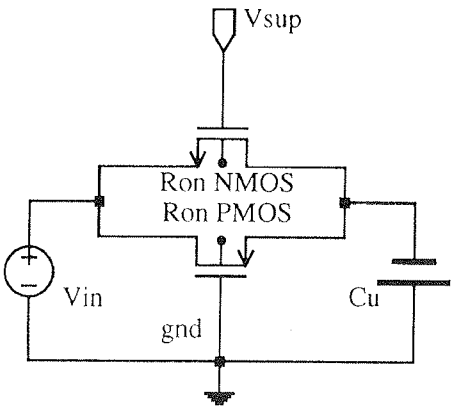


Fig. 4: Circuit for measuring switch ON resistance

supply voltages: V_{sup} = 4V and V_{sup} = 1V. When $V_{sup} \leq V_{THPef} + V_{THNef}$ (V_{THPef} and V_{THNef} are effective threshold voltages including body effects) a range of input voltage exists on the bottom part of the figure 5 where both transistor are off, so correct operation of the switch is not possible. The gate-source voltage must be big enough to prevent OFF condition and to reduce ON resistance according to the settling time requirements, having in mind that the switch dimension must be as small as possible to reduce clock-feed-through effects. This can be achieved on the following three ways: Increasing the supply voltage of the whole analog section, use of different technology with low V_{TH} or use the same supply voltage for analog and digital portion of the chip and increase only the control voltages for the switches. We used last possibility taking into considerations also reliability issues /5/, /1/, which means that terminal voltages V_{gs}, V_{gd} and V_{ds} are limited to rated operating conditions for the technology and controlled by appropriate layout. Clock form generator is realized as suggested on figure 6. Only N-channel MOS transistors are used as switches together with a circuit for clock-feed-through cancellation using MOS transistors

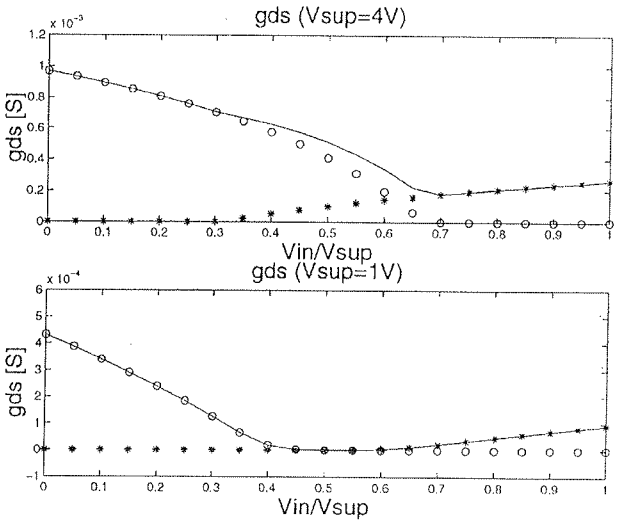


Fig. 5: Conductance of the switch

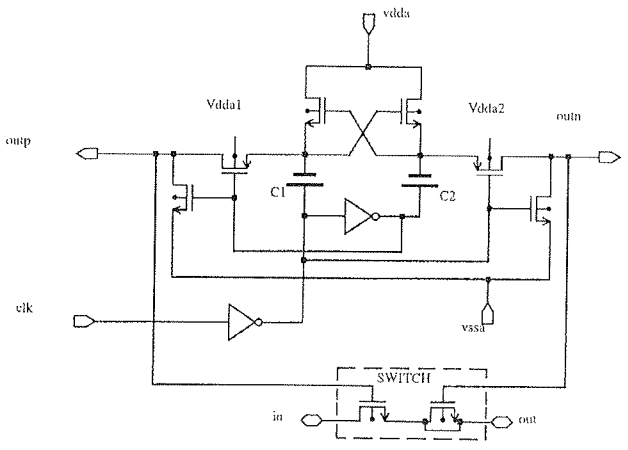


Fig. 6: Circuit for switch gate voltage multiplication

with short circuit between drain and source, driven by opposite clock and having two times smaller dimensions compared to the switch. The gate-source overdrive voltage is limited because capacitors C1 and C2 are selected according to the number of gates and parasitic capacitances connected to the clock phase. Using appropriate layout and careful evaluation of the parasitic capacitances of the clock lines we can assure that clock phase voltage V_{gs} of any switch never exceed allowed maximum voltage (for selected CMOS technology this is: $V_{sup} < 3.6V$). If signal ground is selected at: $V_{agnd} = 0.4V$ and signal swing: $V_{sig} = \pm 0.3V$ the opamp can operate under all conditions and clock voltage of $V_{clk} = 2.4V$ is sufficient to have good over drive of the switch: $0.9 \leq (V_{gs} - V_{THnef}) \leq 2.1V$. Body of MP1 and MP2 are connected to supply voltage Vdda1 and Vdda2 which are generated by similar on chip voltage multiplication circuit as used for the clock phases of the modulator except that these are stable voltages.

3.2.3 Design of modulator´s OPAMP

The modulator´s OPAMP topology can be selected according to the following requirements: $V_{sup} \geq 1.2V$, as big signal swing as possible, low frequency gain $A_0 \geq 60dB$ determined by the modulator´s gain accuracy and stability requirements, as small quiescent supply current as possible, noise better than $100nV/\sqrt{Hz}$ in a 4kHz band (from DR requirements and $V_{sigmax} = 0.3V$) and 0.1% settling time better than $t_{set} \leq 400ns$ for $f_{ovs} = 1MHz$. Because of PSRR requirements (/10/, /3/) fully differential 2 stage topology is selected with P channel folded cascode differential stage and class A common source output stage /9/. Simplified circuit diagram of the modulator´s opamp with cascode compensation is shown on figure 7. Fully differential switched capacitor common mode feedback circuit (not shown on the figure) is driven by similar multiplied clock form generator as used for the modulator. A careful circuit design ensures that signal swing is maximized. A PMOS differential transistors are used for two reasons: to improve PSRR by connecting sources of the differential stage transistors M1 and M2 to their body (N-well) and not to a noisy substrate, while another reason is proper operation of differential stage at low supply voltage. The signal ground voltage V_{agnd} is selected in such a way that transistors M_1 and M_2 are operating in moderate inversion, while M_3 is operating in strong inversion: $V_{agnd} \leq V_{sup} - |V_{THM1}| - V_{dsatM1} - V_{dsatM3} = 0.4V$, assuming $V_{THM1} = 0.6V$ with saturation voltage of 100mV. For

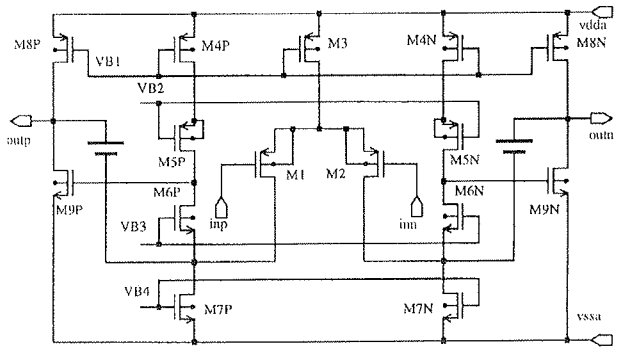


Fig. 7: Opamp of the modulator

voice applications the noise requirements of the modulator´s opamp is not very demanding because 1/f noise is suppressed by digital high-pass filter, while thermal noise requirement is important only for the first OPAMP. Based on noise simulations of the modulator /2/ minimum capacitance of the first S-C integrator was selected as $C_{in} = 0.3pF$, which is sufficient to maintain dynamic range of the modulator´s first integrator. Maximum load on each output of the first opamp (gain of the modulator is 1) is thus $C_{load} = C_{int} + C_{in} + C_{cm} + C_{par} \sim 1.2pF$, where $C_{int} = 2C_{in} = 0.6pF$ is integrator capacitance, $C_{in} = 0.3pF$ is input S-C stage capacitance, $C_{cm} = 0.2pF$ is common mode feedback capacitance and $C_{par} = 0.1pF$ is parasitic capacitance. According to the HSPICE simulations the first integrator consumes approximately 0.2mW at this capacitive load while the second integrator requires only 0.1mW because of 2 times smaller capacitances.

3.2.4 Design of band-gap circuit at low supply voltage

Curvature compensated band-gap voltage is usually built as: $V_{bg} = V_{be} + n\Delta V_{be} \cong 1.22V$ in such a way that temperature coefficient is equal zero at T = 25°C, where: $V_{be} = (kT/q)\ \ln(I/I_S)$, $k = 1.38 \times 10^{-23}$ J/K, $q = 1.6 \times 10^{-19}$C, T is absolute temperature, n is a factor which is selected so, that the TC = 0 at 25°C (usually by resistor ratio), $\Delta V_{be} = V_{be1} - V_{be2} = (kT)/q\ \ln(N)$ and N is the number of forward biased parallel diodes when $I_1 = I_2$ or in other words the ratio of current densities in bipolar transistors Q_1 and Q_2: $N = (JQ_1)/(JQ_2)$. Supply voltage of the original band-gap circuit must be bigger than V_{bg} for proper operation, so $V_{supp} \geq 1.4V$ is required when built in a standard way. Different kind of circuitry must be used for lower supply voltage, which generates smaller reference voltage. Figure 8 shows simplified circuit, which generates reference voltage smaller than 1.22V having similar characteristics as the original band-gap reference circuit (additional circuit for startup and trimming is not shown because of clarity of the figure) and is similar to one described in /6/. The circuit is best described by the following set of equations and assumptions:

- $I_1 = I_2 = I_3$, $V_a = V_b$ (ideal amplifier),
- $R_1 = R_2$,
- $I_1 = I_{1A} + I_{1B}$, $I_2 = I_{2A} + I_{2B}$,
- $I_{1A} = I_s\left(e^{\frac{qV_{be}}{kT}} - 1\right)$, $I_{1B} = \frac{V_{be}}{R_1}$
- $I_{2A} = \frac{\Delta V_{be}}{R_3}$, $I_{2B} = \frac{V_{be}}{R_1}$,
- $\Delta V_{be} = V_{be1} - V_{be2} = \frac{kT}{q}\ln(N)$

and equation 2:

$$V_{ref} = (I_{2A} + I_{2B})R_4 = \frac{R_4}{R_2}\left(V_{be} + \frac{R_2}{R_3}\Delta V_{be}\right) \qquad (2)$$

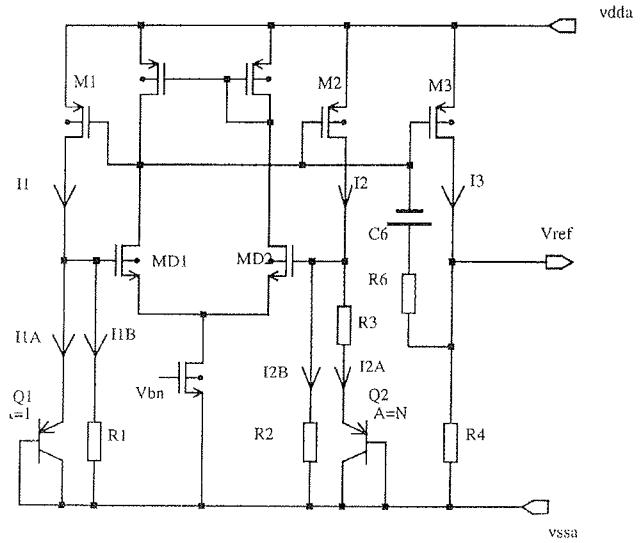


Fig. 8: Band-gap circuit with V_{ref} = 0.6V

This reference voltage is smaller than original reference by a factor R_4/R_2 and has approximately the same characteristics, which is to the first order independent of the absolute values of the resistors. Minimum supply voltage required for this circuit must be bigger than $V_{sup} \geq V_{be}+V_{dsat}$ = 1.0V, where V_{bemax} = 0.85V at T= -40°C and V_{dsat} is minimum saturation voltage of the current source transistor M_1. Another limitation is the amplifier operating point; the only comment necessary is that $V_{be} \geq V_{THMD1} + 2V_{dsat}$, which is possible to achieve with 0.35μm CMOS technology having maximum threshold voltage of V_{TH} = 0.6V and $V_{dsat} \geq$75mV. Because temperature coefficient of forward biased diode voltage is $TC_{Vbe} \cong$ -2mV/°C and temperature coefficient of threshold voltage of the MOS transistor $TC_{VTHn} \cong$ -1.1mV/°C the circuit has 2 limitations: at low temperature forward biased diode voltage is at maximum (for example at temperature -40°C the $V_{be} \cong$ 0.8V)

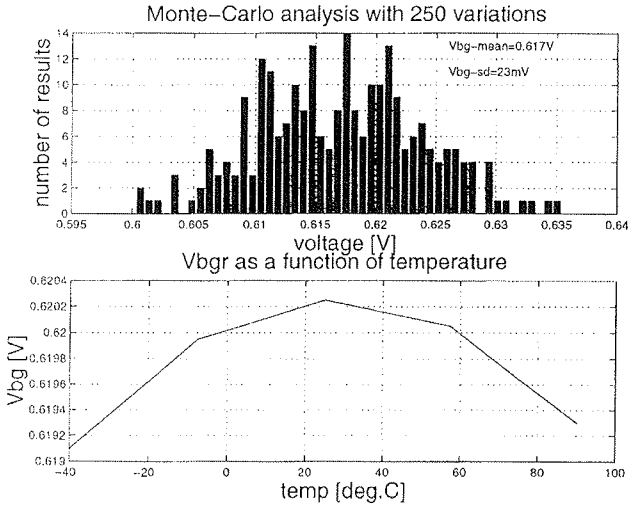


Fig. 9: Temperature behaviour and spread of reference voltage

and at high temperature (for example at T = +90°C $V_{be} \cong$ 0.58V). In first case the limitation is supply voltage and in last case the problem might be proper operation of operational amplifier when threshold voltage of transistor MD1 is at maximum. Carefully designed circuit maintains both conditions.

Having in mind considerations and limitations from the previous paragraph we built band-gap reference circuit which works correctly at $V_{sup} \geq$ 1.2V under all conditions having reference voltage of $V_{ref} \cong$ 0.6V. Figure 9 shows simulation results of temperature behavior and Monte Carlo analysis of the proposed band-gap reference circuit. It has the following characteristics: V_{ref} = 0.6V ± 23mV, TC ≤ 50ppm and current consumption is I_{sup} ≤ 5μA. Compensation of the feedback loop is achieved by pole-zero compensation scheme using R_6 and C_6. A reference voltage must be buffered for further use in A/D and D/A converters.

3.2.5 Low noise programmable gain amplifier

The design of low noise programmable gain amplifier is based on fully differential difference amplifier with programmable resistive feedback circuitry. Required average equivalent input referred rms noise voltage density in a band of interest (B ≅ 3.1kHz) can be calculated according to the equation 3:

$$V_n = \frac{\sqrt{2}V_{sig}}{G\sqrt{B}} 10^{\frac{DR+10}{20}} \cong 18\frac{nV}{\sqrt{Hz}} \qquad (3)$$

where V_{sig} = 0.3V is signal swing, G = 20 is required max. gain of the amplifier, B = 3100Hz is a bandwidth, DR = 76.5dB is required dynamic range of the front-end and √2 is added because of fully differential structure. The architecture of the amplifier is similar to the one used for the modulator with the difference of having 2 big differential stages: one used for feedback and the other for input connection. The common mode feedback is realized by resistive divider, separate differential stage and circuit which controls the current through n-channel folded cascode stage. Simplified circuit diagram of this amplifier is presented on figure 10. To reduce thermal noise, current through the differential stage is 300μA and the transistor sizes are 2000um/2um. The microphone amplifier alone consumes 800uA to achieve required noise characteristics

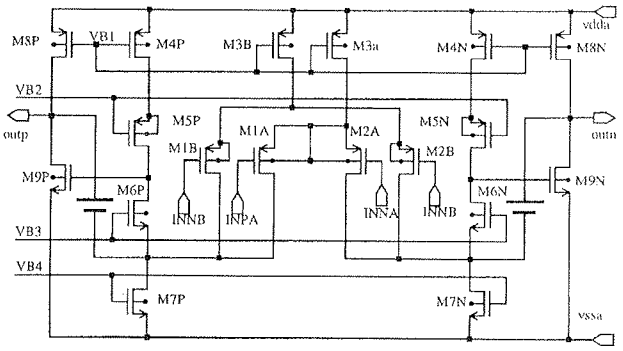


Fig. 10: Simplified circuit diagram of low noise amplifier

(simulation result). The gain is programmable from 0dB to 30dB in 6dB steps. The following characteristics were measured: Vn ≅ 20nV/√Hz which is slightly worse than predicted by the simulations, harmonic distortions at min. gain and max. output signal (0.3V around signal ground) produce HD ≤ -30dB while at bigger gain and smaller input signal the distortions are smaller. Current consumption of amplifier alone was not possible to measure.

4 Conclusions

Design considerations of important modules needed to implement low-power, low-voltage analog front-end, which can be used in various voice integrated circuits are presented in the article. The selection of appropriate architecture and circuit design strategy used during the design phase of some of the modules is presented together with some simulation and measurement results. The operation of the CODEC targeted to V_{sup} = 1.2V is not yet possible for all modules (for example power buffer still need $V_{sup} \geq 1.5V$ for proper operation) and need further innovative effort. The measurement of the complete front-end was thus obtained at $V_{sup} \geq$ 1.5V. Quiescent current consumption is $I_Q \cong 2.5mA$ giving adequate max. dynamic range of DR ≥ 75dB.

REFERENCES

/1/ A.M. Abo and P.R. Gray, "A 1.5V, 10-bit, 14.3 ms/s CMOS pipeline analog-to-digital converter", IEEE JSSC, 34, No.5, 599-606, 1999

/2/ D. Strle, "Noise modeling and simulation of high resolution delta-sigma A/D converters", Proceedings of the 33rd Int. Conference on Microelectronics, Devices and Materials, MIDEM´97, Gozd Martuljek, 157-163, 1997

/3/ D. Strle, "Reduction of Crosstalk in Mixed Signal Integrated Circuits", Proceedings of the International Symposium on VLSI Technology, Systems, and Applications, Taiwan, 74-78, 1997

/4/ D. Strle, A. Pleteršek, K. Riedmuller, T. Karema, "A 2.6V, 20mW, 13-bit CODEC with programmable analogue front-end", Electronic Engineering, 33-36, May 1995

/5/ G.C. Duque, R. Perez, J.M. Valdevere, F. Maloberti, "Fully differential basic building block based on fully differential difference amplifier with unity gain difference feedback", IEEE Trans. on CAS -I, Vol.42, 190-192, March 1995

/6/ H. Banba, H. Shiga, A. Umezava, T. Miyaba, T. Tanzawa, "A CMOS band-gap reference circuit with ssub-1-v operation", IEEE JSSC, 34(5), 670- 226, May 1999

/7/ J.C. Candy, G.C. Themes, "Oversampling methods for A/D and D/A conversion in oversampling delta-sigma converters", IEEE Press, 1991

/8/ R. Gregorian, G.C. Temes, "Analog MOS integrated circuits for signal processing", John Wiley and Sons, 1986

/9/ D.B. Ribner, M.A. Copeland, "Design techniques for cascode CMOS op-amp with improved PSRR and common mode input range", IEEE JSSC, 3, 919-925, Dec. 1984

/10/ B.R. Stanisic, N.K. Verghese, R.A. Rutenbar, L.R. Carley, D.J. Allstot, "Addressing substrate coupling in mixed-mode IC's: simulation and power distribution synthesis", IEEE JSSC, 3, 226-238, March 1994

/11/ Gray K. Yeap, "Practical low power digital VLSI design", Kluwer Academic Publishers, 1998

Dr. Drago Strle
Fakulteta za elektrotehniko in računalništvo
Tržaška 25,
1000 Ljubljana, Slovenia

Prispelo (Arrived): 10.8.99 *Sprejeto (Accepted): 15.9.99*

UPORABA MODIFICIRANE OBLIKE PORAZDELJENE ARITMETIKE ZA OSNOVNO IN KASKADNO IZVEDBO DIGITALNIH SIT

Rudolf Babič, Bojan Jarc
Univerza v Mariboru, Fakulteta za elektrotehniko računalništvo in informatiko, Maribor, Slovenija

Ključne besede: signali digitalni, DSP obdelava signalov digitalna, FIR filtri digitalni s trajanjem omejenim odziva impulznega, DA aritmetika porazdeljena, aritmetika porazdeljena modificirana, izvedbe praktične, izvedbe kaskadne

Povzetek: V prispevku predstavljamo modificirano obliko porazdeljene aritmetike za izvedbo nerekurzivnih digitalnih sit. Modificirana oblika porazdeljene aritmetike temelji na unipolarni predstavitvi v osnovi bipolarnega vhodnega signala. Omogoča zmanjšanje aparaturne kompleksnosti digitalnega sita in zaradi ugodnejšega normiranja delnih vsot koeficientov tudi povečanje dinamičnega območja izhodnega signala. Z dodatno uporabo nasprotno simetričnega zapisa delnih vsot koeficientov smo uspeli zmanjšati potrebno pomnilniško strukturo. Dosegli smo prepolovitev števila pomnilniških lokacij potrebnih za shranjevanje delnih vsot koeficientov. Modificirana oblika porazdeljene aritmetike z nasprotno simetričnim zapisom delnih vsot koeficientov je uporabna tako v osnovni kot v kaskadni realizacijski strukturi. Tudi v kaskadni realizacijski strukturi omogoča povečanje dinamičnega območja izhodnega signala in dodatno zmanjšanje števila potrebnih pomnilniških lokacij. Z rezultati simulacij smo potrdili delovanje modificirane porazdeljene aritmetike in poiskali poteke slabljenja in razmerja signal šum v odvisnosti od kvantizacije vhodnega signala v osnovni in kaskadni izvedbi.

The Modified Distributed Arithmetic Structure for the Basic and the Cascade Digital Filters Realization

Keywords: digital signals, DSP, Digital Signal Processing, FIR digital filters, Finite-Impulse Response digital filters, DA, Distributed Arithmetic, modified distributed arithmetic, hardware realizations, cascade realizations

Abstract: In this article the modified distributed arithmetic structure for the FIR digital filter realization is presented. The modified distributed arithmetic structure is based upon an unipolar presentation of the bipolar input signal. It allows the hardware complexity reduction and due to better normalization of sums of products, the enlargement of dynamic range of the output signal was achieved. With additional use of the anti symmetrical presentation of the sums of products the required memory was reduced. The memory for saving the pre-calculated sums of products was halved. The FIR filter realization in the modified distributed arithmetic structure with the anti symmetrical presentation of sum of products is shown on the figure 1.

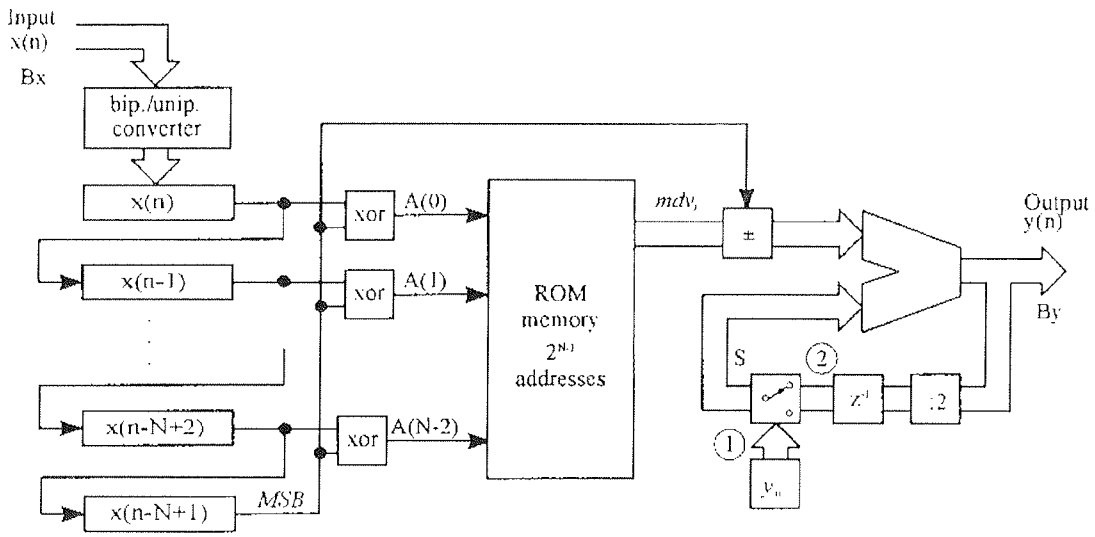


Figure 1: The FIR filter with modified distributed arithmetic structure and a halved number of the memory locations.

The proposed structure can be used for the basic and cascade realization. Also in the cascade realization a further memory reduction and the enlargement of dynamic range of the output signal was achieved. With the simulation the expected operation of the modified distributed arithmetic in the basic and cascade structure was confirmed. Our results shows the attenuation and signal to noise responses of the basic and cascade structures versus the quantization step of the input signal and of the inner arithmetic and logic unit. The number of bits of the input signal varies from B_x=8 to B_x=18 while the number of bits of the sums of products varies from B_{dv}=8 to B_{dv}=26. The enlargement of the dynamic range of the proposed structure results with 3 to 6dB better attenuation of the modified arithmetic structure.

1. Uvod

Porazdeljena aritmetika (PA) predstavlja izvedbo prenosne funkcije digitalnega sita H(z) z operacijo seštevanja in odštevanja vnaprej izračunanih vseh možnih delnih vsot koeficientov shranjenih v pomnilniku tipa EPROM ali ROM brez uporabe množilnikov. Velikost potrebnega pomnilnika raste eksponentno s številom koeficientov impulznega odziva in je določen z 2^N. Pri sitih z N >30 koeficienti dosega že 10^9 naslovov. Zato so prisotna prizadevanja za zmanjšanje naslovnega vektorja. Eden izmed znanih načinov zmanjšanja potrebnega števila pomnilniških lokacij je uporaba nasprotno simetričnih delnih vsot koeficientov /1/. Nasprotno simetrične delne vsote koeficientov lahko s pridom uporabimo v modificirani obliki PA. S tem zmanjšamo aparaturno kompleksnost ter povečamo dinamično območje izhodnega signala. Tako nasprotno simetrični zapis delnih vsot koeficientov kot modificirana PA sta uporabni v kaskadni izvedbi digitalnih sit, kjer dosežemo dodatno zmanjšanje števila pomnilniških lokacij.

2. Klasična oblika porazdeljene aritmetike

PA je bitno-serijski postopek izračuna skalarnega produkta dveh vektorjev. Za nas zanimiv skalarni produkt je konvolucijska vsota nerekurzivnega sita:

$$y(n) = \sum_{k=0}^{N-1} h(k)x(n-k) \qquad (1)$$

V zgornji enačbi h(k) predstavlja k-ti koeficient impulznega odziva, x(n-k) (n-k)-to vrednost vhodnega signala in y(n) n-to vrednost izhodnega signala. N predstavlja število koeficientov impulznega odziva nerekurzivnega digitalnega sita stopnje N-1. Vhodni signal x je običajno omejen v polodprtem intervalu [-1, 1) in ga v binarni obliki predstavimo z dvojiškim komplementom:

$$x(n) = -b_0(n) + \sum_{i=1}^{Bx-1} b_i(n)2^{-i} \qquad (2)$$

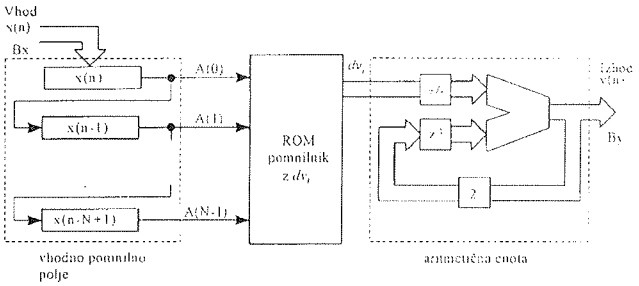
V enačbi (2) predstavlja B_X število bitov za zapis n-te vrednosti vhodnega signala x(n), $b_i(n)$ so binarne spremenljivke vhodnega signala x(n), ki zavzamejo vrednosti 0 ali 1. Pri tem $b_0(n)$ predstavlja predznak in $b_{Bx-1}(n)$ najmanj uteženi bit z utežno vrednostjo $2^{-(Bx-1)}$. Konvolucijsko enačbo (1) lahko prevedemo v obliko

$$y(n) = -dv_0(n) + \sum_{i=1}^{B_x-1} dv_i(n)2^{-i} \qquad (3)$$

v kateri so z $dv_i(n)$ označene delne vsote koeficientov, ki predstavljajo vmesni korak pri računanju y. Izračun delnih vsot koeficientov prikazuje enačba (4).

$$dv_i(n) = \sum_{k=0}^{N-1} h(k)b_i(n-k) \qquad (4)$$

Enačba (3) predstavlja osnovo PA. Za izračun trenutne izhodne vrednosti potrebujemo le operacijo seštevanja in množenja z 2^{-i}. Množenje z 2^{-i} predstavlja pomik vsebine akumulatorja za i bitov na desno. Odštevanje zadnje delne vsote koeficientov dv_0 je izvedeno s prištevanjem dvojiškega komplementa delne vsote koeficientov dv_0. Delne vsote koeficientov $dv_i(n)$ izračunamo vnaprej in jih zapišemo v pomnilnik tipa ROM ali EPROM. Pri tem upoštevamo vse možne nabore binarnih spremenljivk $b_i(n)$. Pomnilnik mora imeti 2N pomnilniških lokacij dolžine B_{dv} bitov, pri čemer B_{dv} predstavlja število bitov za zapis delnih vsot koeficientov. Izvedbo digitalnega sita v PA prikazuje slika 2.



Slika 2: Izvedba FIR digitalnega sita v PA.

3. Modificirana oblika porazdeljene aritmetike

Princip modificirane PA je bil predstavljen v /2/, vendar pri izračunu modificiranih delnih vsot koeficientov ni bila v celoti kompenzirana premaknitev nivoja vhodnega signala. Modificirana PA temelji na unipolarni predstavitvi sicer bipolarnega vhodnega signala zapisanega v dvojiškem komplementu. Unipolarno predstavitev vhodnega signala enostavno dosežemo z negiranjem bita za predznak. S takšnim zapisom vhodnega signala se izognemo odštevanju zadnje delne vsote dv_0 in tako zmanjšamo kompleksnost vezja. Vhodni signal x(n) predstavimo v binarni obliki z:

$$x(n) = \sum_{i=0}^{B_x-1} b_i(n)2^{-i} \qquad (5)$$

Omejen je v polodprtem intervalu [0, 2). Odziv sistema na unipolarni vhodni signal opišemo z enačbo:

$$y'(n) = \sum_{i=0}^{B_x-1} \sum_{k=0}^{N-1} h(k) b_i(n-k) 2^{-i} \qquad (6)$$

$$= \sum_{i=0}^{B_x-1} dv_i(n) 2^{-i}$$

Izhodni signal je unipolaren, premaknjen iz izhodišča za konstantno vrednost K_1. To konstanto dobimo z zapisom konvolucijske vsote za y´(n).

$$y'(n) = \sum_{k=0}^{N-1} h(k)[x(n-k)+1]$$

$$= \sum_{k=0}^{N-1} h(k)x(n-k) + \sum_{k=0}^{N-1} h(k) \qquad (7)$$

$$= y(n) + K_1$$

Pri tem je velikost konstante K_1 odvisna od koeficientov impulznega odziva.

$$K_1 = \sum_{k=0}^{N-1} h(k) \qquad (8)$$

Dodano konstantno vrednost v izhodnem signalu lahko odpravimo z modificiranim zapisom delnih vsot koeficientov.

$$mdv_i = dv_i - \frac{1}{2} \sum_{k=0}^{N-1} h(k) \left[1 + \frac{2^{-Bx}}{1-2^{-Bx}} \right] \qquad (9)$$

To lahko pokažemo z izračunom izhodnega signala z modificiranimi delnimi vsotami koeficientov.

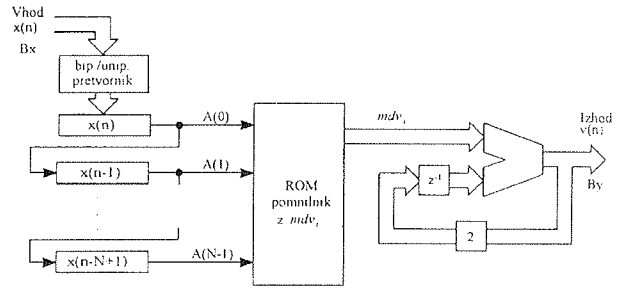
Skupni vsoti delnih vsot koeficientov dvi se odšteva vsota koeficientov impulznega odziva sita in izniči premaknitev, ki nastane zaradi unipolarnega zapisa vhodnega signala.

Na osnovi enačb (9) in (10) lahko narišemo izvedbo digitalnega sita v modificirani PA.

$$y = \sum_{i=0}^{Bx-1} mdv_i 2^{-i}$$

$$= dv_0 + \frac{1}{2}dv_1 + \frac{1}{4}dv_2 + \ldots + \frac{1}{2^{Bx-1}} dv_{Bx-1} - \frac{1}{2} \sum_{k=0}^{N-1} h(k) \left(1 + \frac{2^{-Bx}}{1-2^{-Bx}} \right) \left(1 + \frac{1}{2} + \ldots + \frac{1}{2^{Bx-1}} \right) \qquad (10)$$

$$= dv_0 + \frac{1}{2}dv_1 + \frac{1}{4}dv_2 + \ldots + \frac{1}{2^{Bx-1}} dv_{Bx-1} - \sum_{k=0}^{N-1} h(k)$$



Slika 3: Izvedba digitalnega sita v modificirani PA.

3.1 Prepolovitev števila potrebnih pomnilniških lokacij

Pri izvedbi FIR sita z N koeficienti impulznega odziva v PA potrebujemo 2^N pomnilniških lokacij za zapis delnih vsot koeficientov. Z nasprotno simetričnim zapisom delnih vsot koeficientov in izvedbo sita v modificirani PA bomo število potrebnih pomnilniških lokacij prepolovili.

Zapišimo modificirane delne vsote koeficientov z

$$mdv_i = dv_i - \frac{1}{2} \sum_{k=0}^{N-1} h(k) \qquad (11)$$

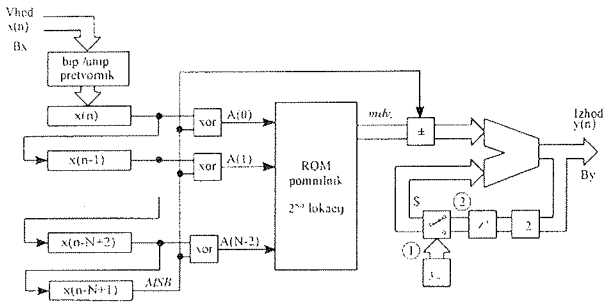
Zaradi nasprotno simetričnega zapisa se pojavi konstantno odstopanje amplitude izhodnega signala z vrednostjo K_2, ki znaša

$$K_2 = 2^{-Bx} \sum_{k=0}^{N-1} h(k) \qquad (12)$$

To odstopanje najlažje odpravimo tako, da prvi delni vsoti koeficientov mdv_{Bx-1}, naslovljeni z vektorjem najniže uteženih bitov vhodnega pomnilnega polja prištejemo negativno polovico vsote koeficientov impulznega odziva. To vrednost označimo z y_0:

$$y_0 = -\frac{1}{2} \sum_{k=0}^{N-1} h(k) \qquad (13)$$

Praktično izvedemo korekcijo prve delne vsote z dodatnim registrom in stikalom v aritmetični enoti kot to prikazuje slika 4.



Slika 4: Izvedba digitalnega sita v modificirani PA in prepolovljenim številom pomnilniških lokacij.

Prvi modificirani delni vsoti izračunani po enačbi (11) se prišteje konstanta y_0 shranjena v dodatnem registru. Takrat je stikalo S v položaju 1. Za preostale modificirane delne vsote koeficientov je stikalo S v položaju 2 in se naslovljeni modificirani delni vsoti koeficientov prišteva z dva deljeni trenutni rezultat iz izhoda aritmetične enote.

V ROM pomnilniku je shranjena le prva polovica nasprotno simetričnih modificiranih delnih vsot izračunanih po enačbi (11). Drugo polovico generiramo iz obstoječih. Z dodanimi ekskluzivnimi ali vrati (XOR) negiramo bite naslovnega vektorja. Predznak tako naslovljeni delni vsoti koeficientov pa zamenjamo z vezjem za generiranje predznaka.

Z omenjenim postopkom smo zmanjšali število pomnilniških lokacij na polovico iz 2^N na 2^{N-1}.

3.2 Povečanje dinamičnega območja izhodnega signala

Za razliko od klasičnih delnih vsot koeficientov pri nizkoprepustnih sitih, ki so izrazito ali pozitivne ali negativne so modificirane delne vsote koeficientov izračunane po enačbi (11) simetrične z nasprotnimi predznaki. Ugotovili bomo, da je v procesu normiranja koeficientov impulznega odziva nasprotno simetrični zapis delnih vsot koeficientov ugodnejši saj dosežemo pri nizkoprepustnih sitih zapis večjih vrednosti v pomnilnik. To pa omogoča povečanje dinamičnega območja izhodnega signala.

Delne vsote koeficientov normiramo iz dveh razlogov:

- da preprečimo prelivanje vrednosti izhodnega signala preko dovoljenega območja [-1, 1) in
- zaradi omejenega območja za zapis delnih vsot koeficientov [-1, 1).

Izhodni signal, vhodni signal in delne vsote koeficientov impulznega odziva digitalnega sita so zapisani v dvojiškem komplementu in omejeni v območju [-1, 1). Da preprečimo prekoračitev območja izhodnega signala, normiramo koeficiente impulznega odziva {h(n)}, n = 0, 1, ..., N-1 glede na maksimalno absolutno vrednost frekvenčnega odziva kot prikazuje enačba:

$$h_{norm}(n) = \frac{h(n)(1-Q_y)}{\max\left|H(e^{j\omega})\right|}, n = 0,1,\ldots,N-1 \qquad (14)$$

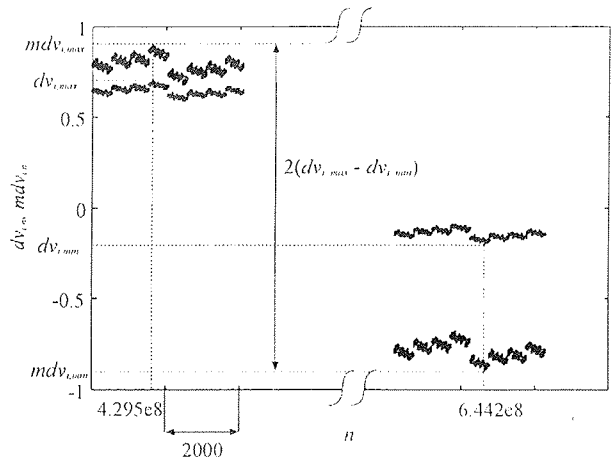
Pri tem predstavlja Q_y stopnjo kvantizacije izhodnega signala [1].

Iz normiranih koeficientov izračunamo maksimalno absolutno vrednost delnih vsot koeficientov. V kolikor ta preseže vrednost 1-Q_{dv}, [2] normiramo (delimo) koeficiente impulznega odziva s faktorjem 2^i. Pri tem je i minimalno naravno število, ki zadosti pogoju, da maksimalna absolutna vrednost delnih vsot koeficientov ne preseže vrednosti 1-Q_{dv}.

Z deljenjem delnih vsot koeficientov s faktorjem 2^i smo za enak faktor zmanjšali tudi amplitudo izhodnega signala, s tem pa tudi zmanjšali dinamično območje. Zato z enakim faktorjem 2^i množimo signal, ki ga vodimo iz aritmetične enote na izhod. Množenje z 2^i je v digitalni tehniki enostavno izvedljivo. Tako povečamo dinamično območje izhodnega signala z zamikom podatkovnih linij aritmetične enote, ki jih vodimo na izhod, za i bitov v levo. Povečanje dinamičnega območja izhodnega signala je aktualno vselej, kadar ima aritmetična enota vsaj i bitov več, kot jih je uporabljenih za zapis izhodnega signala.

Število bitov zamika i je odvisno od lastnosti digitalnega sita oz. od koeficientov impulznega odziva. Slika 5 prikazuje nekaj vrednosti klasičnih (dv_i) in modificiranih nasprotno simetričnih delnih vsot koeficientov (mdv_i) nizkoprepustnega sita stopnje N-1 = 29 z F_p = 0.2 in F_z = 0.3. Za ilustracijo sta prikazani tudi maksimalni in minimalni mejni vrednosti.

Iz slike vidimo, da je razlika med maksimalno in minimalno modificirano delno vsoto koeficientov dvakrat večja od razlike med klasičnima delnima vsotama koe-



Slika 5: Nekaj vrednosti klasičnih in modificiranih delnih vsot koeficientov.

[1] $Q_y = 2^{-(By-1)}$. B_y je število bitov za zapis izhodnega signala.
[2] Q_{dv} predstavlja stopnjo kvantizacije delnih vsot koeficientov.

ficientov. S tem je dinamično območje izhodnega signala sita v modificirani PA dva krat večje kot pri situ v klasični PA. Za sito v modificirani PA ni potrebna korekcija amplitude izhodnega signala.

4. Kaskadna oblika izvedbe digitalnega sita v modificirani PA

Kaskadna oblika izvedbe digitalnega FIR sita v klasični PA predstavlja učinkovit način zmanjševanja števila potrebnih pomnilniških lokacij za shranjevanje delnih vsot koeficientov. Kaskade so lahko izvedene z osnovnimi strukturami prve, druge ali četrte stopnje a zaradi velikega števila kaskad in majhnega ojačenja v prepustnem pasu niso primerne za aparaturno izvedbo. Ta slabost je odpravljena s kaskadnimi strukturami višjih stopenj. Dobimo jih z združevanjem osnovnih struktur /3/.

Modificirano PA lahko uporabimo tudi pri kaskadni realizacijski obliki FIR sit. Predpostavimo, da smo FIR sito stopnje $N-1 = N_1 + N_2 + \ldots + N_M - M$ razbili na M kaskad višjih stopenj s koeficienti impulznih odzivov:

$$\begin{aligned} &\{h_1(n)\}, \quad n = 0,1,\ldots,N_1, \\ &\{h_2(n)\}, \quad n = 0,1,\ldots,N_2, \\ &\qquad \vdots \\ &\{h_M(n)\}, \quad n = 0,1,\ldots,N_M, \end{aligned} \tag{15}$$

Bipolarne vhodne signale kaskad $\{x_m(n)\}, m = 1, 2, \ldots, M$ pretvorimo v unipolarne [3]. Modificirane delne vsote koeficientov posamezne kaskade zapišemo z:

$$mdv_{i,m}(n) = dv_{i,m}(n) - \frac{1}{2}\sum_{k=0}^{N_m-1} h_m(k)$$

$$dv_{i,m}(n) = \sum_{k=0}^{N_m-1} h_m(k) b_{i,m}(n-k) \tag{16}$$

Pri tem smo z $mdv_{i,m}$ označili nasprotno simetrične modificirane delne vsote koeficientov in z $dv_{i,m}$ delne vsote koeficientov kaskade m.

Konstantno odstopanje amplitude izhodnega signala kaskade m odpravimo s prištevanjem konstantnih vrednosti $y_{0,m}$ prvim delnim vsotam koeficientov $mdv_{Bx-1,m}$. Konstanto $y_{0,m}$ izračunamo vnaprej po enačbi (17) in pomnimo v registru z začetnim pogojem kaskade m:

$$y_{0,m} = -\frac{1}{2}\sum_{k=0}^{N_m-1} h_m(k) \tag{17}$$

Zaradi nasprotno simetričnega zapisa delnih vsot koeficientov lahko prepolovimo število pomnilniških lokacij kaskad kot smo to opisali v poglavju 3 in kot to prikazuje slika 4. S tem dodatno zmanjšamo število pomnilniških lokacij posamezne kaskadne strukture na polovično vrednost. Skupni število naslovov se v kaskadni izvedbi zmanjša od 2^N na $2^{N_1-1} + 2^{N_2-1} + \ldots + 2^{N_M-1}$, pri čemer je $N_1 + N_2 + \ldots + N_M - M = N-1$.

V kaskadah, ki imajo značaj nizkoprepustnega sita, ko so klasične delne vsote koeficientov izrazito pozitivne ali negativne, dosežemo z nasprotno simetričnim zapisom modificiranih delnih vsot koeficientov izrazito povečanje dinamičnega območja izhodnega signala. Hkrati pa večje vrednosti zapisanih delnih vsot v pomnilnikih posameznih kaskad ugodno vplivajo na razmerje signal šum (SNR) celotnega vezja.

5. Rezultati

Z matematičnim orodjem Matlab smo v okolju Simulink zgradili /4, 5/ simulacijsko okolje. S pomočjo rezultatov simulacij smo opravili primerjalno analizo sita v klasični in modificirani obliki PA. Za sito v modificirani PA smo uporabili postopek prepolovitve pomnilniških lokacij z nasprotno simetričnim zapisom delnih vsot koeficientov. V simulacijskih strukturah digitalnih sit smo zajeli vplive kvantizacije vhodnega signala, delnih vsot koeficientov, aritmetične enote in izhodnega signala. Opazovali smo časovne odzive struktur na belošumni vhodni signal. Iz odstopanj med kvantiziranimi in referenčnimi odzivi smo določili šum izhodnega signala ter izračunali razmerje med močjo izhodnega signala in izhodnega šuma (SNR). Nad časovnimi odzivi smo opravili hitro Fourierjevo transformacijo in določili osnovne frekvenčne parametre digitalnega sita.

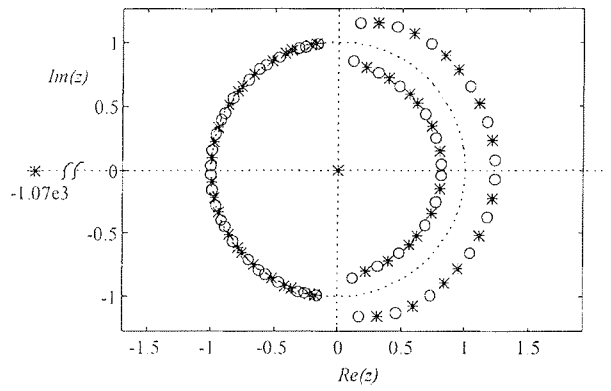
Za primerjalno analizo smo izbrali optimalno nizkoprepustno sito stopnje $N-1 = 100$, s prepustnim pasom $0 \div 0.225$ Fv in zapornim pasom $0.275 \div 0.5$ Fv. Koeficiente impulznega odziva smo izračunali s funkcijo remez /6/ in normirali na maksimalno amplitudo frekvenčnega odziva vrednosti ena. Vrednosti osnovnih referenčnih frekvenčnih parametrov omenjenega sita so:

- ojačenje v prepustnem pasu PBG = -5.182e-4 dB,
- slabljenje v zapornem pasu SBA = -84.506 dB,
- slabljenje sita A = 84.506 dB.

V primerjalni analizi smo zajeli tudi kaskadno obliko izvedbe. Izračunali smo ničle sita stopnje 100 in jih razmestili v dve kaskadni strukturi. Uporabili smo algoritem izbire optimalnih kaskadnih struktur /7/. Razporeditev ničel za obe kaskadni strukturi s stopnjama $N_1-1 = 50$ in $N_2-1 = 50$, prikazuje slika 6.

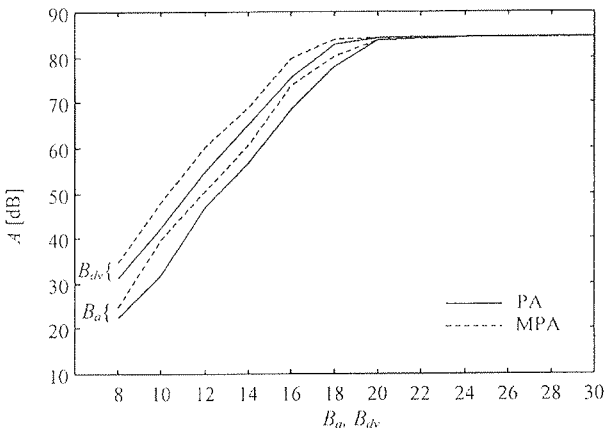
Ločeno smo opazovali vplive kvantizacije vhodnega signala, delnih vsot, aritmetične enote in izhodnega signala na osnovne frekvenčne parametre. Preostale vrednosti smo zapisali z 32 biti.

[3] Negiramo bit predznaka vhodnega signala $x_m(n)$ zapisanega v dvojiškem komplementu.

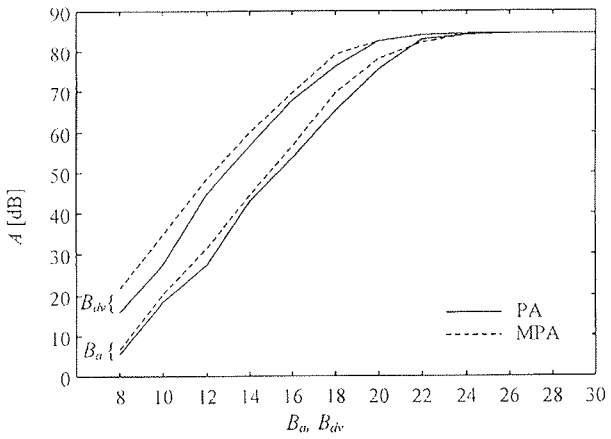


Slika 6: Razporeditev ničel v kaskadni podstrukturi: "o" prva kaskada stopnje N_1-1 = 50, "" druga kaskada stopnje N_2-1 = 50.*

Vpliv omejene dolžine vhodnega ali izhodnega signala na frekvenčne parametre in šumne moči je tako v klasični kot modificirani PA enak. Rezultati so pričakovani in jih nismo prikazali grafično.



a) Osnovna realizacijska struktura

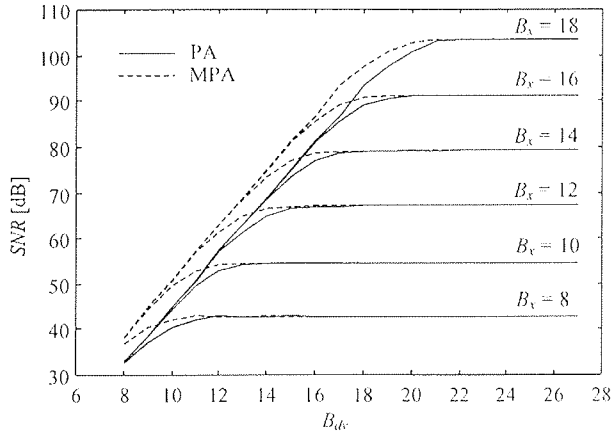


b) Kaskadna realizacijska struktura.

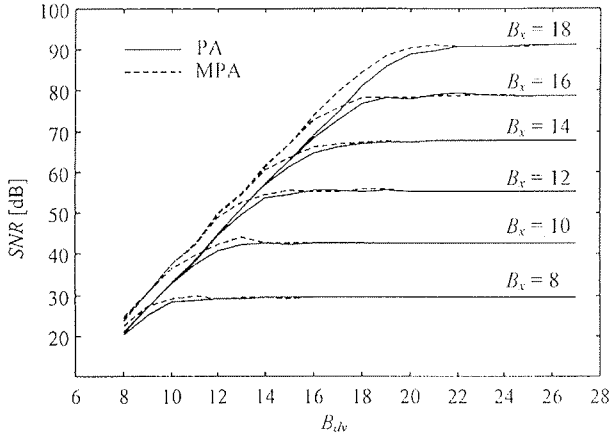
Slika 7: Potek slabljenja A v odvisnosti od števila bitov B_a ali B_{dv} (PA - klasična PA, MPA - modificirana PA).

Zato pa so prisotne razlike pri vplivu kvantizacije delnih vsot koeficientov B_{dv} in številu bitov aritmetične enote B_a na slabljenje A in razmerje signal šum v izhodnem signalu (SNR). Sliki 7a in 7b prikazujeta odvisnost slabljenja A od števila bitov za zapis delnih vsot koeficientov B_{dv} in števila bitov aritmetične enote B_a. V kaskadni obliki smo v posameznih kaskadah izbrali enaki stopnji kvantizacije. Tako v osnovni kot kaskadni realizacijski obliki dosežemo pri enaki stopnji kvantizacije v modificirani PA večje slabljenje A kot pri situ v klasični PA. Referenčno slabljenje A je v obeh izvedbah enako. Večje slabljenje A v modificirani PA smo dosegli z nasprotno simetričnim zapisom delnih vsot koeficientov, ki je omogočil zapis večjih vrednosti delnih vsot koeficientov sita v osnovni realizacijski obliki in v drugi kaskadi kaskadne izvedbene oblike. V prvi kaskadi vrednosti nasprotno simetričnih delnih vsot koeficientov nismo mogli povečati. Zato povečanje slabljenja ni tako izrazito.

Iz rezultatov na slikah 8 a in 8 b lahko določimo potrebno število bitov B_{dv} pri izbrani kvantizaciji vhodnega signala B_x in zahtevanem razmerju SNR. S sitom v modificirani PA dosežemo maksimalno možno razmerje SNR pri manjšem številu bitov B_{dv}, ne glede



a) Osnovna realizacijska struktura



b) Kaskadna realizacijska struktura.

Slika 8: Potek razmerja SNR v odvisnosti od števila bitov Bdv. Bx je parameter (PA - klasična PA, MPA - modificirana PA).

na izbrano število bitov kvantizacije vhodnega signala. Vzrok so večje vrednosti nasprotno simetričnih od klasičnih delnih vsot koeficientov.

6. Zaključek

Z modificirano obliko porazdeljene aritmetike z nasprotno simetričnimi delnimi vsotami koeficientov smo zmanjšali aparaturno kompleksnost digitalnega sita, povečali dinamično območje izhodnega signala in zmanjšali število potrebnih pomnilniških lokacij za zapis vnaprej izračunanih delnih vsot koeficientov. Unipolarni zapis vhodnega signala v mejah [0, 2) je omogočil poenostavitev aritmetične enote, nasprotno simetrični zapis delnih vsot koeficientov pa prepolovitev potrebnega števila pomnilniških lokacij. Pri nizkoprepustnih sitih omogoča nasprotno simetrični zapis povečanje vrednosti modificiranih delnih vsot koeficientov zapisanih v pomnilniku, kar poveča dinamično območje izhodnega signala. Pojav je prisoten tako v osnovni kot v kaskadni realizacijski obliki sit. Pogoj za povečanje dinamičnega območja posamezne kaskade je v prisotnosti izrazito pozitivnih ali negativnih delnih vsot koeficientov, kar je značilno za nizkoprepustna sita oz. za kaskade z nizko prepustnim značajem.

Povečanje dinamičnega območja sit v modificirani PA v osnovni in kaskadni izvedbi ugodno vpliva na povečanje slabljenja sita A in razmerja SNR predvsem pri nižjih stopnjah kvantizacije, ko imamo opravka z omejitvami pri aparaturni kompleksnosti.

7. Literatura

/1/ Stenley A. White, Applications of Distributed Arithmetic to Digital Signal Processing: A Tutorial Review, IEEE ASSP Magazine, pages 4-19, Jul. 1989

/2/ B. Jarc, R. Babič, M. Solar, M. Brumec, "Modificirana oblika porazdeljene aritmetike", Zbornik pete Elektrotehniške in računalniške konference ERK ž96, 19. - 21. september 1996, Portorož, Slovenija, Str. A/113-116.

/3/ R. Babič, M. Solar, B. Stiglic, "High order FIR digital filter realization in distributed arithmetic", V: Proceedings, 6th Mediterranean Electrotechnical Conference, Melecon´91, may 1991.

/4/ J. Hicklin, A. Grace, J. Kinchen, R. Mauceri, "Simulink Dynamic System Simulation Software Users Guide", The Math Works Inc., April 1993.

/5/ J. E. Ciolfi, "Fixed-Point Blockset Users Guide, For Use with SIMULINK ", The Math Works Inc., March 1995.

/6/ T. P. Krauss, L. Shure, J. N. Little, "Signal Processing Toolbox Users Guide: For Use with Matlab", The Math Works Inc., Oct. 1994.

/7/ R. Babič, "Posebnosti porazdeljene aritmetike pri izvedbi nerekurzivnih digitalnih sit", Doktorska disertacija, Univerza v Mariboru, Tehniška fakulteta Maribor, Elektrotehnika, Računalništvo in Informatika, oktober 1991.

doc. dr. Rudolf BABIČ,
mag. Bojan JARC,
oba UNIVERZA V MARIBORU,
FAKULTETA ZA ELEKTROTEHNIKO,
RAČUNALNIŠTVO IN INFORMATIKO
2000 Maribor, Smetanova 17
Slovenija

Prispelo (Arrived): 08.09.99 *Sprejeto (Accepted): 15.09.99*

PREDSTAVLJAMO PODJETJE Z NASLOVNICE
REPRESENT OF THE COMPANY FROM FRONT PAGE

MIKROIKS d.o.o.

MIKROIKS is an engineering company situated in Ljubljana, Slovenia, employing six people, some with long international experience in the field of microelectronics, semiconductors and semiconductor components. The business office is located near the heart of Ljubljana city with excellent communication possibilities.

In the past 10 years of existence, the main activities were in the field of semiconductor technology development, electronic equipment distribution, technical consulting and also lately electronic components distribution.

Besides own production of specific ASIC devices at the beginning of 1997 MIKROIKS entered distribution and sales agent agreement with Murata Elettronica Italy, for distribution of Murata products in Slovenia and Croatia. End of 1998, to Murata passive components MIKROIKS added distribution of active components from STMicroelectronics, one of the largest producers of semiconductors in Europe.

Philosophy of the company has always been to serve the clients in the best way possible. This is why MIKROIKS rather focuses on small number of suppliers with wide range of products and try to introduce and sell their products agressively. STMicroelectronics and Murata huge portfolio of fine semiconductor products, as well as passive components seems ideally fitted to Slovenian market approach and philosophy.

In the field of technological development MIKROIKS cooperated/cooperate with several companies and institutions having bilateral and multilateral research and development projects. Among them are Austria Microsysteme Inc. (A), Semcotec (A), HIPOT (SLO), Belinka (SLO), Delo (SLO), Jožef Stefan Institute (SLO) and Institute for Surface Engineering and Optoelectronics (SLO). The majority of the work was done on development and in several cases production implementation of the following products/processes: plasma surface cleaning of different materials, plasma characterization,ultrafast silicon rectifiers, high voltage rectifiers, special passivation technologies for discrete devices, 1.5μm to 5μm standard and high voltage nwell/double poly/single metal CMOS technologies, mixed high voltage DMOS-bipolar-CMOS technology primarily used to design state of the art integrated circuits to be used in telecommunications.

In the field of equipment distribution MIKROIKS mainly acts as sales agent for different companies like:

- ANATEL from Boulder, USA, which was among the first in the world to start producing instrumentation for measuring TOC (Total Organic Carbon) in clean waters. Their range of fine instruments intended for controlling semiconductor waters is now extended to systems that measure TOC in pharmaceutical, as well as drinking waters.

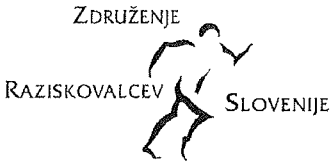
- Pacific Scientific, HIAC/ROYCO division from USA, is a well known company that makes instrumentation used to measure particles in air, gases, water, oils and other solutions. Wherever there is a process that requires a clean media, Hiac Royco has the right instrument to control its purity.

- TECHNICS PLASMA from Muenchen, Germany, is a company that makes industrial microwave plasma systems suitable for surface pretreatment and cleaning of wide range of materials used in microelectronics, high-tech electronics, car and consumer industry.

Founded in 1989 by people who used to work for Iskra Microelectronics division, MIKROIKS in 1999 celebrates its 10th anniversary with optimistic look towards its future development.

MIKROIKS d.o.o.
Stegne 11, 1521 Ljubljana
Tel.+386 (0)61 1512 221
Fax.+386 (0)61 1512 217

PREDSTAVLJAMO ZDRUŽENJE RAZISKOVALCEV SLOVENIJE
WE PRESENT ASSEMBLY OF SLOVENE RESEARCHERS



Spoštovana kolegica, spoštovani kolega!

Vabim Vas, da postanete članica oz. član Združenja raziskovalcev Slovenije: sprejmite njegov statut in podpišite pristopno izjavo, sooblikujte njegov program dela in se vanj aktivno vključujte. Združenje bo izboljšalo Vašo učinkovitost pri reševanju stanovskih problemov ali Vam jo sploh omogočilo. Predvsem pa Vam bo zagotovilo, da se v družbi legitimirate in uveljavite kot raziskovalec oz. razvojnik.

Združenje raziskovalcev Slovenije je prvo stanovsko združenje vseh poklicnih raziskovalcev in razvojnikov Slovenije. člani oz. članice določajo njegove cilje in aktivnosti, da bi vplivali na raziskovalno in razvojno politiko, si zagotovili avtonomen stanovski položaj ter tako dosegali večjo kvaliteto in družbeni pomen raziskovalnega in razvojnega dela.

Združenje raziskovalcev Slovenije je nevladna in nepolitična strokovna stanovska organizacija, ki deluje kot dinamična in aktivna mrežna povezava med posameznicami oz. posamezniki in institucijami. Enakopravno skrbi za vse znanstvene vede, različne vrste raziskovanja in razvojnega dela, tudi izven akademske sfere, ter na različnih in različno geografsko umeščenih raziskovalnih in razvojnih institucijah, ne glede na lastništvo. Spodbuja sinergistično povezovanje in sodelovanje med različnimi disciplinami in institucijami. Sproti evalvira stanje in vlogo raziskovanja in razvoja v družbi.

člani oz. članice Združenja raziskovalcev Slovenije delujejo v odborih za obravnavanje različnih vsebinskih problematik, področno usmerjenih komisijah in drugih delovnih telesih ter v organih Združenja. Povezujejo se s strokovnimi društvi, zvezami in zbornicami ter s sorodnimi tujimi in mednarodnimi organizacijami, z gospodarstvom in drugimi družbenimi podsistemi. Združenje med drugim zagotavlja učinkovito komuniciranje ter vzpostavitev dogovorov in pravil znotraj raziskovalne sfere, evidentiranje in javno predstavitev raziskovalno-razvojnih tem ter dopolnjevanje in izpopolnjevanje znanstveno-raziskovalne in tehnološko-razvojne strategije Slovenije.

Združenje raziskovalcev Slovenije je nova stanovska organizacija in edina te vrste, ki uresničuje manjkajoče funkcije in naloge obstoječih partnerskih oz. komplementarnih organizmov. Katere in kako, je v Vaših rokah! Združite svoje potrebe, zamisli za njihovo zadovoljevanje in ustvarjalno delovanje v skladu z njimi s kolegicami in kolegi, s katerimi Vam bo Združenje omogočilo sooblikovanje intelektualnega in pripadnostnega odnosa. Združenje raziskovalcev Slovenije je prostor za aktivno sodelovanje in intenziviranje vezi med raziskovalci in razvojniki, ki se ob tem tudi osebno vzpostavljajo in krepijo.

Na priloženi disketi se nahajajo dokumenti, ki Vas bodo bolj podrobno seznanili z Združenjem, med njimi sta pristopna izjava in anketa o sooblikovanju programa dela. član oz. članica boste postali tako, da nam pošljete izpolnjeno pristopno izjavo, hkrati pa pričakujemo tudi izpolnjeno anketo, s katero boste sooblikovali program dela in se vanj aktivno vključili. Ker z akcijo pridobivanja novih članic oz. članov ne moremo seči do vsakega zainteresiranega posameznika oz. posameznice, Vas prosimo še, da kopije priložene diskete oz. dokumentov razširite v svojem okolju.

Z zaupanjem v skupno moč prizadevanj vnaprej izražam svoje iskreno pričakovanje in zadovoljstvo, da se boste odločili delovati v Združenju raziskovalcev Slovenije.

Lep pozdrav in na svidenje!

Ljubljana, 25. septembra 1998

dr. Peter Tancig, generalni sekretar

Združenje raziskovalcev Slovenije

- Je nevladna in nepolitična strokovna organizacija prostovoljno vključenih posameznikov, ki se poklicno ukvarjajo z raziskovanjem in razvojem.
- Zastopa avtonomen stanovski položaj raziskovalcev.
- Deluje za doseganje večje kvalitete in družbenega pomena raziskovalnega in razvojnega dela.
- Enakopravno skrbi za vse znanstvene vede, različne vrste raziskovanja in razvojnega dela, tudi izven akademske sfere, ter na različnih in različno geografsko umeščenih raziskovalnih in razvojnih institucij ne glede na lastništvo.
- Spodbuja sinergistično povezovanje in sodelovanje med različnimi disciplinami in institucijami.
- Sproti evalvira stanje in vlogo raziskovanja in razvoja v družbi.
- Uveljavlja akcijske dejavnosti pred institucionalnim bivanjem.
- Zagotavlja infrastrukturne storitve in postavlja pravila notranjega delovanja ter javnost delovanja, pomembne za pospeševanje raziskovalne in razvojne dejavnosti.
- Se financira s članarino in iz drugih virov.

Člani Združenja raziskovalcev Slovenije

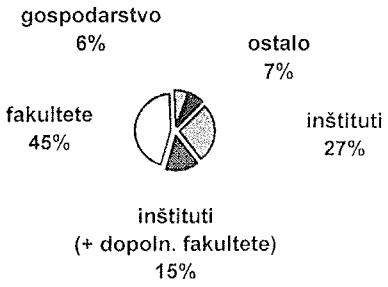
- Usmerjajo program Združenja z določanjem njegovih ciljev in aktivnosti.
- Vplivajo na raziskovalno in razvojno politiko.
- Aktivno delujejo v dinamičnih skupinah za obravnavanje določenih vsebinskih problematik, področno usmerjenih komisijah in delovnih telesih ter drugih organih Združenja.
- Se povezujejo s strokovnimi društvi, zvezami in zbornicami ter s sorodnimi tujimi in mednarodnimi organizacijami, z gospodarstvom in drugimi družbenimi podsistemi.
- Svoje odnose medsebojno intelektualno in pripadnostno oblikujejo, negujejo ob spodbujanju aktivnega sodelovanja in ustvarjalnosti, jih intenzivirajo pri avtonomno sprožanih aktivnostih in ob tem tudi osebno vzpostavljajo in krepijo.
- Lahko postanejo vsi državljani Republike Slovenije, ki se poklicno ukvarjajo z raziskovanjem ali razvojem, potem ko sprejmejo statut Združenja in podpišejo pristopno izjavo.

Nekateri osnovni dokumenti

- pristopna izjava
- statut
- anketa o sooblikovanju programa dela
- predstavitveni oris
- pogosto postavljena vprašanja
- programske usmeritve
- okolje delovanja in načini dela
- od idej do projektov
- organi (januar 1998)
- ustanovni člani (marec 1997)
- iniciativni odbor (december 1996)

Razporeditev članic/-ov po institucijah

(191 članov/-ic - september 1998)



Pogosto postavljena vprašanja

Pogoji za uspešno delovanje Združenja:

- aktivno (so)delovanje članov
- ustrezna logistična in administrativna podpora
- zadovoljevanje interesov članov
- zadostna finančna sredstva za sprejeti program dela

Ali je Združenje potrebno ob obstoječih oblikah (samo)organiziranja raziskovalne sfere?

Da, ker ne gre za konkurenco oz. prekrivanje, ampak za oblikovanje manjkajočih funkcij in nalog. Obstoječim partnerskim oz. komplementarnim organizmom močno Združenje lahko samo koristi:

- **KORIS**: koordinacija direktorjev raziskovalnih institucij, ki se kot skupina ukvarjajo s sistemskim in finančnim položajem svojih ustanov
- **SVIZ**: sindikat, ki pokriva klasične sindikalistične vidike raziskovalne dejavnosti
- **ZIT**: Zveza inženirjev in tehnikov, ne vključuje raziskovalcev, ampak (tudi) razvijalce v podjetjih
- **SATENA**: inženirska akademija, ki podpira in spodbuja razvoj metod tehničnih in naravoslovnih znanosti
- **strokovna društva**: delujejo stanovsko in problemsko na specifičnih vsebinskih področjih.

Združenje raziskovalcev Slovenije je kot univerzalna stanovska organizacija, namenjena in odprta za vse raziskovalce in razvojnike ne glede na njihovo specialnost, edina svoje vrste.

Zakaj nismo ustanovili Raziskovalne zbornice Slovenije?

Na ustanovni skupščini Združenja so bili izraženi skoraj soglasna podpora ustanovitvi Raziskovalne zbornice Slovenije in pričakovanja, da je to naravni naslednji korak pri (samo)organizaciji raziskovalne sfere. Pred ustanovitvijo Zbornice pa je potrebno odgovoriti na številna vprašanja oz. dileme:

- primernost izbrane oblike (Združenje, Zbornica) glede na vizijo in program;
- potrebnost izbrane oblike glede na razmere v okolju;
- obseg in doseg javnih pooblastil;
- obseg in doseg predvidenih dejavnosti;
- obvezno ali neobvezno članstvo in kriteriji za izbor članov;
- doseg članstva: raziskovalci (in tudi razvojniki);
- zakonska (ne)obveznost financiranja predvidenih javnih pooblastil in dejavnosti iz državnega proračuna;
- ureditev v samostojnem zakonu ali v okviru zakona o raziskovalni dejavnosti.

Poleg teh vsebinskih problematik, ki jih bo mogoče dovolj hitro razrešiti znotraj raziskovalne sfere, pa obstaja še niz nedorečenosti sistemskega značaja, do katerih je prišlo zaradi hitrega naraščanja števila zbornic različnih vrst. Tako je npr. problematika obveznega članstva v različnih zbornicah v nekaj primerih privedla do obravnave na Ustavnem sodišču.

Financiranje delovanja Združenja:

Program dela, finančni načrt in organizacijsko-delovna struktura Združenja predstavljajo povezano celoto med seboj soodvisnih sklopov, za uspeh katere je potrebna prisotnost vseh treh. V končni posledici pa Združenje stoji ali pade v odvisnosti od zagotovitve ustreznih sredstev, brez katerih še tako dobrega programa ni mogoče realizirati kljub racionalno zamišljeni izvedbeni organizaciji.

Vseh stroškov za predviden obseg delovanja Združenja ni mogoče kriti iz članske članarine, ki bo vedno pokrivala le manjši del predvidenih odhodkov, zato je potrebno zagotoviti predvsem druge vire financiranja. Po dosedanjih razgovorih je mogoče identificirati naslednje potencialne sofinancerje delovanja Združenja in oceniti časovno faznost njihovega sodelovanja:

faza	sofinancer
I. (l. 1998)	raziskovalni inštituti
	Ministrstvo za znanost in tehnologijo
II. (l. 1999)	fakultete, gospodarstvo, tuji viri
	druga ministrstva

Združenje po svoji delovni in resorski usmeritvi deluje v javnem interesu na področju raziskovalne dejavnosti. S tem je omogočeno, da Ministrstvo za znanost in tehnologijo to dejavnost podpira in sofinancira v okviru svojih proračunskih sredstev.

Odnos do politike (strank, parlamenta, vlade):

- samoumevna nepolitičnost strokovnega Združenja kot celote se ne sme pretvoriti v antipolitičnost, ker je to tudi političnost, predvsem pa je neproduktivna oz. konfliktna
- Združenje naj vključuje tako politično neopredeljene raziskovalce kot raziskovalce različnih političnih opredelitev
- politični poudarki in interesi pa ne smejo vplivati na strokovno delo in odločitve Združenja.

Razmisleki o vsebini avtonomije raziskovalnega dela in avtonomnosti posameznih institucij:

- raziskovalci naj bodo v bodoče del družbe in ne izolirani od nje in njenih problemov; nizka izobrazbena raven v Sloveniji, stopnja strukturne in s tem trajne nezaposlenosti, majhno število najvišje kvalificiranih strokovnjakov v industriji, vse to zahteva našo streznitev
- avtonomija in avtonomnost sta seveda osnovni predpostavki kvalitetnega raziskovalnega dela, dvigne naj se pa zavedanje o umeščenosti raziskovalne sfere v širšo družbo in življenju z njo oz. zanjo
- razvojna in raziskovalna politika države naj vsebujeta mehanizme pozitivne motivacije in spodbud za tesnejše neogrožujoče povezave med "proizvajalci" in "uporabniki" raziskovalnih spoznanj
- te povezave morajo sloneti na sodobnih spoznanjih, po katerih dinamične in aktivne mrežne povezave med posamezniki in institucijami zamenjujejo statično shemo "push - pull".

PROGRAMSKE USMERITVE

ZNANOST IN DRUŽBA - STANJE V RAZVITIH DEŽELAH IN V SLOVENIJI

- Družbe na pragu 21. stoletja so že ločene na tiste, ki imajo znanje (in ga uporabljajo za svoj razvoj), in tiste, ki ga nimajo.
- Tudi znotraj razvitih družb se pojavlja podobna razdelitev (20 % delovnega prebivalstva z ustreznimi znanji in zato ugodnejšim položajem v družbi, 80 % ostalih - posledično deprivilegiranih).
- Znanost in znanje (proizvajanje lastnega, prevzemanje tujega, prenos v uporabo) postajata vedno bolj pomembna in dejavna v vseh podsistemih družbe - ne samo v klasični proizvodni paradigmi, kot je npr. industrija (tehnologija).
- Za sodobne razvite družbe je značilna čedalje tesnejša povezava med "trdimi" in "mehkimi" vedami; človek kot individualno in socialno bitje se znova vrača v središče pozornosti - pa čeprav še vedno prevladujoče s stališča dobičkanosnosti.

- Posamezen raziskovalec v Sloveniji živi in dela preko svojega projekta, v svoji instituciji in v mreži osebnih povezav, nima pa možnosti stanovskega ("cehovskega") organizacijskega in vsebinskega delovanja.
- Med posameznimi vedami, institucijami, strokovnimi društvi in zvezami obstajajo težko prehodne razmejitve, ki zelo otežkočajo povezovanje aktivnosti in sinergistično prepletanje pristopov, kar je sicer v svetu značilno za sodobno znanost.
- Raziskovalna sfera v Sloveniji ima določene značilnosti - predvsem zaradi svoje majhnosti:
  - skupine in posamezniki se praviloma angažirajo na (skoraj) vseh vidikih raziskovalne dejavnosti (poučevanje oz. predajanje znanja, temeljno, aplikativno in razvojno raziskovanje, razvojno in svetovalno delo za neposredno uporabo);
  - nekatere raziskovalne skupine so edine, ki se ukvarjajo z določeno problematiko pri nas;
  - rojstvo novih raziskovalnih skupin oz. odpiranje novih vsebin je zelo težko;
  - raziskovalne skupine so praviloma zelo krhke; potem ko so okrnjene, zmanjšane ali celo odpravljene, jih je skoraj nemogoče (relativno) hitro obnoviti.
- V Sloveniji še obstaja in bi bilo - ob ustreznih pristopih - na razpolago dosti več znanja, kot se ga dejansko uporablja na različnih področjih družbenega razvoja, vključno z gospodarstvom (!).
- Proračunska sredstva za raziskovalno dejavnost so se zmanjšala za 40 % od 1993 do 1996; že samo to dejstvo in njegova posledica - raziskovalna dejavnost tik pred zlomom obstoja - predpostavljata določene vzroke in postavljata številna resna vprašanja:
  - razumevanje oz. zavedanje širše družbe o pomenu znanosti za razvoj;
  - dejanski prispevek znanosti k hitrejšemu in bolj usklajenemu razvoju družbe;
  - neizdelana vizija in strategija razvoja Slovenije, ki bi vključevala znanost in znanje kot bistvena razvojna dejavnika sodobnih razvitih družb;
  - raziskovalci, skupine in institucije si posamič prizadevajo za izboljšanje svojega položaja, ne delujejo pa kot pripadniki določenega stanu oz. podsistema;
  - številne (raz)delitve raziskovalne sfere, ki očitno onemogočajo skupen nastop, pa čeprav tudi v lastnem, preživetvenem interesu;
  - odsotnost stanovske samoorganizacije raziskovalne sfere.

POSLANSTVO ZDRUŽENJA RAZISKOVALCEV SLOVENIJE

- Združenje je institucija civilne družbe (nevladna, nepolitična in nestrankarska).
- Združenje je avtonomna "cehovska" strokovna organizacija prostovoljno vključenih poklicnih raziskovalcev in razvojnikov.
- V razmerju do politike (parlamenta, vlade, strank) je Združenje neodvisna organizacija, ki zastopa avtonomen, stanovski položaj znanosti.
- Združenje sodeluje pri oblikovanju aktivne nacionalne raziskovalno-razvojne politike.
- Združenje skrbi za enakopravno zastopanje različnih dimenzij znanosti in raziskovalnega dela:
  - po vedah (naravoslovno-matematične, tehniške, medicinske, biotehniške, družbene, humanistične);
  - glede na različne vrste raziskovanja (temeljno, aplikativno, razvojno);
  - upoštevajoč tudi razvojno delo izven akademske sfere - v industriji in drugod;
  - na različnih institucijah (univerze, inštituti, raziskovalno-razvojni oddelki v industriji in drugod);
  - po geografski umestitvi (mesta in regije);
  - ne glede na lastništvo (državno, privatno, mešano);
  - ne glede na politično usmerjenost in pripadnost raziskovalcev.
- Združenje odpira in organizira prostor za javni racionalni diskurz o številnih razvojnih temah, s katerimi se sooča Slovenija v času hitre pretvorbe politično-ekonomskega sistema in zgodovinskih sprememb v svetu.

NAMENI ZDRUŽENJA RAZISKOVALCEV SLOVENIJE

- Doseči avtonomijo, ugled, kvaliteto in družbeni pomen raziskovalnega dela.
- Zagotoviti ustrezno mesto znanosti v družbi - tako širšo družbeno skrb za obstoj znanosti kot prispevek znanosti k razvoju družbe.
- Doseči in vzdrževati primerne pogoje za raziskovalno delo.

CILJI ZDRUŽENJA RAZISKOVALCEV SLOVENIJE

Združenje naj postane uspešna, učinkovita in vplivna predstavnica stanovskih interesov poklicne raziskovalne sfere. Zato mora opravljati ustrezne aktivnosti in dosegati določene učinke:

- omogočiti učinkovito komuniciranje znotraj raziskovalne sfere, zato:
  - prizadevati si za čimbolj številno članstvo (pridobivanje, obveščanje, spodbujanje k aktivnemu sodelovanju),
  - animirati člane za razpravo o različnih vprašanjih,
  - spodbujati člane k različnim aktivnostim;
- postaviti pravila notranjega delovanja, med katerimi tudi:
  - vzpostaviti in voditi register članov,

  - skrbeti za izpopolnjevanje, usposabljanje in izobraževanje članov,
  - oblikovati kodeks poklicne etike raziskovalcev in razvojnikov;

- izboljševati položaj in pomen raziskovalne dejavnosti v družbi, zato:
  - skrbeti za družbene ugled, čast in avtonomen položaj svojih članov,
  - ščititi interese raziskovalne dejavnosti in znanja nasploh,
  - skrbeti za stalno evalvacijo stanja in vloge raziskovanja in razvoja v družbi;

- evidentirati in javno odpirati raziskovalno-razvojne teme s posebnim poudarkom na združevanju, prepletanju in sinergiji različnih disciplin (pristopov, vidikov);
- spodbujati multi-, inter- ter krosdisciplinarne povezave na širših projektih in programih ter sodelovanje med različnimi institucijami;
- omogočiti bolj učinkovito umeščenost in povezanost raziskovalne sfere z družbo kot celoto in njenimi podsistemi (segmenti, sektorji, delnimi podsistemi), zato je nujno:
  - spodbujati povezovanje raziskovalne sfere z gospodarstvom in drugimi družbenimi podsistemi,
  - vzpostavljati in vzdrževati aktivne odnose z drugimi družbenimi podsistemi, različnimi javnostmi in politiko (parlamentom, vlado, strankami);

- oblikovati predloge za dopolnjevanje in izpopolnjevanje "bele/modre" knjige "Znanstveno-raziskovalna in tehnološko-razvojna strategija Slovenije".

NAČINI DELOVANJA ZDRUŽENJA RAZISKOVALCEV SLOVENIJE

Osnovna filozofija delovanja je upoštevanje interesa in koristi vseh udeležencev partnerskega odnosa. Zato naj Združenje koristi vsem prostovoljno sodelujočim tako iz raziskovalne sfere (posameznikom, institucijam, strokovnim društvom, ...) kot iz drugih družbenih podsistemov, t.i. "(u)porabnikom" znanja, ter družbi kot celoti. Pomembni elementi takega pristopa so:

- korektna razmejitev vsebin in aktivnosti Združenja v odnosu do obstoječih institucij in drugih oblik organiziranosti na področju raziskovalne dejavnosti;
- odnosi med in s člani Združenja:
  - so osnovani na izčrpnem dvo- in večsmernem komuniciranju ter obveščanju (funkcionalno usmerjeno glasilo, elektronska pošta, elektronske konference - t.i. "elektronska demokracija"),
  - so odzivni in neposredno demokratični (sprotno aktivno odzivanje na pobude članov),
  - se intelektualno in pripadnostno oblikujejo na javnih nastopih (predavanja, soočenja, okrogle mize, problemske in strateške konference...),
  - se negujejo ob spodbujanju aktivnega sodelovanja in ustvarjalnosti,
  - se intenzivirajo ob pomoči (logistika, vsebinska in organizacijska podpora, skrb za integracijske in sinergistične poudarke) pri avtonomno sprožanih aktivnostih članstva,
  - se osebno vzpostavljajo in krepijo tudi na raznih društvenih srečanjih;

- organiziranost in aktivnosti, ki dosegajo poslanstvo in cilje Združenja:
  - organi in predstavniki Združenja,
  - vsebinsko in področno usmerjeni komisije in odbori,
  - *ad hoc* (dinamične) skupine za obravnavanje določenih vsebinskih problematik,
  - povezave s strokovnimi društvi, zvezami in zbornicami,
  - povezovanje s sorodnimi tujimi in mednarodnimi organizacijami;

- domišljeni ciljno usmerjeni aktivnosti in načrti (lastni) ter predlogi aktivnosti in načrtov (drugim poklicanim in odgovornim);
- javno sporočanje o raziskovalno-razvojnih vsebinah.

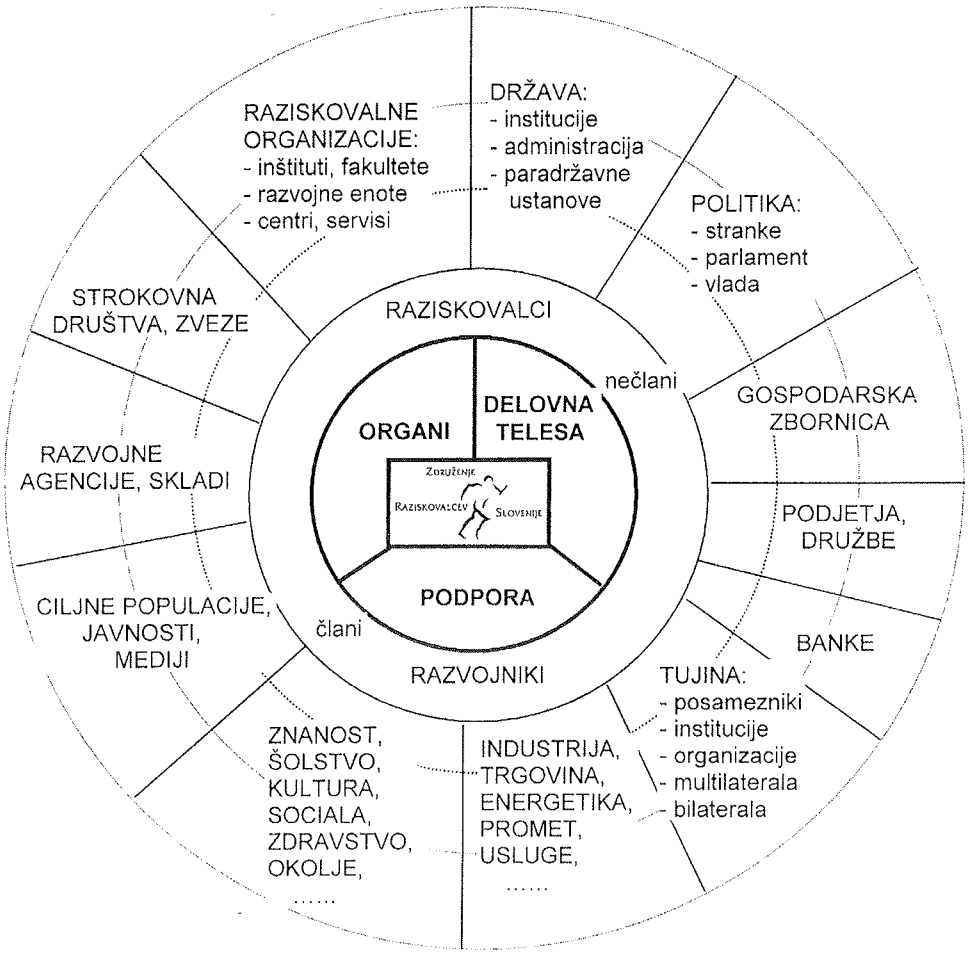
VIZIJA RAZVOJA DRUŽBENE VLOGE ZDRUŽENJA RAZISKOVALCEV SLOVENIJE

Kratkoročna (1 leto)
- Evidentiranje vsebin za javne razprave in izbor njihovih nosilcev.
- Organiziranje javnih soočanj mnenj.
- Odpiranje žgočih družbeno-razvojnih tem.
- Sooblikovanje predlogov raziskovalno-razvojnih tem.

Srednjeročna (2-3 leta)
- Oblikovanje lastne javnosti.
- Vzpostavljanje aktivnega in tvornega dialoga z drugimi javnostmi.

Dolgoročna
- Skupina družbenega vpliva, vzpostavljena preko moči argumentov.
- Pomemben družben faktor za bolj učinkovit in harmoničen razvoj Slovenije.

Okolje delovanja in načini dela



ORGANI	DELOVNA TELESA	PODPORA	ZA VEČJO VLOGO ZNANJA
Skupščina	Odbor	administrativna	dinamične mrežne povezave
Izvršni odbor	Komisije	organizacijska	tele-informacijski sistemi
Generalni sekretar	Programske skupine	logistična	predavanja, srečanja, diskusije
Nadzorni odbor	Projektne skupine	dokumentalistična	okrogle mize, soočanja
Častno razsodišče	Delovne skupine	tele-informacijska	zelene / bele knjige
	Iniciativne skupine	analitična	programske / strateške konference
			akcije, aktivnosti, projekti, programi
			predlogi razvojnih strategij, politik
			borza raziskovalcev
		racionalnosti	katalogi znanj in izkušenj
		sodelovanju	evalvacije programov, projektov
		partnerstvu	javne izjave (pro- / re-aktivne)
		sinergiji	predlogi sprememb (praksa, zakoni)
		komplementarnosti	publikacije, dokumenti

ZDRUŽENJE RAZISKOVALCEV SLOVENIJE

Organi

(izvoljeni ozir. imenovani na skupščini 14. jan. 1998)

Izvršni odbor:

1. dr. Vlasta Jalušič - MIROVNI INŠTITUT; Ljubljana
2. prof.dr. Miha Japelj - KRKA, p.o.; Novo mesto
3. prof.dr. Tomaž Kalin - INSTITUT "JOŽEF STEFAN"; Ljubljana
4. prof.dr. Dušan Nečak - FILOZOFSKA FAKULTETA; Ljubljana
5. dr. Rado Riha - ZRC-SAZU; Ljubljana
6. prof.dr. Lojze Sočan - EKONOMSKA FAKULTETA; Ljubljana - (**podpredsednik**)
7. prof.dr. Bruno Stiglic - FAKULTETA ZA ELEKTROT., RAČUNALN. IN INFORMATIKO; Maribor
8. dr. Matjaž Zwitter - ONKOLOŠKI INŠTITUT; Ljubljana

Nadzorni odbor:

1. prof.dr. Franc Habe - BIOTEHNIŠKA FAKULTETA; Domžale - (**namestnik**)
2. mag. Stane Kavkler - ISKRA TELA, d.d.; Ljubljana - (**član**)
3. prof.dr. Dragan Mihailovič - INSTITUT "JOŽEF STEFAN"; Ljubljana - (**član**)
4. prof.dr. Rasto Ovin - EKONOMSKO-POSLOVNA FAKULTETA; Maribor - (**namestnik**)
5. prof.dr. Adolf Šostar - FAKULTETA ZA STROJNIŠTVO; Maribor - (**član**)
6. dr. Darko Štrajn - PEDAGOŠKI INŠTITUT; Ljubljana - (**namestnik**)

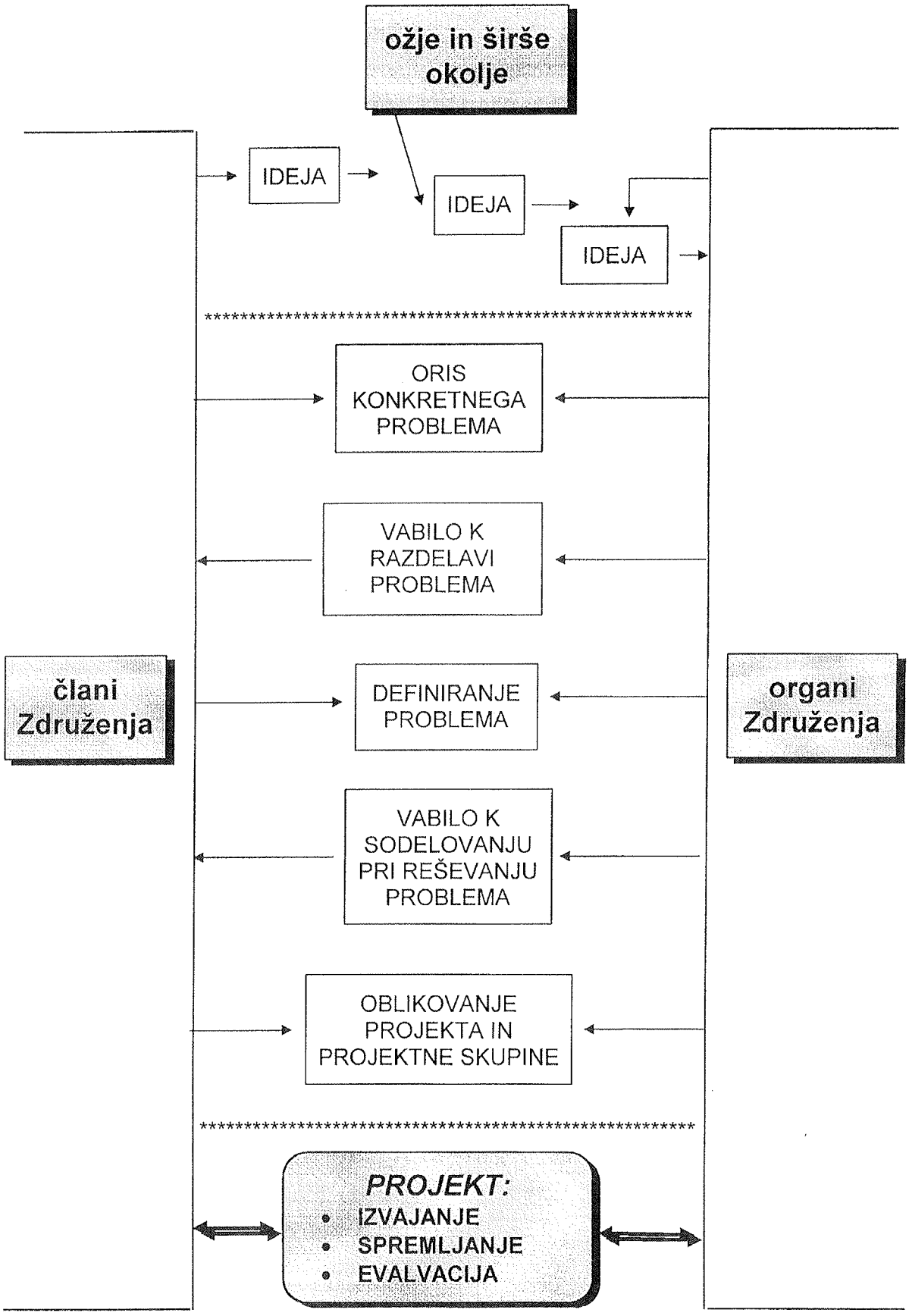
Častno razsodišče:

1. mag. Maja Bučar - FAKULTETA ZA DRUŽBENE VEDE; Ljubljana - (**članica**)
2. dr. Milan Bufon - ZNANSTVENORAZISKOVALNO SREDIŠČE RS; Koper - (**namestnik**)
3. prof.dr. Peter Fajfar - FAKULTETA ZA GRADBENIŠTVO IN GEODEZIJO; Ljubljana - (**član**)
4. Mija Marin, dipl.ing. - CINKARNA; Celje - (**namestnica**)
5. prof.dr. Janek Musek - FILOZOFSKA FAKULTETA; Ljubljana - (**član**)
6. prof.dr. Franci Sluga - NARAVOSLOVNO-TEHNIŠKA FAKULTETA; Ljubljana - (**namestnik**)

Generalni sekretar:

dr. Peter Tancig

Od idej do projektov



ZDRUŽENJE RAZISKOVALCEV SLOVENIJE

USTANOVNI ČLANI

(21. marca 1997 ustanovili Združenje)

mag. Jaro Berce
prof.dr. Robert Blinc
doc.dr. Borut Bohanec
prof.dr. Katja Breskvar
mag. Maja Bučar
prof.dr. Miran Čuk
dr. Kaliopa Dimitrovska Andrews
Trajan Dimkovski, dipl.ing.
prof.dr. Peter Fajfar
dr. Jasna Fischer
doc.dr. Vito Flaker
doc.dr. Matjaž Gams
dr. Marjetka Golež
doc.dr. Marija Gorenšek
mag. Ivan Grebenc
prof.dr. Franc Habe
prof.dr. Milan Hočevar
dr. Milena Horvat
dr. Vlasta Jalušič
prof.dr. Miha Japelj
dr. Roman Jerala
prof.dr. Tomaž Kalin
mag. Stane Kavkler
dr. Ivan Klemenčič
mag. Vera Klopčič
Miloš Kobe, dipl.ing.
dr. Miha Kos
dr. Marija Kosec
doc.dr. Stane Košir
mag. Iztok Košir
prof.dr. Božidar Krajnčič
dr. Tonči Kuzmanić
dr. Tamara Lah
Martin Logar, dipl.ing.
prof.dr. Jože Maček
prof.dr. Tatjana Malavašič
Mija Marin, dipl.ing.
prof.dr. Dragan Mihailovič
dr. Aleš Mihelič
prof.dr. Janek Musek
prof.dr. Dušan Nečak
prof.dr. Stane Pejovnik
Jožef Perne, dipl.ing.
Mitja Peruš, dipl.ing.
dr. Damjan Prelovšek
dr. Marjan Ravbar
dr. Rado Riha
dr. Franc Seme
dr. Tadej Slabe
prof.dr. Franci Sluga
prof.dr. Lojze Sočan
dr. Peter Stanovnik
prof.dr. Bruno Stiglic
dr. Darko Štrajn
prof.dr. Nace Šumi
dr. Peter Tancig
dr. Matjaž Torkar
prof.dr. Vito Turk
dr. Janez Tušek
Marko Vraničar, dipl.ing.
doc.dr. Danilo Zavrtanik
dr. Matjaž Zwitter
doc.dr. Igor Ž. Žagar
prof.dr. Boštjan Žekš
prof.dr. Boris Žemva
mag. Ingrid Žolgar

ZDRUŽENJE RAZISKOVALCEV SLOVENIJE

INICIATIVNI ODBOR

(dokončno oblikovan decembra 1996)

Bojan BORSTNER	Pedagoška fakulteta, Maribor
Katja BRESKVAR	Medicinska fakulteta, Ljubljana
Rudi BRIC	HERMES, SoftLab, Ljubljana
Lucija ČOK	Znanstveno-raziskovalno središče, Koper
Emil ERJAVEC	Biotehnična fakulteta, Ljubljana
Zarjan FABJANČIČ	Ekonomska fakulteta, Ljubljana
Peter FAJFAR	Fakulteta za gradbeništvo in geodezijo, Ljubljana
Jasna FISCHER	Inštitut za novejšo zgodovino, Ljubljana
Katja HOČEVAR	KOLINSKA, d.d., Ljubljana
Miha JAPELJ	KRKA, p.o., Novo mesto
Karel JEZERNIK	Fakulteta za elektrotehniko, Maribor
Tamara LAH	Inštitut za biologijo, Ljubljana
Jože MAČEK	Slovenska akademija znanosti in umetnosti, Ljubljana
Mateja MEŠL	A.L.P. PECA, d.o.o., Črna na Koroškem
Rasto OVIN	Ekonomsko-poslovna fakulteta, Maribor
Stane PEJOVNIK	Kemijski institut, Ljubljana
Janez PEKLENIK	Fakulteta za strojništvo, Ljubljana
Ljubo PIPAN	Fakulteta za računalništvo in informatiko, Ljubljana
Rado RIHA	Znanstveno-raziskovalni center SAZU, Ljubljana
Peter STANOVNIK	Inštitut za ekonomska raziskovanja, Ljubljana
Ivan SVETLIK	Fakulteta za družbene vede, Ljubljana
Peter TANCIG	Iniciativni odbor za ustanovitev ZRS
Vito TURK	Institut "Jožef Stefan", Ljubljana
Jože VIŽINTIN	Fakulteta za strojništvo, Ljubljana
Jože VOGRINC	Institutum Studiorum Humanitatis, Ljubljana
Danijel VRHOVŠEK	LIMNOS, d.o.o., Ljubljana
Maja ŽVANUT	Narodni muzej, Ljubljana

- je sestavljen reprezentativno glede na vede, vrste raziskovanja (vključno z razvojem izven akademske sfere), institucije, geografsko razdelitev, lastništvo
- deluje odprto in soglasno
- določa vsebino in obliko aktivnosti ter dokumentov
- organizira ustanovno skupščino Združenja
- deluje do volilne skupščine Združenja
- posamezni člani se vključijo v strukture Združenja

Združenje raziskovalcev Slovenije
Štefanova 12
1000 Ljubljana
tel.:(061) 12 11 200, faks: (061) 12 11 204
e-splet: http://www.zdr-raziskovalcev.si
e-pošta: tajnistvo@zdr-raziskovalcev.si

VESTI - NEWS

News from AMS

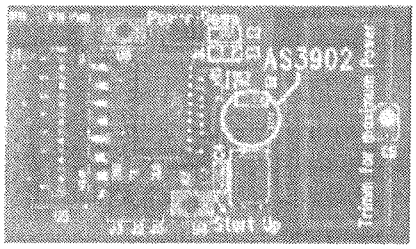
New electronic car key prevents consequences of the "hand effect"

Austria Mikro Systeme International is introducing a further innovative product for automobile applications: The new ASK (Amplitude Shift Keying) AS3902 sender, a chip for electronic car keys in the 433 MHz band that uses a fully integrated PLL-stabilised HF oscillator. The transmission frequency is thus independent from influence by neighbouring objects via the antenna.

The automobile industry offers electronic convenience systems, such as remote keyless entry systems, to an increasing degree as standard equipment of all models, even subcompact-size cars. Traditional systems in the 433 MHz ISM (IndustrialScientific - Medicine) frequency band use surface acoustic wave filter (SAW) oscillators. The SAW oscillators are simple in their structure, but confront the developer with a series of problems that are very difficult to overcome. The "hand effect" - caused by the hand of the user - has a particularly negative impact on the functioning of the oscillator as it detunes the frequency. The car key transmits the signal in a wrong frequency which often cannot be received by the car.

The newly developed AS3902 includes a bi-directional, combined 3-line interface. Keys are called up via this interface, the micro-controller is supplied with the system clock pulses, and it enables efficient power management incl. full power down mode without working clock. In the AS3902, the reference quartz required for the PLL sender is at the same time the clock generator for the micro-controller, which saves component costs. The integrated circuit can be supplied from a single lithium cell in a wide supply voltage range from 2.7 V to 5 V. Because of the differential output block it is ideally suited for use together with a small magnetic loop antenna.

Such an antenna can very easily be designed as a conductorpath on the board. A large loop surface means higher efficiency, less current consumption (long battery life) and larger range. The maximum antenna size of traditional SAW transmitters is, however, severely limited by the hand effect. With the AS3902, the loop size is only limited by the size of the car key.



433 MHz ASK sender application (original size)

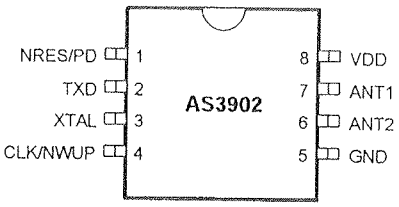
For a typical application, a key based on this circuit needs 3.8 mA at a peak power of 1 mW sent to the antenna.

The AS3902 conforms ta the ETSI EN 300-220 (European Telecommunication Standard). The overall system costs are lower than those of a SAW solution, as only 2 resistors and some capacitors are needed in addition to the reference quartz and the chip.

ISM 433 MHz ASK Transmitter

Key Features

- Supports the European 433 MHz ISM band.
- No frequency pulling by (antenna) load variation due to PLL synthesizer.
- Designed to be conform to EN 300 220-1 requirements.
- ASK data rate range from 0 to 32 kbit/s.
- Supports clock and reset signals for the external μC. Therefore no separate μC XTAL is required.
- Supports total shut down mode without any running XTAL oscillator.
- Typically 2 external resistors and 3 capacitors required.
- FSK operation by XTAL pulling possible.
- 315 MHz US ISM band application possible.
- Wide supply range between 2.7 V to 5 V.
- Low TX current, typical 7 mA @ transmitting a High ("H"), 600 μA @ transmitting a Low ("L").
- Wide operating temperature range from -40 °C to +85 °C.
- Miniature surface mount 8 pin SOIC or MSOP package.



SOIC-8 or MSOP-8

General Description

The AS3902 is a single channel low power 433 MHz ASK transmitter. It uses a fully integrated PLL stabilized RF-oscillator which avoids frequency pulling by approaching the antenna with objects as it occurs at SAW resonator based transmitters. ASK modulation is per-

formed by switching the transmitter on and off by an applied data stream.

The AS3902 contains a bi-directional three line micro-controller (μC) interface to support the μC with a clock and a reset signal and to operate the highly efficient power up/down management (including clock-free total shut-down) of the AS3902 by the μC.

As external components the AS3902 need only a reference XTAL, three capacitors and up to two resistors.

Applications

- Short range radio data transmission.
- Remote keyless entry systems.
- Domestic and consumer remote control units.
- Cordless alarm systems.
- Remote metering.
- Low power telemetry.

Austria Mikro Systeme International announces its MPW-Wafer Train for 2000 including 7 runs for it's new Silicon-Germanium Technology

The multi-product-wafer train schedule for 2000 provides a cheap prototyping service due to shared costs for masks and wafers. The customer delivers GDSII at fixed dates (TAPE-IN) and receives untested packaged samples within a lead time of typically 8 weeks for CMOS processes, 10 weeks for BiCMOS processes and 12 weeks for the SiGe-BiCMOS process.

In addition to the proven 0.6 μm and 0.8 μm CMOS and 0.8 μm BiCMOS technologies Austria Mikro Systeme International is offering 0.35 μm CMOS and 7 start dates for the new 0.8 μm Silicon-Germanium HBT-CMOS technology within this MPW service.

The 5 V CMOS processes are optimised for mixed analog/digital circuits. The high density of the 0.35 μm 3.3 V CMOS process enables the integration of complex mixed-signal systems on a single ASIC. The robust 0.8 μm BiCMOS process BYQ can be used for RF designs up to 2 GHz. For higher frequencies the new Silicon-Germanium HBT-CMOS process BYR is made available, which is based on the proven 0.8 μm mixed-signal CMOS process and includes an additional high performance analog oriented heterojunction-bipolar-transistor module. This advanced process offers high-speed npn-transistors with excellent analog performance such as high fmax and low noise, complementary MOS transistors, very low-parasitic linear capacitors, linear resistors and spiral inductors. The BYR Design-Kits for Cadence AnalogArtist and Hewlett-Packard ADS include simulation models, libraries of transistors and passive devices, logic gates, peripheral cells and simulation models for several packages.

MPW Runs 2000

Process	Tape in	Samples out
0.8 μm 5V CMOS		
CXQ/CYE	11.02.2000	07.04.2000
CXQ/CYE	12.05.2000	07.07.2000
CXQ/CYE	25.08.2000	20.10.2000
CXQ/CYE	24.11.2000	19.01.2001
0.6 μm CMOS		
CUQ/CUP	14.01.2000	10.03.2000
CUQ/CUP	31.03.2000	26.05.2000
CUQ/CUP	09.06.2000	04.08.2000
CUQ/CUP	15.09.2000	10.11.2000
CUQ/CUP	10.11.2000	05.01.2001
0.35 μm CMOS		
CSD/CSI	28.01.2000	24.03.2000
CSD/CSI	28.04.2000	23.06.2000
CSD/CSI	28.07.2000	22.09.2000
CSD/CSI	27.10.2000	22.12.2000
0.8 μm BiCMOS		
BYQ	04.02.2000	14.04.2000
BYQ	24.03.2000	02.06.2000
BYQ	05.05.2000	14.07.2000
BYQ	23.06.2000	01.09.2000
BYQ	11.08.2000	20.10.2000
BYQ	06.10.2000	15.12.2000
BYQ	01.12.2000	09.02.2001
08 μm SiGe		
BYR	04.02.2000	28.04.2000
BYR	24.03.2000	16.06.2000
BYR	05.05.2000	28.07.2000
BYR	23.06.2000	15.09.2000
BYR	11.08.2000	03.11.2000
BYR	06.10.2000	29.12.2000
BYR	01.12.2000	23.12.2001

Austria Mikro Systeme International AG
Schloss Premstätten
A-8141 Unterpremstätten, Austria
Tel.: +43 3136 500-103
Fax: +43 3136 500-491
Email: info@amsint.com
www.amsint.com

News from CMP

Announcement CMP introducing .18μ CMOS

Washington, USA and Grenoble, France - July 19. 1999 CMP today announced at the Microelectronics Education Workshop the introduction ot the HCMOS8 .18μ CMOS process from STMicroelectronics (Crolles, France).

The HCMOS8 process has the following features:

- Gate length : .18μ (drawn), .15μ (effective)
- Triple well
- Power supply 1.8 V
- Threshold voltages:
  - VTN = 420 mV,
  - VTP = 400 mV
- Isat:
  - TN @ 1.8 V : 600μ A/μm
  - TP @ 1.8 V : 280 μA/μm
- 6 metal layers + local interconnect
- Low k inter-level dielectric

Low leakage / low power and 3.3 V power supply options are also available.

Design kits are supported under Cadence, Synopsys, Eldo and Hspice.

Full custom designs are supported using Virtuoso layout editor and LAS synthesizer. The layout verifications (DRC, ERC, extraction, LVS) are fully supported for Diva and Calibre. Transistor-level simulations are supported under Eldo level 59, and Hspice level 50.

Standard-cell designs are supported using Verilog/VHDL descriptions for synthesis and simulation. Synthesis is supported under Synopsys. Simulation is supported under Verilog-XL, Leapfrog and VSS. The automatic place & route is supported under Silicon Ensemble suite of tools.

This process is available for prototyping to Education Institutions and Research Laboratories, on a cooperation basis. No commercial designs are accepted at this early stage. It is expected that llater on, the process will be available on a commercial basis for small volume production to Education Institutions, Research Laboratories and specified Companies. A .15μ process would then be made available Education and Research.

CMP also gave a summary of the achievements to date on the .25μ CMOS process introduced late 1997. A total of 28 have been or are being manufactured. Applications addressed by designers are RF circuitry, filters, opto-electronic circuitry, characterization, inductors, analog memories, very complex systems like neural network (2.7 million transistors in 11 mm^2 from DTU in Denmark and a processor in 50 mm^2 from LIP6 in France). Institutions that submitted circuits are from Denmark, Finland, France, Japan, Sweden, Switzerland. A total of 80 Institutions have been provided with the design rules. It is expected that many more different from a micronic or submicronic process.

Also CMP announced that the .25μ CMOS process becomes now available on a more broader basis, in the frame of a deep submicron consulting from CMP (check with CMP for details)

Finally, CMP announced that an option on the .25μ will be available in Q4 1999: the metal/metal capacitors option. Such an option will allow excellent performances for RF designs.

XXXXXX

CMP is a broker for a number of technologies (prototyping and low velume production). Since 1981, 450 Institutions from 40 countries have been served, through more than 300 runs semiconductor houses have been interfaced.

- Integrated circuits
  - AMS
    - 0.8μ CMOS DLP/DLM
    - 0.6μ CMOS DLP/DLM
    - 0.35μ CMOS DLP/DLM (4LM)
    - 0.8μ BiCMOS DLP/DLM
    - 0.8μ SiGe HBT-CMOS DLP/DLM
  - STMicroelectronics 0.18μ, 0.25μ 6LM
  - PML 0.2μ HEMT GaAs HEMT
- MEMS
  - CMOS and GaAs compatible bulk micromachining MUMPs from MCNC (Europe, Africa, South America...) DOE from CSEM
- Design kits
  - more than 35 design kits
- MCM and 3D packaging
  - L, C, D, 3D
- CAD software
  - CADENCE, MEMSCAP, TANNER,...
- Packaging

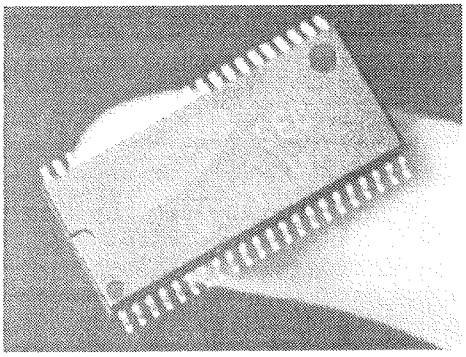
Circuits Multi-Projets
46 avenue Fèlix Viallet
38031 Grenoble Cedex - FRANCE
Tel. : +33 4 76 57 48 04
Fax : +33 4 76 4 7 38 14
E.mail: cmp@archi.imag.fr
WWW: http://tima-cmp.imag.fr/CMP/CMP.html

News from EUROPEAN SEMICONDUCTOR

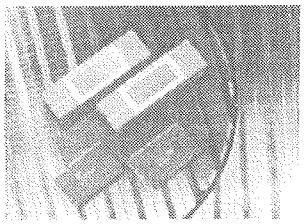
Samsung goes ferroelectric

The leading South Korean DRAM company, Samsung Electronics, has developed a 4 Mbit ferroelectric RAM (right). Competitors in Japan, Europe and the US are still only working on 256 kbit versions, Samsung claims. Operation voltage is 3.3 V and data processing speed is 75 ns. The cell is a 1-transistor/1capacitor structure using capacitor over-bitline (COB) technology.

Samsung estimates that these breakthroughs puts it at least two years ahead of the competition. Engineering samples are to be available by the end of the year.



Samsung has also developed1Gbit DDR SDRAM (double data rate synchronous DRAM, below) using 0.13 μm technology. The 350 MHz chip was developed at Samsung Austin Semiconductor in the US. Samsung says the device uses the same processing architecture and 248 nm lithography as its 0.13 μm 256 Mbit DRAM process.



Litho news

IMEC is calling for major 100 nm CMOS R&D collaboration. IMEC plans to tackle some major bottlenecks on the International Technology Roadmap for Semiconductors (1999) with its 2003 deadline for 100 nm (two years earlier than 1998's SIA roadmap).

The IMEC project will concentrate on optical lithography (illumination, OPC, phase-shift, 193 nm, ...), advanced etch, new gate stacks (high-k gate dielectrics, metallic gate electrodes, ...), ultrashallow gate formation (new architectures, silicide module integration, ...), transistor architectures, back-end-of line architecture (copper, low-k, ...), technological limits and reliability.

ASM Lithography has formally announced its 157 nm lithography programme. The goal is to deliver production tools by 2003.

Strategic partners are Carl Zeiss, optic materials supplier Schott and laser suppliers Cymer and Lambda Physik. In April, a German 157 nm initiative was announced led by Carl Zeiss and involving Schott, Lambda Phyisik, Infineon and Jenoptik. Carl Zeiss and Cymer announced an alliance in May.

ASML and Carl Zeiss have performed initial design studies suggesting the feasibility of a high numerical aperture lens enabling 157 nm to achieve greater resolution and process latitude than 193 nm technology. Challenges include developing a photoresist and process within a time frame much accelerated on previous moves in the industry ASML and IMEC are looking at the possibility of starting a 157 nm process development programme by the middle of next year. At that time ASML expects to have completed design concept studies and to be beginning preparation of the infrastructure for development and prototyping.

Copper developments

Apart from developments in copper/low-k dielectric integration (Applied Materials and Novellus Systems) reported elsewhere in this month's *European Semiconductor, a* number of companies brought products designed to meet the needs of semiconductor manufacturers planning to use copper interonnects.

Dr Yoshio Nishi of **Texas Instruments**' DSP group reported the introduction of copper at 0.18 μm this year for the company's high-end products. The next-generation - at 0.13 μm in early 2001 - will be all-copper.

Dr Fu-Tai Liou, senior vice president of Taiwanese foundry **UMC Group** (which recently achieved the milestone of 50% copper yields) reckons that UMC will solve its yield degradation problems "within several months", although he was "glad to see that TI needed copper at 0.18μm for the required speed" and that "price is not a problem"!

UMC is currently doing copper prototyping to make 0.18μm foundry processes available to early adopters like TI at the end of this quarter, with pilot production at 0.13 μm in Q1/01.

SEZ was promoting its new copper contamination cleaning process for removing copper film from the wafer backside, the bevel/edge and the frontside wafer edge exclusion zone (up to 5 mm). The process has been implemented at **ERSO** in Taiwan, **Sematech** and "several of its member companies" (a Spin-Processor 203 goes to **Lucent** soon).

MKS Instruments launched the Orion Copper CVD Process Monitor, which uses quadrupole mass spectrometry and Orion Windows NT process-monitoring software to maintain repeatability and control process

drift. MKS says it has been tested during continuous on-line monitoring of the entire copper CVD process at pressures up to 5 Torr.

Cabot, which has 80% of the market for CMP slurry, has entered the CMP pad business, following work at alpha and beta sites with W-2000 slurry and experimental pads. Cabot says use of slurry-pad sets will eliminate variability.

Epic-W1 for tungsten CMP is available, with pads for copper (both inter-level dielectric and shallow trench isolation) being sampled. A pad lifetime of 325-500 wafers is claimed. The goal is to replace pads just once a day.

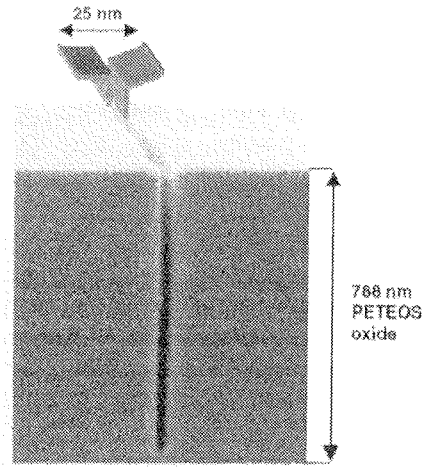
For copper, post-CMP clean is more important so Cabot has developed post-CMP copper cleaning materials which are being tested by Sematech and sampled by two customers. Cabot claims it is working with over 20 companies on copper (including UMC).

Luxtron and **Strasbaugh** have formed a technology and OEM partnership to develop a multisensing in-situ, real-time endpoint detection control system for CMP. Phase one has already evaluated Luxtron's motor current sensing technology in Strasbaugh's 6DS-SP CMP system. Later phases will integrate optical, temperature and film thickness capabilities.

Nanotrench

A multi-national team working at International Sematech's Resist Test Center (Austin TX) has successfully created 25 nm wide trenches. The trenches were produced using a deep UV 193 nm CARL photoresist system developed by Infineon Technology researchers in Erlangen. A chemical biasing step is needed to produce trenches and (in work announced in June) contact holes.

The lithography used a 0.6 NA microstepper and a binary mask. The etch step was performed on an OMEGA plasma system (ICP and MORI modules) from Trikon Technologies (Newport, UK).



Crossection SEM of 25 nm trenches etched in 788 nm (PETEOS) at an aspect ratio of 31.

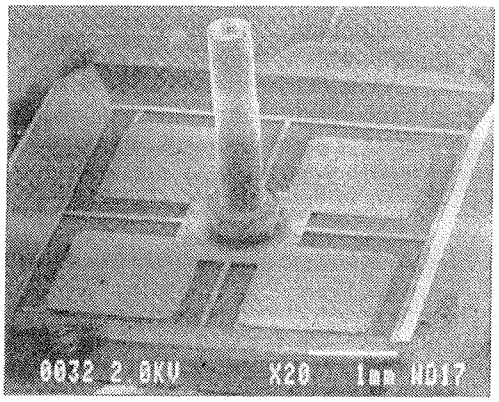
Spinning at 300 mm

Austrian spin-processing tool maker SEZ has entered a joint 300 mm project with Samsung Electronics. Etch and cleaning technologies are to be developed to replace some current batch processes with less expensive and more effective single-wafer techniques. The two companies will be working on sub 0.25 μm applications - front-side polysilicon etchback, removal of metal and non-metal films, and wafer cleaning. SEZ has already installed a Spin-Processor 303 and is performing 300 mm semiconductor wafer reclaim at Samsung.

* Nikon Precision Europe is to deliver a second 300 mm deep UV scanning system to the Semiconductor 300 Infineon Technologies/Motorola joint pilot line in Dresden. The NSR-S203B/300 mm is designed for production below 0.18 μm. The first Nikon system was installed at Dresden last year.

Microgyro licence

NASA's Jet Propulsion Laboratory has licensed microgyroscope technology to Hughes Space and Communications. The device, jointly developed by JPL and Hughes, weighs less than 1 gram and measures 4 x 4 mm.



A silicon machined vibratory micro-gyro produced by JPL/UCLA at the Microdevices Laboratory

The gyroscope can sense very slow rotations down to 1° per hour. Current gyroscopes-on-chip are usually only useful down to 6° per minute. For space applications the rule is "the slower the better" because the slowest of rotations can take craft significantly off target over an extended period.

Engineering development of the instrument was led by JPL's Dr Tony Tang. The Hughes/JPL work began in 1997 and Hughes recently acquired exclusive rights from Caltech to develop the gyro for space applications. JPL also works with UCLA on micro-gyros at the Centre for Space Microelectronics Technology (picture).

BOC Edwards acquisition

BOC Edwards has completed acquisition of FSI's Chemical Management division for $38m. (Parent company BOC is in its turn being taken over by a French/US consortium of Air Liquide and Air Products, *European* Semiconductor, August 1999.)

FSI Chemical Management president Nigel Hunton said: "The additional product development laboratories allow BOC Edwards to more effectively address the rapid technical advances of the semiconductor industry for copper interconnects, low-k materials and higher purity chemistries."

* At Semicon West, BOC Edwards was displaying its copper capabilities. The company offers Cu expertise for electroplating (chemistry delivery and waste management), CVD (precursors, vacuum pumping and exhaust management) and CMP (slurry delivery for pilot and production lines). BOC Edwards worked with SUNY/Albany (State University of New York) to provide a bath with minimal maintenance and superior gap fill.

IMAPS '99

DON'T MISS THE FREE BOOKS AT IMAPS '99

Once again IMAPS is giving away FREE BOOKS as a special benefit for IMAPS '99 attendees. So get to the Chicago Hilton & Towers early, because these books will go quickly!

IMAPS 99

32nd International Symposium on Microelectronics

October 26-28,1999

Chicago Hilton & Towers

Chicago, Illinois

http://209.8.150.53/imaps99

Featured this year are 24 Technical Sessions,15 Professional Development Courses (October 24-25), an Exhibition of over 300 Exhibitors, and the 3D Packaging Workshop (October 25). New this year are two Hands-on Factory Workshops on

Wirebonding and Screen Printing (October 24-25). Class size for the Hands-on Factory Workshops is limited so sign up early.

Also at the Chicago Hilton & Towers (October 23-25) is the Advanced Technology Workshop on the Packaging of MEMS & Microsystems.

New IMAPS '99 Special Event

In cooperation with the Electronics and Photonics Technology Office (EPTO) of the NIST Advanced Technology Program (ATP), IMAPS invites you to participate in the following IMAPS '99 Special Event.

New Funding Opportunities in Electronics Technologies

Tuesday, October 26,1999

5:00 7:00 P.M.

Continental - Section A

Chicago Hilton & Towers

IMAPS invites you to an extended presentation by the NIST Advanced Technology Program. Started in 1990, the ATP is a unique partnership between the U.S. government and American industry to accelerate new ideas, new technologies, and new markets that promise significant payoffs and benefits for the American economy.

Who should attend? If you are from industry, academia or government and are interested in exploring emerging R&D investment directions and opportunities, then don't miss this public presentation. Learn about the ATP and their new funding opportunities. Learn how American companies can successfully compete in ATP electronics competitions. Learn what technologies your colleagues and competitors are developing in partnership with ATP's EPTO.

For more information about this special IMAPS presentation or the Advanced Technology Program, visit their website at **http://www.atp.nist gov** and look under the Electronics and Photonics Technology Office.

KOLEDAR PRIREDITEV - CALENDAR OF EVENTS

OCTOBER

October 4-6, 1999
THERMAL INVESTIGATION ICs AND SYSTEMS
ROME, ITALY,
Contact Bernard Courtois,
TIMA e-mail: Bernard.Courtois@imag.tr
web: www.tima-cmp.imag.fr

October 6-7, 1999
SEMICONDUCTOR SAFETY ASSOCIATION
(EUROPE), PARIS, FRANCE
Contact Dr. BE Watts, SSA (Europe)
Tel: +441327 356776
e-mail: brian.watts@gecm.com
web: wsvw.ssa-euro.org.uk

October 6-7, 1999
TEST, BIRMINGHAM, UK
Contact Lee Walker, Inside Communications
Tel: +44171837 8727
Fax: +44171837 7124
e-mail: eptest@dial.pipex.com
web: wwwinsidel,ctronics.com

October 12-14, 1999
EUROPEAN SMART CARD, ZURICH, SWITZERLAND
Contact Martin Scott, Turret RAI
Tel: +441895 454438
Fax: +441895 454588
e-mail: info@smart.card.uk.com
web: www.smart.card.uk.com/euro.htm

October 17-19, 1999
EUROPEAN ELECTRONICS 99, SINTRA, PORTUGAL
"Sofhvare meets silicon — driving the system-on-chip revolution"
Contact Future Horizons
Tel: +441732 762896
Fax: +441732 763914
e-mail: mail@future-horizons.net
web: www.future-horizons.net

NOVEMBER

November 1-2, 1999
IP99, EDINBURGH, UK
Conference on intellectual property.
Contact John Whitaker, Miller Freeman
Tel: +44 171 861 6376
Fax: +44 171 861 6247
web: www.ip99.com

November 2-3, 1999
"QUO VADIS MEDIA?", DRESDEN, GERMANY
Joint media technical conference. Focus on applications for ultra-pure silicon chip production. Supported by SEMI.
Contact Christian Ernst, Fraunhofer IPA
Tel: +49 711 9701248
Fax: +49 711 9701399
e-mail: che@ipa.fhg.de
web: jointmedia.ipa.fhg.de

November 4-5, 1999
SEMI EUROPE STANDARDS COMMITTEE
BRUSSELS, BELGIUM, Meetings and conference,
Contact Carlos Lee at SEMI Europe
Tel: +32 2 289 6490
Fax: +32 2 511 4345
e-mail: clee@semi.org
web: www.semi.org

November 9-12, 1999
PRODUCTRONICA 99, MUNICH, GERMANY
Contact Messe München
Tel: +49 89 9 49-01
Fax: +49 89 9 49-09
e-mail: info@messe-muenchen.de
web: www.productronic.de

November 15-17, 1999
AREA ARRAY PACKAGING TECHOLOGIES,
BERLIN, GERMANY
Contact Evelyn Erlebach, IEEE-CPMT
Tel: +49 30 467 815-55
Fax: +49 30 467 815-51
e-mail: erlebach@pactech.de

November 15-19, 1999
EUROFE 99, TOLEDO, SPAIN
Europe's first conference on all aspects of field emission.,
Contact Tim E. Harper, CMP Cientifica
Tel: +34 91 640 71 85
Fax: +34 91640 7186
e-mail: tim@cmp-cientifica.com
web: www.cmp-cientifica.com

November 25-26, 1999
ESPID 1, TOULOUSE, FRANCE
First European Symposium on Plasma Process Induced Damage.
Contact Dr D Celier, SFV (French Vacuum Society)
Tel: +33 1 53 01 90 31
Fax: +33 1 42 78 63 20
e-mail: sfv@club-internet.fr
web: www.espid.org

DECEMBER

December 5-8, 1999
INTERNATIONAL ELECTRON DEVICES MEETING,
WASHINGTON DC, USA
Contact Phyllis Mahoney, IEDM manager
Tel: +1 301 527 0900
Fax: +1 301 527 0994
e-mail: pwmahoney@aol.com
web: www.ieee.org/conference/iedm