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CSD-DERIVED FERROELECTRIC THIN FILMS MOLECULAR DESIGN FOR PROPERTIES

Hisao SUZUKI

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Key words: Chemical solution deposition (CSD), lanthanum nickel oxide, Si wafer

Abstract: Chemical solution deposition (CSD) is the smart and cost effective processing method for advanced materials and thin films. For the smart chemical processing of thin films and nanoparticles by the CSD, molecular design of the precursor is essential. In this study, the importance of the molecular design for the chemical processing is focused on the orientation and residual stress control of the ferroelectric thin films. For the orientation and residual stress control of the ferroelectric thin films and, in some cases, oxide thin film electrode such as lanthanum nickel oxide, LaNiO₃ (LNO), which acted as a seeding layer for the orientation control. Namely, we used large side chain groups for the LNO precursor solution to control the film orientation and the residual stress of the ferroelectric thin films, by introducing the nanopores in the LNO layer on a Si wafer to relax the tensile constraint force from a Si wafer.

The other method to relax the tensile stress from a Si substrate with very low coefficient of thermal expansion (C.T.E.) was to reduce the thickness of the Si wafer. The residual compressive stress or strain for the ferroelectric thin film will lead to the following effects; (1) Curie temperature shift towards the higher temperature, (2) Morphotropic phase boundary shift in the case of $Pb(Zr_x Ti_{1,x})O_3$ (PZT), and (3) Enhanced electrical properties. In this study, these effects were experimentally elucidated for the CSD-derived PZT thin films with a composition near MPB.

Feroelektrične tanke plasti izdelane z metodo kemijskega nanosa iz raztopine, CSD – načrtovanje lastnosti s pomočjo molekularne strukture

Kjučne besede: Priprava tankih plasti s sintezo iz raztopin (CSD), Oksidni prevodnik lantanovnikelat (LNO), silicijeva rezina

Izvleček: Priprava tankih plasti s sintezo iz raztopin (Chemicalsolutiondeposition, CSD) je pametna in cenovno ugodna metoda sinteze naprednih materialov in tankih plasti. Za sintezo tankih plasti in nano-delcev je ključno načrtovanje prekurzorjev na molekularnem nivoju. V tem delu je poudarek na pomenu načrtovanja prekurzorjev na molekularnem nivoju za izbrano kristalografsko usmerjenost in kontroliranje napetosti v feroelektričnih tankih plasteh. Načrtovali smo strukturo prekurzorjev feroelektričnih tankih plasti in prevodnih oksidnih plasti na molekularnem nivoju. Oksidni prevodnik lantanovnikelat (LNO) je služil tudi kot nukleacijska plast in omogočil kontrolo kristalografske usmerjenosti feroelektrične plasti. Pripravili smo prekurzor LNO z velikimi stranskimi verigami, iz katerega smo pripravili plasti LNO z nanoporami na silicijevi rezini, na katere smo nadalje nanesli feroelektrične plasti, kar nam je omogočilo kontrolo kristalografske usmerjenosti in napetosti feroelektričnih plasti.

Naslednja metoda relaksiranja nateznih napetosti plasti na podlagah silicija, za katerega je značilen nizek linearni temperaturni razteznostni koeficient, je zmanjševanje debeline podlage. Posledice tega so: (1) pomik Curiejeve temperature k višjim vrednostim, (2) premik morfotropne fazne meje v primeru Pb($Zr_x Ti_{1,x}$)O₃ (PZT) in (3) izboljšane električne lastnosti. V študiji smo omenjene vplive eksperimentalno pojasnili pri tankih plasteh PZTs sestavo blizu morfotropne fazne meje.

1. Introduction

Lead zirconate titanate (Pb(Zr,Ti)O₃:PZT) thin films exhibit high potential for ferroelectric random access memories, microactuators and infrared sensors as well as for Micro-Electro-Mechanical Systems (MEMS) because of their excellent ferroelectric, piezoelectric and pyroelectric properties /1/. In order to deposit PZT films, various techniques have been used, such as CSD, sputtering, and metal organic chemical vapor deposition (MOCVD). Among these techniques, CSD has advantages for producing PZT thin film devices due to its simplicity, easy control of homogeneous compositions and film thickness for large substrates, and low processing temperature, as compared with other techniques /2, 3/.

Electrical properties of PZT films are strongly dependent on several factors such as composition, crystal orientation, thin film electrode, and residual stress. Therefore, it is very important to control these factors. For the case of film orientation, (001)-oriented tetragonal PZT films and (111)-oriented rhombohedral PZT films are expected to show good electrical properties. There are many reports on the orientation control of PZT films /4, 5, 6/. Epitaxial PZT films with different orientations have been deposited on single crystal substrates of MgO and SrTiO₃ /7, 8/. However, highly c-axis oriented PZT films deposited on a silicon substrate are required for many advanced devices. It has been reported that a tetragonal PZT should have large Pr value and large d₃₃ along /001/ direction even for the rhombohedral PZT after the theoretical calculation /9/. Therefore, it is very important to prepare the (001)-oriented PZT films on a silicon substrate.

There are three strategies to control the PZT film orientation. One is the use of the in-situ seeding layer of good lattice matching with the PZT. In the previous study, we investigated the effect of the pre-annealing temperature on the orientation of the resultant PZT thin films, in which insitu seeding layer was formed during pre-annealing /10/. In addition, the novel method of Electric-Field-Assisted Annealing (EFA-A) was demonstrated as the second effective method to control the orientation of the PZT thin films on Pt/Ti/SiO₂/Si substrates through CSD /11/. EFA-A is the method of applying an electric field to thin film during annealing. The XRD intensities of the (001)&(100) planes in the films deposited with an EFA-A increased and that of the (111) plane decreased. However, the ferroelectricity did not improve effectively because the residual cracks still existed in the surface of the films. In this paper, an EFA-A was applied only to the first PZT seeding layer with a same composition. The PZT film was deposited on the seeding layer by rapid thermal annealing (RTA) without an electric field to investigate the relation between crystal orientation, microstructures and electrical properties of the resultant films.

The other factors that affect the electrical properties of the CSD-derived PZT thin films are composition, thin film electrode and the residual stress in the resultant films which strongly depends on the substrate including thin film electrode and the annealing processes as well as the film thickness. The film composition is easy to control if the molecular-designed precursor solution is used. In this paper, we mainly prepared PZT precursor solution with a composition near morphotropic phase boundary (MPB; Pb:Zr:Ti = 120:53:47) and used Pt/Ti/SiO₂/Si substrate because of the compatibility with the semiconductor. Therefore, the last important factor we focused in this paper is the residual stress in the films because ferroelectricity and piezoelectricity should be strongly affected by the residual stress in the films which is strongly affected by the thin film processing.

2. Experimental Procedure

Lead acetate trihydrate, titanium iso-propoxide and zirconium n-propoxide were used as starting materials, and absolute ethanol was used as a solvent to prepare the precursor solution for CSD. The Zr/Ti ratio was mainly 53/47, and excess Pb (20 mol%) was added to the precursor solution to compensate for the lead depletion of lead during processing by the evaporation and diffusion into the platinum electrode. Therefore, the nominal composition of the precursor solution was equivalent to that of Pb_{1.2}(Zr_{0.53}Ti_{0.47})O₃. Details of the precursor solution preparation are described elsewhere /12/. The concentration of the PZT precursor solution was controlled at 0.6 M.

Orientation control of the PZT films were carried out by using in-situ seeding layers of (001)-oriented PbO or (111)-oriented Pt/Pb alloy, which could be deposited during pre-annealing at 350 °C or 420 °C. We also used EFA-A to increase the (001)-oriented grains in the films /11/. Final

annealing was performed at 650 °C for 5 min. in air by the rapid thermal annealing (RAT).

Crystalline phases in the resultant PZT thin films were identified by X-ray diffraction (XRD). For electrical measurement, Au top electrode was sputtered through the metal mask with 200 or $50\mu m$ circular holes. To control the residual stress in the films, we used the back-etching technique to prepare the diaphragm structure with different residual Si substrate thickness /13/.

Dielectric behavior of the resultant PZT thin films was measured by LCR meter (HP-4284A). P-E hysteresis loops and the piezoelectric property for the resultant thin film capacitors were measured by the ferroelectric thin film test system combined with scanning probe microscope (Toyo corporation, FCE-PZ and SII Nanotechnology Inc., SPI3800N).

3. Results and Discussion

3.1. Deposition of highly oriented PZT Film

For the deposition of high performance PZT thin films on a Si wafer, molecular-designed precursor solution is essential. Figure 1 shows the bulk gel of PZT prepared by the careful aging of the precursor solution in a humidity to proceed partial hydrolysis and following polycondensation for a very long period.

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As shown in Fig.1, large and transparent PZT gel was obtained after the long aging, showing the very high homogeneity of the precursor solution, in which metal-oxygen-metal bonding was successfully formed. From such precursor solution, we can easily deposit highly oriented PZT thin films even on the semiconductor compatible Pt(111)/Ti/SiO₂/Si substrate if the proper annealing process was selected. We chose the RTA for the deposition of highly oriented PZT thin films with a MPB composition by using in-situ seeding layers and EFA-A treated PZT seeding layer.

Figure 2 shows the lattice matching of the seeding layers used in this study. By using these seeding layers, we successfully deposited the highly (111)-and (001)&(100)-oriented PZT thin films with different compositions on a Pt(111)/Ti/SiO₂/Si substrate. Figures 3 and 4 exhibit the XRD patterns and cross-sectional images of scanning electron microscope for the PZT films with tetragonal and rhombohedral symmetries.



PZT(120/40/60)

Fig.3 a XRD patterns for PZT thin films with tetragonal symmetry.



PZT(120/60/40)

Fig.3 b XRD patterns for PZT thin films with rhombohedral symmetry.

XRD results demonstrated that highly oriented PZT thin films more than 90% degree of orientation could be deposit by using the in-situ seeding layers for both directions in wide compositional region.



(b)



Fig.4 Cross-sectional SEM images for CSD- derived PZT thin films of MPB composition with (a) (111)- and (b) (001)&(100)- orientation.

In addition, all these films exhibited nice columnar structure of relatively large grain size. Therefore, we can expect good electrical properties for these films, especially for the PZT films with a MPB composition. Orientation mechanism was described elsewhere /14/

3.2. Electrical properties of highly oriented PZT thin films

Molecular design of the precursor solution and the use of seeding layer allowed to deposit highly oriented PZT thin films on a Pt(111)/Ti/SiO₂/Si substrate, especially for the case of the (001)&(100)-oriented films which was expected to exhibit good electrical properties. Therefore, we measured the electrical properties of these oriented PZT thin films. Figure 5 shows effective d_{33} values for the highly oriented PZT thin films. The effective d_{33} values were measured by the continuous charge integration (CCI) method /15/. The effective d_{33} value measured by CCI method includes not only true d_{33} value but also d_{31} and d_{15} values because of the bending effect. Therefore, the effective d_{33} values measured by CCI method are relatively larger than those measured by SPM method with small top electrode. However, CCI method is useful to compare the effective d_{33} values for thin films because of its simplicity. Those two method exhibited same tendency for the piezoelectricity of the PZT thin films as shown below in this paper.



Fig.5 Relation between effective d33 and the compositions for PZT thin films with different film orientations.

Figure 5 demonstrated that CSD-derived highly oriented PZT thin films exhibited highest and excellent piezoelectricity at a MPB composition. In addition, (001)&(100)-oriented films exhibited higher effective d₃₃ values in the case of the rhombohedral symmetry, according to the theoretical calculation /9/. On the other hand, (111)-oriented PZT thin films exhibited higher effective $\mathsf{d}_{\scriptscriptstyle 33}$ value than the (001)&(100)-oriented films. This behavior is controversial collision with a theoretical calculation. We postulated that this behavior was ascribed to the domain orientation in tha (001)&(100)-oriented PZT thin films in the tetragonal region. Then, we tried to deposit highly (001)-oriented PZT thin films in a tetragonal region by using EFA-A derived PZT seeding layer together with a PbO seeding layer. As a result, we successfully deposited highly (001)-oriented PZT thin films with degree of orientation more than 95 % by the XRD measurement. Figures 6 and 7 show the dielectric constant and effective d₃₃ values for the PZT thin films with different composition and film orientation. Because the single crystals of PZT with a MPB composition have not been prepared, we can not compare the actual values of dielectric and piezoelectric constants for the highly oriented PZT thin film and single crystal near the MPB composition. However, these values have been calculated /9/.







Fig.7 Relation between effective d₃₃ and composition of PZT thin films with different orientations.

For the case of dielectric constant, highly (001)-oriented PZT films deposited on the EFA-A derived seeding layer exhibited lower dielectric constants in the tetragonal region according to the theoretical calculation. This is ascribed to the increase in the (001)-oriented grains in the PZT thin films with a tetragonal symmetry, which means the dielectric constant along the a-axis is higher than that along the c-axis in the tetragonal region of PZT. Then, we compared the effective d_{33} values for the PZT thin films in the tetragonal region by using the CCI method and SPM method, as shown in Fig. 7. Figure 7 clearly showed the higher effective d_{33} for the films deposited by the EFA-A in the tetragonal region and exhibited still very high effective d_{33} value more than 400 (pm/V) even if measured by the SPM method.

This value is the highest one for the PZT thin film with a MPB composition measured by the SPM method. Therefore, this figure demonstrated that highly c-axis oriented PZT thin films should exhibit higher piezoelectricity independent of the composition, showing the good agreement with the theoretical calculation after Du et al. /9/.

3.3 Stress induced gigantic piezoelectricity

For the better electrical properties of the CSD-derived highly oriented PZT thin films, residual stress in the resultant films should be controlled. In addition, residual stress could be changed by the device structures. Therefore, we chose the diaphragm structure as the actual device structure which could be used for the MEMS devices. Previous study have reported that the residual stress in the lead titanate thin films on the diaphragm structure with different residual thickness of Si substrate dramatically increased up to around 1.6 GPa, if the residual thickness of Si substrate was decreased below 150mm as shown in Fig.8. Therefore in this study, highly oriented PZT thin film with a MPB composition was deposited on the diaphragm structure with different residual thickness of Si substrate and the piezoelectric constant for the PZT thin films were measured by the SPM method to elucidate the effect of the residual stress in the film. Figure 9 shows the effective d₃₃ values for the PZT thin films with a MPB composition on a diaphragm structure with different residual thickness of Si substrate. As a result, effective d_{33} values dramatically increased at the residual thickness of the Si substrate was 50 µm and reached more than 400 (pm/V). For the case of the lead titanate thin films on the same substrate structure, the residual stress in the films dramatically increased if the residual thickness of Si substrate was decreased below 150µm and reached platoe at aroud 50µm. Therefore, the higher effective $d_{_{\rm 33}}$ value for the PZT thin film on the diaphragm structure with 50µm residual thickness of Si substrate could be ascribed to the residual compressive



Fig. 8 Relation between residual stress in films and residual thickness of Si substrate measured by raman spectroscopy¹³⁾.

stress in the film, showing the stress induced gigantic piezoelectricity. This value is almost same as that of the PZT thin film deposited by using both PbO and EFA-A derived PZT seeding layers. However, in this case, we did not use the EFA-A derived PZT seeding layer. This indicated that the residual stress in the film played an important roll for the piezoelectricity of the resultant PZT thin film.



Fig.9 Effective d₃₃ for PZT thin films with a MPB composition and different residual thickness of Si substrate.

4. Conclusions

This paper focused on the total processing of the CSDderived PZT thin films on the Pt/Ti/SiO₂/Si substrate, including the orientation control method and the stress induced gigantic piezoelectricity. For the highly oriented PZT thin films on a semiconductor compatible Pt/Ti/ SiO₂/Si substrate, molecular-designed precursor solution and the suitable seeding layers were essential. The electrical properties of the resultant thin films with different orientations were elucidated by using several methods. These measurements demonstrated that highly oriented PZT thin films exhibited reasonable electrical properties and showed good agreement with those of the theoretical values. In addition, piezoelectric measurement for the highly oriented PZT thin films on the diaphragm structure exhibited the importance of the residual stress in the film. This paper demonstrates that residual stress control is another essential factor for the high performance MEMS devices, even for the highly oriented PZT thin films.

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TECHNOLOGY AND APPLICATIONS OF MICRODOSING SYSTEMS

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Key words: microdosing system, black box, micro pumps

Abstract: Meeting demands of industrial customers of micro fluidic actuators in application fields like drug delivery systems, lubrication dosing or lab technology, a black box concept has been carried out. Various practical problems and drawbacks of micro pumps like weak dosing accuracy, particle vulnerability, gas bubble intolerance, back pressure dependence and free flow problem are addressed and solved within that black box. To solve these particular problems new concepts and ideas as well as a theoretical understanding and technological optimization of the challenges of the micro dosing systems has been realized.

Feroelektrične tanke plasti izdelane z metodo kemijskega nanosa iz raztopine, CSD – načrtovanje lastnosti s pomočjo molekularne strukture

Kjučne besede: mikrodozirni sistem, črna skrinjica, mikročrpalke

Izvleček: V zvezi z zahtevami industrijskih kupcev mikrofluidnih aktuatorjev na področju dozirnih sistemov za uvajanje zdravil, odmerjanja lubrikantov ali laboratorijskih tehnologij, je bil raziskan koncept črne skrinjice. Veliko praktičnih problemov in pomanjkljivosti mikročrpalk kot npr. slaba dozirna natančnost, občutljivost na delce, netoleranca na plinske mehurčke, vpliv protitlaka in problem prostega toka je rešen s konceptom črne skrinjice. Za razrešitev teh problemov so bili realizirani novi koncepti, ideje, teoretično razumevanje in tehnološko optimiziranje mikrodozirnih sistemov.

1 Introduction

Micro devices especially for micro fluidic applications can be applied to a wide variety of industrial solutions. Key components are micro pumps /1/, micro dosing systems, micro mixers, micro valves, micro reactors and flow sensors and their combination for the use in biotechnology, chemistry and medicine. Furthermore, applications in the field of lab technology and fuel cells can be addressed. Challenges in that field are addressing the improvement of the reliability, dosing accuracy and user safety by the integration of free flow protection, bubble point free filters and improved dosing accuracy to the micro pump modules. Another trend is the development of complete systems, including electronics, sensors and system control.

2 Black box strategy

Piezoelectrical driven micro fluidic actuators like micro pumps can be used in many applications. Requirements like dosing accuracy, back pressure independence, small size, low energy consumption, particle resistance and free flow protection are leading to new technologic solutions to develop the micro pump from a demonstrator to a industrial product. The user of the micro pump is expecting a complete solution from the developer solving all of these requirements. This "black box" approach will be realized solving the requirements above helping the customer to launch new products.

Most user of a micro dosing system have the following task to be solved for their application: there is a given liquid, which has particles and gas bubbles inside, and which is on an inlet pressure level p1. The task now is to ensure a given flow rate Q also at varying outlet pressures p3 without particles and without bubbles at a defined dosing accuracy and avoiding any free flow. The ideal black box has to fulfill all of these demands (fig. 1).



Fig. 1: Black box concept. Main general microdosing problems are solved within that black box.

The best performance for a dosing task show, beside conventional miniature pumps, piezoelectric driven micro

diaphragm pumps with passive check valves. However, it is evident, that no micro pump on the market can meet all of these demands. A black box must be developed around the micro pump.

2.1 Dosing accuracy and back pressure independence

Micro diaphragm pumps are back pressure dependent, current state of the art micro pumps achieve a liquid back pressure of about 50...100 kPa and a air back pressure of about 10...25 kPa. To overcome these limitations, a silicon micro pump has been realised at the Fraunhofer EMFT with a very high compression ratio not known from other micro pumps on the market. With that, the dosing accuracy will be independent to the presence on gas bubble in the pump chamber, which is one of the main reason limiting dosing accuracy of state of the art micro pumps.



Fig. 2: New high pressure micro pump bottom side (left) with inlet and outlet ports and fluidic ports for safety valve, and top side (right) with the round piezo.

This pump (fig. 2) with a chip size of 7x7x1 mm³ can achieve a maximum back pressure with liquids of 600 kPa and an air back pressure of 90 kPa, both values are a factor of three above the state of the art.Both performance data ensure a nearly back pressure independent flow rate and a very



Fig. 3: Pump cube compared to a sugar cube. The system comprise a silicon micro pump chip, driver electronics together with micro controller, silicone gasket, fluidic carrier, and battery. The Pump cube is the smallest pump system worldwide.

good bubble tolerance, two preconditions for a practical dosing accuracy.

2.3 Small size

The silicon micro pump with a size of 7x7x1 mm3 is one of the smallest pump of the world. Together with a very small driver electronic a "pump cube" system was developed, with a total size of less than 1 cm³ including Battery and fluidic carrier.

2.4 Small energy consumption

The driver unit was based on a boost converter technology:



Fig. X: Boost converter.

The electrical driver unit was optimised, the energy consumption is between 40 mW and 500 mW, dependent on piezo capacitance, driving voltage and pump frequency. These systems are ideal for battery driven systems.



Fig. 4: Miniaturised driver unit: size 10mm x 11mm x 4mm, from +100V/-40V rect. @ 8nF load, up to +250 V/-100 V rect. @ 10nF load, max. 500Hz, input 3.3 to 5 VDC, power <40mW
@ 100Hz and +100V/-40V, efficiency factor 23 %, PC comm. RS232.

2.5 Particle resistance

Particles pumped into the micro pump by the pump itself can block valve flaps or actuation diaphragms, leading to a pump failure. Regularly, a hydrophilic filter with small pore size is needed. However, this filter will have a high bubble point, a large gas bubble can block the filter stopping the pump working.

In the micro pump community, this problem is under estimated, and can be a show stopper for micro pumps generally: micro pumps are vulnerable even to small particles. Even if the liquid is "clean" just one particle is enough to kill the micro pump. Every particle will travel through the bottleneck micro pump. For that, micro pumps need in any case a filter with a pore size of a few micros. But if they have that filter, a gas bubble will block that filter, and the micro pump stops pumping, too. The bubble point pressure Δp of a filter is defined as the pressure difference a gas bubble can pass the filter, and dependent on the pore size D of the filter (wetting angle Θ , surface tension σ):

$$\Delta p = \frac{4\sigma \,\cos\Theta}{D} \tag{1}$$

This problem was solved by a new patented filter without bubble point, which has no blocking pressure even if a large bubble is entering the filter.

liquid is passing through hydrophilic filter



bypass of air through hydrophobic filter

Fig. 5: bubble tolerant filter, which can not be blocked by gas bubbles by a hydrophobic gas bypass.

With that bubble tolerant filter, every particle is filtered, the liquid is passing through the hydrophilic filter, whereas the bubbles can bypass through the parallel hydrophobic filter without pressure drop.

2.6 Free flow protection

In many applications, especially medical application, "free flow" must be prevented, if the reservoir is pressurised, no flow through the pump is allowed.



Fig. 6: "free flow" problem of micro pumps with passive check valve: if the inlet reservoir is pressurized, the passive check valve will open even if the pump is off, and unwanted flow occures.

At Fraunhofer EMFT several solutions were developed and patented, a "normally double closed (DNC)" micro valve /2/, and a new safety valve as described below. Both valves are passive and self blocking, the over pressure at the inlet is closing the valve. Fig. 7 shows the concept of the safety valves:

within the silicon micro pump chip a safety valve channel with valve seat is realised during the KOH etching process steps. Next, a rubber diaphragm is mounted to the pump chip.



Fig. 7: safety valve concept: a rubber diaphragm is aligned to the silicon chip which prevents free flow.

Upon application an over pressure at the inlet, the rubber diaphragm is pressed to the valve seat in the chip closing the valve and avoiding free flow. The rubber diaphragm is pressure balanced until the region of the outlet hole, for that the micro pump can open the valve by the over pressure of the pump stroke. Fig. 8 shows measurement results, and a very good function of the safety valve:



Fig. 8: Test of the safety valve with an inlet pressure of p1 = p2 20 kPa, outlet pressure p3 = 0 kPa. The pump switched between ON and OFF state, with different frequencies. The safety valve closed reliable if the pump is OFF.

3 Conclusions

In this paper, methods for a reliable operation of micro dosing systems based on micro pumps are discussed. Bubble independent operation can be nearly achieved with a micro pump with high stiffness of the actuator unit. Bubble tolerant and bubble independent operation is realized by a very high compression ratio. Miniaturization of the packaging and the energy efficient pump driver electronics is the precondition for small size and battery operation. Micro pumps must be protected by particle filter, a bubble tolerant filter is needed to avoid a blockage of that filter by bubbles. Last but not least a free flow protection is needed especially for medical applications. A new safety valve integrated at the micro pump can avoid free flow in a reliable matter.

With that, integration of all of these components into a small and portable device opens the door to many new micro dosing systems.

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HARDWARE IMPLEMENTATION OF AN EARLIEST DEADLINE FIRST TASK SCHEDULING ALGORITHM

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Key words: Embedded systems, real-time, task scheduling, EDF, FPGA.

Abstract: Task scheduling in complex hard real-time systems produces interference during the normal operation of the application, prolongs the reaction times, reduces throughput, and makes temporal analysis of the system more difficult. A coprocessor performing functions of the operating system is proposed, in order to cope with this. The paper presents the implementation of an Earliest Deadline First (EDF) task-scheduling algorithm with hardware means (specifically with the FPGA device). This solution to a great deal eliminates the impact of the scheduling during the normal application execution. In addition, because it is implemented in hardware, it outperforms any software implementation. Two solutions are presented with different trade-offs regarding execution time and silicon consumption.

Aparaturna izvedba razvrščanja opravil po strategiji najbližjega skrajnega roka

Kjučne besede: Vgrajeni sistemi, realni čas, razvrščanje opravil, EDF, FPGA.

Izvleček: Razvrščanje opravil v kompleksnih sistemih, ki delujejo v strogem realnem času, vpliva na obnašanje med izvajanjem aplikacije, podaljšuje odzivne čase, zmanjšuje prehodnost in otežuje časovno analizo izvajanja opravil. Da bi se temu izognili, predlagamo ko-procesor, ki bi izvajal funkcije operacijskega sistema. V članku je opisana izvedba algoritma razvrščanja po strategiji EDF (po najbližjem skrajnem roku) z uporabo strojne opreme (natančneje na osnovi programirljivih vezij - FPGA). Ta rešitev v veliki meri eliminira vpliv razvrščanja med normalnim izvajanjem aplikacije. Poleg tega je zaradi diskretne aparaturne izvedbe hitrejše od katere koli programske. V članku sta predstavljeni dve rešitvi, ki ustrezata različnim kompromisom glede hitrosti izvajanja in porabe prostora na vezju.

1. Introduction

Embedded computer systems have become an important part of everyday life, and will have more and more influence in the future. They appear in industrial applications, cars, home appliances, entertainment electronics, etc. They are becoming increasingly ubiquitous, and we hardly notice them anymore. Because of such growth in importance, some other previously unobserved aspects of embedded systems are becoming more significant. An increasing number of embedded computer systems are being used in applications, where improper functionality may cause large financial losses or may even endanger human lives. Such systems need to be dependable and must react to events within strict time restrictions. As a state-of-the-art, proper construction of such systems is, as yet, more art than engineering, and the increasing complexities of such systems makes these things even worse (Ebert et al. (2009)).

This paper deals with real-time embedded systems. In such systems, the required functionality must be performed in a timely fashion; i.e. regardless of the situation in the system, certain operations must be completed within the predefined time interval. This can only be achieved with proper management of the tasks. Traditionally, this is performed by the operating system. However, proper management of tasks in an embedded system may be a complex and time-consuming procedure that interferes with the normal operation of the system, especially if it is performed on the same processor as the tasks are executed. Because of this, it would be of benefit if such a load could be reduced or eliminated altogether.

One solution is to employ a co-processor that can perform the functionality of the operating system in parallel to the application's execution. The co-processor only interacts with the application when its sequence of tasks needs to be rearranged. Such a solution also decreases the complexity of system design and the analysis of those temporal circumstances that may occur within the system. It also decreases the minimum reaction times and increases the throughput of the system. Nowadays, multi-core processor solutions are available and are becoming more and more popular within embedded systems. Therefore, any implementation where one of the processors' cores is dedicated solely to operating system operations is feasible.

There are two basic kinds of implementation using such a co-processor. Firstly, an additional standard (micro) processor can be used dedicated solely to performing the tasks of the operating system. However, because of the complexities of algorithms for real-time operating systems, it may perform poorly irrespective of its processing power. Although not discussed in this paper, in addition to task scheduling, the co-processor must also perform other functionalities of the operating systems (e.g. tasks synchronization, inter-task communication, etc.), which also influences their overall performances. Communication with the main processor must be synchronized with the co-processor's activities, which may additionally delay the reaction. Such solutions are well known and have been implemented for some time (Halang (1986), Stankovic (1991), Cooling (1993), and others).

The second solution is to employ hardware implementation that is dedicated to operating system functionalities. This approach has become feasible through advances in solid-state technology, especially FPGAs. It virtually eliminates any impact of the operating system during the normal application execution, for several reasons. Firstly, the operating system's functionality may be divided into independent parts, which are then implemented, in parallel, as separate processes on a single hardware device. Secondly, synchronization with the main processor can also be implemented asynchronously to other functionalities and, thus, introduce much less overhead. In addition, because it is implemented with hardware means, this approach outperforms any software implementation regarding speed. An "OS-on-a-chip" may be used with less powerful processors allowing cheaper and more power-efficient solutions. Operation of such a device can also be formally verified and certified for use at higher safety-integrity levels than the programmed implementation. Furthermore, such a device may serve additional purposes. For example, it can be used as an intelligent I/O device, it may implement communication layers in distributed control systems, etc. An example of this, in combination with software and hardware parts, and the middleware functionality, was studied and successfully implemented in the IFATIS project (IFATIS (2005)). Further improvements are expected using the new approach presented in the paper.

This paper focuses on the hardware implementation of one of the most important parts of an operating system, task scheduling. Nevertheless, this part has the most influence on any temporal behaviour of the systems. The hardware implementation of the algorithm is carried out using a Field-Programmable Gate Array (FPGA) device. However, for the production phase, ASIC or custom-built chips would be more cost-effective.

The first part of the paper introduces the tasks and task scheduling for hard real-time embedded systems. The second part describes the implementation of such algorithm based on the Earliest Deadline First (EDF) scheduling strategy. Two solutions are presented with different trade-offs regarding execution time and silicon consumption are presented.

2. Tasks and task scheduling

An embedded application usually consists of several computing processes or tasks. Typically, there are much more tasks than processing facilities to execute them, and some tasks are executed sequentially on a specific processing unit. In order to execute tasks effectively, a proper schedule (or arrangement) of tasks needs to be found that conforms to certain restrictions. This process is known as task scheduling. Task scheduling can be performed in advance (a priori), for simple and static applications. For example, in a so-called cyclic executive, a set of tasks is executed periodically. During each cycle, all active tasks are executed sequentially. It is in the hands of the developer to choose a period such that all tasks finish execution prior to the start of the next cycle. However, in dynamic systems where the task load frequently changes, this simple scheme is inadequate. A task may be dormant (inactive), ready for execution (active) or being executed on the processor. An active task may be temporarily suspended during execution due to the unavailability of certain system resources or because of the need for synchronizations with other tasks, etc. In this case, the schedules of the tasks must be planned dynamically.

Traditionally, some kind of priority is used to determine which task must be executed next. An active task with the highest priority is always executed first. If needed, tasks with lower priority may be temporarily suspended to allow the running of more important ones. However, those priority-based scheduling strategies are inadequate for hard real-time systems. In such systems, a started task must be finished prior to a certain predetermined deadline, regardless of the conditions in the system. Therefore, a schedule of tasks must be set-up in such a way that all tasks meet their deadlines. This is done by taking into account their execution times and other time-delaying factors in the system. If they exist, such a schedule is called 'feasible'. Several deadline-driven scheduling methods do exist. The so-called rate-monotonic scheduling strategy can be used for those multitasking systems where all tasks are executed periodically over a-priori known periods. Here the deadlines of tasks are matched with their periods and the tasks are then executed according to them: tasks with shorter periods are executed before those tasks with longer ones. Repetitive periods of activation are known in advance for each task. Therefore, these periods may be used as priorities, and can be employed with priority-based operating systems. In their widely-recognised publication (Liu et al. (1973)) Liu and Layland show that rate-monotonic strategy yields a feasible schedule if processor utilization is kept below a certain boundary (for instance, for large number of processors, the processor utilization should be below 70%). Another deadline-driven scheduling policy is Earliest-Deadline-First (EDF). It is more flexible than ratemonotonic strategy and can be used in real-case situations where both periodic and a-periodic tasks are present. EDF has also proven to be the best deadline-driven scheduling strategy for single processor systems regarding feasibility and optimality of system utilisation. Because of this, this scheduling strategy was chosen for our research.

2.1 EDF task scheduling

In EDF, the task with the shortest deadline must be executed first. In order to find it, the scheduler must srutinize the

list of ready tasks and find the task with the shortest deadline. This can be represented by a simple pseudo code:

```
min_task_index = 0
min_deadline = ∞
for i=1 to n do
    if taskinfo[i].deadline < min_deadline then
        min_deadline = taskinfo[i].deadline
        min_task_index = i
        end if
end for</pre>
```

The *taskinfo* array holds the information of all ready tasks in the system. Each element consists of a task identification number, worst-case execution time, deadline, etc. This procedure must be executed every time a new task becomes active (i.e. ready for execution), suspended or terminated. Termination or suspension of a task, other than that currently running, does not influence the schedule.

However, this is only part of the work that must be accomplished by the scheduler. Another matter is to prove that the schedule is feasible (i.e. that all active tasks will meet their deadlines). For the EDF, the schedule is feasible if the following equation is fulfilled for each active task:

$$a_k \circ \sum_{i=1}^k l_i, k = 1, ..., n$$
 (1)

This equation states that the sum of the remaining execution times I_i of all tasks T_i scheduled to run before, and including task T_k , added to the current time, must be less or equal to the absolute time of deadline a_k of task T_k . In other words, the cumulative workload to be performed prior and during execution of task T_k must be completed before its deadline. The tasks are sorted by their ascending deadlines. Again, the condition determined by the formula is static, and must be re-evaluated only when one or more of the tasks change their states.

This schedulability check can be converted into a form with a double nested loop, illustrated using the next pseudo code:

```
cumulative_finish_time = current_time
for i=1 to n do
    for j=i+1 to n do
        if taskinfo[j].deadline < taskinfo[i].deadline then
        swap(taskinfo[i],taskinfo[j])
        end if
        end for
        cumulative_finish_time = cumulative_finish_time+
        taskinfo[i].remaining_exec_time
        if cumulative_finish_time > taskinfo[i].deadline then
        raise deadline_violation_error
        end if
    end for
    for
        cumulative_finish_time > taskinfo[i].deadline then
        raise deadline_violation_error
    end if
    end for
    for
```

The first part of the outer-loop is used to sort the data according to the tasks' deadline. As a side effect, the algorithm also puts the task with the shortest deadline in the first place of the array. Therefore, searching for the task with shortest deadline can be combined with a feasibility check. In the second part of the outer-loop, feasibility is tested by first adding the remaining execution time of the current task to the cumulative execution time, and then comparing it to the task's deadline. Because the remaining execution times of separate tasks are represented as relative time intervals, the current execution time is added to the cumulative execution time at the beginning of the code in order to allow for comparison with the deadlines, which are represented as absolute times. It is presumed that the deadlines of the tasks are converted into an absolute form once they become active.

For simplicity, the test whether a task is active or not, is not shown in the code. Usually not all tasks in the system are active (ready to run) at the same time. Inactive tasks should not be considered in the scheduling. The comparison of tasks' deadlines and the feasibility check should only be done if both tasks are active. This can be achieved with additional checks at the beginnings of both loops.

As a drawback, the EDF algorithm described above requires $N^2/2$ iterations (for the N active tasks) which is more than, for example, with priority based task scheduling; in order to find the task with the highest priority, only N iterations are required.

2.2 Modification of the EDF algorithm for hardware implementation

In theory, the basic EDF scheduling algorithm can be easily translated into any hardware synthesis language (e.g. System C or HDL code). However, we found that ordinary in-memory sorting could be very inefficiently implemented in the hardware. Simple hardware circuits are optimal when operating Boolean and integer quantities, therefore, the entire task's information should be transformed into these two types. Furthermore, only simple operations can be usually implemented in the hardware. Complex operations would require several steps for the executing and consuming more hardware resources. Even some integer arithmetic operations (e.g., comparison and addition) would consume considerable amounts of silicon. Therefore, the goal is to minimize the complexity, and reduce the number of steps of the code. In the pseudo-code above, the deadline comparison in the inner-loop requires two read and two write operations in the table (if swap operation is optimized). The basic sort algorithm should be modified in order to reduce the read/write operations One possible modification is shown in the next pseudo code:

cumulative_finish_time = current_time for i=1 to n-1 do moved_data = taskinfo[i] min_data = moved_data min_index = i for j=i+1 to n do curr_data = taskinfo[j] if curr_data.deadline < min_data.deadline then min_data = curr_data min_index = j
end if
end for
taskinfo[min_index] = moved_data
taskinfo[i] = min_data
cumulative_finish_time = cumulative_finish_time+ min_
data.remaining_exec_time
if cumulative_finish_time > min_data.deadline then
raise deadline_violation_error
end if
end for

This code utilizes modified version of a so-called straight selection sorting. The role of the inner-loop is to find the task with the shortest deadline. When such a task is found, it is placed at the beginning of the table. During each iteration of the outer- loop, one element of the array is being sorted. The feasibility check remains the same as before.

Temporary variables such as *min_data*, *min_index*, etc., can be efficiently implemented in the hardware by means of registers. The whole algorithm is now executed as a sequence of simple assignment and arithmetic operations. In the inner-loop only one read operation remains (with an additional read and two write operations outside the loop). Furthermore, because the information needed for the EDF schedulability test is already in the *min_data* variable, an additional read operation can be avoided. The time and memory complexity of this version of the algorithm remains the same as before. However, the total execution time of the outer-loop's body is reduced significantly, and translation into the HDL language is much more efficient.

2.3 Parallelization of the algorithm

Further optimizations of the EDF scheduling algorithm and feasibility test can be achieved if some of the operations are performed in parallel. Obviously, this approach requires multiple processing resources. It cannot be implemented in software using a single processor. However, it can be easily implemented in hardware.

In our case, the first item to be optimized is the inner-loop. If we can eliminate the inner-loop altogether by executing all repeated steps as a single operation, the EDF algorithm may be executed in just N iterations (i.e., the time complexity is O(n)). However, there is data dependency between the loop iterations, e.g., the content of the min_data variable in one iteration of the loop depends on the values from the previous steps. With the given algorithm, the only available optimization technique we can employ is to execute different operation of the loop in pipeline fashion. The pipeline technique is a well-known approach to speed-up instruction execution within the microprocessors. Whilst one piece of information is being processed during one stage, other data element is being processed within another stage. The number of stages depends on the number of different operations to be executed sequentially. Because the speed of the pipeline depends on the slowest stage, it is preferable that the work is divided equally between different stages. Where there is no data dependency between two or more operations, they can be executed simultaneously. For example, in previous algorithm, the write operation and the feasibility check at the end of the outer-loop can be performed in parallel.

An example of such parallelization for 4 tasks is illustrated on Figure 1.

The inner-loop is divided into four stages: data read, comparison, EDF feasibility check, and data write. During comparison of one element of the table, another element can be read. In addition, the feasibility check can be performed at the same time with the write operation. In this way, we can significantly reduce the execution times. However, the time complexity of the algorithm remains the same.

Certain other kinds of sorting should be used for further improvement of the code. We could also eliminate in-memory sorting altogether. One way to do this is to use an auxiliary table where an ordered list of tasks is maintained. This list is incrementally built from data taken from the original taskinfo table; the tasks' data are taken from one table and placed at the proper place in the other one. The pseudo code for this approach would be:

```
for i=1 to n do
    curr_data = taskinfo[i]
    pos = i
    for j=1 to n-i do
    if tasklist[j].deadline>curr_data.deadline then
        pos = j
        break
    end if
    end for
    for j=n-i downto pos do
        tasklist[j+1]=tasklist[j]
    end for
    tasklist[pos] = curr_data
end for
```

The tasklist table is the auxiliary table previously mentioned. In it, only data relevant to the EDF algorithm is kept. One

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
READ	R0	R1	R2	R3			R1	R2	R3			R2	R3			R3		
COMPARE		C0	C1	C2	C3			C1	C2	C3			C2	C3			C3	
EDF						E					Е				Е			Е
WRITE						W					W				W			W

Fig. 1: Example of pipeline execution of EDF algorithm for four tasks.

element of the taskinfo table is taken at the beginning of the loop. Then, the proper place for this task is determined in the second table by finding the position of the first element with the later deadline. From this index on, we shift all elements of the list to the end of the structure. In this way, we prepare a place in which new data is put.

At first glance, the complexity of this algorithm is greater than the previous one. Indeed, if we implement this algorithm sequentially, more execution cycles probably would be required than before. On the other hand, in this code, both inner-loops only have simple bodies. The first loop has no data dependency in it and it can be easily parallelized by comparison of the current task's deadline with those deadlines already in the table. This can be done in parallel if a comparator is used with each element of the array. At first sight, the second loop has obvious data dependency between the two loop iterations. Some elements of the array are accessed and modified from two loop iterations. However, this part of the code is only the sequential program representation of a shift operation. In hardware architectures, shift registers and queues are frequently used where pieces of data are moved in a similar way. Therefore, the second loop can be implemented by linking the elements of the taskinfo table in serial fashion.

This approach also requires modification of the feasibility check. In comparison to previous scenarios, where data is considered to be in ordered fashion, it is now taken from the original table in random order. For the feasibility check, this would require repetitive summation of the remaining execution time according to (1). In order to avoid this, the attributes of the tasklist table have to be expanded with a new variable, which keeps a sum of the remaining execution times for all task prior to and including the current one. This attribute stands for the role of the cumulative finish time variable in previous cases. Every time new task information is put onto the list, its remaining execution time must then be added to all following elements on the list. Notably, these are the same elements as shifted before. In order to obtain the total remaining execution time for the current task, its value is summed with the value of the element before it. Because the deadlines are expressed in absolute form and the execution times are relative intervals, they must be properly converted. This can be done by adding absolute current time to the execution time of the first element on the list. Later on, this value will eventually propagate through all elements on the list.

The parallel version of the EDF algorithm may be summarized as a sequence of four steps, repeated for each active task in the system:

Step 1: Compare the deadlines of all elements on the list with the current one and mark elements with a greater deadline.

Step 2: Shift all marked elements to the end of the list by copying all the data. Update (set) the mark for the last element on the list to be included in the next step.

Step 3: Fill the gap with the current task's information. Add the remaining execution time of the current task to the cumulative execution time for all marked elements. If the first element on the list is updated, set its current cumulative execution time to the values of the current system time.

Step 4: Compare the cumulative execution times with the corresponding deadlines and mark all elements where the deadline would be violated.

An additional step that invalidates all elements on the list is also required. However, this step is done only once at the beginning of the process.

Each step has a fixed execution time, therefore in this way, the time complexity of the EDF algorithm becomes O(n). Further improvements are possible if some of the steps are executed in parallel. If we have the resources for fast comparison during actions 1 and 4, each first and the second pair of steps, can be executed in parallel.

3. Experimental hardware implementation of edf algorithm

Two hardware implementations of EDF scheduling algorithm were tested using a FPGA device. In the first experiment, the optimized version of the algorithm was translated into the HDL language by hand. The pipeline approach was used to speed-up the execution. In the second experiment, the version with the sorted list of tasks was implemented by using a digital schematic design. The basic elements of the design were taken from the existing components library. Xilinx's Spartan2E devices were used during the experiments (Xilinx (2009)). This is an entry-level FPGA device with lower operational frequencies and relatively smaller amounts of configurable logical blocks.

The *taskinfo* table was implemented using dedicated memory blocks (called BRAM), which can be found in all modern FPGA devices. BRAM consists of a small amount (several Kb) of memory elements, which can be configured to have differed bus sizes. Several BRAM block were used in parallel to achieve even wider bus sizes. In this way, it was possible to read or write all components of a single *taskinfo* element at the same time. BRAM blocks were also accessible from the experimental platform. There is no direct equivalent of the *for* loop in hardware. However, it is possible to design counters that generate memory addresses according to the code in the algorithm. The arithmetic operations were performed directly using the HDL code in the first case, and with dedicated comparison components in the second case.

The block diagram, when implementing the first version algorithm, is shown in Figure 2.

Deadline and execution times were kept in two dedicated RAM blocks. The loop-generator generates the values of the loop index variables, which are then converted into memory addresses by the *Read* module. *Compare* and



Fig. 2: Block diagram for first implementation of EDF algorithm.

EDF modules perform the comparison and EDF feasibility checks, respectively. The control block is used as an interface between the FPGA and the main processor. Using this block, the main processor starts the EDF scheduling execution. Control block synchronizes the execution of other blocks by properly setting several control signals. The results of the algorithm (index of the task with the shortest deadline and the error status) are also held here.

To allow parallel execution and pipeline implementation, each block is implemented as a set of processes in the HDL code. The HDL version of the loop-generator for loop variable *j* is:

```
- Loop counter j
process (rst,clk,running)
begin
if rst = '1' or running = '0' then
j <= "000000";
elsif rising_edge(clk) then
if j = itemcount1 then
j <= i + "000001";
else
j <= j + "000001";
end if;
end if;
end j;
end process;</pre>
```

The *itemcount1* variable is set to the number of elements in the table at the beginning. Later, it is decremented within every iteration of the main loop. This variable represents the number of elements that must be processed by the inner loop.

For discrete implementation of the EDF algorithm's second version, for each element in the task list, an appropriate digital logic has been implemented and is represented as a single component. Then several of such components were linked together to implement the task list. This is illustrated in Figure 3.



Fig. 3. Hardware implementation of ordered list of tasks' information

In each step, a single task is evaluated and put into the proper position on the list. The information of the current task is put on the common bus. *Cur_TID*, *Cur_DL*, *Cur_Extis* represents the index of the task, its deadline and its remaining execution time, respectively. Then, a series of control signals (not shown in the picture) are generated to execute different steps of the EDF algorithm for each cell, as described in the previous section. The outer-loop generator, the memory blocks and the control logic are not shown. These are similar to the first case.

A logic diagram for each task list element is shown in Figure 4.



Fig. 4. Logic diagram of the EDF evaluation cell

Each cell has two sets of inputs. One set is fed by the data of the current task and another is feed by data from the previous cell. Two input streams of data are merged into a single output stream to be used during the shift step. The second set of inputs of the first cell is connected to some constant values and to the current time counter, as shown in Figure 3. In this way, no extra logic is required for the first cell on the list. There is one set of outputs connected to the following cell and two logic signals that mark whether the content of the cell should be shifted (*DL_mark*) or if there is a deadline violation error (*Err_mark*).

Each element consists of three registers that contain different attributes of the task list. These registers are connected to the inputs through multiplexers to allow values to be filled-in, either from the common bus or from the previous cell. Each block is logically divided into three parts. The first (the upper) part tracks the index of the task that is in a particular place on the list. The second (middle) part is responsible for deadline comparison and for marking the cell for the shift operation. The third (lower) part of the cell calculates cumulative execution time and marks deadline violations.

During the first step of the algorithm, the comparator in the middle part of the cell is used to determine the elements with the later deadline (larger value). In the second step, the registers of the marked cells are shifted to the right and the current values are put into the gap. In the third step, the current execution time on the common bus is added to the cumulative remaining execution times of marked cells. This is implemented with dedicated addition components in the third part of the cell. In the last step, the cumulative execution times are compared (with yet another comparator) and any violations are signalled. By using both phases of the clock signal, we managed to reduce the execution time of the steps to two clock cycles of the FPGA device. Finally, the tasks are sorted in ascending fashion according to their deadlines. For the task identification, their IDs are associated with the task deadlines and sorted accordingly. The ID register of the first cell contains a task identification that must be executed next.

4. Results of the experiments

The first version of the algorithm, with pipeline execution optimization described at the beginning of the chapter, takes approximately 140 slices for its implementation. This number is independent of the number of tasks. In the second approach, each EDF evaluation cell requires approximately 30 slices of FPGA device. However, in this case the amount of silicon depends linearly on the number of tasks to be evaluated. For example, in the case of 32 tasks, approximately 950 slices are required – almost 7 times more than in the first case. The control logic and loop generator takes an additional 12 slices. This number only slightly increases if more tasks are evaluated. These results are in favour with the first solution if the amount of silicon resources is limited.

On the other hand, the execution time of the first algorithm for 32 tasks is about 600 basic clock cycles and only around 65 in the second one. The second approach is almost 10 times faster than the first one. Only if the number of tasks is small (less than three), the execution times of both solutions become roughly the same. Therefore, the second approach should be considered if hardware resources are not a problem.

5. Conclusion and future work

Current state-of-the-art technology allows for the hardware implementation of software algorithms, even for low-cost

embedded system solutions. Operating systems have well-defined and relatively limited sets of functionalities. Therefore, it is easy to imagine having an "OS-on-a-chip" solution that may be used in the same way as mathematical co-processors two decades ago or as graphical coprocessors are used today. They may even become a part of general processors in the future.

In our future work we will try to achieve the implementation of an EDF algorithm with fixed time execution independent of the number of task (i.e., we want to achieve the O(1) temporal complexity). This is possible if the outer loop is eliminated altogether. Thiscan be achieved if the taskinfo array is maintained as a sorted list continuously, instead of rebuilding it each time a new task becomes active. However, in this case, in addition to task activation, other task operations performed by the operating system must be considered. First, when a task ends its execution, it must be removed from the array. The tasks following it must be shifted towards the beginning of the array. In addition, if a task becomes suspended due to some synchronization mechanism, it must remain on the table but it must not be considered for the running on the processor. Furthermore, some counters for the remaining execution times of the tasks in the list must be updated periodically. All of this significantly increases the silicon consumption and the feasibility of the approach may be questionable.

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OPTICAL MODEL FOR THIN-FILM PHOTOVOLTAIC DEVICES WITH LARGE SURFACE TEXTURES AT THE FRONT SIDE

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Key words: Thin-film silicon solar cells, optical modelling, textured glass, ray tracing, transfer matrix formalism

Abstract: An optical model for simulation of thin-film photovoltaic devices with thick surface-textured front components is presented. The model is based on the combination of incoherent geometric optics and coherent wave optics analysis, which are employed separately to simulate light propagation through the front textured component and the bottom flat thin-film component of the device, respectively. The verified model is implemented into the optical simulator CROWM, which is employed to study the light-trapping potential of the front surface-textured protective glass in thin-film photovoltaic modules. The results show that the texturisation in the range of millimetres significantly improves the quantum efficiency of the PV module, which results in 14.3 % higher J_{sc} compared to the conventional module with flat protective glass.

Optični model za tankoplastne fotonapetostne strukture z velikimi površinskimi teksturami na sprednji strani

Kjučne besede: tankoplastne silicijeve sončne celice, optično modeliranje, teksturirano steklo, metoda sledenja žarkov, metoda prenosnih matrik

Izvleček: V članku je predstavljen optični model za simulacijo tankoplastnih sončnih celic in fotonapetostnih modulov z velikimi površinskimi teksturami na sprednji strani strukture. Model temelji na kombinaciji nekoherentne geometrijske optike in koherentne valovne optike. Prvo uporabljamo za simulacijo potovanja svetlobe skozi sprednjo teksturirano komponento strukture, drugo pa za simulacijo spodnje tankoplastne strukture. Verificirani optični model je implementiran v optičnem simulatorju CROWM ("<u>C</u>ombined <u>Ray Optics / W</u>ave Optics Numerical <u>M</u>odel"), s katerim preučujemo potencial teksturiranega zaščitnega stekla za izboljšanje svetlobnega ujetja v tankoplastnih fotonapetostnih modulih. Rezultati kažejo, da površinska teksturizacija sprednjega stekla v milimetrskem območju bistveno izboljšuje kvantni izkoristek modula, kar se odraža v 14.3 % višji kratkostični gostoti toka v primerjavi s konvencionalnim modulom z gladkim sprednjim steklom.

1. Introduction

Optical modelling and simulation of optoelectronic devices such as solar cells and photovoltaic modules (PV devices) presents a powerful tool for design and optimisation of the device structures and their optical performances /1/. Simulations allow efficient and inexpensive analysis of numerous factors which influence the performance and also offer a predictive power which can be used in the design of novel device concepts. Thin-film PV devices, which are the subject of this paper, are multilayer structures consisting of semi-transparent thin and thick layers /2/. The thickness of the thin layers (semiconductor layers, transparent conductive oxide (TCO) contacts etc.) is in the range of nanometres and micrometres, whereas the thickness of the front or back substrate is in the range of millimetres. The level of interference fringes observed in the measured wavelength-dependent reflection and transmission spectra of thin-film solar cells indicate that coherent light propagation takes place within the thin layers of the device, as opposed to incoherent propagation observed in the thick transparent substrates /3/. Further on, textured interfaces or nanoparticles are employed in the structures to scatter the light and thus increase the optical paths and the absorption of light in the thin layers /4, 5/. The lateral and vertical dimensions of the texture features can be either in the range of nanometres, as is typically the case at internal interfaces, or in the range of microns or even millimetres in the case

of surface-textured glass substrates /6/. Texturisation of solar cells introduces additional complexity that has to be taken into account in optical modelling and simulation of such structures.

Over the years, different optical models have been developed to combine coherent and incoherent propagation of light in thin and thick layers, respectively, and to tackle light scattering effects at nano-textured interfaces inside the solar cell structures /7-13/. However, most of these models cannot be easily applied to simulation of thin-film solar cells with thick surface-textured front components, such as glass substrates with large surface textures, due to several drawbacks. First, most of the models are designed primarily for one specific type of light propagation (coherent or incoherent) and don't allow for combination of both. Second, the limited dimensions of the simulation domain would make most of the models unfeasible for larger structures, such as thick glass layers. And third, the models are often limited to one dimension and don't allow an exact morphology of the surface texture to be specified.

In this paper, we present an optical model which combines light scattering at large textures (from a few microns to a few millimetres) located at the front surface of the PV device with coherent propagation and absorption of the scattered waves in the thin layers of the device. The model is based on the combination of incoherent two-dimensional ray tracing (geometric optics) /13/, which is employed to analyse the thick front substrate, and coherent one-dimensional transfer matrix formalism (wave optics) /14/, which is used for the bottom thin-film component of the device. The development of the model (i.e. the mathematical procedures and the physical background) will be described in detail in Section 2, and verification of the model with other verified optical simulators will be presented in the first part of Section 3. Finally, the developed optical model will be employed to simulate *a*-Si:H PV modules with thick protective glass at the front side, including large front surface textures. The beneficial effects of the texturisation with respect to an improved light trapping within the solar cells will be demonstrated.

2. Development of the optical model

The developed optical model is based on the combination of two fundamentally different numerical methods for the analysis of light propagation, which are applied separately to different parts of the simulated PV device (Fig. 1). The front part of the device (i.e. the incident medium and the thick surface-textured front layer) is treated by means of two-dimensional ray tracing /13/, where geometric optics approach is used to determine the angles and the intensities of light rays reflected or transmitted at the front textured interface. Within the thick front layer, completely incoherent propagation of light rays without any interference effects is assumed, which is justified since both the thickness of the front layer and the dimensions of the texture features are much larger (> 10 µm) than the effective wavelength of light. The surface texture is assumed to be periodic or quasi-periodic, in which case one period of the texture is included in the simulation while periodic boundary conditions are applied to the lateral borders. The bottom, thinfilm part of the PV device (i.e. the flat thin-film multilayer stack), on the other hand, is analysed by means of the transfer matrix formalism /14/. Transfer matrix formalism is a one-dimensional approach from wave optics which allows the analysis of fully coherent light propagation through the thin-film system under arbitrary incident angles, taking into account constructive and destructive interference of the forward and backward propagating waves. In the following sections, both approaches - geometric ray tracing





and thin-film wave optics – and their combination into one efficient optical model are described in detail.

2.1 Ray tracing

The incident illumination in the form of a plane wave is applied from the incident medium at the top border of the simulation domain, following an arbitrary incident angle. The full spectrum of the incident illumination is discretised into a number of monochromatic spectral components, and the simulation then takes place separately for each component (wavelength). Furthermore, the incident illumination is divided into the transverse-electric (TE) and the transverse-magnetic (TM) polarisation relative to the horizontal plane parallel to the interfaces in the thin-film stack. An arbitrary power ratio between the TE and TM polarised incident light can be chosen. All the calculations are performed separately for the TE and TM parts, and they are only combined at the end to produce the final results (see Section 2.3).

Simulation for a single monochromatic spectral component (wavelength λ) begins by dividing the total power of the component among a number of coherent parallel incident rays (separately for TE and TM), which are distributed evenly across the width of the simulation domain (in Fig. 1, only one incident ray is plotted schematically). The basic quantity that is used to define the light rays/waves propagating through the simulated structure is the electric field *E*, which is represented as a complex number (magnitude and phase). The electric fields corresponding to the incident rays are initialised according to Eq. 1,

$$E_{in} = \sqrt{\Re\left\{\frac{2\eta_0}{n_{in}}\right\}} \cdot P_{in} \tag{1}$$

Where P_{in} represents the time-averaged incident power per unit area of the ray, η_0 is the characteristic impedance in

vacuum ($\eta_0 = \sqrt{\mu_0/\epsilon_0}$), and n_{in} is the refractive index of the incident medium (this is typically air for simulation of terrestrial solar cells). In general, the refractive index is a complex value composed of the real part n_{re} and imaginary part k (also called the extinction coefficient), so that $n = n_{re} - j \cdot k$ (j is the imaginary unit). Zero phase is assumed for all the electric fields of the incident rays.

Once the electric fields are initialised at the top border of the simulation domain, each ray is propagating through the incident medium in a straight line following the propagation angle q_{in} until it either (i) impinges upon the textured surface of the thick front layer of the device or (ii) reaches one of the lateral borders of the simulation domain, in which case it simply reappears at the opposite border according to the periodic boundary condition. In the first case, the magnitude and the phase of the electric fields are first corrected according to Eq. 2, where λ represents the wavelength (in vacuum) of the analysed spectral component and *d* is the distance that the ray travelled through the incident medium until reaching the interface point.

$$E = E_{in} \cdot \exp\left(\frac{-i \cdot 2\pi \cdot n_{in} \cdot d}{\lambda}\right)$$
(2)

To determine the reflected and the transmitted components of the electric field from the textured surface, the incident angle θ_{in} , the angle of reflection θ_o , and the angle of refraction θ'_1 are first calculated. These are all relative angles with respect to the local inclination of the texture at the point where the ray impinges upon the surface. While the relative angle of the reflected ray is the same as the incident angle $(\theta'_0 = \theta'_{in})$, the angle of the refracted (transmitted) ray θ'_1 is defined according to Snell's law, as shown in Eq. 3 / 15/,

$$n_{in} \cdot \sin \theta'_{in} = n_1 \cdot \sin \theta'_1 \tag{3}$$

Where n_1 represents the complex refractive index of the thick front layer. In general, the calculated angle θ'_1 is also a complex value, and thus only the real part is taken to define the propagating angle of the transmitted ray. The Fresnel coefficients which determine the reflectance and the transmittance of the electric fields for the TE and TM polarised rays are then calculated according to Eq. 4 / 15/.

$$r^{TE} = \frac{n_{in} \cdot \cos\theta'_{in} - n_{1} \cdot \cos\theta'_{1}}{n_{in} \cdot \cos\theta'_{in} + n_{1} \cdot \cos\theta'_{1}}$$

$$t^{TE} = 1 + r^{TE} = \frac{2 \cdot n_{in} \cdot \cos\theta'_{in}}{n_{in} \cdot \cos\theta'_{in} + n_{1} \cdot \cos\theta'_{1}}$$

$$r^{TM} = \frac{n_{in} \cdot \cos\theta'_{1} - n_{1} \cdot \cos\theta'_{in}}{n_{in} \cdot \cos\theta'_{1} + n_{1} \cdot \cos\theta'_{in}}$$

$$t^{TM} = (1 + r^{TM}) \cdot \frac{\cos\theta'_{in}}{\cos\theta'_{1}} = \frac{2 \cdot n_{in} \cdot \cos\theta'_{in}}{n_{in} \cdot \cos\theta'_{1} + n_{1} \cdot \cos\theta'_{in}}$$
(4)

The reflected and the transmitted rays are then propagating further through the structure following a straight trajectory defined by the new propagating angles. The electric fields of the rays are obeying Eq. 2, where E_{in} and n_{in} are replaced with r. E and n_{in} (reflected ray) or $t \cdot E$ and n_1 (transmitted ray). This propagation takes place until one of the following happens: (i) the ray once again impinges upon the textured interface, in which case the above procedure (Eq. 3 - 4) is repeated, (ii) the ray reaches the top border of the simulation domain and thus escapes out of the structure, contributing to the total reflectance, or (iii) the ray reaches the bottom border of the thick front laver and thus enters the bottom thin-film component of the device. In the latter case, the outgoing ray represents the incident illumination for the bottom multilayer stack which is treated by means of the transfer matrix formalism.

2.2 Transfer matrix formalism

The transfer matrix formalism is a widely established onedimensional method for simulating the propagation of electromagnetic waves through a thin-film multilayer stack with flat parallel interfaces /14/. The method is based on the distribution of the wave propagating through the medium under an arbitrary angle into two components – the transverse component which is traveling perpendicular to the flat interfaces, and the parallel component traveling in parallel along the interfaces. The method then focuses on the propagation of the transverse wave components, since only these waves are able to interact constructively or destructively with each other, whereas the information about the full wave (transverse plus parallel) is retained within the propagating angles.

The incident waves for the bottom thin-film component of the simulated device are generated from the downward-traveling rays coming from the top component. The transition takes place just before the interface between the thick front layer (layer 1 in Fig. 1) and the first thin layer in the thin-film stack (layer 2 in Fig. 1). The transverse electric fields of the incident waves are thus calculated from the electric fields of the outgoing rays according to Eq. 5, taking into account the propagating angle q_1 .

$$E_{T, in}^{TE} = E^{TE}$$

$$E_{T, in}^{TM} = E^{TM} \cdot \cos \theta \qquad (5)$$

Assuming that there is a total of *N*-2 thin layers in the multilayer stack, we can calculate the complex propagation angle θ_i , the phase thickness δ_i , and the transverse impedance $\eta_{\tau,i}$ for each layer in the stack (*i*) according to Eq. 6 – 8 / 15/, where d_i represents the thickness of the layer. Furthermore, for each interface (*i*) in the thin-film multilayer stack, we can determine the transverse Fresnel coefficients given by Eq. 9. The nomenclature is chosen so that the *i*-th interface is located between the *i*-th and the (*i*+1)-th layer.

$$\theta_i = \sin^{-1} \left(\frac{n_1}{n_i} \cdot \sin \theta_1 \right) \qquad i = 2, 3, \dots, N$$
(6)

$$\delta_{i} = \frac{2\pi \cdot n_{i} \cdot d_{i} \cdot \cos \theta_{i}}{\lambda} \qquad i = 2, 3, ..., N - 1$$

$$TE \qquad \eta_{0} \qquad (7)$$

$$\eta_{T,i}^{TB} = \frac{1}{n_i \cdot \cos \theta_i} \qquad i = 1, 2, ..., N$$
$$\eta_{T,i}^{TM} = \frac{\eta_0 \cdot \cos \theta_i}{n_i} \qquad i = 1, 2, ..., N$$
$$(8)$$

$$r_{T,i}^{TN} = \frac{1}{n_i \cdot \cos\theta_i + n_{i+1} \cdot \cos\theta_{i+1}}$$

$$t_{T,i}^{TE} = 1 + r_{T,i}^{TE} = \frac{2 \cdot n_i \cdot \cos\theta_i}{n_i \cdot \cos\theta_i + n_{i+1} \cdot \cos\theta_i}$$

$$i = 1, 2, ..., N-1$$

$$r_{T,i}^{TM} = \frac{n_i \cdot \cos\theta_{i+1} - n_{i+1} \cdot \cos\theta_i}{n_i \cdot \cos\theta_{i+1} + n_{i+1} \cdot \cos\theta_i}$$

$$t_{T,i}^{TM} = 1 + r_{T,i}^{TM} = \frac{2 \cdot n_i \cdot \cos\theta_{i+1}}{n_i \cdot \cos\theta_{i+1} + n_{i+1} \cdot \cos\theta_i}$$
(9)

The simulation of wave propagation through the thin-film stack consists of two steps. First, the reflected and the transmitted fields of the whole stack are calculated by applying the matching and the propagation matrices of the interfaces and the layers, respectively. The matching matrices M give the relation between the forward and the backward propagating transverse electric fields at each side of an interface (Eq. 10), whereas the propagating through P define how the fields are affected by propagating through

a layer (Eq. 11), where indices *a* and *b* stand for the top and bottom border of the layer.

$$\begin{bmatrix} E_{T,i}^{+} \\ E_{T,i}^{-} \end{bmatrix} = \frac{1}{t_{T,i}} \begin{bmatrix} 1 & r_{T,i} \\ r_{T,i} & 1 \end{bmatrix} \cdot \begin{bmatrix} E_{T,i+1}^{+} \\ E_{T,i+1}^{-} \end{bmatrix} = \begin{bmatrix} M_i \end{bmatrix} \cdot \begin{bmatrix} E_{T,i+1}^{+} \\ E_{T,i+1}^{-} \end{bmatrix} = \begin{bmatrix} e_{T,i+1}^{-} & (10) \\ 0 & e_{T,ia} \end{bmatrix} = \begin{bmatrix} e_{T,ia} \\ e_{T,ia} \end{bmatrix} = \begin{bmatrix} e_{T,ia} \\ 0 & e_{T,ia} \end{bmatrix} \cdot \begin{bmatrix} E_{T,ib}^{+} \\ E_{T,ib}^{-} \end{bmatrix} = \begin{bmatrix} P_i \end{bmatrix} \cdot \begin{bmatrix} E_{T,ib}^{+} \\ E_{T,ib}^{-} \end{bmatrix}$$
(11)

The reflected and the transmitted fields of the stack are obtained by multiplying the matrices from the incident medium (thick front layer) to the medium in transmission, as shown in Eq. 12:

$$\begin{bmatrix} E_{T, in} \\ E_{T, reflected} \end{bmatrix} = \begin{bmatrix} M_1 \end{bmatrix} \cdot \begin{bmatrix} P_2 \end{bmatrix} \cdot \begin{bmatrix} M_2 \end{bmatrix} \cdot \dots \cdot \begin{bmatrix} P_{N-1} \end{bmatrix} \cdot \begin{bmatrix} M_{N-1} \end{bmatrix} \cdot \begin{bmatrix} E_{T, transmitted} \\ 0 \end{bmatrix}$$
(12)

In the second step, the total transverse electric and magnetic fields are calculated at each interface throughout the device. This is important to determine the absorptions within the individual layers of the thin-film stack. The fields at the first interface are calculated from the incident and the reflected electric fields according to Eq. 13, and then the fields at the following interfaces are determined by applying the propagation matrix in the recursions shown in Eq. 14.

$$\begin{bmatrix} E_{T,1} \\ H_{T,1} \end{bmatrix} = \begin{bmatrix} E_{T,in} + E_{T,reflected} \\ \frac{1}{\eta_1} (E_{T,in} - E_{T,reflected}) \end{bmatrix}$$
(13)
$$\begin{bmatrix} E_{T,i} \\ H_{T,i} \end{bmatrix} = \begin{bmatrix} \cos(\delta_i) & -j\eta_i \sin(\delta_i) \\ -j\frac{1}{\eta_i} \sin(\delta_i) & \cos(\delta_i) \end{bmatrix} \cdot \begin{bmatrix} E_{T,i-1} \\ H_{T,i-1} \end{bmatrix}$$

$$i = 2, 3, \dots, N-1$$
(14)

Finally, the time-averaged power per unit area entering the *i*-th layer as well as the power lost within the layer can be determined from the Poynting vector according to Eq. 15.

$$P_{i} = \frac{1}{2} \Re \{ E_{T, i-1} \cdot H_{T, i-1}^{*} \} \qquad i = 2, 3, \dots, N$$
$$A_{i} = P_{i} - P_{i+1} \qquad \qquad i = 2, 3, \dots, N-1$$
(15)

The summation of the power losses calculated for each ray entering the thin-film multilayer stack relative to the total incident power gives the total absorptance within each layer of the simulated optoelectronic device, whereas the power of the transmitted waves is contributing to the total transmittance.

2.3 Combination of ray tracing and transfer matrix formalism

Both optical models, ray tracing in the top part (layers 0 and 1) and transfer matrix formalism in the bottom part of the structure (layers 2 - N), are then coupled iteratively at the interface between the thick front layer and the bottom multilayer stack. Rays reaching the interface from the front

layer are injected as waves into the thin-film stack, whereas the waves coming back from the thin-film stack re-enter the front layer as backward-traveling rays. Simulation concludes once almost all of the light (according to some pre-defined threshold) has either escaped out of the structure (contributing to the total reflectance or the total transmittance) or has been absorbed in the device (contributing to the absorptance within the layers). The reflectance, the transmittance, and the absorptance are defined as the ratios of the reflected, transmitted and absorbed power relative to the total incident power, respectively, as defined in Eq. 16.

$$R_{tot} = \frac{P_R}{P_{in}} \qquad T_{tot} = \frac{P_T}{P_{in}} \qquad A = \frac{P_A}{P_{in}}$$
(16)

The primary input parameters of the developed optical model are the geometry and the physical properties of the simulated device, in particular (i) the description of the front surface texture, (ii) the layer thicknesses, (iii) the wavelength-dependent complex refractive indices of the materials, and (iv) the lateral boundaries (period) of the simulation domain, and the properties of the incident illumination, in particular (i) the propagation angle q_{in} , (ii) the spectral (wavelength) range, (iii) the total time-averaged power per unit area P_{in} for each spectral component, and (iv) the polarisation of light (TE and TM components with respect to the lateral plane of the device structure). The primary output parameters are (i) the total reflectance, (ii) the total transmittance of the device, and (iii) the absorptance within the individual layers of the structure.

The combined optical model was implemented in a computer simulator entitled CROWM (Combined Ray Optics / Wave Optics Numerical Model), which runs on a personal computer and allows for many advanced features primarily related to automatic optimisation of PV devices with respect to the desired output characteristics.

3. Simulation results

To demonstrate the applicability of the CROWM simulator based on the developed combined optical model to the analysis of thin-film PV devices, thin-film amorphous silicon (*a*-Si:H) solar cells encapsulated in PV modules with flat and textured front glass surfaces were simulated. The basic solar cell structure without the front component (encapsulation) which was used in all the simulations is constructed as follows: front SnO_2 :In (ITO) transparent conductive oxide (TCO) (70 nm), *p*-a-SiC:H layer (10 nm), *i*-a-Si:H absorber (250 nm), *n*-a-Si:H layer (20 nm), ZnO TCO (80 nm), Ag (300 nm)/substrate. The cell is in the so-called substrate configuration with the non-transparent substrate located at the back side. In all the simulations, realistic refractive indices of all the layers comprising the solar cell were employed /12/.

3.1 Verification of the simulator

To verify the CROWM simulator, the simulation results were compared to the results obtained by other verified optical

simulators for the analysis of thin-film PV devices. Besides the accuracy of the results, the speed of the simulation which represents an important indicator for efficient simulation and optimisation of the analysed structures was also investigated and compared between the models, using a high-end personal computer for all the simulations.

A perfectly flat *a*-Si:H solar cell with 1 mm thick glass layer at the front side (see inset in Fig. 2) was simulated by means of the CROWM and Sun*Shine* optical simulators /7/. The Sun*Shine* is a verified and well-established onedimensional semi-coherent optical simulator based on the scalar scattering theory, applicable to nano-textured interfaces. The external quantum efficiency (*QE*) of the solar cell simulated by both optical models in the wavelength range of 350 – 800 nm is shown in Fig. 2. The *QE* was calculated as the absorptance in the *i*-*a*-Si:H layer, assuming ideal extraction of the charge carriers /7/. It can be observed that identical results are obtained in both cases (curves are overlapping). The simulation times are also similar for both optical models and result in less than 20 seconds.



Fig. 2: Comparison of the quantum efficiencies simulated by means of the CROWM (full line) and SunShine optical simulators (dotted line with symbols) for the a-Si:H solar cell with flat front component (inset).

An a-Si:H solar cell with surface-textured glass layer at the front side was simulated by means of the CROWM and FEMOS-2D optical simulators /8/. FEMOS-2D is a verified fully-coherent two-dimensional simulator based on rigorous solving of electromagnetic wave equations using the finite element method (FEM). However, since FEMOS-2D was not designed for simulation of layers thicker than 10 µm, the dimensions of the front glass were scaled down to comply with this limitation. Thus, a 10 µm thick glass layer with a periodic triangular surface texture with the period $P = 10 \,\mu m$ and amplitude $h = 3 \mu m$ was employed in the simulations (see inset in Fig. 3). The QE results obtained by both simulators are shown in Fig. 3. Good agreement between the results can generally be observed, although slightly lower values are obtained by the FEMOS-2D simulator. These discrepancies can mostly be attributed to the relatively coarse non-adaptive triangular mesh used in FEMOS-2D (10 nm element size), which was required due to the relatively large simulation domain. Despite the coarser grid, however, the FEMOS-2D simulation lasted for more than one day, whereas the simulation by the developed CROWM simulator was completed in less than half an hour (time ratio of more than 1:50). Therefore, CROWM shows great potential for efficient simulation and optimisation of solar cells with thick surface-textured front components with large textures, which can become unwieldy for the conventional numerical methods such as FEM.



Fig. 3: Comparison of the quantum efficiencies simulated by means of the CROWM (full line) and FEMOS-2D optical simulators (dotted line with symbols) for the a-Si:H solar cell with surface-textured front component (inset).

3.2 Simulation of thin-film *a*-Si:H PV devices with thick textured protective glass

When the solar cells are encapsulated in PV modules, they are typically covered with about 100 µm of ethylene-vinyl acetate (EVA) foil, serving as an air-tight seal, and 4 mm of flat protective glass /1/. From the optical point of view, this additional component at the front side of the solar cell represents an optical barrier for the light entering the structure. Despite the better refractive index grading which is assured in this system (the refractive indices of glass and EVA are between those of air and ITO), incoherent properties of the thick glass and EVA foil do not lead to improved, but rather worse anti-reflecting properties compared to the initial solar cell structure. Simulations with the developed optical model show that the initial non-encapsulated a-Si:H solar cell illuminated with the standard AM1.5 solar spectrum exhibits the short-circuit current density J_{sc} = 12.43 mA/cm². After encapsulation, however, the additional reflections at the air/glass and EVA/TCO interfaces as well as the parasitic absorption within glass and EVA foil reduce $J_{\rm sc}$ to 11.51 mA/cm², which is a 7.4 % decrease compared to the non-encapsulated solar cell.

To improve the performance of thin-film solar cells, light trapping within the thin absorber layers of the device needs

to be assured. Improved light trapping in state-of-the-art a-Si:H solar cells is typically achieved by nano-textured internal interfaces, which introduce efficient scattering of the light propagating through the device /4/. Besides the internal interfaces, however, light scattering can also be achieved by the front protective glass. For this purpose, texturisation in form of spikes or grooves needs to be realised for example on the surface of the protective glass sheet /6/. This has two effects for the incident light rays impinging perpendicularly upon the textured surface. First, the rays transmitted through the air/glass interface are refracted into larger incident angles, which results in prolonged optical paths through the absorber layers of the cell and thus an increased $J_{\rm sc}$. And second, the rays reflected from the textured air/glass interface have a chance to impinge upon the interface and enter the device once more, which results in a decreased total reflectance from the solar module.

To demonstrate the light-trapping potential of the front protective glass in solar modules, flat *a*-Si:H solar cells covered with 100 μ m of EVA foil and 4 mm of flat and



Fig. 4: Structure of the a-Si:H solar cell encapsulated by 100 μm thick film of EVA foil and 4 mm thick surface-textured glass (a). The profile of the surface texture of the glass sheet is also shown (b).

surface-textured glass are simulated by means of the CROWM simulator. The refractive indices of EVA and glass are assumed to be the same in these simulations, and thus the reflection/refraction effects at the glass/EVA interface can be neglected. In the case of texturing, quasi random triangular one-dimensional texturisation with the period of 2 mm and peak-to-peak amplitude of 1 mm is applied to the top of the front glass, as shown in Fig. 4a. A more detailed plot of the textured surface of the glass sheet is presented in Fig. 4b.

The simulated trajectories of ray propagation through the surface-textured glass prior to reaching the thin-film *a*-Si:H solar cell are plotted in Fig. 5a. The rays impinging perpendicularly upon the textured surface (thick vertical lines at



Fig. 5: Ray propagation through the surface-textured glass (a) and angular distribution of the transmitted ray power at the interface with the front TCO of the solar cell (b).

the top of the figure) are refracted into large propagating angles, and multiple reflection/refraction events can also be observed, leading to lower reflectance. Simulations show that in the wavelength range of 350 – 900 nm, only 0.4 % of the total incident power is reflected by the textured air/glass interface, whereas in the case of flat glass, this value is more than ten times larger (4.4 %). The angular distribution of the transmitted ray power at the bottom border (EVA/TCO) of the front protective layer is presented in Fig. 5b. The figure indicates that the majority of the transmitted ray power is impinging upon the underlying solar cell with incident angles larger than 20 degrees, which will result in longer effective optical paths through the thin absorber layers and thus an increased efficiency of the solar cell.

The simulated quantum efficiencies of thin-film a-Si:H solar cells encapsulated with flat and surface-textured glass are presented in Fig. 6. A substantial increase in QE over the entire wavelength range can be observed for the surfacetextured module, which can be attributed directly to the enhanced light trapping achieved by the texturisation of glass. Simulations show that J_{sc} = 13.16 mA/cm² can be achieved in this case, which is 14.3 % higher than $J_{\rm sc}$ of the flat module (11.51 mA/cm²), and 5.9 % higher than J_{sc} of the non-encapsulated cell (12.43 mA/cm²). These results indicate that surface texturisation of the protective glass not only compensates for the negative effects of encapsulation, but further improves the short-circuit current density of the cell and thus the efficiency of the solar module. The challenge remains, however, to further optimise the morphology of the surface texturisation in order to achieve the highest possible efficiency of the photovoltaic device and to test the effect also for solar cells with nano-textured internal interfaces.



Fig. 6: Simulated quantum efficiency of thin-film a-Si:H solar cell encapsulated with flat (full line) and surface-textured glass (dashed line). CROWM simulator was used in both simulations.

4. Conclusions

An optical model based on the combination of twodimensional ray tracing and one-dimensional transfer matrix formalism was developed and applied to simulation of thin-film PV devices with thick surface-textured components at the front side. The model was implemented in the CROWM (Combined Ray Optics / Wave Optics Numerical Model) optical simulator. CROWM was verified by means of two established optical simulators based on the scalar scattering theory and the finite element method. In the case of cells with thick surface-textured front components, CROWM shows the potential to greatly reduce the simulation times and thus allows for more efficient analysis of the investigated structures. By means of the developed optical model, a-Si:H solar cells with flat interfaces encapsulated with thick flat and surface-textured glass were simulated. The results show that surface-textured protective glass improves light trapping within the thin absorber layers of the solar cell and thus significantly boosts the short-circuit current of the photovoltaic device.

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COMPENSATION AND SIGNAL CONDITIONING OF CAPACITIVE PRESSURE SENSORS

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Key words: digital temperature compensation, Chisholm approximation, Padé approximation, capacitance to digital converter.

Abstract: Implementation of a novel digital temperature compensation method, developed for piezoresistive pressure sensors, to the field of capacitive sensors is presented. Possibilities for the compensation of sensor parameters such as sensor nonlinearity and temperature sensitivity are analyzed. In order to achieve effective compensation and linearization, different approaches to digital descriptions of sensor characteristic are investigated and reported, such as two-dimensional rational polynomial description and Chisholm approximants. Results of sensor response are compared against reference pressure source and most effective digital temperature compensation is proposed.

Kompenzacija in obdelava signalov kapacitivnih senzorjev tlaka

Kjučne besede: digitalna temperaturna kompenzacija, Chisholm-ova aproksimacija, Padé-jeva aproksimacija, kapacitivno-digitalni pretvornik

Izvleček: V prispevku je predstavljene aplikacija metod digitalnih temperaturnih kompenzacij s področja piezorezistivnih senzorjev tlaka na področje kapacitivnih senzorjev tlaka. Analizirane so možnosti kompenzacije senzorskih parametrov kot sta nelinearnost in temperaturna občutljivost. Opisani so različni pristopi k digitalnemu opisu senzorske karakteristike, dvodimenzionalna polinomska aproksimacija in Chisholmovi aproksimanti. Rezultati kompenziranega senzorskega odziva so primerjani z referenčnimi meritvami tlaka. Na osnovi izmerjenih rezultatov je predlagana najbolj učinkovita metoda digitalne temperaturne kompenzacije kapacitivnih senzorjev tlaka.

1. Introduction

Sensors that exhibit a change in electrical capacitance as a response to a change in physical stimulus represent an attractive approach for use in modern sensor systems due to their extensive range of applications such as humidity, pressure, position sensors etc. Their broader range of applications include biomedical, touch & non-touch switch technology, proximity sensing, fingerprinting, automotive applications, robotics, materials property, and applications in motion sensors. This versatile sensor category offers higher precision and robustness, simpler construction and lower power consumption than resistive-based alternatives. However, they traditionally require more complex interfacing circuits, which represented a major disadvantage in the past. In a capacitive sensor, the physical parameter being measured by varying one or more of the quantities in the basic equation of capacitance

$$C = \varepsilon \frac{A}{d} \tag{1}$$

where ε is the permittivity of the dielectric, A is the overlap area of the capacitor plates, and d is the distance between the plates. For example, humidity sensors typically work by varying the permittivity ε , pressure sensors by varying distance d and position sensors by varying area A or distance d. Measurement of the sensor capacitance is generally achieved by applying an excitation source to the capacitor electrodes which is used to turn variance in capacitance into a variance in voltage, current, frequency or pulse width variation. Translation from voltage or current to a digital word requires an additional analog to digital converter (ADC).

The expected variance in capacitance is generally in the order of several pF or less. In many cases the stimulus capacitance change is much smaller than the parasitic capacitances present in the measuring circuit, hence representing a difficult interfacing task. However, a modification of conventional sigma-delta analog to digital converter architecture has been identified as a suitable basis for monolithic Capacitance to Digital Converter (CDC) /1/. Circuit itself is parasitic insensitive, and can be configured to work with both floating (access to both sensor terminals) and grounded configuration sensors (one terminal grounded).

Precision capacitive sensor interface products are based on a well established sigma-delta ($\Sigma\Delta$) conversion technology. Converters utilizing $\Sigma\Delta$ principle offer excellent linearity and resolution and are appropriate for most sensor interfacing applications. A typical $\Sigma\Delta$ converter ADC consists of switched-capacitor modulator followed by a digital filter. The modulator operation is based on balancing, over time, an unknown charge with a known reference charge of variable polarity /1, 2/.

Charge from reference terminal and input terminal are summed in an integrator. The integrator is inside a feedback loop, whose action is to control the polarity of the reference charge so that the integrator output averages to zero. This occurs when the magnitude of the average reference charge is equal over time to the input charge, hence the name - charge balancing converter. The reference charge is derived by charging a known capacitor to a known (reference) voltage. The polarity of reference voltage is varied. In a conventional voltage input $\Sigma\Delta$ converter, the unknown charge is derived from charging a fixed capacitor to an unknown input voltage, while in the capacitance to digital converter (CDC) realization, the voltage is fixed and the capacitor is variable. Such arrangement provides the high precision and accuracy that are typical for $\Sigma\Delta$ ADCs /3,4/. Modern implementations enable measurement of capacitances in atto Farad (aF) range /4, 5/, with effective noise resolution of 21 bits and corresponding resolution down to 4 aF. They offer measurements of common-mode capacitance up to 17 pF on 4 pF range with 4 fF measurement accuracy. These implementations offer complete sensor solutions, however their application is limited to indication of temperature and humidity dependence problem /6/ of capacitive sensors, while not offering an effective implementation for compensation of these unwanted quantities. In the following work an effective method of temperature compensation of capacitive pressure sensors will be presented.

2. Setup and measurements

The layout of designed capacitive sensor measurement system is depicted in Figure 1. Capacitive sensor with the CDC AD7746 is shown leftmost. The sensor is connected via interface module to the I^2C - USB converter, which is used to interface the sensor to the host PC.



Fig. 1: General layout of the capacitive sensor evaluation module.

A dedicated electronic interface module was designed. This module enables data transmission and control of CDC AD7746. The module itself is based on a CY8C24794 Programmable System on Chip (PSoC) circuit. The hardware is used to directly map the CDC to the controlling PC. Designed PC software performs the functions of CDC status and data reading. In fact, the controlling software implements all functions of AD7746: from capacitance channel setup to the temperature sensor channel setup as well as channel excitation, common mode capacitance setting, offset and gain of capacitance measurement channel.

Measurement range optimization was performed in order to get maximal span of CDC measurement range. Measured device, the LTCC capacitive sensor /7/, exhibits negative slope of sensor characteristic. Therefore, the measurement range optimization must be performed at maximal pressure readout with minimal pressure applied and vice versa.

This indicates that the offset compensation must be performed before the gain compensation. Sensor offset response is compensated by setting AD7746 registers CAPDACA and CAPOFFSET. The register value CAPDACA value affects coarse setting of offset response and the CAPOFFSET affects fine setting of sensor response. The procedure of offset setting is comprised of coarse and fine offset setting. Because of negative sensor characteristic slope, the fine offset value is initially set at maximum and the coarse value is altered from its initial zero value in such manner, that the raw sensor readout maintains its maximal value. The setting of CAPDACA register is performed by successive approximation approach, starting at MSB of CAPDACA register. The subsequent bits are tested against raw sensor output. If the sensor output exceeds the maximal sensor readout (FFFF₁₆) when corresponding bit is set to 1, then the bit is set to zero and the algorithm advances towards lower bits. After the coarse register was set, the CAPOFFSET register is processed in a similar manner. The result of this algorithm is a maximal sensor response value at applied offset pressure.

After successful optimization of offset value, the gain parameter is set in a similar manner. Minimal sensor response is set with alteration of CAPGAIN register, which actually changes the clock rate of front-end of CDC. The procedure starts with minimal setting of CAPGAIN register. The bits of CAPGAIN register are tested according to described successive approximation algorithm, just the bit-testing criteria is now minimal CDC readout. The result of this algorithm is minimal sensor response at maximal applied pressure. Initial measurements were performed at "Jožef Stefan Institute" /7/. The aim of these measurements was the determination of optimal settings of AD7746 and the tested LTCC sensor. Results of these measurements are depicted in Figure 2. Figure 2 shows the results of sensor characteristic in up and down scan of pressure range. Tested sensor exhibited practically no hysteresis, but the deviation form ideal straight line indicated the necessity for sensor characteristic linearization. The measurements were performed at a room temperature.

Measurements were repeated in HYB d.o.o., Šentjernej. This time, the scan was performed at three different temperatures. Sensor with interface electronic circuit were placed in the temperature chamber and measurement of raw response value was performed at three different temperatures. As the aimed temperature range was set



Fig. 2: Initial pressure sensor measurements.

at 0 °C ... 70 °C, the temperature calibration points were selected at 0 °C, 35 °C and 70 °C. The measurements have demonstrated the susceptibility of initial electronic circuit design to electromagnetic interference. Initially it was believed that the long integration setting of AD7746 will solve the problem of 50 Hz hum. As the temperature measurements were performed at temperatures, below room temperature, the chamber compressor switching affected the sensor readout as depicted in Figure 3.



Fig. 3: Sensor readout at lower temperatures.

Figure 3 is showing raw CDC response versus number of samples. The sample rate was set at two samples per second. The left part of Figure 3 is showing disturbed CDC readout when temperature chamber compressor was switched. Pressure was increased from offset to full scale in three increments. The right part of Figure 3 is showing the CDC readout with compressor turned off and again



Fig. 4: CDC readout stability.

with three pressure settings, ranging from offset to maximal pressure. As the temperature was elevated above room temperature, the CDC readout diminished, as the compressor is not needed for achievement of higher temperatures. Sensor was fitted with additional shielding (tin foil) and the shielding terminal was grounded in further measurements. Results of raw CDC response stability are shown in Figure 4 at three different temperatures at 0 °C, 35 °C and 70 °C.

Sensor responses were evaluated and stabilized CDC raw response points were obtained at different temperatures. Results of stabilized raw CDC readouts at different temperatures are depicted in Figure 5. At each temperature setting, three pressure points were obtained. Acquired stability results are showing 12 % of sensor response degradation over temperature increase from 0 °C to 35 °C. This turned our attention to more elaborate temperature analysis of sensor properties.



Fig. 5: Stabilized CDC readouts vs. pressure over entire temperature range.

Acquired sensor characteristics were redisplayed as a function of temperature. Resulting data is depicted in Figure 6. This enabled further sensor temperature properties assessment. Analysis from Figure 6 has shown, that tested sensor exhibits a typical pressure span of 1400 counts over 2000 mbar range, which yields approximately an average sensitivity of -0.7 counts/mbar. The temperature coefficient of offset was evaluated as a normalized sensor response over observed temperature range. A large sensor offset temperature coefficient was found at 0.3% FS/°C, which results in total 21% change of sensor offset over temperature range. More encouraging was a low temperature coefficient of sensitivity value, which was estimated at 0.04% FS/°C.



Fig. 6: Stabilized CDC readouts vs. temperature over entire pressure range.

A fairly consistent 3% change in sensitivity was found over temperature calibration range. This indicates the simplicity of sensitivity compensation. On the other hand, a large dependence of sensor offset requires a more complex offset compensation algorithm.

3. Temperature compensation

As the CDC produces a digital capacitance readout, we focused our work towards digital implementations of temperature compensations. The CDC features $\Sigma\Delta$ approach, the sample rate is limited to several tenths of samples (90 SPS maximum for AD7746), indicating that the increasing complexity of digital processing after acquisition of raw sensor data is not the limiting factor for the entire sensor signal processing.

Temperature compensation of capacitive sensor requires an accurate mathematical description of sensor characteristic in two directions. In case of investigated pressure sensor, the input axes comprise raw pressure and temperature readout and the result is the compensated pressure. Compensation complexity level is depending on sensor nonlinearity of temperature and pressure characteristic. Most adaptable and versatile digital description of sensor characteristic is achieved by Taylor expansion of sensor characteristic. Sensor characteristic expansion can be further segmetned into intervals by writing an expansion around interval ($p_{ocOFFSET}$, $T_{ocOFFSET}$).

$$\Delta p = p_{oc} - p_{ocOFFSET}$$

$$\Delta T = T_{oc} - T_{ocOFFSET}$$
(2)

where the raw pressure readout p_{oc} and raw temperature readout T_{oc} are offset with corresponding values $p_{ocOFFSET}$ and $T_{ocOFFSET}$ respectively. Segmentation using (2) further reduces the calibration error.

Taylor series description (3) represents a general approach to sensor characteristic description using segmentation, recommended by IEEE1541.2 standard /8/.

$$p = \sum_{i=00j=}^{N_P} \sum_{j=0}^{N_T} A_{ij} \cdot \Delta p^i \cdot \Delta T^j$$
(3)

Where Δp represents an offset corrected raw readout from capacitive sensor, ΔT represents the offset corrected raw readout from temperature sensor residing on sensor signal conditioner and the N_p and N_{τ} represent the order of Taylor series.

However, such representation requires $N_{p} \cdot N_{\tau}$ calibration points, which is unacceptable. Another major drawback is the use of floating – point calculation coefficients A_{ij} and involution operator. Although algorithms for fast evaluation of (3) were presented /9/, time consuming mathematical operations will reduce the output update rate. On the other hand, the Taylor expansion provides a reasonable start point for initial coefficient relevance. coefficients A_{ij} are obtained by solving a system of linear equations. However, this system is resolved by computing a Vandermonde matrix, which is generally ill conditioned. In order accommodate abovementioned drawbacks, a two – dimensional Padé approximant, also named Chisholm approximant /10/, is evaluated. This evaluation inherently reduces the number of required calibration points by one.

$$A(p_{oc} T_{od}) = \sum_{i=0}^{N_{p}} \sum_{j=0}^{N_{p}} a_{ij} \cdot \Delta p^{i} \cdot \Delta T^{j}$$

$$B(p_{oc} T_{od}) = \sum_{i=0}^{N_{p}} \sum_{j=0}^{N_{p}} b_{ij} \cdot \Delta p^{i} \cdot \Delta T^{j}$$

$$p(p_{oc}, T_{oc}) = \frac{A(p_{oc}, T_{oc})}{B(p_{oc}, T_{oc})} \quad \text{where} \quad b_{00} = 1$$
(4)

For effective temperature compensation of capacitive sensor signal conditioner a two-dimensional rational polynomial for pressure calculation is used /11/. This type of digital temperature compensation enables correction of nonlinearities up to second order.

$$p = \frac{A_0 + \Delta P + A_1 \cdot \Delta P^2 + A_2 \cdot \Delta T + A_3 \cdot \Delta T^2}{A_4 + A_5 \cdot \Delta T + A_6 \cdot \Delta T^2}$$
(5)

Where A_0 through A_6 are calibration coefficients of pressure sensor. Pressure sensor characteristic can be described with inverse proportion of A_4 to sensor sensitivity and the ratio of A_0/A_4 in proportion to sensor offset. Ratio of coefficients A_2 and A_5 are in direct proportion to linear dependence of sensor temperature sensitivity, while the ratio of coefficients A_3 and A_6 represents the quadratic dependence of sensor temperature sensitivity. Value of p corresponds to the normalized pressure output. The value of p lies within interval /0..1). Value of Δp represents an offset corrected raw readout from capacitive sensor, while the value of ΔT represents the offset corrected raw readout from temperature sensor residing on sensor signal conditioner according to equation (2).

Note that in a given formulations of sensor characteristic description (3) and (4), the actual temperature and capacitance readouts have only indirect significance to final measured quantity p, since the calculation of sensor characteristic description does not depend on actual value of capacitance or temperature.

In case of presented sensor, the pressure dependence of sensor characteristic can be described with linear relationship, while the temperature dependence can be described with quadratic relationship. Measurement resolution was set at 16 bits, maximum obtained resolution of AD7746 for described measurement setup.

The abovementioned observations result in a simplified form of temperature compensation principle for capacitive sensor by setting coefficient A_o in (2) – the quadratic dependence of capacitive pressure sensor to zero, thus reducing the number of calibration points.

The solution for the unknown coefficients $A_{\sigma}...A_{6}$ can be found by solving a system of linear equations, obtained from calibration data, depicted in Figure 6. Seven calibration points are selected and ordered into calibration scenario. Calibration scenario represents a sequence of calibration points, comprised of boundary values, which define the pressure and temperature calibration interval. Remaining calibration points are selected at mid – scale of temperature and pressure range, which result in total nine calibration point mesh. The excess two calibration points are used for verification of total calibration error.

4. Results

Software for acquisition, analysis and calibration of capacitive sensors was designed. Table 1 summarizes the evaluation of data depicted in Figure 6. First seven calibration points were used for evaluation of calibration coefficients.

CP#	P _{cal} (mbar)	T(°C)	p _{oc}	T _{oc}
1	0	0	26526	16406
2	1000	0	25767	16406
3	2000	0	25123	16406
4	0	35	26366	16524
5	2000	35	25006	16524
6	0	70	26245	16651
7	2000	70	24902	16651
8	1000	35	25630	16524
9	1000	70	25522	16651

Additional test points, which were obtained during the acquisition stage of the calibration process, are summarized in Table 2. The first two test points were a part of acquisition of the calibration process and the remaining points were obtained during temperature scan.

TP#	P(mbar)	p _{oc}	T _{oc}	T(°C)
1	1000	25630	16524	35
2	1000	25522	16651	70
3	0	26446	16465	15
4	1000	25698	16465	15
5	2000	25064	16465	15
6	0	26305	16587	55
7	1000	25576	16587	55
8	2000	24954	16587	55

Table 2: Input testpoint data.

Data was first analyzed using a Taylor expansion for coefficient relevance assessment. This description uses 9 calibration points in order to determine all calibration coefficients. Calibration coefficients were obtained by solving a linear system of equations based on Taylor expansion (3). Resulting calibration coefficients are summarized in Table 3. Taylor expansion coefficients confirm the small nonlinearity (A_{o2}) of characterized sensor in pressure direction. Furthermore, results in Table 3 show that linear and quadratic terms are dominant for successful sensor compensation, while the small cross – products between pressure and temperature direction indicate, that sensor characteristic evaluation can be simplified.

Table 3: Calculated calibration coefficients of Taylor	•
expansion.	

A ₀₀	1772.47	A ₁₂	7.18E-07
A ₀₁	-1.35	A ₂₀	1.94E-03
A ₀₂	-1.40E-05	A ₂₁	1.72E-07
A ₁₀	-3.49	A ₂₂	-6.66E-10
A ₁₁	-8.71E-05		

Evaluation of a Taylor expansion (2) using coefficients listed in Table 3 was performed. Equation (2) was evaluated at testpoints in Table 2. Results are shown in Table 4, which lists the calibration error ε .

$$\varepsilon = \left| \frac{P_{CAL} - P_{EVAL}}{FS} \right| \cdot 100\%$$
(6)

Where P_{CAL} represents calibration pressure point, P_{EVAL} , evaluation pressure and FS the output pressure span. Results summarized in Table 4 are in fair agreement with calibration pressure points. A 0.5% discrepancy was found at the endpoint of temperature calibration range at testpoint 8 (*T*=70°C).

Table 4: Calculated calibration coefficients of Taylor expansion.

T _{oc}	p _{oc}	P _{CAL}	P _{EVAL}	ε(%)
16465	25064	2000	1995.69	-0.22
16465	25698	1000	993.60	-0.32
16465	26446	0	-6.92	-0.35
16587	24954	2000	1995.48	-0.23
16587	25576	1000	992.37	-0.38
16587	26305	0	-9.36	-0.47

Simplification is performed by introduction of Chisholm approximant for sensor characteristic description. Chisholm approximant of degree (1,2) would require 11 calibration coefficients.

This lead to evaluation of a linear Padé (1,1) approximant, which requires 7 coefficients for evaluation. Calibration dataset was taken from first seven calibration points in Table 1. Resulting coefficients are summarized in Table 5.

Table 5: Resulting Padé (1, 1) calibration coefficients.

a ₀₀	1666.67	b ₀₀	1
a ₀₁	-1.47	b ₀₁	1.68E-03
a ₁₀	-0.60	b ₁₀	5.48E-04
a ₁₁	-3.51E-03	b ₁₁	-6.28E-07

Equation (4) was evaluated at testpoints in Table 2. Results are shown in Table 6, which lists the calibration error ε according to equation (4).

Results in Table 6 are in fair agreement with calibration pressure points. A rather large 1.5% discrepancy occurs at the endpoint of temperature calibration range at testpoint 2 ($T=70^{\circ}$ C).

TP#	P _{cal} (mbar)	P _{EVAL} (mbar)	ε(%)
1	1000	1000	0.0
2	1000	1030.7	1.53
3	0	-8.7	0.43
4	1000	972.7	1.36
5	2000	1995.84	0.20
6	0	-5.32	0.26
7	1000	1011.6	0.58
8	2000	1996.55	0.17

Table 6: Evaluation error at testpoint data.

In order to further improve compensation accuracy, a Padé (2,2) approximant was analyzed. A full evaluation of Padé (2,2) approximant would require a set of 17 calibration points, which is unacceptable for mass production of sensors. The original evaluation was therefore normalized with coefficient $4/A_4$ factor and cross products terms of temperature and pressure were neglected. In order to minimize computational errors, coefficients were weighed according to:

$$p = \frac{2^2 \cdot \Delta P + 2^{-24} \cdot A_0 \cdot \Delta P^2 + A_1 + 2^{-9} \cdot A_2 \cdot \Delta T + 2^{-18} \cdot A_3 \cdot \Delta T^2}{A_4 + 2^{-9} \cdot A_5 \cdot \Delta T + 2^{-18} \cdot A_6 \cdot \Delta T^2}$$
(7)

Evaluation of system of linear equations based on equation (4) yields the calibration coefficients summarized in Table 2.

Table 7: Resulting calibration coefficients.

A _o	A ₁	A ₂	A ₃	A_4	A ₅	A ₆
-8192	-5057	4999	-1391	-12931	2147	-1202

Equation (4) was evaluated at testpoints in Table 3. Results are shown in Table 8. A maximum 0.4% deviation from measured data was found at 0 mbar both at 0 °C and 70 °C, while the compensation remains well in typical industrial sensor applications (0.5% admissible temperature error over entire temperature calibration range).

Table 8: Evaluation error at testpoint data.

TP#	P _{cal} (mbar)	P _{EVAL} (mbar)	ε(%)
1	1000	1006	0.3
2	1000	1003	0.15
3	0	-8	0.4
4	1000	998	0.1
5	2000	1997	0.15
6	0	-7	0.35
7	1000	999	0.05
8	2000	1996	0.2

4. Conclusions

Implementation of a digital temperature compensation method, developed for piezoresistive pressure sensors, to the field of capacitive sensors was presented. Possibilities for the compensation of sensor parameters such as sensor nonlinearity and temperature sensitivity were analyzed. In order to achieve effective compensation and linearization, different digital descriptions of sensor characteristic were investigated and reported, such as two-dimensional rational polynomial description derived from Padé approximations. Evaluation results of sensor response were compared against reference pressure source and most effective digital temperature compensation was proposed. Proposed digital compensation yields maximum 0.4% FS error on a compensation range 0 - 70 °C and enables integer arithmetic, thus making proposed approach appropriate for use in modern sensor signal conditioning integrated circuits.

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THICK FILM SENSING ELEMENTS ON LTCC STRUCTURES

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Key words: thick film resistors, LTCC substrates, gauge factors, electrical characteristics

Abstract: The ceramic micro electro-mechanical systems (Ceramic-MEMS) are fabricated as 3D structures in many cases by the low-temperature co-fired ceramics (LTCC). The sensors of mechanical quantities are fundamental parts of MEMS and thick-film resistor materials can be used to sense mechanical deformations in the MEMS structures. The paper deals with thick film resistors fired on LTCC structures. The microstructures of LTCC tapes were investigated. The compatibility between thick film resistor materials and LTCC tapes was studied. The possible interactions between thick film layers and LTCC substrates were thoroughly investigated by scanning electron microscope and EDX (Energy dispersive Analysis). Thick-film piezo-resistors as strain-gauges were made with 2000 series (Du Pont) resistors with a known good characteristics (i.e., low noise and "superior" stability of fired resistors) and 3414-B (ESL, high gauge factors). Electrical characteristics and gauge factors were evaluated.

Debeloplastni senzorski elementi realizirani v LTCC strukturah

Kjučne besede: debeloplastni upori, LTCC podlage, faktorji gauge, električne karakteristike

Izvleček: Tehnologija LTCC (Low Temperature Co-fired Ceramics - keramika z nizko temperaturo žganja) je zelo primerna za izdelavo keramičnih modulov - tako večplastnih elektronskih vezij kot struktur z membranami, konzolami, mostički, pokopanimi kanali in votlinami. Tipičen primer takega keramičnega mikrosistema so mikro elektro mehanski sistemi (MEMS – Micro Electro Mechanical Systems).

LTCC material se sintra do visoke gostote pri razmeroma nizkih temperaturah, okrog 850°C. Da se material lahko zgosti pri teh nizkih temperaturah, je sestavljen iz nizko taljivega kristalizirajočega stekla in keramičnega polnila, večinoma Al₂O₃. Pred žganjem je LTCC material (zmes steklenih in keramičnih delcev ter polimernega materiala) v obliki fleksibilnih folijah različnih debelin. Na posamezne folije se z metodo sitotiska lahko izdelajo različne debeloplastne strukture. Z laminacijo večjega števila tako pripravljenih folij lahko izdelamo 2D ali 3D LTCC strukture. Nato se laminirane strukture toplotno obdelajo - žgejo - pri višjih temperaturah. Med žganjem polimerni material izgori, steklo pa se zasintra v gosto in neporozno strukturo.

Za različne MEMS aplikacije, realizirane v LTCC tehnologiji, je potrebna tudi integracija senzorjev deformacije oz. tlaka. Kot senzorski elementi za te senzorje se uporabljajo debeloplastni upori z razmeroma visokimi faktorji gauge. Večina teh debeloplastnih materialov je prilagojena za žganje na razmeroma nereaktivnih oz. inertnih Al₂O₃ podlagah. Če izdelamo senzorske elemente na LTCC podlagah, materiali reagirajo s steklasto fazo v podlagah, kar spremeni - v glavnem poslabša - njihove električne karakteristike. V prispevku bomo poročali o preiskavah debeloplastnih uporovnih senzorskih elementov, realiziranih na LTCC strukturah. Podali bomo njihove karakteristike in ocenili uporabnost za senzorske aplikacije.

1. Introduction

Electro-mechanical systems (MEMS) are fabricated from different materials by various technologies. They are mainly produced by the micro-machining of silicon, but in some applications ceramic materials are a very useful alternative. The laminated 3D structures made by Low-Temperature Co-fired Ceramics (LTCC) are especially convenient for ceramic MEMS. The LTCC materials are sintered at the relatively low temperatures around 850°C. To sinter to a dense and non-porous structure at these, rather low, temperatures, it has to contain some (or a great deal) low-melting-point glass phase. LTCCs are based on mixture of crystallisable glass and ceramics filler; for example, alumina /1-5/ .Unfired LTCC tapes are a mixture of glass and ceramic particles, for example, alumina, and an organic phase. During firing, first the organics burn out at around 450°C, leaving a mixture

of glass and ceramic particles. At higher temperatures the glass phase melts and the material sinters to a dense and non-porous structure.

The whole process flow of the LTCC technology is schematically shown in Fig. 1. The green tapes are cut into the required dimensions. Vias are punched and filled with a conductor material. After this the conducting layers are screen printed. The substrates are then visually examined and put together into multilayer "packets. These "packets" are laminated under a pressure at temperatures around 80°C and fired at relatively low temperatures of around 850°C, which are typically used for thick-film processing.

Sensors for mechanical quantities are often fundamental parts of MEMS, and screen printed and fired thick-film resistor can be used to sense the mechanical deformations in MEMS structures. Some characteristics of fired LTCC



Fig. 1: Schematically presented the process flow of the LTCC technology

materials as compared with alumina for which most thick film materials are optimised are listed in Table 1.

Table 1: Some characteristics of LTCC and 94-99.5% Al₂O₃ ceramics

Property	LTCC	Al ₂ O ₃ 94-99.5%
TCE (10 ⁻⁶ K)	5.8-7	7.6-8.3
Density (g/cm²)	2.5-3.2	3.7-3.9
Flexural strength (MPa)	170-320	300
Young modulus (GPa)	90-110	215-415
Thermal cond. (Wm/K)	2-4.5	20-26
Diel. Constant	7.5-8	9.2-9.8
Loss tg. (x10 ⁻³)	1.5-2	0.5
Resistivity (ohm.cm)	10 ¹² -10 ¹⁴	10 ¹² -10 ¹⁴
Breakdown voltage (V/100μm)	>4000	3000-4000

Arguably the most important are relatively low elastic moduli of LTCC ceramics as compared with alumina ceramics. This means an increased sensitivity of sensing elements due to the larger deformation. In other words, for the same dimensions of the substrate / diaphragm the operating range



Fig. 2: The deflections of diaphragms made with the alumina and the LTCC at an applied pressure of 100 kPa

can be extended. The deformations of alumina and LTCC based membranes under same conditions are presented in Fig. 2. Some sensors and structures, realised in the LTCC technology are presented in Fig. 3.



Fig. 3: Some sensors and 3D structures realised in the LTCC technology

The changes in resistance of a resistor under an applied stress are partly due to deformation, i.e. the changes in the dimensions of the resistor, and partly due to an alteration in the specific resistivity as a result of changes in the microstructure of the material /6/. The gauge factor (*GF*) of a resistor is defined as the ratio of the relative change in resistance ($\Delta R/R$) and the strain (= $\Delta I/I$):

$$GF = \frac{\Delta R/R}{\Delta l/l} \tag{1}$$

Geometrical factors alone result in gauge factors of 2-2.5. Gauge factors higher than this are due to microstructural changes, i.e. changes to the specific conductivity. The GFs of thick-film resistors are mostly between 3 and 15. Within the same resistor series the GFs and the current noise indices of thick-film resistors increase with increasing sheet resistivity /7,8/. Therefore, in most cases resistors with intermediate sheet resistivities are used for the strain sensors as a useful compromise between sensitivity and relatively low noise and also because of their relatively low power consumption. Prototypes of sensors with piezoresistive sensing elements on alumina and on LTCC are shown in Fig. 4.



Fig. 4: Prototypes of pressure sensors with piezoresistive elements realised on alumina (left) and LTCC (right)

The Du Pont (DP) 951 LTCC tapes were evaluates as they are, at least according to the data from the literature, the

material which is most widely used. For strain sensors 2041 (Du Pont, 10 kohm/sq.) and 3414-B (Electro Science Labs., 10 kohm/sq.) resistors were evaluated. The 2041 resistor was chosen because of its low noise whereas the 3414-B was developed specially for use in strain gauges /8/. As a reference resistors were printed and fired on alumina substrates.

2. Experimental

The LTCC substrates were made by laminating three layers of LTCC tape at 70°C and a pressure of 20 MPa. The laminated green tapes were fired for 1 hour at 450°C (organic binder burnout) and 15 minutes at 875°C.

Thick film resistors printed on LTCC and alumina substrates were terminated by Pd/Ag conductors and fired. The dimensions of the resistors for microstructural analysis and X-ray diffraction (XRD) analysis, which were printed and fired without conductor terminations, were 12.5x12.5 mm².

The changes of resistivity as a function of substrate deformation (gauge factors) were measured with the simple device. The ceramic substrate is supported on both sides. The load is applied to the middle of the substrate with a micrometer and this induces a tensile strain in the resistor. The magnitude of the strain is given by the equation (2)/9/.

$$\varepsilon = \Delta l/l = \frac{6 d t}{L^2} \left(1 - \frac{l}{2 L} \right) \left(1 - \frac{2 x}{L} \right)$$
(2)

where *d* is deflection, *t* is substrate thickness, *L* is distance between support edges, *l* is resistor length and *x* is distance from the centre. The gauge factors are calculated using equations (1) and (2) from the strain and resistivity changes. The test structures with resistors (the bending test) are shown in Fig. 5.

Cold (from -25° C to 25° C) and hot (from 25° C to 125° C) TCRs were calculated from resistivity measurements at -25° C, 25° C, and 125° C. The current noise was measured in dB on 100 mW loaded resistors using the Quan Tech method (Quan Tech Model 315-C).

For the microstructural investigation the samples were mounted in epoxy in a cross-sectional orientation and then cut and polished using standard metallographic techniques. A JEOL JSM 5800 scanning electron microscope (SEM)



Fig. 5: Test structures for resistivity vs. deformation measurements. An alumina substrate is on the top and a LTCC substrate on the bottom

equipped with an energy-dispersive X-ray analyser (EDS) was used for the overall microstructural and compositional analysis. Prior to analysis in the SEM, the samples were coated with carbon to provide electrical conductivity and to avoid charging effects.

3. Results and discussion

The microstructures of the green and the fired LTCC material are shown in Figs. 6.a and 6.b, respectively /4,6/. The unfired material is a mixture of darker alumina and lighter glass particles. After firing the material is densely sintered with dark alumina grains in the glass matrix.



Fig. 6a: Microstructure of a green LTCC tape



Fig. 6b: Microstructure of a LTCC tape fired at 875°C

Electrical characteristics of thick film resistors fired on alumina (used as a reference) and LTCC substrates, i.e. sheet resistivities, cold (from -25°C to 25°C) and hot (from 25°C to 125°C) TCRs, noise indices and gauge factors are presented in Table 2. Noise indices are given in dB and in uV/V.Resistivities vs. temperature are shown in Figs. 7.a and 7.b for 2041 and 3414 resistors, respectively. Gauge factors of resistors which are important for "sensing" characteristics are more or less independent of substrates and are between 10 and 11 for 2041 and around 19 for 3414

Resistor	Substrate	Sheet resistivity (kohm/sq.)	CTCR (10 ⁻⁶ /K)	HTCR (10 ⁻⁶ /K)	Noise (dB)	Noise (µV/V)	GF
2041	Al_2O_3	8.0	-55	15	-21	0.09	10.5
	DP 951	12.5	-40	20	-20	0.10	11.4
3414-B	Al_2O_3	2.9	-45	-15	-4	0.63	19.1
	DP 951	9.3	-430	-360	5	1.74	18.8

Table 2: Sheet resistivities, cold and hot TCRs, noise indices and gauge factors

resistors. In the case of 2041 resistors the other electrical characteristics are not changed too much when fired on LTCC substrates. In the case of 3414-B resistors sheet resistivities, TCRs and noise indices increased significantly indicating that characteristics of this material "sensitive" to reactions between glassy LTCC substrates and active layers. The results indicate that the 2041 resistors could be used as sensing elements when fired on Du Pont 951 LTCC substrates while 3414 resistors are still useful due the high gauge factors but high noise indices and very high TCRs must be taken in the consideration.







Fig. 7b: Resistivities vs. temperature for 3414 resistors fired on alumina and LTCC substrates

The microstructures of 2041 and 3414 resistors on LTCC substrates are shown in Figs. 8.a and 8.b, respectively. The formation of a new phase at the 2041 / LTCC interface can not be observed. .In the case of the 3414 resistor the lighter layer formed at the resistor / LTCC interface. The

light phase in this layer contains over 12 mol. % of PbO which indicates the diffusion of a PbO rich glass from the resistor into the LTCC during firing. That means more extensive interactions between 3414 resistors and glassy LTCC substrates and thereof more significant influence on resistors' characteristics.



Fig. 8a: Cross-section of the 2041 resistor fired at 875°C on the LTCC substrate



Fig. 8b: Cross-section of the 3414 resistor fired at 875°C on the LTCC substrate

4. Conclusions

Thick film resistors 2041 (Du Pont, 10 kohm/sq.) and 3414-B (Electro Science Labs., 10 kohm/sq.) resistors

were printed and fired on alumina and LTCC substrates. Electrical characteristics and gauge factors were measured. The interactions between glassy LTCC materials and resistors were investigated by SEM and EDS. Gauge factors of resistors which are important for "sensing" characteristics are more or less independent of the substrates and are between 10 and 11 for 2041 and around 19 for 3414 resistors. In the case of 3414-B resistors sheet resistivities, TCRs and noise indices increased significantly indicating that characteristics of this material "sensitive" to reactions between glassy LTCC substrates and active layers. SEM and EDS analysis did not detect he formation of a new phase at the 2041 / LTCC interface. .In the case of the 3414 resistor the lighter PbO rich layer formed at the resistor / LTCC interface. These results indicate interactions between 3414 resistors and glassy LTCC substrates which influence the resistors' electrical characteristics.

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REŠEVANJE PROBLEMATIKE ELEKTROMAGNETNE ZDRUŽLJIVOSTI SENZORJA ELEKTRIČNEGA TOKA S PROGRAMSKIM ORODJEM ANSYS

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Kjučne besede: tokovni senzor, tuljavica z zračnim jedrom, ANSYS, elektromagnetna združljivost

Izvleček: Odpravljanje oz. minimiziranje zunanjih elektromagnetih vplivov na določeno napravo je lahko zamudno opravilo. Če želimo ta postopek pospešiti, je uporaba računalniških orodij pri tem nepogrešljiva. Primer programskega orodja, ki s pomočjo metode končnih diferenc (FEM-finite element method) izračunava vrednosti želenih fizikalnih količin, je ANSYS.

Merilni del elektronskega števca električne energije, ki ga obravnavamo v prispevku, zaznava električni tok preko pojava magnetne indukcije. Za detekcijo magnetnega polja uporabljamo tuljavice z zračnim jedrom. Senzorski del je zaščiten pred zunanjim magnetnim poljem z oklopom, katerega oblika je pogojena z raznimi dejavniki, zato njegova oblika ni optimalna.

V prispevku s pomočjo programskega orodja ANSYS simuliramo vpliv zunanje nehomogene EM motnje na pogrešek takšnega števca električne energije. V prvem delu simulacije določimo velikost osnovnega merjenega magnetnega polja, ki ga povzroča merjeni električni tok in v drugem delu velikost motilnega polja. Simuliramo, kako sprememba oblike in materiala oklopa vpliva na velikost motilnega polja na mestu tokovnih senzorjev. Pokažemo tudi odvisnost velikosti pogreška števca od položaja motnje. Rezultate nekaterih simulacij primerjamo z meritvami.

Solving electromagnetic compatibility issues of electric current sensors with ANSYS

Key words: current sensor, air core coil, ANSYS, electromagnetic compatibility

Abstract: It can be very time-consuming work to eliminate or at least to minimize external electromagnetic influence on a device. To speed up that phase of the product development the aid of computer programs is necessary. An example of such a computer software is ANSYS. It uses finite element method numerical technique for calculation of physical quantities of our interest.

The electronic energy meter being analyzed in our work uses magnetic induction to reconstruct the measured electric current. In this energy meter air core coils are used for detection of magnetic field. The sensor part of the meter is protected from external magnetic fields using a shield of non-optimal shape. The shape of the shield is non-optimal because it's limited by numerous other factors.

We used ANSYS to simulate influence of external inhomogeneous magnetic field on accuracy of such energy meter. We have first determined the magnitude of the measured magnetic field which is induced by the measured current and then the magnitude (and phase) of the external field. Our simulations show how external magnetic field influences on accuracy changes when shape and material of the shield change. It is also shown how the measurement error changes with changing position of the external magnetic field source. Results of some simulations are compared to measurements.

1 Uvod

Tako kot pri vsaki elektronski napravi je tudi pri elektronskem števcu električne energije pomembno, da je čimbolj neobčutljiv na zunanje elektromagnetne (EM) motnje. Nas je zanimalo, v kakšni meri lahko zunanje magnetno polje vpliva na izmerjeno velikost električnega toka števca. Meritve so bile opravljene na števcu lskraemeco MT173. Za merilni senzor se v tem števcu uporablja tuljavica z zračnim jedrom, ki je neobčutljiva na zunanje statično magnetno polje. Inducirana napetost na tuljavici je sorazmerna spremembi magnetnega pretoka skozi tuljavico, en. (1). Ali je zaznani magnetni pretok skozi tuljavico posledica merjenega električnega toka ali zgolj zunanja motnja, na tem mestu ne moremo ločiti.

$$U_{i} = -N \frac{d\left(\int_{S} \vec{B}(\vec{r}, t) d\vec{S}\right)}{dt}$$
(1)

Vpliv zunanjega magnetnega polja na senzor toka je odvisen tudi od stopnje homogenosti tega polja. Vpliv homogenega polja se v števcu kompenzira z diferencialno vezavo merilnih tuljavic, vpliv nehomogenega polja pa z oklopom iz feromagnetnega materiala, (Slika 1).



Slika 1: Senzorski del števca z oklopom.

V nadaljevanju prispevka se bomo posvetili zgolj vplivu nehomogenega magnetnega polja na točnost števca.

2 Simulacije v programu ANSYS

Da lahko izračunamo delež vpliva zunanje EM motnje na izmerke, potrebujemo najprej podatek o velikosti merjenega magnetnega polja. Zato smo s programskim orodjem ANSYS najprej simulirali električni tok skozi tokovni ovoj in beležili velikost magnetnega polja na mestu merilnih tuljavic. Nato smo simulirali še znano zunanjo motnjo in beležili velikost magnetnega polja na mestu merilnih tuljavic, ki ga je povzročila ta motnja.

2.1 Simulacija velikosti merjenega polja

V tej simulaciji smo določili povprečno amplitudo magnetnega polja v volumnu vsake od obeh tuljavic pri danem električnem toku I_M skozi ovoj.



Slika 2: Tokovni ovoj in merilni tuljavici.

Na Sliki 2 vidimo obliko ovoja, poziciji tuljavic ter obliko in velikost magnetnega polja na mestu tuljavic. Če privzamemo, da tuljavica zaznava le komponento polja, ki je vzporedna simetrijski osi tuljavic, dobimo pri toku skozi ovoj $I_M = 10A$, povprečno zaznano gostoto magnetnega polja $B_z = 0.87$ mT. Ta podatek potrebujemo v nadaljevanju, za določitev deleža motnje v primerjavi z merjenim poljem. Magnetno polje B_z smo izračunali kot razliko krajevnih povprečij znotraj volumna posamezne tuljavice po enačbi:

$$B_{Z} = \underbrace{\frac{(B_{Z})_{i} \Delta V^{i}}{V}}_{notranja \ tuljavica} - \underbrace{\frac{(B_{Z})_{j} \Delta V^{j}}{V}}_{zunanja \ tuljavica}$$
(2)

saj sta merilni tuljavici vezani diferencialno. Odvisnost velikosti polja ${\rm B_Z}$ od velikosti merjenega toka ${\rm I_M}$ lahko sedaj zapišemo kot

$$B_Z = k_B I_M \tag{3}$$

kjer je izračunana konstanta $k_B = 87 \mu T/A$.

2.2 Simulacija vpliva zunanje nehomogene EM motnje na točnost števca

Sedaj lahko izračunamo velikost magnetnega polja, ki ga povzroča zunanja nehomogena izmenična EM motnja. Za vir motnje smo uporabili tuljavo z železnim jedrom v obliki črke E, katero smo postavili blizu senzorskega dela števca (Slika 3). Ko se s tako tuljavo približamo tuljavicam, se na različnih merilnih tuljavicah inducira različna napetost, saj je magnetno polje precej nehomogeno (Slika 4).



Slika 3: Nehomogena magnetna motnja.

Amplituda nehomogenega magnetnega polja na mestu tuljavic se z uporabo oklopa zmanjša. Ker pa je poleg povprečne amplitude polja pomembna tudi razlika amplitud polja na mestih različnih tuljavic, rešitev problema ni trivialna. Simulacija motilnega polja (Slika 4) je zato eden hitrejših načinov za določanje pričakovanega pogreška števca, ki je posledica te motnje.



Slika 4: Nehomogeno motilno magnetno polje.

Pogrešek je sorazmeren z razliko amplitude magnetnega polja na mestih tuljavic v istem ovoju po spodnji enačbi:

$$err\left[\%\right] = \frac{B_{motnja}}{B_Z} 100$$
(4)

Vrednost za B_{motnja} izračunamo na enak način kot za B_z , en.(2), le da je tokrat izvor polja EM motnja in ne merjeni tok.

Najprej smo simulirali, pri kateri legi motnje lahko pričakujemo največji pogrešek na določeni fazi. Motnjo smo postavili nad merilno fazo L2 in simulirali polje v odvisnosti od pomika vzdolž tokovnega ovoja (Slika 5).



Slika 5: Položaj motilne tuljave. Zgornji oklop ni prikazan zaradi preglednosti.

Glede na rezultate simulacije lahko pričakujemo največji pogrešek na posamezni fazi pri položaju EM motnje v bližini robu zgornjega oklopa (Slika 6).



Slika 6: Simulirana amplituda motnje na posamezni fazi od položaja motnje glede na y os (x=28mm).





Ko smo ugotovili položaj največje motnje glede na y os, smo postavili motnjo v ta položaj in variirali še položaj motilne tuljave glede na x os (Slika 7). To smo nato primerjali z meritvami.



Slika 8: Izmerjen pogrešek števca pri I_{M} =5A.

2.3 Primerjava rezultatov simulacij z meritvami

Če želimo rezultate simulacij primerjati z meritvami pogreška števca (Slika 8), moramo vedeti, kako se motnja odraža na pogrešku. Merjeni tok I_M je v fazi z gonilno napetostjo U_G, medtem ko električni tok skozi motilno tuljavo I_T zaostaja za gonilno napetostjo za kot Φ_T :

$$U_G = (U_G)_0 e^{i\omega t}$$

$$I_M = (I_M)_0 e^{i\omega t}$$
(5)

Kot Φ_{τ} je določen z induktivnostjo in upornostjo tuljave:

$$\Phi_T = \arctan\left(\frac{\omega L}{R}\right)$$
$$= \frac{2\pi 50 s^{-1} 6,011 H}{540 \Omega} \doteq 74^{\circ}$$
(6)

Pri treh meritvah, katerih rezultati so prikazani na Sliki 8, je bila motilna tuljava priključena enkrat na napetost faze L1, enkrat na napetost faze L2 in enkrat na napetost faze L3, vsakič z nasprotno polariteto. Tri krivulje na Sliki 8 prikazujejo te tri različne meritve. Če želimo rezultate simulacij (Slika 7) primerjati z rezultati meritev (Slika 8), moramo sešteti projekcije simuliranih amplitud motnje na posamezni fazi na vsako merjeno fazo. Pomagajmo si s kazalčnim diagramom na Sliki 9. Na tem diagramu vidimo primer, ko je motilna tuljava priključena na napetost faze L2. Tok skozi tuljavo I_T ter B_{motnia} kasnita za napetostjo U_{L2} za kot Φ_T =74° in ker je tuljavica priključena z nasprotno fazo, zavrtimo motnjo še za dodatnih 180°. Poiščemo projekcijo vektorja motnje B_{motnia} oz. I_T na faze L1, L2 in L3 za ta primer, en. (7). Ko imamo enkrat vse tri projekcije motnje, lahko izračunamo pričakovan pogrešek po en. (4).

$$B_{motnja}^{L1} = B_{motnja} \underbrace{\cos(-\Phi_T + 180^\circ - 120^\circ)}_{k_{L2}^{L2}}$$
$$B_{motnja}^{L2} = B_{motnja} \underbrace{\cos(-\Phi_T + 180^\circ)}_{k_{L2}^{L2}}$$
$$B_{motnja}^{L3} = B_{motnja} \underbrace{\cos(-\Phi_T + 180^\circ - 240^\circ)}_{k_{L2}^{L3}}$$
(7)



Slika 9: Kazalčni diagram.

Še prej pa moramo upoštevati, da je B_{motnja} krajevno odvisna in ni enaka na lokacijah tuljavic v različnih fazah, en. (8). Upoštevati moramo različne vrednosti B_{motnja} za projekcije

$$B_{motnja} = B_{motnja}(\vec{r})$$
(8)

na različne faze. Enačbe (7) moramo torej popraviti v:

$$B_{motnja}^{L1} = B_{motnja} (L1) k_{L2}^{L1}$$

$$B_{motnja}^{L2} = B_{motnja} (L2) k_{L2}^{L2}$$

$$B_{motnja}^{L3} = B_{motnja} (L3) k_{L2}^{L3}$$
(9)

Vrednosti za B_{motnja}(Lx) dobimo iz simulacij (Slika 7) in predstavljajo velikost motnje na posamezni fazi, izračunane na enak način kot merjeno polje, en. (2). Pogrešek števca, ko je motnja v fazi L2, lahko izračunamo po spodnji enačbi:

$$err_{motnjavL2} [\%] = \frac{\Delta P}{P_0} 100 =$$

$$= \frac{U_0 \Delta I_{L1} + U_0 \Delta I_{L2} + U_0 \Delta I_{L3}}{3U_0 I_M} 100 =$$

$$= \frac{\Delta I_{L1} + \Delta I_{L2} + \Delta I_{L3}}{3I_M} 100 =$$

$$= \frac{(B_{motnja}^{L1} + B_{motnja}^{L2} + B_{motnja}^{L3})/k_B}{3B_Z / k_B} 100 =$$

$$= \frac{B_{motnja}^{L1} + B_{motnja}^{L2} + B_{motnja}^{L3}}{3B_Z} 100$$

V imenovalcu je vrednost $3B_z$, ker je bil pogrešek števca merjen pri simetrični obremenitvi števca. Tok z amplitudo I_M je torej tekel skozi vse tri tokovne ovoje. Sedaj lahko primerjamo izmerjen pogrešek z rezultati simulacije.

$$err_{motnjavL2}(x)[\%] =$$

$$= \frac{B_{motnja}^{L1}(x) + B_{motnja}^{L2}(x) + B_{motnja}^{L3}(x)}{3B_{Z}} 100$$
(11)

Če želimo imeti profil pogreška, ko se pomikamo z motnjo po x osi, upoštevamo enačbo (11). S pomočjo enačb (9) in (11) lahko sedaj vsako simulirano točko amplitude motnje B_{motnia}(Lx) s Slike 7 pretvorimo v pripadajoč pogrešek. Dobimo rezultat prikazan na Sliki 10. Če želimo postopek ponoviti še za ostala dva primera, spremenimo le koeficiente k_x^{γ} . Potrebno je zamenjati vloge faz in obdržati njihovo prvotno zaporedje.



Slika 10: Primerjava rezultatov simulacije in meritev, ko je motnja v fazi z L2.

Na Sliki 11 je prikazano vrtenje faz v smeri urinega kazalca, kar ustreza preklopu motnje iz prvotne faze L2 v fazo L1 in nato v L3. Ob tem se preslikajo koeficienti iz enačbe (9) na način, kot je prikazano v enačbi (12). Sedaj lahko popravimo enačbe (9),



Slika 11: Vrtenje faz v smeri urinega kazalca.

$$U_{G} = U_{L2} \rightarrow U_{LI} \rightarrow U_{L3}$$

$$k_{L2}^{L1} \rightarrow k_{L1}^{L3} \rightarrow k_{L3}^{L2}$$

$$k_{L2}^{L2} \rightarrow k_{L1}^{L1} \rightarrow k_{L3}^{L3}$$

$$k_{L2}^{L3} \rightarrow k_{L1}^{L2} \rightarrow k_{L3}^{L1}$$
(12)

za ostali dve meritvi. Ko je motnja v fazi z L1 pišemo:

$$B_{motnja}^{L1} = B_{motnja} (L1) k_{L1}^{L1}$$

$$B_{motnja}^{L2} = B_{motnja} (L2) k_{L1}^{L2}$$

$$B_{motnja}^{L3} = B_{motnja} (L3) k_{L1}^{L3}$$
(13)

in ko upoštevamo relacije, en. (12), lahko to izrazimo z znanimi koeficienti k_{12}^{Y} . Z uporabo enačb (14) in (11) lahko

končno dobimo simuliran pogrešek, ko je motnja v fazi z L1. Tega primerjamo z meritvami (Slika 12).

$$B_{motnja}^{L1} = B_{motnja}(L1)k_{L2}^{L2}$$

$$B_{motnja}^{L2} = B_{motnja}(L2)k_{L2}^{L3}$$

$$B_{motnja}^{L3} = B_{motnja}(L3)k_{L2}^{L1}$$
(14)



Slika 12: Primerjava rezultatov simulacije in meritev, ko je motnja v fazi z L1.

Na enak način, kot smo izračunali simuliran pogrešek za primer, ko je motnja v fazi z L1, izračunamo še za primer, ko je motnja v fazi z L3. Dobimo spodnji set enačb:

$$B_{motnja}^{L1} = B_{motnja} (L1) k_{L2}^{L3}$$

$$B_{motnja}^{L2} = B_{motnja} (L2) k_{L2}^{L1}$$

$$B_{motnja}^{L3} = B_{motnja} (L3) k_{L2}^{L2}$$
(15)

in simuliran pogrešek primerjamo z meritvami (Slika 13).



Slika 13: Primerjava rezultatov simulacije in meritev, ko je motnja v fazi z L3.

Opazimo, da se ob uporabljenem modelu rezultati simulacij zadovoljivo prilegajo meritvam in na podlagi simulacij lahko sklepamo na dejanski pogrešek števca zaradi zunanje motnje. V nadaljevanju pogledamo primer dveh sprememb oklopa in posledičen pričakovan pogrešek, ki ga napovejo simulacije. Za konec simuliramo še pogrešek, kakršnega bi pomerili, če bi odstranili zgornji in spodnji oklop, saj nas zanima koliko dejansko pridobimo z uporabo le-tega.

2.4 Simulacija vpliva spremembe oklopa na odpornost števca proti zunanji nehomogeni EM motnji

Prva sprememba, ki smo jo preverili, je bila zgolj sprememba materiala zgornjega oklopa. Pogledali smo, kakšen pogrešek lahko pričakujemo, če za zgornji material namesto dinamo pločevine (μ_r =1200) vzamemo navadno železo (μ_r =600). Simulacija pokaže v povprečju okoli 50%



Slika 14: Vpliv spremembe materiala zgornjega oklopa.

povečanje pogreška (Slika 14).

Druga sprememba je bila sprememba oblike zgornjega oklopa, ki je bil iz dinamo pločevine. Spremenili smo obliko dela zgornjega oklopa pri priključnici. Tega smo zapognili navzdol proti tokovnim ovojem (Slika 15). Pogrešek (Slika 16) se v primerjavi z izhodiščno obliko oklopa v povprečju zmanjša za približno 20%.



Slika 15: Spremenjena oblika zgornjega oklopa.

Za primerjavo smo pogledali še, kakšen pogrešek lahko pričakujemo, če ne bi imeli nobenega oklopa (Slika 17). To nam da vpogled, koliko se z uporabo oklopa poveča odpornost števca na tovrstne motnje. Vidimo, da je pričakovan pogrešek števca brez obeh oklopov približno 10-krat večji od pričakovanega (in izmerjenega) pogreška števca s katerimkoli od obeh prikazanih oklopov.



Slika 16: Simuliran pogrešek ob spremembi oblike zgornjega oklopa.



Slika 17: Pogrešek, kakršnega pričakujemo brez oklopov.

3 Zaključek

S pomočjo programskega orodja ANSYS lahko zelo preprosto preverimo različne spremembe v senzorskem delu elektronskega števca električne energije. Ujemanje med rezultati simulacij in meritvami je zadovoljivo, kar kaže na to, da je postavljeni model ustrezen. Z modelom, ki bi še bolje opisoval razmere v merilnem delu, bi lahko dobili še bolj natančne rezultate.

Takšno orodje nam omogoča, da lahko hitro in učinkovito preverimo razne nove ideje. Če bi namreč želeli preveriti vpliv različnih sprememb oklopov z dejanskimi meritvami, bi potrebovali bistveno več časa in ljudi, ki bi morali sodelovati v tem procesu.

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WELD QUALITY EVALUATION IN RADIO-FREQUENCY PVC WELDING PROCESS

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Key words: Radio-frequency welding, dielectric heating, PVC joining, polarisation, medical bag sealing

Abstract: This article presents the technology and typical equipment for radio frequency welding of dielectric polar materials. This type of technology is used in production of PVC medical bags (drainage dialysis bags, peritoneal bags, solution bags, EVA bags etc.). The procedure is known and established in industry, but many different nonlinear process variables make the process complex and hard to tune. On the basis of the described experiment it is possible to conclude about the relationships between weld thickness, weld tensile strength and the energy input into the weld. Results show that weld thickness measurement could be used as a non-destructive method for evaluating weld strength.

Določanje kakovosti vara pri postopku radiofrekvenčnega varjenja PVC folij

Kjučne besede: Radiofrekvenčno varjenje, dielektrično segrevanje , spajanje PVC, polarizacija, varjenje PVC vrečk

Izvleček: V članku je predstavljena tehnologija in oprema za radiofrekvenčno varjenje dielektričnih materialov. Ta tehnologija se v veliki meri uporablja pri izdelavi medicinskih pripomočkov iz PVC-ja (dializne in raztopinske vrečke, drenažne vrečke, vrečke za umetno hrano ipd.). Postopek je sicer že uveljavljen in poznan, vendar je, zaradi velikega števila procesnih parametrov in nelinearnih povezav med njimi, precej kompleksen. Na podlagi interpretacije rezultatov izvedenega eksperimenta je možno sklepati o povezavi med debelino vara, natezno trdnostjo in vnosom energije na mestu vara. S tem se odpira možnost uporabe postopka merjenja debeline vara kot neporušno metodo za ocenjevanje kakovosti vara.

1. Introduction

Use of synthetic materials in industry has been increasing exponentially in the last few decades. An example of a product with high demand for quality and repeatability is a bag for peritoneal dialysis. Peritoneal dialysis bags are made of PVC sheets and PVC tubes which are joined with radio frequency dielectric welding procedure, known also as high frequency capacitive welding. The benefits of this process are short welding cycle, high energy efficiency and possibility to automate the production. Major drawback is that only nonconductive materials with a polar structure and reasonably high dielectric loss factor "e_r tan δ " can be joined using this procedure.

The radio frequency welding procedure is present in different fields of industry. In automotive field Mitelea et al. /1/ were researching weld strengths of some dielectric materials with fabric insertion. Automotive sun-blinds are produced with radiofrequency welding procedure. Some statistical studies on weld strength of PVC with fabric insertion were made. The use of dielectric heating in food processing industry /2/ was researched by Zhao Y. et al. The use of radio frequency heating in wood processing industry for drying and gluing /3/ is described by Resnik J. Optional use of radio frequency process in future polymeric hermetic enclosures for in vivo environment /4/ was considered by Negin Amanat et al. H.T. Sanchéz et al. developed SCADA system /5/ for radio frequency welding procedure of PVC bags for clinical use. Based on on-line sampling of voltage amplitude during weld-ing cycle and statistic comparison to an ideal welding curve, potentially bad products could be eliminated in real time.

Some scientists conducted research on the electromagnetic field and temperature distribution in the specimen during welding. T. Leuca et al. presented the modelling of the electromagnetic field coupled with thermal field through radio frequency applicator /6/. C. Petrescu et al. used genetic algorithms to predict optimal parameters of radio frequency applicator with respect to uniform temperature distribution over the heated material /7/, electric and thermal distribution were modelled and calculated by 2D-FEM.

2. Theoretical background of electromagnetic dielectric heating

Electromagnetic dielectric heating is a volumetric heating method, since the heat is generated internally in the dielectric material. Temperature profile of heated material has a peak value in the centre of the material cross section. In a heating process, both dyes have lower temperature than the heated material itself. In case of a mass production the dyes have to be cooled in order to prevent arcing and maintain stability of the process, which is quite opposite to conventional methods of heating PVC films by introducing heat from heated plates.

Dielectric materials, as for example PVC, have polar molecule structure. One side of the molecule exhibits more positive charge and the other side exhibits more negative charge. Dipole moment, D, of such molecule, is proportional to a single charge (-Q or +Q) multiplied with their displacement r.

$$\mathsf{D} = \mathsf{Q}\mathsf{r} \tag{1}$$

The distance between charges is related to chemical bonding and is considered to be constant. However molecules can rotate and vibrate. The amplitudes depend on the torque and surrounding local viscosity. Their motion tends to have a phase lag due to molecular friction and inertial effects.



Fig. 1: Polarization of dipole molecules

Normally, when dielectric material isn't exposed to outer electric field, the molecules are randomly oriented throughout the volume, so the material is macroscopically electrically neutral (Figure 1, a). When dielectric material is exposed to electrical field, the dipole molecules tend to align along it (Figure 1, b and c). This process is known as dipole polarization. If the polarity of outer electric field is changing rapidly with time, the dipole molecules try to follow that by rotation. With each rotation some heat is generated due to intermolecular friction. The input power per unit volume, provided by the radio frequency welding machine, is proportional to the frequency and amplitude of the applied alternating electrical field, material permittivity and material loss factor eq. (2) /8/ .

$$P_{T_{out}} = E^2 2\pi n \varepsilon_r \varepsilon_0 \tan \delta$$
 (2)

The RF welding process can be described with a model of a lossy capacitor (Figure 2), where the upper and lower dye are acting as capacitor plates and the heat is created in the dielectric material between them. Electrically it can be modelled as an ideal capacitor with resistor connected in parallel (Figure 2).

The admittance of such a circuit can be calculated as in eq. (3), where "A" stands for capacitor plates area and "d" stands for distance between the plates /9/.

$$Y = \frac{j\omega A\varepsilon_o\varepsilon_r(\omega)}{d} + \frac{\omega A\varepsilon_o\varepsilon_r(\omega)}{d}$$
(3)

The frequency ranges that are allowed in dielectric heating and welding applications are limited to one of the ISM¹





Fig. 2: U-I Vector diagram with equivalent electrical scheme

bands, defined by the ITU-R /10/ organization. In general all the devices operating in these bands must tolerate any interference generated by other ISM equipment. Most of radio frequency welding machines use 27.12 MHz, since it is the most tolerant band in ISM radio frequency spectrum.

The power needed to heat up the dielectric material without considering losses at a contact area between dyes and material can be calculated as product of material density, volume, specific heat capacity and the time derivative of temperature eq. (4)

$$P_{T,in} = \frac{\rho V c \Delta T}{\Delta t} \tag{4}$$

Since the material in radio frequency welding applications is rather thin (in the range of millimetres) and the contact area is big, there are considerable heat losses from the heated material to the dyes.

In literature /8/ we can find some equations that successfully calculate power required to heat dielectric material while also taking into the account the heat losses. One of them is eq. (5), as follows

$$P_{V} = \frac{\pi^{3}k\Delta T}{4d^{2}f\left(\frac{\pi^{2}kt}{c\rho d^{2}}\right)}$$
(5)

In eq. (5) "k" is the dielectric's thermal conductivity in W/m-°C, " Δ T" is the necessary dielectric temperature rise, "d" is the initial total thickness of the dielectric material while being pressed between the dyes, "t" is the heating time in seconds, " ρ " is the density of the dielectric in kg/m³ and "c" is the specific heat of the dielectric in J/kg-°C.

Function "f" (eq. (6)) from denominator of eq. (5) is a thirddegree polynomial

$$f(x) = 0.59 + 0.73x - 0.07x^2 - 0.29x^3$$
(6)

where variable "x" is defined as:

$$x = \log_{10} \left(\frac{\pi^2 kt}{cpd^2} \right) \tag{7}$$

The expression in eq. (5) is valid when the value of "x" in eq. (7) is within the range of $0.1 \le x \le 10$.

3. RF Welding machine and identification of process variables

The typical RF welding machine consists of a high frequency generator (Figure 3, D) and an impedance matching capacitor which regulates the electrical power transmission to the load. The load is basically capacitor with PVC foil as dielectric material and tool acting as bottom/top capacitor plates. As a rule of thumb, the power needed to join two PVC foils with a thickness of 0.5 mm is about 25 W/ $cm^2/11/$, for thinner foils the power increases exponentially due to higher heat transfer to dyes.



Fig. 3: Typical RF welding machine

The upper and lower dye (Figure 3, B and C) play three roles:

- 1) Provide high frequency electrical energy to the material
- 2) Enable fusion of the melted material due to the applied mechanical pressure
- 3) Determine the size and the shape of the weld

The dyes (in literature also referred as "electrode" or simply "tool") are usually made of highly conductive and easy to machine materials, such as copper or brass. Uniform height, rigid construction and parallel mounting on the machine are crucial for high quality welds.

The press (Figure 3, A) provides pressure in the material during heating in order to avoid or minimize the possibility for material deconsolidation /12/.

Radio frequency dielectric heating is a dynamic process. During the welding cycle temperature of dielectric material is rising, at the same time distance between upper and lower dye is decreasing due to lower material viscosity. With smaller distance between the dyes, electric power absorption in the load is changing, eq. (2), as well as heat absorption in the load, eq. (5). On top of that, material loss angle and material permittivity exhibit positive nonlinear trend with temperature rise. As a consequence dielectric medium absorbs more energy (eq. (2)). This effect is also known as "thermal runaway" /13/.

To control all the welding parameters, modern radio frequency welding machines have a control system that is able to tune the power transferred to the load by changing the capacitance of the variable capacitor. It is also possible (for the operator) to adjust following process variables on the control panel:

- Dye clamping force (usually it is a pneumatic or hydraulic system)
- Spacers for limiting minimum distance between the dyes
- Anode current starting value (starting position of variable capacitor plate)²
- Final anode current during welding (function of variable capacitor capacitance)
- Velocity of variable capacitor plates during tuning2
- Pre welding time2
- Welding time
- Cooling time after welding

Upper electrode defines welding shape by its construction, as can be seen in Figure 4. Lower dye can be flat or with opposite contour. Use of buffer material prevents arcing and minimizes heat loses from dielectric material to the lower dye. In cases when besides welding also cutting with radio frequency is applied, the use of buffer material is essential. Buffer material must have high dielectric strength and low dielectric loss factor.



Fig. 4: Section thru welding configuration

Time diagram of a typical welding cycle in a single phase radio frequency welding procedure with automatic power tuning is shown in Figure 5. Process consists of three successive phases:



Fig. 5: Welding sequence

2 Only machines with automatic tuning control system

Phase 1:	Initialisation phase: the press closes, radio frequen- cy source is switched on and a variable capacitor is
	set on a pre-welding value. Control system controls
	only variable capacitor's plate position. Dielectric
	material between the dyes is under full compressive
	load and it begins to heat-up with low intensity. This
	phase can be seen in Figure 5, between T_0 and T_1 .
Phase 2:	Heating phase: after initial delay (t_o , Figure 5),
	control system is switched from a capacitor plate
	position control to an anode current control. Inten-
	sity of heating rises till the anode current set point
	is reached. Temperature of material rises above
	glass transition, material changes from solid domain
	to flow domain. Distance between the upper and
	lower dye is decreasing due to excess material flow.
	On Figure 5 this phase can be identified as area
	between T_1 and T_2
Phase 3	Consolidation phase: The radiofrequency heating
	source is switched off, the press remains closed,
	material temperature begins to fall. Weld shape is
	formed with a material changeover from flow domain
	into a solid domain. After pre-determined delay the
	press opens and the welding procedure is finished.

Energy input (in arbitrary units) from a radio-frequency source to the material is defined by area under the anode current curve (with the assumption of constant voltage). It can be calculated as an integral of the anode current over time (eq. (8)).

$$P_{in,arb} = \int_{T_0}^{T_2} I_a(t) dt$$
 (8)

4. Experimental investigation of the relationship between weld section thickness and weld strength

The optimal set of parameters for radio frequency welding process is hard to obtain and maintain during the production. Environmental conditions, such as humidity and temperature together with material thickness and electrical characteristics non-uniformity, can have big influence on weld quality. Due to many variables, the radio frequency welding procedure can be categorised as a complex process. There is a lack of simple, efficient and generalised model to predict and evaluate the optimal set of parameters.

In order to evaluate the repeatability of welding process and to perform sensitivity test of some parameters, an experiment has been performed, using a RF sealing machines for PVC solution bags production. Altogether 400 samples were welded with 5 sets of welding parameters. The experiment took place in a clean room environment with controlled ambient temperature and humidity. The first set of samples was welded as a reference, so the standard production parameters were used. In other 4 samples sets anode current value, as well as welding time were varied.

The test welding tool consists of two dyes in line, so with each welding cycle we got 4 samples marked "A1", "A2", "B1" and "B2" (Figure 6).



Fig. 6: Location of the samples on RF welding machine (top view – two independent PVC films in tubular form, which run under two separated dyes mounted on a tool plate)

The process parameters which were changed in the experiment are listed in Table 1. For each set of the samples only one parameter was changed at a time, others remained fixed and equal to standard welding parameters.

Table	1:	Parameter	values	for	sample s	sets
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Welding param- eters	Flat welding time /s/	Power adjustment po- tentiometer /110/
Standard production parameters	2	5
Increased power	2	8
Decreased power	2	2
longer welding time	3	5
Shorter welding time	1	5

Actual anode current profile for each welding cycle in the experiment was recorded with a digital oscilloscope and input energy (arbitrary units) for each welding cycle was calculated from the eq. (8). Input energy (arbitrary units) and anode current curves (arbitrary units) comparison for all five parameter sets used in the experiment can be seen in Figure 7. Average input energy in arbitrary units for each set of experiment is listed in Table 2.

Typical process control tests performed in production, with which the welding process is evaluated, are nondestructive, such as dimensional and optical inspection of the product integrity (all welds present, welds well defined, tactile feeling of the welds), weld thickness, peel test and leakage test. It would be time consuming to perform destructive tensile tests on regular basis although standard manual peel test gives good feeling about weld force.

That is why one of the main goals of this experiment was to find out if there is any connection between tensile breaking force needed to break the specimens apart and welding set-up.

In the experiment, thickness of a weld zone was measured in the middle of a weld for every sample after the radio frequency welding procedure. Locations were marked as "A1", "A2", "B1" and "B2" – see Figure 6.

For each set of samples the average thickness for a particular group of samples was calculated. The results are



Fig. 7: Time series of anode current amplitude (measured as a voltage drop on a resistor) recorded with DSO

shown in a column chart (Figure 11). Initial total thickness of the material was 0.7 mm - two sheets, 0.35 mm each.

After the weld thickness measurement samples were precisely cut on 20 mm bands, according to Figure 6, the same samples were clamped into a tensile strength testing machine, as shown in Figure 9, and records of maximum destruction tensile force for each sample were taken. Again, the average values for each of the sample groups in each set of experiment, were calculated. The results are presented in Figure 10.



Fig. 8: Magnified picture of a weld cross section; weld edge with extruded material is clearly seen

5. Interpretation of results

Generally, weld thickness decreases with longer welding time and higher input power. Dependence of weld thickness on power is more pronounced, as expected.

Tensile strength dependence on welding time and power is not so obvious. However, using short welding times and lower power do not produce satisfactory results.

This means that for a good weld input power threshold must be exceeded. This is demonstrated by observing



Fig. 9: Sketch of a tensile test Fb=pull force; vb=pull speed(10mm/min)

sample B2 which was not welded well applying minimum power (thickness equal to original thickness, tensile force practically equals to zero). For this particular case power set to value "2" is right below allowable power threshold.

In practice this means that by obtaining weld thickness in the range of 45 - 65% of total material thickness should guarantee its high tensile strength. Thicknesses above 80% of the original film thickness usually mean low weld peel force while thicknesses below 40% of the original film thickness usually cause sharp welding edges that can be easily broken.



Fig. 10: Average tensile breaking force of the samples



Fig. 11: Average weld thickness of the samples

In further analysis only sample groups "A2" and "B1" were taken into account. Since only center of the tool was clamped by pneumatic valve, tool edges exhibited deformation which resulted in higher distance between top and bottom dye. This is why samples of groups "A1" and "B2" show exceeded nonuniformity and were intentionally omitted.

Input energy, calculated by eq. 8, depends mainly on two machine parameters: welding time and anode current setpoint. In order to fix as many variables as possible, only the samples with the same welding pre-set time were considered. Samples obtained by welding sets with "decreased power", "normal welding parameters" and "increased power" share the same pre-set welding time, so they could be compared together.

It is expected that the weld strength is a function of input energy with a global maximum somewhere over the range of input energy, under assumption that minimal power needed to start melting of material is exceeded. The similar assumption should be valid for weld thickness, which should decrease with increasing input energy.

These assumptions are confirmed observing graphical representation of breaking force versus input energy (arbitrary units) and graphical representation of weld thickness versus input energy (Figure 12). Nonlinear dependence between those variables exists. In Figure 12 lines represent polynomial fit to the data.

Without a doubt this experiment should be performed with more intermediate power set points to obtain more data and allow more accurate interpretation of results

Table 2: Average arbitrary input energy for each set of experiment

	Average input energy (arbitrary units)	Standard deviation of input energy
Shorter welding time	3,0	0,04
Decreased power	4,5	0,03
Normal welding pa- rameters	5,8	0,05
Increased power	7,9	0,09
Longer welding time	8,6	0,06

6. Conclusion

It can be seen (Figure 10 and Figure 11) that there is a relationship between weld thickness and tensile breaking force. In nearly all cases the maximum breaking force is achieved on samples with thicknesses of about 45% to 65% of initial material thickness. As expected, break force begins to decrease with decreasing weld thickness since weld edge effects, and not the weld body itself, start to define its strength.

This result is very encouraging and gives some benefit to production process control. Only by obtaining weld thick-



Fig. 12: Data point distribution of breaking force and weld thickness with respect to arbitrary heating energy for samples A2 and B1. Lines represent polynomial fit to the data

nesses in the range of 45 – 65% should guarantee high weld tensile strength. Thicknesses above 80% of the original film thickness usually mean low weld peel force while thicknesses below 40% of the original film thickness usually cause sharp welding edges that can be easily broken.

We should also comment that if welding power below threshold power is applied (some of samples A1 and B2) we observe larger nonuniformities in weld thickness and break force. Again, if production control finds samples with large thickness nonuniformities and low manual peel force, it should trigger alarm and technicians should start looking for its cause.

We will focus future experiments in obtaining more data to confirm conclusions presented in this article with higher reliability.

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47. Mednarodna konferenca o mikroelektroniki, elektronskih sestavnih delih in materialih – MIDEM 2011

Delavnica o organskih polprevodnikih, tehnologijah in napravah Workshop on Organic Semiconductors, Technologies and Devices

28. september do 30. september 2011 v prostorih in soorganizaciji Univerze v Novi Gorici, v Ajdovščini

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Sedeminštirideseta mednarodna konferenca o mikroelektroniki, elektronskih sestavnih delih in materialih – MIDEM 2011 (47th International Conference on Microelectronics, Devices and Materials) nadaljuje uspešno tradicijo mednarodnih konferenc MIDEM, ki jih vsako leto prireja Strokovno društvo za mikroelektroniko, elektronske sestavne dele in materiale - MIDEM. Področje elektronskih komponent je zelo pomembno in dinamično področje tehničnih znanosti in tehnologij. Problematika se zelo hitro spreminja, potrebno je slediti vsem spremembam, ki se pojavljajo v svetu in doma. Domačim in tujim strokovnjakom nudi možnost izmenjave izkušenj, primerjavo dosežkov in preverjanje raziskovalnih smeri. Na konferenci so predavatelji predstavili najnovejši dosežke na naslednjih področjih:

- senzorji
- tehnike načrtovanja monolitnih in hibridnih integriranih vezij,
- tehnologije izdelave monolitnih in hibridnih integriranih vezij,
- modeliranje tehnoloških procesov in delovanje sestavnih delov,
- tehnike testiranja vezij in podsistemov,
- fizika polprevodnikov,
- novi materiali za elektroniko in njihova uporaba,
- materialoznanstvo in tehnologija izdelave materialov za elektroniko,
- optoelektronika,
- polprevodniški, tankoplastni in debeloplastni senzorji,
- zanesljivost in analiza načinov odpovedi elektronskih

komponent in vezij,

- analizne tehnike v elektroniki in materialoznanstvu.

Na konferenci je bilo letos predstavljeno 44 rednih in 10 vabljenih predavanj v šestih sekcijah z naslednjimi vsebinami:

- materiali, tehnologije in elektronski sestavni deli,
- elektronika
- optoelektronika,
- tanki in debeli filmi,
- integrirana vezja,
- senzorji in aktuatorji.

Na konferenci so bili predstavljeni najnovejši dosežki raziskovalcev iz domačih in tujih raziskovalnih skupin in podjetij. Pomembno vlogo sta odigrali vabljeni predavanji, ki sta povzemala zadnje dosežke iz evropskega in svetovnega vrha izbranih tematik. (Program konference je v prilogi poročila).

Vabljeni predavanji sta bili naslednji:

- M. Richter, M. Wackerle, S. Kibler: Technology and Applications of Microdosing Systems
- H. Suzuki: CSD-derived Ferroelectric Thin Films Moleculardesign for Properties

Ob bok vsakoletni mednarodni konferenci o mikroelektroniki, elektronskih sestavnih delih in materialih – MIDEM (International Conference on Microelectronics, Devices and Materials) prireja Strokovno društvo MIDEM na nove, posebno aktualne in zanimive teme enodnevno delavnico. Tokrat je bila izbrana tematika o organskih polprevodnikih, tehnologijah in napravah in pripravljena delavnica z naslovom »Workshop on Organic semiconductors, technologies and devices«. Na delavnici so bile predstavljene novosti s področja organskih polprevodnikov in njihova praktična uporaba. Vabljeni predavatelji so ugledni strokovnjaki iz akademskega in industrijskega okolja. Poleg akademskih dosežkov so bili predstavljeni tudi najnovejši dosežki na področju industrijskega razvoja naprednih organskih polprevodniških tehnologij s poudarkom na razvoju praktičnih aplikacij. Delavnica je dala vpogled v nove možnosti in trende, ki jih ponujajo organski polprevodniki.

Na delavnici so bili predstavljeni najnovejši dosežki raziskovalcev iz domačih in tujih raziskovalnih skupin in podjetij. Pomembno vlogo so odigrala vabljena predavanja, ki so povzemala zadnje dosežke iz evropskega in svetovnega vrha izbranih tematik.

V delavnici je bilo predstavljeno osem vabljenih predavanj:

- **R. Lazzaroni:** Organic Semiconducting Nanostructures Via Conjugated Polymer Self-Assembly
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Pred konferenco je bil izdelan zbornik s 54 referati (16 tujih avtorjev), skupaj v obsegu 274 strani.

Konference so se udeležili strokovnjaki iz raziskovalnih institucij, univerz in industrije. Skupno število udeležencev konference je bilo 59, od tega 46 domačih in 13 tujih udeležencev, kar kaže na visok trend naraščanja obiska konferenc MIDEM.

Glede na navedene podatke in kvaliteto vabljenih in rednih prispevkov smo organizatorji, upamo pa tudi da udeleženci konference, z letošnjo konferenco zelo zadovoljni. To nam je v motivacijo in izziv pri pripravi aktualnih znanstvenih in razvojnih tem ter organizacije konference MIDEM 2012.

Konferenco je delno sofinanciralo Ministrstvo za visoko šolstvo, znanost in tehnologijo v sodelovanju z Javno agencijo za tehnološki razvoj v okviru akcije INO-11 (pogodba št. INO-02), za kar se jim globoko zahvaljujemo.

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43	POLONA ŠORLI	STROKOVNO DRUŠTVO MIDEM, Ljubljana	Slovenija
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39	JOŽEF PERNE	TC SEMTO	Slovenija	
40	MATJAŽ KOŽELJ	IJS, Ljubljana	Slovenija	
41	BRUNO CVIKL	IJS, Ljubljana	Slovenija	

P.Šorli, I.Pompe

Petindvajsetletnica Strokovnega društva za mikroelektroniko, elektronske sestavne dele in materiale MIDEM



Foto: Marjan Smerke

Ob petindvajsetletnici Strokovnega društva za mikroelektroniko, elektronske sestavne dele in materiale MIDEM je na Fakulteti za elektrotehniko Univerze v Ljubljani 26. maja 2011 potekla slavnostna akademija, s katero smo člani, prijatelji in podporniki društva počastili obletnico društva. Na slavnostni akademiji je predsednik društva prof. dr. Marko Topič v nagovoru poudaril pomen strokovnih društev kot veznih členov med akademsko sfero in industrijo, saj predstavljajo možnost sodelovanja, vzpostavljanja in ohranjanja ne le strokovnih, temveč tudi neformalnih, prijateljskih stikov. Podelil je priznanja najzaslužnejšim članom društva za njihovo nesebično in požrtvovalno strokovno delo ter za pomoč in sodelovanje pri društvenih aktivnostih. Med prejemniki priznanj so bili vsi trije bivši predsedniki društva MIDEM, dr. Rudolf Ročak, prof. dr. Marija Kosec in prof. dr. Slavko Amon, dolgoletni aktivni člani, ter nekaj ustanov in podjetij, ki so društvo ves čas podpirala. Med podjetji sta to podjetji Mikroiks d.o.o., Ljubljana in Hyb d.o.o., Šentjernej, med zavodi pa Tehnološki center za sklope, elemente, materiale, tehnologije in opremo za elektrotehniko (TC SEMTO, Ljubljana), Fakulteta za elektrotehniko Univerze v Ljubljani in Institut Jožef Stefan. Profesorica Marija Kosec je dogodek zaključila s slavnostnim predavanjem "Materiali še kar osvajajo svet: globalno in lokalno", v katerem je predstavila posebne lastnosti nekaterih materialov, ki jih uporabljamo v elektroniki.

Ob častitljivi petindvajsetletnici Strokovnega društva za mikroelektroniko, elektronske sestavne dele in materiale MIDEM velja obuditi spomine na ,predzgodovino' društva, ki sega v prva leta po drugi svetovni vojni.

Jugoslovanski komite za elektroniko, telekomunikacije, avtomatizacijo in nuklearno tehniko (ETAN) je bil ustanovljen leta 1953 z namenom, da ustvari možnosti za interdisciplinarno povezovanje strokovnjakov različnih področij tehnike. Že leta 1955 je ETAN začel organizirati strokovne konference, ki so omogočila prikaz dela na omenjenih področjih. Pomladi leta 1962 je prišlo do reorganizacije komiteja; delo je od takrat potekalo v strokovnih odborih za posamezna področja. Tako je bil jeseni 1962 v Ljubljani ustanovljen Zvezni strokovni odbor za elektronske sestavne dele (*Savezni stručni odbor za elektronske sastavne delove i materijale*) SSOSD. V Sloveniji je bilo namreč že kmalu po 2. svetovni vojni precej strokovnjakov z različnih področij, ki so se intenzivno ukvarjali z razvojem elektronskih sestavnih delov in so bili vključeni v ETAN od začetka njegovega delovanja.

V okviru ETAN so leta 1959 v Ljubljani organizirali Prvo jugoslovansko posvetovanje o sestavnih delih za elektronske naprave z 200 udeleženci in 22 preglednimi referati, ki je predstavljalo forum za usmerjanje razvoja industrije elektronskih sestavnih delov v Jugoslaviji. Naslednje srečanje leta 1963 je organiziral že odbor SSOSD.

Področja delovanja SSOSD so v prvem desetletju delovanja obsegala upore, kondenzatorje, dušilke in transformatorje, elektronske cevi, polprevodniške elemente in materiale, magnetne materiale, elektromehanske sestavne dele, sestavne dele za signalizacijo in varnostne naprave, pretvornike fizikalnih veličin v električne, instrumente za vgradnjo, kable in vodnike ter ostale mehanske dele za avtomatizacijo. Ob ustanovitvi leta 1963 mikroelektronika še ni bila pomembno področje, ker pa je z leti njen pomen naraščal in seveda število ljudi, ki so se z njo ukvarjali, so v SSOSD tudi formalno vključili mikroelektroniko. Tako se je leta 1977 odbor z novim statutom preimenoval v Strokovno sekcijo za elektronsko sestavne dele, mikroelektroniko in materiale (*Stručna sekcija za elektronske sastavne delove, mikroelektroniku i materijale*) SSESD. SSOSD oziroma kasneje SSESD je od leta 1963 organiziral letne simpozije o sestavnih delih (SD), ki so zatem nekaj desetletij potekali na Gospodarskem razstavišču v Ljubljani sočasno z razstavo elektronike. Srečanja SD so postala letna zbirališča strokovnjakov s področja elektronskih sestavnih delov in materialov tako iz raziskovalnih skupin kot iz industrije. Zborniki posvetovanj predstavljajo neprecenljiv vir podatkov o razvoju elektronskih sestavnih delov, materialov za elektroniko in mikroelektronike v Sloveniji in Jugoslaviji.

SSESD se je poleg organizacije konferenc ukvarjal še z vrsto drugih področij. Že leta 1965 so izdelali predlog nomenklature elektronskih sestavnih delov. Od leta 1969 so izdajali strokovno revijo Informacije SSESD, ki je štirikrat letno poleg društvenih vesti objavljala strokovne članke.

K aktivnemu delovanju v domačem okolju sta pripomogla dolgoletna sponzorja, Iskrini podjetji Industrija elementov za elektroniko, Ljubljana in Industrija kondenzatorjev, Semič. Zaradi dobrega sodelovanja z domačo industrijo je SSESD v osemdesetih letih prejšnjega stoletja načel tematiko nadomeščanja uvoznih materialov za elektroniko z domačimi. Leta 1984 je komisija SSESD za materiale s finančno podporo Gospodarske zbornice Jugoslavije izdala Študijo o možnostih substitucije uvoznih materialov za elektronsko in elektroindustrijo Jugoslavije.

SSESD si je poleg delovanja v domačem okolju izrazito prizadeval ustvarjati mednarodne stike in sodelovanja, vendar za formalno povezovanje z mednarodnimi društvi ali zvezami kot sekcija ETAN ni imel pooblastil. Od leta 1984 so se število članov, aktivnosti in tudi obseg finančnega poslovanja SSESD tako povečali, da je Izvršilni odbor začel premišljevati o ustanovitvi strokovnega društva v okviru ETAN.

Jugoslovanska zakonodaja ni dopuščala prav veliko svobode pri ustanavljanju neodvisnih društev v okviru posameznih republik, zato je bil 29. 1 1986 društvo ustanovljeno kot Strokovno društvo za mikroelektroniko, elektronske sestavne dele in materiale v občini Ljubljana Šiška. Kratko ime društva MIDEM je zapisano v zapisniku Ustanovne skupščine društva. Pobudniki ustanovitve, navedeni po abecednem redu, so bili Franc Jan (Iskra-Hipot, Šentjernej), Alojzij Keber (Institut Jožef Stefan), Vladimir Klavs (Elektrotehniška zveza Slovenije, Ljubljana), Marjeta Limpel (Iskra-IEZE - Tozd Feriti, Ljubljana), Milan Mekinda, Rudi Ročak (Iskra-Mikroelektronika, Ljubljana), Stanislav Solar (Iskra-Avtoelektrika, Nova Gorica), Milan Slokan, Pavle Tepina (oba SSESD, Ljubljana) in Herman Vidmar (Elektrotehniška zveza Slovenije, Ljubljana). Prvi predsednik društva je postal, kot že omenjeno, dr. Rudi Ročak. Društvo je bilo včlanjeno v ETAN in v Elektrotehniško zvezo Slovenije.

Za dr. Rudolfom Ročakom je vodenje društva leta 1996 prevzela prof. dr. Marija Kosec (IJS), leta 2005 jo je nasledil prof. dr. Slavko Amon (Fakulteta za elektrotehniko Univerze v Ljubljani). Od pomladi 2011 je predsednik društva prof. dr. Marko Topič (Fakulteta za elektrotehniko Univerze v Ljubljani). Po osamosvojitvi Slovenije je društvo MIDEM postalo mednarodno strokovno društvo in prvi tuji član je postal profesor dr. Radomir Kužel (Karlova Univerza, Praga, Češka Republika). Društvo MIDEM je član Mednarodnega združenja za mikroelektroniko in sestave (International Microelectronics and Packaging Society IMAPS).

Kot že omenjeno, sodi med dejavnosti društva od leta 1969 izdajanje strokovne revije za mikroelektroniko, elektronske sestavne dele in materiale "Informacije MIDEM", ki jo od leta 1988 ureja dr. Iztok Šorli. Revija izhaja štirikrat letno in je za leto 2010 dosegla faktor vpliva 0.25.

Društvo vsako leto organizira mednarodno konferenco o mikroelektroniki, sestavnih delih in materialih z delavnico, ki je z vrsto vabljenih predavateljev namenjena poglobljenemu obravnavanju izbranih tem, na primer testiranja elektronskih vezij, optoelektronike, zelene elektronike ali plazemskih tehnologij. Konec septembra je v Ajdovščini potekala že 47. Mednarodna konferenca o mikroelektroniki, sestavnih delih in materialih z delavnico o organskih polprevodnikih – MIDEM 2011.

Ob koncu prispevka se velja spomniti misli pokojnega dolgoletnega člana društva Milana Slokana na ustanovni skupščini društva MIDEM leta 1986, namreč, da ustanovitve društva «ne bi bilo brez ljudi, ki so s prostovoljnim delom pripravili vse v življenju SSOSD in SSESD izvedene prireditve in akcije in ki so vse to povezovali z delovanjem ETAN-a«. Misli gospoda Slokana ostajajao aktualne tudi ob spominih na preteklih petindvajset let: društvo ne bi obstalo brez zavzetega dela mnogih članov, ki jim gre iskrena zahvala za opravljeno delo.

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Avtorja prispevka :

Dr. Barbara Malič Dr. Iztok Šorli

Podeljene Zoisove nagrade in priznanja, priznanje Ambasador znanosti in Puhova priznanja

V Unionski dvorani v Ljubljani je bila 24. novembra 2011 podelitev Zoisovih nagrad in priznanj, priznanja Ambasador znanosti in Puhovih priznanj. Odbor Republike Slovenije za Zoisovo nagrado, Zoisovo priznanje, priznanje Ambasador znanosti RS in Puhovo priznanje, ki mu predseduje akademik prof.dr. Tadej Bajd, je sklenil, da v letu 2011 podeli dve Zoisovi nagradi za življenjsko delo, dve Zoisovi nagradi za vrhunske dosežke na področju znanstveno raziskovalne in razvojne dejavnosti, pet Zoisovih priznanj za pomembne dosežke na področju znanstveno raziskovalne in razvojne dejavnosti, eno priznanje Ambasador znanosti RS in eno Puhovo priznanje za izume, razvojne dosežke in uporabo znanstvenih izsledkov pri uvajanju novosti v gospodarsko prakso.

Svečani dogodek nas je še toliko bolj razveselil, saj sta med nagrajenci tudi člana društva MIDEM, **prof. dr. Miran Mozetič in doc. dr. Uroš Cvelbar**. Z gospodom Ludvikom Kumarjem iz podjetja Kolektor so prejeli

PUHOVO PRIZNANJE za izume, razvojne dosežke in uporabo znanstvenih izsledkov pri uvajanju novosti v gospodarsko prakso.



Fotografija iz arhiva MVZT. Z leve proti desni: akad. Prof. dr. Tadej Bajd, prof. dr. Miran Mozetič, doc. dr. Uroš Cvelbar in Ludvik Kumar.

Podjetje Kolektor je bilo ustanovljeno leta 1963 v Idriji kot proizvajalec komutatorjev. Grafitne komutatorje so začeli razvijati na prelomu tisočletja. To so izdelki z izjemnimi kemijskimi in električnimi lastnostmi. Klasični proizvodni postopek komutatorjev je tehnološko zahteven in okolju neprijazen zaradi okolju nevarnih snovi. Temeljni namen sodelovanja med podjetjem Kolektor in Institutom Jožef Stefan (IJS) je bil v razvoju povsem novega alternativnega tehnološkega postopka. Nagrajenci so v letih med 2004 in 2006 opravljali raziskave na področju interakcije termodinamsko neravnovesne plinske plazme z mikrokompozitnimi vrstami materiala. Sistematične raziskave so pokazale, da je mogoče okolju neprijazne mokre kemijske postopke zamenjati s suhimi postopki, ki temeljijo na uporabi termodinamsko neravnovesnih stanj plina. Na podlagi temeljnih spoznanj je bil izdelan prototip novega mikrokompozitnega komutatorja. Raziskovalci projekta so prav tako razvili, optimizirali in izdelali ustrezno proizvodno linijo, ki je uspešno prestala vsa testiranja kupcev. Nov proizvodni postopek je okolju prijazen, hkrati pa ga odlikujeta izredna zanesljivost in cenovna primernost z veliko dodane vrednosti. Podjetje Kolektor na trgu dosega več kot 60 % svetovne proizvodnje. Proizvodni postopek in naprava sta zaščitena s patenti v ustreznih državah.

Nominirani raziskovalci dokazujejo prevladujočo resnico, da razvoj novih tehnologij sledi zakonitosti: temeljne raziskave, uporabne raziskave, razvoj prototipa, razvoj proizvodne linije, poskusna proizvodnja s prilagoditvijo industrijskemu okolju in redna proizvodnja. Treba je poudariti, da so nominiranci vrhunski raziskovalci z bogato zbirko znanstvenih in uporabnih del in patentov.

Na podlagi zapisanega ugotavljamo, da so raziskovalci in dobitniki Puhovega priznanja za leto 2011 dr. Miran Mozetič, dr. Uroš Cvelbar in Ludvik Kumar dosegli izjemne raziskovalne, razvojne, ekonomske in okoljske učinke pri postavitvi novega suhega postopka proizvodnje grafitnih komutatorjev.

V imenu članov društva MIDEM nagrajencem izrekam iskrene čestitke!

Marko Topič Predsednik društva MIDEM



The primary objective of the conference is the information exchange between academic and industrial partners on electronic devices and systems. The conference topics are mainly physics of semiconductors, electronic devices and systems, packaging and interconnections, sensors and MEMS, integrated circuits and many others. The conference will be held in capital of Moravia - Brno, which is situated in centre of Europe, with many historical and natural memorable places.

Conference topics:

- Electronic Devices and Systems
- Signal Processing and Mixed-Signal Testing
- Physics and Structures of Semiconductors
- Microelectronic Sensors and MEMS
- Microelectronic Technology and Materials
- Packaging and Interconnections
- Lead Free Soldering
- Manufacturing, Quality, and Reliability
- Integrated Circuit Design, CAD and CAE Tools
- Software Tools for Education
- Optoelectronics and Microwave
- Power Electronics

Important dates:

- January 10, 2011 Submission of Abstracts
- January 31, 2012 Notification of Acceptance
- March 20, 2012 Submission of Camera-ready Full Papers
- May 10, 2012 Reviewers comments
- May 20, 2012 Early Registration (Reduced Conference Fee)
- June 1, 2012 Submission of Camera-ready Full Papers Reviewed Version
- June 28-29, 2012 Conference Sessions

More information on http://www.imaps.cz/eds

The best conferences papers will be published in Radioengeneering (IF = 0,503) <u>www.radioeng.cz</u>, or internet journal Electroscope <u>www.electroscope.zcu.cz</u>

Conference organized in cooperation with Brno University of Technology, Faculty of Electrical Engineering and Communication, 616 00 Brno, Czech Republic

IMCS 2012 - The 14th International Meeting on Chemical Sensors

May 20 - 23, 2012, Nürnberg/Nuremberg, Germany

I am pleased to announce that a special issue of Sensors and Actuators B: Chemical will be published for IMCS 2012 - the 14th International Meeting on Chemical Sensors, Nuremberg, Germany, May 20-23 2012.

All authors who contribute to the conference either with an oral or with a poster presentation are invited to submit an extended manuscript of their contribution to Sensors and Actuators B: Chemical. There will be a special and fully peerreviewed IMCS volume. Details can be found at www.IMCS2012.de/proceedings.html

Please note:

The 4-page conference proceedings article is a must for all authors. It will be distributed to the conference participants on CD-ROM. Some times after the conference, all 4-page conference proceedings articles will receive a Digital Object Identifier (DOI) and will be published online. After receipt of their DOI all articles will be fully citable.

The special volume of Sensors and Actuators B: Chemical is an offer for all authors who wish to publish additionally an extended comprehensive full paper in a prestigious journal.

Please be reminded of the approaching submission deadline.

I hope to see you in Nuremberg in 2012.

Best regards

Prof. Ralf Moos, Host of IMCS 2012 Department of Functional Materials University of Bayreuth, Germany

Informacije MIDEM

Strokovna revija za mikroelektroniko, elektronske sestavine dele in materiale

NAVODILA AVTORJEM

Informacije MIDEM je znanstveno-strokovno-društvena publikacija Strokovnega društva za mikroelektroniko, elektronske sestavne dele in materiale - MIDEM. Revija objavlja prispevke s področja mikroelektronike, elektronskih sestavnih delov in materialov. Ob oddaji člankov morajo avtorji predlagati uredništvu razvrstitev dela v skladu s tipologijo za vode-nje bibliografij v okviru sistema COBISS.

Znanstveni in strokovni prispevki bodo recenzirani.

Znanstveno-strokovni prispevki morajo biti pripravljeni na naslednji način:

- 1. Naslov dela, imena in priimki avtorjev brez titul, imena institucij in firm
- 2. Ključne besede in povzetek (največ 250 besed).
- 3. Naslov dela v angleščini.
- Ključne besede v angleščini (Key words) in podaljšani povzetek (Extended Abstract) v anglešcčini, če je članek napisan v slovenščini
- Uvod, glavni del, zaključek, zahvale, dodatki in literatura v skladu z IMRAD shemo (Introduction, Methods, Results And Discsussion).
- Polna imena in priimki avtorjev s titulami, naslovi institucij in firm, v katerih so zaposleni ter tel./Fax/Email podatki.
- Prispevki naj bodo oblikovani enostransko na A4 stra-neh v enem stolpcu z dvojnim razmikom, velikost črk namanj 12pt. Priporočena dolžina članka je 12-15 strani brez slik.

Ostali prispevki, kot so poljudni cčlanki, aplikacijski članki, novice iz stroke, vesti iz delovnih organizacij, inštitutov in fakultet, obvestila o akcijah društva MIDEM in njegovih članov ter drugi prispevki so dobrodošli.

Ostala splošna navodila

- 1. V članku je potrebno uporabljati SI sistem enot oz. v oklepaju navesti alternativne enote.
- Risbe je potrebno izdelati ali iztiskati na belem papirju. Širina risb naj bo do 7.5 oz.15 cm. Vsaka risba, tabela ali fotografija naj ima številko in podnapis, ki označuje njeno vsebino. Risb, tabel in fotografij ni potrebno lepi-ti med tekst, ampak jih je potrebno ločeno priložiti članku. V tekstu je treba označiti mesto, kjer jih je potrebno vstaviti.
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- 4. Uredniški odbor ne bo sprejel strokovnih prispevkov, ki ne bodo poslani v dveh izvodih skupaj z elektronsko verzijo prispevka na disketi ali zgoščenki v formatih ASCII ali Word for Windows. Grafične datoteke naj bodo priložene ločeno in so lahko v formatu TIFF, EPS, JPEG, VMF ali GIF.
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Informacije MIDEM

Journal of Microelectronics, Electronic Components and Materials

INSTRUCTIONS FOR AUTHORS

Informacije MIDEM is a scientific-professional-social publication of Professional Society for Microelectronics, Electronic Components and Materials – MIDEM. In the Journal, scientific and professional contributions are published covering the field of microelectronics, electronic components and materials.

Authors should suggest to the Editorial board the classification of their contribution such as : original scientific paper, review scientific paper, professional paper...

Scientific and professional papers are subject to review.

Each scientific contribution should include the following:

- 1. Title of the paper, authors' names, name of the institution/ company.
- Key Words (5-10 words) and Abstract (200-250 words), stating how the work advances state of the art in the field.
- 3. Introduction, main text, conclusion, acknowledgements, appendix and references following the IMRAD scheme (Introduction, Methods, Results And Discsussion).
- 4. Full authors' names, titles and complete company/institution address, including Tel./Fax/Email.
- 5. Manuscripts should be typed double-spaced on one side of A4 page format in font size 12pt. Recommended length of manuscript (figures not included) is 12-15 pages
- 6. Slovene authors writing in English language must submit title, key words and abstract also in Slovene language.
- Authors writing in Slovene language must submit title, key words and extended abstract (500-700 words) also in English language.

Other types of contributions such as popular papers, application papers, scientific news, news from companies, institutes and universities, reports on actions of MIDEM Society and its members as well as other relevant contributions, of appropriate length, are also welcome.

General informations

- 1. Authors should use SI units and provide alternative units in parentheses wherever necessary.
- 2. Illustrations should be in black on white paper. Their width should be up to 7.5 or 15 cm. Each illustration, table or photograph should be numbered and with legend added. Illustrations, tables and photographs must not be included in the text but added separately. However, their position in the text should be clearly marked.
- 3. Contributions may be written and will be published in Slovene or English language.
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- 5. Authors are fully responsible for the content of the paper.

Contributions are to be sent to the address below.

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MIDEM

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