

Design and Analysis of Low Power Master Slave Flip-Flops

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Abstract: In this paper, a comparative analysis of existing architectures for flip-flop along with the proposed design is made. The comparison is done on the basis of power, delay, PDP and transistor count. Due to continuous increase in integration of transistors and growing needs of portable equipments, low power design is of prime importance. All simulations are performed on TSpice using BSIM models in 130 nm process node. The simulation results show that for all supply voltages, all clock frequencies and all data activities proposed flip-flop consumes the lowest power. Proposed flip-flop has the second shortest delay and the second lowest PDP and also occupies low area. So this design is best suited for low power and high performance applications.

Key words: Pass transistor, Short circuit current, Flip-flop, Optimization, clock distribution network

Načrtovanje in analiza master-slave flip-flop vezij nizkih moči

Povzetek: V članku je predstavljena primerjalna analiza obstoječih arhitektur flip-flop vezij in predlagan načrt. Primerjava je bila opravljena na osnovi moči, zakasnitev PDP in števila tranzistorjev. Ob konstantnem naraščanju integracije tranzistorjev in uporabi prenosnih naprav ima načrtovanje vezij nizkih moči zelo pomembno. Simulacije so bile izvedene s pomočjo TSpicea z uporabo BSIM modelov v 130 nm koraku. Simulacije izkazujejo nizko porabo moči pri vseh frekvencah ure in podatkovnih aktivnostih flip fropa. Predlagan flip flop ima drugi najkrajši čas zakasnitev in drugo najnižjo vrednost PDP ter zaseda malo prostora, kar mu omogoča najboljšo uporabo za visoko zmogljive aplikacije z nizko porabo.

Ključne besede: prehodni tranzistor, kratkostično vezje, flip-flop, optimizacija, razporeditvena mreža ure

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1. Introduction

In many digital very large scale integration (VLSI) designs, the clock system that includes clock distribution network and flip-flops is one of the highest power consuming components. It accounts for 30% to 60% of the total system power, out of which 90% is consumed by the flip-flops and the last branches of the clock distribution network that is driving the flip-flop [1]. Scaling of transistor feature sizes has provided a remarkable advancement in silicon industry for last three decades. However, while the performance increases due to scaling, the power density increases substantially every generation due to higher integration density. Furthermore, the demand for power-sensitive design has grown significantly in recent years due to tremendous growth in portable applications. Consequently, the need for power-efficient design techniques has grown considerably [2]. In the present design consideration

the power consumption and chip area requirements are small and the operating speed is high compared to conventional discrete I.C. design, so low power design with high performance is becoming increasingly important [3]. There are three major sources of power consumption in a digital CMOS circuits. The average power is given by the following equation [4]:

$$P_{avg} = p_t (C_L V_{dd} f_{clk}) + I_{sc} V_{dd} + I_{leakage} V_{dd} \quad (1)$$

The first term represents the switching component of power, where C_L is the effective switched loading capacitance, f_{clk} is the clock frequency and p_t is the probability that a power consuming transition occurs (or activity factor). The second term represents the direct path short circuit current I_{sc} , which arises when both the NMOS and PMOS transistor networks are simultaneously active or on, conducting current from the supply V_{dd} to ground. The third term is leakage power. The

leakage current can arise from substrate injection, gate leakage and sub threshold effects. $I_{leakage}$ is primarily determined by the CMOS fabrication process technology and modeled based on its characterization.

A conventional ASIC design mostly uses an edge-triggered flip-flop as a sequencing element due to simplicity of its timing model. Specifically, the amount of time available to a combinational block that lies between two flip-flops is fixed. This constrains timing uncertainties within each combinational block, which is important for design steps at higher abstraction level such as logic synthesis when implementation details are unknown [5]. For big circuits implementing complex functionalities like control units, microprocessors, usually a very large number of flip-flops are used. So these flip-flops heavily affect the performance of the entire system. This paper focuses on the minimization of power dissipation in the edge triggered flip-flops.

Flip-flops appear in several configurations, such as D flip-flops, T flip-flops and J-K flip-flops where the D flip-flop is the most common. To lower the complexity of circuit design, a large portion of the most digital circuits is synchronous in the sense that they operate using a clock. A conventional single edge-triggered (SET) flip-flop typically latch data either on the rising or the falling edge of the clock cycle. The SET flip-flops are usually configured as master-slave flip-flops, i.e. a sequential structure using two latches, called master and slave respectively, in cascade [6].

This paper is organized into six sections. Section 2 compares the existing single edge triggered flip-flop structures. In section 3, new flip-flop structure is proposed. The nominal simulation conditions, along with analysis and optimization performed during simulation, are discussed in Section 4. In section 5 results are presented and performance for new proposed design and conventional designs are compared in terms of power, delay, PDP and transistor count. Section 6 ends the paper with conclusion.

2. Existing single edge triggered flip-flops

2.1 Push Pull Flip-Flop

To improve the performance of a conventional Transmission Gate Flip-Flop (TGFF shown in Figure 1) [7, 8], addition of an inverter and transmission gate between the outputs of master and slave latches to accomplish a push-pull effect at the slave latch, was proposed in [9]. This increased 4 transistors. To compensate this increment of transistor count, two transmission gates are

eliminated in the Push Pull Flip-Flop from the feedback paths of conventional TGFF. The static Push Pull Flip-Flop (PPFF) is shown in Figure 2.

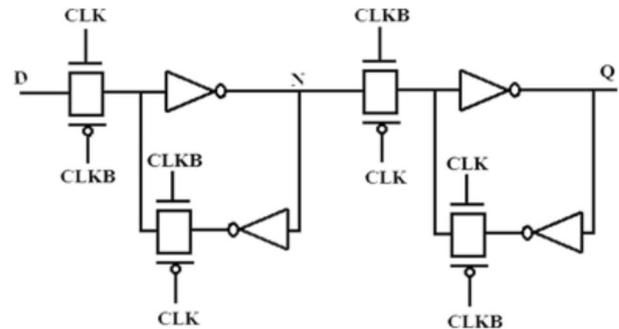


Figure 1: Conventional Transmission Gate Flip-Flop (TGFF)

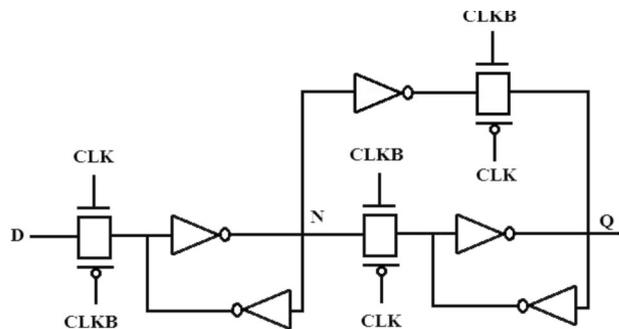


Figure 2: Push Pull Flip-Flop (PPFF)

2.5 Pass Flip-Flop

To save power, the number of transistors of the proposed flip-flop was reduced in [10]. The four transistors in the feedback path of conventional TGFF are replaced by single PMOS transistor. Hence, total 6 transistors are reduced in this flip-flop. This semi-static Pass Flip-Flop (Pass FF) is shown in Figure 3.

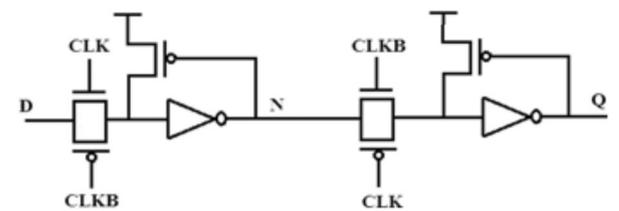


Figure 3: Pass Flip-Flop (Pass FF)

2.6 Pass Isolation Flip-Flop

To activate the feedback path of pass FF only during OFF cycle, a PMOS transistor was added in the feedback in [10]. This semi-static Pass Isolation Flip-Flop (PIFF) is shown in Figure 4. As compare to Pass FF, the number of transistors of this flip-flop is increased by two but this reduces short circuit current during ON cycle. It also improves speed as compare to Pass FF.

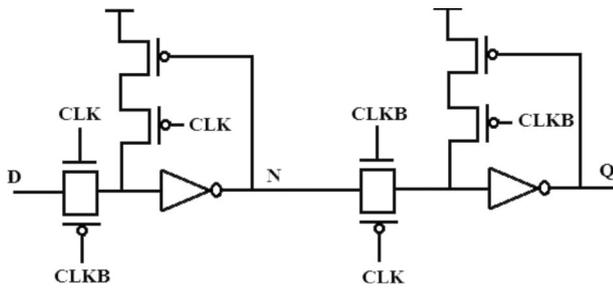


Figure 4: Pass Isolation Flip-Flop (PIFF)

2.2 C²MOS Flip-Flop

Figure 5 shows the static C²MOS Flip-Flop [11]. This flip-flop consists of a C²MOS feedback at the outputs of the master and the slave latches. When clock is at logic 'HIGH', the clocked inverter CLKI1 latches the input D to an intermediate node N. The feedback consisting of clocked inverter CLKI2 and inverter I1 maintains this logic level at node N when clock is at logic level 'HIGH'. Similarly when CLK changes to logic 'LOW', the slave latch gets functional and clocked inverter CLKI3 transfers the logic level from node N to the output Q. The feedback consisting of clocked inverter CLKI4 and inverter I2 maintains this logic level at output node Q when clock is grounded. There are 20 transistors in this circuit, C²MOSFF has largest area but this flip-flop shows the shortest delay and the lowest PDP.

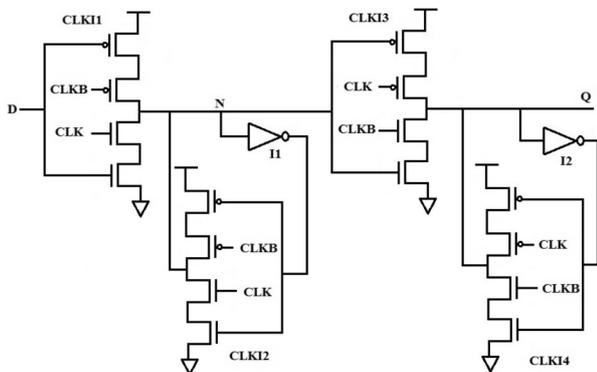


Figure 5: C²MOS Flip-Flop (C²MOS FF)

2.4 High Performance Flip Flop

In High Performance Flip-Flop (HPFF), a feedback is provided from the output node of the slave inverter to a specific internal node in the master-stage as shown in Figure 6. This flip-flop was proposed by [12]. This feedback is provided by only a single transistor. So this has lesser number of transistors as compare to other proposed flip flops discussed in this section. The main advantage of this design is reduced device count and decreased parasitic capacitance at internal nodes of the flip flop which results in improved power-delay product.

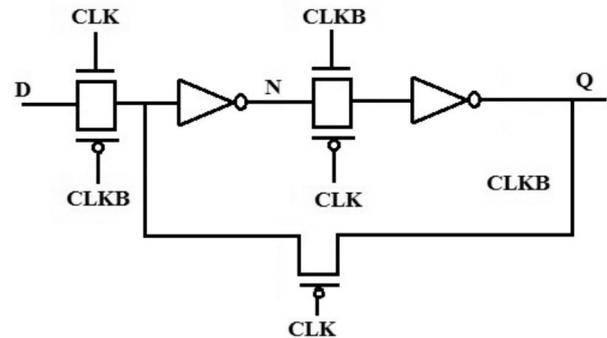


Figure 6: High Performance Flip-Flop (HPFF)

2.3 Area Efficient Flip-Flop

The Area Efficient flip-flop was proposed in [13]. This semi-static flip-flop is illustrated in Figure 7. This flip-flop has lesser transistor count as compared to above discussed flip-flops except HPFF. In this design the feedback circuit of the master section is removed and in slave section, feedback loop consists of a transmission gate. When clock level is 'HIGH', master latch is functional and inverse of the data is stored to an intermediate node N. When clock goes to 'LOW' logic level, the slave latch becomes functional and produces data at the output Q and QB.

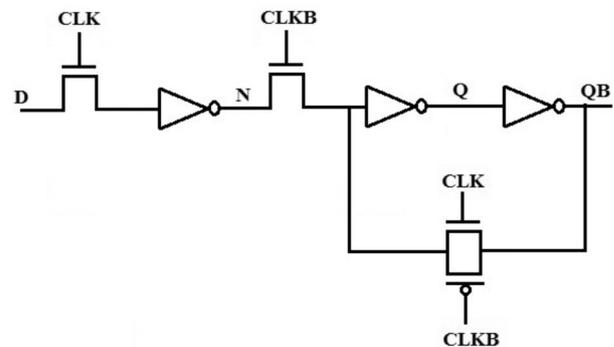


Figure 7: Area Efficient Flip-Flop (Area Efficient FF)

3. Proposed single edge triggered flip-flop

One method to reduce the transistor count is to use an NMOS for latch input. However, since the output of an NMOS can only reach a voltage level of V_{dd} - V_t when it is at logic 1, it results in increased power dissipation [9]. So in the proposed flip-flop (proposed FF), transmission gates are used in both master and slave latches as shown in Figure 8. This reduces the power dissipation.

The feedback path is improved in the proposed flip-flop. Most of the conventional static designs use two

feedback loops one each in the master as well as the slave stage. This increases the total parasitic capacitance at the internal flip-flop nodes, leading to higher dynamic power dissipation and reduced performance. This also results in total chip area overhead due to increased transistor count [12]. In the proposed flip-flop, the feedback circuit of the master section is removed and there is feedback in slave section to make the flip-flop semi-static in nature. This flip-flop is a modification of the pass flip-flop. The feedback PMOS of Pass flip-flop’s master section is removed and in slave section a PMOS transistor with complemented clock signal and an inverter are used to make feedback path functional only during OFF cycle of clock. This reduces short circuit current during ON cycle as compare to pass flip-flop. In the proposed design, device count is reduced and parasitic capacitances at internal nodes of the flip-flop are decreased which results in improved power dissipation. If there is reduction in the number of clocked transistors of design, the clock load capacitance is reduced, leading to low power consumption in the clock distribution network [14]. Thus by reducing the number of clocked transistors, the power dissipation of the proposed design is further reduced.

This flip-flop is negative edge triggered flip-flop. In the proposed FF when clock level is ‘HIGH’, master latch is activated and inverse of the data is stored to an intermediate node N (output of master latch). When clock goes to ‘LOW’ logic level, slave latch becomes functional and produces data at the output Q. This is a low area flip-flop and has the smallest power dissipation with the second lowest PDP.

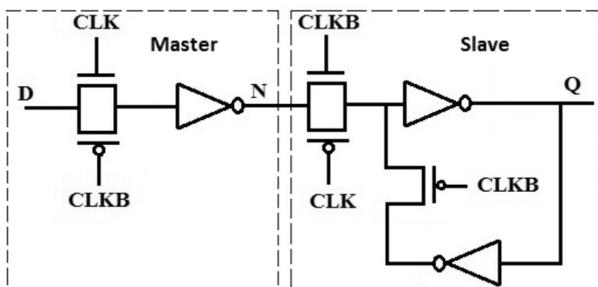


Figure 8: Proposed flip-flop (Proposed FF)

Table 1: CMOS simulation parameters

S. No.	1	2	3	4	5	6	7	8	9	10
Particulars	CMOS Technology	Min. Gate Width	Max. Gate Width	MOSFET Model	Nominal Supply Voltage	Temperature	Duty Cycle	Nominal Clock Frequency	Sequence Length	Rise and Fall Time of Clock & Data
Value	130 nm	260 nm	0.910 μm	BSIM 3v3 level 53	1.3 V	25° C	50 %	400 MHz	16 Data Cycles	100 ps

4. Simulation

Simulation parameters used for comparison, are shown in table 1. Under nominal condition, a 16-cycle sequence (1111010110010000) with an activity factor of 18.75% is supplied at the input for average power measurements. Power consumption based on this data sequence of 18.75% was considered as the real parameter for characterizing power dissipation of a flip-flop design. The dynamic power consumption is dependent on switching activities at various nodes of the circuit. It varies with different data rates and circuit topologies. Hence to obtain a fair idea of power dissipation for a circuit topology, different data patterns should be applied with different activity rates [15]. So in simulations, following five different data sequences have been adopted to compare the power consumption of flip-flop structures discussed in this paper:

- i) 1111111111111111 (A=0)
- ii) 0000000000000000 (A=0)
- iii) 1111010110010000 (A=0.18)
- iv) 1100110011001100 (A=0.5)
- v) 1010101010101010 (A=1)

Where “A” is the data activity. The results are carried out for the period of 16 data sequences. All simulations are performed on TSpice using BSIM 3v3 level 53 models in 130 nm process node. The supply voltage is varied from 1 V to 2 V and the clock frequency is varied from 100 MHz to 1 GHz.

4.1 Analysis

Various parameters of the flip-flops can be compared. In general, a PDP-based comparison is appropriate for low power portable systems in which battery life is the primary index of energy efficiency [16]. In this paper, our main interest is in SETFF usage for low-power applications. Therefore power consumption is selected for comparing different flip-flops. Additionally delay and PDP are also compared of the discussed flip flops.

4.2 Optimization

There is always a tradeoff between power dissipation and propagation delay of a circuit. A flip-flop can be optimized for either high performance or low power,

but both the parameters are critical. In this work, the designs are simulated to achieve minimum power dissipation. Transistor count is also included to maintain a fair level of comparison. The transistors, that are not located on critical path, are implemented with minimum size to reduce area overhead and to minimize power dissipation.

5. Result and discussion

Figure 9 and Figure 10 indicate the power consumption in microwatts at different supply voltages for 18.75% data activity and 400 MHz clock frequency. These figures show that power increases with increase in supply voltage because all three types of power (i.e. switching power, short circuit power and leakage power) depend on supply voltage and the switching power is proportional to the square of the supply voltage. Approximately 90% power dissipation in CMOS logic is due to the dynamic (switching) power [17]. So power dissipation rapidly reduces with reduction in the supply voltage. Table 2 indicates the power consumption in microwatts at different supply voltages for 18.75% data activity and 400 MHz clock frequency. The simulation results indicate that the proposed FF has the least average power dissipation among all the designs for all supply voltages. For fair comparison, the average of power consumption at all voltages is taken except 1 V, because at 1 V two previously proposed flip-flops failed. This result shows that the proposed FF has 41.25%, 34.91%, 46.51%, 43.65%, 28.02% and 70.22% improvement in average power consumption when compared to the previously proposed flip-flops discussed in section 2 respectively. Proposed FF has up to 70.22% improvement in average power consumption. Among previously proposed flip-flops discussed in section 2, HPFF shows the lowest power consumption for all supply voltages. PPFF and Area efficient FF failed at 1 V. Area efficient FF shows the worst power consumption for all voltages.

Figure 11 shows, all flip-flops consume the largest power at 1 GHz clock frequency and the smallest power at

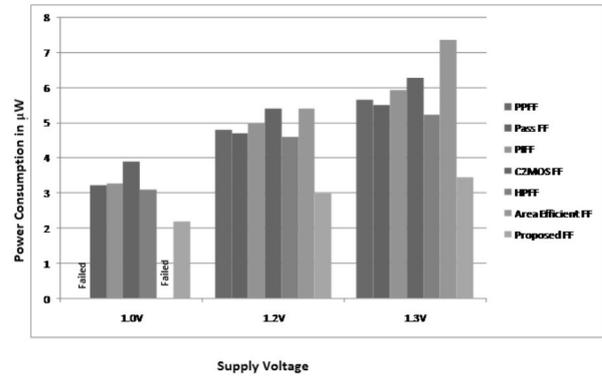


Figure 9: Power consumption as a function of supply voltage for 1.0 V, 1.2 V and 1.3 V

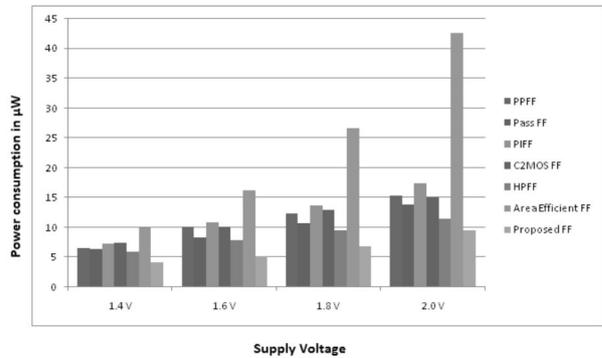


Figure 10: Power consumption as a function of supply voltage for 1.4 V, 1.6 V, 1.8 V and 2.0 V

100 MHz clock frequency. As clock frequency increases, power consumption increases. Table 3 shows power consumption in microwatts as a function of clock frequency. Table shows that for all clock frequencies, the proposed FF has the better power consumption than all the existing flip-flops discussed in section 2. For fair comparison, the average of power consumption at all clock frequencies is taken. This average result shows that the proposed FF has 39.42%, 38.97%, 44.39%, 44.85%, 33.60% and 53.37% improvement in average power consumption when compared to the previously proposed flip-flops discussed in section 2 respectively. Table 3 shows that the proposed FF has up to 53.37% improvement in average power consumption.

Table 2: Power consumption in µW as a function of supply voltage

VDD (V)	PPFF	Pass FF	PIFF	C2MOS FF	HPFF	Area Efficient FF	Proposed FF
1.0	Failed	3.23	3.28	3.9	3.1	Failed	2.2
1.2	4.8	4.7	4.97	5.4	4.6	5.41	3.0
1.3	5.65	5.52	5.94	6.30	5.24	7.38	3.44
1.4	6.5	6.4	7.34	7.4	6.0	10	4.1
1.6	10.1	8.4	10.90	10.1	7.9	16.2	5.2
1.8	12.4	10.7	13.64	12.9	9.5	26.6	6.9
2.0	15.4	13.8	17.42	15.1	11.5	42.6	9.6
Average excluding 1 V	9.14	8.25	10.04	9.53	7.46	18.03	5.37

Table 3: Power consumption in μW as a function of clock frequency

CLOCK (MHz)	PPFF	Pass FF	PIFF	C2MOS FF	HPFF	Area Efficient FF	Proposed FF
100	3.5	3.1	3.63	3.0	2.50	4.7	1.7
200	4.2	4.0	5.01	4.0	3.30	5.5	2.2
250	4.5	4.2	4.25	4.4	3.80	5.9	2.4
400	5.7	5.5	5.94	6.3	5.20	7.4	3.4
10000	9.5	10.4	11.00	12.4	10.20	12.1	6.9
Average	5.48	5.44	5.97	6.02	5.00	7.12	3.32

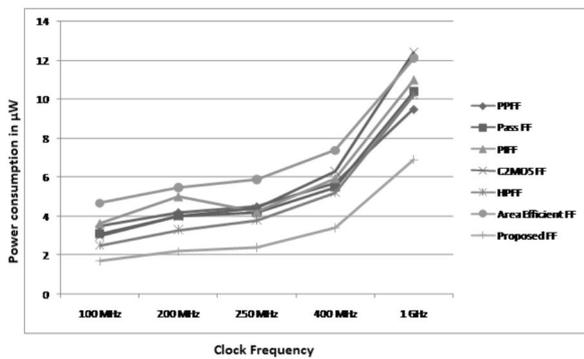


Figure 11: Power consumption as a function of clock frequency

Among previously proposed flip-flops discussed in section 2, HPFF shows better power consumption at all clock frequencies except 1 GHz, at this frequency PPFF shows the better power consumption. Area efficient FF has the highest power consumption for all clock frequencies except 1 GHz. As clock frequency is increased, power consumption of C²MOSFF increases and near 1 GHz clock frequency C²MOSFF consumes the highest power.

Figure 12 shows, 100% data activity exhibits the largest power consumption and 0% data activity exhibits the smallest power consumption. For all switching activities, the proposed flip-flop shows better power dissipation than all the discussed previously proposed flip-flops. Power Consumption in μW as a function of data activity is shown in Table 4. For fair comparison, the average of power consumption at all data activities is taken.

Table 4: Power consumption in μW as a function of data activity

Data Activity	PPFF	Pass FF	PIFF	C ² MOS FF	HPFF	Area Efficient FF	Proposed FF
0% (all 1's)	3.3	3.6	3.80	4.3	4.00	6.2	2.5
0% (all 0's)	3.2	3.5	3.64	4.8	4.00	3.5	2.4
18.75%	5.7	5.5	5.94	6.3	5.24	7.4	3.4
50%	5.7	5.7	6.13	6.3	5.20	7.5	3.4
100%	8.4	7.9	8.22	8.4	6.60	9.7	4.4
Average	5.26	5.24	5.55	6.02	5.01	6.86	3.22

en. This average result shows that the proposed FF has 38.78%, 38.55%, 41.98%, 46.51%, 35.73% and 53.06% improvement in average power consumption when compared to the previously proposed flip-flops discussed in section 2 respectively. Proposed FF has up to 53.06% improvement in average power consumption. Area Efficient FF consumes the highest power for all switching activity except zero switching activity (when all are 0's). For this zero switching activity (when all are 0's), C²MOSFF consumes the highest power. Among previously proposed flip-flops discussed in section 2, HPFF shows better power consumption at all data activities except 0% switching activity (when all are 0's or all are 1's), for 0% switching activity PPFF exhibits better power dissipation.

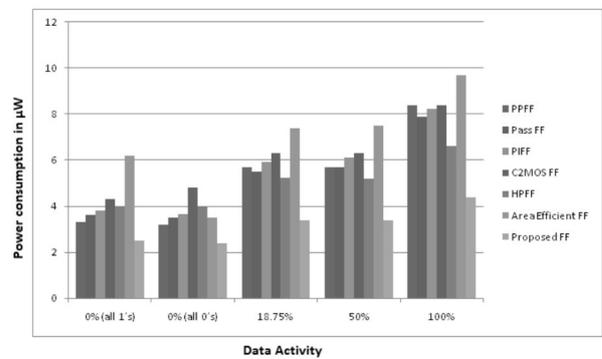


Figure 12: Power consumption dependence on data activity rates

Table 5 shows average clock to output (C_Q) delay in ps at different supply voltages for 18.75% data activ-

Table 5: Average clock to Q delay in pS

VDD (V)	PPFF	Pass FF	PIFF	C ² MOS FF	HPFF	Area Efficient FF	Proposed FF
1.0	Failed	238.15	166.35	106.9	247.65	Failed	172
1.2	137.85	133.6	126.65	41.35	119.95	593.2	86.6
1.3	99.99	79.77	63.78	25.61	74.31	293.43	39.47
1.4	116.4	103.55	43.52	18.25	56.35	193.65	72.75
1.6	132.4	100.3	9.90	13.35	41.25	98.25	6.65
1.8	111.75	81.3	78.61	11.55	34.05	58.4	46.35
2.0	95.3	66.15	69.54	10.3	30.3	43.75	43.25
Average excluding 1 V	115.62	94.11	65.33	20.07	59.37	213.45	49.18

ity and 400 MHz clock frequency. The simulation results indicate that the proposed FF has the lowest delay among all the designs for 1.6 V supply voltage and the second lowest delay for 1.2 V and 1.3 V. For fair comparison, the average of delay at all voltages is taken. This result shows that the proposed FF has 57.46%, 47.74%, 24.72%, 17.16% and 76.96% improvement in average delay when compared to the previously proposed flip-flops discussed in section 2 respectively except C²MOS-FF. The proposed FF has up to 76.96% improvement in average delay and has the second lowest delay.

C²MOSFF shows 59.19% lesser average delay when compared to proposed FF. C²MOSFF shows the lowest delay for all supply voltages except 1.6 V, at this voltage proposed FF shows the lowest delay.

PIFF shows the second lowest delay for 1 V, 1.4 V and 1.6 V. For 1 V HPFF exhibits the longest delay. As supply voltage increases, delay of HPFF decreases as compared to other flip-flops and for 1.8 V, 2 V this flip-flop shows the second lowest delay. For 1.2 V, 1.3 V and 1.4 V Area Efficient FF shows the highest delay but as the supply voltage increases its delay improves. As supply voltage increases, delay of PPFF increases as compared to other flip-flops and for 1.6 V, 1.8 V, 2 V this flip-flop shows the worst delay. Overall Area Efficient FF has the worst delay and C²MOSFF has the smallest delay.

Table 6: PDP_{C_Q} as a function of supply voltage

VDD (V)	PPFF 10-18J	Pass FF 10-18J	PIFF 10-18J	C2MOS FF 10-18J	HPFF 10-18J	Area Efficient FF	Proposed FF 10-18J
1.0	Failed	769.22	545.63	416.91	767.72	Failed	378.40
1.2	661.68	627.92	629.45	223.30	551.77	3209.21	259.80
1.3	564.94	440.33	378.85	161.34	389.38	2165.51	135.78
1.4	756.60	662.72	319.44	135.10	338.10	1936.50	298.27
1.6	1337.24	842.52	107.91	134.84	325.88	1591.65	34.58
1.8	1385.70	869.91	1072.24	149.00	323.48	1553.44	319.81
2.0	1467.62	912.87	1211.39	155.53	348.45	1863.75	415.20
Average excluding 1V	1028.96	726.05	619.88	159.85	379.51	2053.34	243.91

Figure 13 and Figure 14 show the clock to Q PDP for discussed flip-flops as a function of supply voltage. These figures show that for 1 V, 1.3 V, 1.6 V proposed FF shows the lowest PDP while for 1.2 V, 1.4 V, 1.8 V it shows the second lowest PDP. Table 6 shows the clock to Q PDP as a function of supply voltage. For fair comparison, the average of PDP at all voltages is taken except 1 V, because at 1 V two existing flip-flops failed. This average result shows that the proposed FF has 76.30%, 66.41%, 60.65%, 35.73% and 88.12% improvement in PDP when compared to the previously proposed flip-flops discussed in section 2 respectively except C²MOSFF, it has 34.46% better PDP than the proposed FF. The proposed FF has up to 88.12% improvement in PDP. For 1.2 V, 1.4 V, 1.8 V and 2 V C²MOSFF shows the lowest PDP while for 1 V and 1.3 V this flip-flop shows the second lowest PDP. At 1.6 V PIFF shows the second lowest PDP. PPFF and Area Efficient FF failed at 1 V. For 1 V, Pass FF has the worst PDP and for all other voltages Area Efficient FF has the worst PDP. Overall Figure 13 and Figure 14 show that C²MOSFF and proposed FF has the lowest and second lowest PDP respectively while Area efficient FF shows the worst PDP.

Table 7 illustrates the transistor count for the various flip-flop designs discussed in this paper (excluding the inverter to generate the complementary clock signals). The proposed FF has eleven transistors and five clocked transistors. Proposed FF has one more transis-

Table 7: Transistor count of discussed flip-flops

Flip Flop	PPFF	Pass FF	PIFF	C ² MOS FF	HPFF	Area Efficient FF	Proposed FF
No of transistor	16	10	12	20	9	10	11
No of clocked transistor	6	4	6	8	5	4	5

tors than Pass FF, Area efficient FF and two more transistors than HPFF but table 2 shows that the proposed FF has 34.91%, 70.22%, 28.02% improvement in average power consumption, table 5 shows that the proposed FF has 47.74%, 76.96%, 17.16% improvement in average delay and table 6 shows that the proposed FF has 66.41%, 88.12%, 35.73% improvement in PDP over these flip-flops respectively. It is further seen that C²MOSFF occupies the largest silicon area but it shows the smallest delay and the smallest PDP. PPFF has the second largest transistor count.

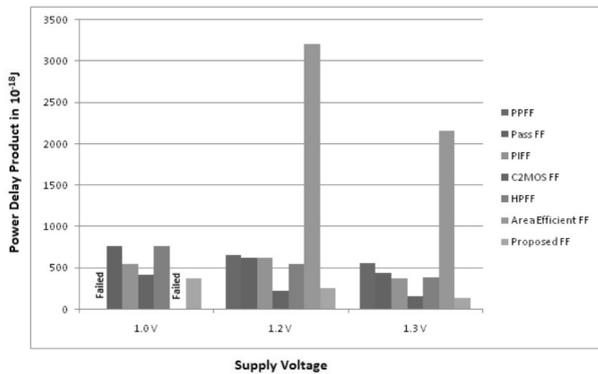


Figure 13: PDP dependence on supply voltage for 1.0 V, 1.2 V and 1.3 V

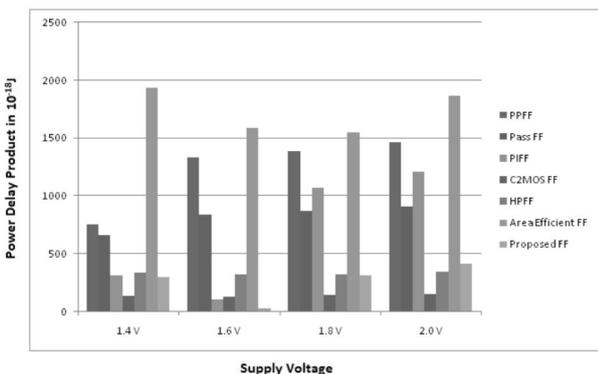


Figure 14: PDP dependence on supply voltage for 1.4 V, 1.6 V, 1.8 V and 2.0 V

6. Conclusion

A comparative analysis of single input single edge triggered flip-flops has been done. Among previously proposed flip-flops discussed in section 2, HPFF shows the lowest power consumption for all supply voltages and for all clock frequencies except 1 GHz, at this frequency

PPFF shows the better power consumption. PPFF and Area efficient FF failed at 1 V. Area efficient FF shows the worst power consumption for all voltages and for all clock frequencies except 1 GHz. As clock frequency is increased, power consumption of C²MOSFF increases and near 1 GHz clock frequency C²MOSFF consumes the highest power. Area Efficient FF consumes the highest power for all switching activity except zero switching activity (when all are 0's), for this activity C²MOSFF consumes the highest power. Among previously proposed flip-flops discussed in section 2, HPFF shows better power consumption at all data activities except 0% switching activity (when all are 0's or all are 1's), for this 0% switching activity PPFF exhibits better power dissipation. For low supply voltages Area Efficient FF shows the highest delay but as the supply voltage increases its delay improves, while the delay of PPFF increases with increment of supply voltage as compared to other flip-flops. Area Efficient FF has the worst delay and C²MOSFF has the smallest delay. C²MOSFF has the lowest PDP and this flip-flop has 34.46% better PDP than the proposed FF while Area efficient FF shows the worst PDP. It is further seen that C²MOSFF has largest transistor count but C²MOSFF shows the shortest delay and the lowest PDP. Area efficient FF has only ten transistors but this flip-flop has the highest power consumption, the highest delay and the worst PDP. So the Area efficient FF is not suited for low power or high performance applications.

The new flip-flop structure has been proposed in this paper. The proposed flip-flop structure is compared on the basis of power, delay, PDP and transistor count with the existing flip-flop structures. For all supply voltages, all clock frequencies and all data activities, the proposed FF has better power consumption than all the existing flip-flops discussed in section 2 and proposed FF has up to 70.22% improvement in average power consumption. The simulation results indicate that the proposed FF has the lesser delay than all the existing flip-flop designs discussed in section 2 except C²MOSFF. Proposed FF has up to 76.96% improvement in average delay but C²MOSFF shows 59.19% lesser average delay when compared to the proposed FF. The proposed FF has better PDP than all the existing flip-flop designs discussed in section 2 except C²MOSFF. The proposed FF has up to 88.12% improvement in PDP, C²MOSFF has 34.46% better PDP than the proposed FF. However C²MOSFF uses nine more transistors than the proposed

FF, so proposed FF has lesser area, cost and power as compare to the C²MOSFF.

Among all flip-flops compared, the proposed FF is found to be the best energy efficient having the second lowest PDP and the second shortest delay. The proposed FF has up to 70.22% improvement in average power dissipation, up to 76.96% improvement in delay and up to 88.12% improvement in PDP. So, proposed FF is best suited for low power and high performance applications.

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